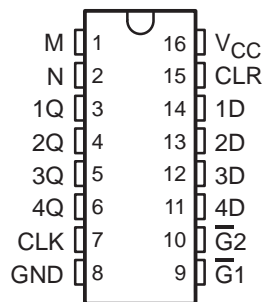


# SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

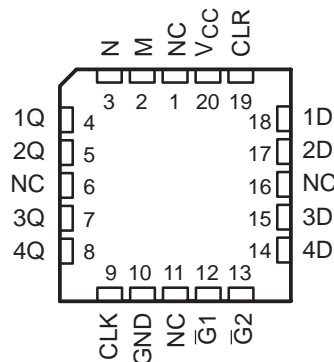
SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

- 3-State Outputs Interface Directly With System Bus
- Gated Output-Control Lines for Enabling or Disabling the Outputs
- Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes:
  - Parallel Load
  - Do Nothing (Hold)
- For Application as Bus Buffer Registers
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

SN54173, SN54LS173A . . . J OR W PACKAGE  
SN74173 . . . N PACKAGE  
SN74LS173A . . . D or N PACKAGE  
(TOP VIEW)



SN54LS173A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

TYPE	TYPICAL PROPAGATION DELAY TIME	MAXIMUM CLOCK FREQUENCY
'173	23 ns	35 MHz
'LS173A	18 ns	50 MHz

## description

The '173 and 'LS173A 4-bit registers include D-type flip-flops featuring totem-pole 3-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these flip-flops with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. Up to 128 of the SN74173 or SN74LS173A outputs can be connected to a common bus and still drive two Series 54/74 or 54LS/74LS TTL normalized loads, respectively. Similarly, up to 49 of the SN54173 or SN54LS173A outputs can be connected to a common bus and drive one additional Series 54/74 or 54LS/74LS TTL normalized load, respectively. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Gated enable inputs are provided on these devices for controlling the entry of data into the flip-flops. When both data-enable ( $\overline{G1}$ ,  $\overline{G2}$ ) inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output-control (M, N) inputs also are provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output-control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

The SN54173 and SN54LS173A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74173 and SN74LS173A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54173, SN54LS173A, SN74173, SN74LS173A

## 4-BIT D-TYPE REGISTERS

### WITH 3-STATE OUTPUTS

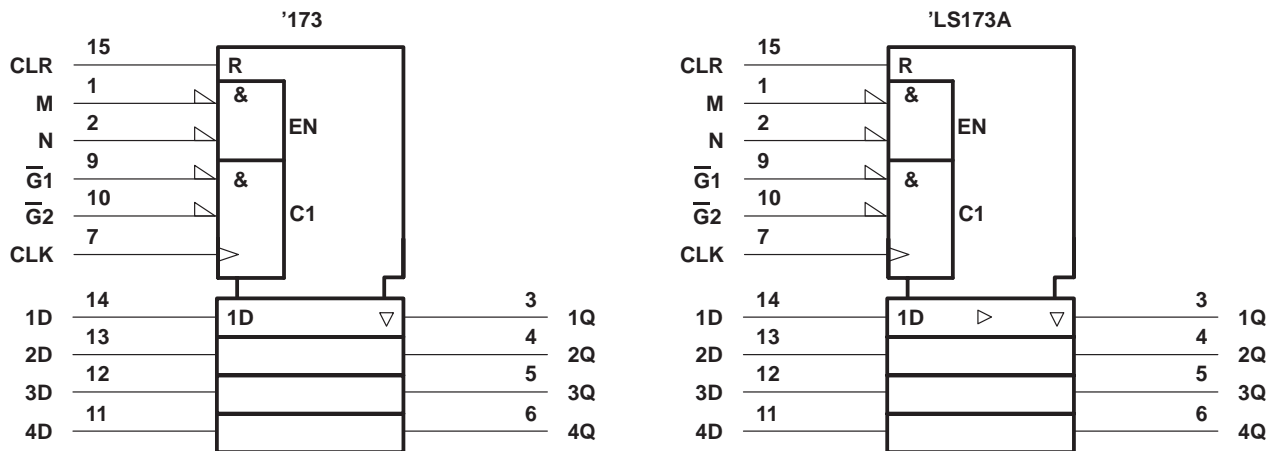
SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

FUNCTION TABLE

		INPUTS			OUTPUT Q
CLR	CLK	DATA ENABLE		DATA D	
		$\overline{G1}$	$\overline{G2}$		
H	X	X	X	X	L
L	L	X	X	X	$Q_0$
L	$\uparrow$	H	X	X	$Q_0$
L	$\uparrow$	X	H	X	$Q_0$
L	$\uparrow$	L	L	L	L
L	$\uparrow$	L	L	H	H

When either M or N (or both) is (are) high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

### logic symbol†

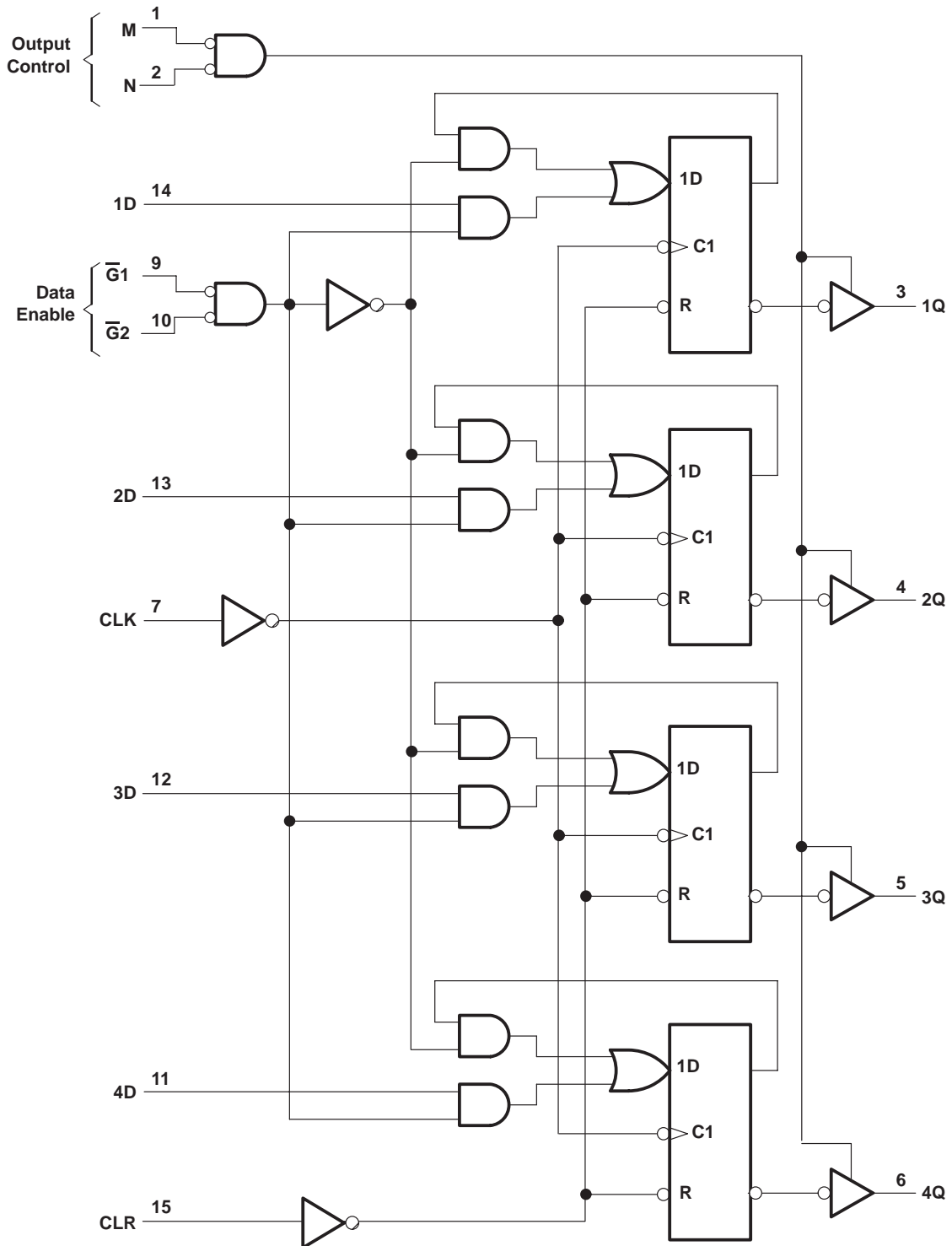


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

SN54173, SN54LS173A, SN74173, SN74LS173A  
**4-BIT D-TYPE REGISTERS  
 WITH 3-STATE OUTPUTS**

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

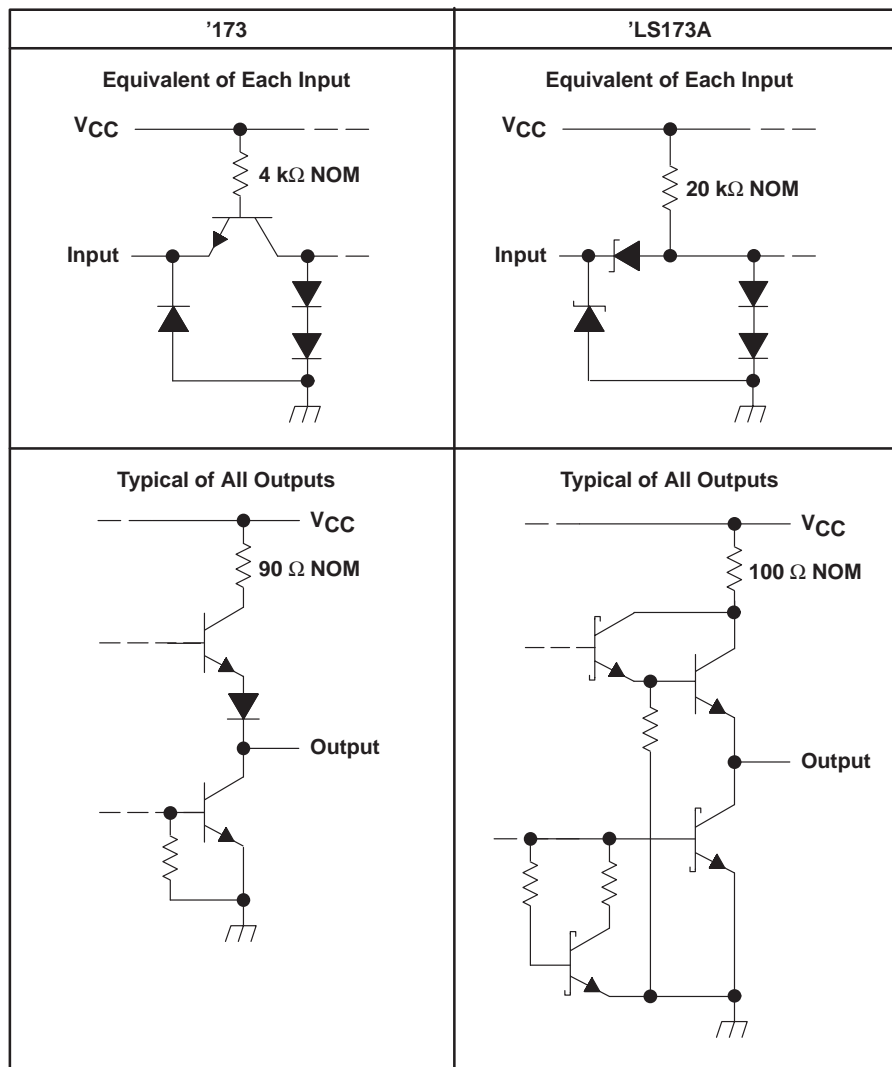
# SN54173, SN54LS173A, SN74173, SN74LS173A

## 4-BIT D-TYPE REGISTERS

### WITH 3-STATE OUTPUTS

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

#### schematics of inputs and outputs



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	–0.5 V to 7 V
Input voltage: '173	–0.5 V to 5.5 V
'LS173A	–0.5 V to 7 V
Off-state output voltage	–0.5 V to 5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	113°C/W
N package	78°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

## recommended operating conditions (see Note 3)

		SN54173			SN74173			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I <sub>OH</sub>	High-level output current			-2			-5.2	mA
I <sub>OL</sub>	Low-level output current			16			16	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54173			SN74173			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V <sub>IH</sub>	High-level input voltage	2			2			V	
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA		-1.5			-1.5	V	
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, V <sub>IH</sub> = 2 V, I <sub>OH</sub> = MAX		2.4			2.4	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA					0.4	V	
I <sub>O(off)</sub>	Off-state (high-impedance state) output current	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V		V <sub>O</sub> = 2.4 V		40		μA	
				V <sub>O</sub> = 0.4 V		-40			
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		1			1	mA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V		40			40	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-1.6			-1.6	mA	
I <sub>OS</sub>	Short-circuit output current§	V <sub>CC</sub> = MAX		-30			-70	mA	
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX, See Note 4		50	72		50	72	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 4: I<sub>CC</sub> is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N,  $\overline{G1}$ ,  $\overline{G2}$ , and all data inputs grounded; and CLK and M at 4.5 V.

## timing requirements over recommended operating conditions (unless otherwise noted)

		SN54173		SN74173		UNIT
		MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Input clock frequency		25		25	MHz
t <sub>w</sub>	Pulse duration	CLK or CLR		20	20	ns
t <sub>su</sub>	Setup time	Data enable ( $\overline{G1}$ , $\overline{G2}$ )		17	17	ns
		Data		10	10	
		CLR (inactive state)		10	10	
t <sub>h</sub>	Hold time	Data enable ( $\overline{G1}$ , $\overline{G2}$ )		2	2	ns
		Data		10	10	



**SN54173, SN54LS173A, SN74173, SN74LS173A**  
**4-BIT D-TYPE REGISTERS**  
**WITH 3-STATE OUTPUTS**

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 400\ \Omega$  (see Figure 1)**

PARAMETER	TEST CONDITIONS	SN54173			SN74173			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$f_{max}$	Maximum clock frequency	25	35		25	35		MHz
$t_{PHL}$	Propagation delay time, high-to-low-level output from clear input		18	27		18	27	ns
$t_{PLH}$	Propagation delay time, low-to-high-level output from clock input		28	43		28	43	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from clock input		19	31		19	31	
$t_{PZH}$	Output enable time to high level	7	16	30	7	16	30	ns
$t_{PZL}$	Output enable time to low level	7	21	30	7	21	30	
$t_{PHZ}$	Output disable time from high level	3	5	14	3	5	14	ns
$t_{PLZ}$	Output disable time from low level	3	11	20	3	11	20	



# SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

## recommended operating conditions

		SN54LS173A			SN74LS173A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I <sub>OH</sub>	High-level output current			-1			-2.6	mA
I <sub>OL</sub>	Low-level output current			12			24	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS173A			SN74LS173A			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT	
V <sub>IH</sub>	High-level input voltage	2			2			V	
V <sub>IL</sub>	Low-level input voltage	0.7			0.8			V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			V	
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>ILmax</sub> , I <sub>OH</sub> = MAX			2.4 3.4			V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 12 mA		0.25 0.4		0.25 0.4		V	
		I <sub>OL</sub> = 24 mA				0.35 0.5		V	
I <sub>O(off)</sub>	Off-state (high-impedance state) output current	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 2.7 V		20		20		V	
		V <sub>O</sub> = 0.4 V		-20		-20			
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1			mA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20			μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4			mA	
I <sub>OS</sub>	Short-circuit output current§	V <sub>CC</sub> = MAX			-30 -130		-30 -130		mA
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX, See Note 4			19 30		19 24		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 4: I<sub>CC</sub> is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N,  $\overline{G1}$ ,  $\overline{G2}$ , and all data inputs grounded; and CLK and M at 4.5 V.

## timing requirements over recommended operating conditions (unless otherwise noted)

		SN54LS173A		SN74LS173A		UNIT
		MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Input clock frequency	30		25		MHz
t <sub>w</sub>	Pulse duration	CLK or CLR		25		ns
t <sub>su</sub>	Setup time	Data enable ( $\overline{G1}$ , $\overline{G2}$ )		35		ns
		Data		17		
		CLR (inactive state)		10		
t <sub>h</sub>	Hold time	Data enable ( $\overline{G1}$ , $\overline{G2}$ )		0		ns
		Data		3		



**SN54173, SN54LS173A, SN74173, SN74LS173A**  
**4-BIT D-TYPE REGISTERS**  
**WITH 3-STATE OUTPUTS**

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

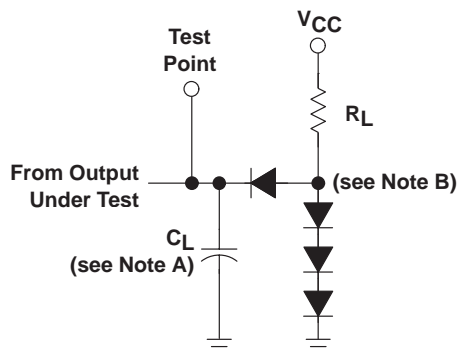
**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 667\ \Omega$  (see Figure 2)**

PARAMETER	TEST CONDITIONS	SN54LS173A			SN74LS173A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$f_{max}$	Maximum clock frequency	30	50		30	50		MHz
$t_{PHL}$	Propagation delay time, high-to-low-level output from clear input		26	35		26	35	ns
$t_{PLH}$	Propagation delay time, low-to-high-level output from clock input		17	25		17	25	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from clock input		22	30		22	30	
$t_{PZH}$	Output enable time to high level		15	23		15	23	ns
$t_{PZL}$	Output enable time to low level		18	27		18	27	
$t_{PHZ}$	Output disable time from high level		11	20		11	20	ns
$t_{PLZ}$	Output disable time from low level		11	17		11	17	

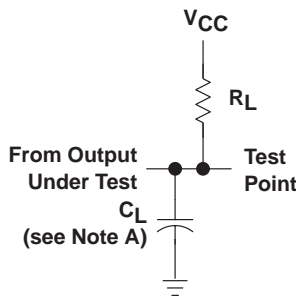




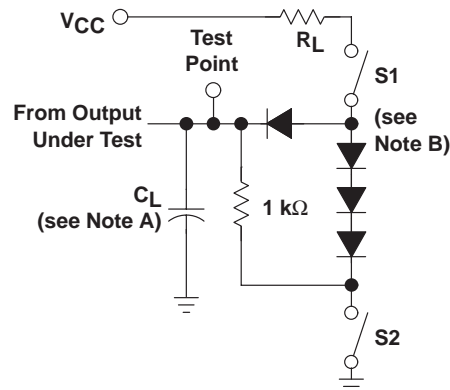
PARAMETER MEASUREMENT INFORMATION  
SERIES 54/74 AND 54S/74S DEVICES



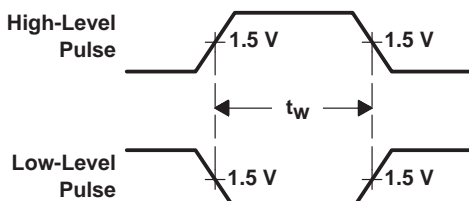
LOAD CIRCUIT  
FOR 2-STATE TOTEM-POLE OUTPUTS



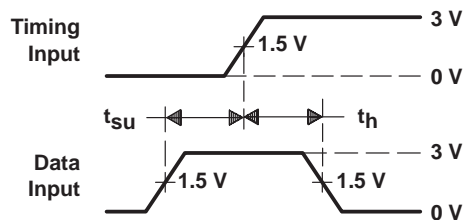
LOAD CIRCUIT  
FOR OPEN-COLLECTOR OUTPUTS



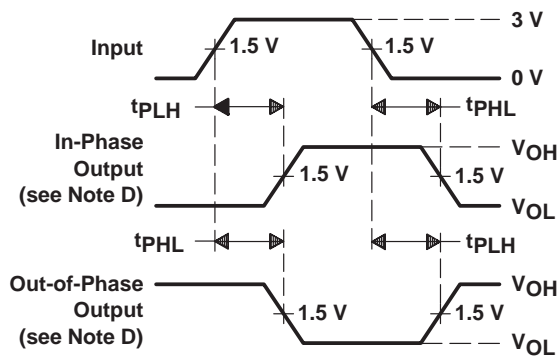
LOAD CIRCUIT  
FOR 3-STATE OUTPUTS



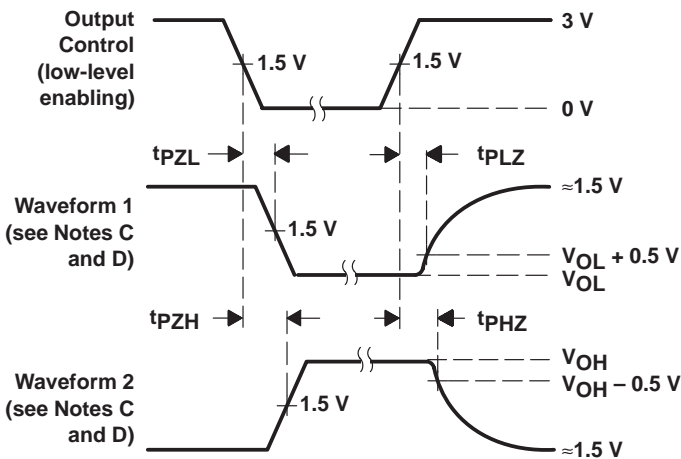
VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

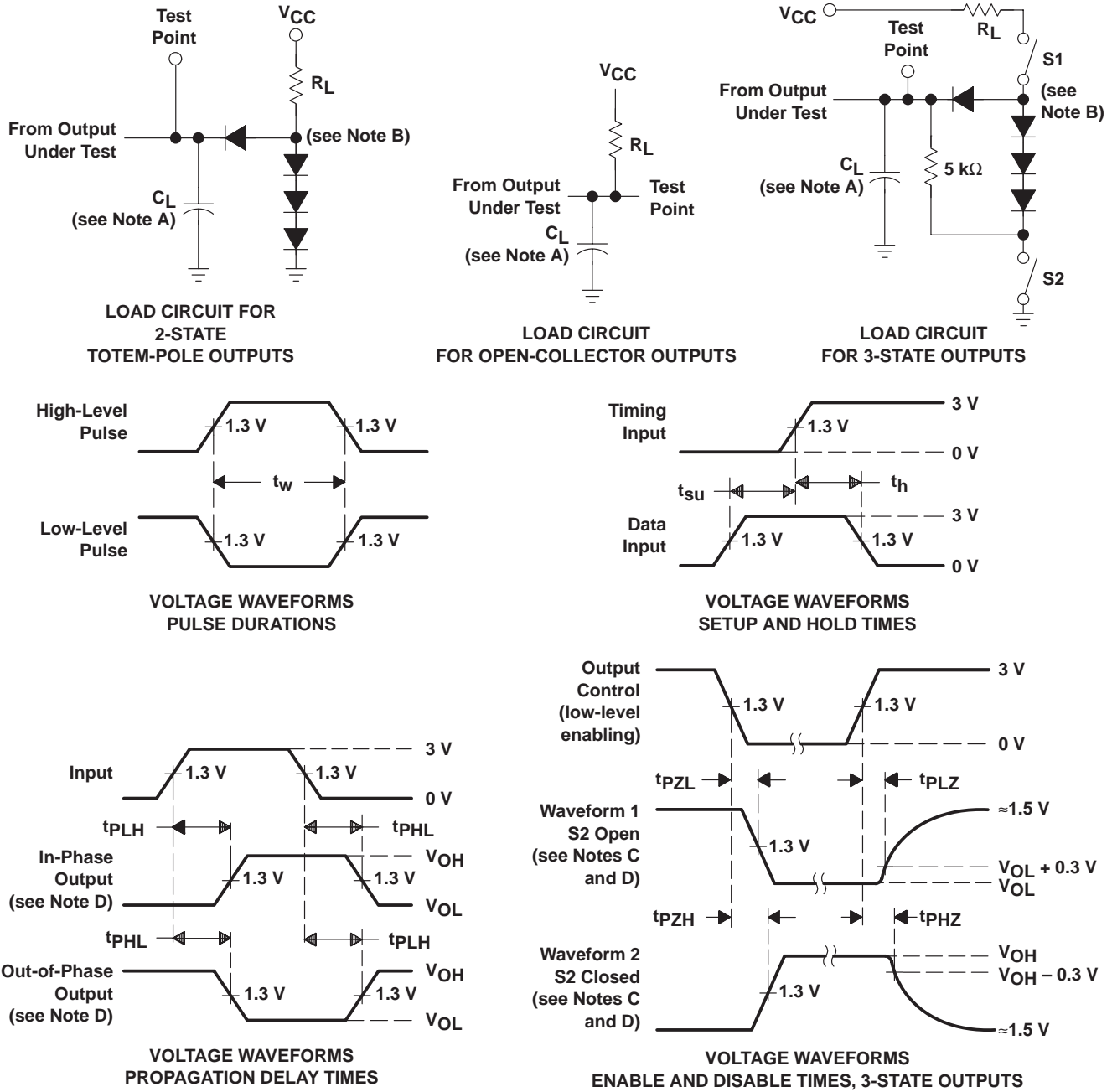
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All diodes are 1N3064 or equivalent.  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ .  
E. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O \approx 50 \Omega$ ,  $t_r$  and  $t_f \leq 7$  ns for Series 54/74 devices and  $t_r$  and  $t_f \leq 2.5$  ns for Series 54S/74S devices.  
F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**SN54173, SN54LS173A, SN74173, SN74LS173A**  
**4-BIT D-TYPE REGISTERS**  
**WITH 3-STATE OUTPUTS**

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54LS/74LS DEVICES**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All diodes are 1N3064 or equivalent.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ .  
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.  
 F. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O \approx 50 \Omega$ ,  $t_r \leq 15$  ns,  $t_f \leq 6$  ns.  
 G. The outputs are measured one at a time with one input transition per measurement.

**Figure 2. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">JM38510/36101BEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 36101BEA
JM38510/36101BEA.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 36101BEA
<a href="#">JM38510/36101BFA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 36101BFA
JM38510/36101BFA.A	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 36101BFA
<a href="#">M38510/36101BEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 36101BEA
<a href="#">M38510/36101BFA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 36101BFA
<a href="#">SN54173J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54173J
SN54173J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54173J
<a href="#">SN54LS173AJ</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS173AJ
SN54LS173AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS173AJ
<a href="#">SN74LS173AD</a>	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS173A
SN74LS173AD.A	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS173A
<a href="#">SN74LS173AN</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS173AN
SN74LS173AN.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS173AN
<a href="#">SNJ54173J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54173J
SNJ54173J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54173J
<a href="#">SNJ54LS173AFK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 173AFK
SNJ54LS173AFK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 173AFK
<a href="#">SNJ54LS173AJ</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS173AJ
SNJ54LS173AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS173AJ

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

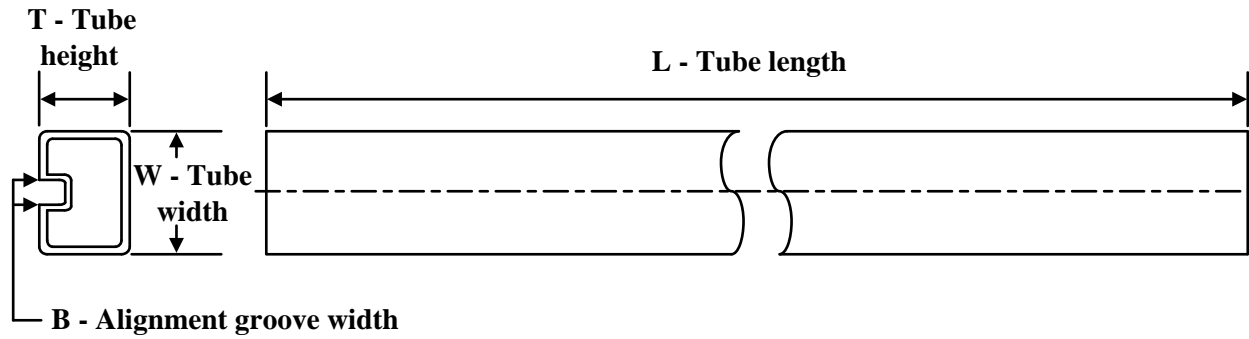
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS173A, SN74LS173A :**

- Catalog : [SN74LS173A](#)
- Military : [SN54LS173A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TUBE**


\*All dimensions are nominal



Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JM38510/36101BFA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/36101BFA.A	W	CFP	16	25	506.98	26.16	6220	NA
M38510/36101BFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LS173AD	D	SOIC	16	40	507	8	3940	4.32
SN74LS173AD.A	D	SOIC	16	40	507	8	3940	4.32
SN74LS173AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS173AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS173AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS173AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS173AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS173AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

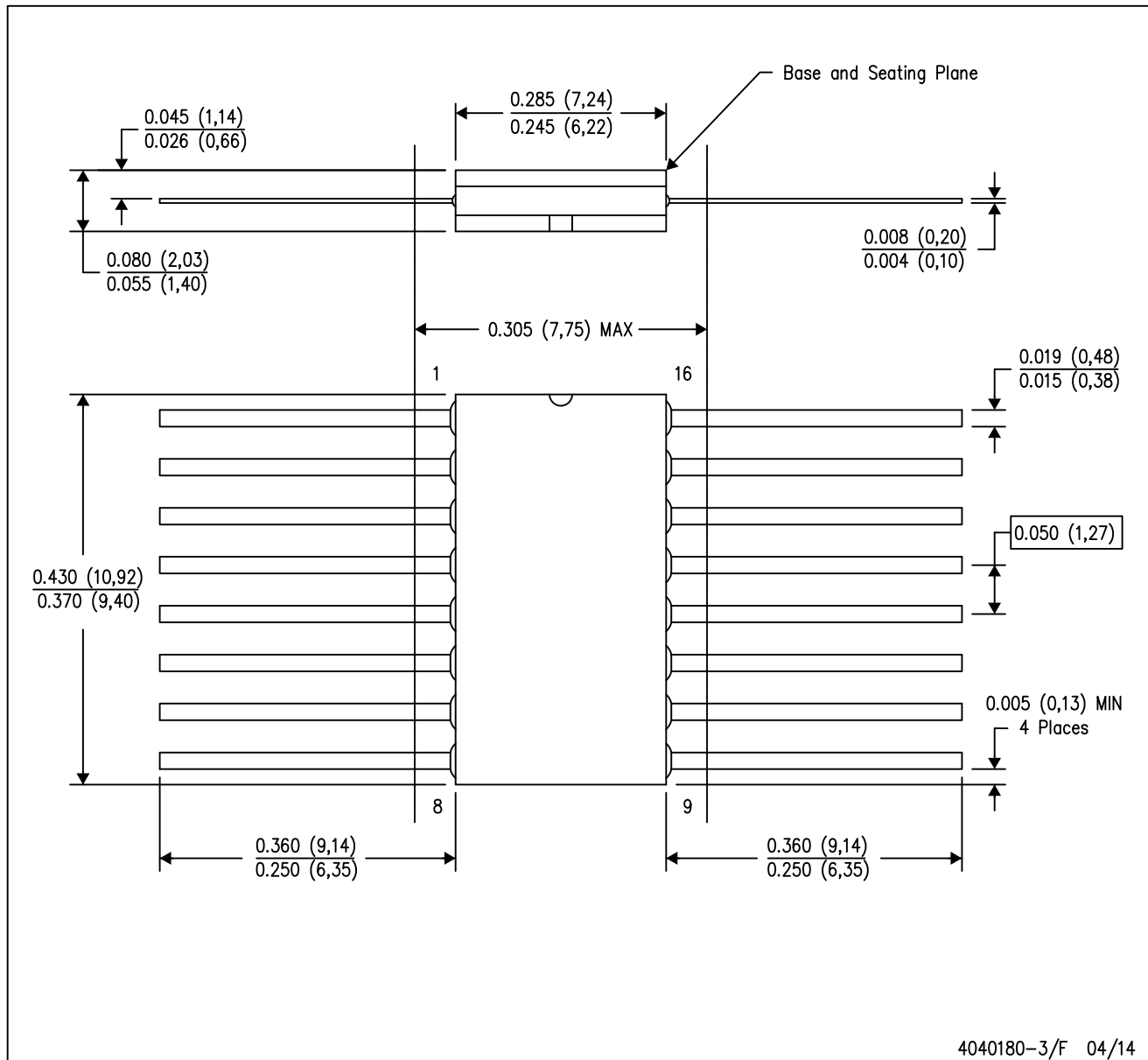


4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

## GENERIC PACKAGE VIEW

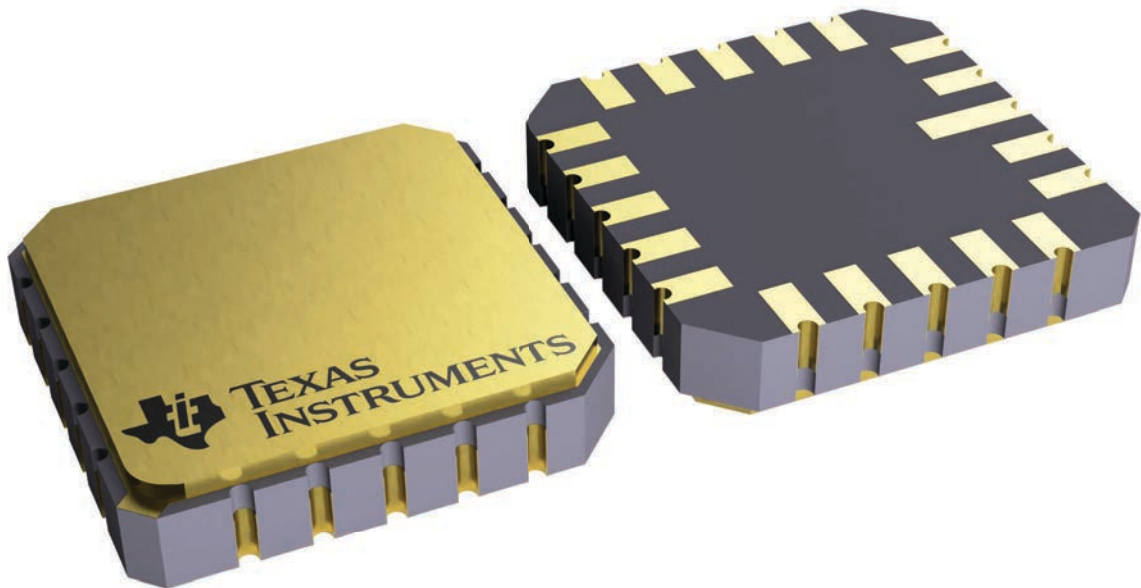
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\



J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025