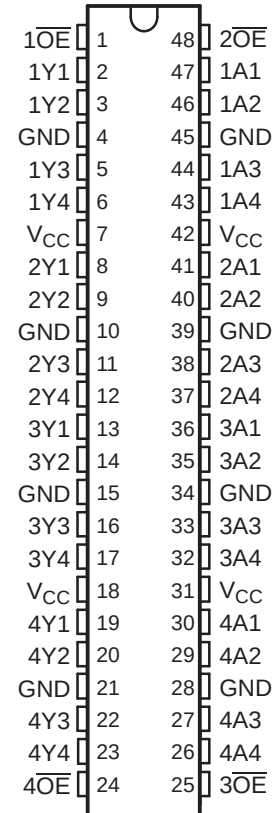


## FEATURES

- Members of the Texas Instruments Widebus™ Family
- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce) <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54LVTH162244... WD PACKAGE  
SN74LVTH162244... DGG OR DL PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

### ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE <sup>(1)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING  |
|----------------|------------------------|--------------|-----------------------|-------------------|
| –40°C to 85°C  | FBGA – GRD             | Reel of 1000 | 74LVTH162244GRDR      | LL2244            |
|                | FBGA – ZRD (Pb-free)   |              | 74LVTH162244ZRDR      |                   |
|                | SSOP – DL              | Tube of 25   | SN74LVTH162244DL      | LVTH162244        |
|                |                        |              | SN74LVTH162244DLG4    |                   |
|                |                        | Reel of 1000 | SN74LVTH162244DLR     |                   |
|                |                        |              | 74LVTH162244DLRG4     |                   |
|                | TSSOP – DGG            | Reel of 2000 | SN74LVTH162244DGGR    | LVTH162244        |
|                |                        |              | 74LVTH162244DGGRG4    |                   |
|                |                        |              | 74LVTH162244GRE4      |                   |
|                | VFBGA – GQL            | Reel of 1000 | SN74LVTH162244KR      | LL2244            |
|                | VFBGA – ZQL (Pb-free)  |              | 74LVTH162244ZQLR      |                   |
| –55°C to 125°C | CFP – WD               | Tube         | SNJ54LVTH162244WD     | SNJ54LVTH162244WD |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

## **DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

The 'LVTH162244 devices are 16-bit buffers and line drivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

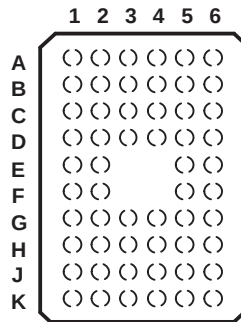
The outputs, which are designed to source or sink up to 12 mA, include equivalent 22- $\Omega$  series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**GQL OR ZQL PACKAGE  
(TOP VIEW)**

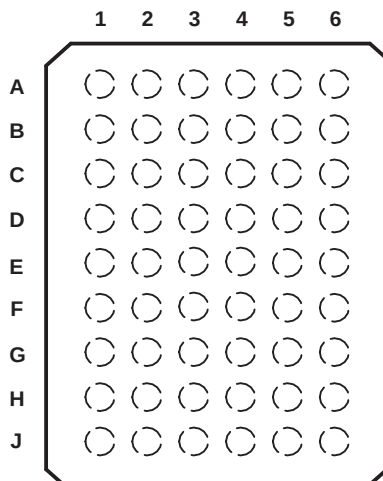


**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(56-Ball GQL/ZQL Package)**

|          | 1                 | 2   | 3               | 4               | 5   | 6                 |
|----------|-------------------|-----|-----------------|-----------------|-----|-------------------|
| <b>A</b> | 1 $\overline{OE}$ | NC  | NC              | NC              | NC  | 2 $\overline{OE}$ |
| <b>B</b> | 1Y2               | 1Y1 | GND             | GND             | 1A1 | 1A2               |
| <b>C</b> | 1Y4               | 1Y3 | V <sub>CC</sub> | V <sub>CC</sub> | 1A3 | 1A4               |
| <b>D</b> | 2Y2               | 2Y1 | GND             | GND             | 2A1 | 2A2               |
| <b>E</b> | 2Y4               | 2Y3 |                 |                 | 2A3 | 2A4               |
| <b>F</b> | 3Y1               | 3Y2 |                 |                 | 3A2 | 3A1               |
| <b>G</b> | 3Y3               | 3Y4 | GND             | GND             | 3A4 | 3A3               |
| <b>H</b> | 4Y1               | 4Y2 | V <sub>CC</sub> | V <sub>CC</sub> | 4A2 | 4A1               |
| <b>J</b> | 4Y3               | 4Y4 | GND             | GND             | 4A4 | 4A3               |
| <b>K</b> | 4 $\overline{OE}$ | NC  | NC              | NC              | NC  | 3 $\overline{OE}$ |

(1) NC – No internal connection

**GRD OR ZRD PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(54-Ball GRD/ZRD Package)**

|          | 1   | 2   | 3                 | 4                 | 5   | 6   |
|----------|-----|-----|-------------------|-------------------|-----|-----|
| <b>A</b> | 1Y1 | NC  | 1 $\overline{OE}$ | 2 $\overline{OE}$ | NC  | 1A1 |
| <b>B</b> | 1Y3 | 1Y2 | NC                | NC                | 1A2 | 1A3 |
| <b>C</b> | 2Y1 | 1Y4 | V <sub>CC</sub>   | V <sub>CC</sub>   | 1A4 | 2A1 |
| <b>D</b> | 2Y3 | 2Y2 | GND               | GND               | 2A2 | 2A3 |
| <b>E</b> | 3Y1 | 2Y4 | GND               | GND               | 2A4 | 3A1 |
| <b>F</b> | 3Y3 | 3Y2 | GND               | GND               | 3A2 | 3A3 |
| <b>G</b> | 4Y1 | 3Y4 | V <sub>CC</sub>   | V <sub>CC</sub>   | 3A4 | 4A1 |
| <b>H</b> | 4Y3 | 4Y2 | NC                | NC                | 4A2 | 4A3 |
| <b>J</b> | 4Y4 | NC  | 4 $\overline{OE}$ | 3 $\overline{OE}$ | NC  | 4A4 |

(1) NC – No internal connection

**FUNCTION TABLE  
(EACH 4-BIT BUFFER)**

| INPUTS          |   | OUTPUT<br>Y |
|-----------------|---|-------------|
| $\overline{OE}$ | A |             |
| L               | H | H           |
| L               | L | L           |
| H               | X | Z           |

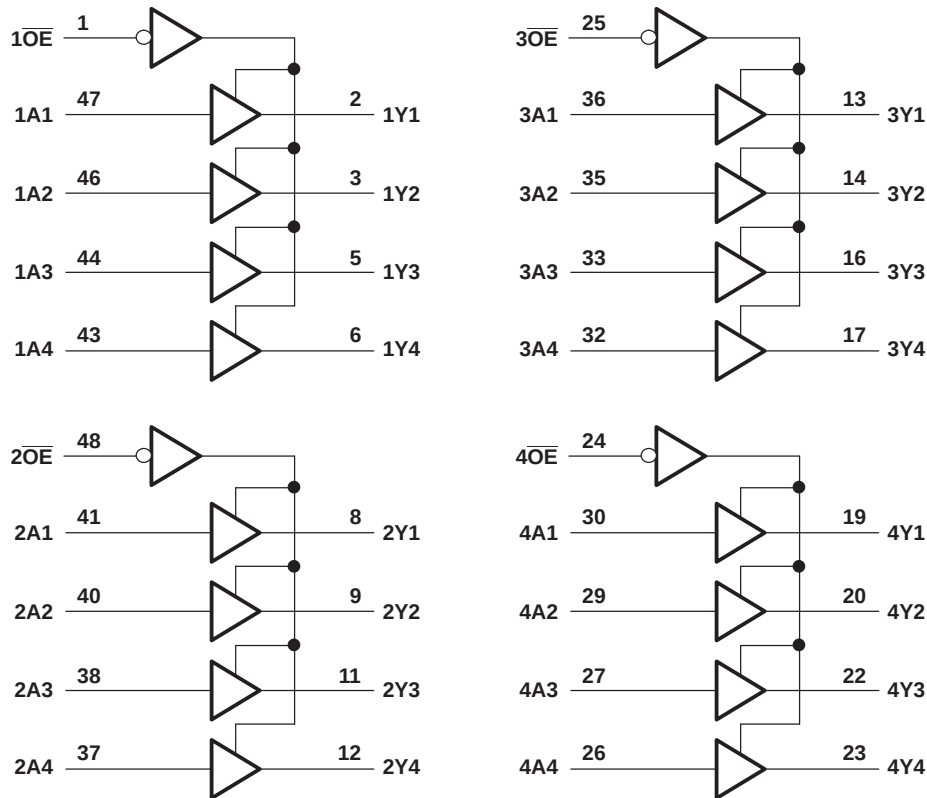
# SN54LVTH162244, SN74LVTH162244

## 3.3-V ABT 16-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

SCBS258N – JUNE 1993 – REVISED NOVEMBER 2006

#### LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DL, and WD packages.

#### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|               |                                                                                             | MIN             | MAX            | UNIT |
|---------------|---------------------------------------------------------------------------------------------|-----------------|----------------|------|
| $V_{CC}$      | Supply voltage range                                                                        | -0.5            | 4.6            | V    |
| $V_I$         | Input voltage range <sup>(2)</sup>                                                          | -0.5            | 7              | V    |
| $V_O$         | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | -0.5            | 7              | V    |
| $V_O$         | Voltage range applied to any output in the high state <sup>(2)</sup>                        | -0.5            | $V_{CC} + 0.5$ | V    |
| $I_O$         | Current into any output in the low state                                                    |                 | 30             | mA   |
| $I_O$         | Current into any output in the high state <sup>(3)</sup>                                    |                 | 30             | mA   |
| $I_{IK}$      | Input clamp current                                                                         | $V_I < 0$       | -50            | mA   |
| $I_{OK}$      | Output clamp current                                                                        | $V_O < 0$       | -50            | mA   |
| $\theta_{JA}$ | Package thermal impedance <sup>(4)</sup>                                                    | DGG package     | 70             | °C/W |
|               |                                                                                             | DL package      | 63             |      |
|               |                                                                                             | GQL/ZQL package | 42             |      |
|               |                                                                                             | GRD/ZRD package | 36             |      |
| $T_{stg}$     | Storage temperature range                                                                   | -65             | 150            | °C   |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This current flows only when the output is in the high state and  $V_O > V_{CC}$ .

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

|                     |                                    |                 | SN54LVTH162244 |     | SN74LVTH162244 |     | UNIT |
|---------------------|------------------------------------|-----------------|----------------|-----|----------------|-----|------|
|                     |                                    |                 | MIN            | MAX | MIN            | MAX |      |
| V <sub>CC</sub>     | Supply voltage                     |                 | 2.7            | 3.6 | 2.7            | 3.6 | V    |
| V <sub>IH</sub>     | High-level input voltage           |                 | 2              |     | 2              |     | V    |
| V <sub>IL</sub>     | Low-level input voltage            |                 |                | 0.8 |                | 0.8 | V    |
| V <sub>I</sub>      | Input voltage                      |                 |                | 5.5 |                | 5.5 | V    |
| I <sub>OH</sub>     | High-level output current          |                 |                | –12 |                | –12 | mA   |
| I <sub>OL</sub>     | Low-level output current           |                 |                | 12  |                | 12  | mA   |
| Δt/Δv               | Input transition rise or fall rate | Outputs enabled |                | 10  |                | 10  | ns/V |
| Δt/ΔV <sub>CC</sub> | Power-up ramp rate                 |                 | 200            |     | 200            |     | μs/V |
| T <sub>A</sub>      | Operating free-air temperature     |                 | –55            | 125 | –40            | 85  | °C   |

(1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                       |                | TEST CONDITIONS                                                                                              |                                  | SN54LVTH162244      |                    | SN74LVTH162244 |     | UNIT |
|---------------------------------|----------------|--------------------------------------------------------------------------------------------------------------|----------------------------------|---------------------|--------------------|----------------|-----|------|
|                                 |                |                                                                                                              |                                  | MIN                 | TYP <sup>(1)</sup> | MAX            | MIN |      |
| V <sub>IK</sub>                 |                | V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = −18 mA                                                             |                                  | −1.2                |                    | −1.2           |     | V    |
| V <sub>OH</sub>                 |                | V <sub>CC</sub> = 3 V, I <sub>OH</sub> = −12 mA                                                              |                                  | 2                   |                    | 2              |     | V    |
| V <sub>OL</sub>                 |                | V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 12 mA                                                               |                                  | 0.8                 |                    | 0.8            |     | V    |
| I <sub>I</sub>                  |                | V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V                                                         |                                  | 10                  |                    | 10             |     | μA   |
|                                 | Control inputs | V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND                                             |                                  | ±1                  |                    | ±1             |     |      |
|                                 | Data inputs    | V <sub>CC</sub> = 3.6 V                                                                                      | V <sub>I</sub> = V <sub>CC</sub> | 1                   |                    | 1              |     |      |
|                                 |                |                                                                                                              | V <sub>I</sub> = 0               | −5                  |                    | −5             |     |      |
| I <sub>off</sub>                |                | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V                                           |                                  |                     |                    | ±100           |     | μA   |
| I <sub>I(hold)</sub>            | Data inputs    | V <sub>CC</sub> = 3 V                                                                                        | V <sub>I</sub> = 0.8 V           | 75                  |                    | 75             |     | μA   |
|                                 |                |                                                                                                              | V <sub>I</sub> = 2 V             | −75                 |                    | −75            |     |      |
|                                 |                | V <sub>CC</sub> = 3.6 V, <sup>(2)</sup> V <sub>I</sub> = 0 to 3.6 V                                          |                                  |                     |                    | 500<br>−750    |     |      |
| I <sub>OZH</sub>                |                | V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 3 V                                                                |                                  | 5                   |                    | 5              |     | μA   |
| I <sub>OZL</sub>                |                | V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0.5 V                                                              |                                  | −5                  |                    | −5             |     | μA   |
| I <sub>OZPU</sub>               |                | V <sub>CC</sub> = 0 to 1.5 V, V <sub>O</sub> = 0.5 V to 3 V, $\overline{OE}$ = don't care                    |                                  | ±100 <sup>(3)</sup> |                    | ±100           |     | μA   |
| I <sub>OZPD</sub>               |                | V <sub>CC</sub> = 1.5 V to 0, V <sub>O</sub> = 0.5 V to 3 V, $\overline{OE}$ = don't care                    |                                  | ±100 <sup>(3)</sup> |                    | ±100           |     | μA   |
| I <sub>CC</sub>                 |                | V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND                         | Outputs high                     | 0.19                |                    | 0.19           |     | mA   |
|                                 |                |                                                                                                              | Outputs low                      | 5                   |                    | 5              |     |      |
|                                 |                |                                                                                                              | Outputs disabled                 | 0.19                |                    | 0.19           |     |      |
| ΔI <sub>CC</sub> <sup>(4)</sup> |                | V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND |                                  | 0.2                 |                    | 0.2            |     | mA   |
| C <sub>i</sub>                  |                | V <sub>I</sub> = 3 V or 0                                                                                    |                                  | 4                   |                    | 4              |     | pF   |
| C <sub>o</sub>                  |                | V <sub>O</sub> = 3 V or 0                                                                                    |                                  | 9                   |                    | 9              |     | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

# SN54LVTH162244, SN74LVTH162244

## 3.3-V ABT 16-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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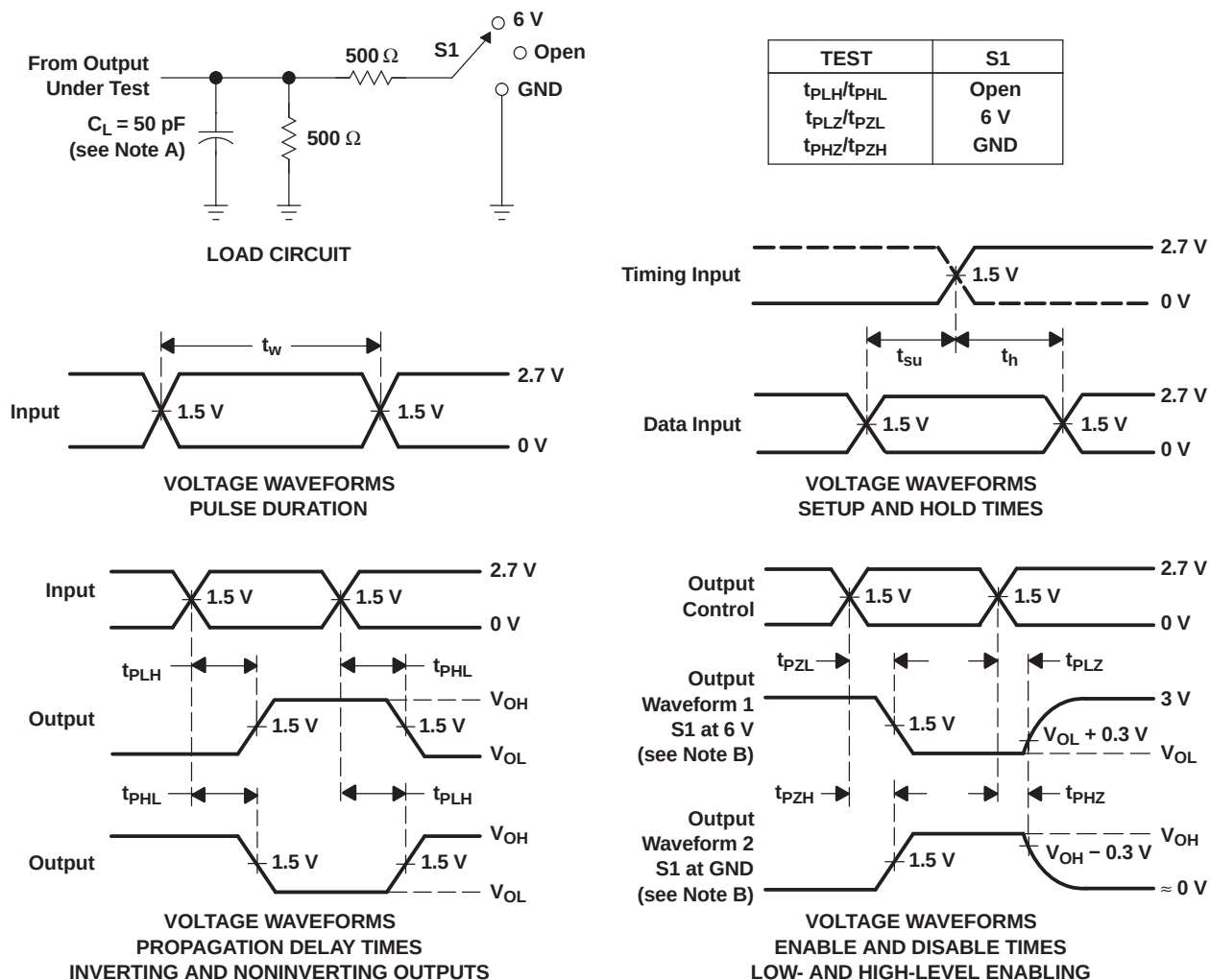
### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see [Figure 1](#))

| PARAMETER           | FROM<br>(INPUT) | TO<br>(OUTPUT) | SN54LVTH162244                     |     |                         |     | SN74LVTH162244                     |                    |                         |     | UNIT |     |
|---------------------|-----------------|----------------|------------------------------------|-----|-------------------------|-----|------------------------------------|--------------------|-------------------------|-----|------|-----|
|                     |                 |                | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |                    | V <sub>CC</sub> = 2.7 V |     |      |     |
|                     |                 |                | MIN                                | MAX | MIN                     | MAX | MIN                                | TYP <sup>(1)</sup> | MAX                     | MIN |      | MAX |
| t <sub>PLH</sub>    | A               | Y              | 1.1                                | 4.6 | 5.1                     |     | 1.4                                | 3.4                | 4                       | 4.8 |      | ns  |
| t <sub>PHL</sub>    |                 |                | 1.1                                | 3.9 | 4.5                     |     | 1.2                                | 2.9                | 3.6                     | 4.1 |      |     |
| t <sub>PZH</sub>    | OE              | Y              | 1.1                                | 5.4 | 6.7                     |     | 1.2                                | 3.9                | 5.1                     | 6.5 |      | ns  |
| t <sub>PZL</sub>    |                 |                | 1.3                                | 4.9 | 6.1                     |     | 1.4                                | 3.8                | 4.5                     | 5.8 |      |     |
| t <sub>PHZ</sub>    | OE              | Y              | 1.6                                | 5.9 | 6.5                     |     | 2.2                                | 4.4                | 5.0                     | 5.4 |      | ns  |
| t <sub>PLZ</sub>    |                 |                | 1                                  | 5.9 | 5.8                     |     | 2                                  | 4.2                | 5.0                     | 5.4 |      |     |
| t <sub>sk(LH)</sub> |                 |                |                                    |     |                         |     |                                    |                    | 0.5                     |     |      | ns  |
| t <sub>sk(HL)</sub> |                 |                |                                    |     |                         |     |                                    |                    | 0.5                     |     |      |     |

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                          |
|------------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------------------------|
| <a href="#">5962-9680901QXA</a>    | Active        | Production           | CFP (WD)   48    | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9680901QX<br>A<br>SNJ54LVTH16224<br>4WD |
| <a href="#">5962-9680901VXA</a>    | Active        | Production           | CFP (WD)   48    | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9680901VX<br>A<br>SNV54LVTH16224<br>4WD |
| 74LVTH162244DLR1G4                 | Active        | Production           | SSOP (DL)   48   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH162244                                   |
| 74LVTH162244DLR1G4.B               | Active        | Production           | SSOP (DL)   48   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH162244                                   |
| 8W2244DGGRG4                       | Active        | Production           | TSSOP (DGG)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH162244                                   |
| 8W2244DGGRG4.B                     | Active        | Production           | TSSOP (DGG)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH162244                                   |
| <a href="#">SN74LVTH162244DGGR</a> | Active        | Production           | TSSOP (DGG)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH162244                                   |
| SN74LVTH162244DGGR.B               | Active        | Production           | TSSOP (DGG)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH162244                                   |
| <a href="#">SN74LVTH162244DL</a>   | Active        | Production           | SSOP (DL)   48   | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH162244                                   |
| SN74LVTH162244DL.B                 | Active        | Production           | SSOP (DL)   48   | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH162244                                   |
| <a href="#">SN74LVTH162244DLR</a>  | Active        | Production           | SSOP (DL)   48   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH162244                                   |
| SN74LVTH162244DLR.B                | Active        | Production           | SSOP (DL)   48   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH162244                                   |
| <a href="#">SNJ54LVTH162244WD</a>  | Active        | Production           | CFP (WD)   48    | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9680901QX<br>A<br>SNJ54LVTH16224<br>4WD |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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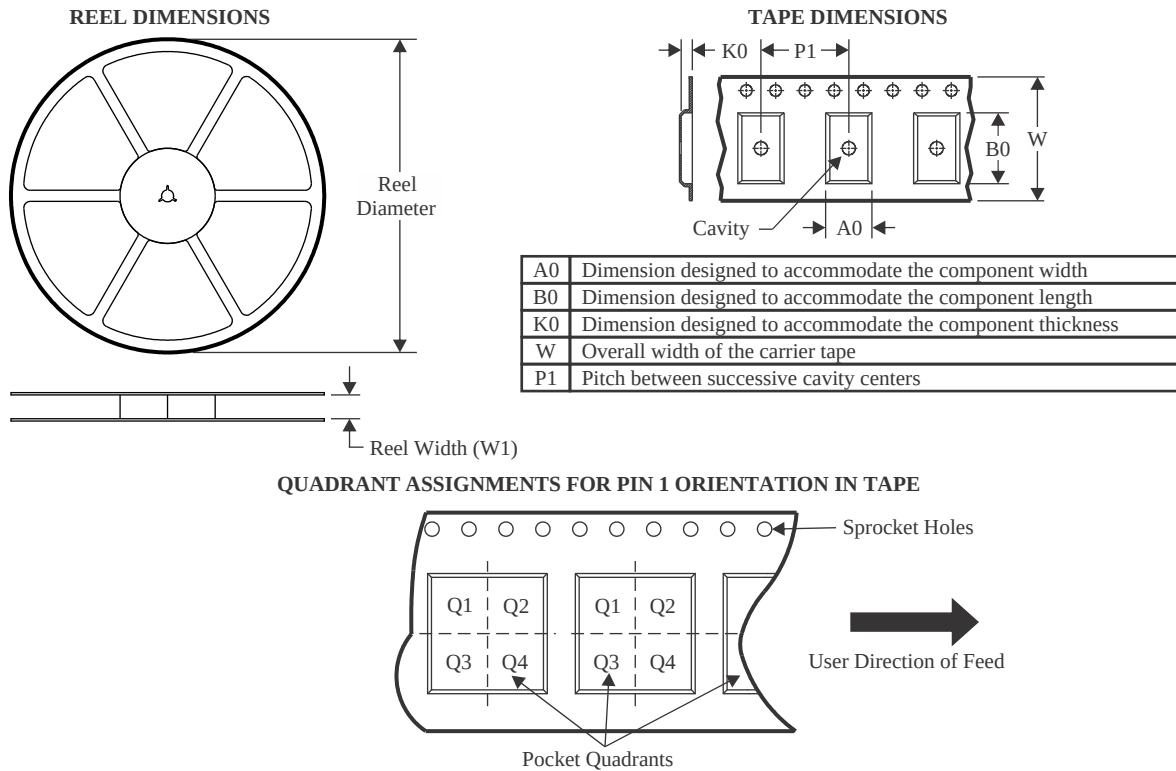
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVTH162244, SN54LVTH162244-SP, SN74LVTH162244 :**

- Catalog : [SN74LVTH162244](#), [SN54LVTH162244](#)
- Enhanced Product : [SN74LVTH162244-EP](#), [SN74LVTH162244-EP](#)
- Military : [SN54LVTH162244](#)
- Space : [SN54LVTH162244-SP](#)

**NOTE: Qualified Version Definitions:**

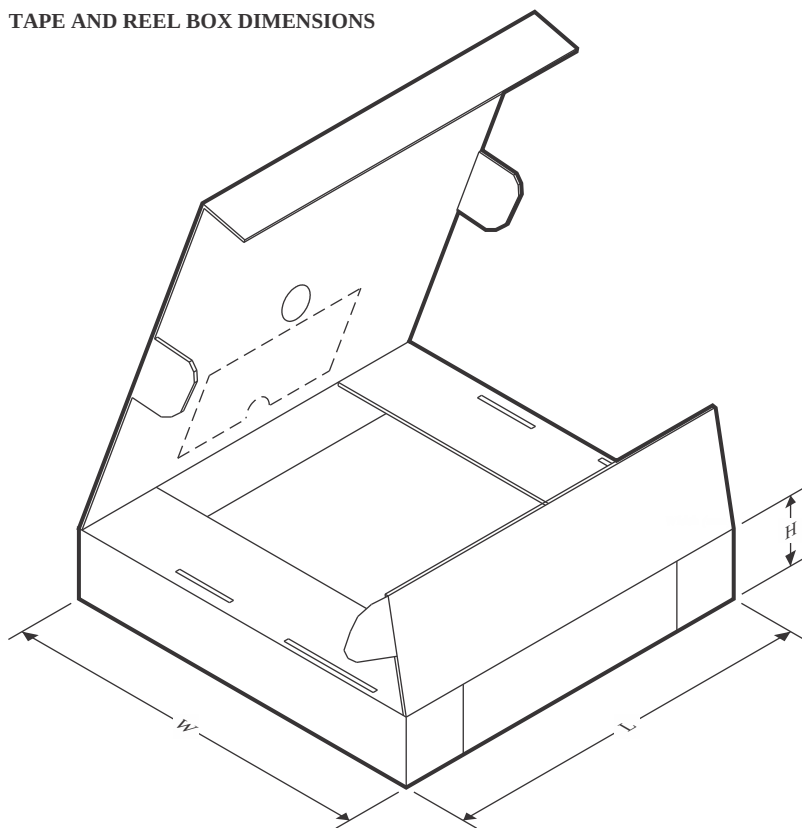
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74LVTH162244DLR1G4 | SSOP         | DL              | 48   | 1000 | 330.0              | 32.4               | 11.35   | 16.2    | 3.1     | 16.0    | 32.0   | Q1            |
| 8W2244DGGRG4       | TSSOP        | DGG             | 48   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |
| SN74LVTH162244DGGR | TSSOP        | DGG             | 48   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |
| SN74LVTH162244DLR  | SSOP         | DL              | 48   | 1000 | 330.0              | 32.4               | 11.35   | 16.2    | 3.1     | 16.0    | 32.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74LVTH162244DLR1G4 | SSOP         | DL              | 48   | 1000 | 356.0       | 356.0      | 53.0        |
| 8W2244DGGRG4       | TSSOP        | DGG             | 48   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74LVTH162244DGGR | TSSOP        | DGG             | 48   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74LVTH162244DLR  | SSOP         | DL              | 48   | 1000 | 356.0       | 356.0      | 53.0        |

## TUBE

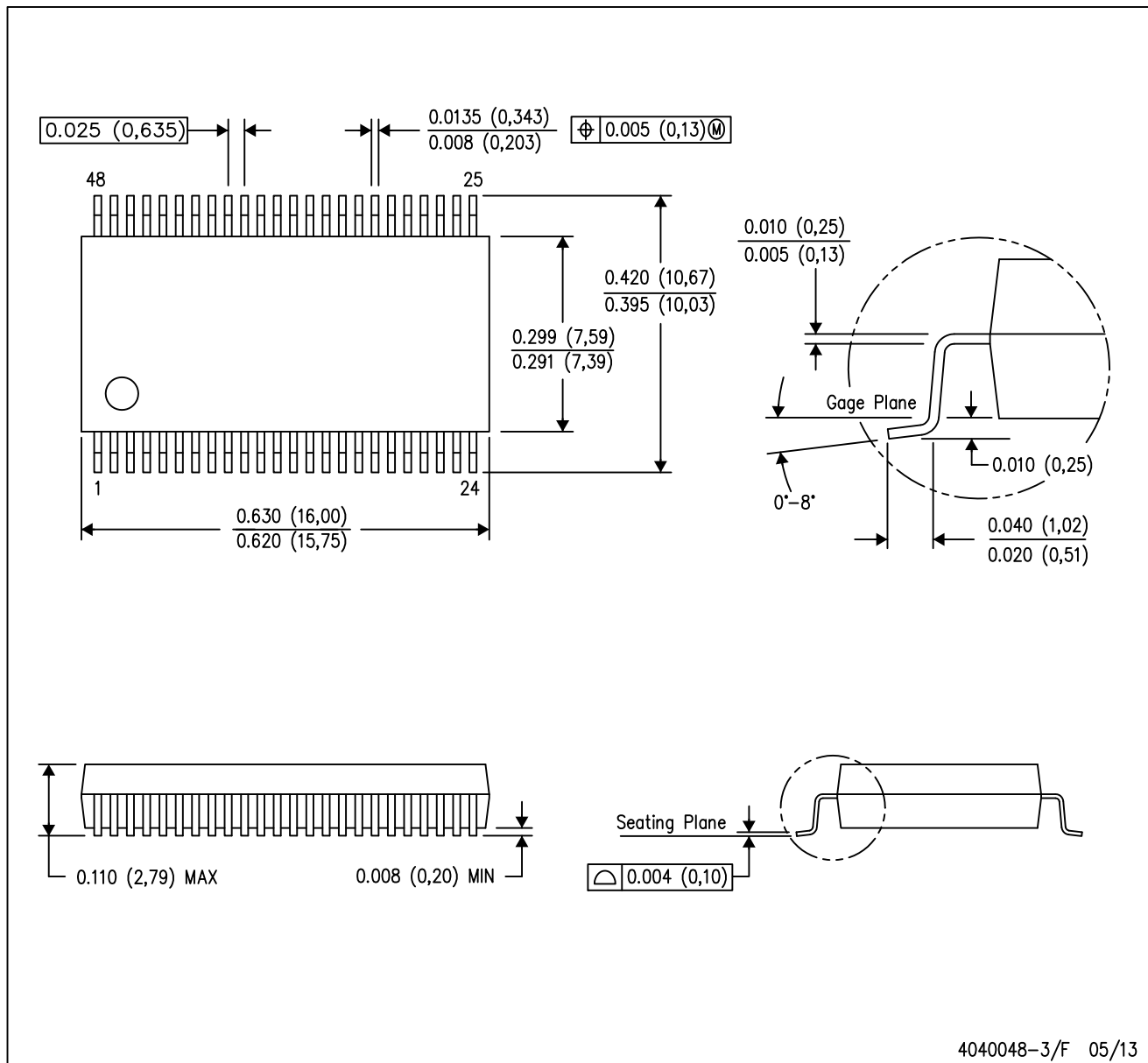


\*All dimensions are nominal

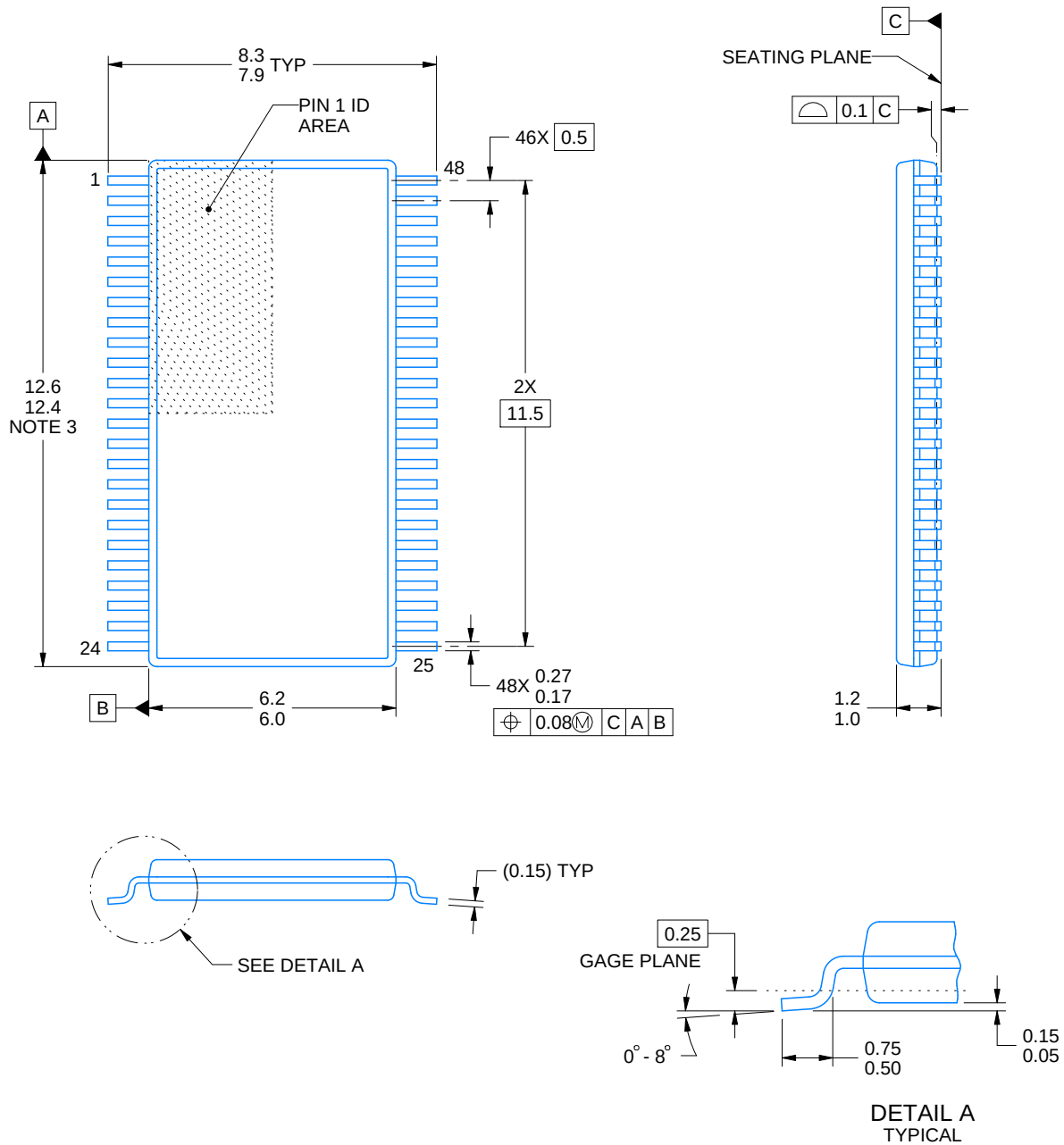
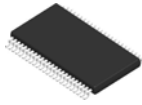
| Device             | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVTH162244DL   | DL           | SSOP         | 48   | 25  | 473.7  | 14.24  | 5110   | 7.87   |
| SN74LVTH162244DL.B | DL           | SSOP         | 48   | 25  | 473.7  | 14.24  | 5110   | 7.87   |

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MO-118



4214859/B 11/2020

## NOTES:

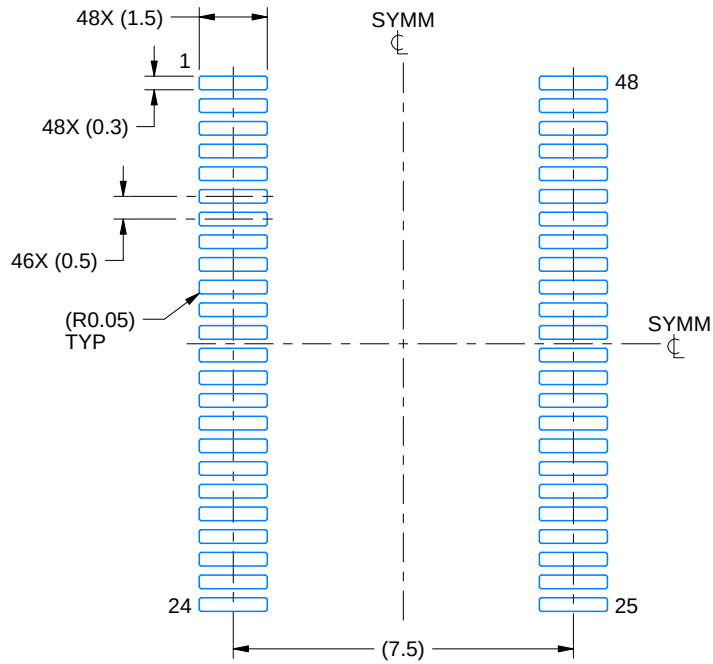
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

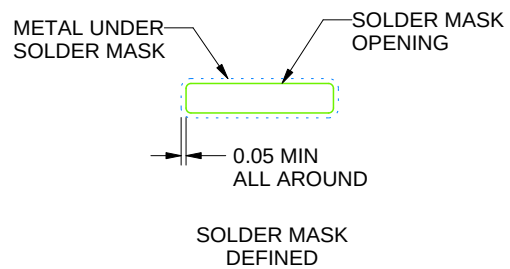
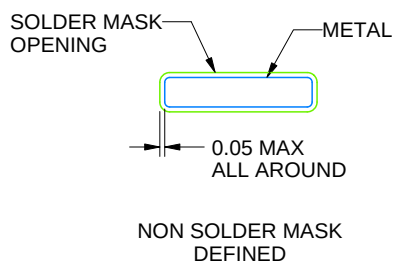
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

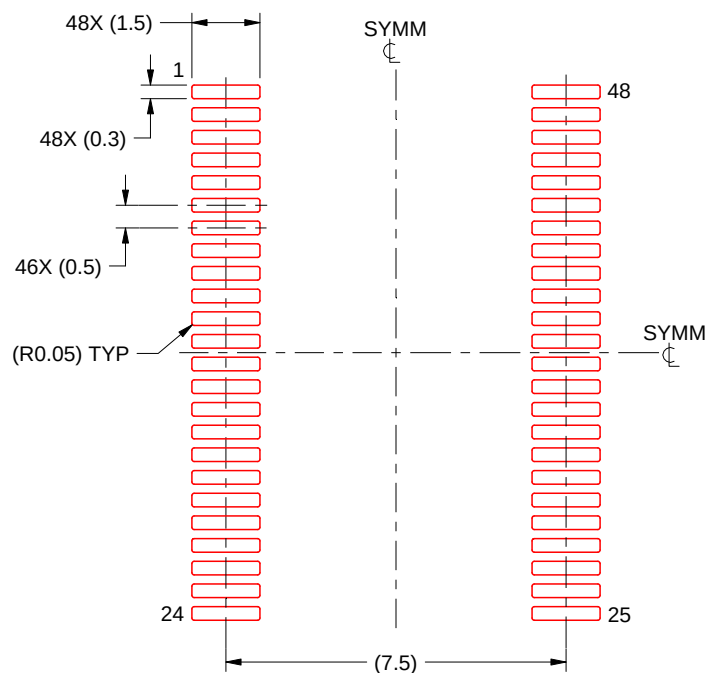
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

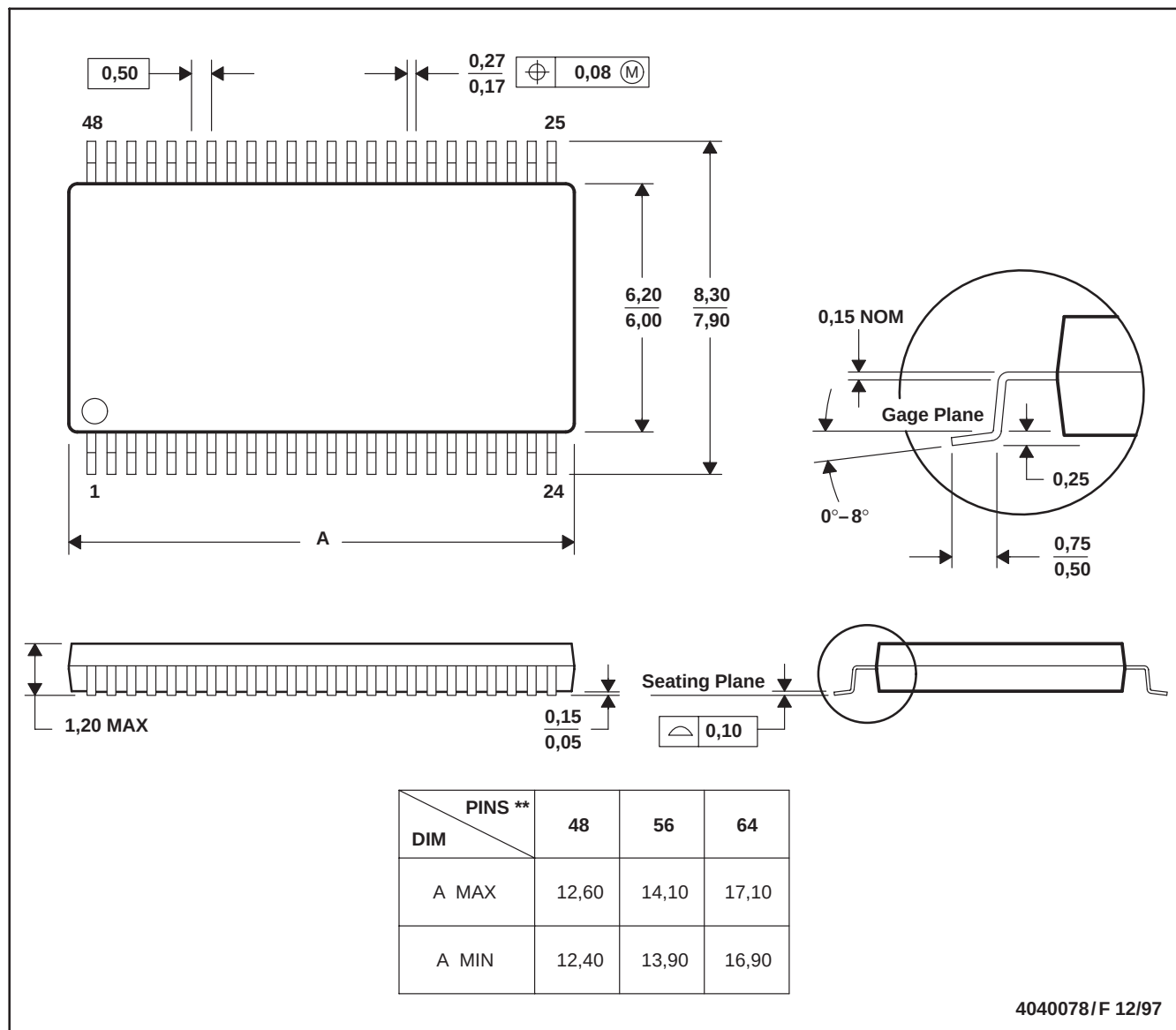
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

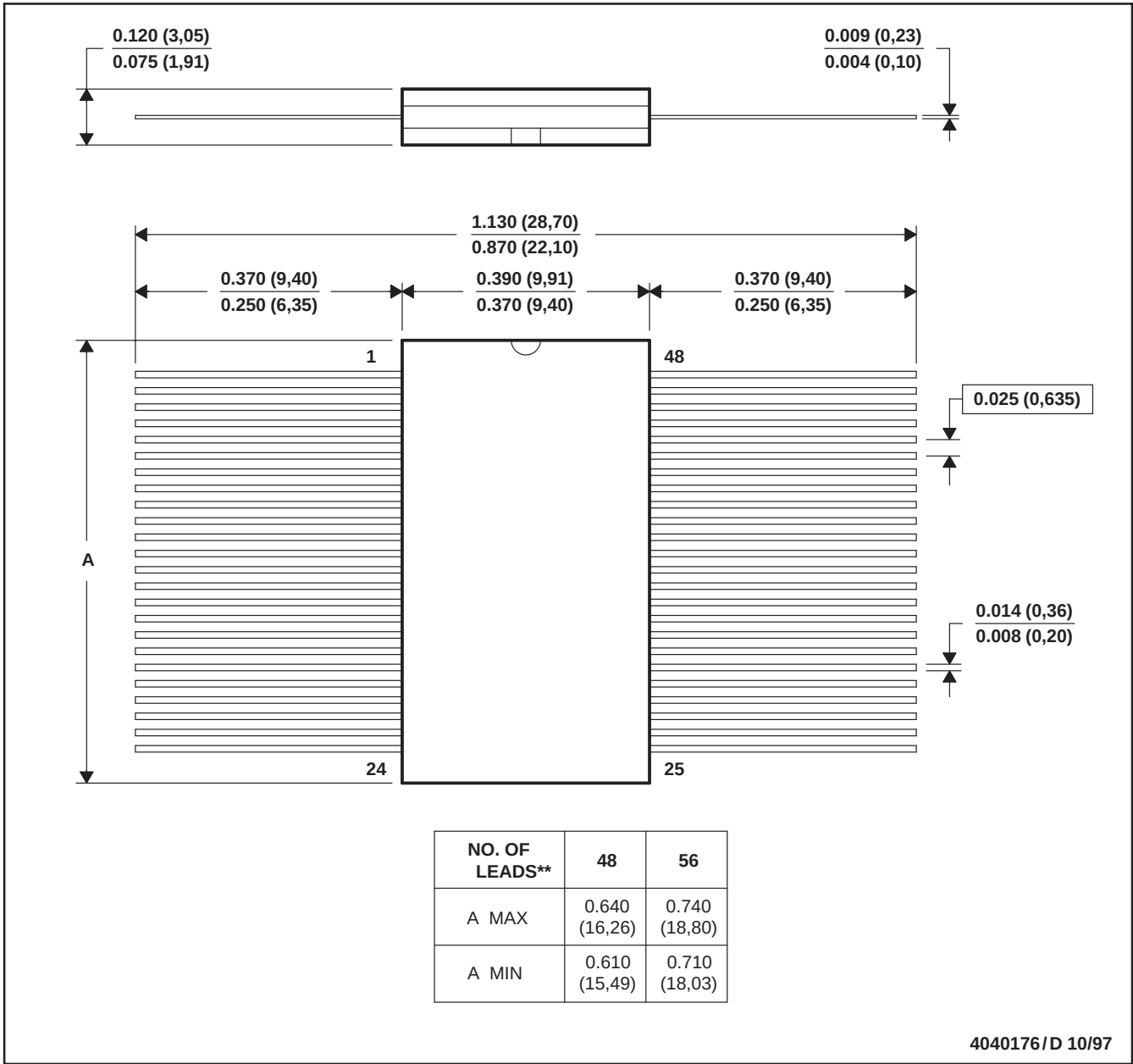
48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

WD (R-GDFP-F\*\*)  
48 LEADS SHOWN

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package can be hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only  
E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
GDFP1-F56 and JEDEC MO-146AB

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