3.3V ECL Differential LVPECL/LVDS to LVTTL/LVCMOS Translator

Check for Samples: SN65EPT23

FEATURES

- **Dual 3.3 V Differential LVPECL/LVDS to LVTTL/LVCMOS Buffer Translator**
- **24 mA LVTTL Ouputs**
- **Operating Range**
  - **V_{CC} = 3.0 V to 3.6 V**
  - **GND = 0 V**
- **Support for Clock Frequencies > 300 MHz**
- **2.0 ns Typical Propagation Delay**
- **Built-in Temperature Compensation**
- **Drop in Compatible to MC100EPT23**

APPLICATIONS

- **Data and Clock Transmission Over Backplane**
- **Signaling Level Conversion for Clock or Data**

DESCRIPTION

The SN65EPT23 is a low power dual LVPECL/LVDS to LVTTL/LVCMOS translator device. The device includes circuitry to maintain inputs at Vcc/2 when left open. The SN65EPT23 is housed in an industry standard SOIC-8 package and is also available in TSSOP-8 option.

PINOUT ASSIGNMENT

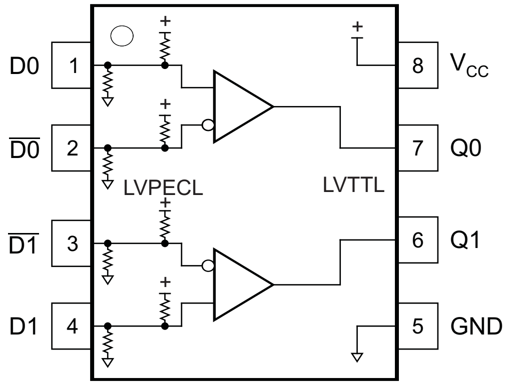

Table 1. Pin Description

PIN	FUNCTION
Q_0, Q_1	LVTTL/LVCMOS Outputs
D_0, $\overline{D}_0$, D_1, $\overline{D}_1$	Differential LVPECL/LVDS/CML Inputs
V_{CC}	Positive Supply
GND	Ground

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65EPT23D/DR	EPT23	SOIC	NiPdAu
SN65EPT23DGK/DGKR	SSTI	MSOP	NiPdAu

(1) Leaded device option not initially available; contact TI sales representative for further information.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	CONDITION	VALUE	UNIT
Absolute supply voltage, V_{CC}	GND = 0V	3.8	V
Absolute input voltage, V_I	GND = 0 and Vi ≤ V_{CC}	0 to 3.8	V
Output current	Continuous	50	mA
	Surge	100	
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING T_A < 25°C (mW)	THERMAL RESISTANCE, JUNCTION TO AMBIENT NO AIRFLOW	DERATING FACTOR T_A > 25°C (mW/°C)	POWER RATING T_A = 85°C (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
MSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to Board Thermal Resistance	SOIC	79	°C/W
		MSOP	120	
θ_{JC}	Junction-to Case Thermal Resistance	SOIC	98	°C/W
		MSOP	74	

KEY ATTRIBUTES

CHARACTERISTICS	VALUE
Moisture sensitivity level	Level 1
Flammability rating (Oxygen Index: 28 to 34)	UL 94 V-0 at 0.125 in
ESD-HBM	2 kV
ESD-machine model	200 V
ESD-charge device model	2 kV
Internal pull down resistor	50 kΩ
Internal pull up resistor	50 kΩ
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test	

LVTTL OUTPUT DC CHARACTERISTICS[1] (V_{CC} = 3.3 V; GND = 0 V, TA = -40C to 85C)[2]

PARAMETER		CONDITION	–40°C			25°C			85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Output short circuit current		–180	–140	–50	-180	–144	–50	–180	–148	–50	mA
V_{OH}	Output high voltage[3]	I_{OH} = –3.0 mA	2.4			2.4			2.4			V
V_{OL}	Output low voltage	I_{OL} = 24 mA			0.5			0.5			0.5	V

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(1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) All values vary 1:1 with Vcc; Vcc can vary ±0.3V
(3) LVTTL output R_L = 500 Ω to GND

LVPECL INPUT DC CHARACTERISTICS[1] (V_{CC} = 3.3 V; GND = 0.0 V)[2]

PARAMETER			–40°C			25°C			85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CCH}	Power supply current (Outputs set to high)			15	25		15	25		15	25	mA
I_{CCL}	Power supply current (Outputs set to low)			15	25		15	25		15	25	mA
V_{IH}	Input high voltage		2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input low voltage		1355		1675	1355		1675	1355		1675	mV
V_{IHCMR}	Input high voltage common mode range (Differential) [3]		1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input high current				150			150			150	µA
I_{IL}	Input low current	D	–150			–150			–150		0.5	µA
		$\overline{D}$										

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(1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input and output parameters vary 1:1 with V_{CC}. V_{CC} can vary ±0.3 V.
(3) V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}. V_{IHCMR} is referenced to most positive side of differential signal

AC CHARACTERISTICS[1] (V_{CC} = 3.0 V to 3.6 V; GND = 0.0 V)[2] [3]

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Max switching frequency[4] (Figure 1–Figure 3)	300			300			300			MHz
t_{PLH} / t_{PHL}	Propagation delay low to high; output at 1.5V	1.1	1.3	1.9	1.1	1.3	1.9	1.1	1.3	1.9	ns
T_{SK++}	Output to output skew++			110			110			110	ps
T_{SK--}	Output to output skew- -			110			110			110	ps
T_{SKPP}	Part to part skew [5]			400			400			400	ps
t_{JITTER}	Random clock jitter (RMS)[6]			10			10			10	ps
V_{PP}	Input voltage swing [7]	150		1200	150		1200	150		1200	mV
t_r/t_f	Output rise/fall times (0.8 V – 2.0 V)	250	560	800	250	580	800	250	600	800	ps

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(1) Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input parameters vary 1:1 with V_{CC}. V_{CC} can vary ±0.3V .
(3) TTL output R_L = 500 Ω to GND and C_L = 20 pF to GND see Figure 4.
(4) F_{max} assures for functionality only; V_{OL} and V_{OH} levels are assured at DC only
(5) Skews are measured between outputs under identical conditions.
(6) Measured with V_{ID} = 1.5 V_{PP} at V_{CM} = 2.0 V and 1.2 V
(7) 200 mV input assured full logic swing at the output.

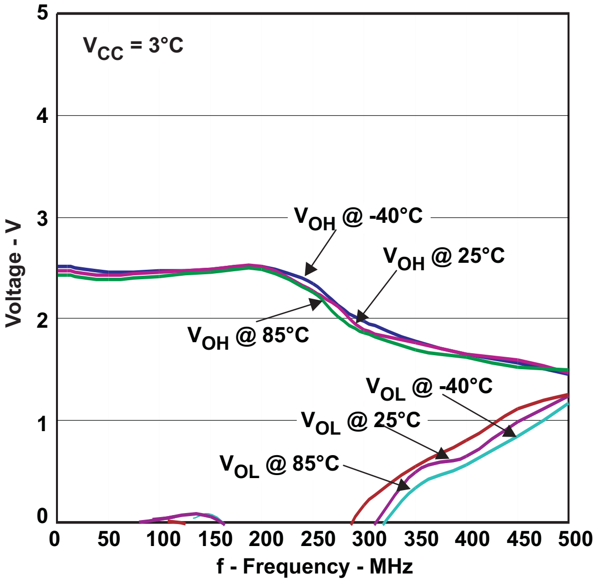

Figure 1. Maximum Switching Frequency V_{CC} = 3.0 V

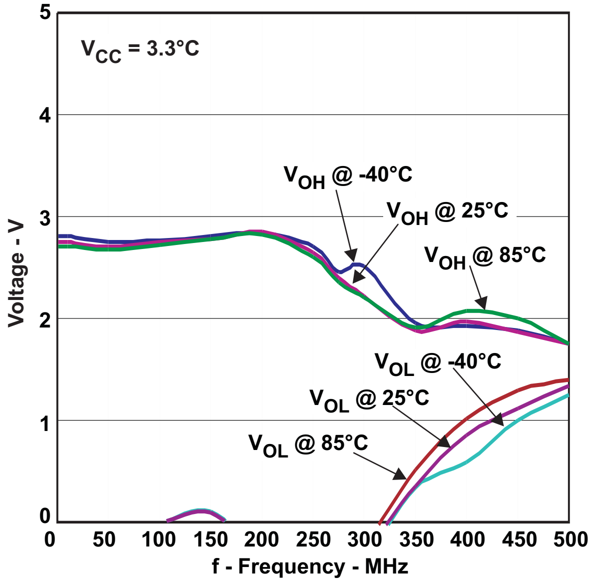

Figure 2. Maximum Switching Frequency V_{CC} = 3.3 V

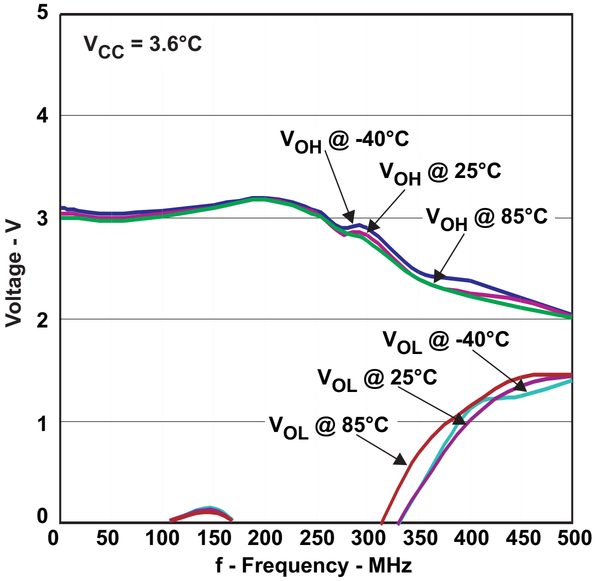

Figure 3. Maximum Switching Frequency V_{CC} = 3.6 V

Typical Output Loading Used for Device Evaluation

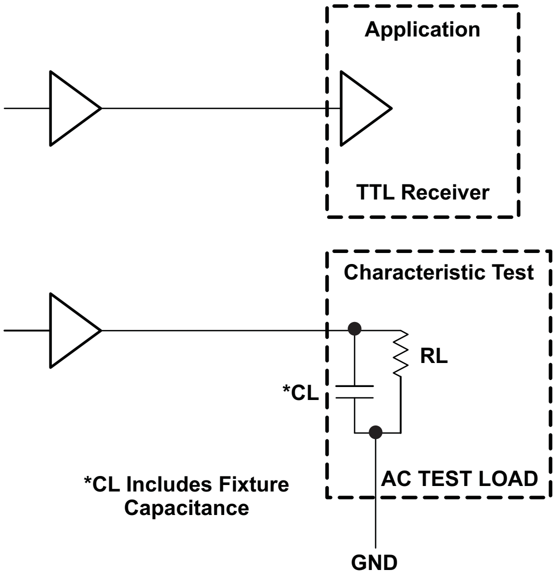

Figure 4. TTL Output Loading Used for Device Evaluation

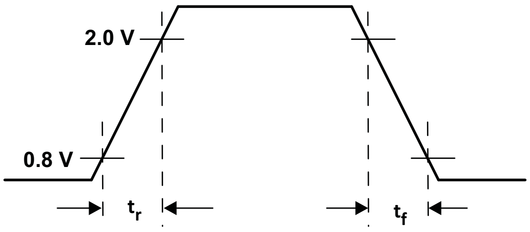

Figure 5. Output Rise and Fall Times

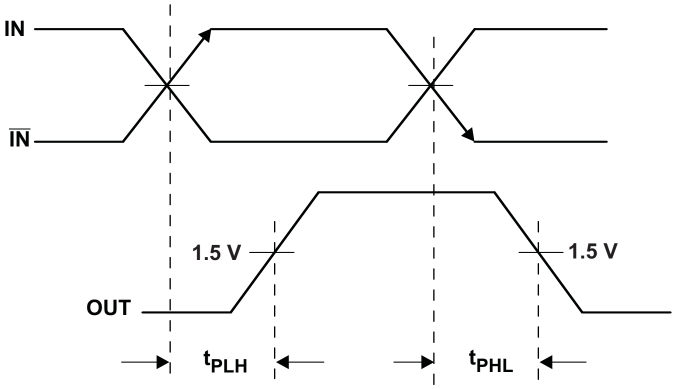

Figure 6. Output Propagation Delay

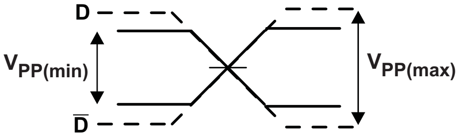

Figure 7. Input Voltage Swing

REVISION HISTORY

Changes from Original (November 2009) to Revision A	**Page**
• Deleted last row from the Pin Description Table (EP)	1

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65EPT23D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	EPT23
SN65EPT23D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	EPT23
SN65EPT23DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	Call TI | Nipdauag	Level-1-260C-UNLIM	-40 to 85	SSTI
SN65EPT23DGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	SSTI
SN65EPT23DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	SSTI
SN65EPT23DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SSTI
SN65EPT23DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	EPT23
SN65EPT23DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	EPT23

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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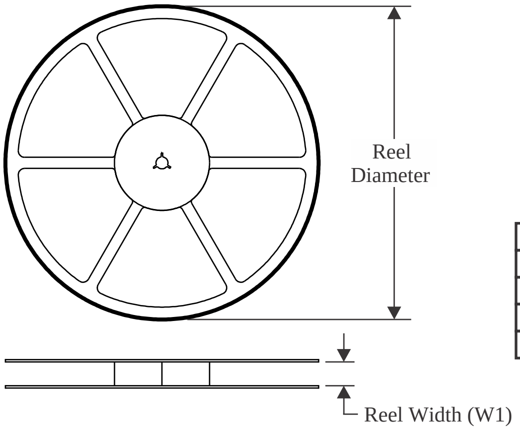
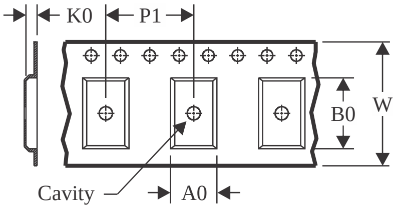
TAPE AND REEL INFORMATION

REEL DIMENSIONS

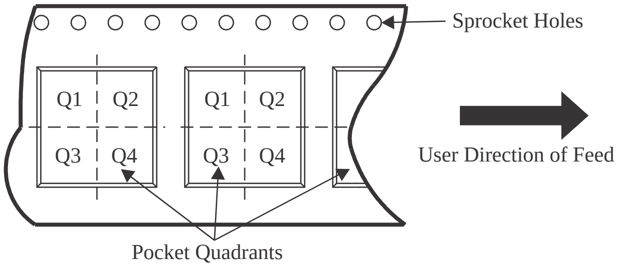


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

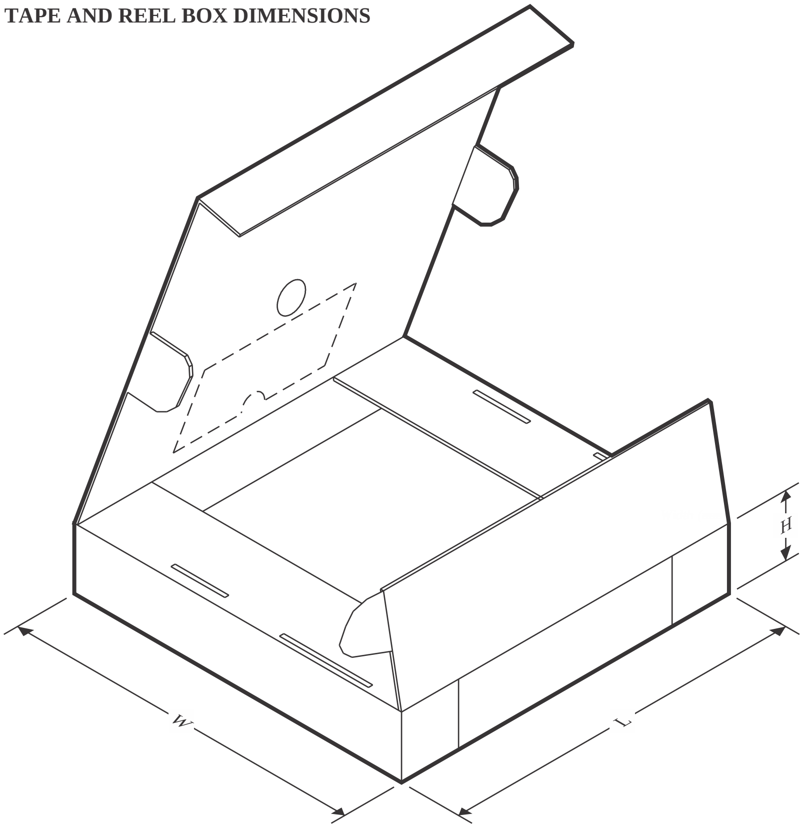
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65EPT23DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

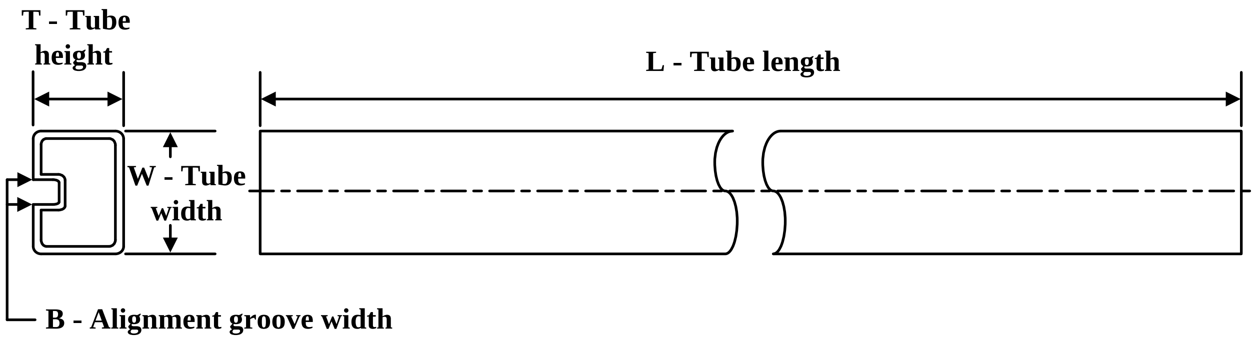
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

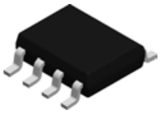
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65EPT23DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65EPT23D	D	SOIC	8	75	506.6	8	3940	4.32
SN65EPT23D.B	D	SOIC	8	75	506.6	8	3940	4.32
SN65EPT23DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
SN65EPT23DGK.B	DGK	VSSOP	8	80	330.2	6.6	3005	1.88

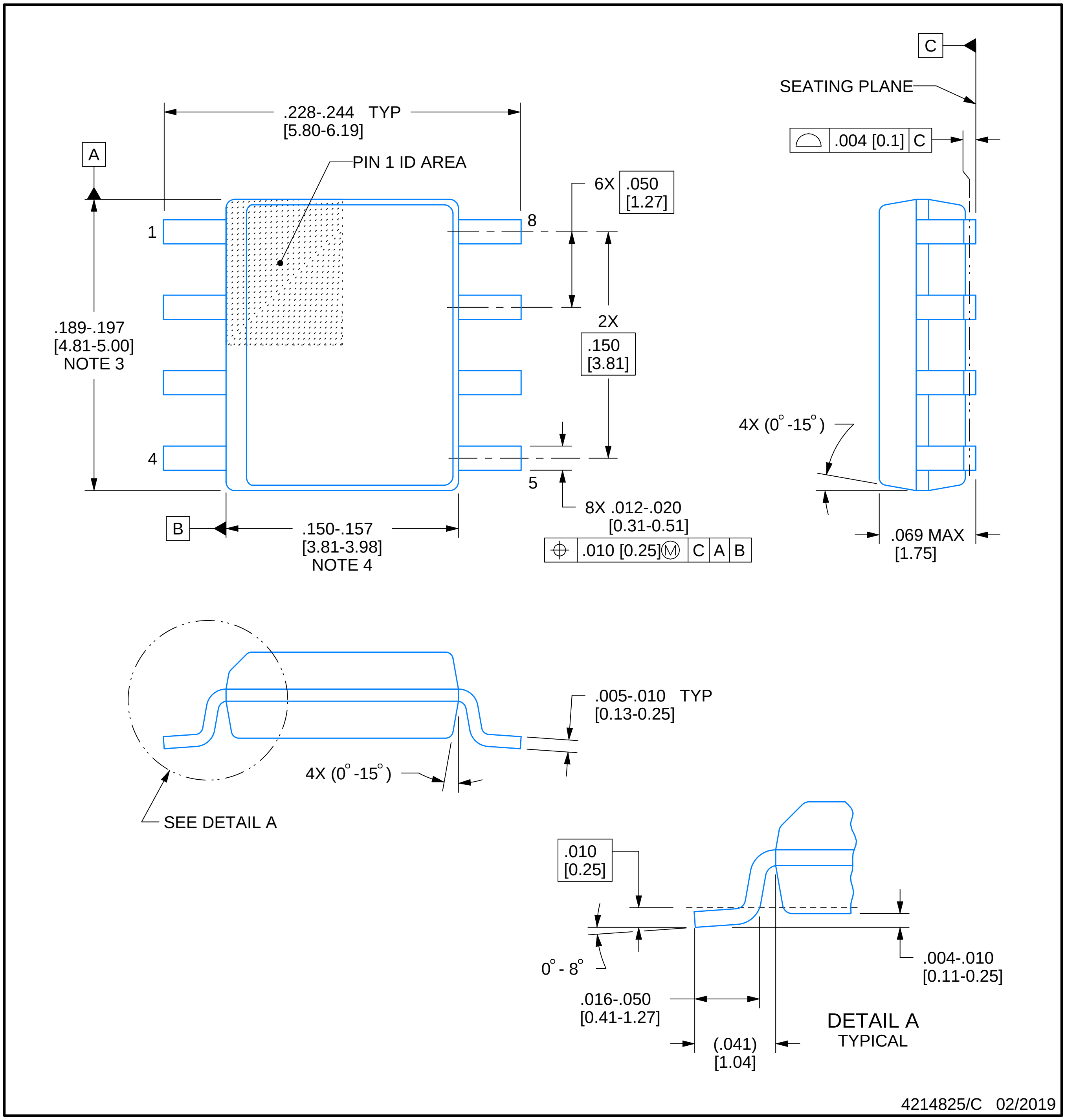


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

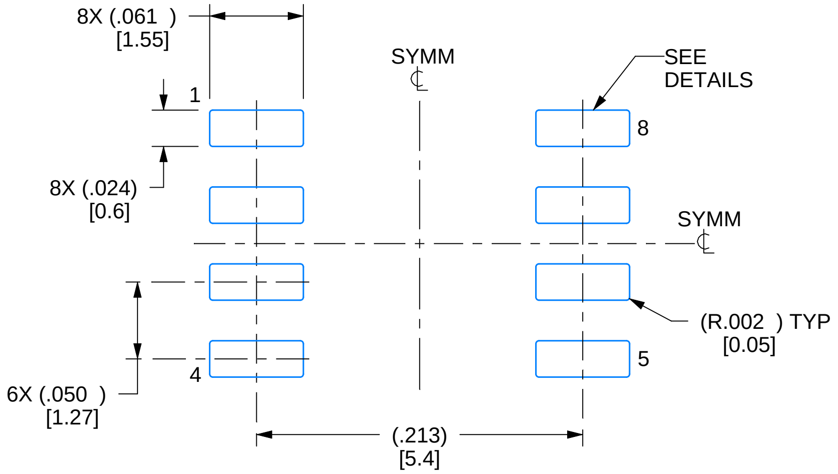


4214825/C 02/2019

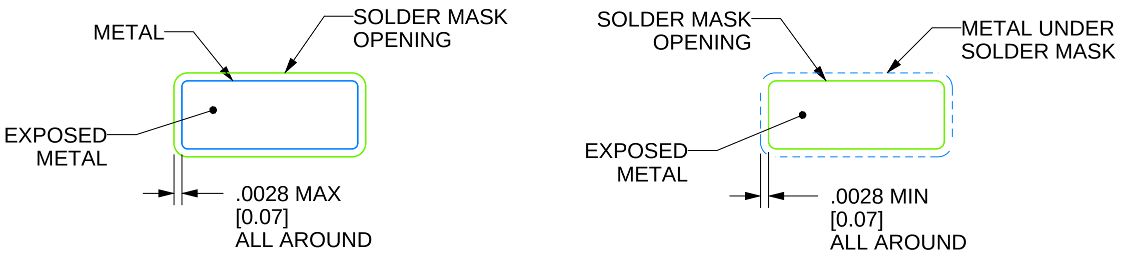
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



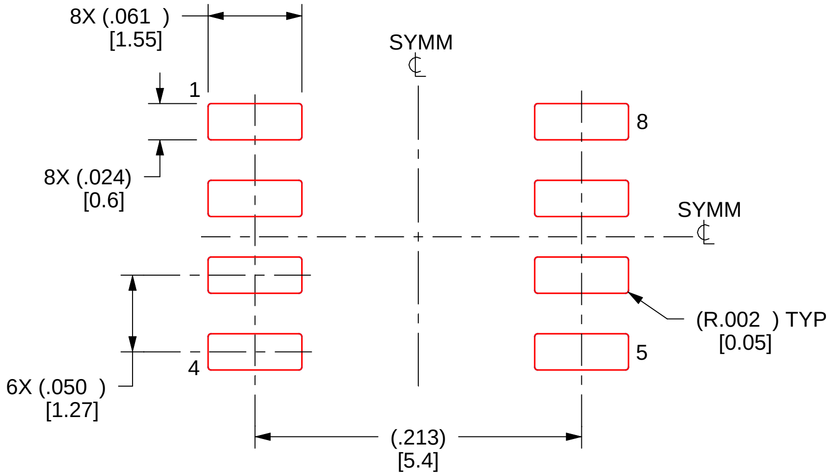
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

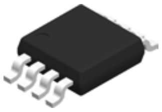


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

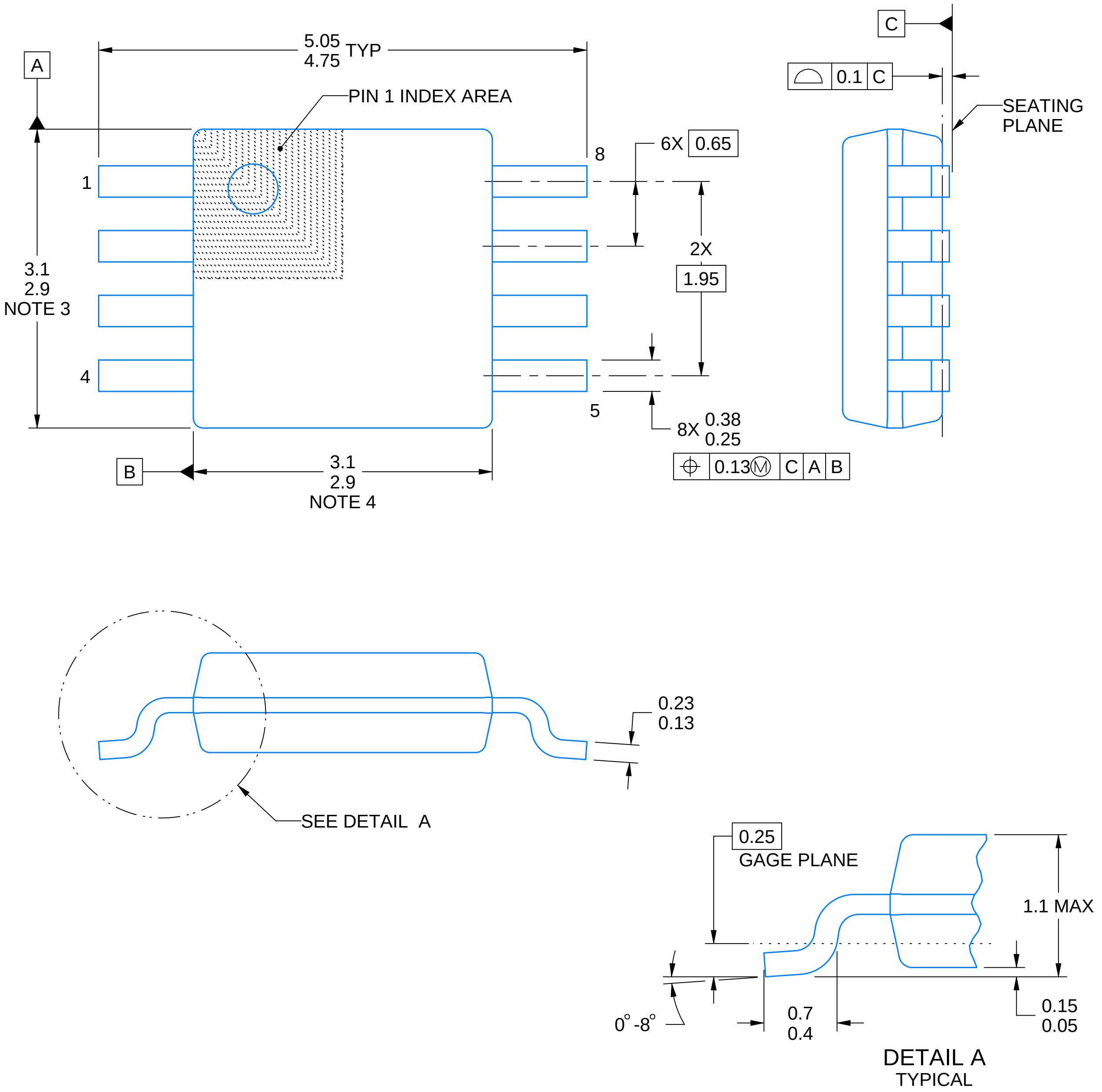
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

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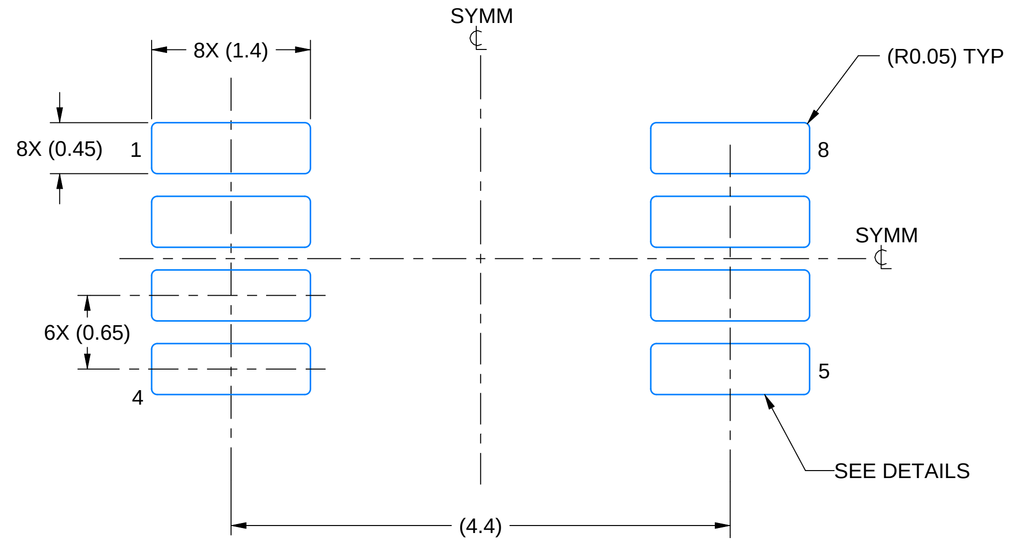
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK
DEFINED
(PREFERRED)

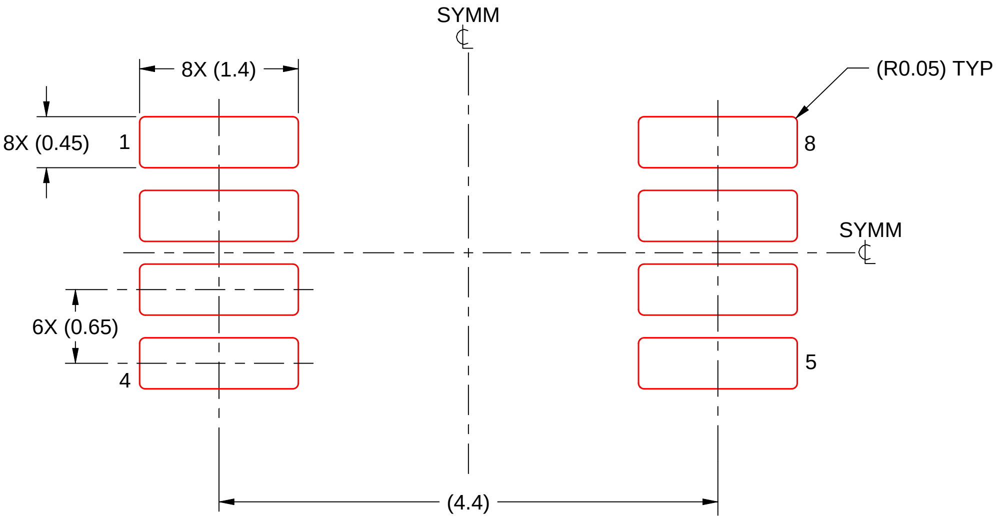
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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