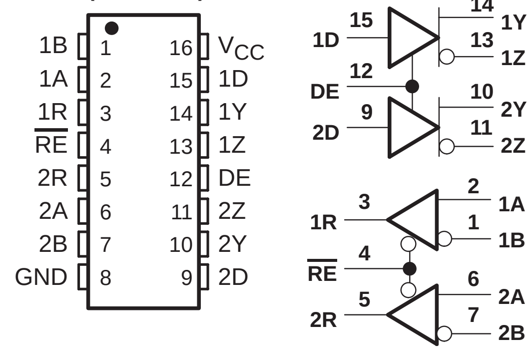
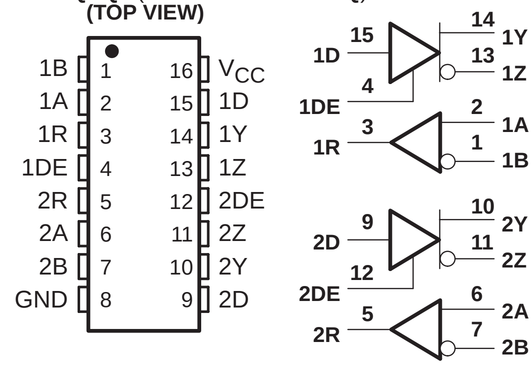
- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Low-Voltage Differential 50-Ω Line Drivers and Receivers**
- **Signaling Rates up to 500 Mbps**
- **Bus-Terminal ESD Exceeds 12 kV**
- **Operates From a Single 3.3 V Supply**
- **Low-Voltage Differential Signaling With Typical Output Voltages of 340 mV With a 50-Ω Load**
- **Valid Output With as Little as 50-mV Input Voltage Difference**
- **Propagation Delay Times**
  - **Driver: 1.7 ns Typ**
  - **Receiver: 3.7 ns Typ**
- **Power Dissipation at 200 MHz**
  - **Driver: 50 mW Typical**
  - **Receiver: 60 mW Typical**
- **LVTTL Input Levels Are 5 V Tolerant**
- **Driver Is High Impedance When Disabled or With $V_{CC}$ < 1.5 V**
- **Receiver Has Open-Circuit Fail Safe**

**SN65LVDM050QDQ1** (Marked as **LVDM050Q**)
**(TOP VIEW)**




**SN65LVDM051QDQ1** (Marked as **LVDM051Q**)
**(TOP VIEW)**




## description

The SN65LVDM050, and SN65LVDM051 are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 500 Mbps (per TIA/EIA-644 definition). These circuits are similar to TIA/EIA-644 standard compliant devices (SN65LVDS) counterparts, except that the output current of the drivers is doubled. This modification provides a minimum differential output voltage magnitude of 247 mV across a 50-Ω load simulating two transmission lines in parallel. This allows having data buses with more than one driver or with two line termination resistors. The receivers detect a voltage difference of 50 mV with up to 1 V of ground potential difference between a transmitter and receiver.

The intended application of these devices and signaling techniques is point-to-point and multipoint, baseband data transmission over a controlled impedance media of approximately 100 Ω of characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables.

## description (continued)

The SN65LVDM050Q and SN65LVDM051Q are characterized for operation from −40°C to 125°C. Additionally, Q1 suffixed parts are qualified in accordance with AEC-Q100 stress test qualification for integrated circuits.

**AVAILABLE OPTIONS†**

| $T_A$ | PACKAGE‡ SMALL OUTLINE (D) |
|---|---|
| −40°C to 125°C | SN65LVDM050QDQ1 |
| | SN65LVDM051QDQ1 |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

**NOTE:**
The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application-specific characteristics.

### Function Tables

**SN65LVDM050 and SN65LVDM051 RECEIVER**

| INPUTS | | OUTPUT |
|---|---|---|
| $V_{ID} = V_A - V_B$ | $\overline{RE}$ | R |
| $V_{ID} \geq 50$ mV | L | H |
| −50 MV < $V_{ID}$ < 50 mV | L | ? |
| $V_{ID} \leq -50$ mV | L | L |
| Open | L | H |
| X | H | Z |

H = high level, L = low level, Z = high impedance, X = don’t care

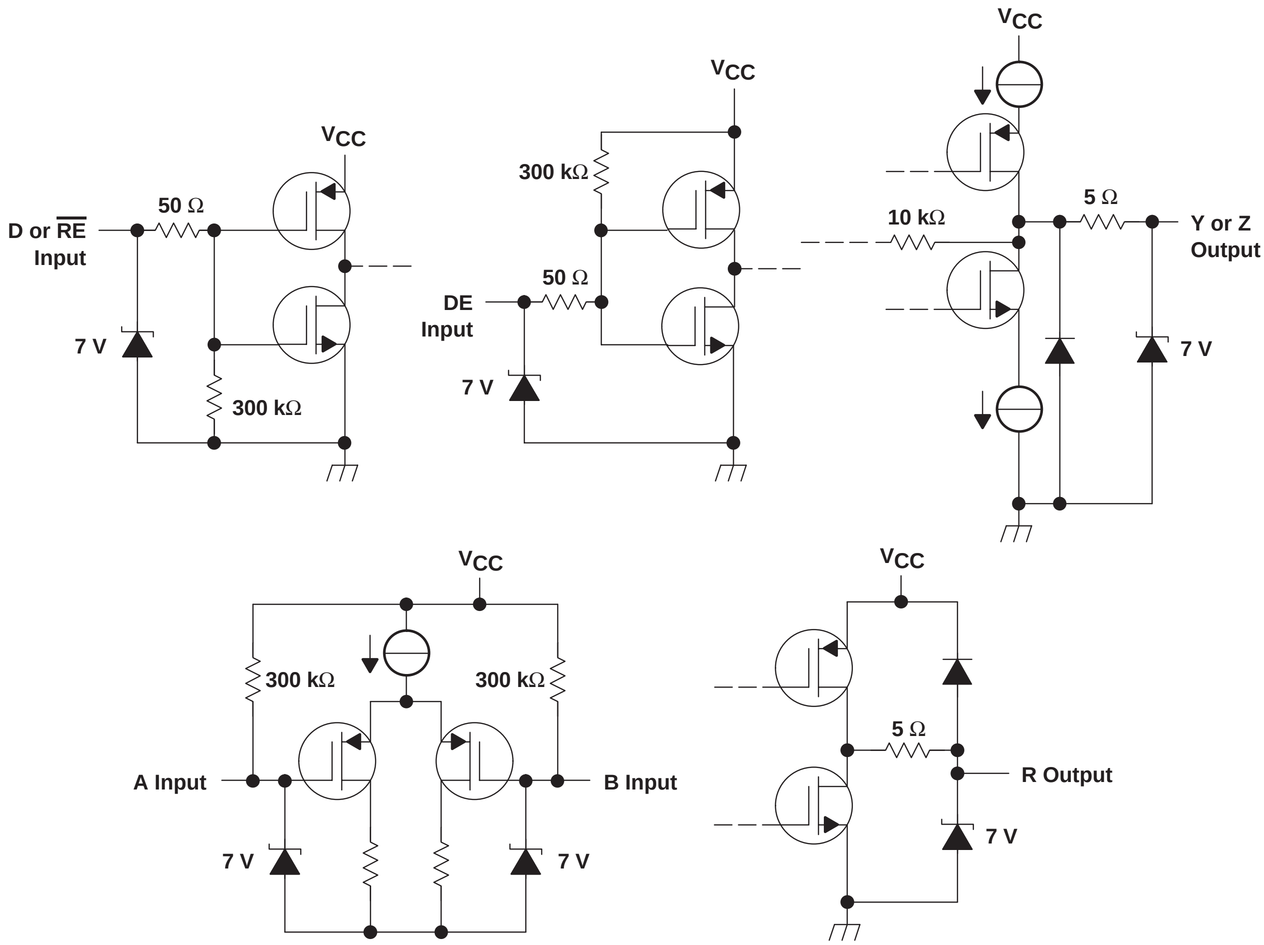
### Function Tables (Continued)

**SN65LVDM050 and SN65LVDM051 DRIVER**

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| D | DE | Y | Z |
| L | H | L | H |
| H | H | H | L |
| Open | H | L | H |
| X | L | Z | Z |

H = high level, L = low level, Z = high impedance, X = don’t care

## equivalent input and output schematic diagrams



## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −0.5 V to 4 V
Voltage range (D, R, DE, $\overline{RE}$) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −0.5 V to 6 V
Voltage range (Y, Z, A, and B) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −0.5 V to 4 V
Electrostatic discharge: Y, Z, A, B , and GND (see Note 2) . . . . . . . . . . . . . . . . . . CLass 3, A:12 kV, B:600 V
All . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . Class 3, A:7 kV, B:500 V
Continuous power dissipation . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . see dissipation rating table
Storage temperature range . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 250°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$‡ | $T_A = 85°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|
| D(8) | 635 mW | 5.1 mW/°C | 330 mW | — |
| D(14) | 987 mW | 7.9 mW/°C | 513 mW | — |
| D(16) | 1110 mW | 8.9 mW/°C | 577 mW | 223 mW |
| DGK | 424 mW | 3.4 mW/°C | 220 mW | — |
| PW (14) | 736 mW | 5.9 mW/°C | 383 mW | — |
| PW (16) | 839 mW | 6.7 mW/°C | 437 mW | — |

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 3 | 3.3 | 3.6 | V |
| High-level input voltage, $V_{IH}$ | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | | | 0.8 | V |
| Magnitude of differential input voltage, $\|V_{ID}\|$ | 0.1 | | 0.6 | V |
| Common-mode input voltage, $V_{IC}$ (see Figure 6) | $\frac{\|V_{ID}\|}{2}$ | | $2.4 - \frac{\|V_{ID}\|}{2}$ | V |
| | | | $V_{CC}-0.8$ | |
| Operating free-air temperature, $T_A$ | −40 | | 125 | °C |

## device electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current | SN65LVDM050 | Drivers and receivers enabled, no receiver loads, driver $R_L = 50\ \Omega$ | | 19 | 27 | mA |
| | | | Drivers enabled, receivers disabled, $R_L = 50\ \Omega$ | | 16 | 24 | |
| | | | Drivers disabled, receivers enabled, no loads | | 4 | 6 | |
| | | | Disabled | | 0.5 | 1 | |
| | | SN65LVDM051 | Drivers enabled, no receiver loads, driver $R_L = 50\ \Omega$ | | 19 | 27 | mA |
| | | | Drivers disabled, No loads | | 4 | 6 | |

† All typical values are at 25°C and with a 3.3 V supply.

## driver electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\|V_{OD}\|$ | Differential output voltage magnitude | | $R_L = 50\ \Omega$, See Figure 1 and Figure 2 | 247 | 340 | 454 | mV |
| $\Delta\|V_{OD}\|$ | Change in differential output voltage magnitude between logic states | | | −50 | | 50 | |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | | See Figure 3 | 1.125 | 1.2 | 1.375 | V |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage between logic states | | | −50 | | 50 | mV |
| $V_{OC(PP)}$ | Peak-to-peak common-mode output voltage | | | | 50 | | mV |
| $I_{IH}$ | High-level input current | DE | $V_{IH} = 5$ V | | −0.5 | −20 | µA |
| | | D | | | 2 | 20 | |
| $I_{IL}$ | Low-level input current | DE | $V_{IL} = 0.8$ V | | −0.5 | −10 | µA |
| | | D | | | 2 | 10 | |
| $I_{OS}$ | Short-circuit output current | | $V_{OY}$ or $V_{OZ} = 0$ V | | 7 | 10 | mA |
| | | | $V_{OD} = 0$ V | | 7 | 10 | |
| $I_{OZ}$ | High-impedance output current | | $V_{OD} = 600$ mV | | | ±1 | µA |
| | | | $V_O = 0$ V or $V_{CC}$ | | | ±1 | |
| $I_{O(OFF)}$ | Power-off output current | | $V_{CC} = 0$ V, $V_O = 3.6$ V | | | ±1.5 | µA |
| $C_{IN}$ | Input capacitance | | | | 3 | | pF |

## receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going differential input voltage threshold | See Figure 4 and Table 1 | | | 50 | mV |
| $V_{IT-}$ | Negative-going differential input voltage threshold | | −50 | | | |
| $V_{OH}$ | High-level output voltage | $I_{OH} = -8$ mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL} = 8$ mA | | | 0.4 | V |
| $I_I$ | Input current (A or B inputs) | $V_I = 0$ | −2 | −11 | −20 | µA |
| | | $V_I = 2.4$ V | −1.2 | −3 | | |
| $I_{I(OFF)}$ | Power-off input current (A or B inputs) | $V_{CC} = 0$ | | | ±20 | µA |
| $I_{IH}$ | High-level input current (enables) | $V_{IH} = 5$ V | | | 10 | µA |
| $I_{IL}$ | Low-level input current (enables) | $V_{IL} = 0.8$ V | | | 10 | µA |
| $I_{OZ}$ | High-impedance output current | $V_O = 0$ or 5 V | | | ±10 | µA |
| $C_I$ | Input capacitance | | | 5 | | pF |

† All typical values are at 25°C and with a 3.3-V supply.

## driver switching characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $R_L$ = 50Ω, $C_L$ = 10 pF, See Figure 5 | | 1.7 | 3 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 1.7 | 3 | ns |
| $t_r$ | Differential output signal rise time | | | 0.6 | 1.2 | ns |
| $t_f$ | Differential output signal fall time | | | 0.6 | 1.2 | ns |
| $t_{sk(p)}$ | Pulse skew ($\|t_{pHL} - t_{pLH}\|$) | | | 750 | | ps |
| $t_{sk(o)}$ | Channel-to-channel output skew‡ | | | 100 | | ps |
| $t_{sk(pp)}$ | Part-to-part skew§ | | | | 1 | ns |
| $t_{PZH}$ | Propagation delay time, high-impedance-to-high-level output | See Figure 6 | | 6 | 10 | ns |
| $t_{PZL}$ | Propagation delay time, high-impedance-to-low-level output | | | 6 | 10 | ns |
| $t_{PHZ}$ | Propagation delay time, high-level-to-high-impedance output | | | 4 | 10 | ns |
| $t_{PLZ}$ | Propagation delay time, low-level-to-high-impedance output | | | 5 | 10 | ns |

† All typical values are at 25°C and with a 3.3-V supply.
‡ $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.
§ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

## receiver switching characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 10 pF, See Figure 7 | | 3.7 | 4.5 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 3.7 | 4.5 | ns |
| $t_{sk(p)}$ | Pulse skew ($\|t_{pHL} - t_{pLH}\|$) | | | 0.1 | | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew | | | 0.2 | | ns |
| $t_{sk(pp)}$ | Part-to-part skew‡ | | | | 1 | ns |
| $t_r$ | Output signal rise time | $C_L$ = 10 pF, See Figure 7 | | 0.7 | 1.5 | ns |
| $t_f$ | Output signal fall time | | | 0.9 | 1.5 | ns |
| $t_{PZH}$ | Propagation delay time, high-level-to-high-impedance output | See Figure 8 | | 2.5 | | ns |
| $t_{PZL}$ | Propagation delay time, low-level-to-low-impedance output | | | 2.5 | | ns |
| $t_{PHZ}$ | Propagation delay time, high-impedance-to-high-level output | | | 7 | | ns |
| $t_{PLZ}$ | Propagation delay time, low-impedance-to-high-level output | | | 4 | | ns |

† All typical values are at 25°C and with a 3.3-V supply.
‡ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

## PARAMETER MEASUREMENT INFORMATION

### driver

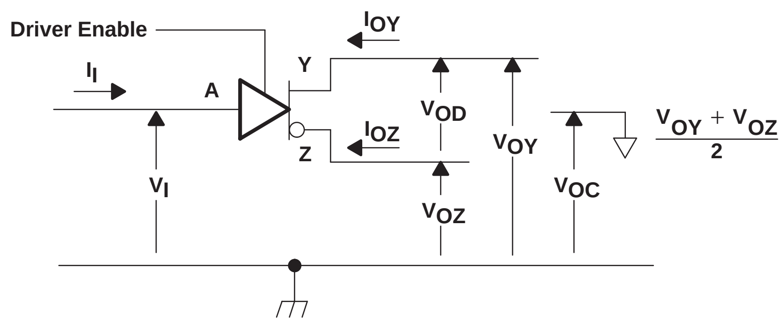
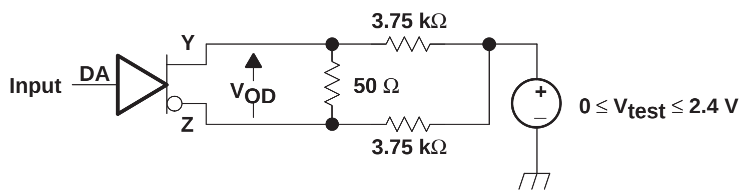
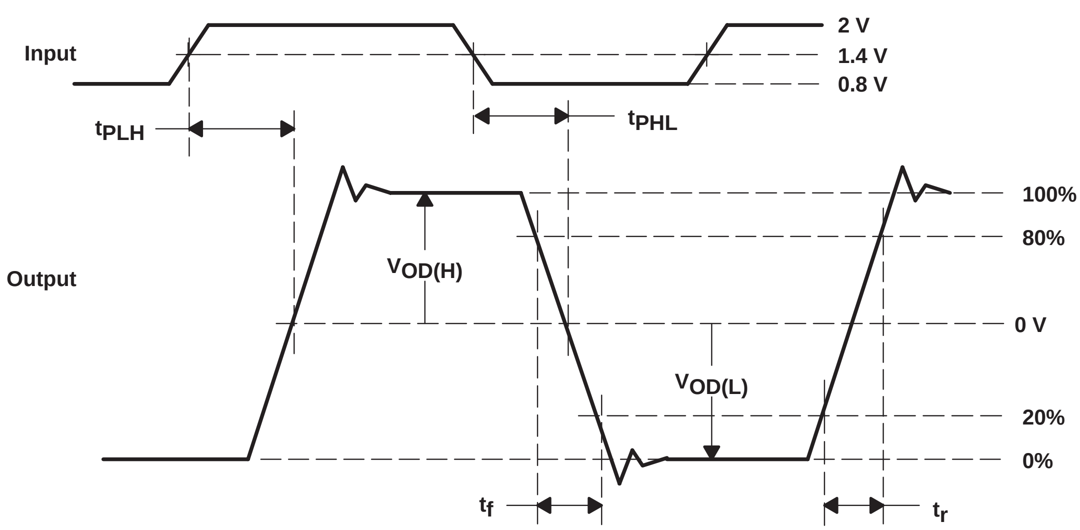



**Figure 1. Driver Voltage and Current Definitions**



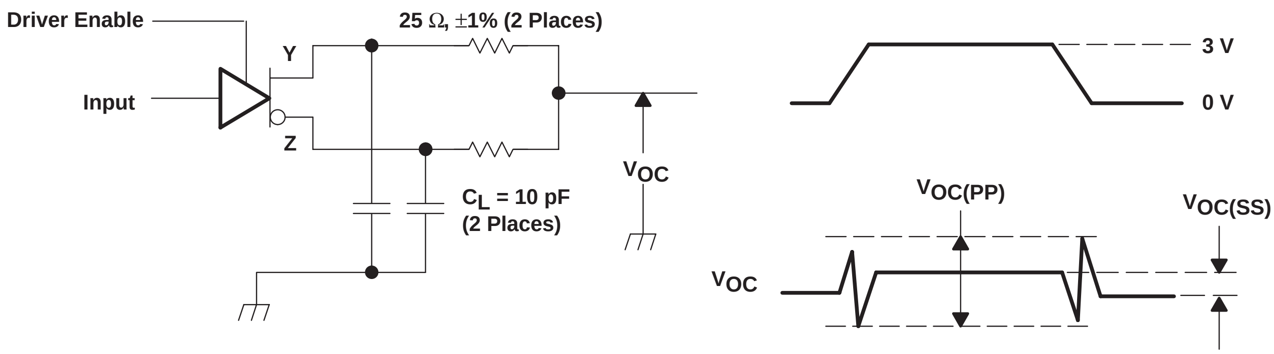




NOTE A: All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . $C_L$ includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

**Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal**

## PARAMETER MEASUREMENT INFORMATION

### driver (continued)




NOTE A: All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . $C_L$ includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a −3 dB bandwidth of at least 300 MHz.

**Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage**

## PARAMETER MEASUREMENT INFORMATION

### receiver

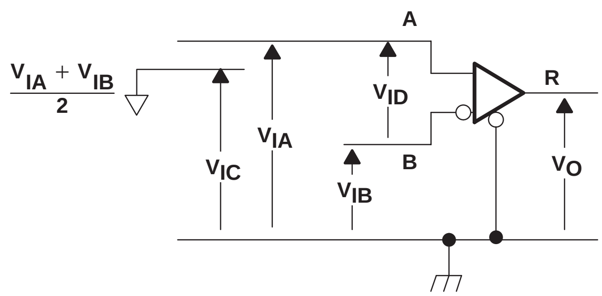



**Figure 4. Receiver Voltage Definitions**

**Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages**

| APPLIED VOLTAGES (V) | | RESULTING DIFFERENTIAL INPUT VOLTAGE (mV) | RESULTING COMMON-MODE INPUT VOLTAGE (V) |
|---|---|---|---|
| $V_{IA}$ | $V_{IB}$ | $V_{ID}$ | $V_{IC}$ |
| 1.225 | 1.175 | 50 | 1.2 |
| 1.175 | 1.225 | −50 | 1.2 |
| 2.375 | 2.325 | 50 | 2.35 |
| 2.325 | 2.375 | −50 | 2.35 |
| 0.05 | 0 | 50 | 0.05 |
| 0 | 0.05 | −50 | 0.05 |
| 1.5 | 0.9 | 600 | 1.2 |
| 0.9 | 1.5 | −600 | 1.2 |
| 2.4 | 1.8 | 600 | 2.1 |
| 1.8 | 2.4 | −600 | 2.1 |
| 0.6 | 0 | 600 | 0.3 |
| 0 | 0.6 | −600 | 0.3 |

## PARAMETER MEASUREMENT INFORMATION

### driver

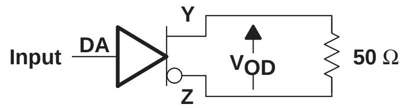
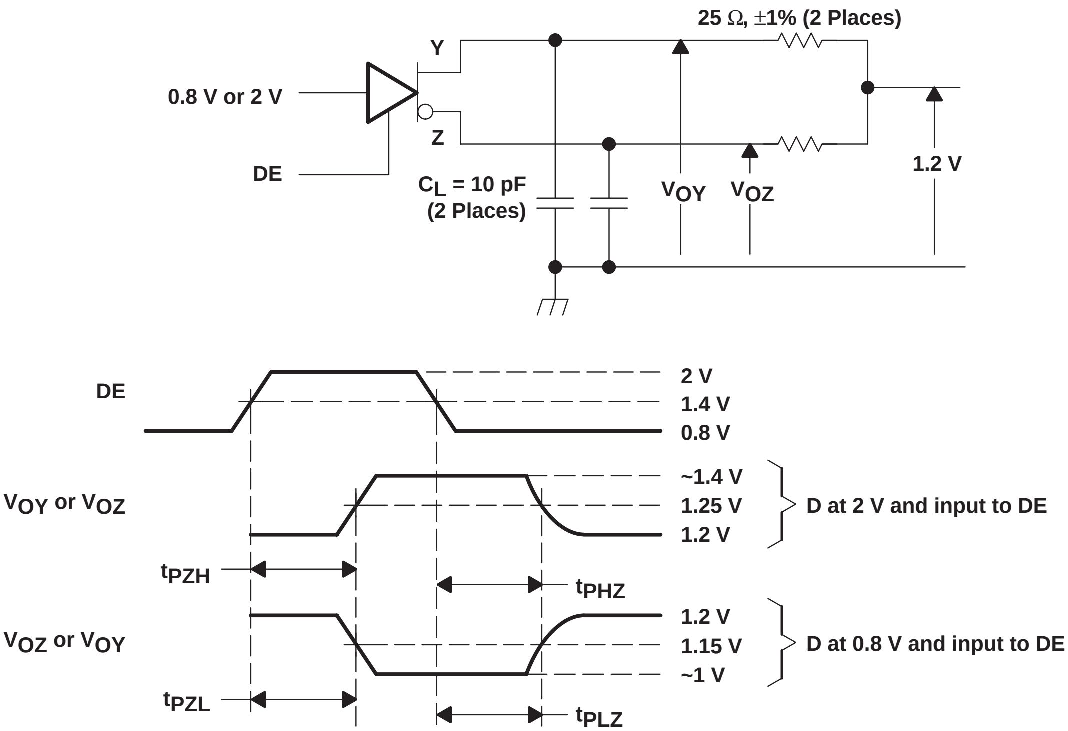



Figure 5. Timing Test Circuit

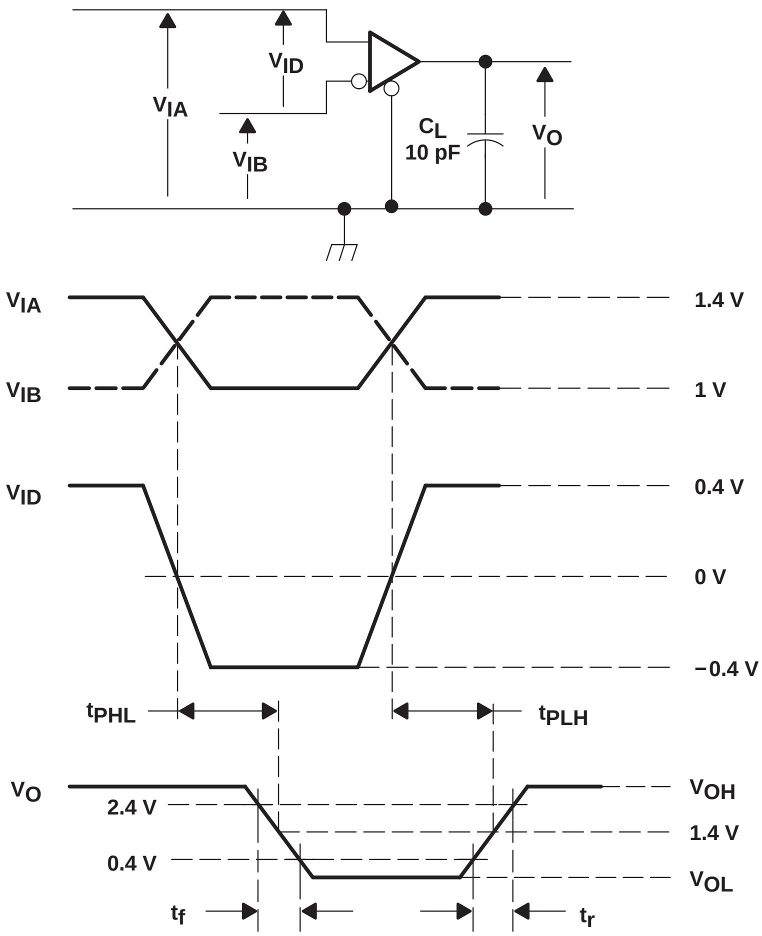



NOTE A: All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f$ ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . $C_L$ includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 6. Enable and Disable Time Circuit and Definitions

## PARAMETER MEASUREMENT INFORMATION

### receiver

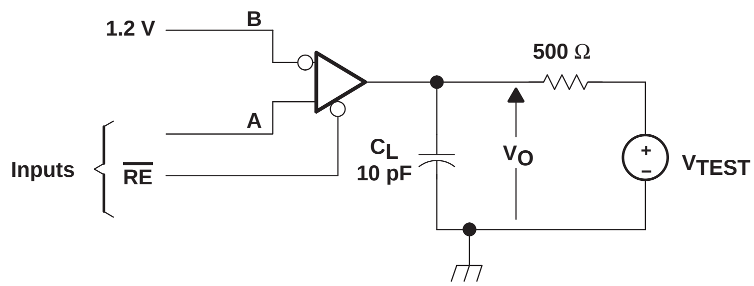



NOTE A: All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. $C_L$ includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

**Figure 7. Timing Test Circuit and Waveforms**

## PARAMETER MEASUREMENT INFORMATION

### receiver (continued)




NOTE A: All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. $C_L$ includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

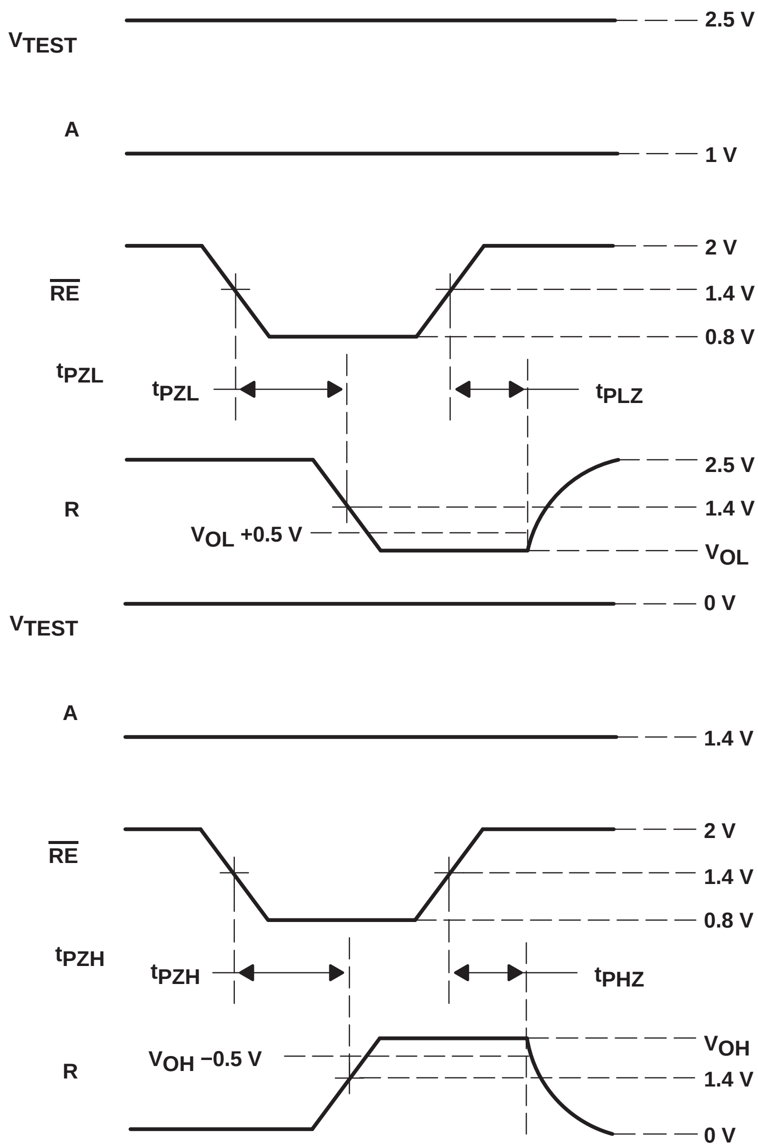



**Figure 8. Enable/Disable Time Test Circuit and Waveforms**

## TYPICAL CHARACTERISTICS

**COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE**

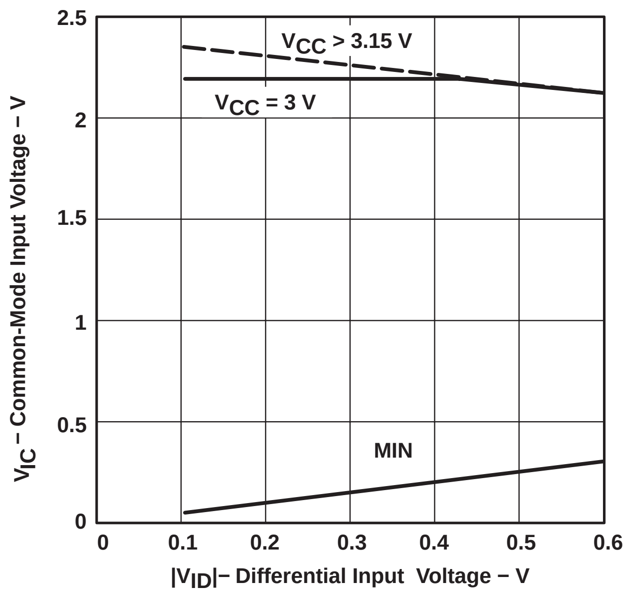



**Figure 9**

**DRIVER LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

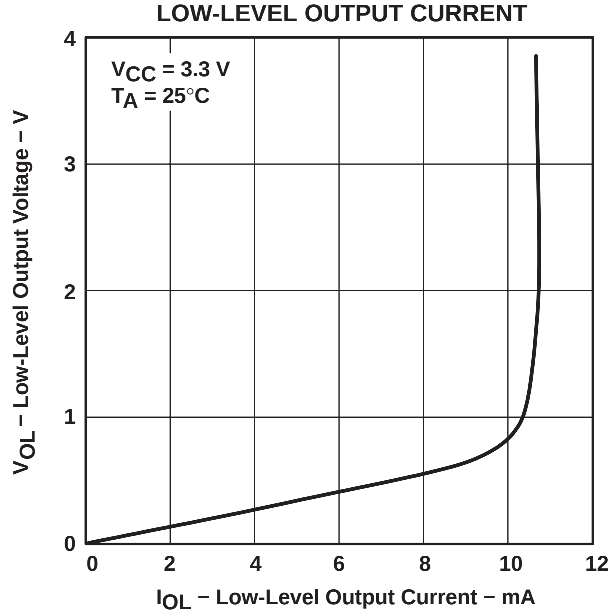



**Figure 10**

**DRIVER HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

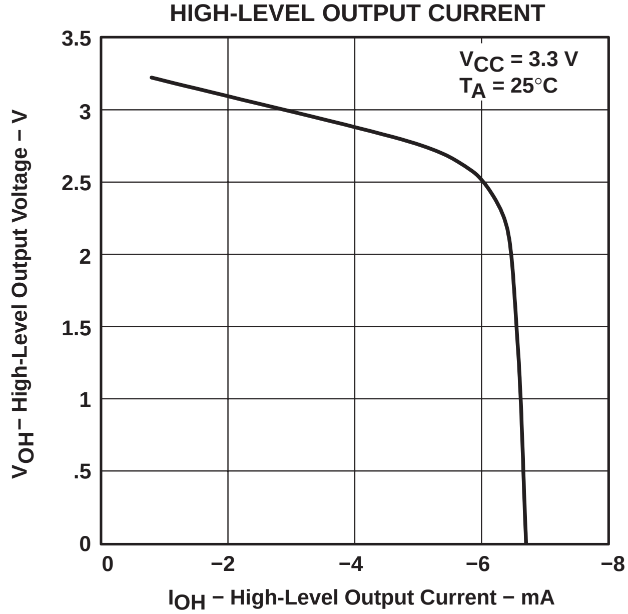



**Figure 11**

## TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

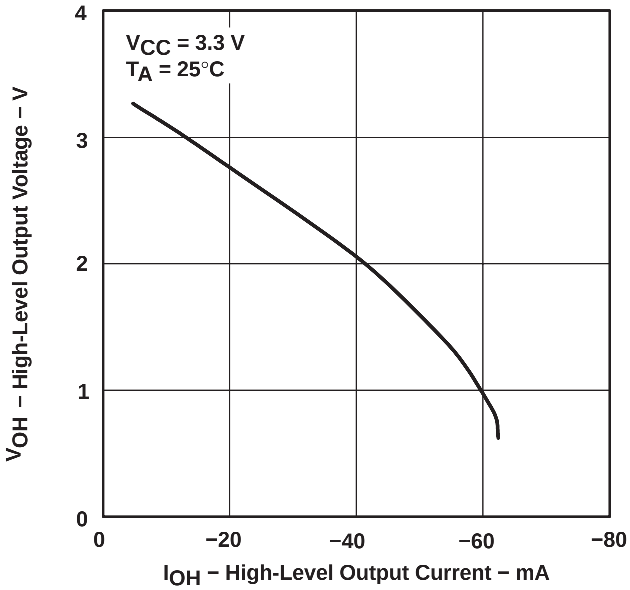



Figure 12

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

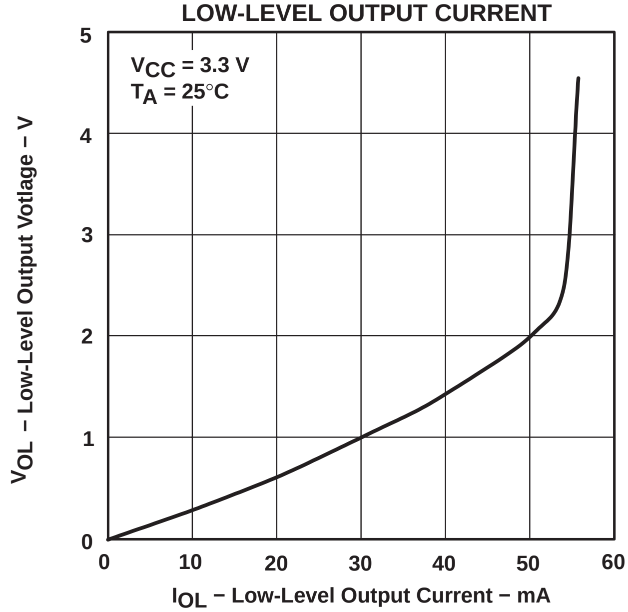



Figure 13

DRIVER
HIGH-TO-LOW LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

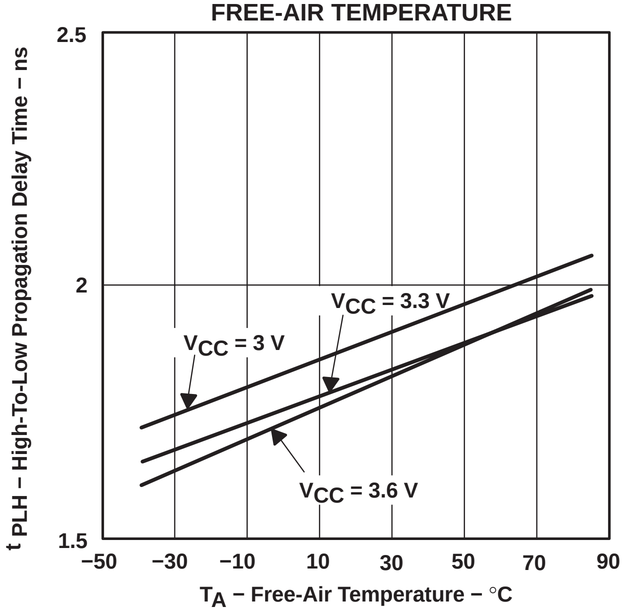



Figure 14

DRIVER
LOW-TO-HIGH LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

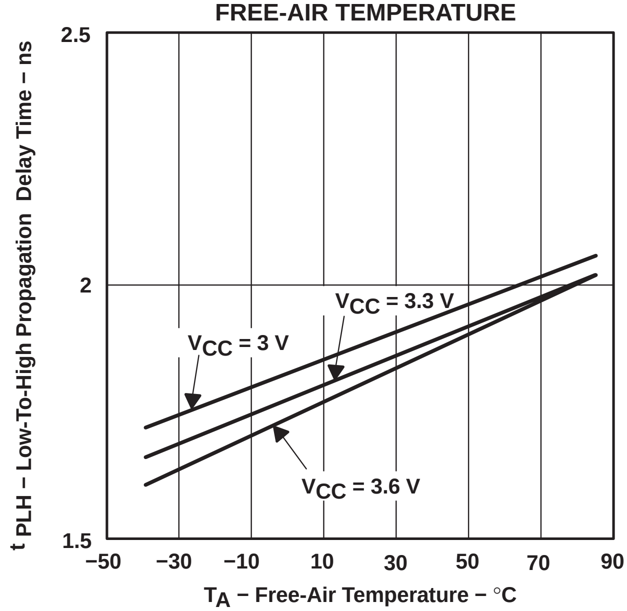



Figure 15

## TYPICAL CHARACTERISTICS

RECEIVER
HIGH-TO-LOW LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

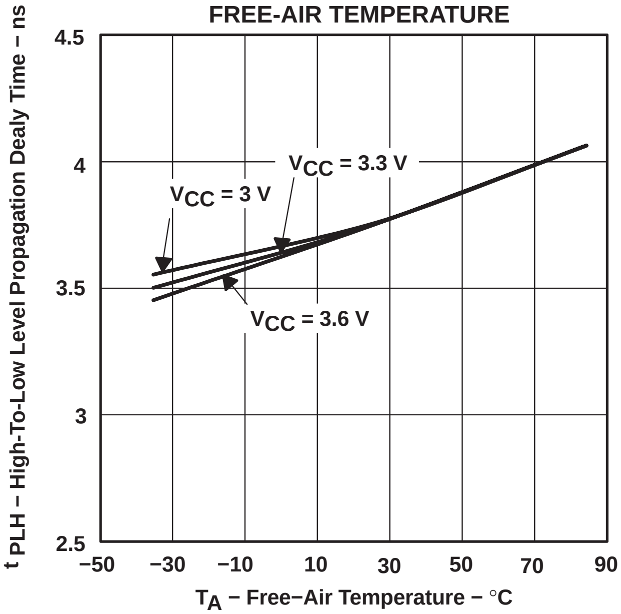



Figure 16

RECEIVER
LOW-TO-HIGH LEVEL PROPAGATION DELAY TIME
vs
FREE−AIR TEMPERATURE

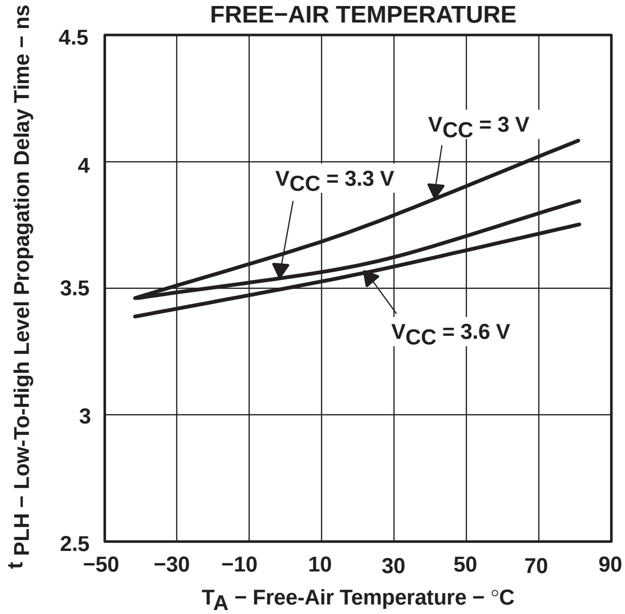



Figure 17

## APPLICATION INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission. Ground differences are less than 1 V with a low common-mode output and balanced interface for very low noise emissions. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers maintain ECL speeds without the power and dual supply requirements.

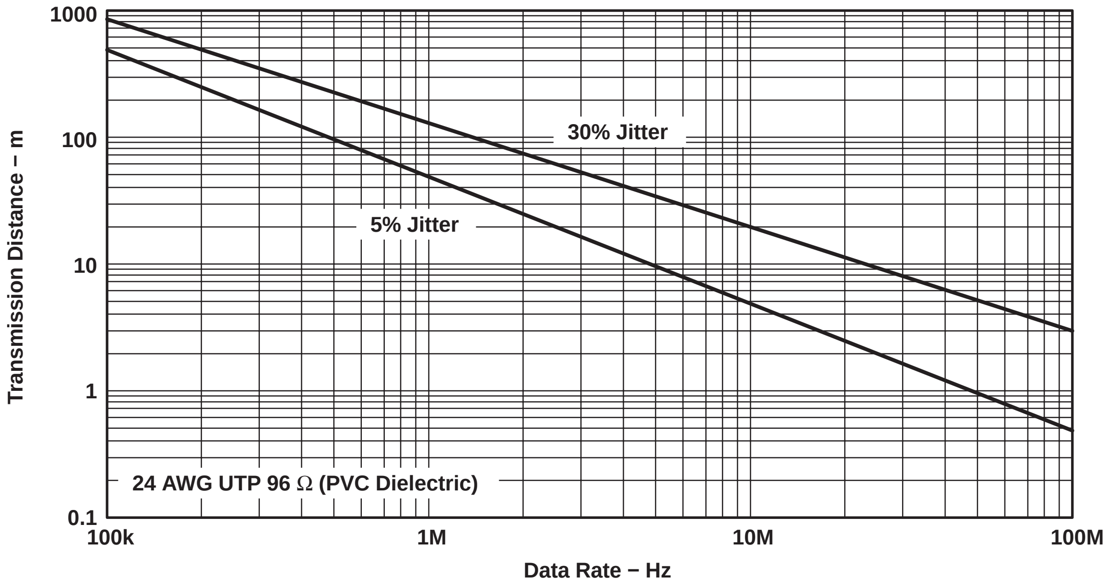



**Figure 18. Data Transmission Distance Versus Rate**

## APPLICATION INFORMATION

### fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between −50 mV and 50 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different, however, in how it handles the open-input circuit situation.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near $V_{CC}$ through 300-kΩ resistors as shown in Figure 18. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level, regardless of the differential input voltage.

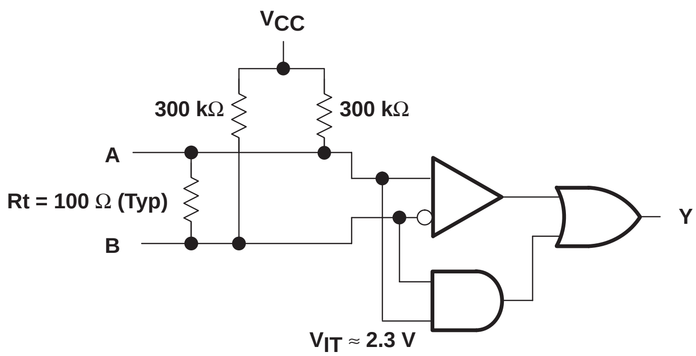



**Figure 19. Open-Circuit Fail Safe of the LVDS Receiver**

It is only under these conditions that the output of the receiver is valid with less than a 50-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN65LVDM050QDG4Q1 | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM050Q |
| SN65LVDM050QDG4Q1.B | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM050Q |
| SN65LVDM050QDQ1 | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM050Q |
| SN65LVDM050QDQ1.B | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM050Q |
| SN65LVDM050QDRG4Q1 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM050Q |
| SN65LVDM050QDRG4Q1.B | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM050Q |
| SN65LVDM050QDRQ1 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM050Q |
| SN65LVDM050QDRQ1.B | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM050Q |
| SN65LVDM051QDQ1 | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM051Q |
| SN65LVDM051QDQ1.B | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM051Q |
| SN65LVDM051QDRG4Q1 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM051Q |
| SN65LVDM051QDRG4Q1.B | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM051Q |
| SN65LVDM051QDRQ1 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM051Q |
| SN65LVDM051QDRQ1.B | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVDM051Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN65LVDM050-Q1, SN65LVDM051-Q1 :**

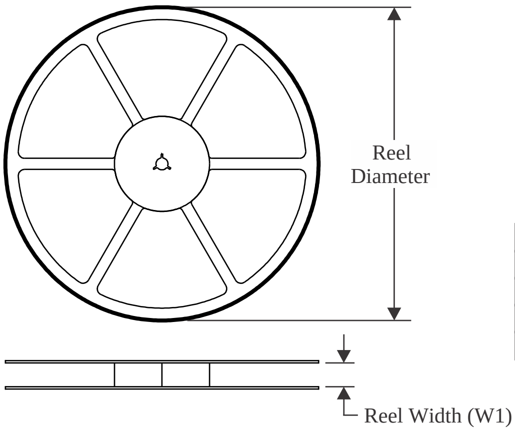
- Catalog : SN65LVDM050, SN65LVDM051

NOTE: Qualified Version Definitions:

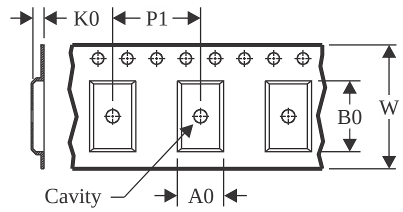
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

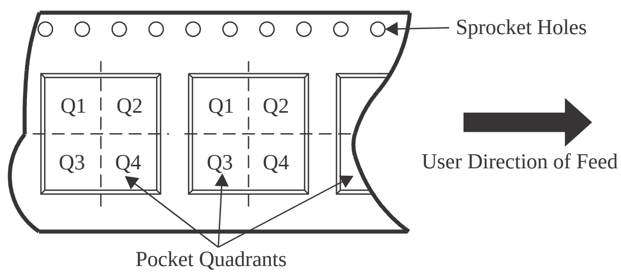



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

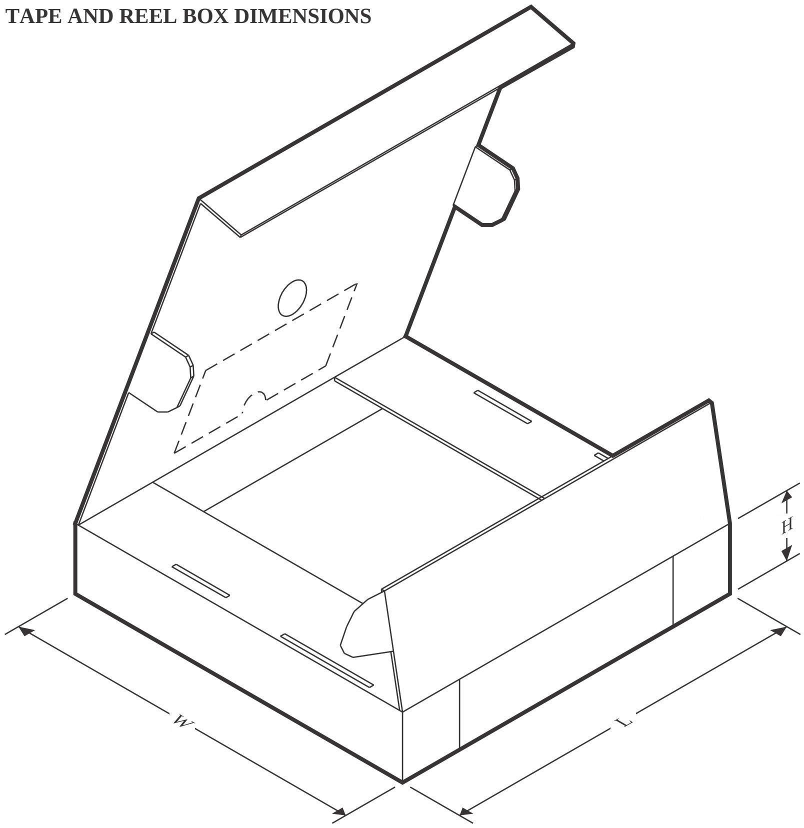
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LVDM050QDRQ1 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN65LVDM051QDRG4Q1 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN65LVDM051QDRQ1 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

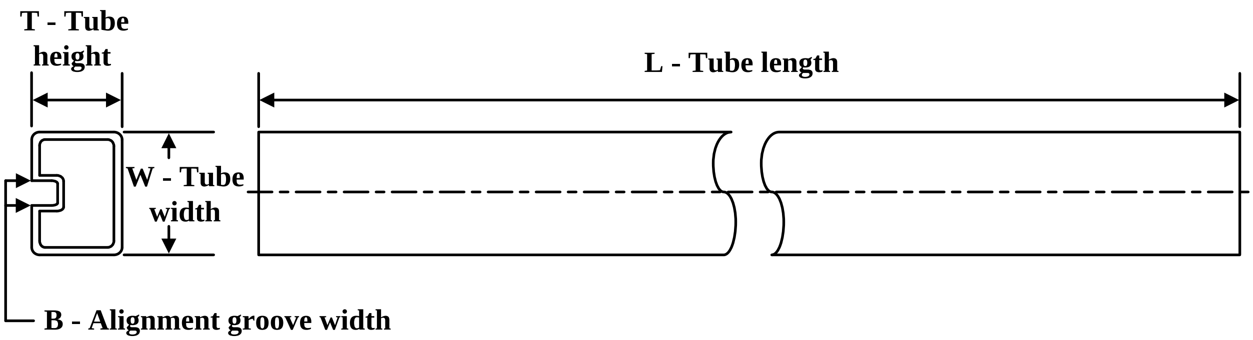
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65LVDM050QDRQ1 | SOIC | D | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| SN65LVDM051QDRG4Q1 | SOIC | D | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| SN65LVDM051QDRQ1 | SOIC | D | 16 | 2500 | 350.0 | 350.0 | 43.0 |

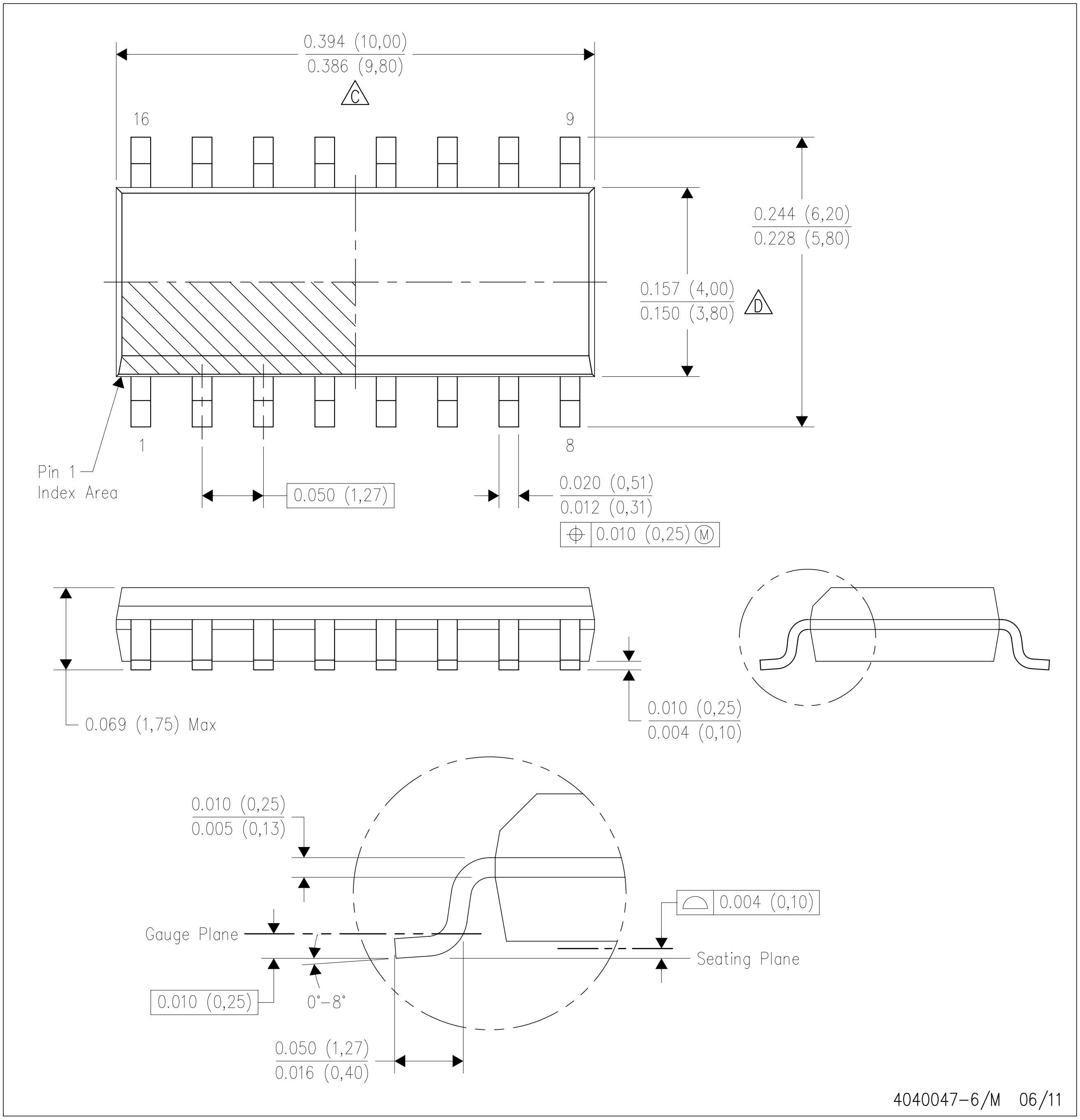
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN65LVDM050QDG4Q1 | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |
| SN65LVDM050QDG4Q1.B | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |
| SN65LVDM050QDQ1 | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |
| SN65LVDM050QDQ1.B | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |
| SN65LVDM051QDQ1 | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |
| SN65LVDM051QDQ1.B | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AC.

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