TEXAS INSTRUMENTS

SN65LVDS387, SN75LVDS387, SN65LVDS389
SN75LVDS389, SN65LVDS391, SN75LVDS391

SLLS362G – SEPTEMBER 1999 – REVISED JANUARY 2016

SNx5LVDS3xx High-Speed Differential Line Drivers

1 Features

- Four ('391), Eight ('389), or Sixteen ('387) Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard
- Designed for Signaling Rates Up to 630 Mbps With Very Low Radiation (EMI)
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load
- Propagation Delay Times Less Than 2.9 ns
- Output Skew Is Less Than 150 ps
- Part-to-Part Skew Is Less Than 1.5 ns
- 35-mW Total Power Dissipation in Each Driver Operating at 200 MHz
- Driver Is High-Impedance When Disabled or With V_{CC} < 1.5 V
- SN65' Version Bus-Pin ESD Protection Exceeds 15 kV
- Packaged in Thin Shrink Small-Outline Package With 20-mil Pin Pitch
- Low-Voltage TTL (LVTTL) Logic Inputs Are 5-V Tolerant

2 Applications

- Wireless Infrastructure
- Telecom Infrastructure
- Printer

3 Description

This family of 4, 8, and 16 differential line drivers implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the 16 current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVDS387	TSSOP (64)	17.00 mm × 6.10 mm
SN75LVDS387	TSSOP (38)	9.70 mm × 4.40 mm
SN65LVDS389	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm
SN75LVDS389	TSSOP (64)	17.00 mm × 6.10 mm
SN65LVDS391	TSSOP (38)	9.70 mm × 4.40 mm
SN75LVDS391	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

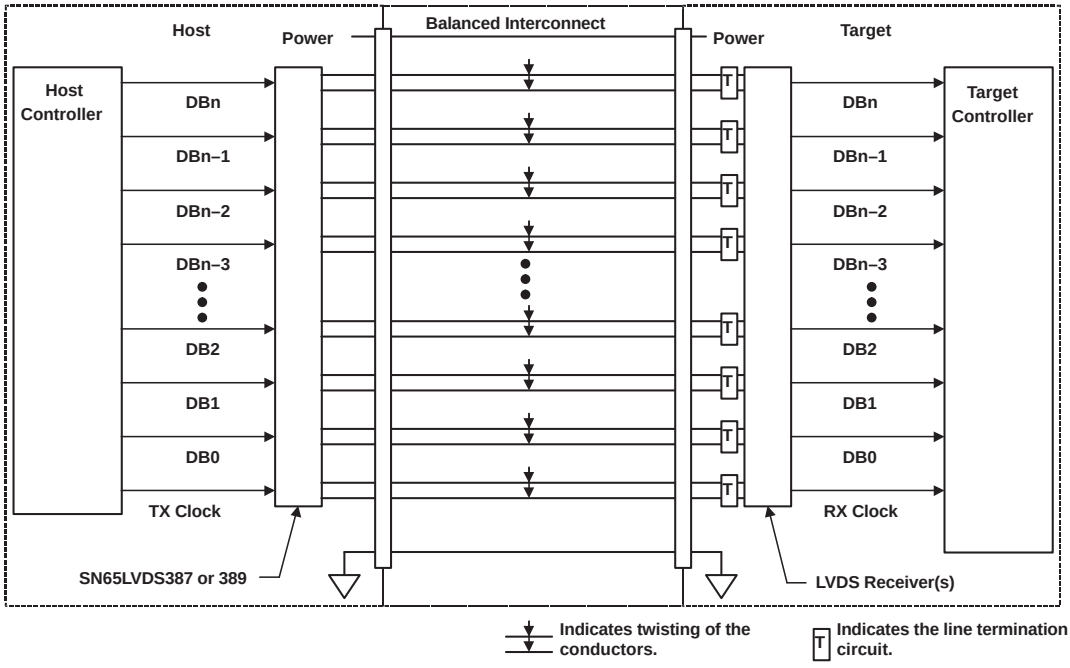


Table of Contents

4 Revision History

Changes from Revision F (December 2014) to Revision G **Page**

- Changed C3A From: pin 20 To: pin 21 in the *Pin Functions: SNx5LVDS387* table ... 5

Changes from Revision E (November 2004) to Revision F **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Description (Continued)

When disabled, the driver outputs are high-impedance. Each driver input (A) and enable (EN) have an internal pulldown that will drive the input to a low level when open-circuited.

The SN65LVDS387, SN65LVDS389, and SN65LVDS391 devices are characterized for operation from –40°C to 85°C. The SN75LVDS387, SN75LVDS389, and SN75LVDS391 devices are characterized for operation from 0°C to 70°C.

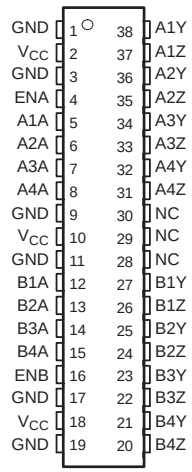
6 Device Options

PART NUMBER(1)	TEMPERATURE RANGE	NUMBER OF DRIVERS	BUS-PIN ESD
SN65LVDS387DGG	–40°C to 85°C	16	15 kV
SN75LVDS387DGG	0°C to 70°C	16	4 kV
SN65LVDS389DBT	–40°C to 85°C	8	15 kV
SN75LVDS389DBT	0°C to 70°C	8	4 kV
SN65LVDS391D	–40°C to 85°C	4	15 kV
SN75LVDS391D	0°C to 70°C	4	4 kV
SN65LVDS391PW	–40°C to 85°C	4	15 kV
SN75LVDS391PW	0°C to 70°C	4	4 kV

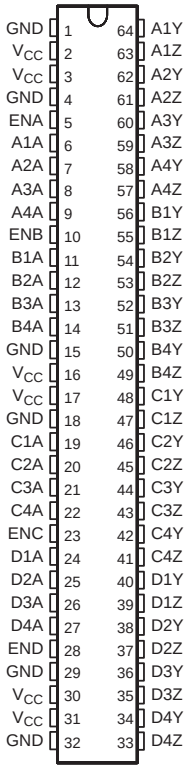
(1) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (for example, SN65LVDS387DGGR).

7 Pin Configuration and Functions

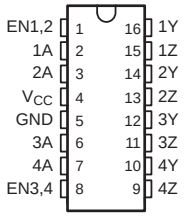
'LVDS389
DBT PACKAGE
(TOP VIEW)



'LVDS387
DGG PACKAGE
(TOP VIEW)



'LVDS391
D OR PW PACKAGE
(TOP VIEW)



Pin Functions: SNx5LVDS391

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	4	–	Supply voltage
GND	5	–	Ground
1A	2	I	LVTTL input signal
1Y	16	O	Differential (LVDS) non-inverting output
1Z	15	O	Differential (LVDS) inverting output
2A	3	I	LVTTL input signal
2Y	14	O	Differential (LVDS) non-inverting output
2Z	13	O	Differential (LVDS) inverting output
3A	6	I	LVTTL input signal
3Y	12	O	Differential (LVDS) non-inverting output
3Z	11	O	Differential (LVDS) inverting output
4A	7	I	LVTTL input signal
4Y	10	O	Differential (LVDS) non-inverting output
4Z	9	O	Differential (LVDS) inverting output
EN1,2	1	I	Enable for channels 1 and 2
EN3,4	8	I	Enable for channels 3 and 4

Pin Functions: SNx5LVDS389

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	2, 10, 18	–	Supply voltage
GND	1, 3, 9, 11, 17, 19	–	Ground
A1A	5	I	LVTTL input signal
A1Y	38	O	Differential (LVDS) non-inverting output
A1Z	37	O	Differential (LVDS) inverting output
A2A	6	I	LVTTL input signal
A2Y	36	O	Differential (LVDS) non-inverting output
A2Z	35	O	Differential (LVDS) inverting output
A3A	7	I	LVTTL input signal
A3Y	34	O	Differential (LVDS) non-inverting output
A3Z	33	O	Differential (LVDS) inverting output
A4A	8	I	LVTTL input signal
A4Y	32	O	Differential (LVDS) non-inverting output
A4Z	31	O	Differential (LVDS) inverting output
B1A	12	I	LVTTL input signal
B1Y	27	O	Differential (LVDS) non-inverting output
B1Z	26	O	Differential (LVDS) inverting output
B2A	13	I	LVTTL input signal
B2Y	25	O	Differential (LVDS) non-inverting output
B2Z	24	O	Differential (LVDS) inverting output
B3A	14	I	LVTTL input signal
B3Y	23	O	Differential (LVDS) non-inverting output
B3Z	22	O	Differential (LVDS) inverting output
B4A	15	I	LVTTL input signal
B4Y	21	O	Differential (LVDS) non-inverting output
B4B	20	O	Differential (LVDS) inverting output

Pin Functions: SNx5LVDS389 (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
ENA	4	I	Enable for channel A
ENB	16	I	Enable for channel B
NC	28, 29, 30	–	No connection

Pin Functions: SNx5LVDS387

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	2, 3, 16, 17, 30, 31	–	Supply voltage
GND	1, 4, 15, 18, 29, 32	–	Ground
A1A	6	I	LVTTL input signal
A1Y	64	O	Differential (LVDS) non-inverting output
A1Z	73	O	Differential (LVDS) inverting output
A2A	7	I	LVTTL input signal
A2Y	62	O	Differential (LVDS) non-inverting output
A2Z	61	O	Differential (LVDS) inverting output
A3A	8	I	LVTTL input signal
A3Y	60	O	Differential (LVDS) non-inverting output
A3Z	59	O	Differential (LVDS) inverting output
A4A	9	I	LVTTL input signal
A4Y	58	O	Differential (LVDS) non-inverting output
A4Z	57	O	Differential (LVDS) inverting output
B1A	11	I	LVTTL input signal
B1Y	56	O	Differential (LVDS) non-inverting output
B1Z	55	O	Differential (LVDS) inverting output
B2A	12	I	LVTTL input signal
B2Y	54	O	Differential (LVDS) non-inverting output
B2Z	53	O	Differential (LVDS) inverting output
B3A	13	I	LVTTL input signal
B3Y	52	O	Differential (LVDS) non-inverting output
B3Z	51	O	Differential (LVDS) inverting output
B4A	14	I	LVTTL input signal
B4Y	50	O	Differential (LVDS) non-inverting output
B4B	49	O	Differential (LVDS) inverting output
C1A	19	I	LVTTL input signal
C1Y	48	O	Differential (LVDS) non-inverting output
C1Z	47	O	Differential (LVDS) inverting output
C2A	20	I	LVTTL input signal
C2Y	46	O	Differential (LVDS) non-inverting output
C2Z	45	O	Differential (LVDS) inverting output
C3A	21	I	LVTTL input signal
C3Y	44	O	Differential (LVDS) non-inverting output
C3Z	43	O	Differential (LVDS) inverting output
C4A	22	I	LVTTL input signal
C4Y	42	O	Differential (LVDS) non-inverting output
C4Z	41	O	Differential (LVDS) inverting output

Pin Functions: SNx5LVDS387 (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
D1A	24	I	LVTTL input signal
D1Y	40	O	Differential (LVDS) non-inverting output
D1Z	39	O	Differential (LVDS) inverting output
D2A	25	I	LVTTL input signal
D2Y	38	O	Differential (LVDS) non-inverting output
D2Z	37	O	Differential (LVDS) inverting output
D3A	26	I	LVTTL input signal
D3Y	36	O	Differential (LVDS) non-inverting output
D3Z	35	O	Differential (LVDS) inverting output
D4A	27	I	LVTTL input signal
D4Y	34	O	Differential (LVDS) non-inverting output
B4B	33	O	Differential (LVDS) inverting output
ENA	5	I	Enable for channel A
ENB	10	I	Enable for channel B
ENC	23	I	Enable for channel C
END	26	I	Enable for channel D

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range, V_{CC} (2)		–0.5	4	V
Input voltage range	Inputs	–0.5	6	V
	Y or Z	–0.5	4	V
Continuous power dissipation		See *Thermal Information*		
Lead temperature 1.6 mm (1/16 in) from case for 10 seconds			260	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground pin.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	SN65' (Y, Z, and GND)	Class 3, A	±15000	V
			Class 3, B	±400	V
		SN75' (Y, Z, and GND)	Class 3, A	±4000	V
			Class 3, B	±400	V
Lead temperature 1.6 mm (1/16 in) from case for 10 seconds				260	°C

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
T_A	Operating free-air temperature	SN75'	0		70	°C
		SN65'	–40		85	°C

8.4 Thermal Information

THERMAL METRIC(1)	SN65LVDS387 SN75LVDS389	SN75LVDS387 SN65LVDS391	SN65LVDS389 SN75LVDS391		UNIT
	DGG	DBT	D	PW	
	64 PINS	38 PINS	16 PINS	16 PINS	
Derating Factor Above T_A = 25°C(2)	16.7	8.5	7.6	6.2	mW/°C
Power Rating: $T_A \leq$ 25°C	2094	1071	950	774	mW
Power Rating: T_A = 70°C	1342	688	608	496	
Power Rating: T_A = 85°C	1089	556	494	402	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) and with no air flow.

8.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100 Ω, See Figure 9 and Figure 10		247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states			–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 11		1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	mV
I_{CC}	Supply current	'LVDS387	Enabled, R_L = 100 Ω, V_{IN} = 0.8 V or 2 V		85	95	mA
		'LVDS389			50	70	
		'LVDS391			20	26	
		'LVDS387	Disabled, V_{IN} = 0 V or V_{CC}		0.5	1.5	
		'LVDS389			0.5	1.5	
		'LVDS391			0.5	1.3	
I_{IH}	High-level input current	V_{IH} = 2 V			3	20	µA
I_{IL}	Low-level input current	V_{IL} = 0.8 V			2	10	µA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V				±24	mA
		V_{OD} = 0 V				±12	mA
I_{OZ}	High-impedance output current	V_O = 0 V or V_{CC}				±1	µA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 2.4 V				±1	µA
C_{IN}	Input capacitance	V_I = 0.4sin(4E6πt) + 0.5 V			5		pF
C_O	Output capacitance	V_I = 0.4sin(4E6πt) + 0.5 V, Disabled			9.4		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

8.6 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 12	0.9	1.7	2.9	ns
t_{PHL}	Propagation delay time, high-to-low-level output		0.9	1.6	2.9	ns
t_r	Differential output signal rise time		0.4	0.8	1	ns
t_f	Differential output signal fall time		0.4	0.8	1	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			150	500	ps
$t_{sk(o)}$	Output skew(2)			80	150	ps
$t_{sk(pp)}$	Part-to-part skew(3)				1.5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 13		6.4	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			5.9	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			3.5	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			4.5	15	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of any two devices characterized in this data sheet when both devices operate with the same supply voltage, at the same temperature, and have the same test circuits.

8.7 Typical Characteristics

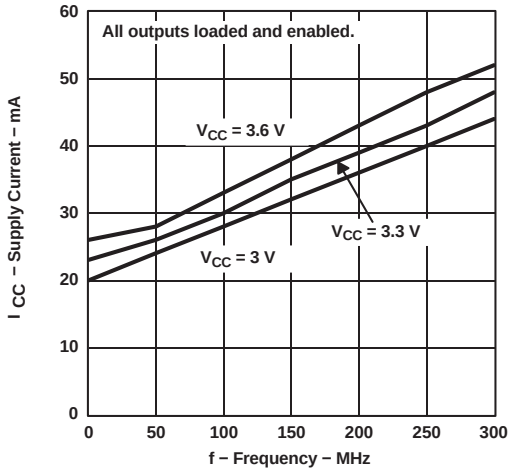


Figure 1. 'LVDS391 Supply Current vs (RMS) Switching Frequency

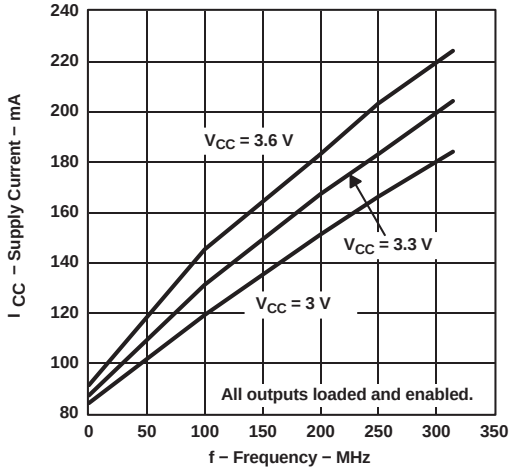


Figure 2. 'LVDS387 Supply Current (RMS) vs Switching Frequency

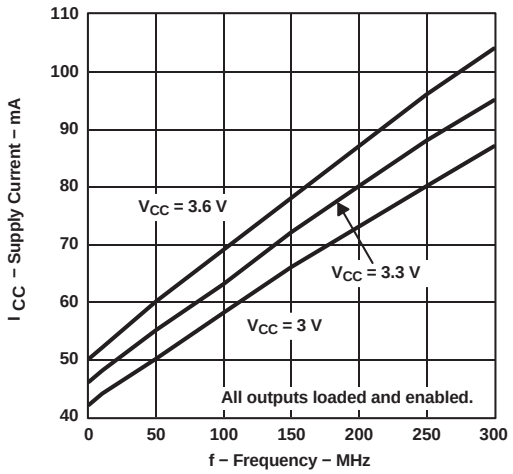


Figure 3. 'LVDS389 Supply Current (RMS) vs Switching Frequency

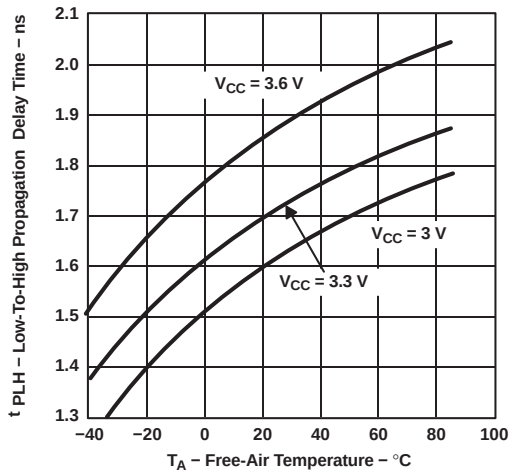


Figure 4. Low-to-High Propagation Delay Time vs Free-Air Temperature

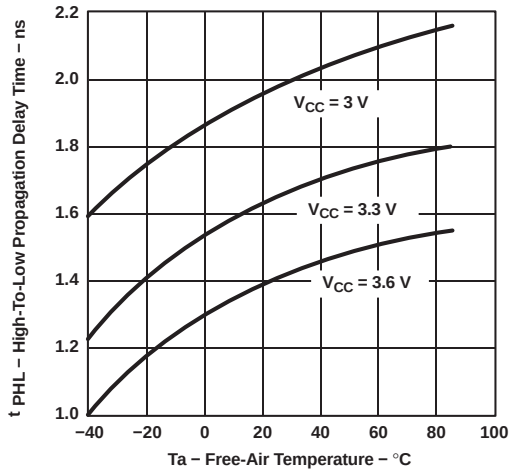


Figure 5. High-to-Low Propagation Delay Time vs Free-Air Temperature

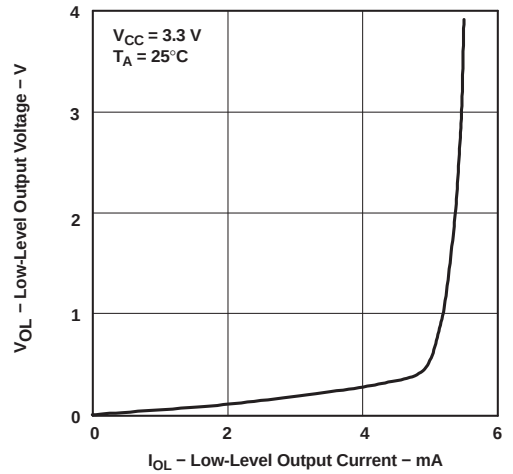


Figure 6. Low-Level Output Voltage vs Low-Level Output Current

Typical Characteristics (continued)

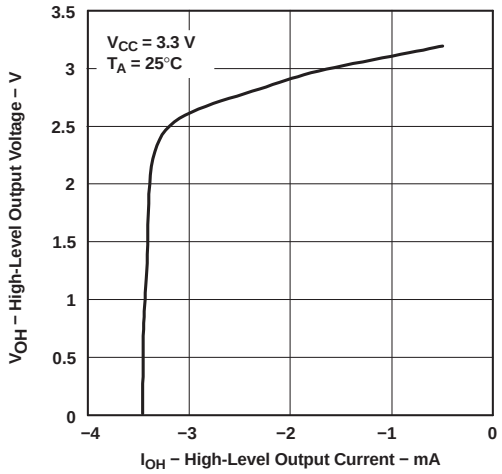


Figure 7. High-Level Output Voltage vs High-Level Output Current

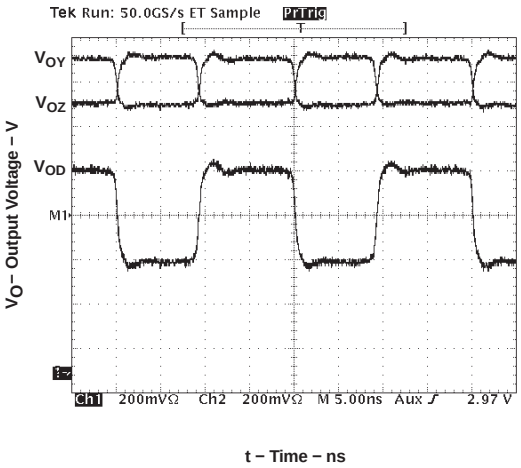


Figure 8. Output Voltage vs Time

9 Parameter Measurement Information

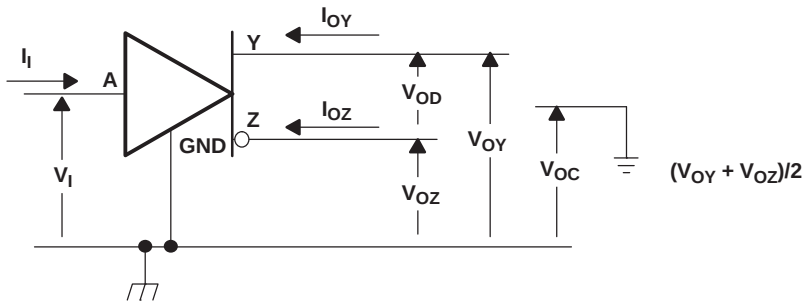


Figure 9. Voltage and Current Definitions

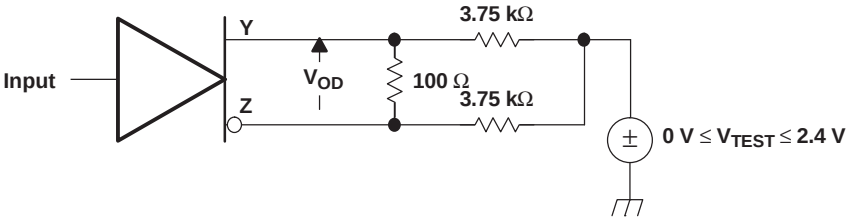
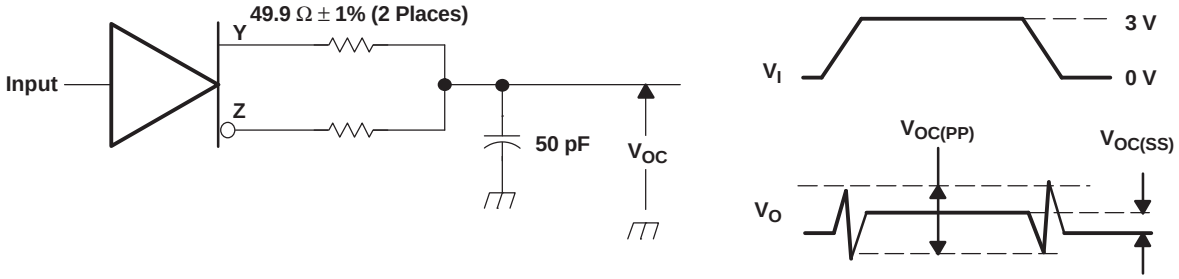


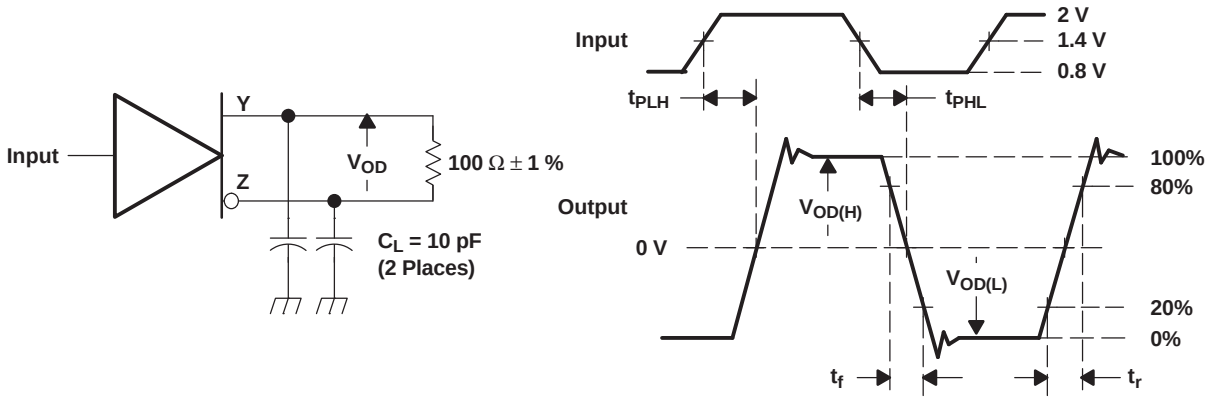
Figure 10. V_{OD} Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

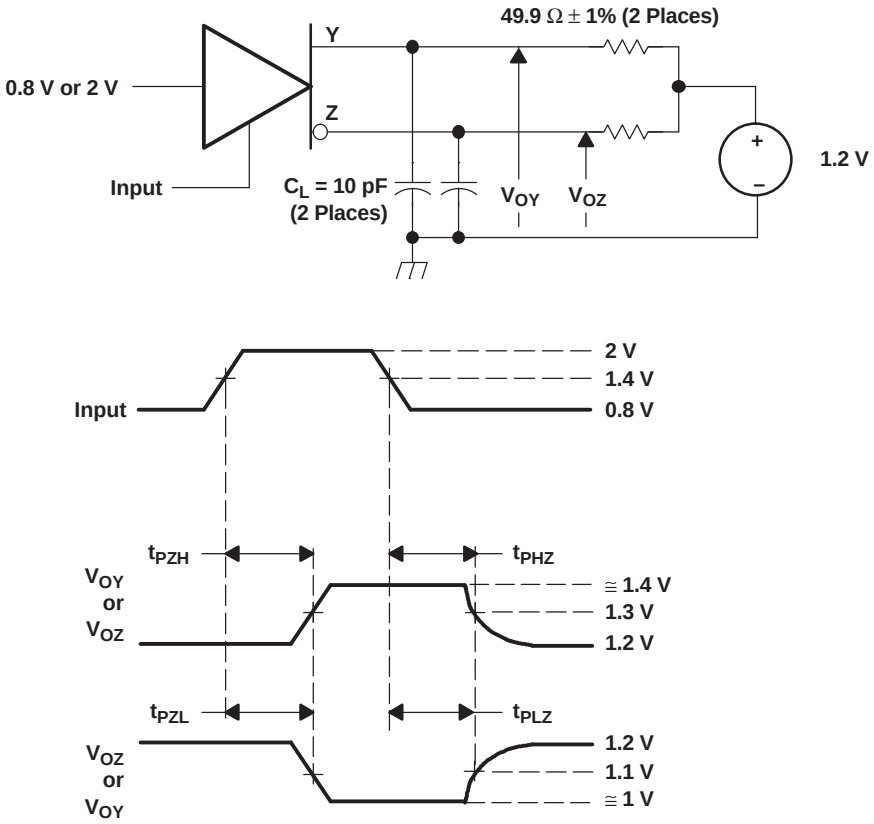
Figure 11. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

Parameter Measurement Information (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test.

Figure 12. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test.

Figure 13. Enable and Disable Time Circuit and Definitions

10 Detailed Description

10.1 Overview

The SNx5LVDSxx devices are quad-, eight-, and 16-channel LVDS line drivers. They operate from a single supply that is nominally 3.3 V, but can be as low as 3 V and as high as 3.6 V. The input signals to the SNx5LVDSxx device are LVTTL signals. The outputs of the device are differential signals complying with the LVDS standard (TIA/EIA-644A). The differential output signal operates with a signal level of 340 mV, nominally, at a common-mode voltage of 1.2 V. This low differential output voltage results in a low emitted radiated energy, which is dependent on the signal slew rate. The differential nature of the output provides immunity to common-mode coupled signals.

The SNx5LVDSxx device is intended to drive a 100-Ω transmission line. This transmission line may be a printed-circuit board (PCB) or cabled interconnect. With transmission lines, the optimum signal quality and power delivery is reached when the transmission line is terminated with a load equal to the characteristic impedance of the interconnect. Likewise, the driven 100-Ω transmission line should be terminated with a matched resistance.

10.2 Functional Block Diagram

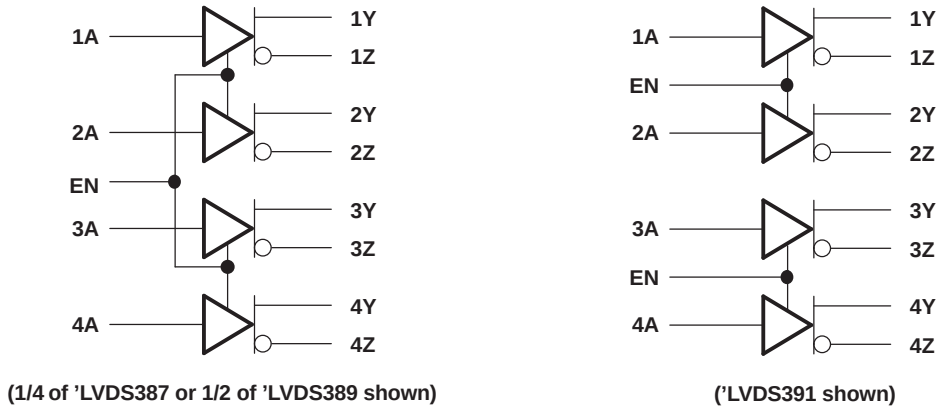


Figure 14. Logic Diagram (Positive Logic)

10.3 Feature Description

10.3.1 Driver Output Voltage and Power-On Reset

The SNx5LVDSxx driver operates and meets all the specified performance requirements for supply voltages in the range of 3.0 V to 3.6 V. When the supply voltage drops below 1.5 V (or is turning on and has not yet reached 1.5 V), power-on reset circuitry sets the driver output to a high-impedance state.

10.3.2 5-V Input Tolerance

5-V and 3.3-V TTL logic standards share the same input high-voltage and input low-voltage thresholds, namely 2.0 V and 0.8 V, respectively. Although the maximum supply voltage for the SNx5LVDSxx is 3.6 V, the driver can operate and meet all performance requirements when the input signals are as high as 5 V. This allows operation with 3.3-V TTL as well as 5-V TTL logic. 3.3-V CMOS and 5-V CMOS inputs are also allowable, although one should ensure that the duty-cycle distortion that will result from the TTL (ground-referenced) thresholds are acceptable.

10.3.3 NC Pins

NC (not connected) pins are pins where the die is not physically connected to the lead frame or package. For optimum thermal performance, a good rule of thumb is to ground the NC pins at the board level.

10.3.4 Unused Enable Pins

Unused enable pins should be tied to V_{CC} or GND as appropriate.

Feature Description (continued)

10.3.5 Driver Equivalent Schematics

The SNx5LVDSxx equivalent output schematic diagrams are shown in Figure 15. The driver input is represented by a CMOS inverter stage with a 7-V Zener diode. The input stage is high-impedance, and includes an internal pulldown to ground. If the driver input is left open, the driver input provides a low-level signal to the rest of the driver circuitry, resulting in a low-level signal at the driver output pins. The Zener diode provides ESD protection. The driver output stage is a differential pair, one half of which is shown in Figure 15. Like the input stage, the driver output includes Zener diodes for ESD protection. The schematic shows an output stage that includes a set of current sources (nominally 3.5 mA) that are connected to the output load circuit based upon the input stage signal. To the first order, the SNx5LVDSxx output stage acts a constant-current source.

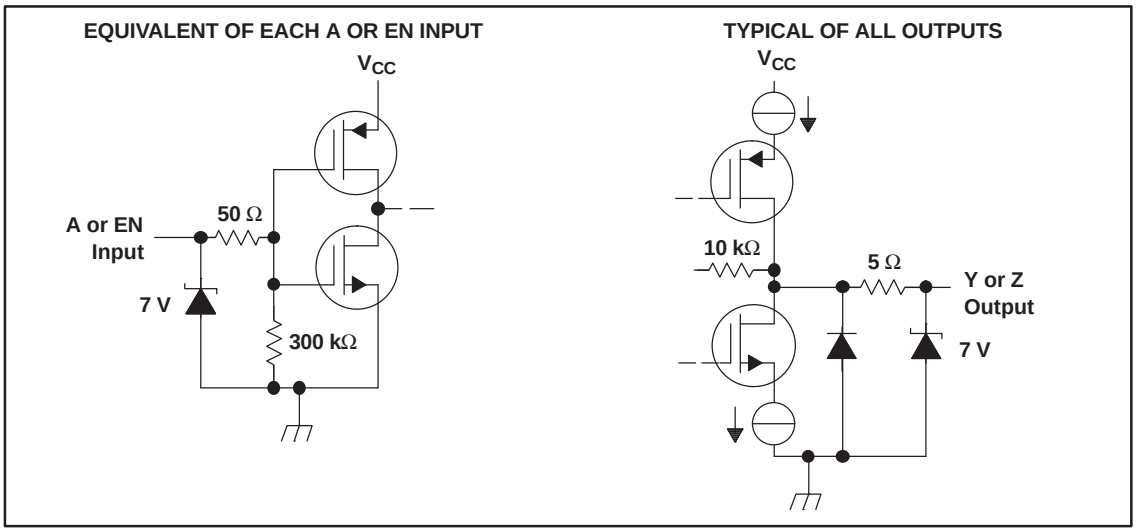


Figure 15. Equivalent Input and Output Schematic Diagrams

10.4 Device Functional Modes

Table 1 provides the truth table for the SNx5LVDSxx devices.

Table 1. Driver Function Table(1)

INPUT	ENABLE	OUTPUTS	
A	EN	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z
OPEN	H	L	H

(1) H = high-level, L = low-level, X = irrelevant, Z = high-impedance (off)

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The intended application of this device and signaling technique is for point-to-point and multidrop baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media can be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with the companion 16- or 8-channel receivers, the SN65LVDS386 or SN65LVDS388, over 200 million data transfers per second in single-edge clocked systems are possible with very little power.

NOTE

The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.

11.1.1 Signaling Rate vs Distance

The ultimate data transfer rate over a given cable or trace length involves many variables. Starting with the capabilities of this LVDS driver to reproduce a data pulse as short as 1.6 ns (a 630-Mbps signaling rate) with less than 500 ps of pulse distortion, any degradation of this pulse by the transmission media will necessarily reduce the timing margin at the receiving end of the data link.

The timing uncertainty induced by the transmission media is commonly referred to as jitter and comes from numerous sources. The characteristics of a particular transmission media can be quantified by using an eye pattern measurement such as shown in Figure 16, which shows about 340 ps of jitter or 20% of the data pulse width.

Application Information (continued)

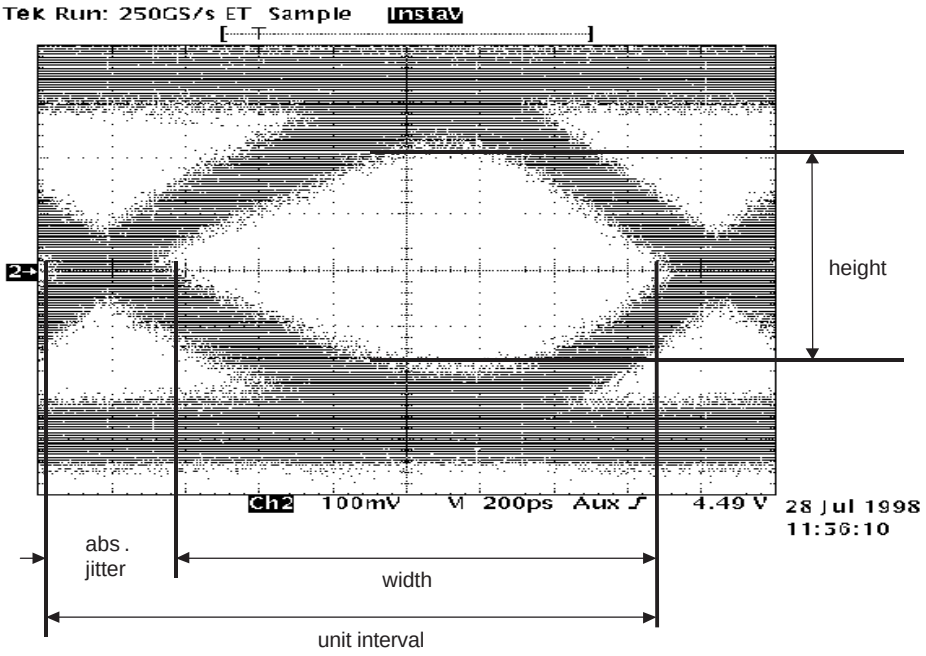


Figure 16. Typical LVDS Eye Pattern

A generally accepted range of jitter at the receiver inputs that allows data recovery is 5% to 20% of the unit interval (data pulse width). Table 2 shows the signaling rate achieved on various cables and lengths at a 5% eye pattern jitter with a typical LVDS driver.

Table 2. Signaling Rates for Various Cables for 5% Eye Pattern Jitter

LENGTH (m)	CABLE					
	A(1) (Mbps)	B(2) (Mbps)	C(3) (Mbps)	D(4) (Mbps)	E(5) (Mbps)	F(6) (Mbps)
1	240	200	240	270	180	230
5	205	210	230	250	215	230
10	180	150	195	200	145	180

(1) Cable A: CAT 3, specified up to 16 MHz, no shield, outside conductor diameter (ø) 0.52 mm
(2) Cable B: CAT 5, specified up to 100 MHz, no shield, ø 0.52 mm
(3) Cable C: CAT 5, specified up to 100 MHz, taped over all shield, ø 0.52 mm
(4) Cable D: CAT 5 (exceeding CAT 5), specified up to 300 MHz, braided over all shield plus taped individual shield for any pair, ø 0.64 mm (AWG22)
(5) Cable E: CAT 5 (exceeding CAT 5), specified up to 350 MHz, ø 0.64 mm (AWG22), no shield
(6) Cable F: CAT 5 (exceeding CAT 5), specified up to 350 MHz, *self-shielded*, ø 0.64 mm (AWG22)

During synchronous parallel transfers, skew between the data and clock lines will also reduce the timing margin. This should be accounted for in the system timing budget. Fortunately, the low output skew of this LVDS driver will generally be a small portion of this budget.

11.2 Typical Application

11.2.1 Point-to-Point Communications

The most basic application for LVDS buffers, as found in this data sheet, is for point-to-point communications of digital data, as shown in Figure 17.

Typical Application (continued)

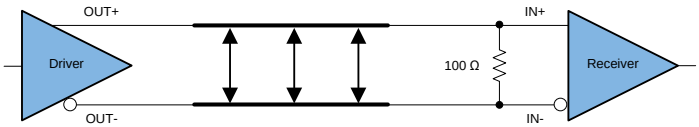


Figure 17. Point-to-Point Topology

A point-to-point communications channel has a single transmitter (driver) and a single receiver. This communications topology is often referred to as simplex. In Figure 17 the driver receives a single-ended input signal and the receiver outputs a single-ended recovered signal. The LVDS driver converts the single-ended input to a differential signal for transmission over a balanced interconnecting media of 100-Ω characteristic impedance. The conversion from a single-ended signal to an LVDS signal retains the digital data payload while translating to a signal whose features are more appropriate for communication over extended distances or in a noisy environment.

11.2.1.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	3.0 to 3.6 V
Driver Input Voltage	0.8 to 3.3 V
Driver Signaling Rate	DC to 200 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	1
Receiver Supply Voltage (V_{CCR})	3.0 to 3.6 V
Receiver Input Voltage	0 to 2.4 V
Receiver Signaling Rate	DC to 200 Mbps
Ground shift between driver and receiver	±1 V

11.2.1.2 Detailed Design Procedure

11.2.1.2.1 Driver Supply Voltage

The SNx5LVDSxx driver is operated from a single supply. The device can support operation with a supply as low as 3 V and as high as 3.6 V. The differential output voltage is nominally 340 mV over the complete output range. The minimum output voltage stays within the specified LVDS limits (247 mV to 454 mV) for the complete 3-V to 3.6-V supply range.

11.2.1.2.2 Driver Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very-low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 µF to 1000 µF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one should resort to the use of smaller capacitors (nF to µF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula according to Johnson[1], equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV; however, this figure varies depending on the noise budget available in your design. (1)

$$C_{chip} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \quad (1)$$

$$C_{LVDS} = \left(\frac{1A}{0.2V} \right) \times 200\ ps = 0.001\ \mu F \quad (2)$$

The following example lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 µF) and the value of capacitance found above (0.001 µF). You should place the smallest value of capacitance as close as possible to the chip.

Figure 18. Recommended LVDS Bypass Capacitor Layout

11.2.1.2.3 Driver Output Voltage

The SNx5LVDSxx driver output is a 1.2-V common-mode voltage, with a nominal differential output signal of 340 mV. This 340 mV is the absolute value of the differential swing (V_{OD} = |V^+ – V^-|). The peak-to-peak differential voltage is twice this value, or 680 mV.

11.2.1.2.4 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the LVDS standard, the key points which will be included here. This media may be a twisted pair, twinax, flat ribbon cable, or PCB traces.

The nominal characteristic impedance of the interconnect should be between 100 Ω and 120 Ω with variation no more than 10% (90 Ω to 132 Ω).

11.2.1.2.5 PCB Transmission Lines

As per SNLA187, Figure 19 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. Figure 19 shows examples of edge-coupled microstrips, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, S is less than 2 W, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

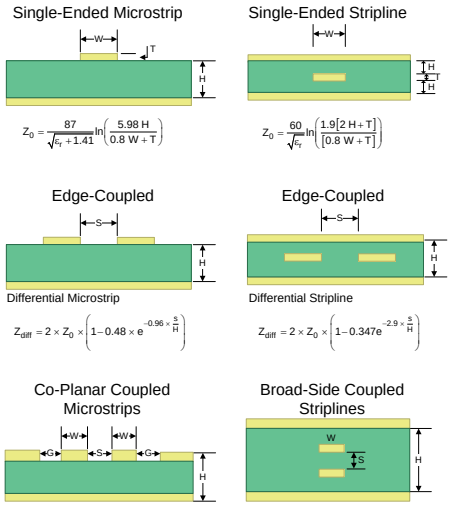


Figure 19. Controlled-Impedance Transmission Lines

11.2.1.2.6 Termination Resistor

As shown earlier, an LVDS communication channel employs a current source driving a transmission line which is terminated with a resistive load. This load serves to convert the transmitted current into a voltage at the receiver input. To ensure incident wave switching (which is necessary to operate the channel at the highest signaling rate), the termination resistance should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistance is within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistance should be between 90 Ω and 110 Ω.

The line termination resistance should be located as close as possible to the receiver, thereby minimizing the stub length from the resistor to the receiver. The limiting case would be to incorporate the termination resistor into the receiver, which is exactly what is offered with the TI ‘LVDT receivers.

While we talk in this section about point-to-point communications, a word of caution is useful when a multidrop topology is used. In such topologies, line termination resistors are to be located only at the end(s) of the transmission line. In such an environment, LVDS receivers could be used for loads branching off the main bus with an LVDT receiver used only at the bus end.

11.2.1.2.7 Driver NC Pins

NC (not connected) pins are pins where the die is not physically connected to the lead frame or package. For optimum thermal performance, a good rule of thumb is to ground the NC pins at the board level.

11.2.1.3 Application Curve

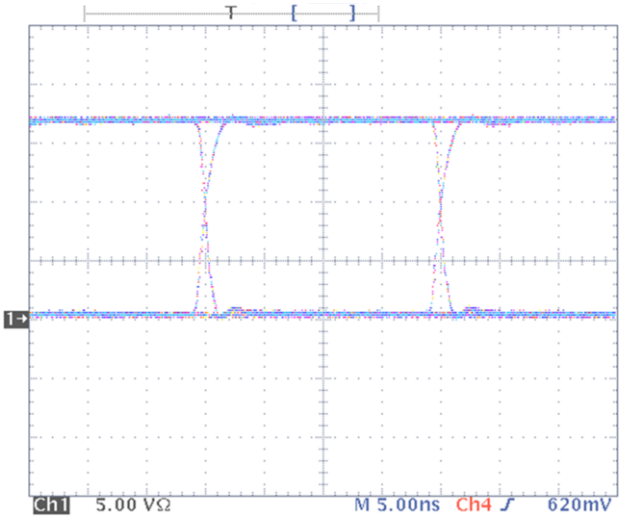


Figure 20. Typical Driver Output Eye Pattern in Point-to-Point System

11.2.2 Multidrop Communications

A second common application of LVDS buffers is a multidrop topology. In a multidrop configuration, a single driver and a shared bus are present along with two or more receivers (with a maximum permissible number of 32 receivers). Figure 21 shows an example of a multidrop system.

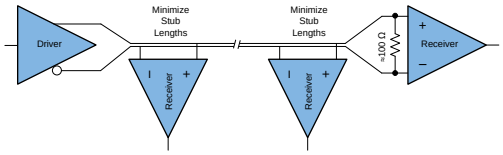


Figure 21. Multidrop Topology

11.2.2.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	3.0 to 3.6 V
Driver Input Voltage	0.8 to 3.3 V
Driver Signaling Rate	DC to 200 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	2 to 32
Receiver Supply Voltage (V_{CCR})	3.0 to 3.6 V
Receiver Input Voltage	0 to 2.4 V
Receiver Signaling Rate	DC to 200 Mbps
Ground shift between driver and receiver	±1 V

11.2.2.2 Detailed Design Procedure

11.2.2.2.1 Interconnecting Media

The interconnect in a multidrop system differs considerably from a point-to-point system. While point-to-point interconnects are straightforward and well understood, the bus type architecture encountered with multidrop systems requires more careful attention. We will use Figure 21 above to explore these details.

The most basic multidrop system would include a single driver, located at a bus origin, with multiple receiver nodes branching off the main line, and a final receiver at the end of the transmission line, co-located with a bus termination resistor. While this would be the most basic multidrop system, it has several considerations not yet explored.

The location of the transmitter at one bus end allows the design concerns to be simplified, but this comes at the cost of flexibility. With a transmitter located at the origin, a single bus termination at the far-end is required. The far-end termination absorbs the incident traveling wave. The flexibility lost with this arrangement is thus: if the single transmitter needed to be relocated on the bus, at any location other than the origin, we would be faced with a bus with one open-circuited end, and one properly terminated end. Locating the transmitter say in the middle of the bus may be desired to reduce (by ½) the maximum flight time from the transmitter to receiver.

Another new feature in Figure 21 is clear in that every node branching off the main line results in stubs. The stubs should be minimized in any case, but have the unintended effect of locally changing the loaded impedance of the bus.

To a good approximation, the characteristic transmission line impedance seen into any cut point in the unloaded multipoint or multidrop bus is defined by $\sqrt{L/C}$, where L is the inductance per unit length and C is the capacitance per unit length. As capacitance is added to the bus in the form of devices and interconnections, the bus characteristic impedance is lowered. This may result in signal reflections from the impedance mismatch between the unloaded and loaded segments of the bus.

If the number of loads is constant and can be distributed evenly along the line, reflections can be reduced by changing the bus termination resistors to match the loaded characteristic impedance. Normally, the number of loads are not constant or distributed evenly and the reflections resulting from any mismatching should be accounted for in the noise budget.

11.2.2.3 Application Curve

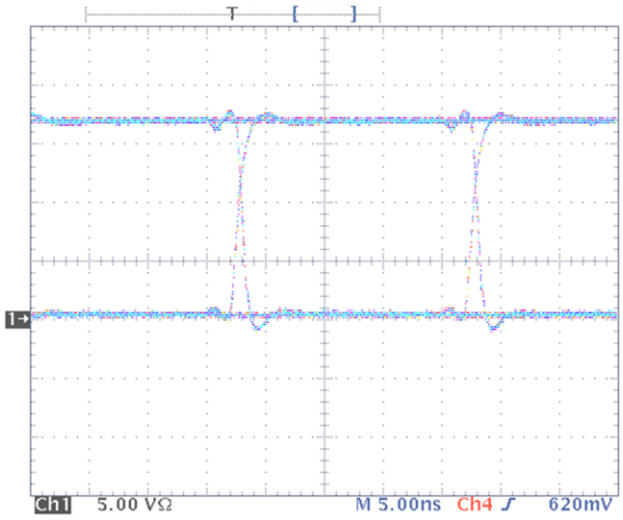


Figure 22. Typical Driver Output Eye Pattern in Multidrop System

12 Power Supply Recommendations

The LVDS driver and receivers in this data sheet are designed to operate from a single power supply. Both drivers and receivers operate with supply voltages in the range of 2.4 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than |±1 V|. Board-level and local device-level bypass capacitance should be used and are covered in *Driver Bypass Capacitance*.

13 Layout

13.1 Layout Guidelines

13.1.1 Microstrip vs Stripline Topologies

As per SLLD009, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 23.

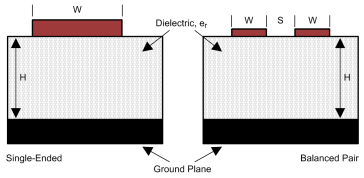


Figure 23. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1(1), 2(2), and 3(3) provide formulas for Z_O and t_{PD} for differential and single-ended traces. (1) (2) (3)

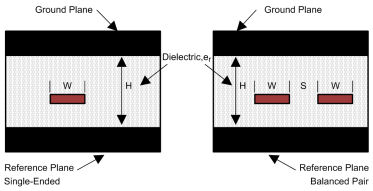


Figure 24. Stripline Topology

13.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 µm or 0.0003 in (minimum).
- Copper plating should be 25.4 µm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(2) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(3) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

Layout Guidelines (continued)

13.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you should decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 25.

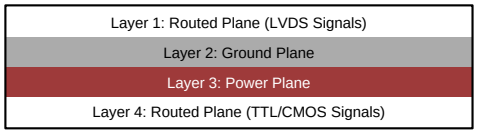


Figure 25. Four-Layer PCB Board

NOTE

The separation between layers 2 and 3 should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in Figure 26.

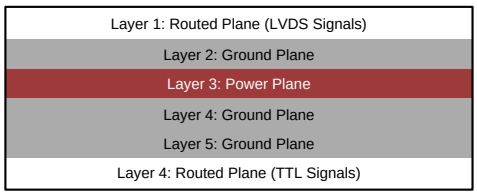


Figure 26. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

13.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces should be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

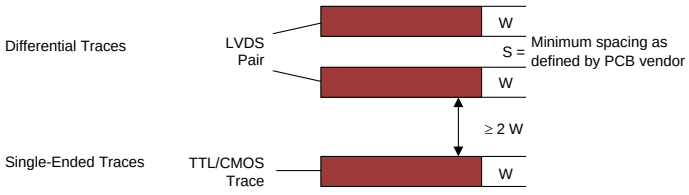


Figure 27. 3-W Rule for Single-Ended and Differential Traces (Top View)

Layout Guidelines (continued)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

13.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

13.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 28.

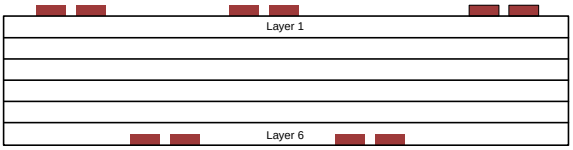


Figure 28. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 29. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

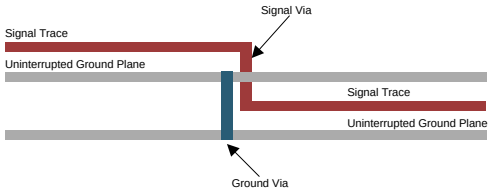


Figure 29. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

14 Device and Documentation Support

14.1 Device Support

14.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

14.1.2 Other LVDS Products

For other products and application notes in the LVDS and LVDM product families visit our Web site at http://www.ti.com/sc/datatran.

14.2 Documentation Support

14.2.1 Related Information

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signaling Design Notes* (SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)
- *Evaluating the LVDS EVM* (SLLA033)

14.3 Related Links

Table 3 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65LVDS387	Click here	Click here	Click here	Click here	Click here
SN75LVDS387	Click here	Click here	Click here	Click here	Click here
SN65LVDS389	Click here	Click here	Click here	Click here	Click here
SN75LVDS389	Click here	Click here	Click here	Click here	Click here
SN65LVDS391	Click here	Click here	Click here	Click here	Click here
SN75LVDS391	Click here	Click here	Click here	Click here	Click here

14.4 Trademarks

Rogers is a trademark of Rogers Corporation.
All other trademarks are the property of their respective owners.

14.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS387DGG	ACTIVE	TSSOP	DGG	64	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS387	Samples
SN65LVDS387DGGG4	ACTIVE	TSSOP	DGG	64	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS387	Samples
SN65LVDS387DGGR	ACTIVE	TSSOP	DGG	64	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS387	Samples
SN65LVDS389DBT	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS389	Samples
SN65LVDS389DBTG4	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS389	Samples
SN65LVDS389DBTR	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS389	Samples
SN65LVDS391D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS391	Samples
SN65LVDS391DG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS391	Samples
SN65LVDS391DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS391	Samples
SN65LVDS391DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS391	Samples
SN65LVDS391PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS391	Samples
SN65LVDS391PWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS391	Samples
SN65LVDS391PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS391	Samples
SN75LVDS387DGG	ACTIVE	TSSOP	DGG	64	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDS387	Samples
SN75LVDS387DGGR	ACTIVE	TSSOP	DGG	64	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDS387	Samples
SN75LVDS387DGGRG4	ACTIVE	TSSOP	DGG	64	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDS387	Samples
SN75LVDS389DBT	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDS389	Samples
SN75LVDS389DBTR	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDS389	Samples
SN75LVDS389DBTRG4	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDS389	Samples
SN75LVDS391D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS391	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVDS391DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS391	Samples
SN75LVDS391PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	DS391	Samples
SN75LVDS391PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	DS391	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

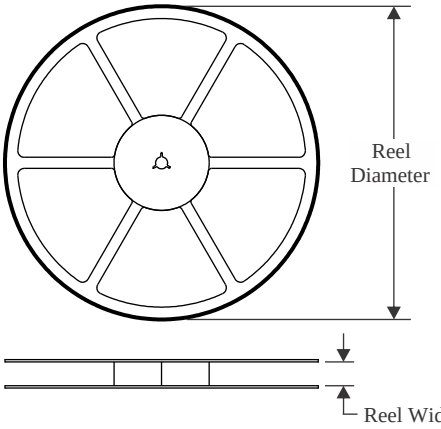
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

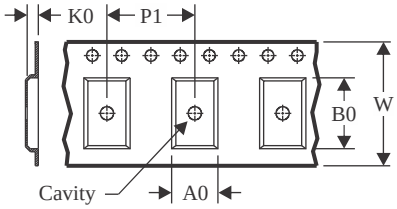
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

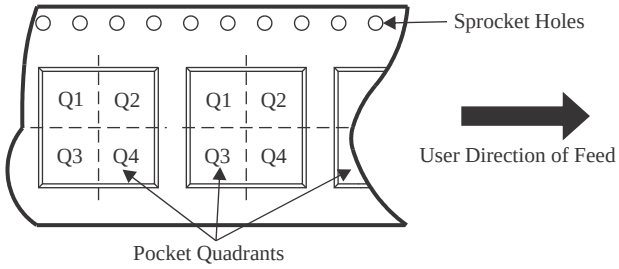


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

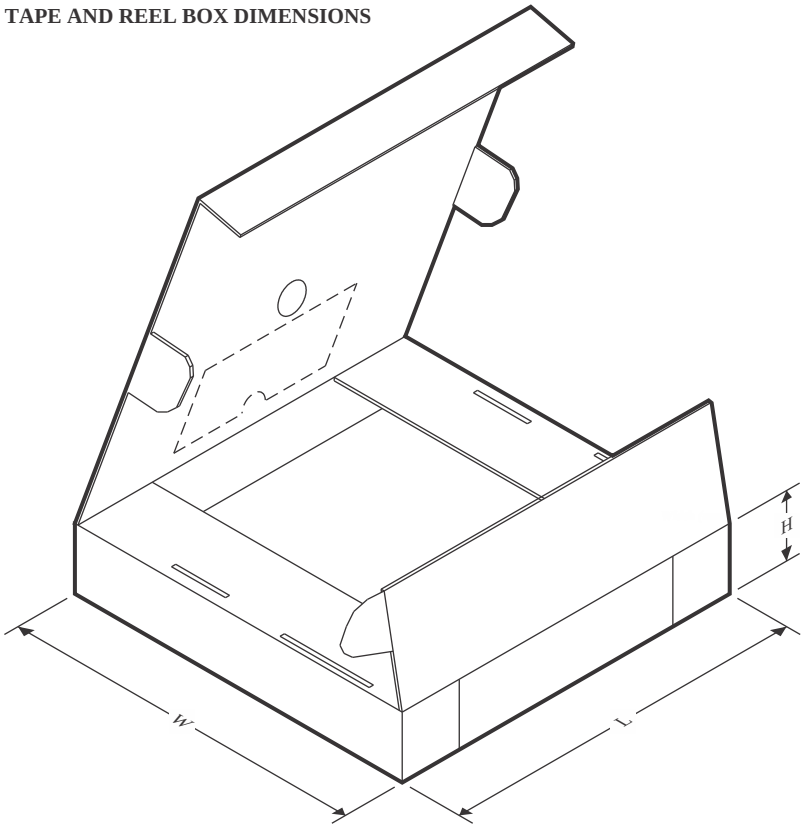
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS387DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN65LVDS389DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN65LVDS391DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS391PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75LVDS387DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN75LVDS389DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN75LVDS391DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75LVDS391PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

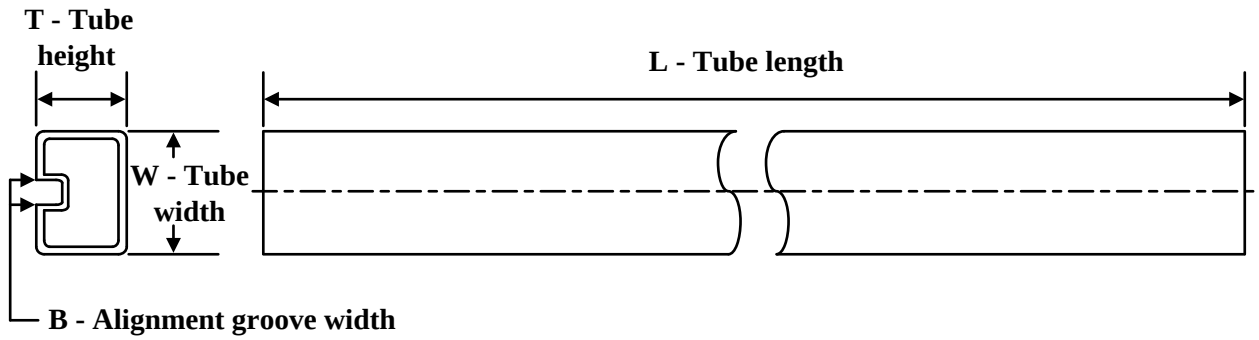
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS387DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0
SN65LVDS389DBTR	TSSOP	DBT	38	2000	350.0	350.0	43.0
SN65LVDS391DR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDS391PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN75LVDS387DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0
SN75LVDS389DBTR	TSSOP	DBT	38	2000	350.0	350.0	43.0
SN75LVDS391DR	SOIC	D	16	2500	350.0	350.0	43.0
SN75LVDS391PWR	TSSOP	PW	16	2000	350.0	350.0	43.0

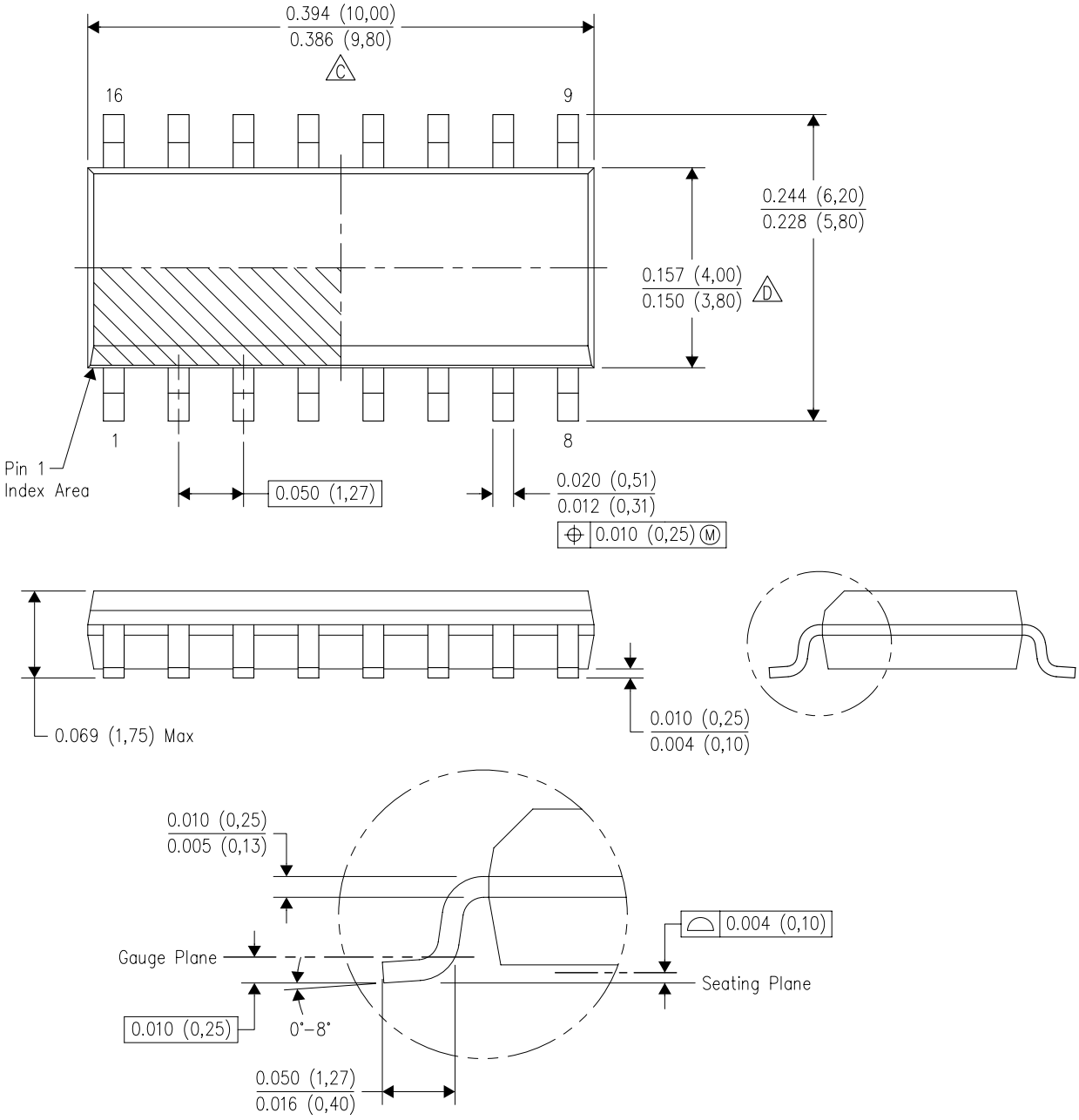
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS387DGG	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDS387DGGG4	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDS389DBT	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN65LVDS389DBTG4	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN65LVDS391D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS391DG4	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS391PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS391PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN75LVDS387DGG	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN75LVDS389DBT	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN75LVDS391D	D	SOIC	16	40	505.46	6.76	3810	4
SN75LVDS391PW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



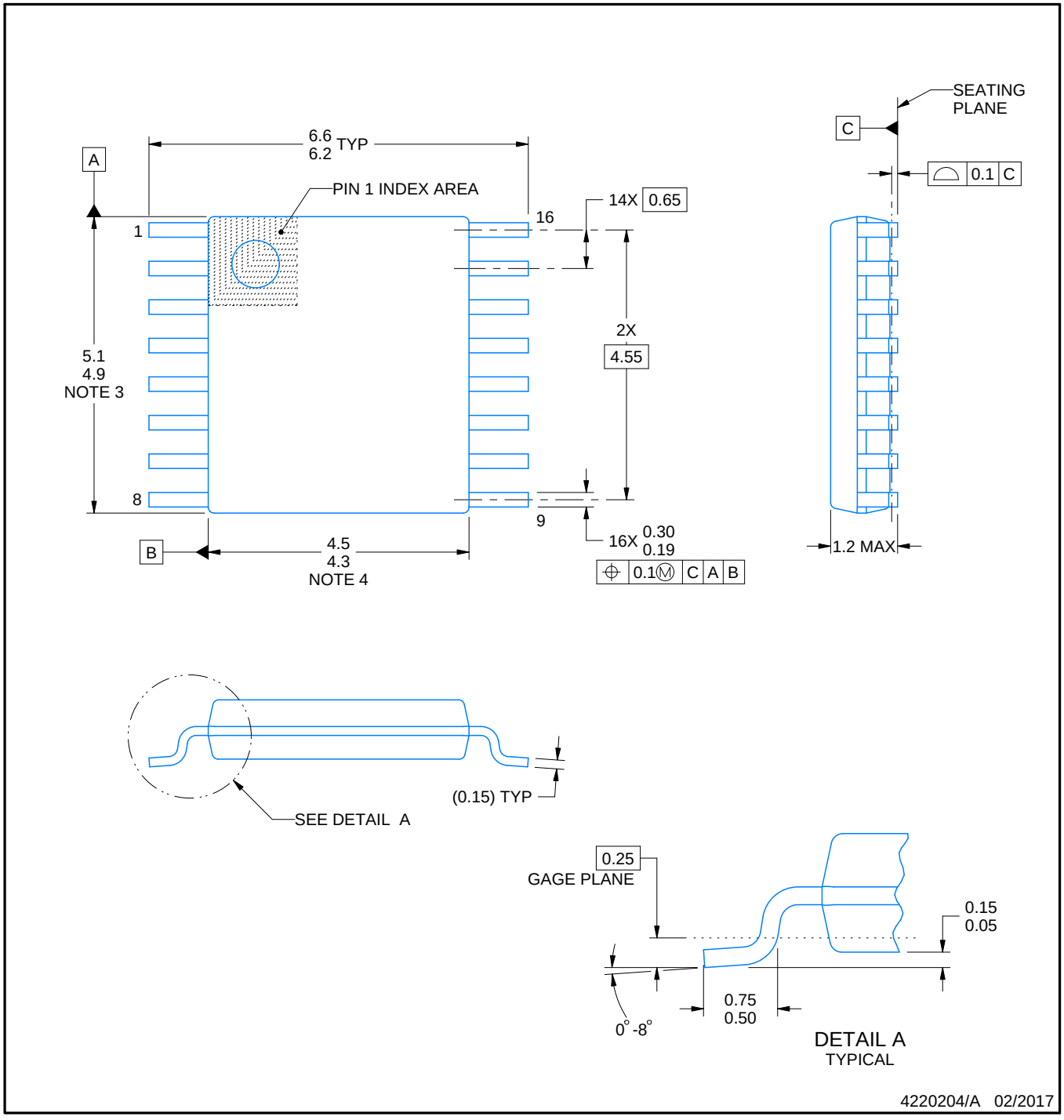
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

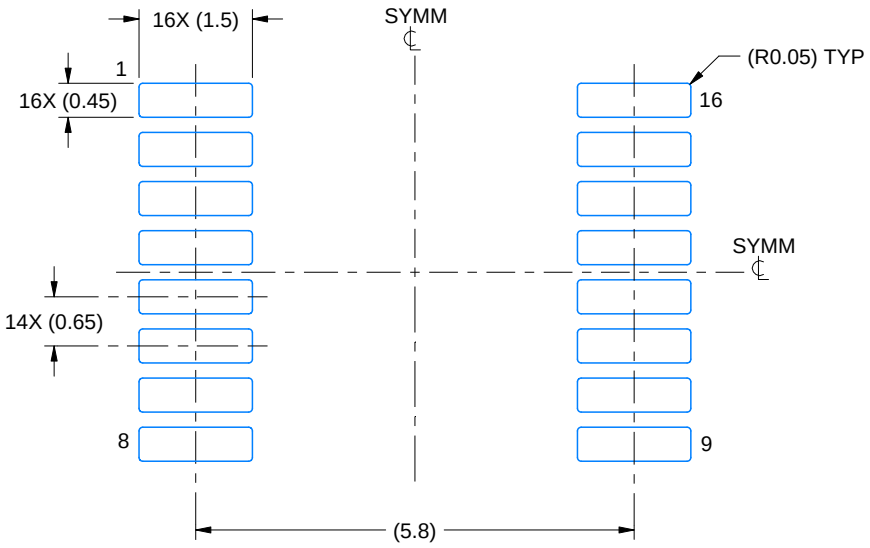
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

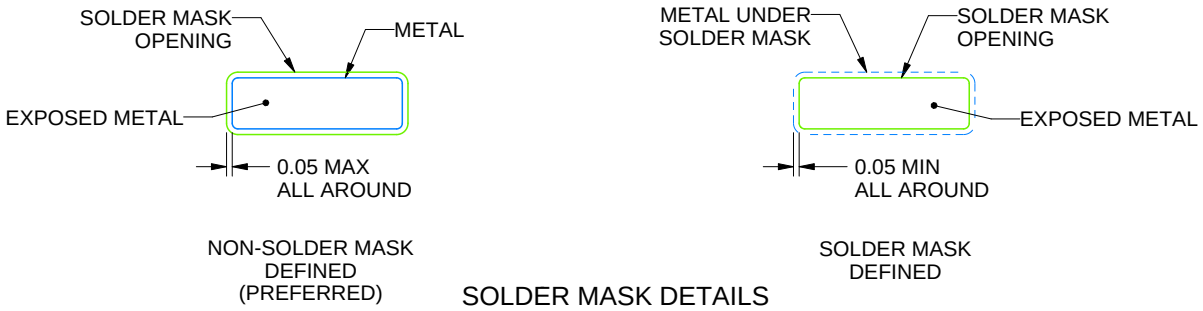


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

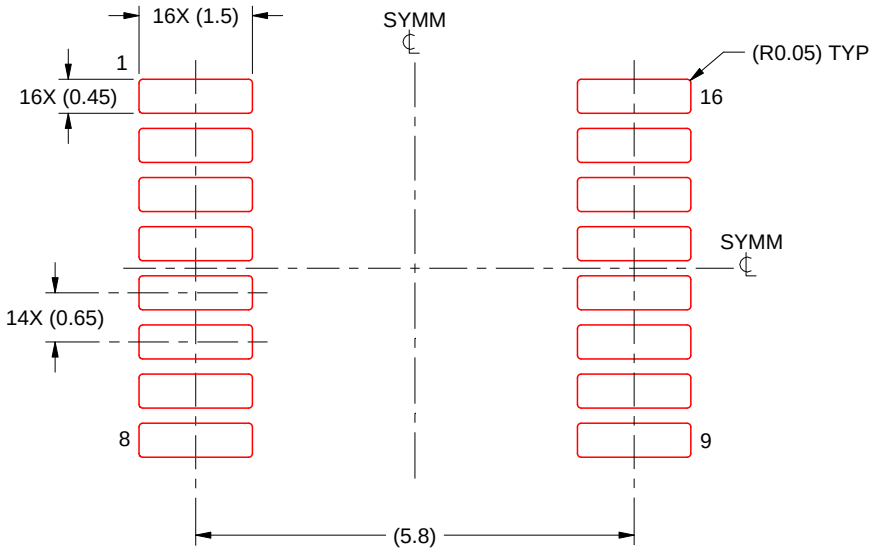


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

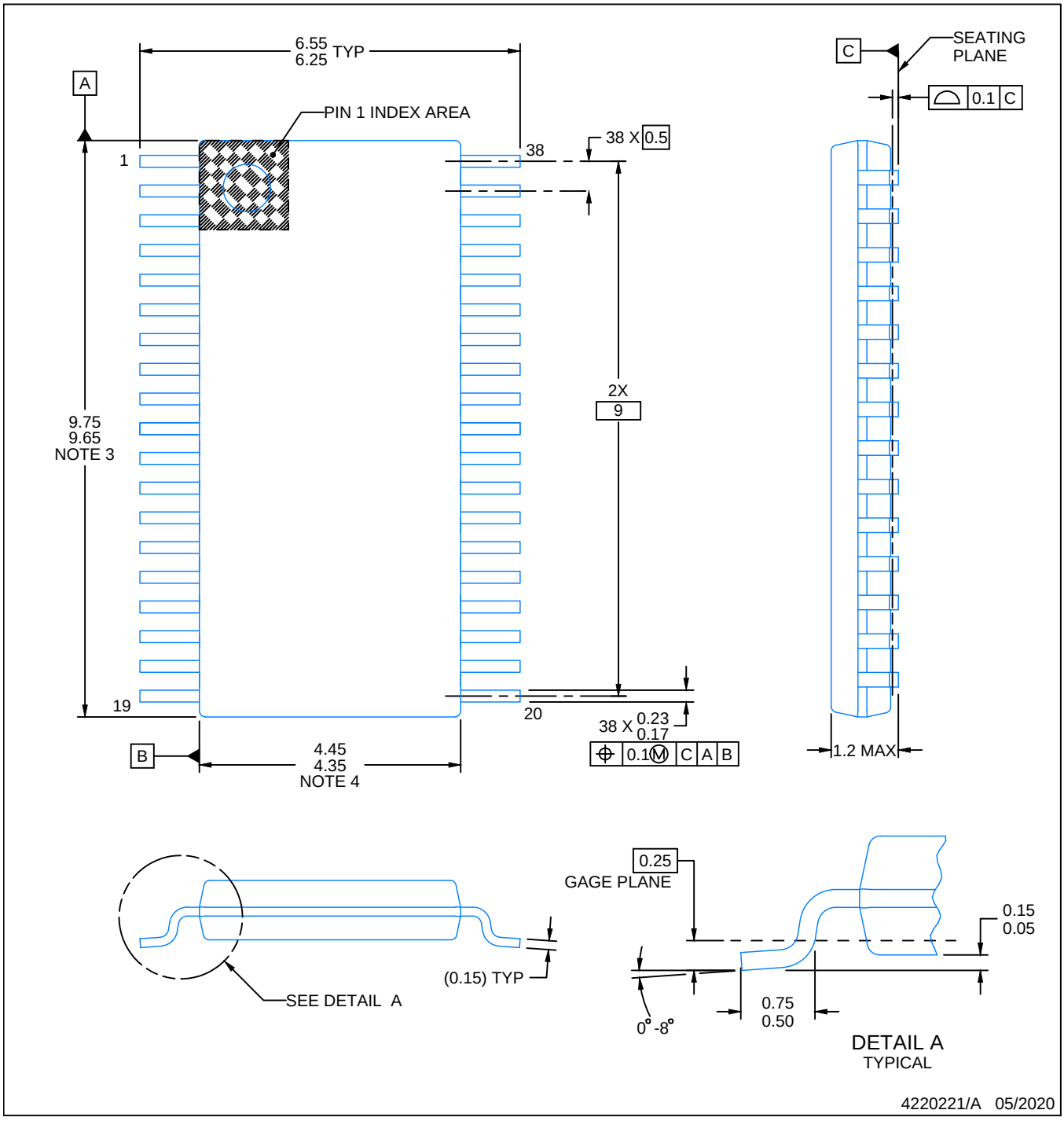
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBT0038A

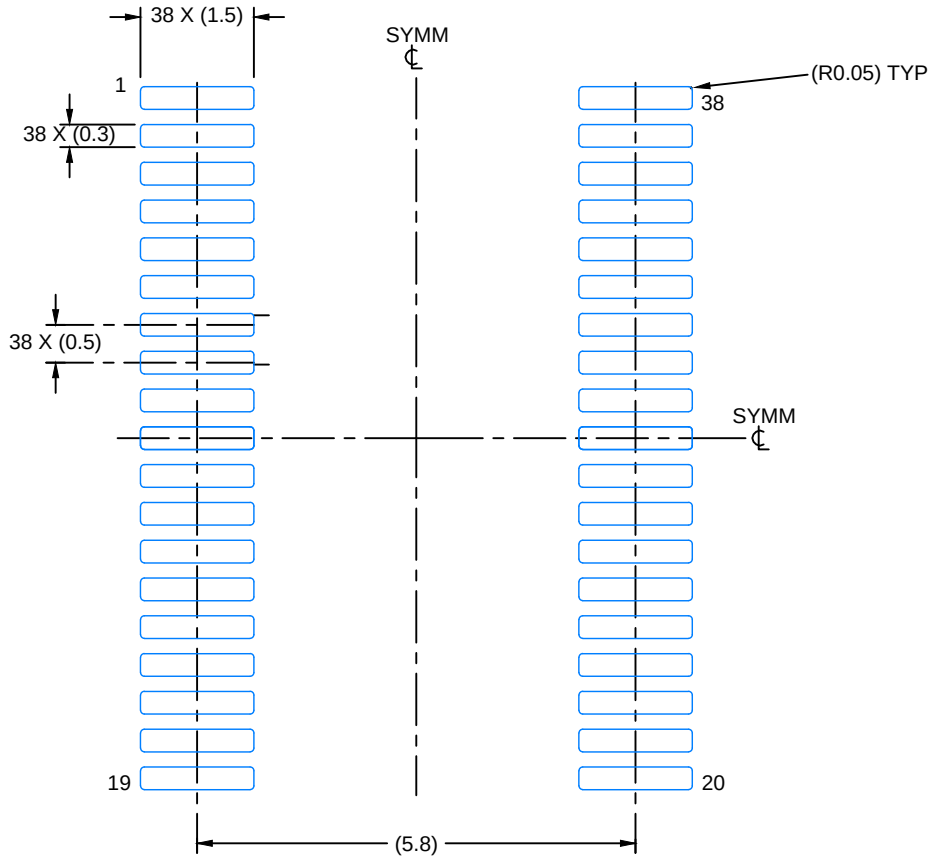
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

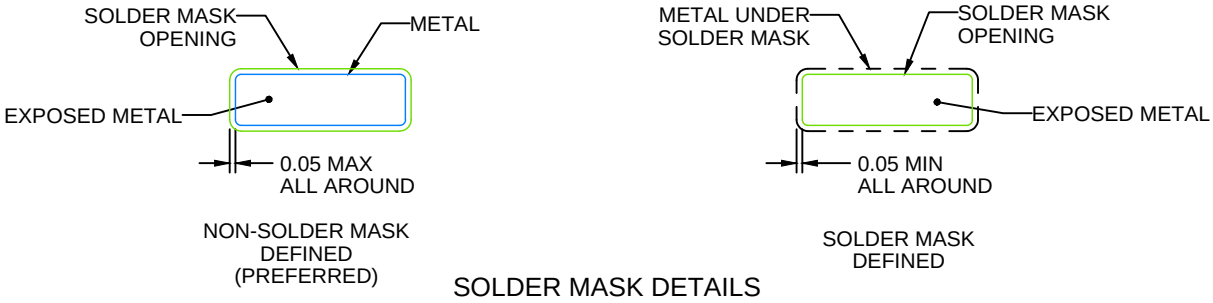


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

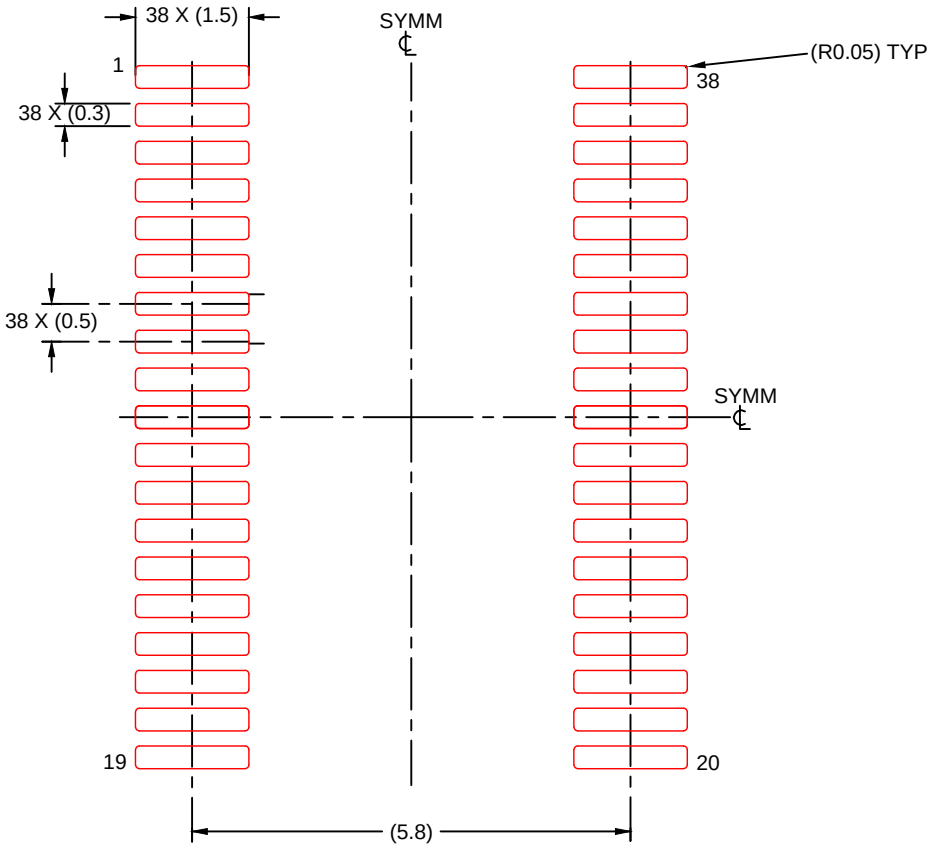


SOLDER MASK DETAILS

4220221/A 05/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

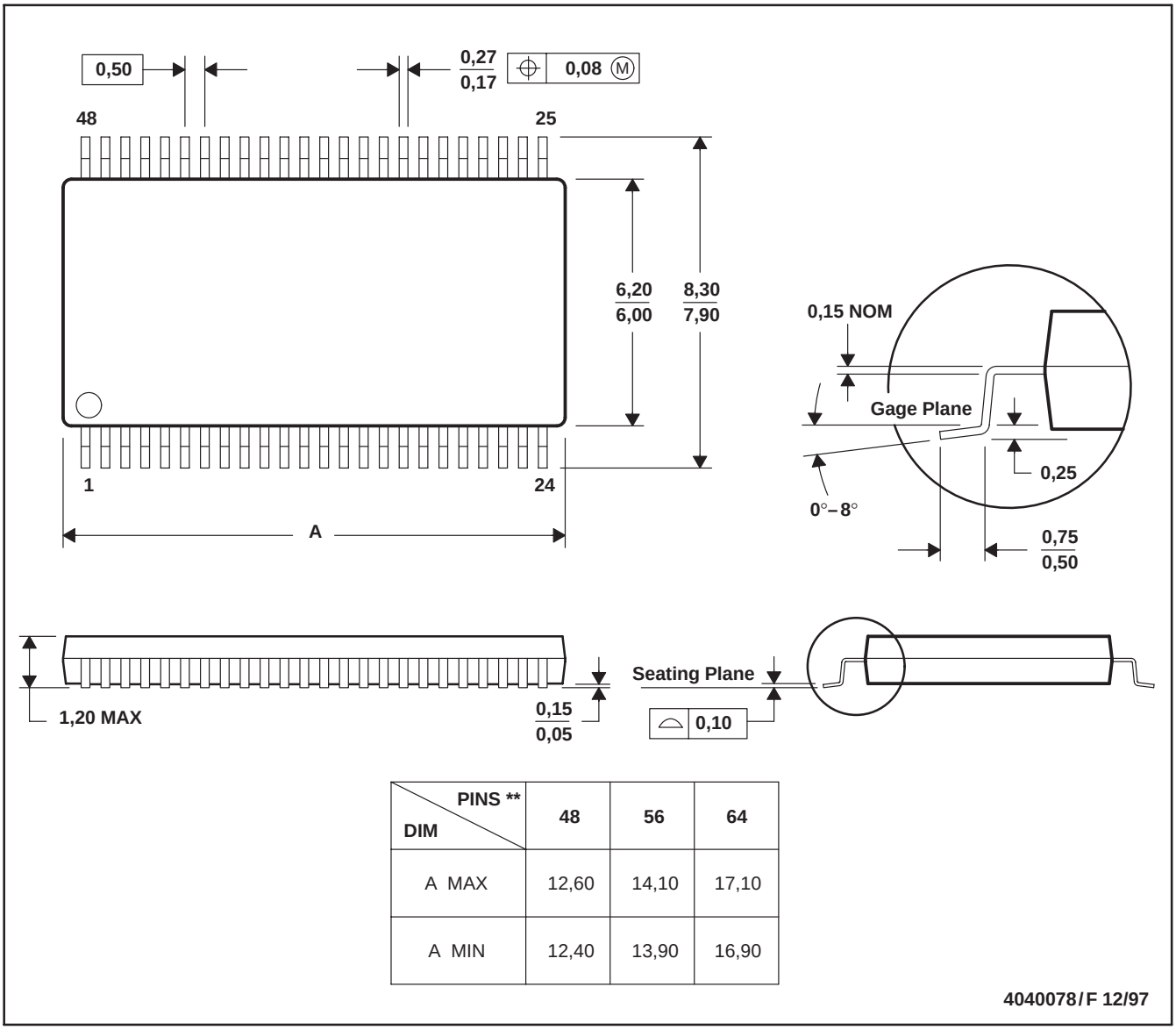
4220221/A 05/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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