SN65LVDS93B-Q1 10 MHz - 85 MHz Automotive 28-bit Flat Panel Display Link LVDS SerDes Transmitter

1 Features

- AEC-Q100 Qualified for Automotive Applications
  - Temperature Grade 3: –40°C to 85°C
  - HBM ESD Classification 3
  - CDM ESD Classification C6
- LVDS Display Series Interfaces Directly to LCD Display Panels With Integrated LVDS
- Package: 14-mm x 6.1-mm TSSOP
- 1.8-V Up to 3.3-V Tolerant Data Inputs to Connect Directly to Low-Power, Low-Voltage Application and Graphic Processors
- Transfer Rate up to 85 Mpps (Mega Pixel Per Second); Pixel Clock Frequency Range 10 MHz to 85 MHz; Max 2.38 Gbps data rate supported
- Suited for Display Resolutions Ranging From HVGA up to HD With Low EMI
- Operates From a Single 3.3-V Supply and 170 mW (Typical) at 75 MHz
- 28 Data Channels Plus Clock in Low-Voltage TTL to 4 Data Channels Plus Clock Out Low-Voltage Differential
- Consumes Less Than 1 mW When Disabled
- Selectable Rising or Falling Clock Edge Triggered Inputs
- Support Spread Spectrum Clocking (SSC)
- Supports RGB 888 to LVDS I Conversion

2 Applications

- Automotive Display for Navigation
- Automotive Cluster display
- Automotive Center Stack Display

3 Description

The SN65LVDS93B-Q1 transmitter contains four 7-bit parallel-load serial-out shift registers, a 7X clock synthesizer, and five Low-Voltage Differential Signaling (LVDS) line drivers in a single integrated circuit. These functions allow 28 bits of single-ended LVTTL data to be synchronously transmitted over five balanced-pair conductors for receipt by a compatible receiver, such as the DS90CR286A-Q1 and LCD panels with integrated LVDS receiver.

When transmitting, data bits D0 through D27 are each loaded into registers upon the edge of the input clock signal (CLKIN). The rising or falling edge of the clock can be selected via the clock select (CLKSEL) pin. The frequency of CLKIN is multiplied seven times, and then used to unload the data registers in 7-bit slices and serially. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

The SN65LVDS93B-Q1 requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is selecting a clock rising edge by inputting a high level to CLKSEL or a falling edge with a low-level input, and the possible use of the Shutdown/Clear ($\overline{SHTDN}$). $\overline{SHTDN}$ is an active-low input to inhibit the clock, and shut off the LVDS output drivers for lower power consumption. A low-level on this signal clears all internal registers to a low-level.

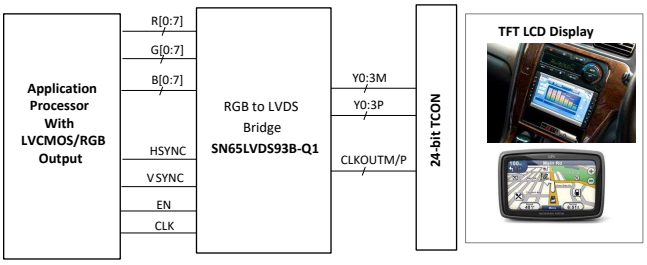
The SN65LVDS93B-Q1 is characterized for operation over ambient air temperatures of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVDS93B-Q1	TSSOP (56)	14.00 mm x 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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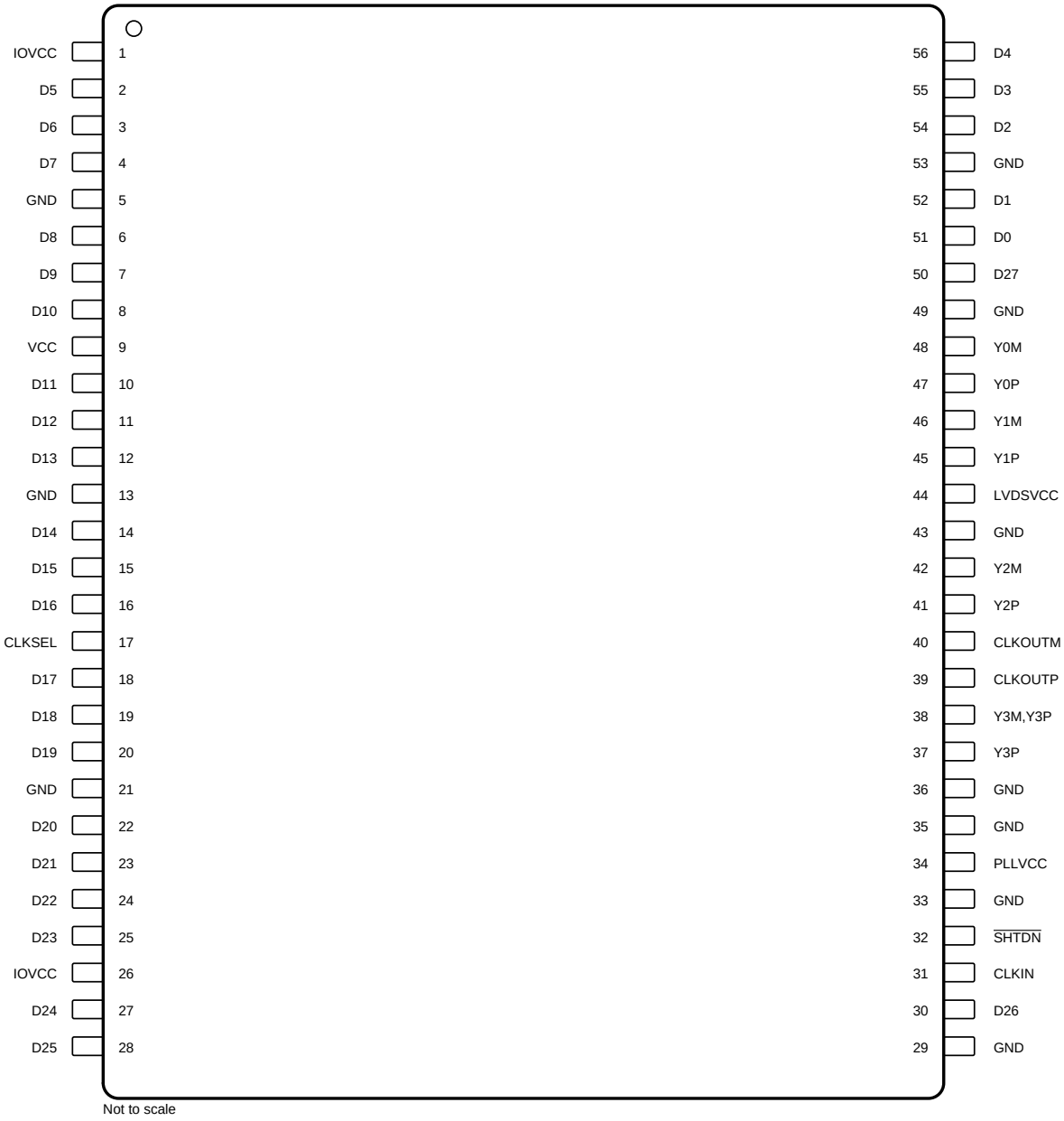
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2018) to Revision A	Page
• Changed the device status From: *Advanced Information* To: *Production* data	1

5 Pin Configuration and Functions

DGG Package
56-PIN (TSSOP)
(Top View)



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLKIN	31	CMOS IN with pulldn	Input pixel clock; rising or falling clock polarity is selectable by Control input CLKSEL.
CLKOUTP	39	LVDS Out	Differential LVDS pixel clock output. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted).
CLKOUTM	40		
CLKSEL	17	CMOS IN with pulldn	Selects between rising edge input clock trigger (CLKSEL = V_{IH}) and falling edge input clock trigger (CLKSEL = V_{IL}).
D5, D6, D7, D8 D9, D10, D11, D12 D13, D14, D15, D16 D17, D18, D19, D20 D21, D22, D23, D24 D25, D26, D27 D0, D1, D2, D3, D4	2, 3, 4, 6 7, 8, 10, 11 12, 14, 15 , 16 18, 19, 20, 22 23, 24, 25, 27 28, 30, 50 51, 52, 54, 55, 56	CMOS IN with pulldn	Data inputs; supports 1.8 V to 3.3 V input voltage selectable by VDD supply. To connect a graphic source successfully to a display, the bit assignment of D[27:0] is critical (and not necessarily intuitive). For input bit assignment see to for details. Note: if application only requires 18-bit color, connect unused inputs D5, D10, D11, D16, D17, D23, and D27 to GND.
GND	5, 13, 21, 29, 33, 35, 36, 43, 49, 53	Power Supply(1)	Supply ground for VCC, IOVCC, LVDSVCC, and PLLVCC.
IOVCC	1, 26	Power Supply(1)	I/O supply reference voltage (1.8 V up to 3.3 V matching the GPU data output signal swing)
LVDSVCC	44	Power Supply(1)	3.3 V LVDS output analog supply
PLLVCC	34	Power Supply(1)	3.3 V PLL analog supply
$\overline{\text{SHTDN}}$	32	CMOS IN with pulldn	Device shut down; pull low (de-assert) to shut down the device (low power, resets all registers) and high (assert) for normal operation.
VCC	9	Power Supply(1)	3.3 V digital supply voltage
Y0P	47	LVDS Out	Differential LVDS data outputs. Outputs are high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted)
Y0M	48		
Y1P	45		
Y1M	45		
Y2P	41		
Y2M	42		
Y3P	37	LVDS Out	Differential LVDS Data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted). Note: if the application only requires 18-bit color, this output can be left open.
Y3M	38		

(1) For a multilayer pcb, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Supply voltage range, VCC, IOVCC, LVDSVCC, PLLVCC(2)	–0.5	4	V
Voltage range at any output terminal	–0.5	VCC + 0.5	V
Voltage range at any input terminal	–0.5	IOVCC + 0.5	V
Continuous power dissipation	See *Thermal Information*		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) All voltages are with respect to the GND terminals.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. e.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, VCC		3	3.3	3.6	V
LVDS output Supply voltage, LVDSVCC		3	3.3	3.6	
PLL analog supply voltage, PLLVCC		3	3.3	3.6	
IO input reference supply voltage, IOVCC		1.62	1.8 / 2.5 / 3.3	3.6	
Power supply noise on any VCC terminal				0.1	
High-level input voltage, V_{IH}	IOVCC = 1.8 V	IOVCC/2 + 0.3 V			V
	IOVCC = 2.5 V	IOVCC/2 + 0.4 V			
	IOVCC = 3.3 V	IOVCC/2 + 0.5 V			
Low-level input voltage, V_{IL}	IOVCC = 1.8 V			IOVCC/2 - 0.3 V	V
	IOVCC = 2.5 V			IOVCC/2 - 0.4 V	
	IOVCC = 3.3 V			IOVCC/2 - 0.5 V	
Differential load impedance, Z_L		90		132	Ω
Operating free-air temperature, T_A		–40		85	°C
Virtual junction temperature, T_J				105	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN65LVDS93B-Q1 DGG (TSSOP) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Thermal Information (continued)

THERMAL METRIC[1]		SN65LVDS93B-Q1 DGG (TSSOP) 56 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_T	Input voltage threshold	R_L = 100Ω, See Figure 5		IOVCC/2		V
$\|V_{OD}\|$	Differential steady-state output voltage magnitude		250		450	mV
$\Delta\|V_{OD}\|$	Change in the steady-state differential output voltage magnitude between opposite binary states			1	35	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 5 $t_{R/F}$ (Dx, CLKin) = 1ns	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				35	mV
I_{IH}	High-level input current	V_{IH} = IOVCC			25	µA
I_{IL}	Low-level input current	V_{IL} = 0 V			±10	µA
I_{OS}	Short-circuit output current	V_{OY} = 0 V			±24	mA
		V_{OD} = 0 V			±12	mA
I_{OZ}	High-impedance state output current	V_O = 0 V to VCC			±20	µA
R_{pdn}	Input pull-down integrated resistor on all inputs (Dx, CLKSEL, $\overline{SHTDN}$, CLKIN)	IOVCC = 1.8 V		200		kΩ
		IOVCC = 3.3 V		100		
I_Q	Quiescent current (average)	disabled, all inputs at GND; $\overline{SHTDN}$ = V_{IL}		10	100	µA
I_{CC}	Supply current (average)	$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), grayscale pattern (Figure 6) VCC = 3.3 V, f_{CLK} = 75 MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		51.9		mA
		$I_{(IOVCC)}$ with IOVCC = 3.3 V		0.4		
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.1		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), worst-case pattern (Figure 7), VCC = 3.6 V, f_{CLK} = 75 MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		63.7		mA
		$I_{(IOVCC)}$ with IOVCC = 3.3 V		1.3		
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.5		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), worst-case pattern (Figure 7), f_{CLK} = 85 MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		75.1		mA
		$I_{(IOVCC)}$ with IOVCC = 3.6 V		1.5		
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.6		
C_I	Input capacitance			2		pF

(1) All typical values are at VCC = 3.3 V, T_A = 25°C.

6.6 Timing Requirements

PARAMETER		MIN	MAX	UNIT
Input clock period, t_c		7.4	100	ns
Input clock modulation	with modulation frequency 30 kHz		8%	
	with modulation frequency 50 kHz		6%	
High-level input clock pulse width duration, t_w		0.4 t_c	0.6 t_c	ns
Input signal transition time, t_t			3	ns

Timing Requirements (continued)

PARAMETER	MIN	MAX	UNIT
Data set up time, D0 through D27 before CLKIN (See Figure 4)	2		ns
Data hold time, D0 through D27 after CLKIN	0.8		ns

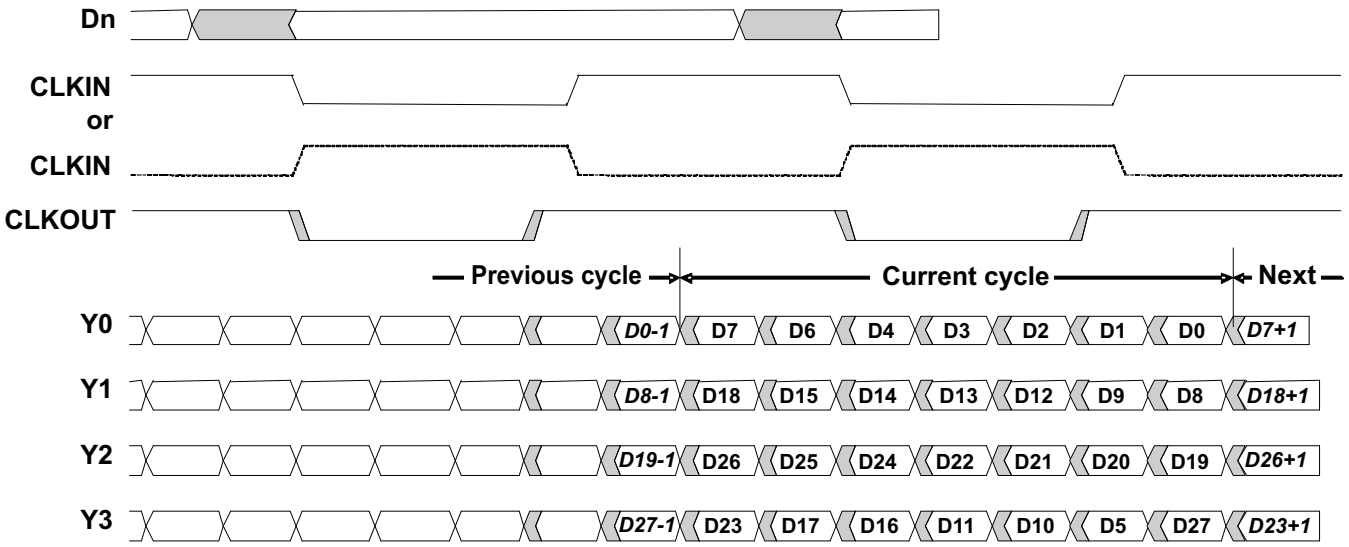


Figure 1. Typical SN65LVDS93B-Q1 Load and Shift Sequences

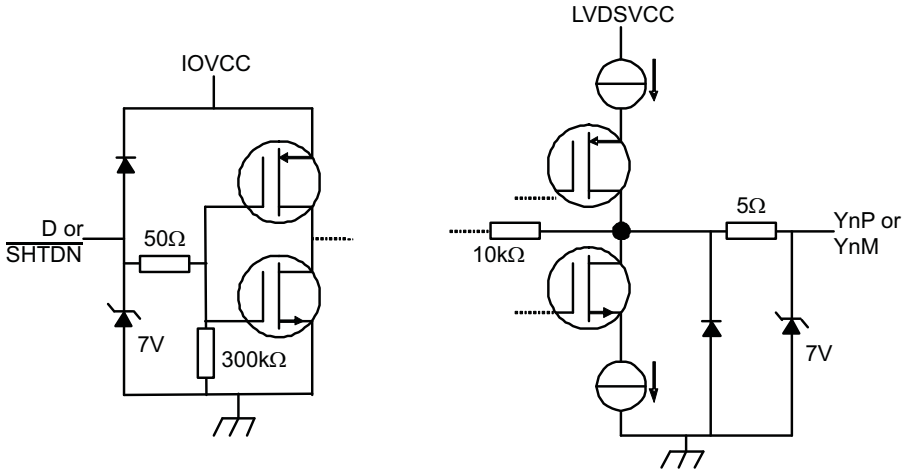


Figure 2. Equivalent Input and Output Schematic Diagrams

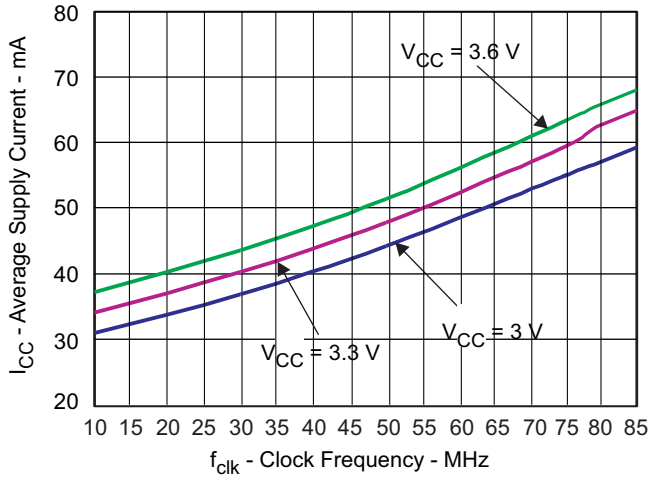
6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_0	Delay time, CLKOUT↑ after Yn valid (serial bit position 0, equal D1, D9, D20, D5)	See Figure 8, t_C = 10ns, |Input clock jitter| < 25ps (2)	-0.1	0	0.1	ns
t_1	Delay time, CLKOUT↑ after Yn valid (serial bit position 1, equal D0, D8, D19, D27)		$^1/_7\ t_c$ - 0.1		$^1/_7\ t_c$ + 0.1	ns
t_2	Delay time, CLKOUT↑ after Yn valid (serial bit position 2, equal D7, D18, D26. D23)		$^2/_7\ t_c$ - 0.1		$^2/_7\ t_c$ + 0.1	ns
t_3	Delay time, CLKOUT↑ after Yn valid (serial bit position 3; equal D6, D15, D25, D17)		$^3/_7\ t_c$ - 0.1		$^3/_7\ t_c$ + 0.1	ns
t_4	Delay time, CLKOUT↑ after Yn valid (serial bit position 4, equal D4, D14, D24, D16)		$^4/_7\ t_c$ - 0.1		$^4/_7\ t_c$ + 0.1	ns
t_5	Delay time, CLKOUT↑ after Yn valid (serial bit position 5, equal D3, D13, D22, D11)		$^5/_7\ t_c$ - 0.1		$^5/_7\ t_c$ + 0.1	ns
t_6	Delay time, CLKOUT↑ after Yn valid (serial bit position 6, equal D2, D12, D21, D10)		$^6/_7\ t_c$ - 0.1		$^6/_7\ t_c$ + 0.1	ns
$t_{c(o)}$	Output clock period			t_c		ns
$\Delta t_{c(o)}$	Output clock cycle-to-cycle jitter (3)	t_C = 10ns; clean reference clock, see Figure 9		±35		ps
		t_C = 10ns with 0.05UI added noise modulated at 3MHz, see Figure 9		±44		
		t_C = 7.4ns; clean reference clock, see Figure 9		±35		
		t_C = 7.4ns with 0.05UI added noise modulated at 3MHz, see Figure 9		±42		
t_w	High-level output clock pulse duration			$^4/_7\ t_c$		ns
$t_{r/f}$	Differential output voltage transition time (t_r or t_f)	See Figure 5		225	500	ps
t_{en}	Enable time, $\overline{SHTDN}$↑ to phase lock (Yn valid)	$f_{(clk)}$ = 85MHz, See Figure 10		10		µs
t_{dis}	Disable time, $\overline{SHTDN}$↓ to off-state (CLKOUT high-impedance)	$f_{(clk)}$ = 85MHz, See Figure 11		12		ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) |Input clock jitter| is the magnitude of the change in the input clock period.
(3) The output clock cycle-to-cycle jitter is the largest recorded change in the output clock period from one cycle to the next cycle observed over 15,000 cycles.Tektronix TDSJIT3 Jitter Analysis software was used to derive the maximum and minimum jitter value.

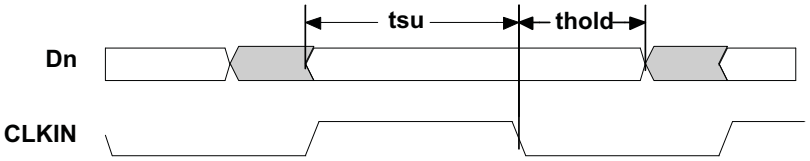
6.8 Typical Characteristics



Total Device Current (Using Grayscale pattern) Over Pixel Clock Frequency

Figure 3. Average Grayscale I_{CC} vs Clock Frequency

7 Parameter Measurement Information



All input timing is defined at IOVDD / 2 on an input signal with a 10% to 90% rise or fall time of less than 3 ns. CLKSEL = 0 V.

Figure 4. Set Up and Hold Time Definition

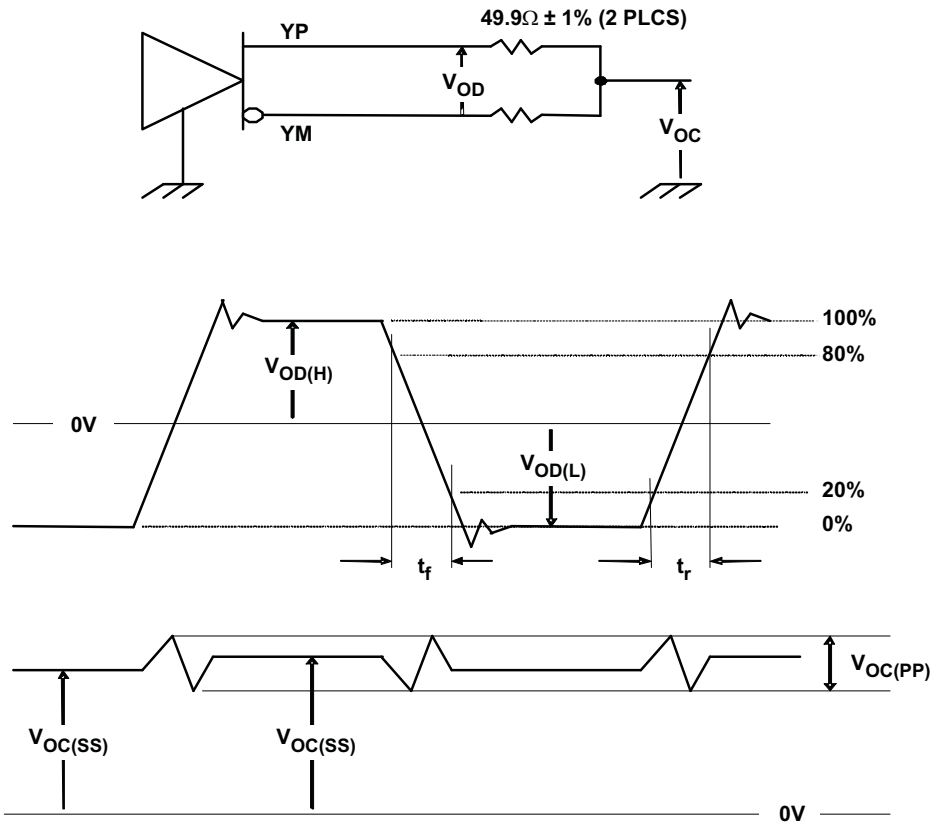
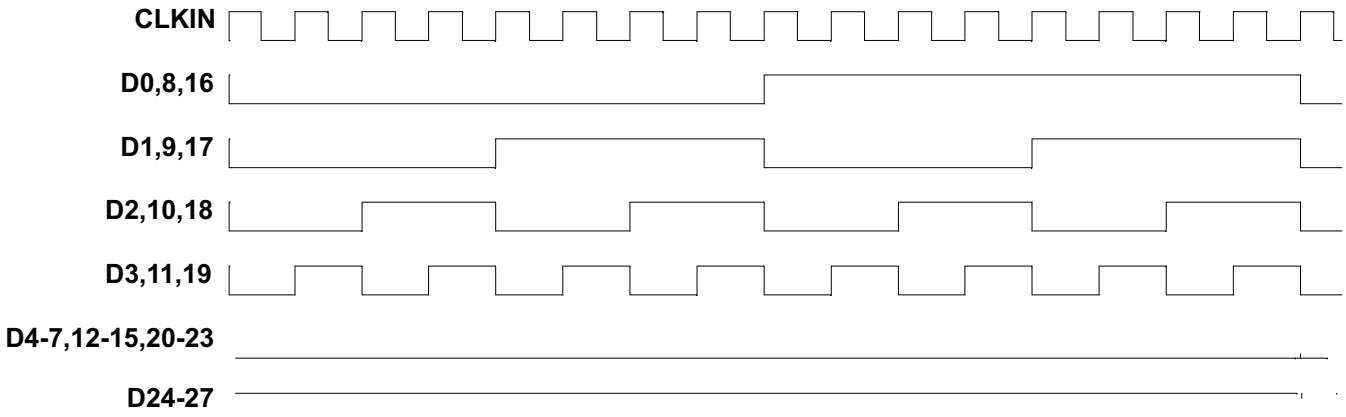
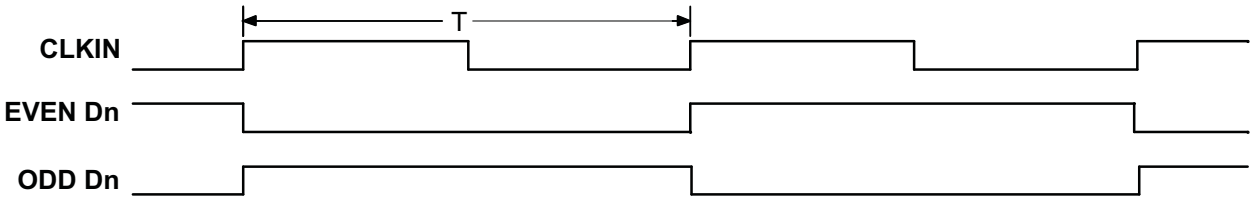


Figure 5. Test Load and Voltage Definitions for LVDS Outputs



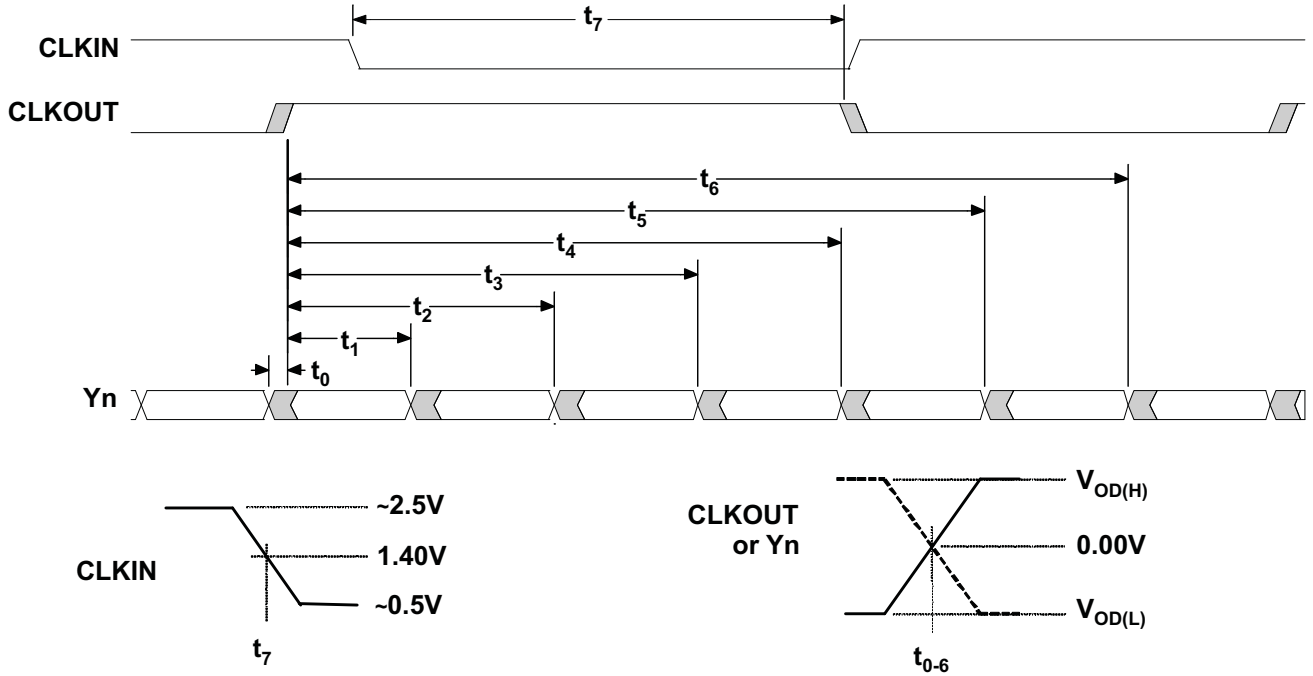
The 16 grayscale test pattern test device power consumption for a typical display pattern.

Figure 6. 16 Grayscale Test Pattern



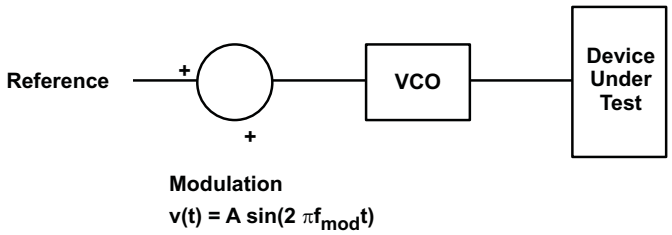
The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs.

Figure 7. Worst-Case Power Test Pattern



CLKOUT is shown with CLKSEL at high-level.
CLKIN polarity depends on CLKSEL input level.

Figure 8. SN65LVDS93B-Q1 Timing Definitions



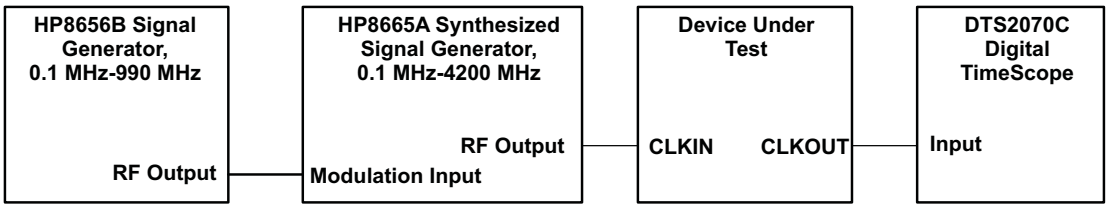


Figure 9. Output Clock Jitter Test Set Up

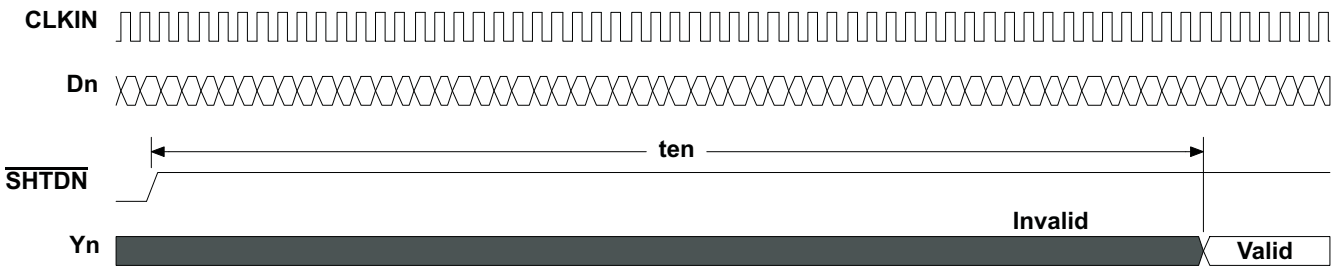


Figure 10. Enable Time Waveforms

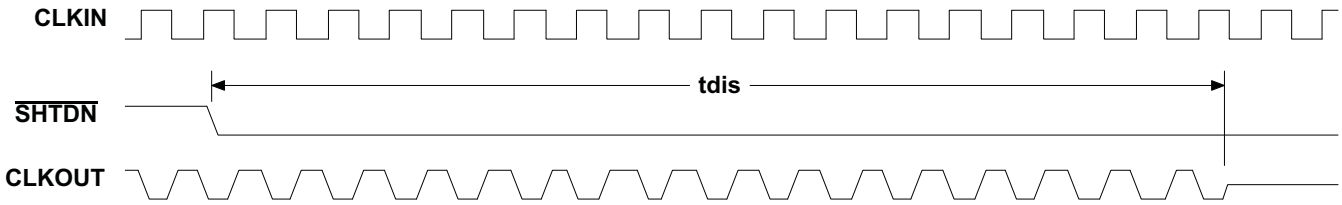


Figure 11. Disable Time Waveforms

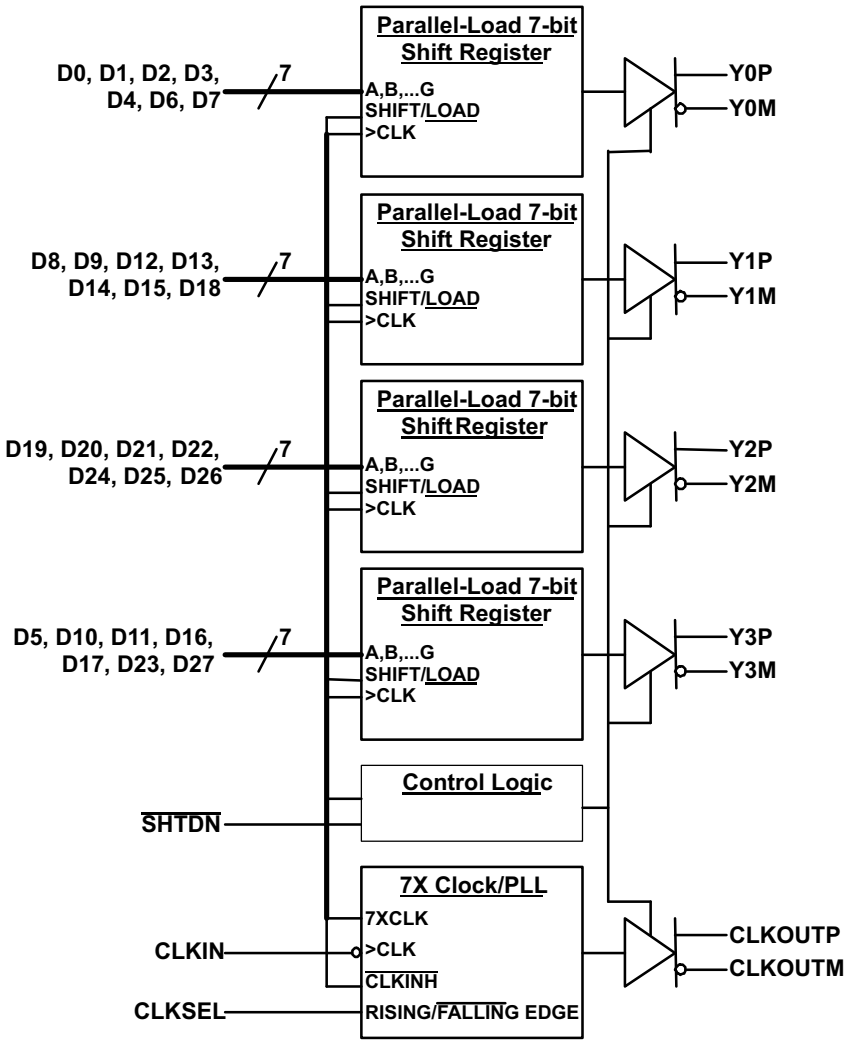
8 Detailed Description

8.1 Overview

The SN65LVDS93B-Q1 takes in three (or four) data words each containing seven single-ended data bits and converts this to an LVDS serial output. Each serial output runs at seven times that of the parallel data rate. The deserializer (receiver) device operates in the reverse manner. The three (or four) LVDS serial inputs are transformed back to the original seven-bit parallel single-ended data. Additional TI solutions are available in 21:3 or 28:4 SerDes ratios.

- The 21-bit devices are designed for 6-bit RGB video for a total of 18 bits in addition to three extra bits for horizontal synchronization, vertical synchronization, and data enable.
- The 28-bit devices are intended for 8-bit RGB video applications. Again, the extra four bits are for horizontal synchronization, vertical synchronization, data enable, and the remaining is the reserved bit. These 28-bit devices can also be used in 6-bit and 4-bit RGB applications as shown in the subsequent system diagrams.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 TTL Input Data

The data inputs to the transmitter come from the graphics processor and consist of up to 24 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, an enable bit, and a spare bit. The data can be loaded into the registers upon either the rising or falling edge of the input clock selectable by the CLKSEL pin. Data inputs are 1.8 V to 3.3 V tolerant for the SN65LVDS93B-Q1 and can connect directly to low-power, low-voltage application and graphic processors. The bit mapping is listed in Table 1.

Table 1. Pixel Bit Ordering

	RED	GREEN	BLUE
LSB	R0	G0	B0
	R1	G1	B1
	R2	G2	B2
4-bit MSB	R3	G3	B3
	R4	G4	B4
6-bit MSB	R5	G5	B5
	R6	G6	B6
8-bit MSB	R7	G7	B7

8.3.2 LVDS Output Data

The pixel data assignment is listed in Table 2 for 24-bit, 18-bit, and 12-bit color hosts.

Table 2. Pixel Data Assignment

SERIAL CHANNEL	DATA BITS	8-BIT			6-BIT	4-BIT	
		FORMAT-1	FORMAT-2	FORMAT-3		NON-LINEAR STEP SIZE	LINEAR STEP SIZE
Y0	D0	R0	R2	R2	R0	R2	VCC
	D1	R1	R3	R3	R1	R3	GND
	D2	R2	R4	R4	R2	R0	R0
	D3	R3	R5	R5	R3	R1	R1
	D4	R4	R6	R6	R4	R2	R2
	D6	R5	R7	R7	R5	R3	R3
	D7	G0	G2	G2	G0	G2	VCC
Y1	D8	G1	G3	G3	G1	G3	GND
	D9	G2	G4	G4	G2	G0	G0
	D12	G3	G5	G5	G3	G1	G1
	D13	G4	G6	G6	G4	G2	G2
	D14	G5	G7	G7	G5	G3	G3
	D15	B0	B2	B2	B0	B2	VCC
	D18	B1	B3	B3	B1	B3	GND
Y2	D19	B2	B4	B4	B2	B0	B0
	D20	B3	B5	B5	B3	B1	B1
	D21	B4	B6	B6	B4	B2	B2
	D22	B5	B7	B7	B5	B3	B3
	D24	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	D25	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
	D26	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE

Table 2. Pixel Data Assignment (continued)

SERIAL CHANNEL	DATA BITS	8-BIT			6-BIT	4-BIT	
		FORMAT-1	FORMAT-2	FORMAT-3		NON-LINEAR STEP SIZE	LINEAR STEP SIZE
Y3	D27	R6	R0	GND	GND	GND	GND
	D5	R7	R1	GND	GND	GND	GND
	D10	G6	G0	GND	GND	GND	GND
	D11	G7	G1	GND	GND	GND	GND
	D16	B6	B0	GND	GND	GND	GND
	D17	B7	B1	GND	GND	GND	GND
	D23	RSVD	RSVD	GND	GND	GND	GND
CLKOUT	CLKIN	CLK	CLK	CLK	CLK	CLK	CLK

8.4 Device Functional Modes

8.4.1 Input Clock Edge

The transmission of data bits D0 through D27 occurs as each are loaded into registers upon the edge of the CLKIN signal, where the rising or falling edge of the clock may be selected via CLKSEL. The selection of a clock rising edge occurs by inputting a high level to CLKSEL, which is achieved by populating pull-up resistor to pull CLKSEL=high. Inputting a low level to select a clock falling edge is achieved by directly connecting CLKSEL to GND.

8.4.2 Low Power Mode

The SN65LVDS93B-Q1 can be put in low-power consumption mode by active-low input SHTDN#. Connecting pin SHTDN# to GND will inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low-level on this signal clears all internal registers to a low-level. Populate a pull-up to VCC on SHTDN# to enable the device for normal operation.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section describes the power up sequence, provides information on device connectivity to various GPU and LCD display panels, and offers a PCB routing example.

9.2 Typical Application

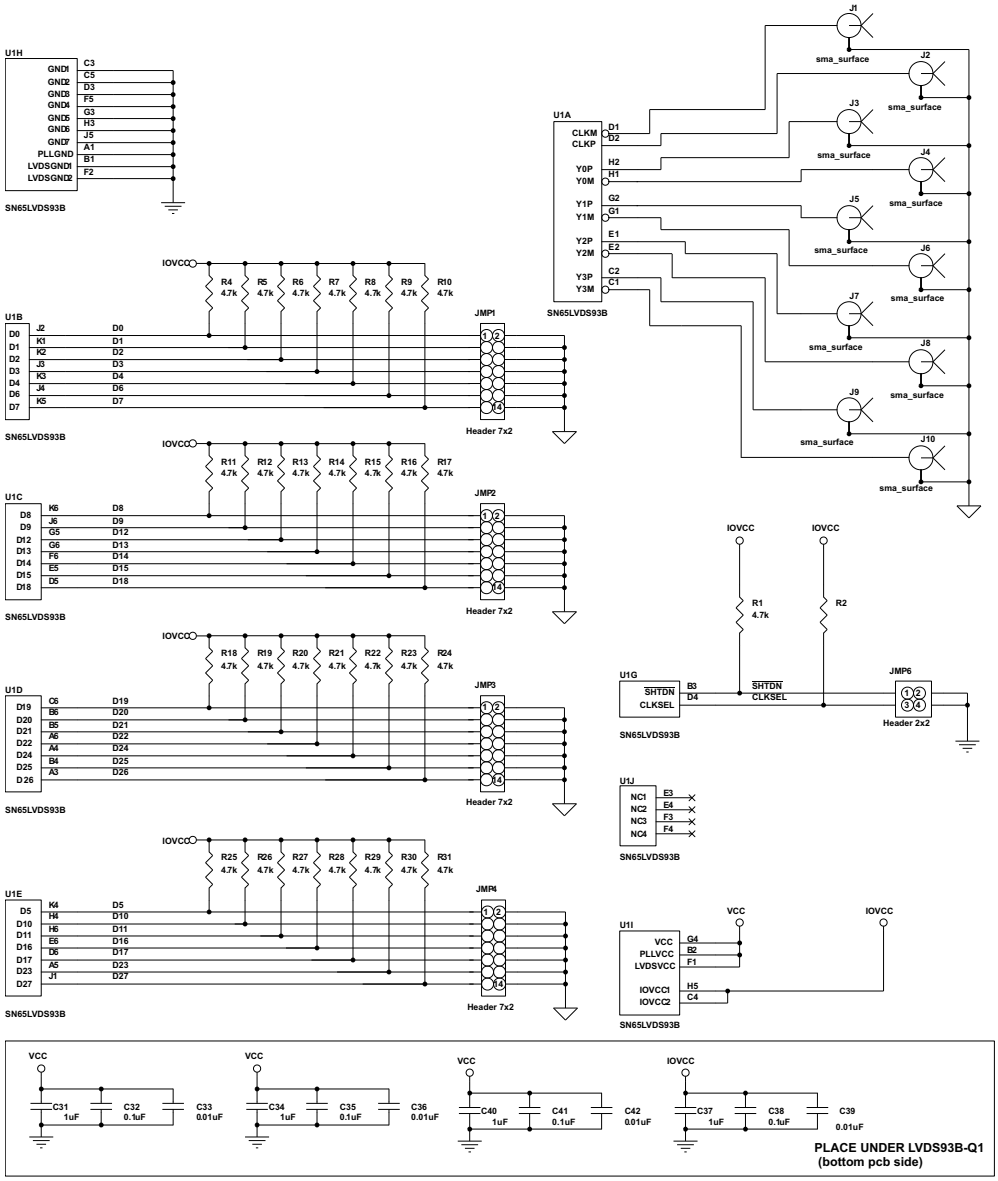


Figure 12. Schematic Example

Typical Application (continued)

9.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
VCC	3.3 V
VCCIO	1.8 V
CLKIN	Falling edge
SHTDN#	High
Format	18-bit GPU to 24-bit LCD

9.2.2 Detailed Design Procedure

9.2.2.1 Power Up Sequence

The SN65LVDS93B-Q1 does not require a specific power up sequence.

It is permitted to power up IOVCC while VCC, VCCPLL, and VCCLVDS remain powered down and connected to GND. The input level of the $\overline{\text{SHTDN}}$ during this time does not matter as only the input stage is powered up while all other device blocks are still powered down.

It is also permitted to power up all 3.3V power domains while IOVCC is still powered down to GND. The device will not suffer damage. However, in this case, all the I/Os are detected as logic HIGH, regardless of their true input voltage level. Hence, connecting $\overline{\text{SHTDN}}$ to GND will still be interpreted as a logic HIGH; the LVDS output stage will turn on. The power consumption in this condition is significantly higher than standby mode, but still lower than normal mode.

The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

Power up sequence (SN65LVDS93B-Q1 $\overline{\text{SHTDN}}$ input initially low):

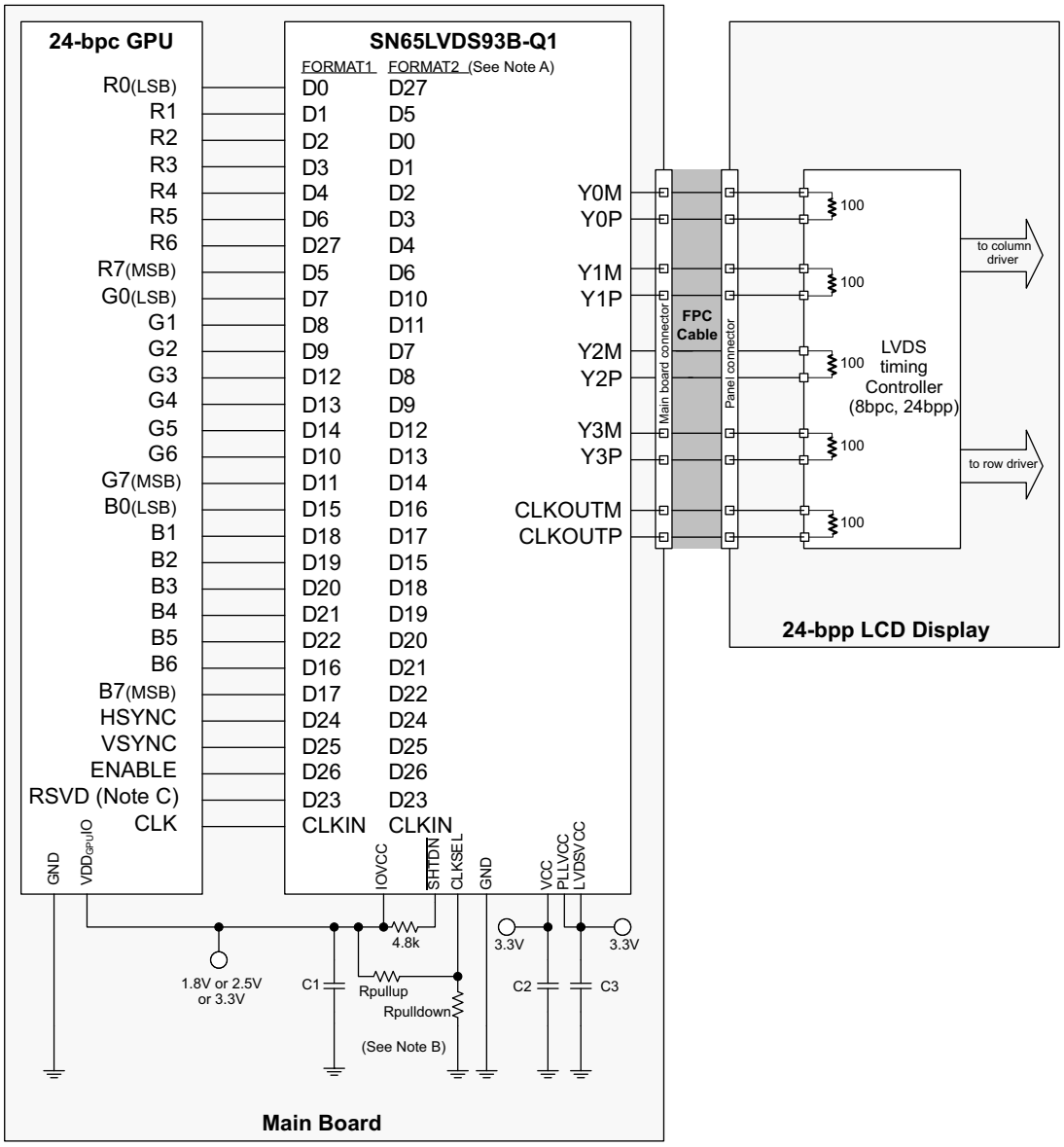
A. Ramp up LCD power (maybe 0.5ms to 10ms) but keep backlight turned off.
B. Wait for additional 0-200ms to ensure display noise won't occur.
C. Enable video source output; start sending black video data.
D. Toggle SN65LVDS93B-Q1 shutdown to $\overline{\text{SHTDN}} = V_{IH}$.
E. Send >1ms of black video data; this allows the SN65LVDS93B-Q1 to be phase locked, and the display to show black data first.
F. Start sending true image data.
G. Enable backlight.

Power Down sequence (SN65LVDS93B-Q1 $\overline{\text{SHTDN}}$ input initially high):

A. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low.
B. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for >2 frame times.
C. Set SN65LVDS93B-Q1 input $\overline{\text{SHTDN}}$ = GND; wait for 250ns.
D. Disable the video output of the video source.
E. Remove power from the LCD panel for lowest system power.

9.2.2.2 Signal Connectivity

While there is no formal industry standardized specification for the input interface of LVDS LCD panels, the industry has aligned over the years on a certain data format (bit order). Figure 13 through Figure 15 show how each signal should be connected from the graphic source through the SN65LVDS93B-Q1 input, output and LVDS LCD panel input. Detailed notes are provided with each figure.



Note A. **FORMAT**: The majority of 24-bit LCD display panels require the two most significant bits (2 MSB) of each color to be transferred over the 4th serial data output Y3. A few 24-bit LCD display panels require the two LSBs of each color to be transmitted over the Y3 output. The system designer needs to verify which format is expected by checking the LCD display data sheet.

- Format 1: use with displays expecting the 2 MSB to be transmitted over the 4th data channel Y3. This is the dominate data format for LCD panels.
- Format 2: use with displays expecting the 2 LSB to be transmitted over the 4th data channel.

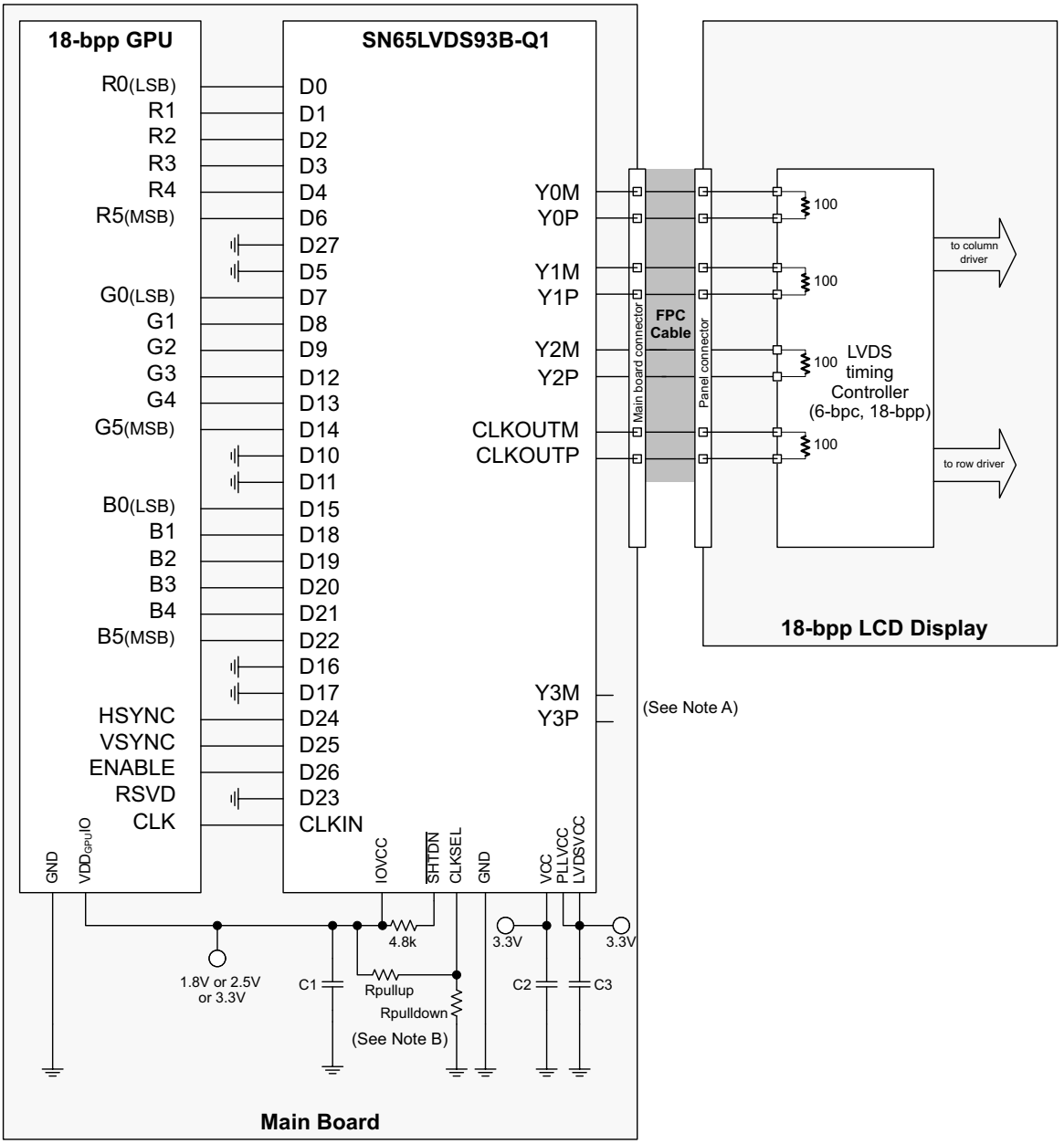
Note B. **Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Note C. If RSVD is not driven to a valid logic level, then an external connection to GND is recommended.

Note D. RSVD must be driven to a valid logic level. All unused SN65LVDS93B-Q1 inputs must be tied to a valid logic level.

Figure 13. 24-Bit Color Host to 24-Bit LCD Panel Application

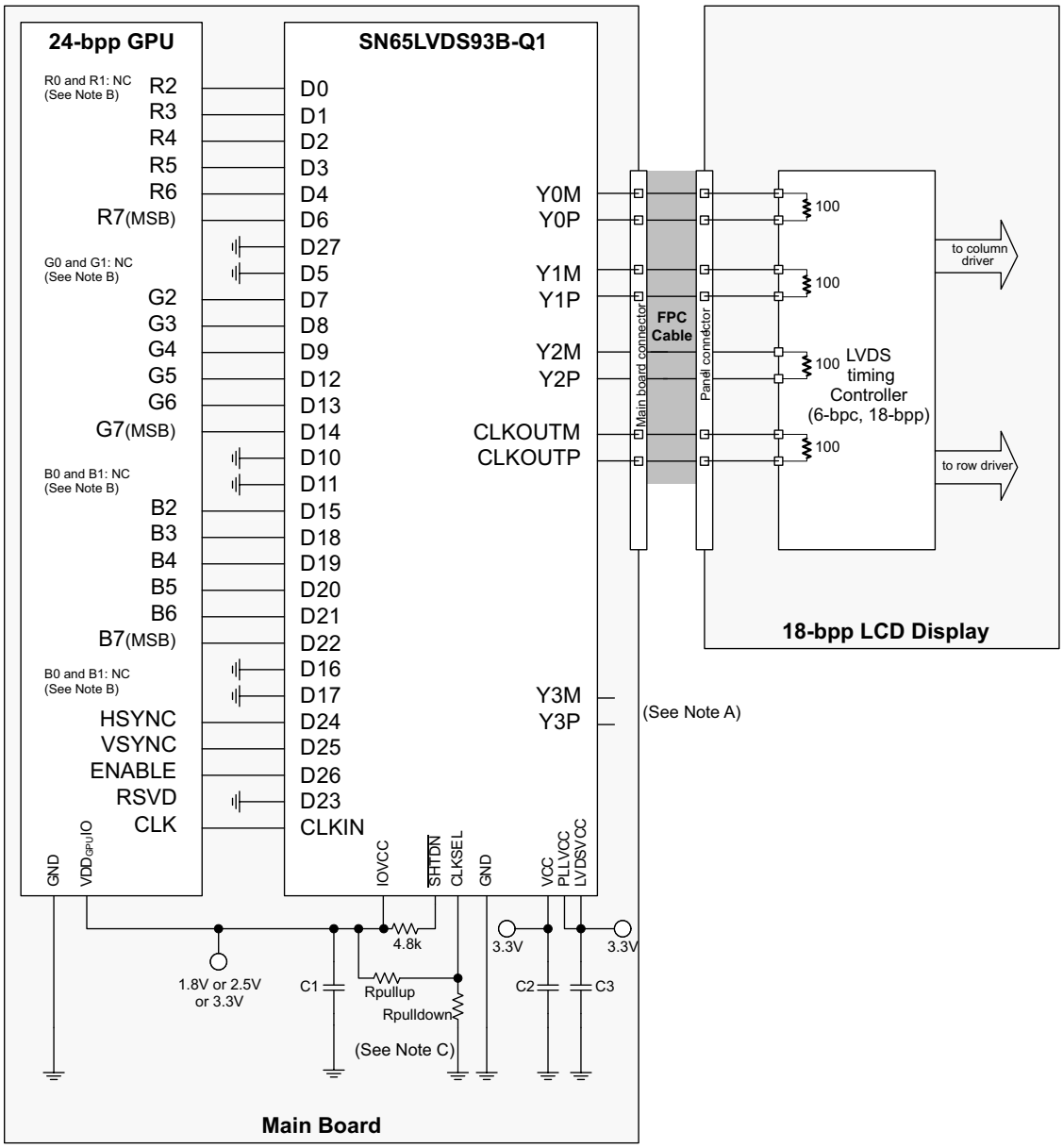


Note A. Leave output Y3 NC.

Note B.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 14. 18-Bit Color Host to 18-Bit Color LCD Panel Display Application



Note A. Leave output Y3 NC.

Note B. **R0, R1, G0, G1, B0, B1**: For improved image quality, the GPU should dither the 24-bit output pixel down to18-bit per pixel.

NoteC.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 15. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application

9.2.2.3 PCB Routing

Figure 16 shows a possible breakout of the data input and output signals on two layers of a printed circuit board.

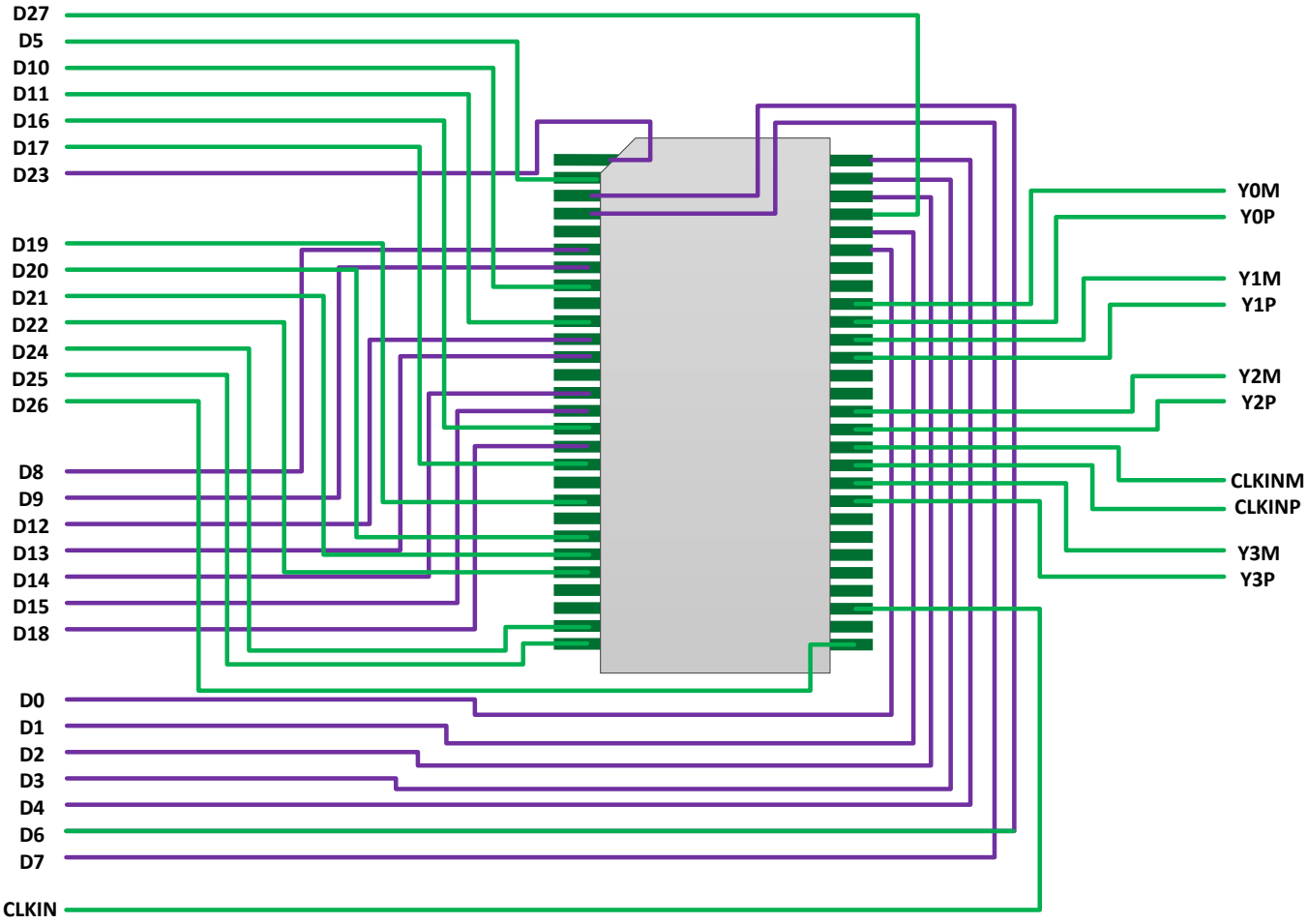


Figure 16. Printed Circuit Board Routing Example (See Figure 12 for the Schematic)

9.2.3 Application Curve

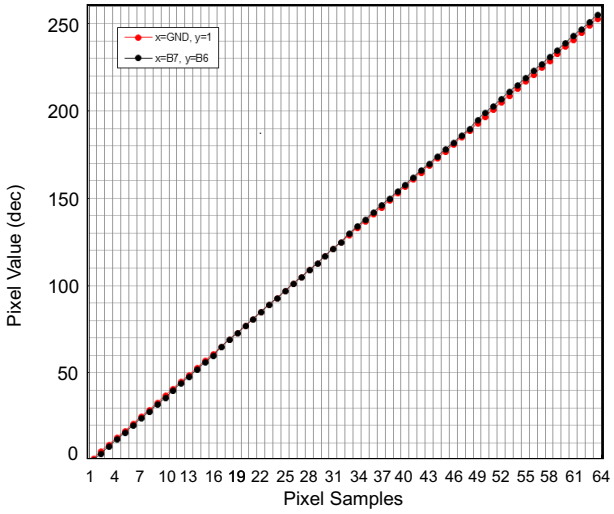


Figure 17. 18b GPU to 24b LCD

10 Power Supply Recommendations

Power supply PLL, IO, and LVDS pins must be uncoupled from each.

11 Layout

11.1 Layout Guidelines

11.1.1 Board Stackup

There is no fundamental information about how many layers should be used and how the board stackup should look. Again, the easiest way the get good results is to use the design from the EVMs of Texas Instruments. The magazine *Elektronik Praxis* has published an article with an analysis of different board stackups. These are listed in Table 3. Generally, the use of microstrip traces needs at least two layers, whereas one of them must be a GND plane. Better is the use of a four-layer PCB, with a GND and a VCC plane and two signal layers. If the circuit is complex and signals must be routed as stripline, because of propagation delay and/or characteristic impedance, a six-layer stackup should be used.

Table 3. Possible Board Stackup on a Four-Layer PCB

	MODEL 1	MODEL 2	MODEL 3	MODEL 4
Layer 1	SIG	SIG	SIG	GND
Layer 2	SIG	GND	GND	SIG
Layer 3	VCC	VCC	SIG	VCC
Layer 4	GND	SIG	VCC	SIG
Decoupling	Good	Good	Bad	Bad
EMC	Bad	Bad	Bad	Bad
Signal Integrity	Bad	Bad	Good	Bad
Self Disturbance	Satisfaction	Satisfaction	Satisfaction	High

11.1.2 Power and Ground Planes

A complete ground plane in high-speed design is essential. Additionally, a complete power plane is recommended as well. In a complex system, several regulated voltages can be present. The best solution is for every voltage to have its own layer and its own ground plane. But this would result in a huge number of layers just for ground and supply voltages. What are the alternatives? Split the ground planes and the power planes? In a mixed-signal design, e.g., using data converters, the manufacturer often recommends splitting the analog ground and the digital ground to avoid noise coupling between the digital part and the sensitive analog part. Take care when using split ground planes because:

- Split ground planes act as slot antennas and radiate.
- A routed trace over a gap creates large loop areas, because the return current cannot flow beside the signal, and the signal can induce noise into the nonrelated reference plane (Figure 18).
- With a proper signal routing, crosstalk also can arise in the return current path due to discontinuities in the ground plane. Always take care of the return current (Figure 19).

For Figure 19, do not route a signal referenced to digital ground over analog ground and vice versa. The return current cannot take the direct way along the signal trace and so a loop area occurs. Furthermore, the signal induces noise, due to crosstalk (dotted red line) into the analog ground plane.

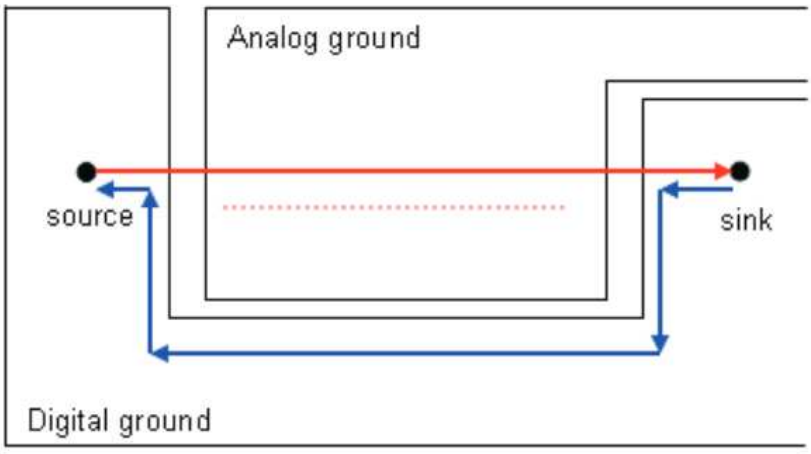


Figure 18. Loop Area and Crosstalk Due to Poor Signal Routing and Ground Splitting

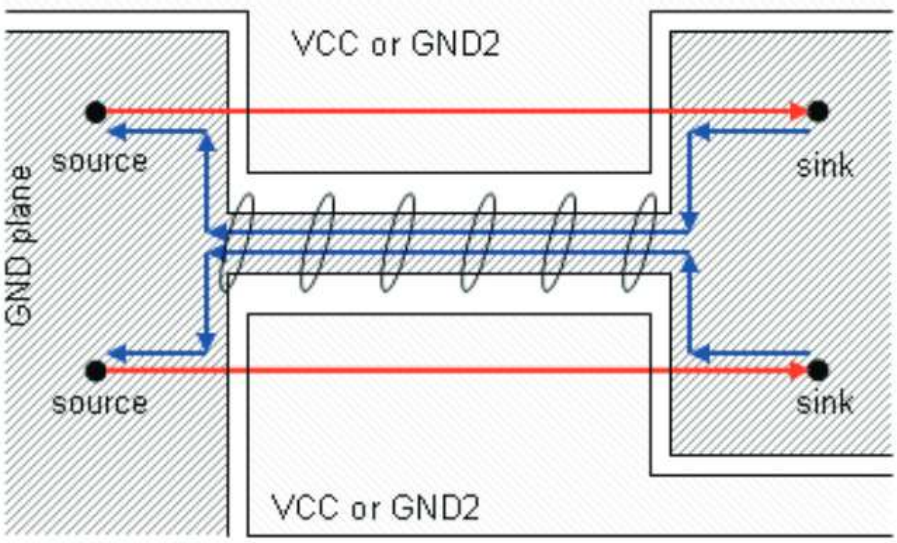


Figure 19. Crosstalk Induced by the Return Current Path

11.1.3 Traces, Vias, and Other PCB Components

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner, and the characteristic impedance changes. This impedance change causes reflections.

- Avoid right-angle bends in a trace and try to route them at least with two 45° corners. To minimize any impedance change, the best routing would be a round bend (see Figure 20).
- Separate high-speed signals (e.g., clock signals) from low-speed signals and digital from analog signals; again, placement is important.
- To minimize crosstalk not only between two signals on one layer but also between adjacent layers, route them with 90° to each other.

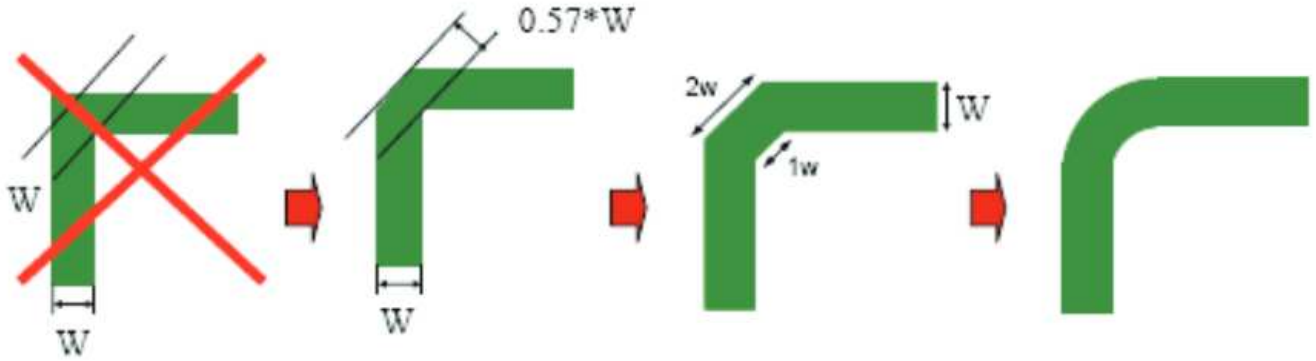


Figure 20. Poor and Good Right Angle Bends

11.2 Layout Example

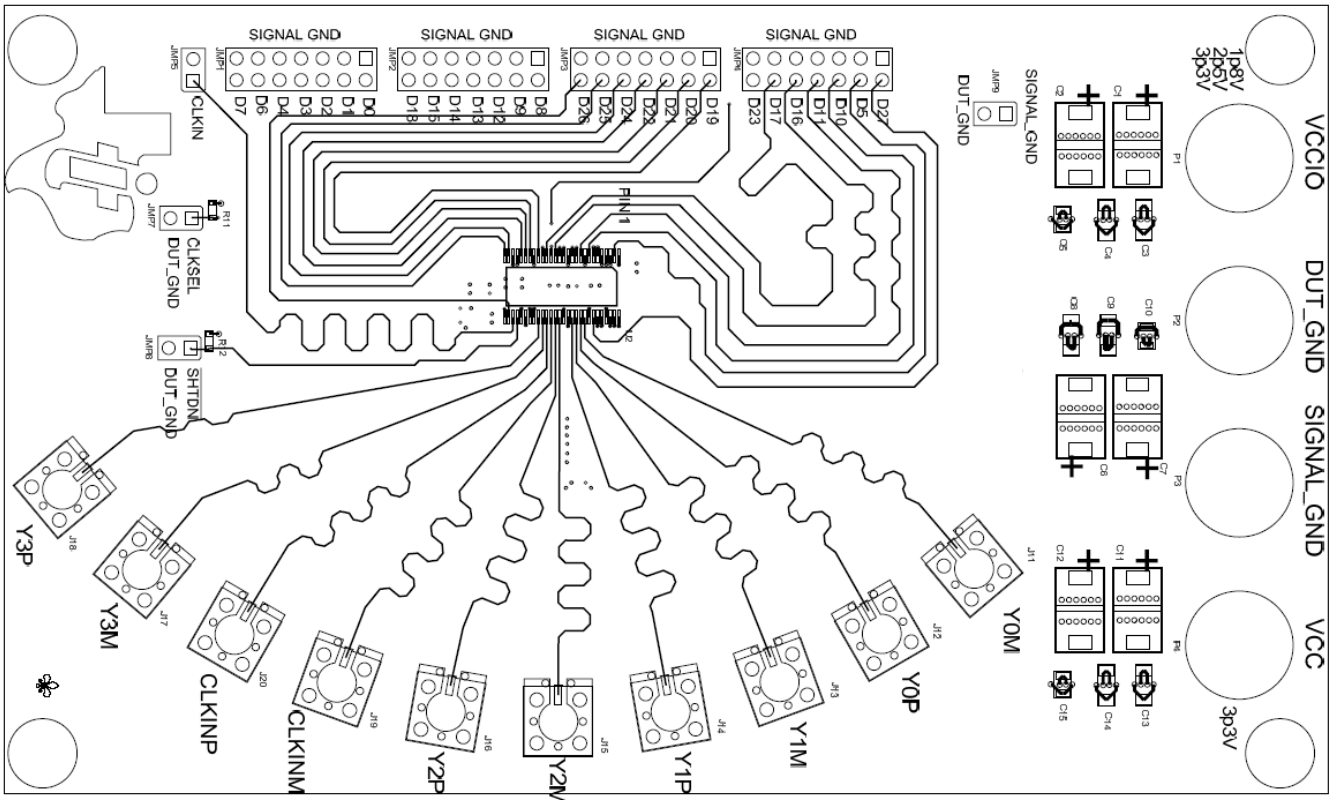


Figure 21. EVM Top Layer – TSSOP Package

Layout Example (continued)

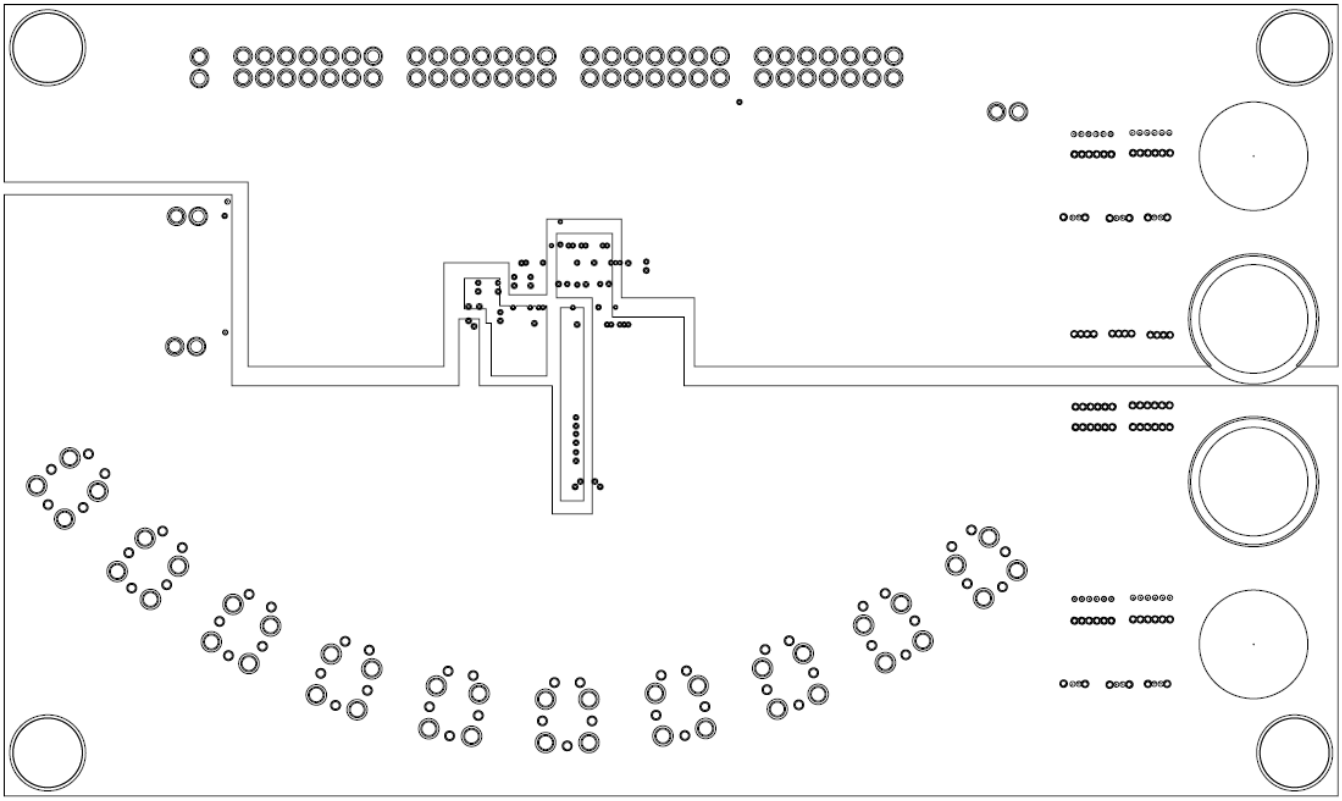


Figure 22. EVM VCC Layer – TSSOP Package

12 Device and Documentation Support

12.1 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS93BIDGGRQ1	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS93BQ
SN65LVDS93BIDGGRQ1.A	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS93BQ
SN65LVDS93BIDGGTQ1	Active	Production	TSSOP (DGG) | 56	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS93BQ
SN65LVDS93BIDGGTQ1.A	Active	Production	TSSOP (DGG) | 56	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS93BQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN65LVDS93B-Q1 :

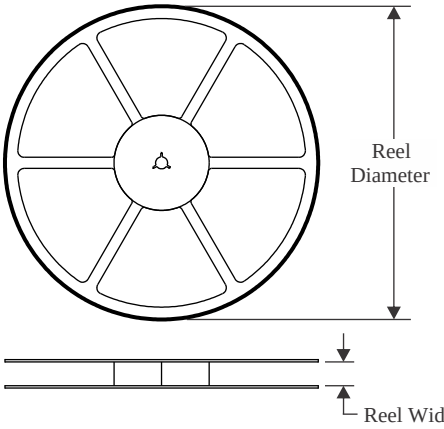
- Catalog : SN65LVDS93B

NOTE: Qualified Version Definitions:

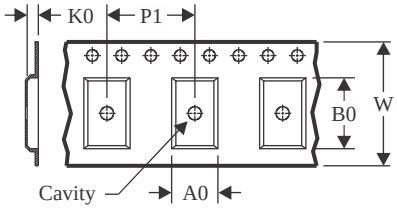
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

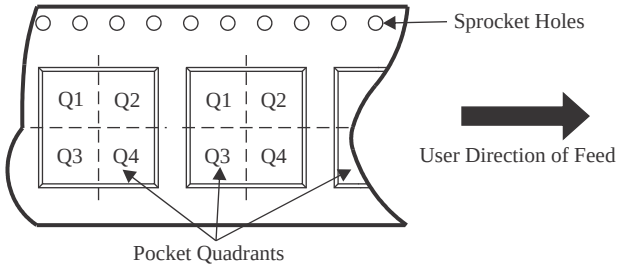


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

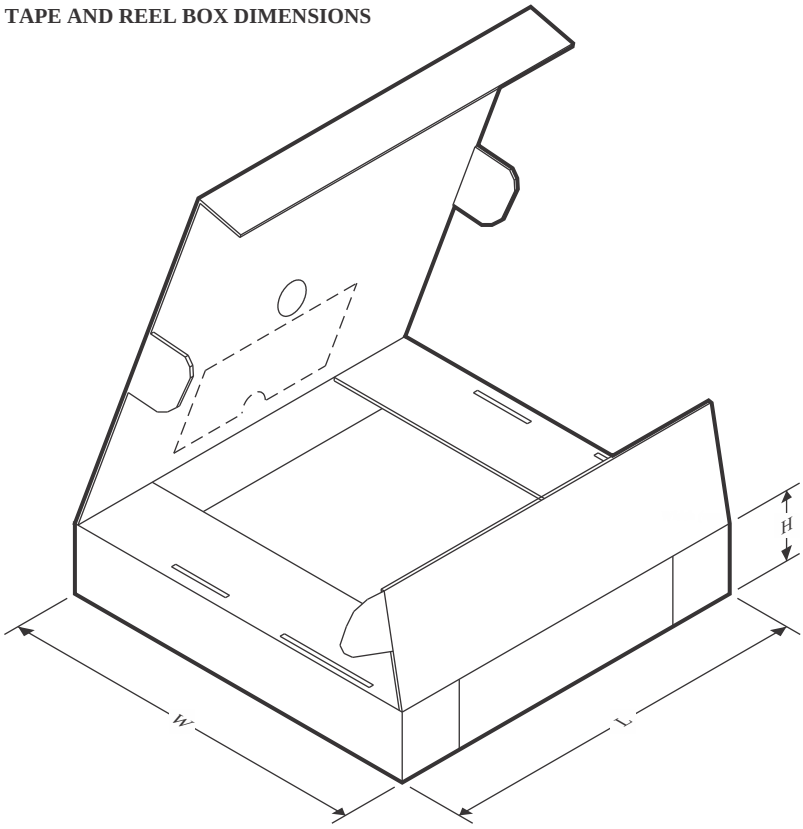
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS93BIDGGRQ1	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN65LVDS93BIDGGTQ1	TSSOP	DGG	56	250	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

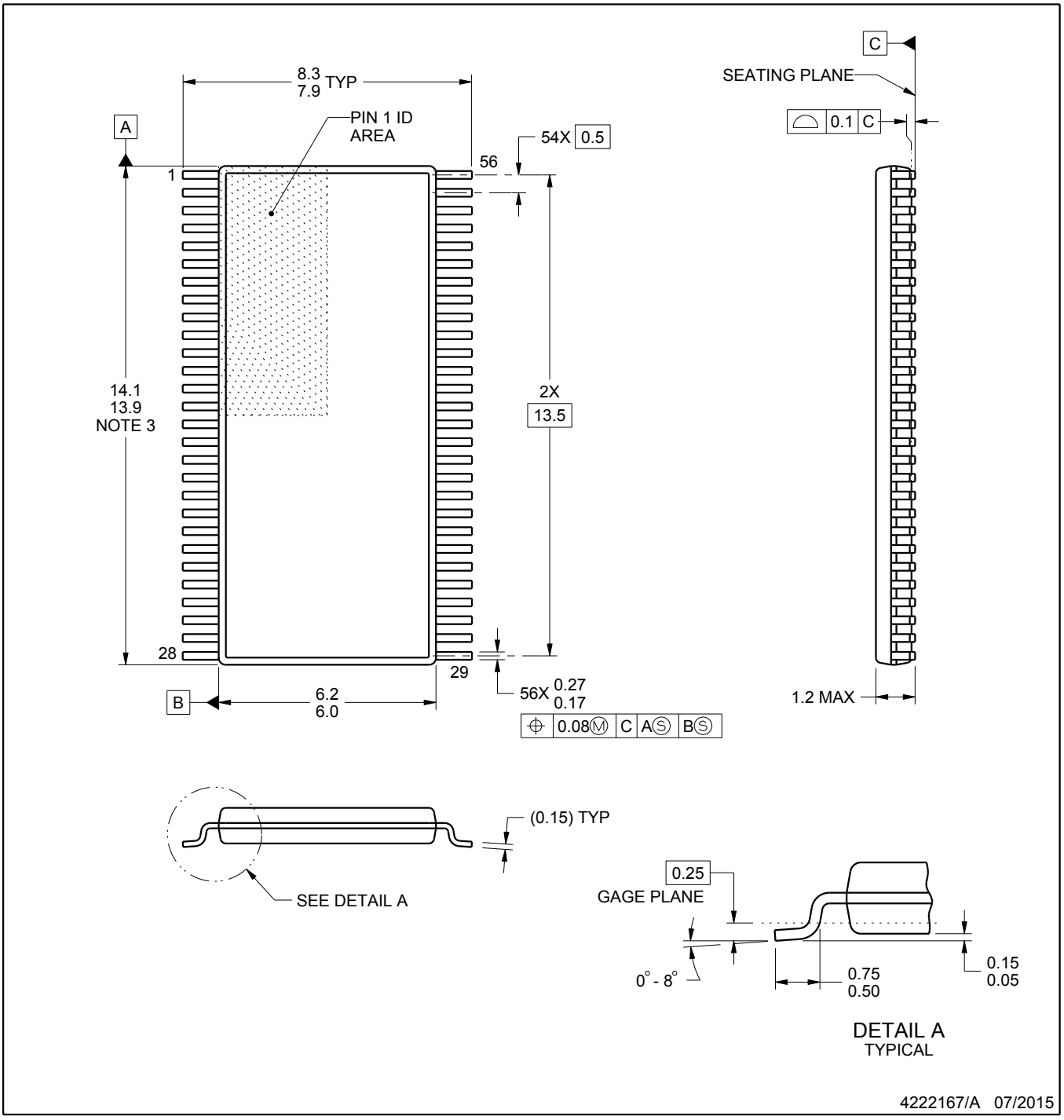
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS93BIDGGRQ1	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN65LVDS93BIDGGTQ1	TSSOP	DGG	56	250	356.0	356.0	45.0

PACKAGE OUTLINE

DGG0056A

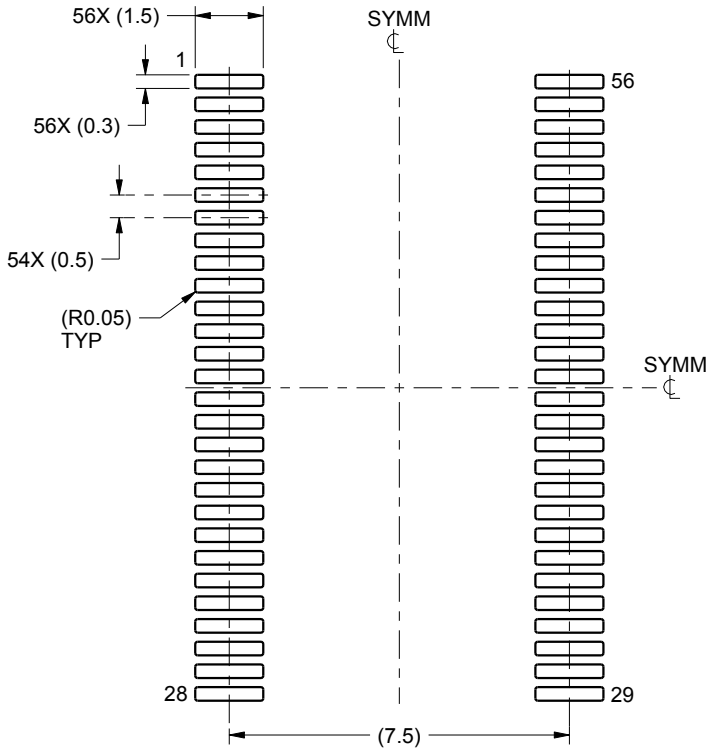
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

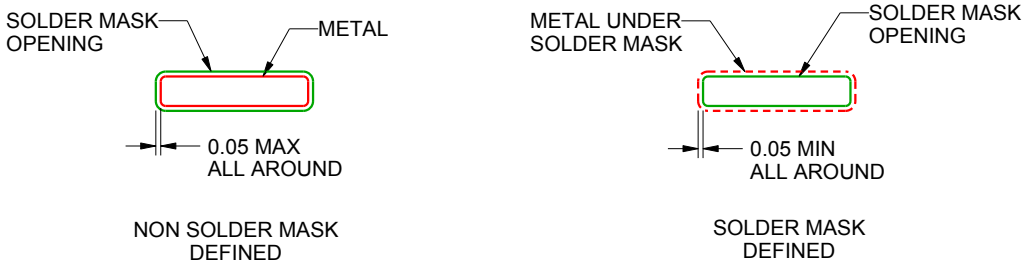


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

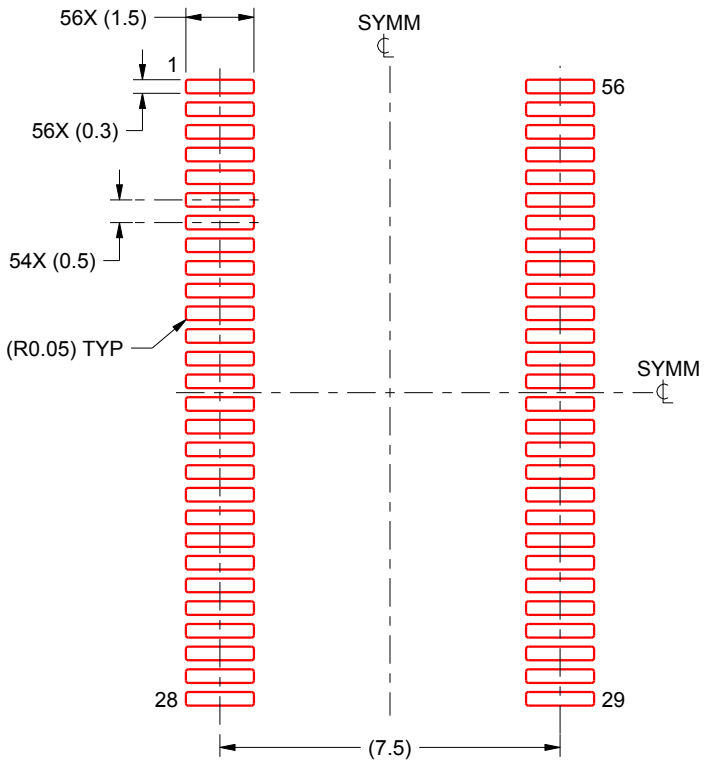


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025