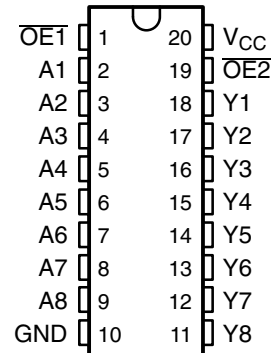# SN74ABT541B-Q1
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCBS762A – JUNE 2003 – REVISED JANUARY 2008

- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 150 V Using Machine Model (C = 200 pF, R = 0)**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) <1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**

PW PACKAGE
(TOP VIEW)

$\overline{OE1}$	1	20	V_{CC}
A1	2	19	$\overline{OE2}$
A2	3	18	Y1
A3	4	17	Y2
A4	5	16	Y3
A5	6	15	Y4
A6	7	14	Y5
A7	8	13	Y6
A8	9	12	Y7
GND	10	11	Y8

description

The SN74ABT541B octal buffer and line driver is ideal for driving bus lines or buffering memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW	Tape and reel	SN74ABT541BIPWRQ1	AB541IQ1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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EPIC-IIB is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

1

SN74ABT541B-Q1
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS
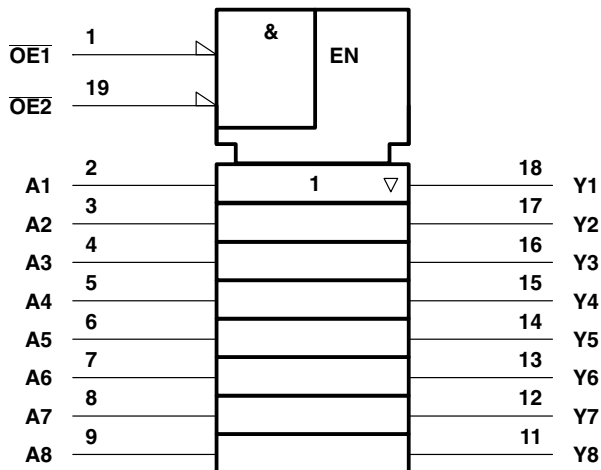
logic symbol[†]

logic diagram (positive logic)

To Seven Other Channels
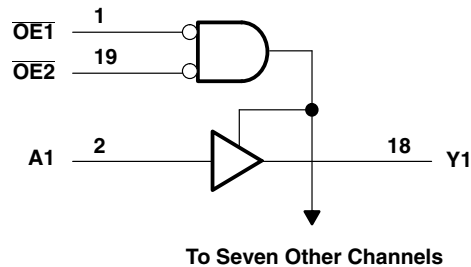
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O .... −0.5 V to 5.5 V
Current into any output in the low state, I_O .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA
Package thermal impedance, θ_{JA} (see Note 2) .... 128°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$T_A = 25°C$ MIN	$T_A = 25°C$ TYP[†]	$T_A = 25°C$ MAX	MIN	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2		−1.2	V
V_{OH}	$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA	2.5			2.5		
	$V_{CC} = 5$ V,	$I_{OH} = -3$ mA	3			3		V
	$V_{CC} = 4.5$ V	$I_{OH} = -32$ mA	2			2		
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 64$ mA			0.55		0.55	V
V_{hys}				100				mV
I_I	$V_{CC} = 5.5$ V,	$V_I = V_{CC}$ or GND			±1		±1	µA
I_{OZPU}	$V_{CC} = 0$ to 2.1 V, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$				±50		±50	µA
I_{OZPD}	$V_{CC} = 2.1$ V to 0, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$				±50		±50	µA
I_{OZH}	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			10		10	µA
I_{OZL}	$V_{CC} = 5.5$ V,	$V_O = 0.5$ V			−10		−10	µA
I_{off}	$V_{CC} = 0$,	V_I or $V_O \leq 4.5$ V			±100		±100	µA
I_{CEX}	$V_{CC} = 5.5$ V, $V_O = 5.5$ V	Outputs high			50		50	µA
I_O[‡]	$V_{CC} = 5.5$ V,	$V_O = 2.5$ V	−50	−140	−180	−50	−180	mA
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high		5	250		250	µA
		Outputs low		22	30		30	mA
		Outputs disabled		1	250		250	µA
ΔI_{CC}[§]	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1.5		1.5	mA
		Outputs disabled			50		50	µA
		Control inputs			1.5		1.5	mA
C_i	$V_I = 2.5$ V or 0.5 V			3				pF
C_o	$V_O = 2.5$ V or 0.5 V			6				pF

† All typical values are at $V_{CC} = 5$ V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25°C$ MIN	$V_{CC} = 5$ V, $T_A = 25°C$ TYP	$V_{CC} = 5$ V, $T_A = 25°C$ MAX	MIN	MAX	UNIT
t_{PLH}	A	Y	1	2	3.2	1	3.6	ns
t_{PHL}			1	2.6	3.5	1	3.9	
t_{PZH}	$\overline{OE}$	Y	2	3.5	4.5	2	4	ns
t_{PZL}			1.9	4	5.1	1.9	5.9	
t_{PHZ}	$\overline{OE}$	Y	2.2	4.4	5.4	2.2	5.8	ns
t_{PLZ}			1.5	3	4	1.5	4.4	
$t_{sk(o)}$[¶]					0.5		0.5	ns

¶ Skew between any two outputs of the same package switching in the same direction

PARAMETER MEASUREMENT INFORMATION
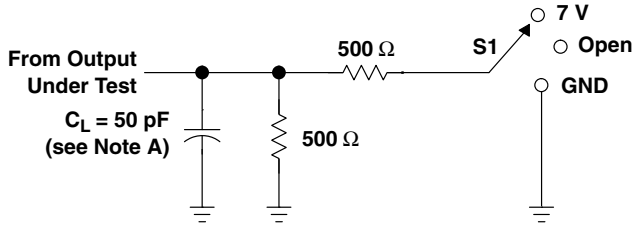
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT
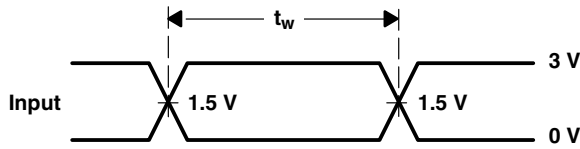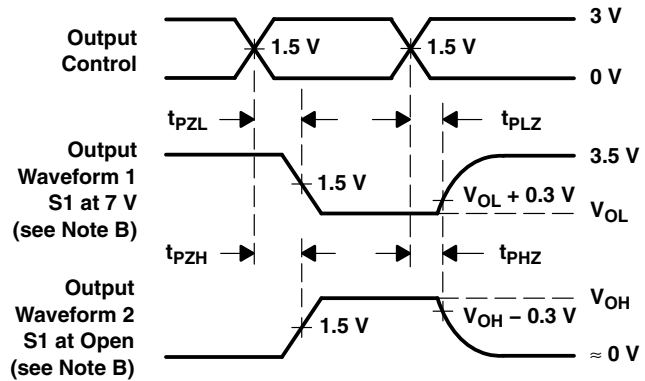
VOLTAGE WAVEFORMS
PULSE DURATION
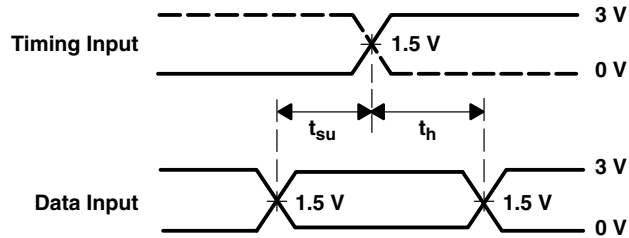
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
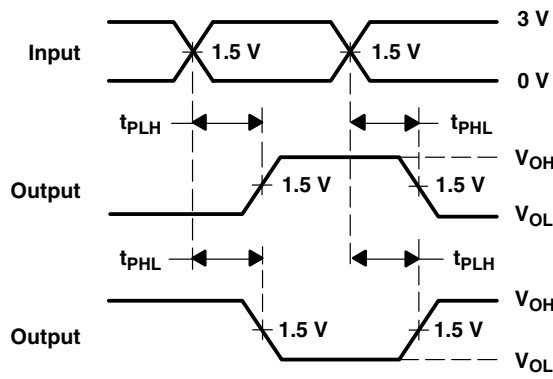
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
  B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
    Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
  D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CABT541BIPWRG4Q1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB541IQ1	Samples
SN74ABT541BIPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB541IQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74ABT541B-Q1 :

● Catalog: SN74ABT541B

● Enhanced Product: SN74ABT541B-EP

NOTE: Qualified Version Definitions:

    ● Catalog - TI's standard catalog product

    ● Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

| Q1 | Q2 |
| Q3 | Q4 |

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CABT541BIPWRG4Q1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CABT541BIPWRG4Q1	TSSOP	PW	20	2000	356.0	356.0	35.0

4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK OPENING
METAL
EXPOSED METAL
0.05 MAX
ALL AROUND
NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER SOLDER MASK
SOLDER MASK OPENING
EXPOSED METAL
0.05 MIN
ALL AROUND
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220206/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.5)

SYMM

(R0.05) TYP

1

20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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