

## SN74AC241 Octal Buffers/Drivers with 3-State Outputs

### 1 Features

- Operation of 2V to 6V  $V_{CC}$
- Inputs accept voltages to 6V
- Max  $t_{pd}$  of 7.5ns at 5V

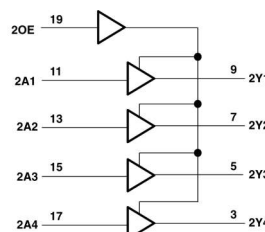
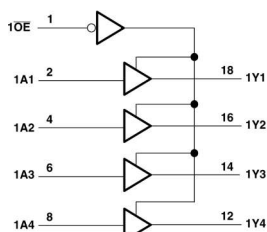
### 2 Description

These octal buffers and line drivers are designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

#### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
SN74AC241	N (PDIP, 20)	24.33mm × 9.4mm	24.33mm × 6.35mm
	DW (SOIC, 20)	12.8mm × 10.3mm	12.8mm × 7.5mm
	NS (SOP, 20)	12.6mm × 7.8mm	12.6mm × 5.3mm
	DB (SSOP, 20)	7.2mm × 7.8mm	7.2mm × 5.3mm
	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm × 4.4mm

- (1) For more information, see [Section 10](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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### 3 Pin Configuration and Functions

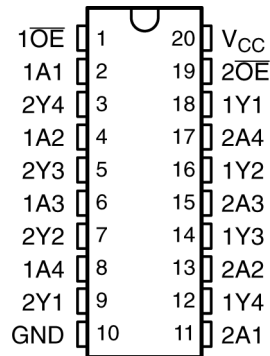


Figure 3-1. SN54AC241 DB, DW, N, NS, Or PW Package (Top View)

Table 3-1. Pin Functions

NAME <sup>1</sup>	PIN	TYPE	DESCRIPTION
1OE	1	I	Output enable 1
1A1	2	I	1A1 input
2Y4	3	O	2Y4 output
1A2	4	I	1A2 input
2Y3	5	O	2Y3 output
1A3	6	I	1A3 input
2Y2	7	O	2Y2 output
1A4	8	I	1A4 input
2Y1	9	O	2Y1 output
GND	10	—	Ground pin
2A1	11	I	2A1 input
1Y4	12	O	1Y4 output
2A2	13	I	2A2 input
1Y3	14	O	1Y3 output
2A3	15	I	2A3 input
1Y2	16	O	1Y2 output
2A4	17	I	2A4 input
1Y1	18	O	1Y1 output
2OE	19	I	Output enable 2
VCC	20	—	Power pin

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub> <sup>1</sup>	Input voltage range	-0.5	V <sub>CC</sub> +0.5	V
V <sub>O</sub> <sup>1</sup>	Output voltage range	-0.5	V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	Input clamp current	(V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> )	±20	mA
I <sub>OK</sub>	Output clamp current	(V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20	mA
I <sub>O</sub>	Continuous output current	(V <sub>O</sub> = 0 or V <sub>CC</sub> )	±50	mA
	Continuous current through V <sub>CC</sub> or GND		±200	mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>cc</sub> = 3 V	2.1	V
		V <sub>cc</sub> = 4.5 V	3.15	
		V <sub>cc</sub> = 5.5 V	3.85	
V <sub>IL</sub>	Low-level input voltage	V <sub>cc</sub> = 3 V	0.9	V
		V <sub>cc</sub> = 4.5 V	1.35	
		V <sub>cc</sub> = 5.5 V	1.65	
V <sub>I</sub>	Input voltage	0	V <sub>cc</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>cc</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>cc</sub> = 3 V	-12	mA
		V <sub>cc</sub> = 4.5 V	-24	
		V <sub>cc</sub> = 5.5 V	-24	
I <sub>OL</sub>	Low-level output current	V <sub>cc</sub> = 3 V	12	mA
		V <sub>cc</sub> = 4.5 V	24	
		V <sub>cc</sub> = 5.5 V	24	
Δt/Δv	Input transition rise or fall rate		8	ns/V
T <sub>a</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### 4.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>	DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SOP)	PW (TSSOP)	UNIT
	20 PINS					
R <sub>θJA</sub>	70	58	69	60	126.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN74AC241		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>oh</sub> = -50 μA	3 V	2.9			2.9	V	
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I <sub>oh</sub> = -12 mA	3 V	2.56			2.46		
		4.5 V	3.86			3.76		
	I <sub>oh</sub> = -24 mA	5.5 V	4.86			4.76		
		5.5 V						
V <sub>OL</sub>	I <sub>ol</sub> = 50 μA	3 V				0.1	V	
		4.5 V				0.1		
		5.5 V				0.1		
	I <sub>ol</sub> = 12 mA	3 V				0.36		0.44
		4.5 V				0.36		0.44
	I <sub>ol</sub> = 24 mA	5.5 V				0.36		0.44
		5.5 V						
	I <sub>ol</sub> = 50 mA <sup>(1)</sup>	5.5 V						
	I <sub>ol</sub> = 75 mA <sup>(1)</sup>	5.5 V						1.65
	I <sub>I</sub>	Data inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V				±0.1
Control inputs		V <sub>I</sub> = V <sub>CC</sub> or GND				±0.1	±1	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I(OE)</sub> = V <sub>IL</sub> or V <sub>IH</sub>		5.5 V			±0.25	±2.5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		5.5 V			4	40	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		5 V	2.5				pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

## 4.5 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			SN74AC241		UNIT
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	1.5	6	9	1.5	10	ns
t <sub>PHL</sub>			1.5	6	9	1	10.5	
t <sub>PZH</sub>	OE or OE	Y	1.5	6.5	12.5	1	13	ns
t <sub>PZL</sub>			1.5	7	12	1.5	13	
t <sub>PHZ</sub>	OE or OE	Y	2	8	12	2	12.5	ns
t <sub>PLZ</sub>			1.5	7	12.5	1	13.5	

## 4.6 Switching Characteristics, V<sub>CC</sub> = 5 V ± 0.5 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			SN74AC241		UNIT
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	1.5	5	7	1	7.5	ns
t <sub>PHL</sub>			1.5	4.5	7	1	7.5	

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 over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

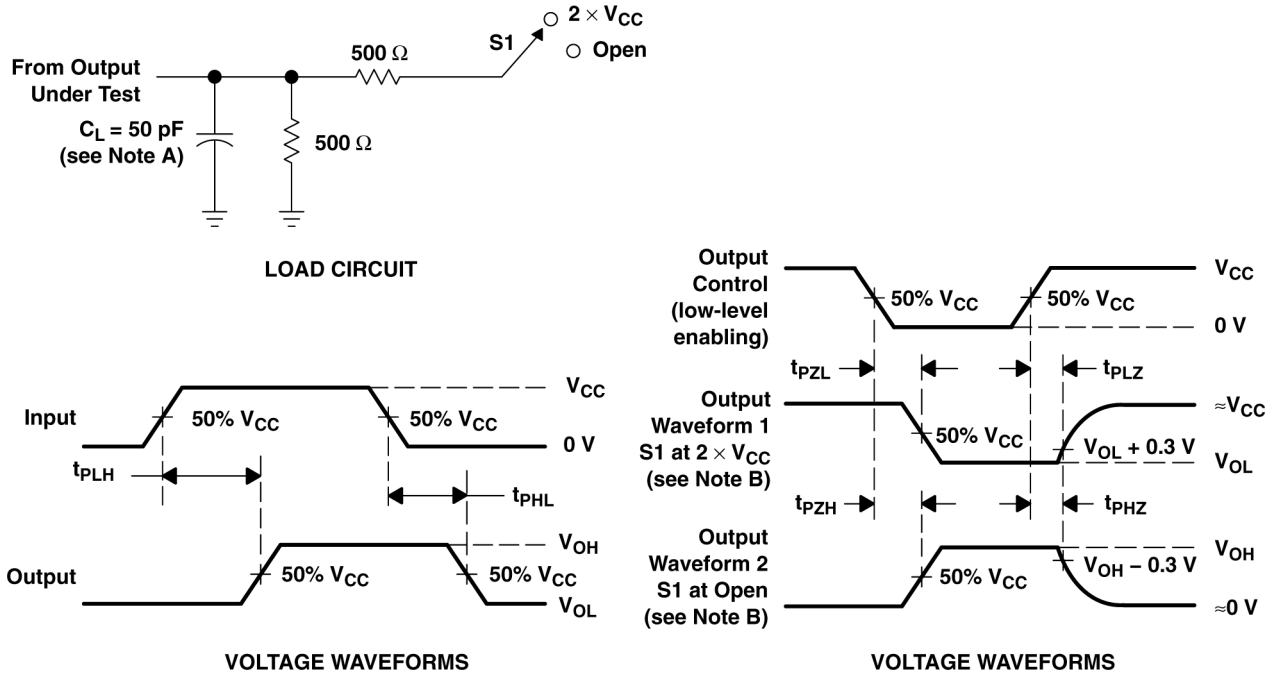
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN74AC241		UNIT
			MIN	TYP	MAX	MIN	MAX	
$t_{PZH}$	$\overline{OE}$ or OE	Y	1.5	5.5	9	1	9.5	ns
$t_{PZL}$			1.5	5.5	9	1	9.5	
$t_{PHZ}$	$\overline{OE}$ or OE	Y	1.5	6.5	10	1	10.5	ns
$t_{PLZ}$			1.5	6	10	1	10.5	

## 4.7 Operating Characteristics

 $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per buffer/driver	$C_1 = 50\text{ pF}$ , $f = 1\text{ MHz}$	45	pF

## 5 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.

**Figure 5-1. Load Circuit and Voltage Waveforms**

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open

## 6 Detailed Description

### 6.1 Overview

The 'AC241 devices are organized as two 4-bit buffers/drivers with separate complementary output-enable ( $\overline{1OE}$  and  $2OE$ ) inputs. When  $\overline{1OE}$  is low or  $2OE$  is high, the device passes noninverted data from the A inputs to the Y outputs. When  $\overline{1OE}$  is high or  $2OE$  is low, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor and  $OE$  should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking or the current-sourcing capability of the driver.

### 6.2 Functional Block Diagram

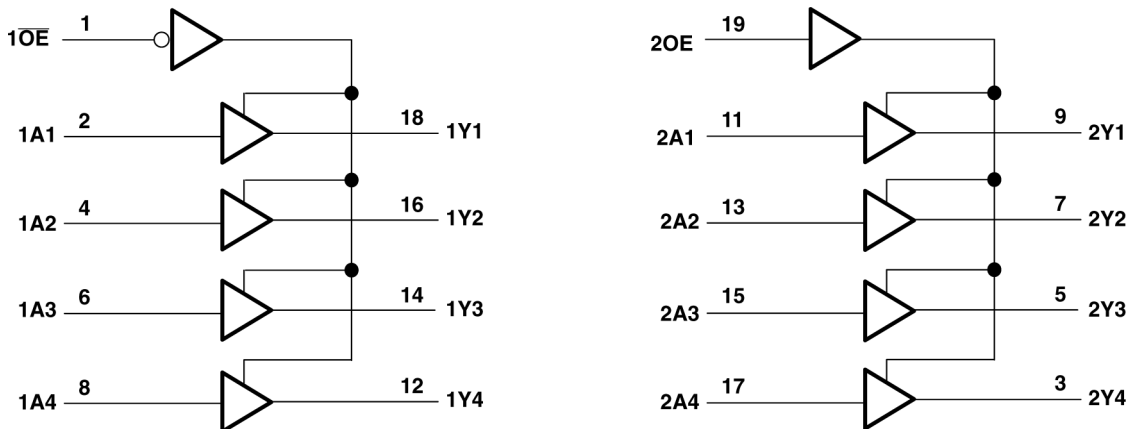


Figure 6-1. Logic Diagram (Positive Logic)

### 6.3 Device Functional Modes

Table 6-1. Function Tables

INPUTS		OUTPUT 1Y
$\overline{1OE}$	1A	
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT 2Y
2OE	2A	
H	H	H
H	L	L
L	X	Z

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in [Section 4.2](#).

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1  $\mu\text{F}$  and if there are multiple  $V_{CC}$  terminals, then TI recommends .01  $\mu\text{F}$  or .022  $\mu\text{F}$  for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

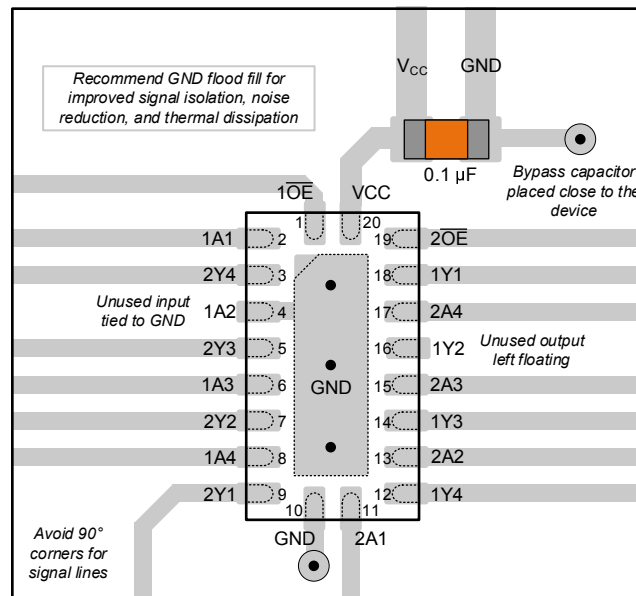
### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

##### 7.2.1.1 Layout Example



**Figure 7-1. Example Layout for the SN74AC241**

## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 8-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AC241	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

Changes from Revision F (May 2023) to Revision G (March 2024)	Page
• Updated high-level input voltage values in <i>Recommended Operating Conditions</i> table.....	4
• Updated R $\theta$ JA value: PW = 83 to 126.2, all values in °C/W .....	4

Changes from Revision E (October 2003) to Revision F (May 2023)	Page
• Added <i>Package Information</i> table, <i>Pin Functions</i> table, and <i>Thermal Information</i> table.....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74AC241DBR</a>	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC241
SN74AC241DBR.A	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC241
<a href="#">SN74AC241DW</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-40 to 85	AC241
<a href="#">SN74AC241DWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC241
SN74AC241DWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC241
<a href="#">SN74AC241N</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC241N
SN74AC241N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC241N
<a href="#">SN74AC241NSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC241
SN74AC241NSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC241
<a href="#">SN74AC241PW</a>	Obsolete	Production	TSSOP (PW)   20	-	-	Call TI	Call TI	-40 to 85	AC241
<a href="#">SN74AC241PWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC241
SN74AC241PWR.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC241

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

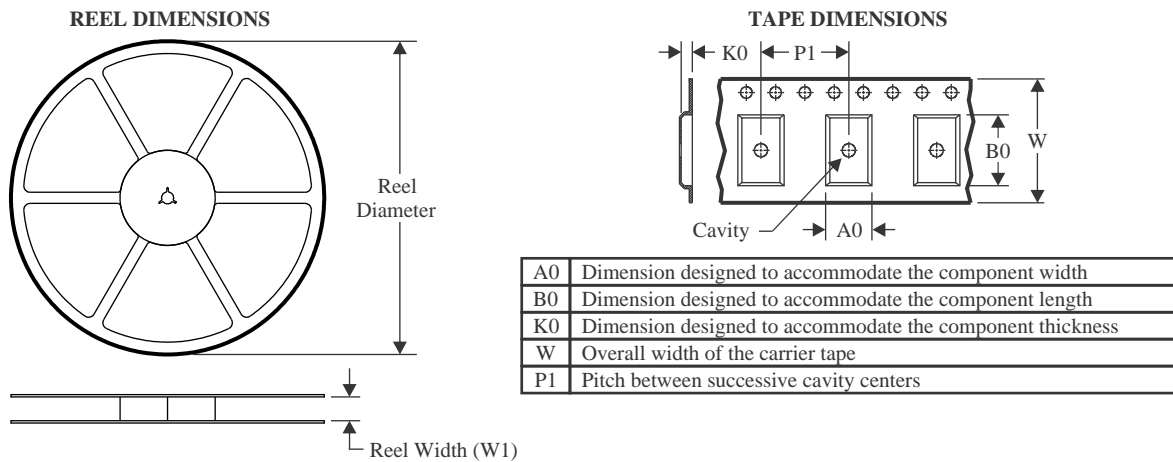
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

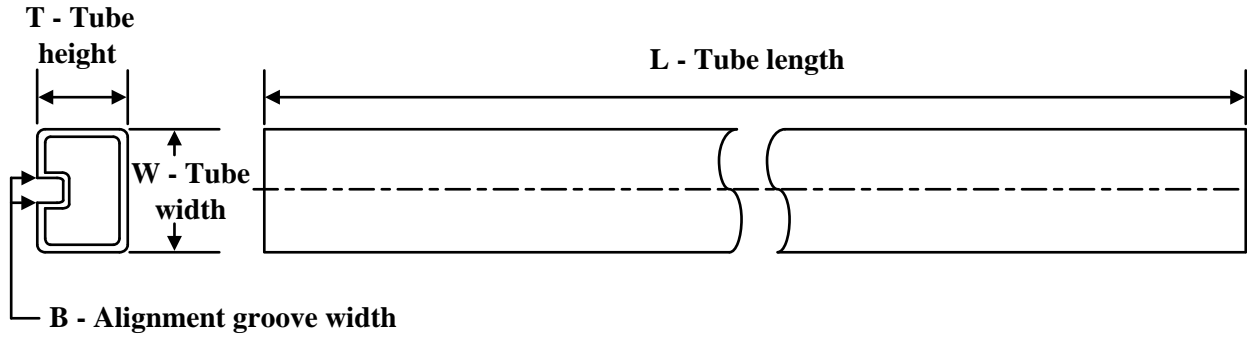

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC241DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC241DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AC241NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AC241PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC241DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AC241DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AC241NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AC241PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AC241N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AC241N.A	N	PDIP	20	20	506	13.97	11230	4.32

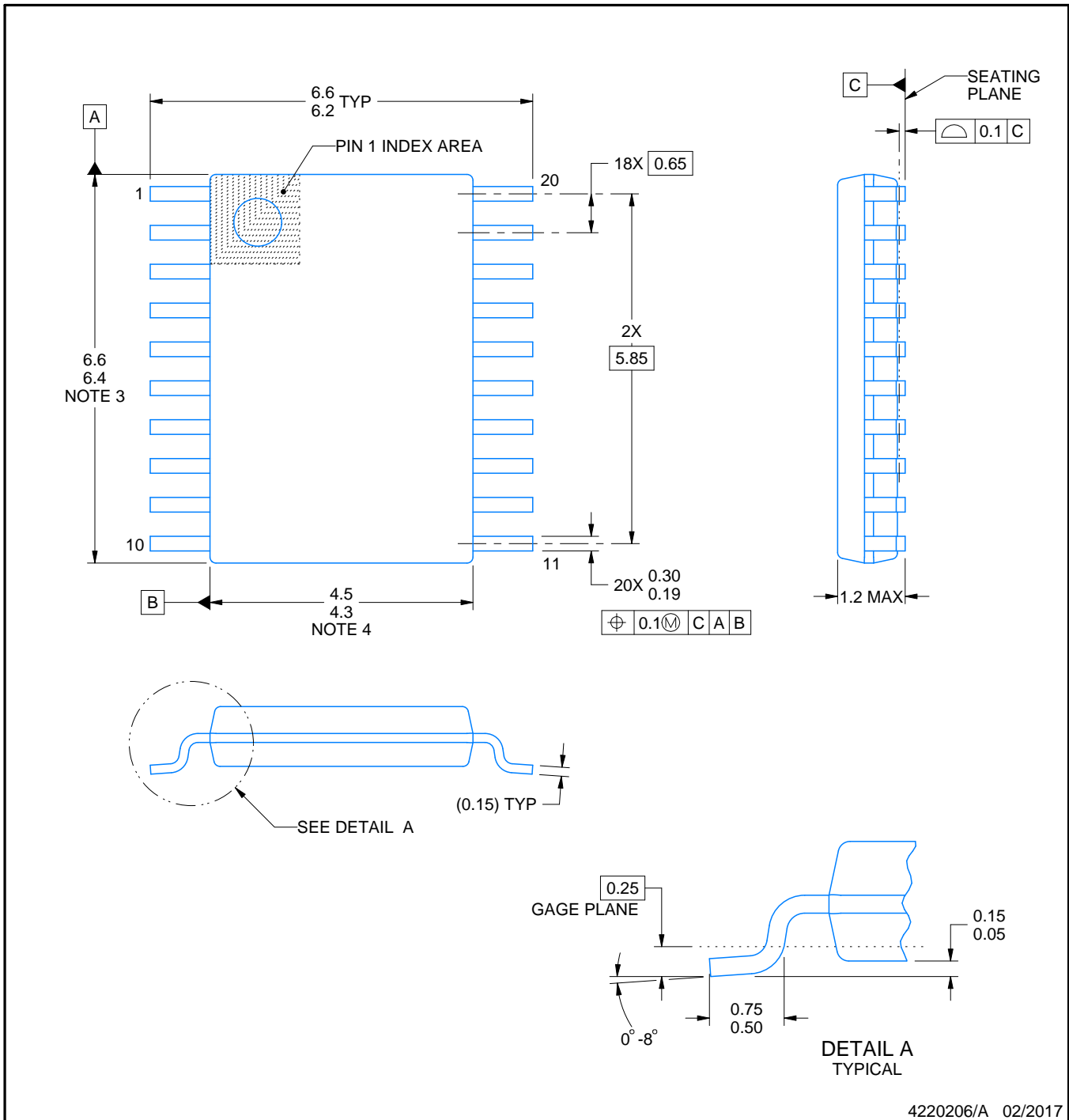
PW0020A



# PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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