

## SN74AHC139 Dual 2- to 4-Bit Decoders/Demultiplexers

### 1 Features

- Operating range 2V to 5.5V
- Designed specifically for high-speed memory decoders and data-transmission systems
- Incorporate two enable inputs to simplify cascading or data reception
- Latch-up performance exceeds 250mA per JESD 17
- ESD protection exceeds JESD 22:
  - 2000V human-body model (A114-A)
  - 1000V charged-device model (C101)

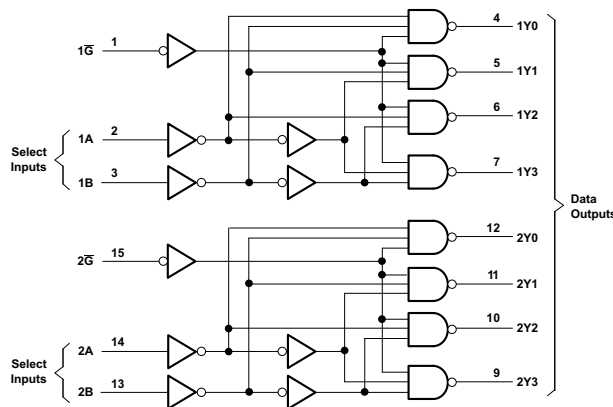
### 2 Description

The SN74AHC139 are dual 2-line to 4-line decoders/demultiplexers designed for 2V to 5.5V  $V_{CC}$  operation. These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

#### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> | BODY SIZE <sup>(3)</sup> |
|-------------|------------------------|-----------------------------|--------------------------|
| SN74AHC139  | D (SOIC, 16)           | 9.90 mm × 6mm               | 9.90 mm × 3.90 mm        |
|             | DB (SSOP, 16)          | 6.20 mm × 7.8mm             | 6.20 mm × 5.30 mm        |
|             | N (PDIP, 16)           | 19.31 mm × 9.4mm            | 19.31 mm × 6.35 mm       |
|             | NS (SOP, 16)           | 5mm × 6.4mm                 | 5mm × 4.4mm              |
|             | PW (TSSOP, 16)         | 5.00 mm × 6.4mm             | 5.00 mm × 4.40 mm        |
|             | DGV (TVSOP, 16)        | 3.6mm × 6.4mm               | 3.6mm × 4.4mm            |
|             | RGY (VQFN, 16)         | 4mm × 3.5mm                 | 4mm × 3.5mm              |

- (1) For more information, see [Section 10](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable
- (3) The body size (length × width) is a nominal value and does not include pins.



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

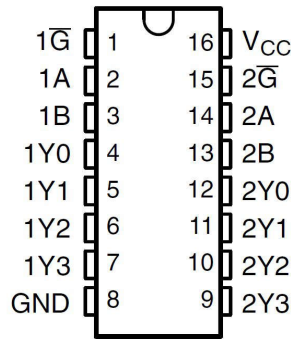
#### Logic Diagram, Each Gate (Positive Logic)



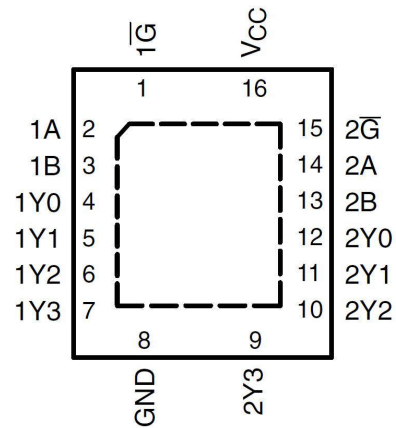
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### 3 Pin Configuration and Functions



**Figure 3-1. SN74AHC139 D, DB, DGV, N, NS, or PW Package (Top View)**



**Figure 3-2. SN74AHC139 RGY Package (Top View)**

**Table 3-1. Pin Functions**

| PIN |                   | I/O | DESCRIPTION                          |
|-----|-------------------|-----|--------------------------------------|
| NO. | NAME              |     |                                      |
| 1   | $\overline{1G}$   | I   | Channel 1, output enable, active low |
| 2   | 1A <sub>0</sub>   | I   | Channel 1, address select 0          |
| 3   | 1A <sub>1</sub>   | I   | Channel 1, address select 1          |
| 4   | 1Y <sub>0</sub>   | O   | Channel 1, output 0                  |
| 5   | 1Y <sub>1</sub>   | O   | Channel 1, output 1                  |
| 6   | 1Y <sub>2</sub>   | O   | Channel 1, output 2                  |
| 7   | 1Y <sub>3</sub>   | O   | Channel 1, output 3                  |
| 8   | GND               | —   | Ground                               |
| 9   | 2Y <sub>3</sub>   | O   | Channel 2, output 3                  |
| 10  | 2Y <sub>2</sub>   | O   | Channel 2, output 2                  |
| 11  | 2Y <sub>1</sub>   | O   | Channel 2, output 1                  |
| 12  | 2Y <sub>0</sub>   | O   | Channel 2, output 0                  |
| 13  | 2A <sub>1</sub>   | I   | Channel 2, address select 1          |
| 14  | 2A <sub>0</sub>   | I   | Channel 2, address select 0          |
| 15  | $\overline{2G}_0$ | I   | Channel 2, output enable, active low |
| 16  | V <sub>CC</sub>   | —   | Positive supply                      |

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                      |  | MIN  | MAX            | UNIT                            |
|----------------------|--|------|----------------|---------------------------------|
| $V_{CC}$             | Supply voltage                             | -0.5 | 7              | V                               |
| $V_I$ <sup>(2)</sup> | Input voltage                              | -0.5 | 7              | V                               |
| $V_O$ <sup>(2)</sup> | Output voltage                             | -0.5 | $V_{CC} + 0.5$ | V                               |
| $I_{IK}$             | Input clamp current                        |      | -20            | mA                              |
|                      |  |      |                | ( $V_I < 0$ )                   |
| $I_{OK}$             | Output clamp current                       |      | ±20            | mA                              |
|                      |  |      |                | ( $V_O < 0$ or $V_O > V_{CC}$ ) |
| $I_O$                | Continuous output current                  |      | ±25            | mA                              |
|                      |  |      |                | ( $V_O = 0$ to $V_{CC}$ )       |
|                      | Continuous current through $V_{CC}$ or GND |      | ±75            | mA                              |
| $T_{stg}$            | Storage temperature                        | -65  | 150            | °C                              |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 ESD Ratings

|             |                         | VALUE   | UNIT  |
|-------------|-------------------------|---|-------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001              | ±2000 |
|             |                         | Charged device model (CDM), per JEDEC specification JESD22-C101 | ±1000 |
|             |                         |   | V     |

### 4.3 Recommended Operating Conditions

|                     |                                    | SN54AHC139                               |          | SN74AHC139 |          | UNIT |
|---------------------|------------------------------------|--|----------|------------|----------|------|
|                     |                                    | MIN                                      | MAX      | MIN        | MAX      |      |
| $V_{CC}$            | Supply voltage                     | 2  | 5.5      | 2          | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 2\text{ V}$                    | 1.5      | 1.5        |          | V    |
|                     |                                    | $V_{CC} = 3\text{ V}$                    | 2.1      | 2.1        |          |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$                  | 3.85     | 3.85       |          |      |
| $V_{IL}$            | Low-level Input voltage            | $V_{CC} = 2\text{ V}$                    |          | 0.5        | 0.5      | V    |
|                     |                                    | $V_{CC} = 3\text{ V}$                    |          | 0.9        | 0.9      |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$                  |          | 1.65       | 1.65     |      |
| $V_I$               | Input voltage                      | 0  | 5.5      | 0          | 5.5      | V    |
| $V_O$               | Output voltage                     | 0  | $V_{CC}$ | 0          | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          | $V_{CC} = 2\text{ V}$                    |          | -50        | -50      | mA   |
|                     |                                    | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |          | -4         | -4       |      |
|                     |                                    | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$   |          | -8         | -8       |      |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 2\text{ V}$                    |          | 50         | 50       | mA   |
|                     |                                    | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |          | 4          | 4        |      |
|                     |                                    | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$   |          | 8          | 8        |      |
| $\Delta t/\Delta v$ | Input Transition rise or fall rate | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 100      | 100        |          | ns/V |
|                     |                                    | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$   | 20       | 20         |          |      |
| $T_A$               | Operating free-air temperature     | -55                                      | 125      | -40        | 125      | °C   |

### 4.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | SN74AHC139 |           |             |          |         |            |            | UNIT |
|-------------------------------|--|------------|-----------|-------------|----------|---------|------------|------------|------|
|                               |  | D (SOIC)   | DB (SSOP) | DGV (TVSOP) | N (PDIP) | NS (SO) | PW (TSSOP) | RGY (VQFN) |      |
|                               |  | 16         |           |             |          |         |            |            |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 73         | 82        | 120         | 67       | 64      | 135.9      | 52.9       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

### 4.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS   | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     | T <sub>A</sub> = –40°C TO 85°C |     | T <sub>A</sub> = –40°C TO 125°C |     | UNIT |
|-----------------|---|-----------------|-----------------------|-----|--------------------------------|-----|---------------------------------|-----|------|
|                 |   |                 |                       |     | SN74AHC139                     |     | Recommended                     |     |      |
|                 |   |                 | MIN                   | TYP | MAX                            | MIN | MAX                             | MIN |      |
| V <sub>OH</sub> | I <sub>OH</sub> = –50 μA                                    | 2 V             | 1.9                   | 2   | 1.9                            | 1.9 | 1.9                             | V   |      |
|                 |   | 3 V             | 2.9                   | 3   | 2.9                            | 2.9 | 2.9                             |     |      |
|                 |   | 4.5 V           | 4.4                   | 4.5 | 4.4                            | 4.4 | 4.4                             |     |      |
|                 | I <sub>OH</sub> = –4 mA                                     | 3 V             | 2.58                  |     | 2.48                           |     | 2.48                            |     |      |
|                 |   | 4.5 V           | 3.94                  |     | 3.8                            |     | 3.8                             |     |      |
| V <sub>OL</sub> | I <sub>OL</sub> = 50 μA                                     | 2 V             | 0.1                   |     | 0.1                            |     | 0.1                             |     | V    |
|                 |   | 3 V             | 0.1                   |     | 0.1                            |     | 0.1                             |     |      |
|                 |   | 4.5 V           | 0.1                   |     | 0.1                            |     | 0.1                             |     |      |
|                 | I <sub>OH</sub> = 4 mA                                      | 3 V             | 0.36                  |     | 0.44                           |     | 0.5                             |     |      |
|                 |   | 4.5 V           | 0.36                  |     | 0.44                           |     | 0.5                             |     |      |
| I <sub>I</sub>  | V <sub>I</sub> = 5.5 V or GND                               | 0 V to 5.5 V    | ±0.1                  |     | ±1                             |     | ±1                              |     | μA   |
| I <sub>CC</sub> | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           | 4                     |     | 40                             |     | 40                              |     | μA   |
| C <sub>i</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5 V             | 2 10                  |     | 10                             |     |                                 |     | pF   |

### 4.6 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see [Figure 5-1](#))

| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE       | T <sub>A</sub> = 25°C |                    | T <sub>A</sub> = –40°C TO 85°C |      | T <sub>A</sub> = –40°C TO 125°C |      | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|--------------------|--------------------------------|------|---------------------------------|------|------|
|                  |              |             |                        |                       |                    | SN74AHC139                     |      | Recommended                     |      |      |
|                  |              |             |                        | TYP                   | MAX                | MIN                            | MAX  | MIN                             | MAX  |      |
| t <sub>PLH</sub> | A or B       | Y           | C <sub>L</sub> = 15 pF | 7.2 <sup>(1)</sup>    | 11 <sup>(1)</sup>  | 1                              | 13   | 1                               | 13   | ns   |
| t <sub>PHL</sub> |              |             |                        | 7.2 <sup>(1)</sup>    | 11 <sup>(1)</sup>  | 1                              | 13   | 1                               | 13   |      |
| t <sub>PLH</sub> | G̅           | Y           | C <sub>L</sub> = 15 pF | 6.4 <sup>(1)</sup>    | 9.2 <sup>(1)</sup> | 1                              | 11   | 1                               | 11   | ns   |
| t <sub>PHL</sub> |              |             |                        | 6.4 <sup>(1)</sup>    | 9.2 <sup>(1)</sup> | 1                              | 11   | 1                               | 11   |      |
| t <sub>PLH</sub> | A or B       | Y           | C <sub>L</sub> = 50 pF | 9.7                   | 14.5               | 1                              | 16.5 | 1                               | 16.5 | ns   |
| t <sub>PHL</sub> |              |             |                        | 9.7                   | 14.5               | 1                              | 16.5 | 1                               | 16.5 |      |
| t <sub>PLH</sub> | G̅           | Y           | C <sub>L</sub> = 50 pF | 8.9                   | 12.7               | 1                              | 14.5 | 1                               | 14.5 | ns   |
| t <sub>PHL</sub> |              |             |                        | 8.9                   | 12.7               | 1                              | 14.5 | 1                               | 14.5 |      |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

#### 4.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Figure 5-1](#))

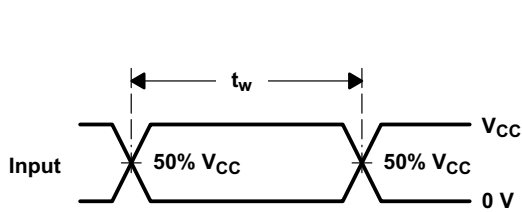
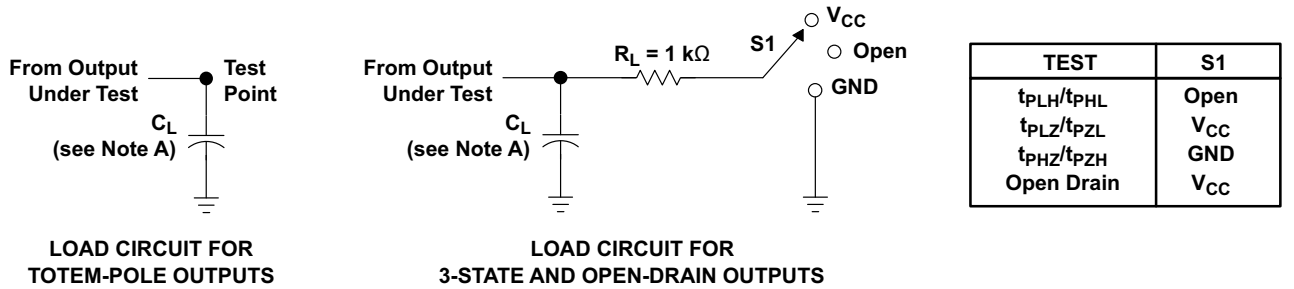
| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |                    | $T_A = -40^\circ\text{C TO } 85^\circ\text{C}$ |      | $T_A = -40^\circ\text{C TO } 125^\circ\text{C}$ |      | UNIT |
|-----------|-----------------|----------------|----------------------|--------------------------|--------------------|--|------|---|------|------|
|           |                 |                |                      | TYP                      | MAX                | Recommended                                    |      | Recommended                                     |      |      |
|           |                 |                |                      |                          |                    | SN74AHC139                                     |      | SN74AHC139                                      |      |      |
|           |                 |                |                      |                          |                    | MIN  | MAX  | MIN   | MAX  |      |
| $t_{PLH}$ | A or B          | Y              | $C_L = 15\text{ pF}$ | 5 <sup>(1)</sup>         | 7.2 <sup>(1)</sup> | 1  | 8.5  | 1   | 8.5  | ns   |
| $t_{PHL}$ |                 |                |                      | 5 <sup>(1)</sup>         | 7.2 <sup>(1)</sup> | 1  | 8.5  | 1   | 8.5  |      |
| $t_{PLH}$ | $\bar{G}$       | Y              | $C_L = 15\text{ pF}$ | 4.4 <sup>(1)</sup>       | 6.3 <sup>(1)</sup> | 1  | 7.5  | 1   | 7.5  | ns   |
| $t_{PHL}$ |                 |                |                      | 4.4 <sup>(1)</sup>       | 6.3 <sup>(1)</sup> | 1  | 7.5  | 1   | 7.5  |      |
| $t_{PLH}$ | A or B          | Y              | $C_L = 50\text{ pF}$ | 6.5                      | 9.5                | 1  | 10.5 | 1   | 10.5 | ns   |
| $t_{PHL}$ |                 |                |                      | 6.5                      | 9.5                | 1  | 10.5 | 1   | 10.5 |      |
| $t_{PLH}$ | $\bar{G}$       | Y              | $C_L = 50\text{ pF}$ | 5.9                      | 8.3                | 1  | 9.5  | 1   | 9.5  | ns   |
| $t_{PHL}$ |                 |                |                      | 5.9                      | 8.3                | 1  | 9.5  | 1   | 9.5  |      |

#### 4.8 Operating Characteristics

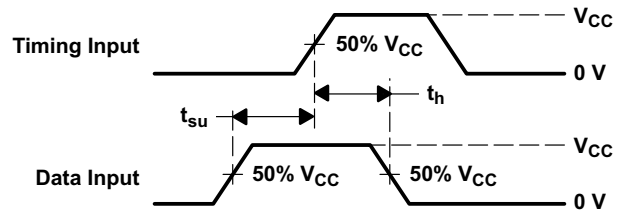
$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |                               | TEST CONDITIONS             | TYP | UNIT |
|-----------|-------------------------------|-----------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 13  | pF   |

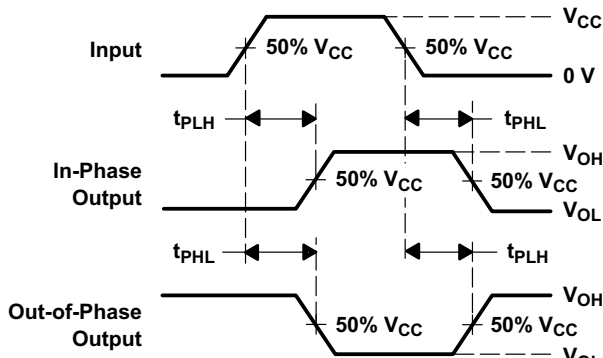
## 5 Parameter Measurement Information



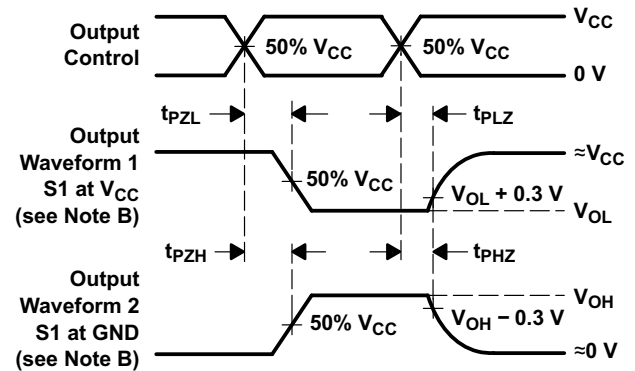
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- C<sub>L</sub> includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 3 ns, t<sub>f</sub> ≤ 3 ns.
- The outputs are measured one at a time with one input transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms

## 6 Detailed Description

### 6.1 Overview

The SN74AHC139 is a high speed silicon gate CMOS decoder well suited to memory address decoding or data routing applications. It contains two 2:4 decoders.

Each channel of the SN74AHC139 has two address select inputs (A1 and A0). The circuit functions as a normal one-of-four decoder.

One strobe input ( $\overline{G}$ ) is provided for each channel to simplify cascading and to facilitate demultiplexing. When the input strobe for a channel is active, that channel's outputs are forced into the high state.

The demultiplexing function is accomplished by first using the select inputs to choose the desired output, and then using the strobe input as the data input.

The outputs for the SN74AHC139 are normally high, and low when selected.

### 6.2 Functional Block Diagram

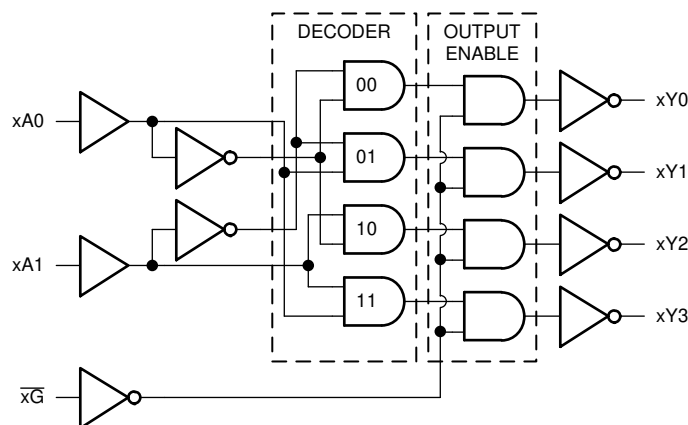


Figure 6-1. Logic Diagram, Each Gate (Positive Logic)

### 6.3 Feature Description

#### 6.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10k $\Omega$  resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.



### 6.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in [Implications of Slow or Floating CMOS Inputs](#).

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10k $\Omega$  resistor, however, is recommended and will typically meet all requirements.

### 6.4 Device Functional Modes

**Function Table (each channel)**

| INPUTS <sup>1</sup> |        |    | OUTPUT <sup>2</sup> |    |    |    |
|---------------------|--------|----|---------------------|----|----|----|
| $\bar{G}$           | SELECT |    | Y0                  | Y1 | Y2 | Y3 |
|                     | A1     | A0 |                     |    |    |    |
| H                   | X      | X  | H                   | H  | H  | H  |
| L                   | L      | L  | L                   | H  | H  | H  |
| L                   | L      | H  | H                   | L  | H  | H  |
| L                   | H      | L  | H                   | H  | L  | H  |
| L                   | H      | H  | H                   | H  | H  | L  |

1. L = Low; H = High; X = Don't care
2. L = Driving low; H = Driving high

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

The SN74AHC139 device is used to control multiple devices that operate on a shared data bus. A decoder allows a binary encoded input to activate only one of the device's outputs. This makes this device an excellent choice for solid state memory applications where multiple devices have to be read or written to with a limited number of GPIO pins used on the system controller. The decoder is used to activate the chip select (CS) input to the selected memory device, and the controller can then read or write from that device alone when using a shared bus.

### 7.2 Typical Application

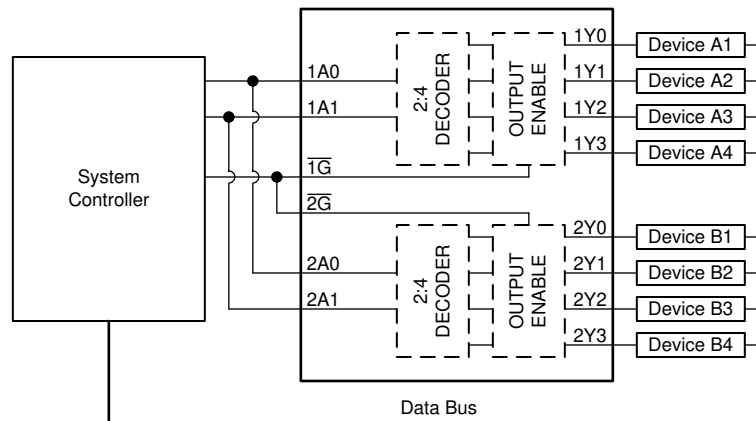


Figure 7-1. Typical Application Block Diagram

## 7.2.1 Design Requirements

### 7.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AHC139 plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AHC139 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AHC139 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AHC139 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 7.2.1.2 Input Considerations

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AHC139 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k $\Omega$  resistor value is often used due to these factors.

The SN74AHC139 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 7.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 7.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50\text{pF}$ . This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHC139 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(\text{max})})\Omega$ . Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in  $M\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

### 7.2.3 Application Curve

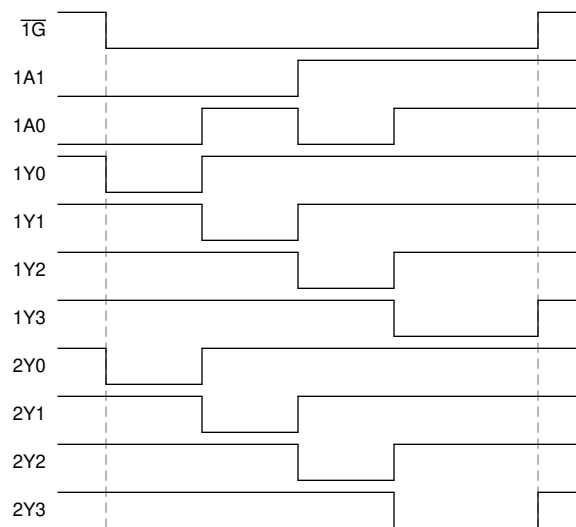


Figure 7-2. Application Timing Diagram

## 7.3 Power Supply Recommendations

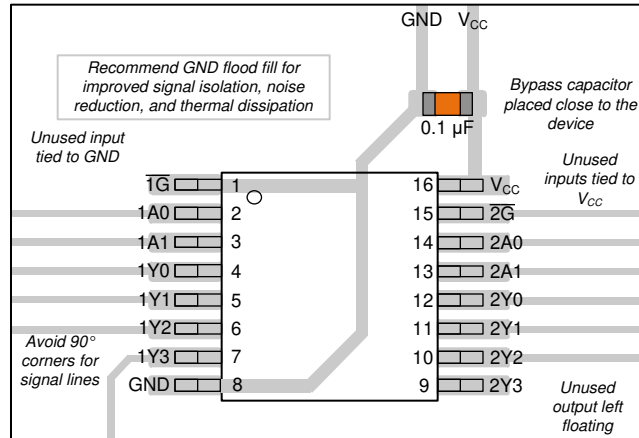
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A  $0.1\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The  $0.1\mu\text{F}$  and  $1\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 7.4 Layout

### 7.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

**7.4.2 Layout Example**



**Figure 7-3. Example Layout for the SN74AHC139**

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Understanding Schmitt Triggers](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)
- Texas Instruments, [CMOS Power Consumption and Cpd Calculation](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#)

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision M (July 2024) to Revision N (January 2025)</b> | <b>Page</b> |
|---|-------------|
| • Updated descriptions in <i>Pin Functions</i> table.....               | 3           |

| <b>Changes from Revision L (June 2013) to Revision M (July 2024)</b>  | <b>Page</b> |
|---|-------------|
| • Deleted machine model from <i>Features</i> section.....   | 1           |
| • Added <i>Package Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , Application and Implementation section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | 1           |
| • Updated thermal values for RθJA: PW = 108 to 135.9, RGY = 39 to 52.9, all values in °C/W .....  | 5           |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN74AHC139D      | OBSOLETE      | SOIC         | D               | 16   |             | TBD             | Call TI                              | Call TI              | -40 to 125   | AHC139                  |         |
| SN74AHC139DBR    | ACTIVE        | SSOP         | DB              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | HA139                   | Samples |
| SN74AHC139DGVR   | ACTIVE        | TVSOP        | DGV             | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | HA139                   | Samples |
| SN74AHC139DR     | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | AHC139                  | Samples |
| SN74AHC139N      | ACTIVE        | PDIP         | N               | 16   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | -40 to 125   | SN74AHC139N             | Samples |
| SN74AHC139NSR    | ACTIVE        | SOP          | NS              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | AHC139                  | Samples |
| SN74AHC139PW     | OBSOLETE      | TSSOP        | PW              | 16   |             | TBD             | Call TI                              | Call TI              | -40 to 125   | HA139                   |         |
| SN74AHC139PWR    | ACTIVE        | TSSOP        | PW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | HA139                   | Samples |
| SN74AHC139RGYR   | ACTIVE        | VQFN         | RGY             | 16   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | HA139                   | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AHC139 :**

- Automotive : [SN74AHC139-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC139DBR  | SSOP         | DB              | 16   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74AHC139DGVR | TVSOP        | DGV             | 16   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74AHC139DR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74AHC139NSR  | SOP          | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74AHC139PWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74AHC139PWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74AHC139RGYR | VQFN         | RGY             | 16   | 3000 | 330.0              | 12.4               | 3.8     | 4.3     | 1.5     | 8.0     | 12.0   | Q1            |
| SN74AHC139RGYR | VQFN         | RGY             | 16   | 3000 | 330.0              | 12.4               | 3.8     | 4.3     | 1.5     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC139DBR  | SSOP         | DB              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AHC139DGVR | TVSOP        | DGV             | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AHC139DR   | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74AHC139NSR  | SOP          | NS              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AHC139PWR  | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AHC139PWR  | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74AHC139RGYR | VQFN         | RGY             | 16   | 3000 | 360.0       | 360.0      | 36.0        |
| SN74AHC139RGYR | VQFN         | RGY             | 16   | 3000 | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74AHC139N | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74AHC139N | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

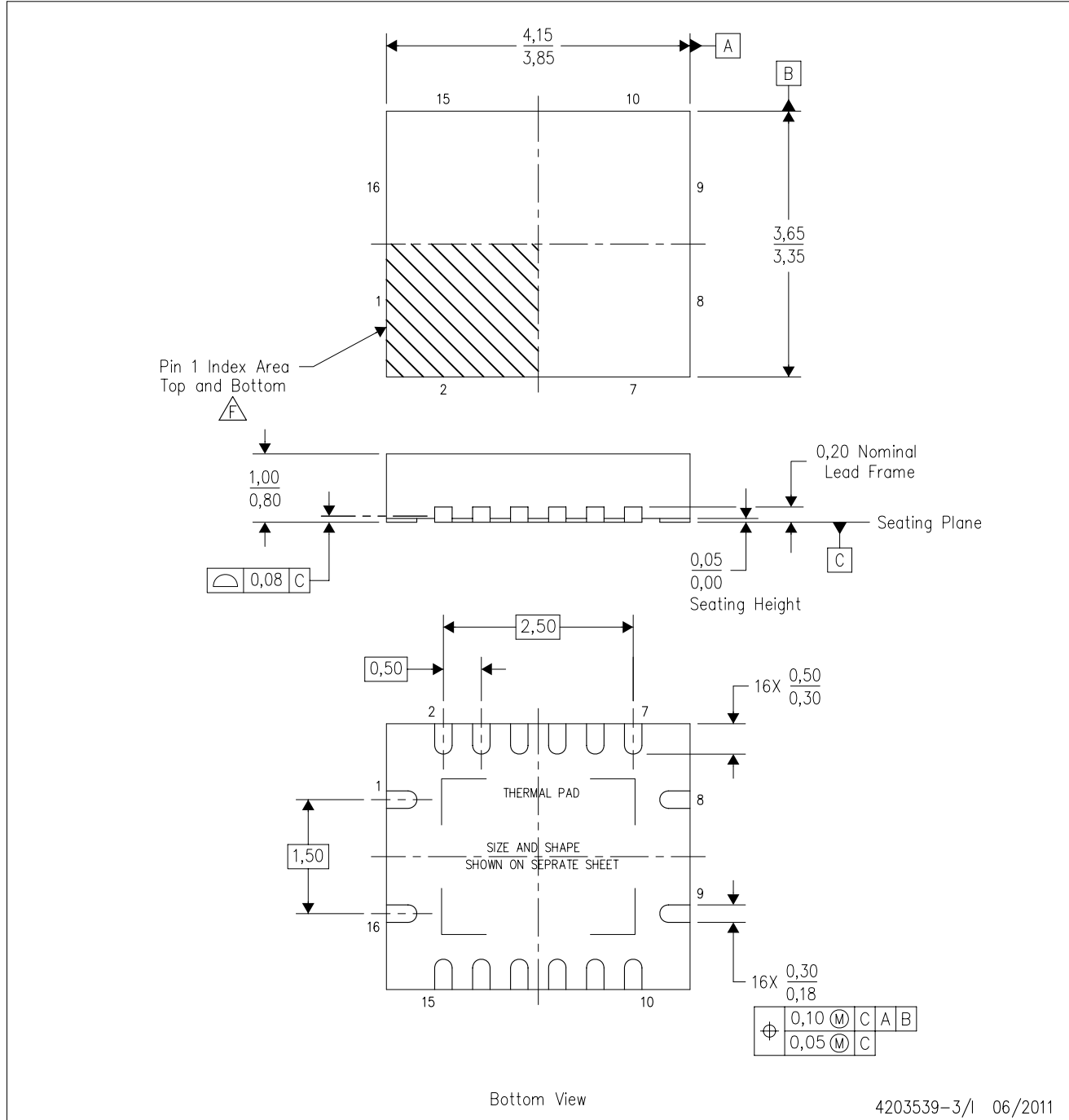
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

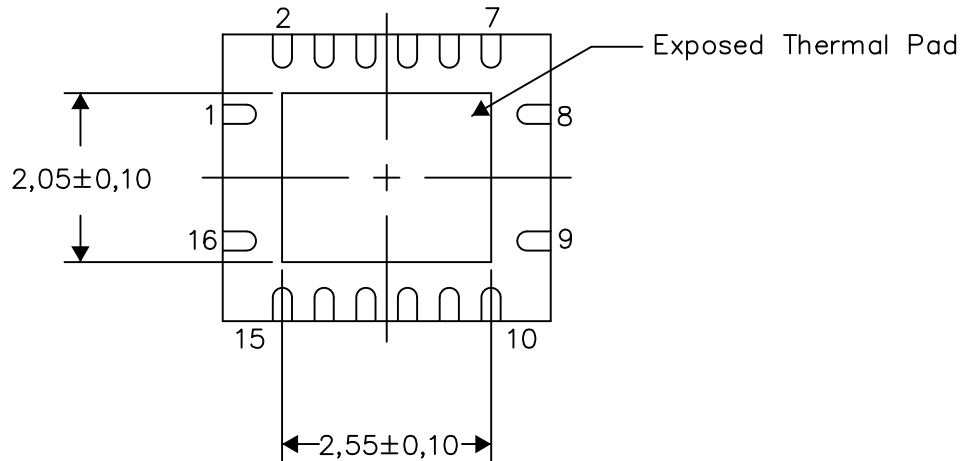
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

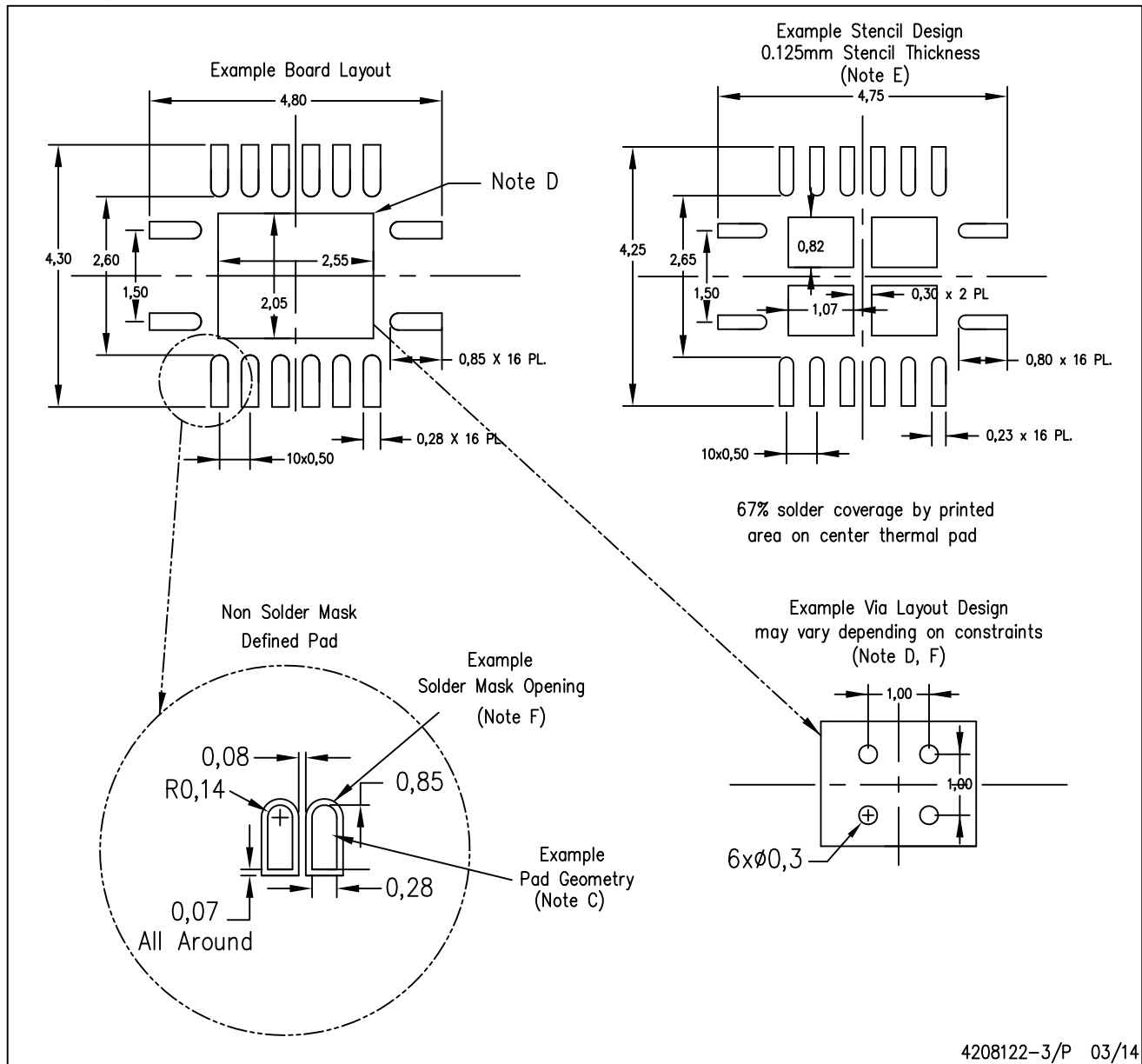
Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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