

# SN74AHC4066 Quadruple Bilateral Analog Switch

## 1 Features

- 1V to 5.5V  $V_{CC}$  operation
- Supports mixed-mode voltage operation on all ports
- High on-off output-voltage ratio
- Low crosstalk between switches
- Individual switch controls
- Extremely low input current
- ESD protection exceeds JESD 22:
  - 2000V Human-Body Model (A114-A)
  - 200V Machine Model (A115-A)
  - 1000V Charged-Device Model (C101)

## 2 Applications

- Analog signal switching or multiplexing:
  - Signal gating, modulator, squelch control, demodulator, chopper, commutating switch
- Digital signal switching and multiplexing
  - [Audio and video signal routing](#)
- Transmission-gate logic implementation
- Analog-to-digital and digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain
- Motor speed control
- [Battery chargers](#)
- [DC-DC converter](#)

## 3 Description

This quadruple silicon-gate CMOS analog switch is designed for 1V to 5.5V  $V_{CC}$  operation.

The switch is designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 5.5V (peak) to be transmitted in either direction.

Each switch section has its own enable input control (C). A high-level voltage applied to C turns on the associated switch section.

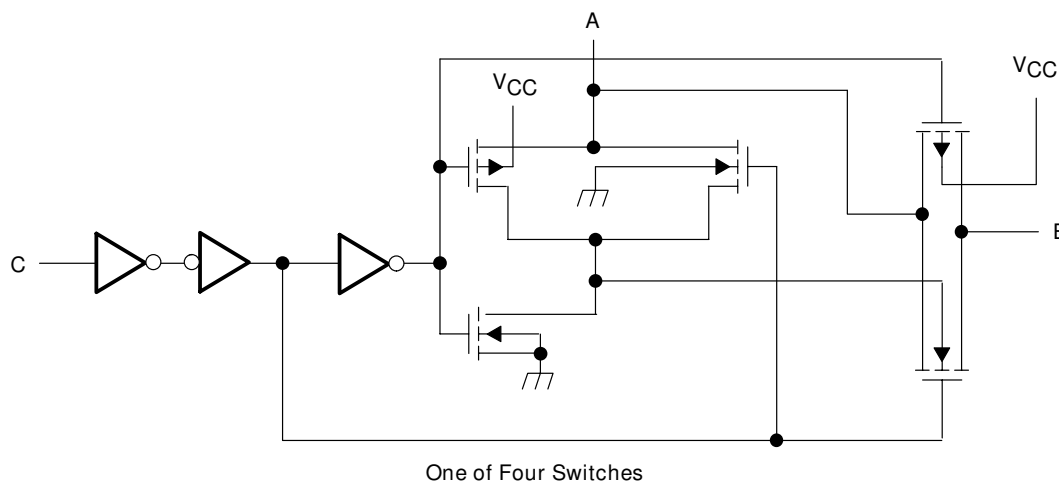
Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
SN74AHC4066	D (SOIC, 14)	8.65mm × 6mm
	PW (TSSOP, 14)	5mm × 6.4mm
	RGY (VQFN, 14)	3.5mm × 3.5mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



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### Logic Diagram, Each Switch (Positive Logic)



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## 4 Pin Configuration and Functions

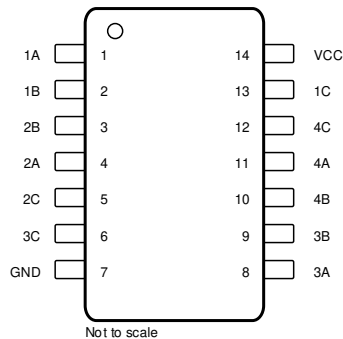


Figure 4-1. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

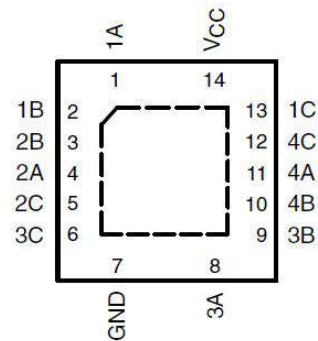


Figure 4-2. RGY Package, 14-Pin QFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1A	1	I/O	Switch 1 input/output
1B	2	I/O	Switch 1 output/input
2B	3	I/O	Switch 2 output/input
2A	4	I/O	Switch 2 input/output
2C	5	I	Switch 2 control
3C	6	I	Switch 3 control
GND	7	—	Ground
3A	8	I/O	Switch 3 input/output
3B	9	I/O	Switch 3 output/input
4B	10	I/O	Switch 4 output/input
4A	11	I/O	Switch 4 input/output
4C	12	I	Switch 4 control
1C	13	I	Switch 1 control
V <sub>CC</sub>	14	—	Power

(1) I = input, O = output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>	-0.5	7	V
V <sub>I</sub>	Input voltage range	-0.5	7	V
V <sub>IO</sub>	Switch I/O voltage range	-0.5 to V <sub>CC</sub>	+0.5	V
I <sub>IK</sub>	Control-input clamp current	V <sub>I</sub> < 0	-20	mA
I <sub>I</sub>	I/O port diode current	V <sub>I</sub> < 0 or V <sub>IO</sub> > V <sub>CC</sub>	±50	mA
	On-state switch current	V <sub>IO</sub> = 0 to V <sub>CC</sub>	±25	mA
	Continuous current through V <sub>CC</sub> or GND		±50	mA
T <sub>stg</sub>	Storage temperature	-60	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	±2000	V
		±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. CDM value for N package only.

### 5.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHC4066			UNIT
		D	PW	RGY	
		14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	127.7	150.6	91.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	81.8	78.2	91.8	°C/W
R <sub>θJC(bottom)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	50.0	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	84.2	93.7	66.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	39.5	24.6	20.0	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	83.7	93.1	66.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(2)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1 (1)	5.5	V
V <sub>IH</sub>	High-level input voltage, control inputs	V <sub>CC</sub> = 2V	1.5	V
		V <sub>CC</sub> = 2.3V to 2.7V	V <sub>CC</sub> × 0.7	
		V <sub>CC</sub> = 3V to 3.6V	V <sub>CC</sub> × 0.7	
		V <sub>CC</sub> = 4.5V to 5.5V	V <sub>CC</sub> × 0.7	
V <sub>IL</sub>	Low-level input voltage, control inputs	V <sub>CC</sub> = 2V	0.5	V
		V <sub>CC</sub> = 2.3V to 2.7V	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3V to 3.6V	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5V to 5.5V	V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Control input voltage	0	5.5	V
V <sub>I/O</sub>	Input/output voltage	0	V <sub>CC</sub>	V
Δt/Δv	Input transition rise and fall time	V <sub>CC</sub> = 2.3V to 2.7V	200	ns/V
		V <sub>CC</sub> = 3V to 3.6V	100	
		V <sub>CC</sub> = 4.5V to 5.5V	20	
T <sub>A</sub>	Operating free-air temperature	−40	85	°C

(1) With supply voltages at or below 2V, the analog switch on-state resistance becomes very nonlinear. Only digital signals should be transmitted at these low supply voltages.

(2) All unused inputs of the device must be held at V<sub>CC</sub> or GND for proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

## 5.5 Electrical Characteristics

T<sub>A</sub> = −40 to +85 °C unless otherwise specified.

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
r <sub>on</sub>	On-state switch resistance I <sub>T</sub> = −1mA, V <sub>I</sub> = 0 to V <sub>CC</sub> , V <sub>C</sub> = V <sub>IH</sub> (see <a href="#">Figure 6-1</a> )	2.3V		38	180		225	Ω
		3V		29	150		190	
		4.5V		21	75		100	
r <sub>on(p)</sub>	Peak on-state resistance I <sub>T</sub> = −1mA V <sub>I</sub> = V <sub>CC</sub> to GND V <sub>C</sub> = V <sub>IH</sub>	2.3V		143	500		600	Ω
		3V		57	180		225	
		4.5V		31	100		125	
Δr <sub>on</sub>	Difference in on-state resistance between switches I <sub>T</sub> = −1mA V <sub>I</sub> = V <sub>CC</sub> to GND V <sub>C</sub> = V <sub>IH</sub>	2.3V		6	30		40	Ω
		3V		3	20		30	
		4.5V		2	15		20	
I <sub>IH</sub> I <sub>IL</sub>	Control input current V <sub>C</sub> = 0 or V <sub>CC</sub>	5.5			±0.1		±1	μA
I <sub>s(off)</sub>	Off-state switch leakage current V <sub>I</sub> = V <sub>CC</sub> and V <sub>O</sub> = GND, or V <sub>I</sub> = GND and V <sub>O</sub> = V <sub>CC</sub> , V <sub>C</sub> = V <sub>IL</sub> (see <a href="#">Figure 6-2</a> )	5.5V			±0.1		±1	μA

## 5.5 Electrical Characteristics (continued)

$T_A = -40$  to  $+85$  °C unless otherwise specified.

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figure 6-3)	5.5V				$\pm 1$	$\mu\text{A}$
$I_{CC}$	Supply current	$V_I = V_{CC}$ or GND	5.5V				20	$\mu\text{A}$
$C_{iC}$	Control input capacitance			1.5				pF
$C_{iO}$	Switch input/output capacitance			5.5				pF
$C_F$	Feed-through capacitance			0.5				pF

## 5.6 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT	
				MIN	TYP	MAX				
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	A or B	B or A	$C_L = 50\text{pF}$ (see Figure 6-4)		1.2	10		16	ns
$t_{PZH}$ , $t_{PZL}$	Switch turn-on time	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$ , (see Figure 6-5)		3.3	15		20	ns
$t_{PLZ}$ , $t_{PHZ}$	Switch turn-off time	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$ , (see Figure 6-5)		6	15		23	ns
$t_{PLZ}$ , $t_{PHZ}$	Propagation delay time	A or B	B or A	$C_L = 50\text{pF}$ (see Figure 6-6)		2.6	12		18	ns
$t_{PLZ}$ , $t_{PHZ}$	Switch turn-on time	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$ , (see Figure 6-8)		4.2	25		32	ns
$t_{PLZ}$ , $t_{PHZ}$	Switch turn-off time	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$ , (see Figure 6-8)		9.6	25		32	ns

## 5.7 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT	
				MIN	TYP	MAX				
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	A or B	B or A	$C_L = 50\text{pF}$ (see Figure 6-4)		0.8	6		10	ns
$t_{PZH}$ , $t_{PZL}$	Switch turn-on time	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$ , (see Figure 6-5)		2.3	11		15	ns
$t_{PLZ}$ , $t_{PHZ}$	Switch turn-off time	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$ , (see Figure 6-5)		4.5	11		15	ns
$t_{PLZ}$ , $t_{PHZ}$	Propagation delay time	A or B	B or A	$C_L = 50\text{pF}$ (see Figure 6-6)		1.5	9		12	ns
$t_{PLZ}$ , $t_{PHZ}$	Switch turn-on time	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$ , (see Figure 6-8)		3	18		22	ns

## 5.7 Switching Characteristics (continued)

over recommended operating free-air temperature range,  $V_{CC} = 3.3V \pm 0.3V$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLZ}$ , $t_{PHZ}$ Switch turn-off time	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$ , (see Figure 6-8)		7.2	18		22	ns

## 5.8 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5V \pm 0.5V$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$ , $t_{PHL}$ Propagation delay time	A or B	B or A	$C_L = 50\text{pF}$ (see Figure 6-4)		0.3	4		7	ns
$t_{PZH}$ , $t_{PZL}$ Switch turn-on time	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$ , (see Figure 6-5)		1.6	7		10	ns
$t_{PLZ}$ , $t_{PHZ}$ Switch turn-off time	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$ , (see Figure 6-5)		3.2	7		10	ns
$t_{PLZ}$ , $t_{PHZ}$ Propagation delay time	A or B	B or A	$C_L = 50\text{pF}$ (see Figure 6-6)		0.6	6		8	ns
$t_{PLZ}$ , $t_{PHZ}$ Switch turn-on time	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$ , (see Figure 6-8)		2.1	12		16	ns
$t_{PLZ}$ , $t_{PHZ}$ Switch turn-off time	C	A or B	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$ , (see Figure 6-8)		5.1	12		16	ns

## 5.9 Analog Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			UNIT
					MIN	TYP	MAX	
Frequency response (switch on)	A or B	B or A	$C_L = 50\text{pF}$ , $R_L = 600\Omega$ $f_{in} = 1\text{MHz}$ (sine wave) $20\log_{10}(V_O/V_I) = -3\text{ dB}$ (see Figure 6-4)	2.3V		60	MHz	
				3V		75		
				4.5V		100		
Crosstalk (between any switches)	A or B	B or A	$C_L = 50\text{pF}$ , $R_L = 600\Omega$ $f_{in} = 1\text{MHz}$ (sine wave) (see Figure 6-4)	2.3V		-45	dB	
				3V		-45		
				4.5V		-45		
Crosstalk (control input to signal output)	C	A or B	$C_L = 50\text{pF}$ , $R_L = 600\Omega$ , $f_{in} =$ $1\text{MHz}$ (sine wave) (see Figure 6-4)	2.3V		15	mV	
				3V		20		
				4.5V		50		
Feed-through attenuation (switch off)	A or B	B or A	$C_L = 50\text{pF}$ , $R_L = 600\Omega$ , $f_{in} =$ $1\text{MHz}$ (sine wave) (see Figure 6-4)	2.3V		-40	dB	
				3V		-40		
				4.5V		-40		

### 5.9 Analog Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			UNIT
					MIN	TYP	MAX	
Sine-wave distortion	A or B	B or A	C <sub>L</sub> = 50pF, R <sub>L</sub> = 10kΩ, f <sub>in</sub> = 1kHz (sine wave) (see <a href="#">Figure 6-4</a> )	V <sub>I</sub> = 2V <sub>p-p</sub>	2.3V		0.1	%
				V <sub>I</sub> = 2.5V <sub>p-p</sub>	3V		0.1	
				V <sub>I</sub> = 4V <sub>p-p</sub>	4.5V		0.1	

### 5.10 Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	C <sub>L</sub> = 50pF, f = 10MHz	4.5	pF

## 6 Parameter Measurement Information

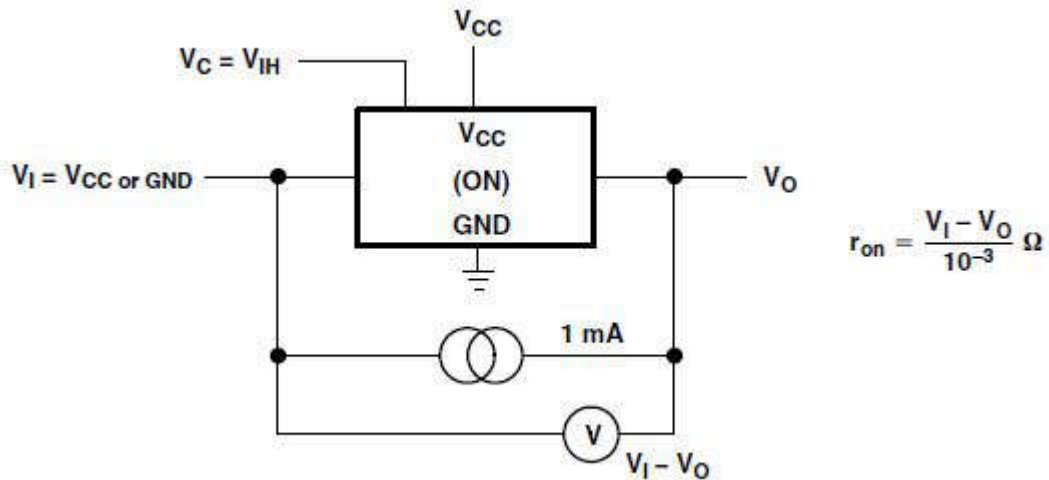


Figure 6-1. ON-State Resistance Test Circuit

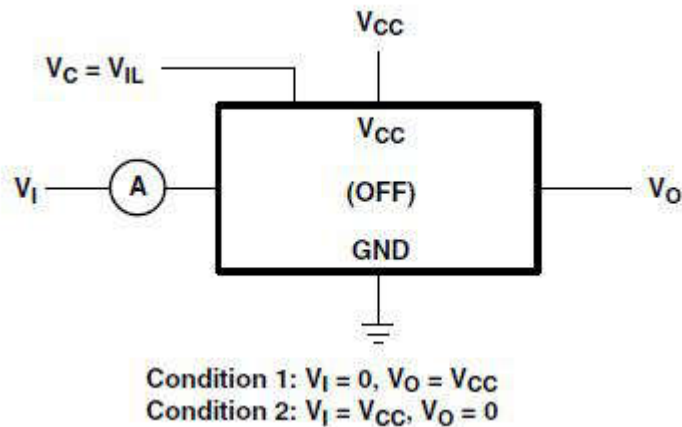


Figure 6-2. OFF-State Switch Leakage-Current Test Circuit

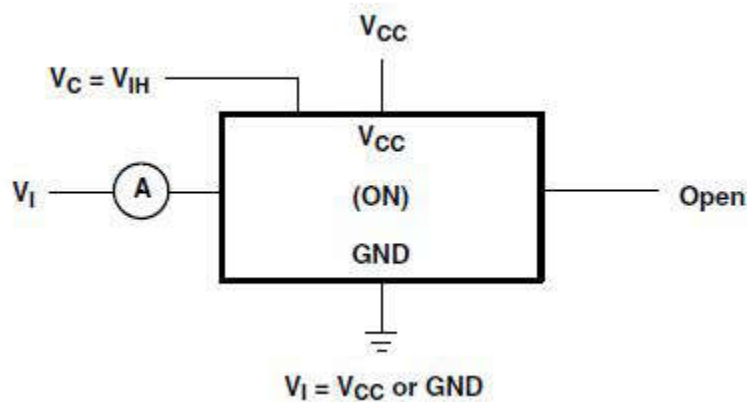


Figure 6-3. ON-State Leakage-Current Test Circuit



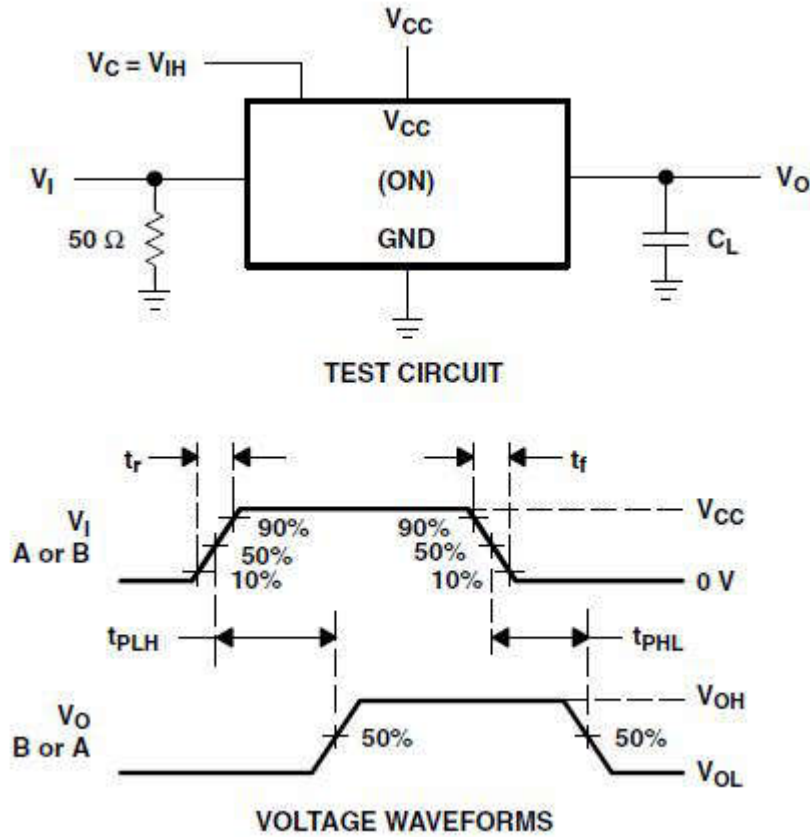
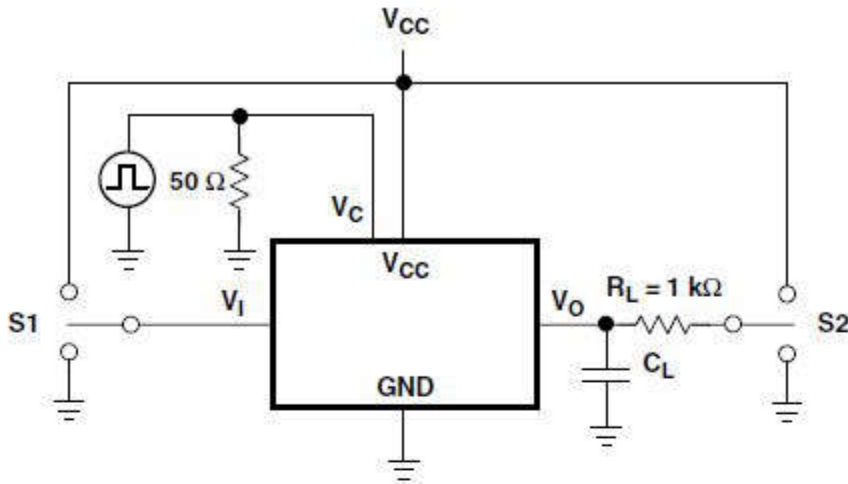
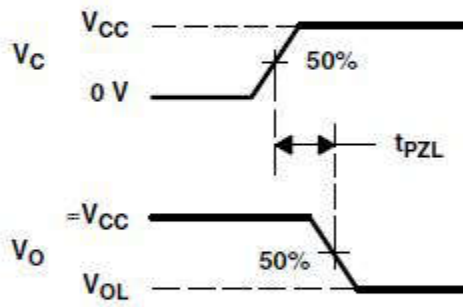


Figure 6-4. Propagation Delay Time, Signal Input to Signal Output

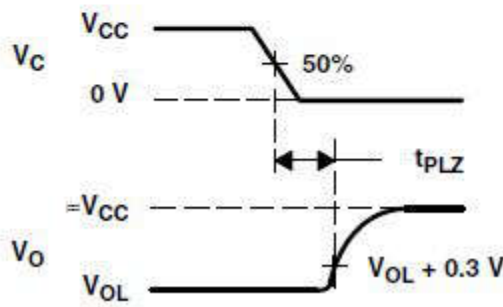
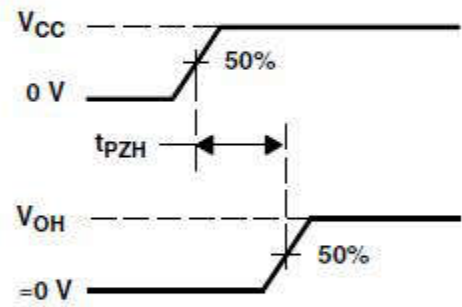


TEST CIRCUIT

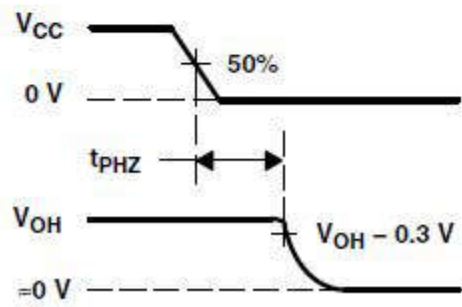
TEST	S1	S2
$t_{pZL}$	GND	$V_{CC}$
$t_{pZH}$	$V_{CC}$	GND
$t_{pLZ}$	GND	$V_{CC}$
$t_{pHZ}$	$V_{CC}$	GND



( $t_{pZL}$ ,  $t_{pZH}$ )



( $t_{pLZ}$ ,  $t_{pHZ}$ )



VOLTAGE WAVEFORMS

Figure 6-5. Switching Time ( $t_{pZL}$ ,  $t_{pLZ}$ ,  $t_{pZH}$ ,  $t_{pHZ}$ ), Control to Signal Output

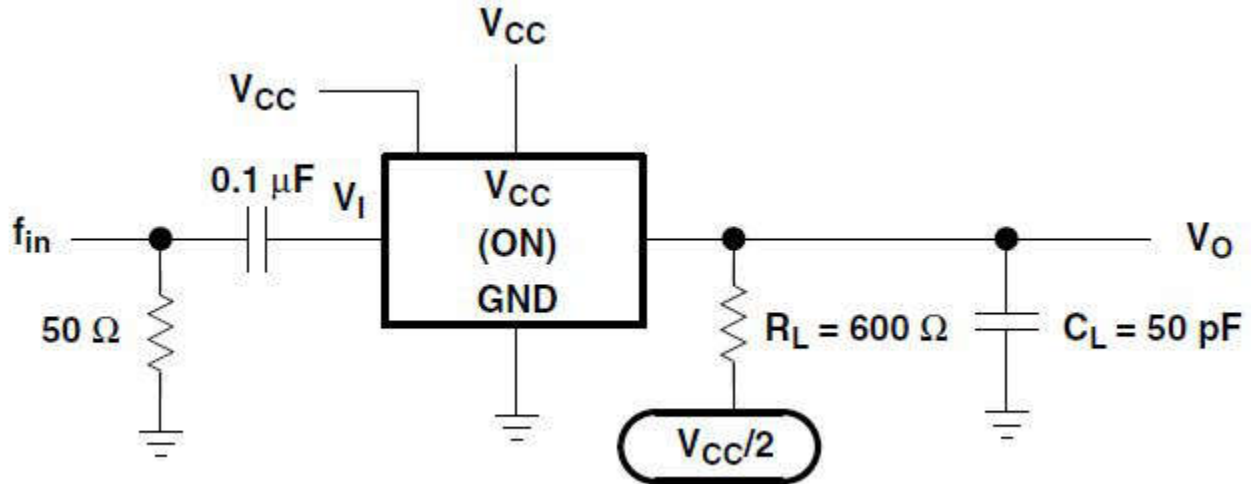


Figure 6-6. Frequency Response (Switch On)

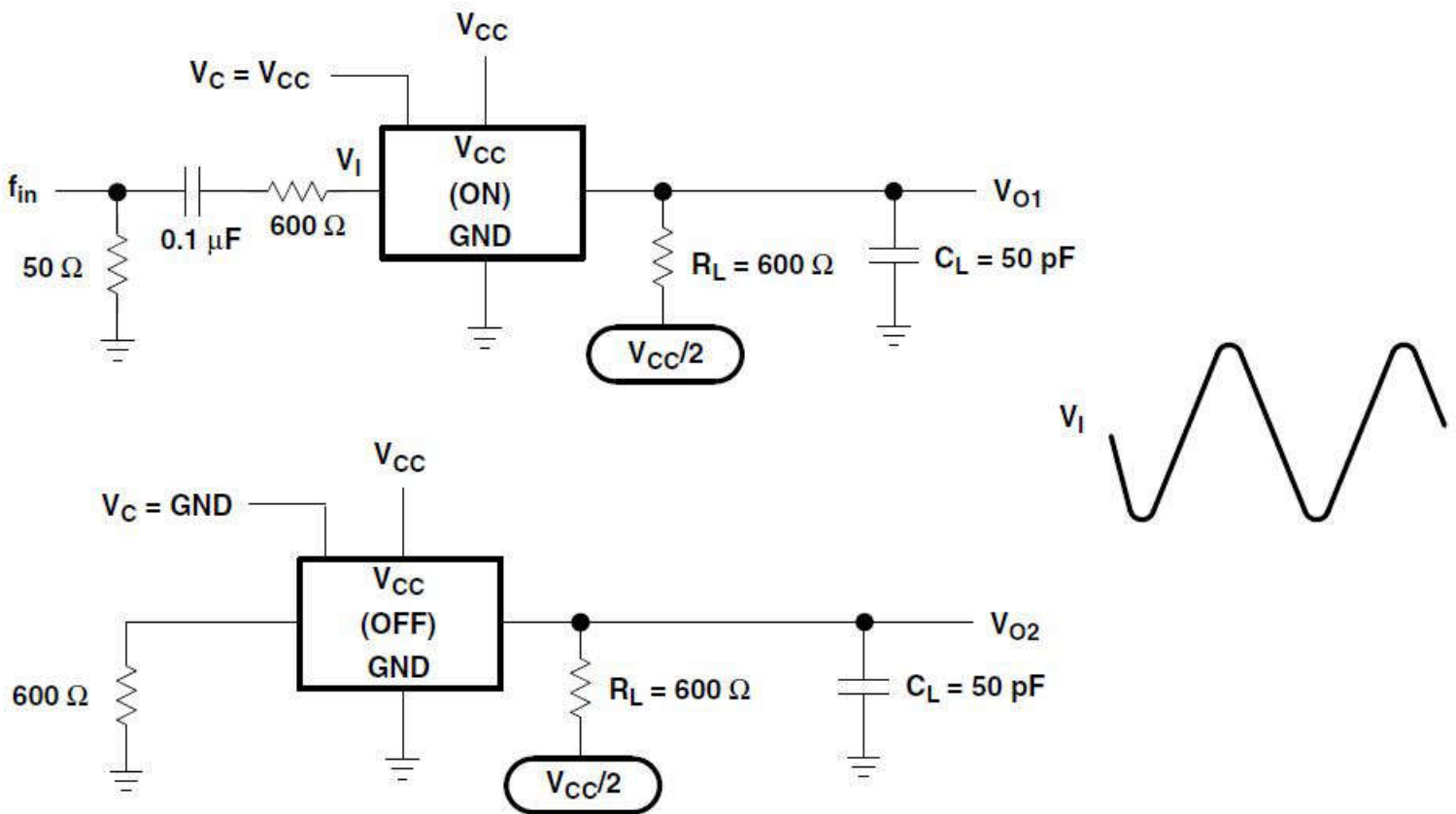


Figure 6-7. Crosstalk Between Any Two Switches

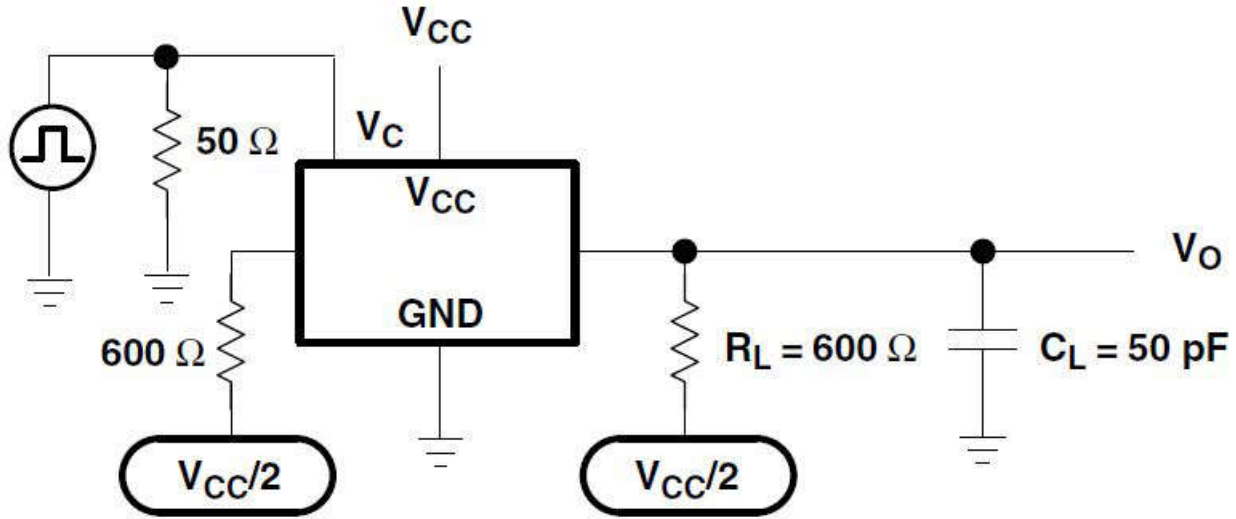


Figure 6-8. Crosstalk (Control Input - Switch Output)

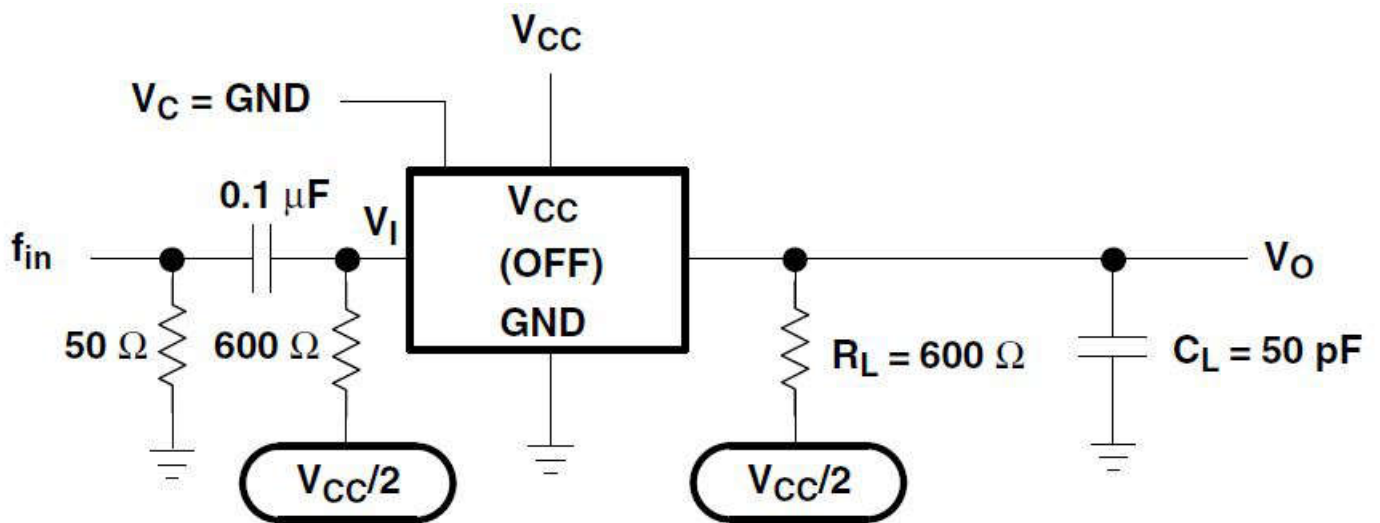


Figure 6-9. Feed-Through Attenuation (Switch Off)

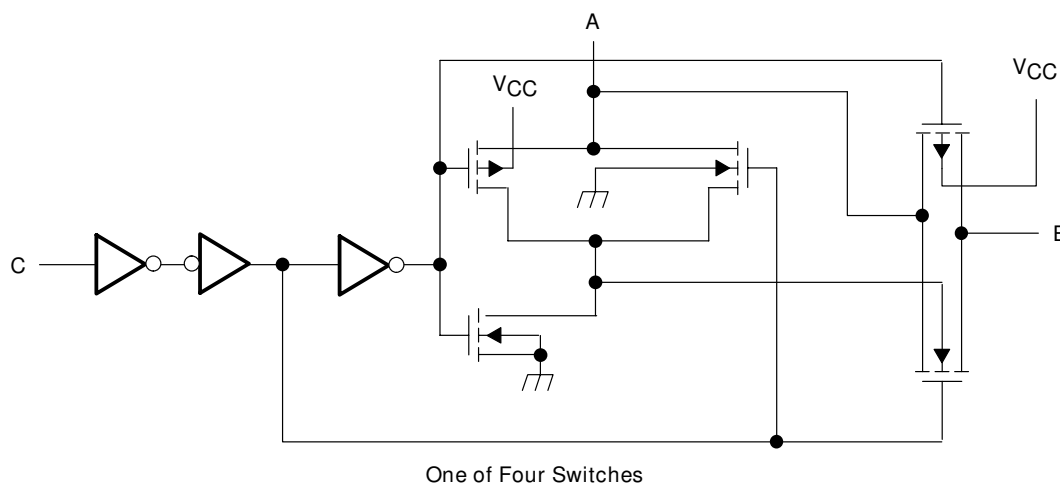


## 7 Detailed Description

### 7.1 Overview

The SN74AHC4066 device is a silicon-gate CMOS quadruple analog switch designed for 1V to 6V VCC operation. It is designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 6V (peak) to be transmitted in either direction. A high-level voltage applied to the control pin C enables the respective switch to begin propagating signals across the device.

### 7.2 Functional Block Diagram



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**Figure 7-1. Logic Diagram, Each Switch (Positive Logic)**

### 7.3 Device Functional Modes

Table 7-1 lists the functions for the SN74AHC4066 device.

**Table 7-1. Function Table  
(Each Switch)**

INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application notes](#)

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (June 2003) to Revision A (February 2024)</b>	<b>Page</b>
• Updated the data sheet to only include the <i>D</i> , <i>PW</i> , or <i>RGY</i> packages.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated the <i>Thermal Information</i> .....	3
• Updated V <sub>CC</sub> operation from: 2V - 5.5V to: 1V - 5.5V.....	4

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC4066D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	AHC4066	
SN74AHC4066DBR	NRND	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA4066	
SN74AHC4066DGVR	NRND	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA4066	
SN74AHC4066DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC4066	Samples
SN74AHC4066N	NRND	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC4066N	
SN74AHC4066NSR	NRND	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC4066	
SN74AHC4066PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	HA4066	
SN74AHC4066PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA4066	Samples
SN74AHC4066RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HA4066	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

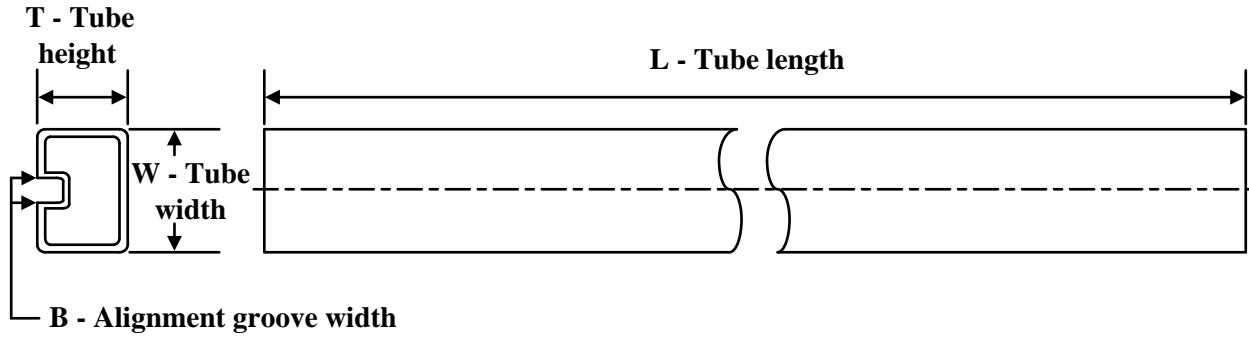

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC4066DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC4066DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC4066DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC4066DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC4066NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC4066PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC4066PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC4066RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC4066DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHC4066DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHC4066DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHC4066DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC4066NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AHC4066PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC4066PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC4066RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHC4066N	N	PDIP	14	25	506	13.97	11230	4.32

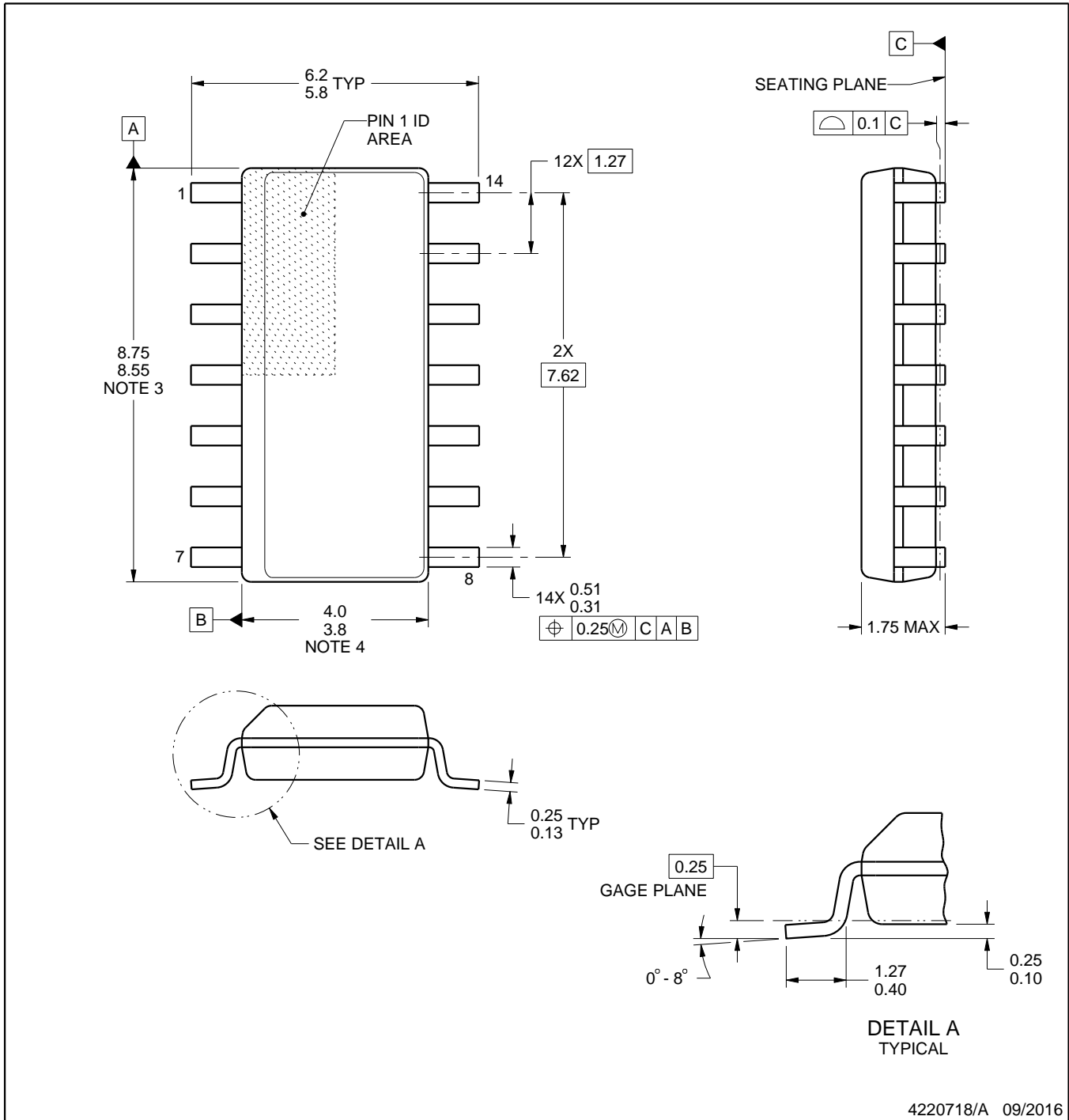
D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

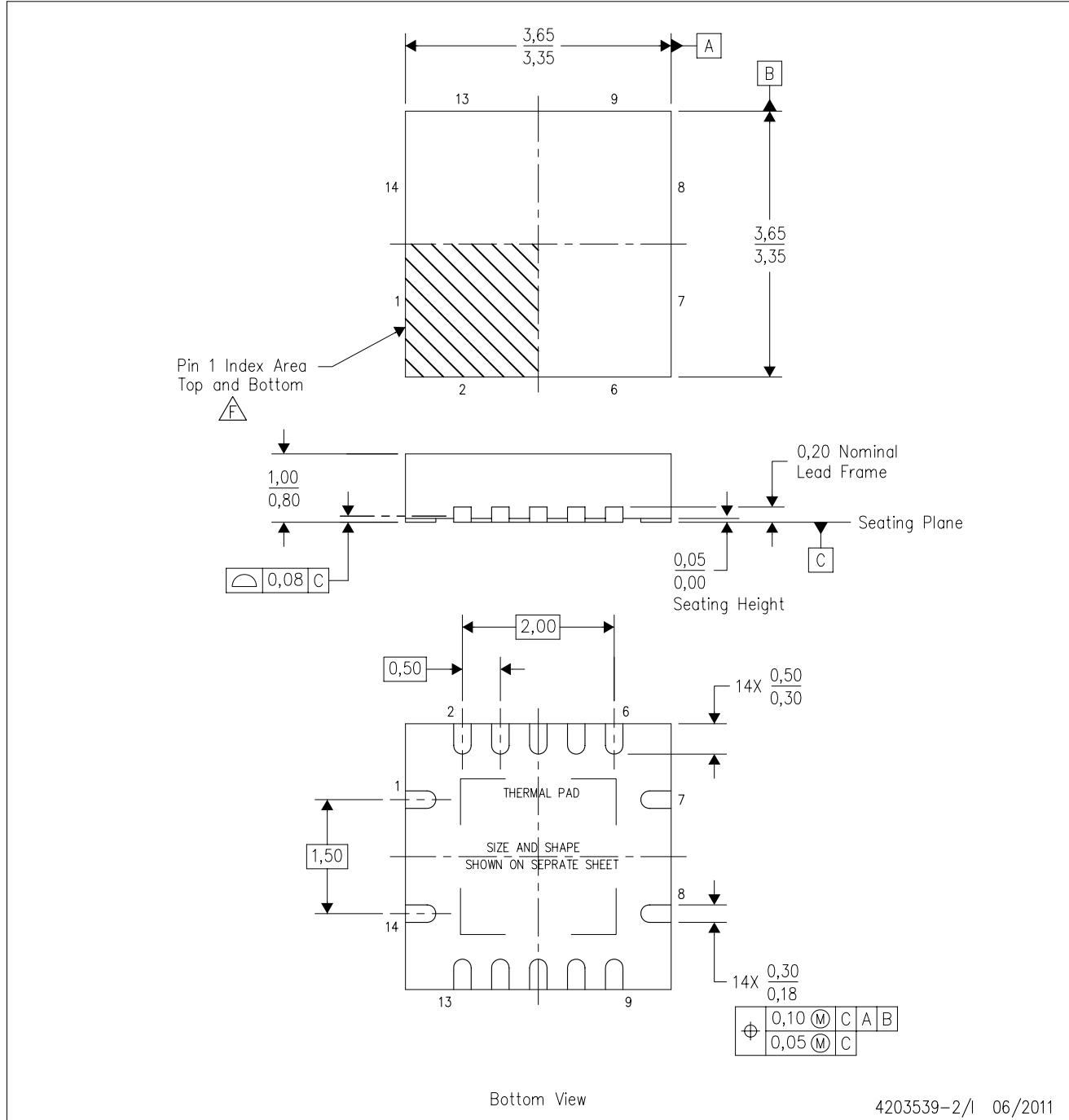
4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - $\triangle F$  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.



## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

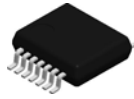
24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

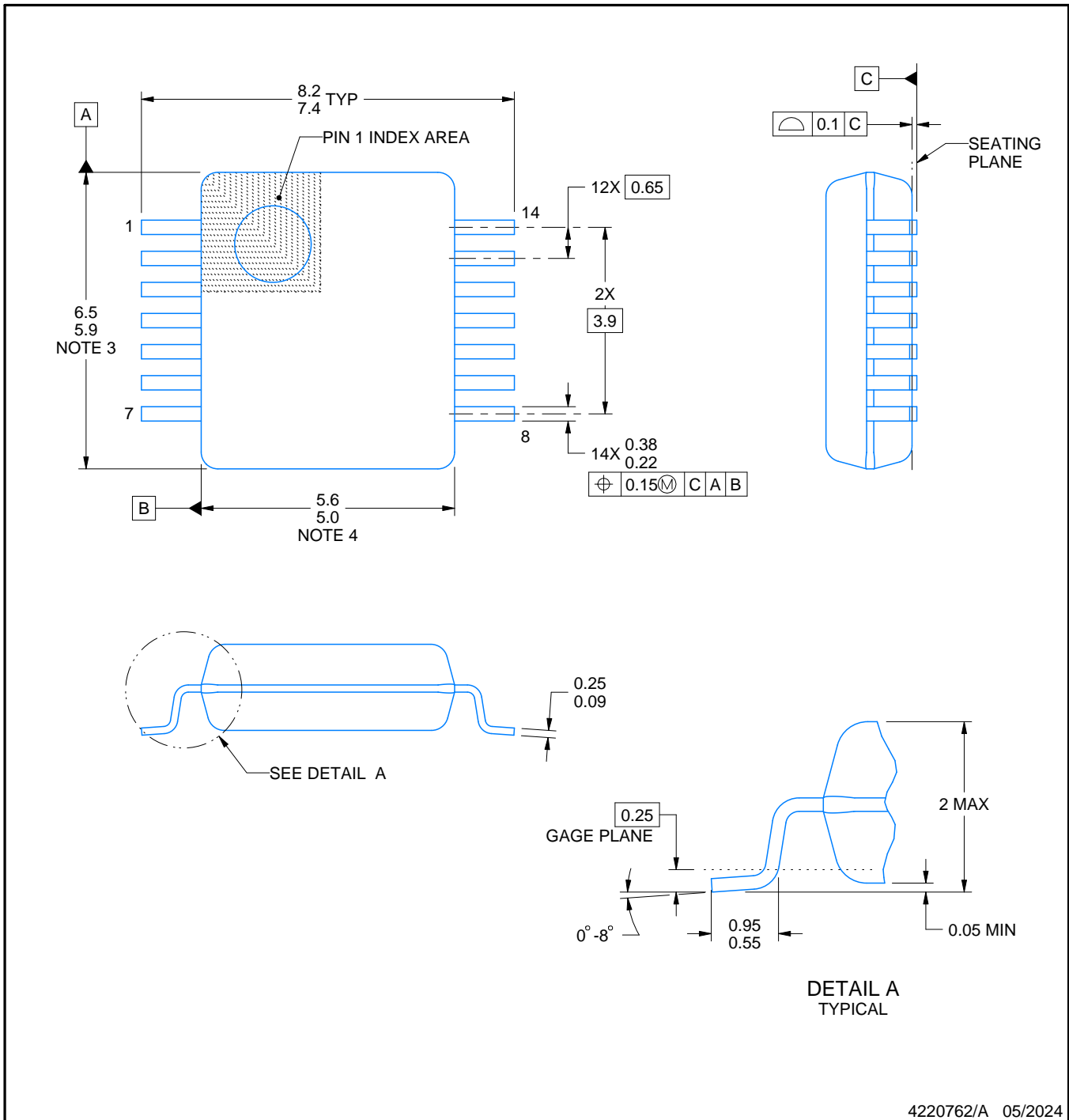
# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

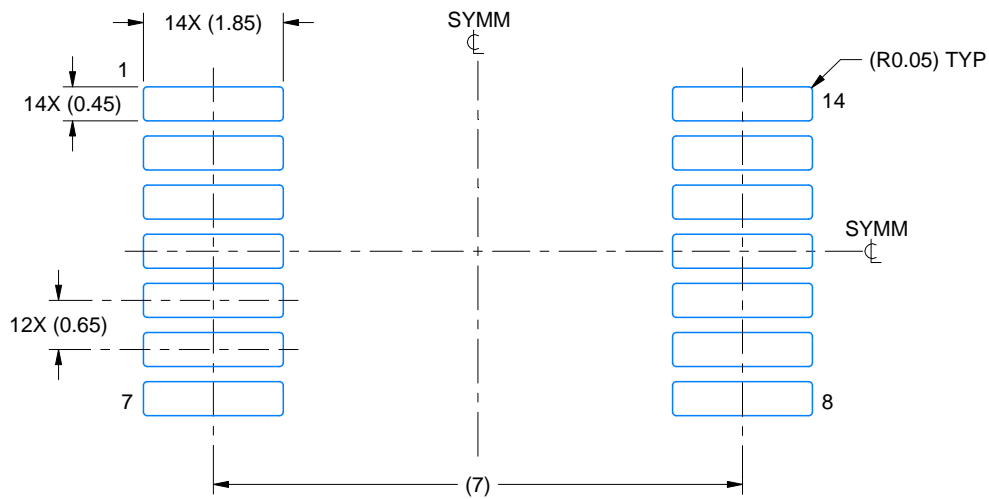
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

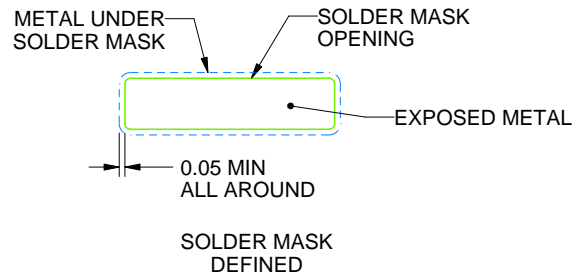
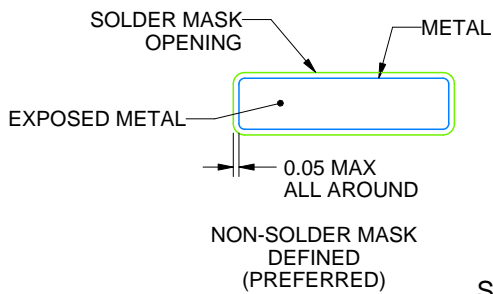
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

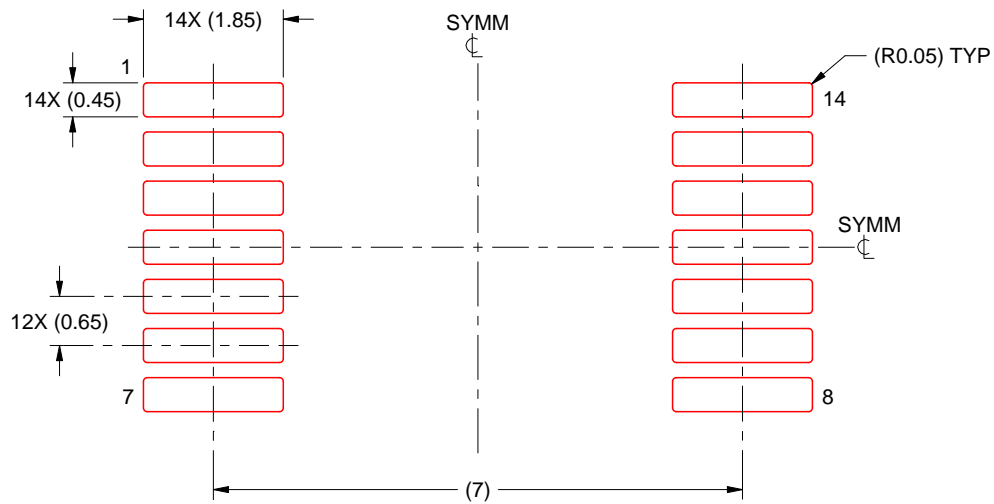
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



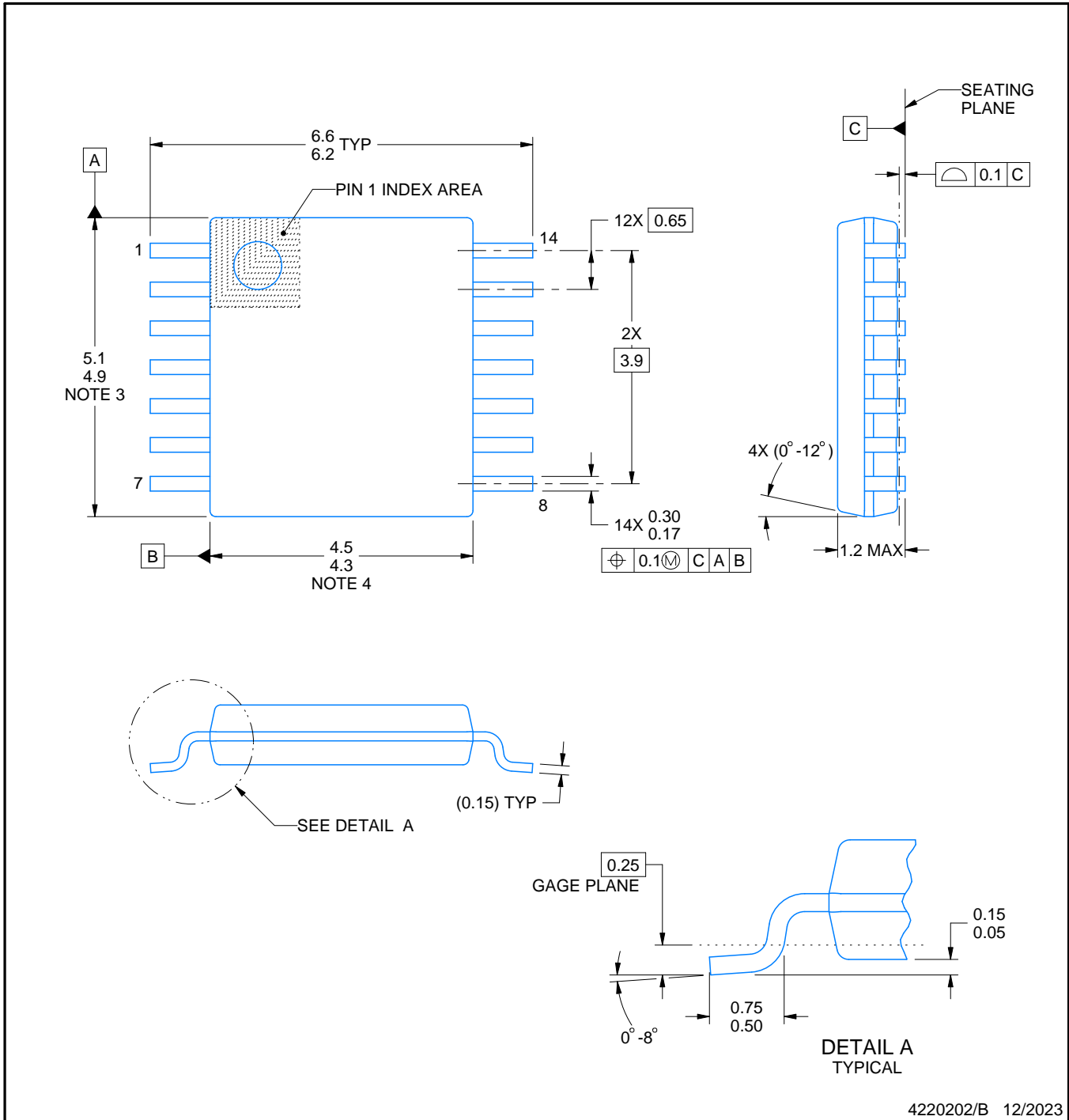
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

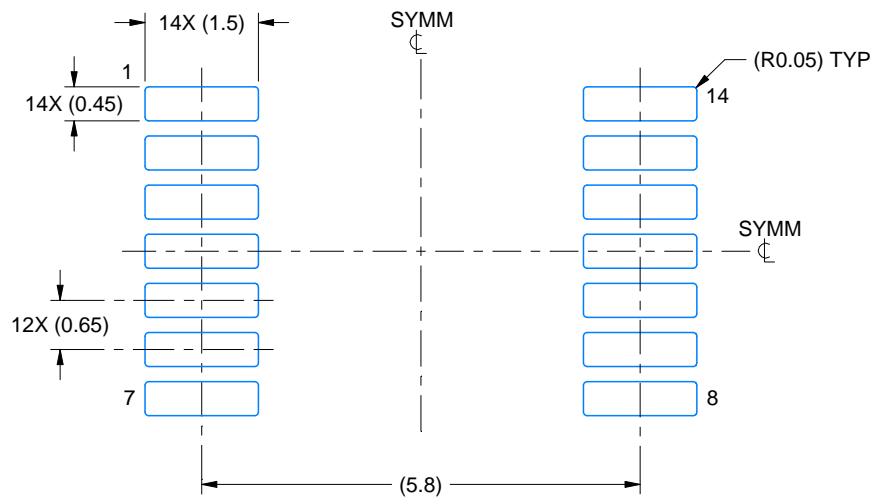
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

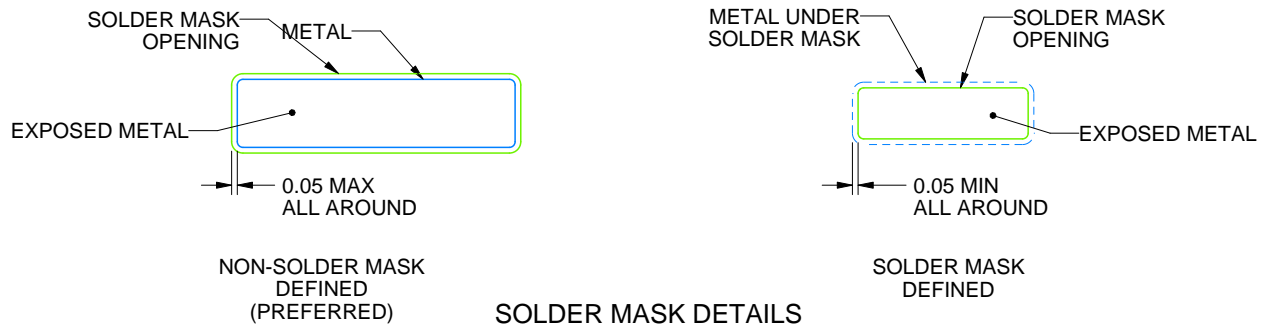
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

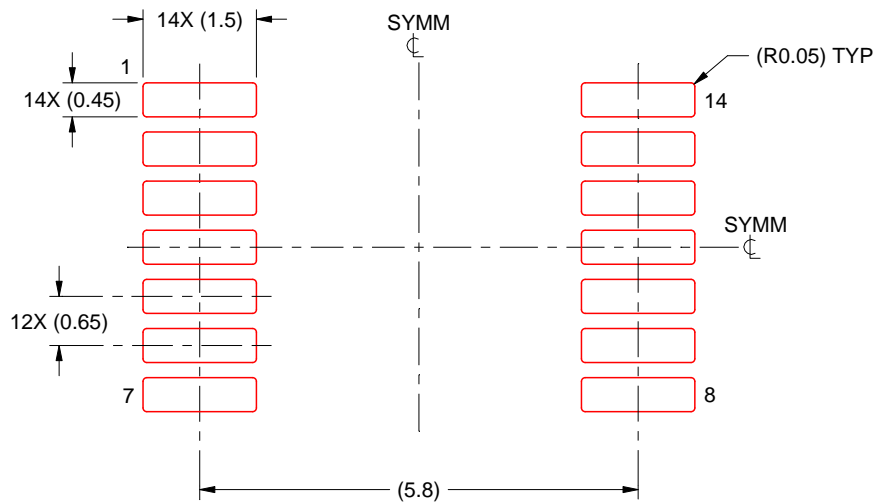


# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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