

SN74AHCT595-Q1 Automotive 8-Bit Shift Registers With 3-State Output Registers

1 Features

- AEC-Q100 qualified for automotive applications:
 - Device temperature grade 1: -40°C to +125°C
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C4B
- Available in wettable flank QFN package
- Operating range 4.5V to 5.5V V_{CC}
- TTL-Compatible inputs
- Low delay, 6ns typ (25°C, 5V)
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Network switches
- Power infrastructures
- PCs and notebooks
- LED displays
- Servers

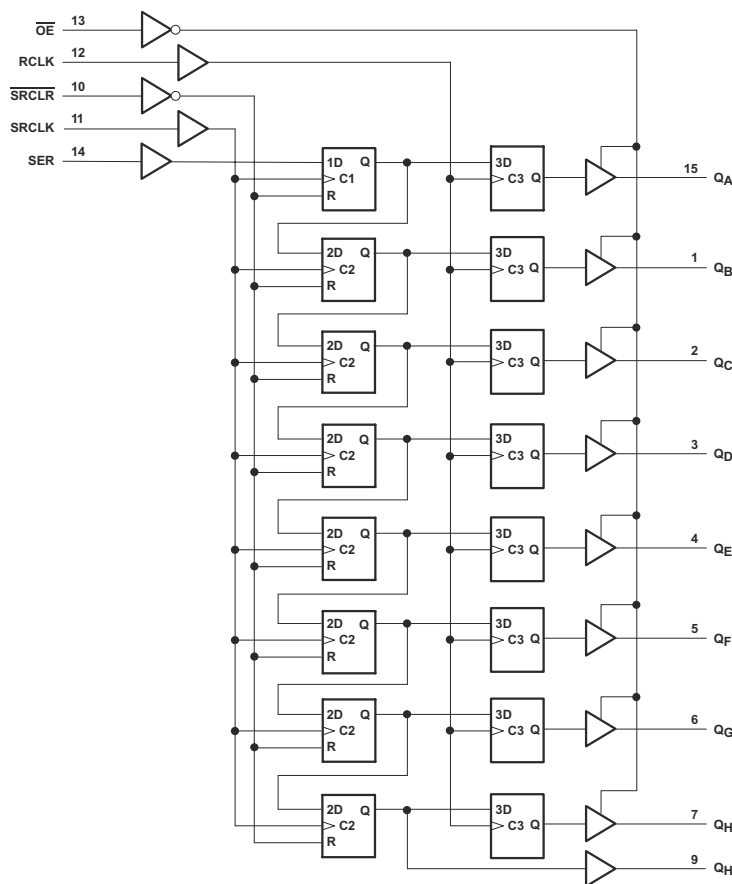
3 Description

The SN74AHCT595-Q1 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE (NOM) ⁽³⁾
SN74AHCT595-Q1	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	PW (TSSOP, 16)	5.0mm × 6.4mm	5.0mm × 4.4mm

- For more information, see [Section 11](#).
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Pin numbers shown are for the PW and BQB packages.

Simplified Schematic



Table of Contents

1 Features	1	7.3 Feature Description.....	10
2 Applications	1	7.4 Device Functional Modes.....	12
3 Description	1	8 Application and Implementation	13
4 Pin Configuration and Functions	3	8.1 Application Information.....	13
5 Specifications	4	8.2 Typical Application.....	13
5.1 Absolute Maximum Ratings.....	4	8.3 Power Supply Recommendations.....	14
5.2 ESD Ratings.....	4	8.4 Layout.....	14
5.3 Recommended Operating Conditions.....	4	9 Device and Documentation Support	16
5.4 Thermal Information.....	4	9.1 Documentation Support.....	16
5.5 Electrical Characteristics.....	5	9.2 Receiving Notification of Documentation Updates....	16
5.6 Timing Characteristics.....	5	9.3 Support Resources.....	16
5.7 Switching Characteristics.....	6	9.4 Trademarks.....	16
5.8 Noise Characteristics.....	6	9.5 Electrostatic Discharge Caution.....	16
5.9 Typical Characteristics.....	7	9.6 Glossary.....	16
6 Parameter Measurement Information	8	10 Revision History	16
7 Detailed Description	9	11 Mechanical, Packaging, and Orderable Information	16
7.1 Overview.....	9		
7.2 Functional Block Diagram.....	9		

4 Pin Configuration and Functions

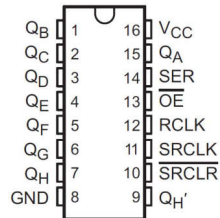


Figure 4-1.
SN74AHCT595-Q1 PW Package (Top View)

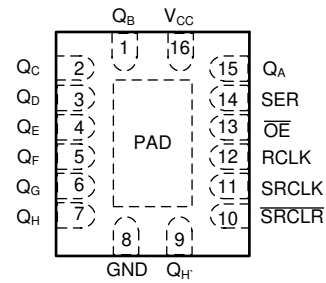


Figure 4-2. SN74AHCT595-Q1 BQB Package, 16-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
Q _B	1	O	Q _B Output
Q _C	2	O	Q _C Output
Q _D	3	O	Q _D Output
Q _E	4	O	Q _E Output
Q _F	5	O	Q _F Output
Q _G	6	O	Q _G Output
Q _H	7	O	Q _H Output
GND	8	—	Ground Pin
Q _H '	9	O	Q _H ' Output
SRCLR	10	I	SRCLR Input
SRCLK	11	I	SRCLK Input
RCLK	12	I	RCLK Input
OE	13	I	Output Enable
SER	14	I	SER Input
Q _A	15	O	Q _A Output
V _{CC}	16	—	Power Pin
Thermal Pad ⁽²⁾		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) I = input, O = output

(2) BQB package only

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I	Input voltage range ⁽²⁾	-0.5	7	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	7	V
V _O	Output voltage range ⁽²⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < -0.5V	-20	mA
I _{OK}	Output clamp current	V _O < -0.5V or V _O > V _{CC} + 0.5V	±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±25	mA
	Continuous output current through V _{CC} or GND		±75	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
V _{CC}	Supply voltage		4.5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 5V	2		V
V _{IL}	Low-Level input voltage	V _{CC} = 5V		0.8	V
V _I	Input Voltage		0	5.5	V
V _O	Output Voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 5V ± 0.5V		-8	mA
I _{OL}	Low-level output current	V _{CC} = 5V ± 0.5V		8	mA
Δt/Δv	Input transition rise or fall rate	V _{CC} = 5V ± 0.5V		20	ns/V
T _A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		WBQB (WQFN)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	105.6	135.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	96.6	70.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	75.4	81.3	°C/W

5.4 Thermal Information (continued)

THERMAL METRIC ⁽¹⁾		WBQB (WQFN)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	
Ψ_{JT}	Junction-to-top characterization parameter	19.1	22.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	75.4	80.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	56.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 125^\circ\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	$I_{OH} = -50\mu\text{A}$	4.5V	4.4	4.5		4.4		V	
	$I_{OH} = -8\text{mA}$	4.5V	3.94			3.8			
V_{OL}	$I_{OL} = 50\mu\text{A}$	4.5V			0.1		0.1	V	
	$I_{OL} = 8\text{mA}$	4.5V			0.36		0.44		
I_I	$V_I = 5.5\text{V or GND and } V_{CC} = 0\text{V to } 5.5\text{V}$	0V to 5.5V			± 0.1		± 1	μA	
I_{OZ}	$V_O = V_{CC} \text{ or GND and } V_{CC} = 5.5\text{V}$	5.5V			± 0.25		± 2.5	μA	
I_{CC}	$V_I = V_{CC} \text{ or GND, } I_O = 0, \text{ and } V_{CC} = 5.5\text{V}$	5.5V			4		40	μA	
ΔI_{CC}	One input at 3.4V, Other inputs at V_{CC} or GND	5V			1.35		1.5	mA	
C_I	$V_I = V_{CC} \text{ or GND}$	5V		4	10		10	pF	
C_O	$V_O = V_{CC} \text{ or GND}$	5V		5				pF	
C_{PD}	No load, $F = 1\text{MHz}$	5V		129				pF	

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	MAX	MIN	MAX	
t_H	Hold time	SER after SRCLK \uparrow	$5\text{V} \pm 0.5\text{V}$	2		2		ns
t_{SU}	Setup time	SER before SRCLK \uparrow	$5\text{V} \pm 0.5\text{V}$	3		3		ns
t_{SU}	Setup time	SRCLK \uparrow before RCLK \uparrow	$5\text{V} \pm 0.5\text{V}$	5		5		ns
t_{SU}	Setup time	SRCLR high (inactive) before SRCLK \uparrow	$5\text{V} \pm 0.5\text{V}$	2.9		3.8		ns
t_{SU}	Setup time	SRCLR low before RCLK \uparrow	$5\text{V} \pm 0.5\text{V}$	5		5		ns
t_W	Pulse duration	RCLK or SRCLK high or low	$5\text{V} \pm 0.5\text{V}$	5		5.5		ns
t_W	Pulse duration	SRCLR low	$5\text{V} \pm 0.5\text{V}$	5		5.5		ns

5.7 Switching Characteristics

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
F _{MAX}	-	-	C _L = 15pF	5V ± 0.5V	135	175		115			MHz
t _{PZL}	\overline{OE}	Q	C _L = 15pF	5V ± 0.5V		5.4	8.6			12	ns
t _{PZH}	\overline{OE}	Q	C _L = 15pF	5V ± 0.5V		4.3	8.6			12	ns
t _{PLZ}	\overline{OE}	Q	C _L = 15pF	5V ± 0.5V		3.8	8	1		10.5	ns
t _{PHZ}	\overline{OE}	Q	C _L = 15pF	5V ± 0.5V		3.8	8	1		10.5	ns
t _{PLH}	RCLK	QA-QH	C _L = 15pF	5V ± 0.5V		4.3	7.4	1		9.5	ns
t _{PHL}	RCLK	QA-QH	C _L = 15pF	5V ± 0.5V		4.3	7.4	1		9.5	ns
t _{PLH}	SRCLK	QH'	C _L = 15pF	5V ± 0.5V		4.5	8.2	1		10.4	ns
t _{PHL}	SRCLK	QH'	C _L = 15pF	5V ± 0.5V		4.5	8.2	1		10.4	ns
t _{PHL}	\overline{SRCLR}	QH'	C _L = 15pF	5V ± 0.5V		4.5	8	1		10.1	ns
F _{MAX}	-	-	C _L = 50pF	5V ± 0.5V	120	140		95			MHz
t _{PZL}	\overline{OE}	Q	C _L = 50pF	5V ± 0.5V		6.8	10.6			14.4	ns
t _{PZH}	\overline{OE}	Q	C _L = 50pF	5V ± 0.5V		5.7	10.6			14.4	ns
t _{PLZ}	\overline{OE}	Q	C _L = 50pF	5V ± 0.5V		3.4	10.3			13.2	ns
t _{PHZ}	\overline{OE}	Q	C _L = 50pF	5V ± 0.5V		3.5	10.3			13.2	ns
t _{PLH}	RCLK	QA-QH	C _L = 50pF	5V ± 0.5V		5.6	9.4	1		11.5	ns
t _{PHL}	RCLK	QA-QH	C _L = 50pF	5V ± 0.5V		5.6	9.4	1		11.5	ns
t _{PLH}	SRCLK	QH'	C _L = 50pF	5V ± 0.5V		6.4	10.2	1		12.4	ns
t _{PHL}	SRCLK	QH'	C _L = 50pF	5V ± 0.5V		6.4	10.2	1		12.4	ns
t _{PHL}	\overline{SRCLR}	QH'	C _L = 50pF	5V ± 0.5V		6.4	10	1		12.1	ns

5.8 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.2	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}	-0.9	-0.2		V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}	4.4	4.7		V
V _{IH(D)}	High-level dynamic input voltage	2			V
V _{IL(D)}	Low-level dynamic input voltage			0.8	V

5.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

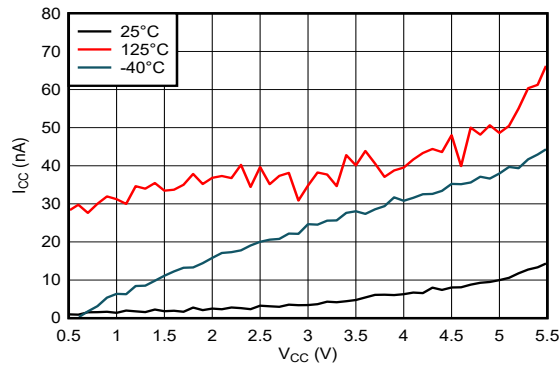


Figure 5-1. Supply Current Across Supply Voltage

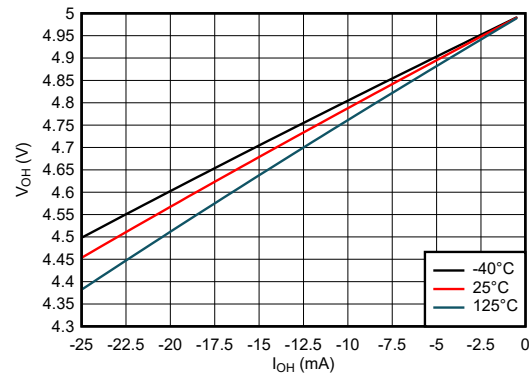


Figure 5-2. Output Voltage vs Current in HIGH State; 5V Supply

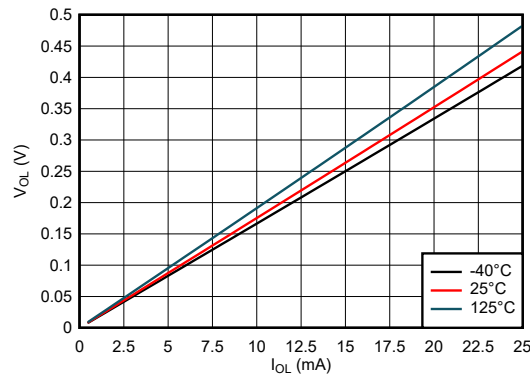


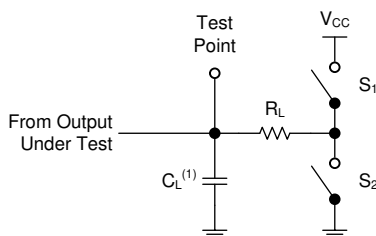
Figure 5-3. Output Voltage vs Current in LOW State; 5V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR \leq 1MHz, $Z_O = 50\Omega$, $t_f < 2.5\text{ns}$.

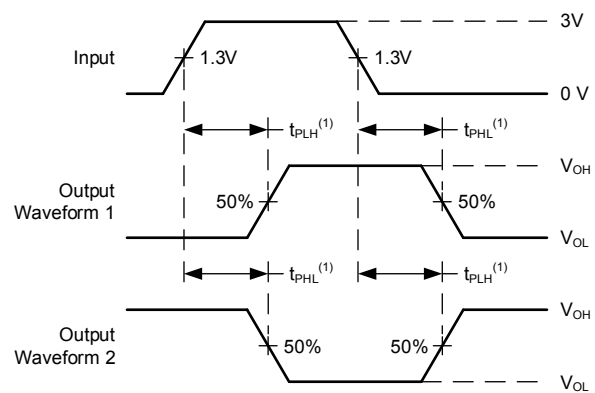
The outputs are measured individually with one input transition per measurement.

TEST	S1	S2	R_L	C_L	ΔV	V_{CC}
t_{PLH} , t_{PHL}	OPEN	OPEN	—	15pF, 50pF	—	ALL
t_{PLZ} , t_{PZL}	CLOSED	OPEN	1 k Ω	15pF, 50pF	0.15V	$\leq 2.5V$
t_{PHZ} , t_{PZH}	OPEN	CLOSED	1 k Ω	15pF, 50pF	0.15V	$\leq 2.5V$
t_{PLZ} , t_{PZL}	CLOSED	OPEN	1 k Ω	15pF, 50pF	0.3V	$> 2.5V$
t_{PHZ} , t_{PZH}	OPEN	CLOSED	1 k Ω	15pF, 50pF	0.3V	$> 2.5V$



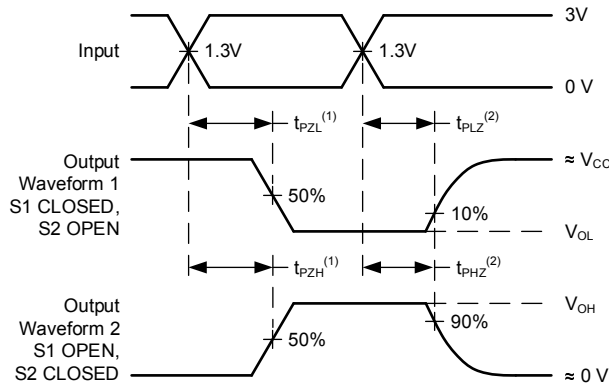
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

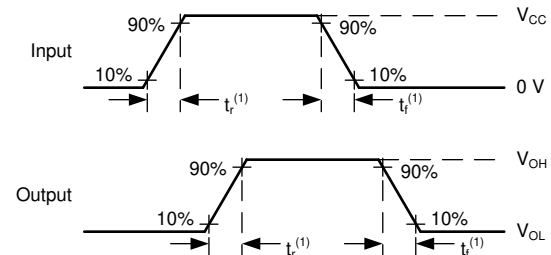
Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_{PZL} and t_{PZH} is the same as t_{en} .

(2) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis} .

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

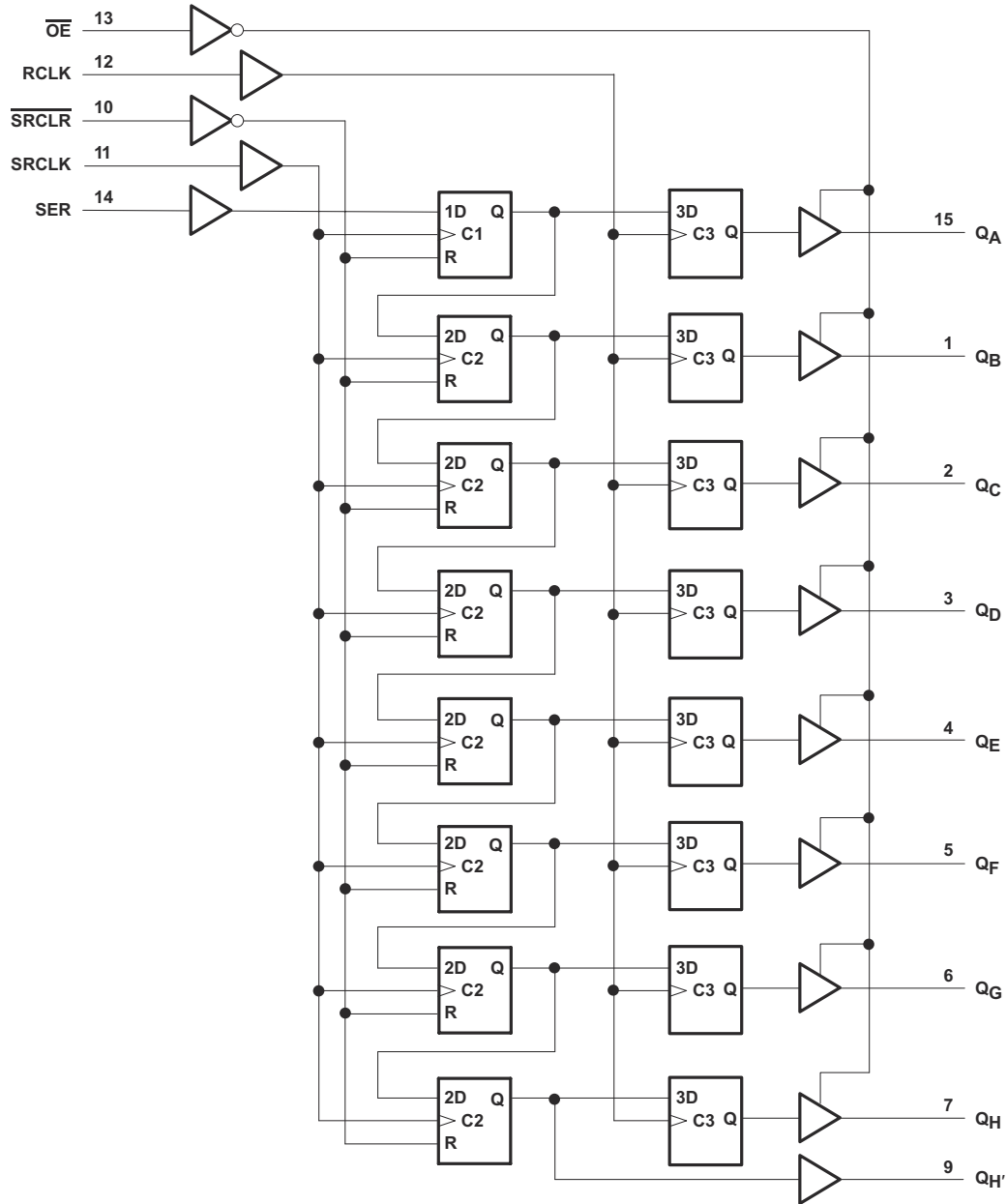
Figure 6-4. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74AHCT595-Q1 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for the shift and storage registers. The shift register has a direct overriding clear ($\overline{\text{SRCLR}}$) input, serial (SER) input, and serial outputs for cascading. When the output-enable ($\overline{\text{OE}}$) input is high, the outputs are in the high-impedance state. Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, then the shift register always is one clock pulse ahead of the storage register.

7.2 Functional Block Diagram



Pin numbers shown are for the PW and BQB packages.

7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

7.3.3 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the [Implications of Slow or Floating CMOS Inputs](#) application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and typically will meet all requirements.

7.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet where packages include this feature.

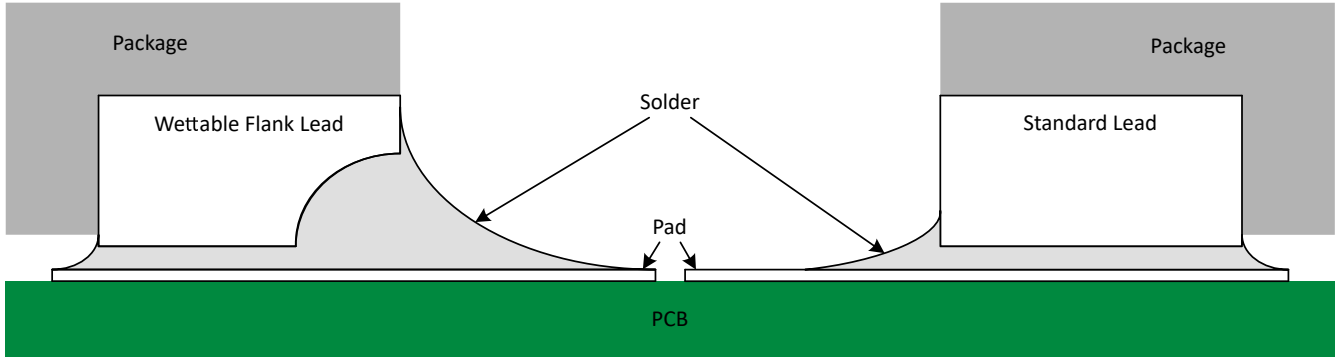


Figure 7-1. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 7-1, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

7.3.5 Clamp Diode Structure

As Figure 7-2 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

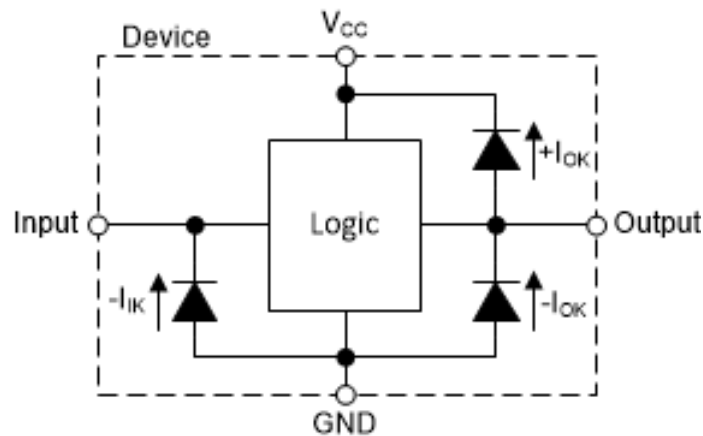


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	\overline{OE}	
X	X	X	X	H	Outputs Q _A – Q _H are disabled.
X	X	X	X	L	Outputs Q _A – Q _H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the storage register.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AHCT595-Q1 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8V V_{IL} and 2V V_{IH} . This feature makes it an excellent choice for translating up from 3.3V to 5V. Figure 8-1 shows this type of translation.

8.2 Typical Application

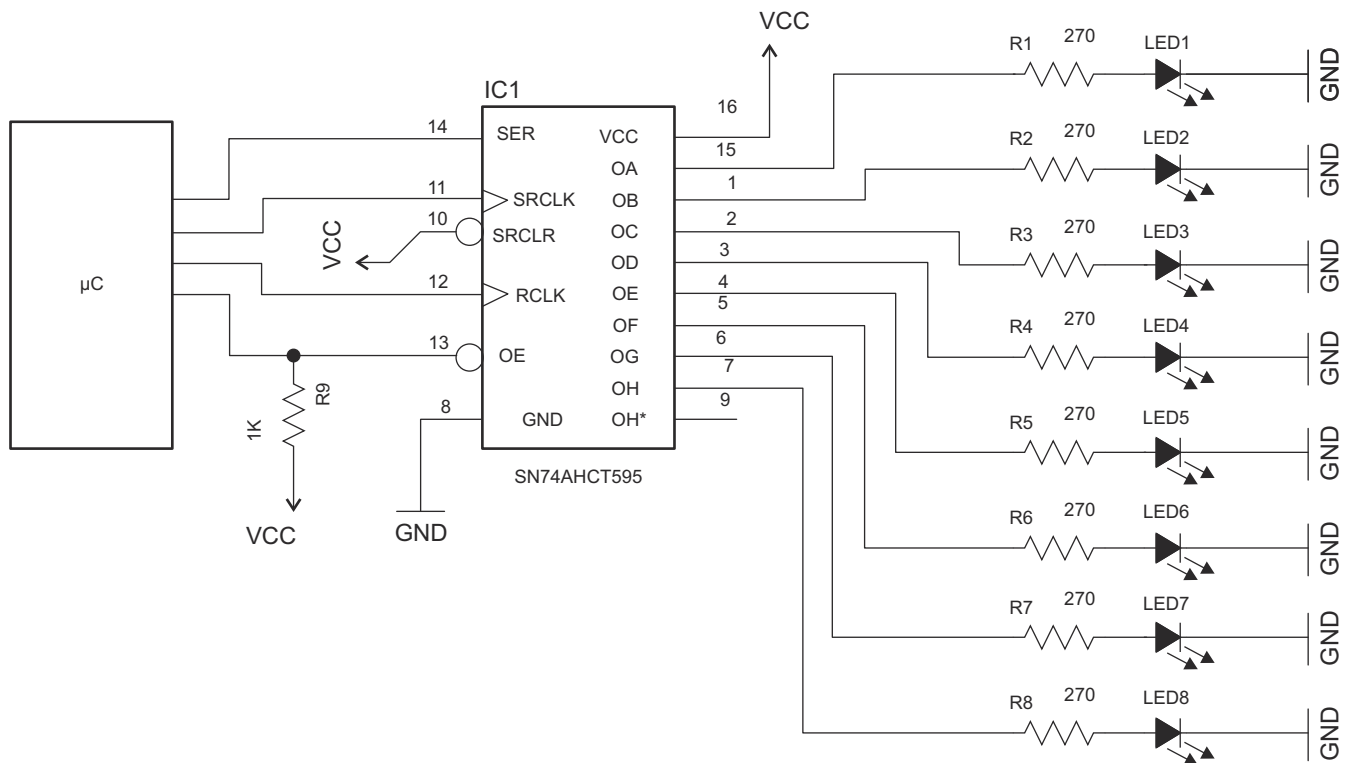


Figure 8-1. Specific Application Schematic

8.2.1 Design Requirements

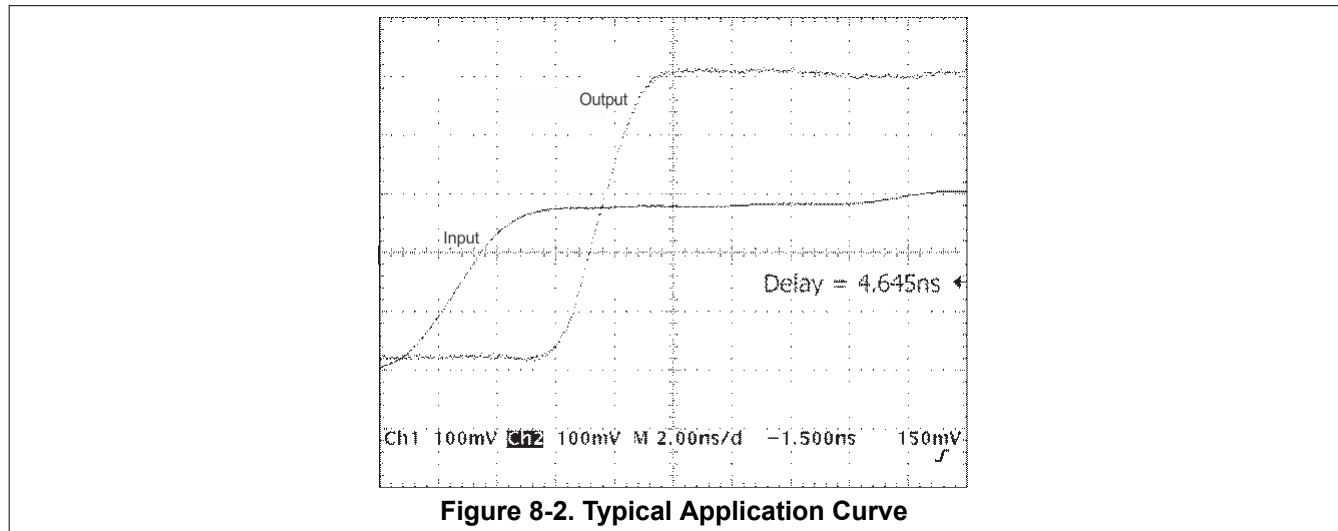
This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended input conditions
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid V_{CC}

- Recommend output conditions
 - Load currents should not exceed 25mA per output and 50mA total for the part
 - Outputs should not be pulled above V_{CC}

8.2.3 Application Curves



8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended; if there are multiple V_{CC} pins, then 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 μ F and a 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 8-3](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

8.4.2 Layout Example

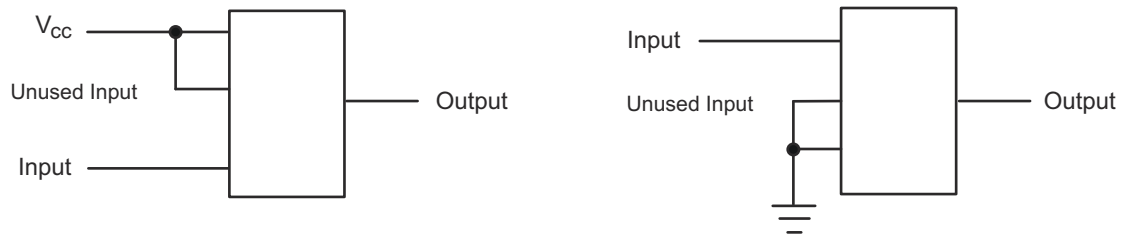


Figure 8-3. Layout Diagram

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#)
- Texas Instruments, [Understanding Schmitt Triggers](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CAHCT595QWBQBRQ1	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AT595Q
CAHCT595QWBQBRQ1.A	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AT595Q
SN74AHCT595QPWRQ1	Active	Production	TSSOP (PW) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHT595Q
SN74AHCT595QPWRQ1.A	Active	Production	TSSOP (PW) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHT595Q
SN74AHCT595QPWRQ1.B	Active	Production	TSSOP (PW) 16	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHCT595-Q1 :

- Catalog : [SN74AHCT595](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAHCT595QWBQRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74AHCT595QPWRQ1	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAHCT595QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74AHCT595QPWRQ1	TSSOP	PW	16	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

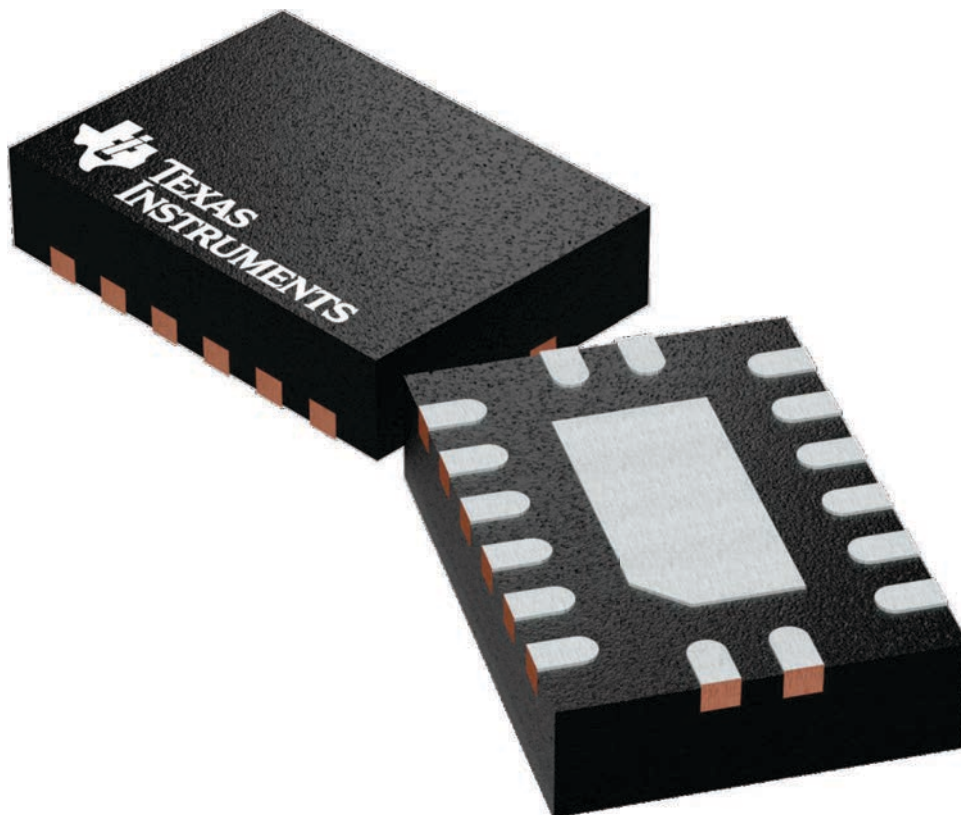
BQB 16

WQFN - 0.8 mm max height

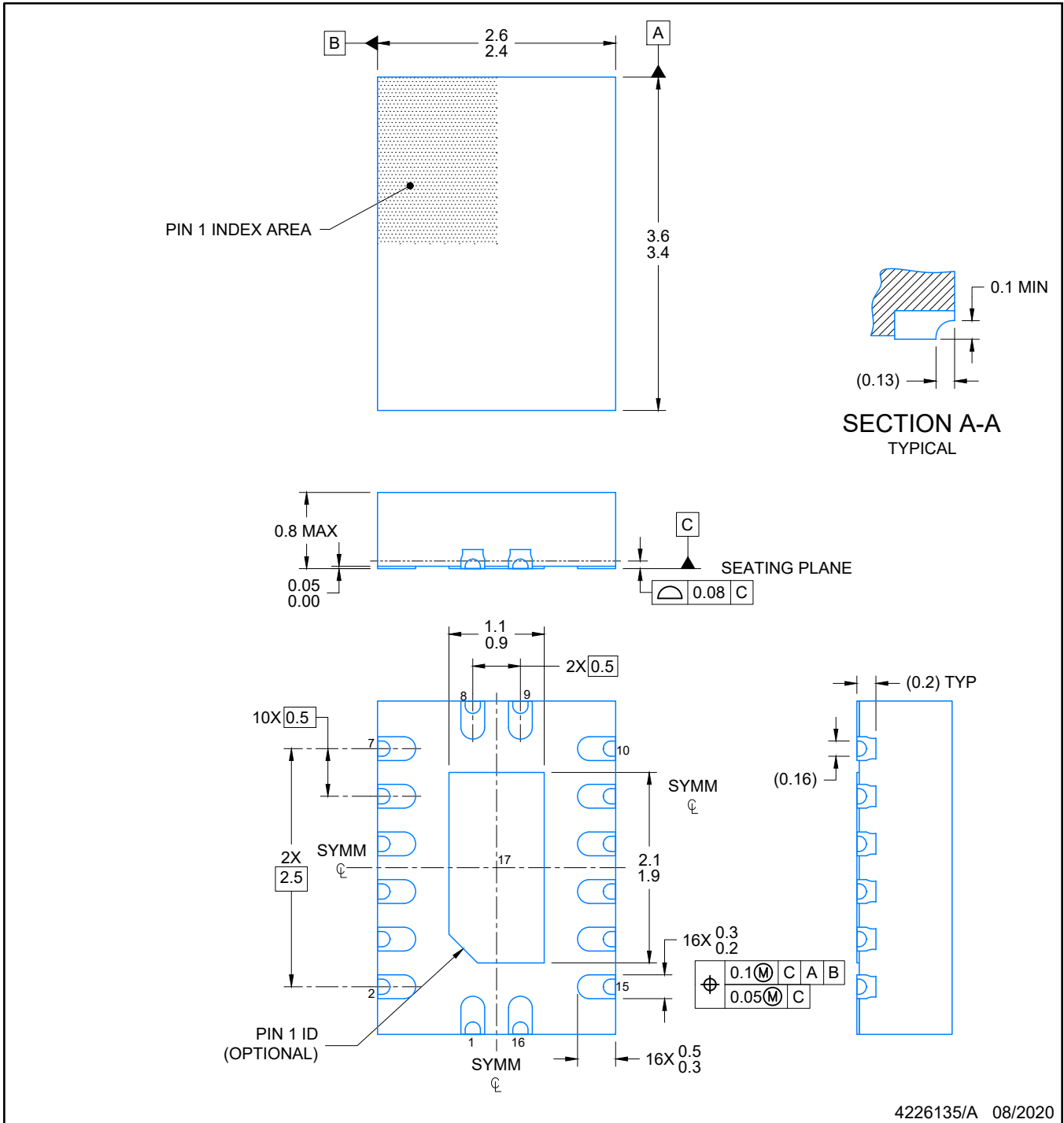
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



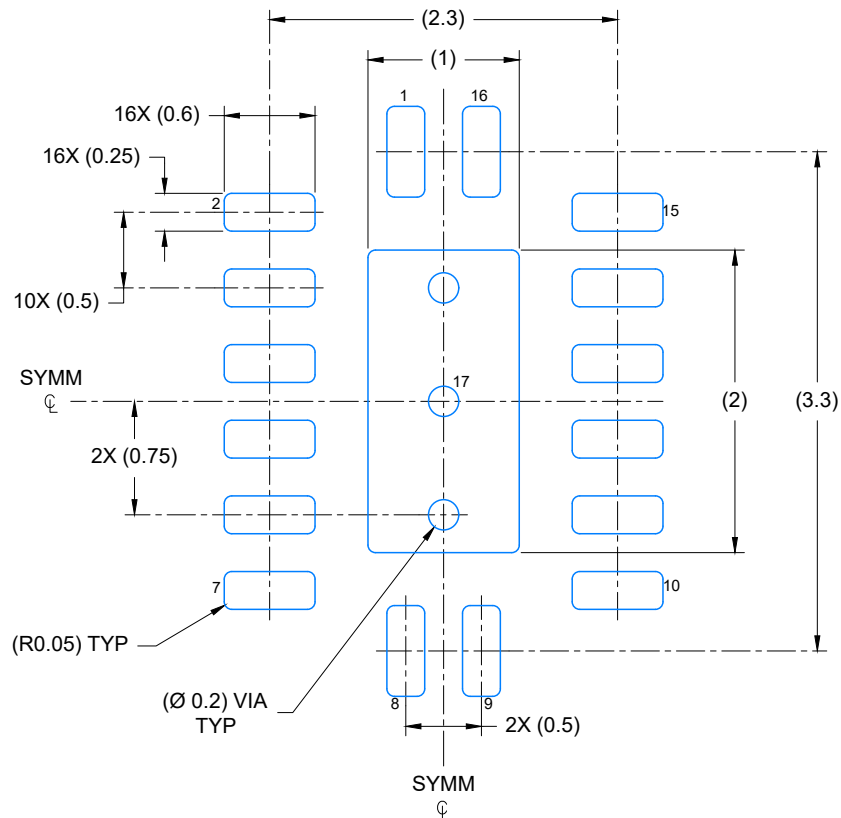
4226161/A



4226135/A 08/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

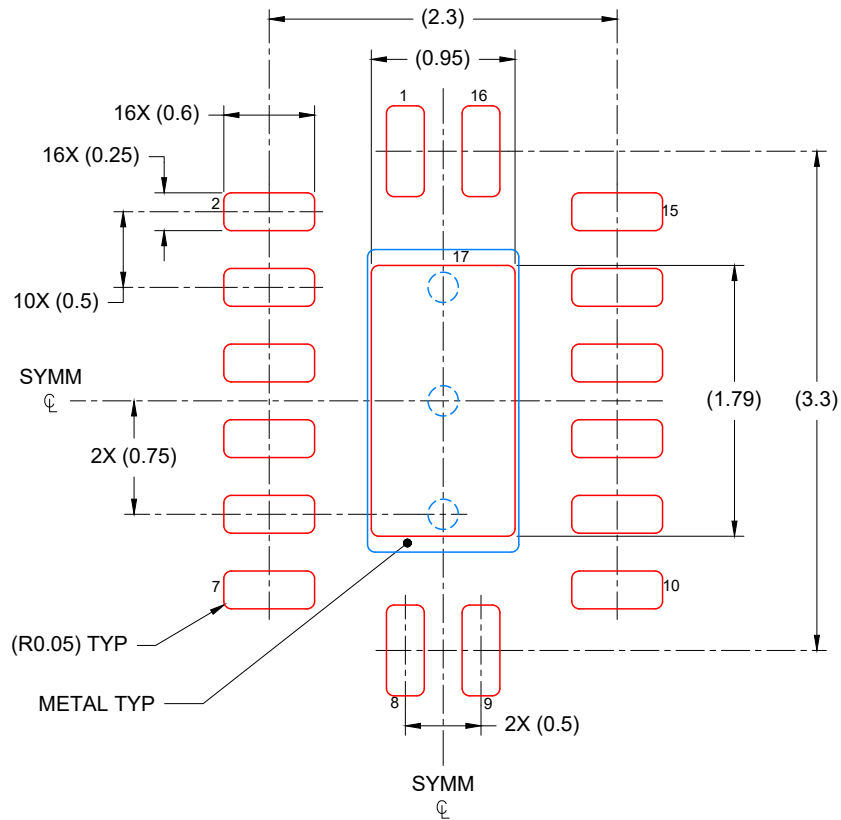


LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



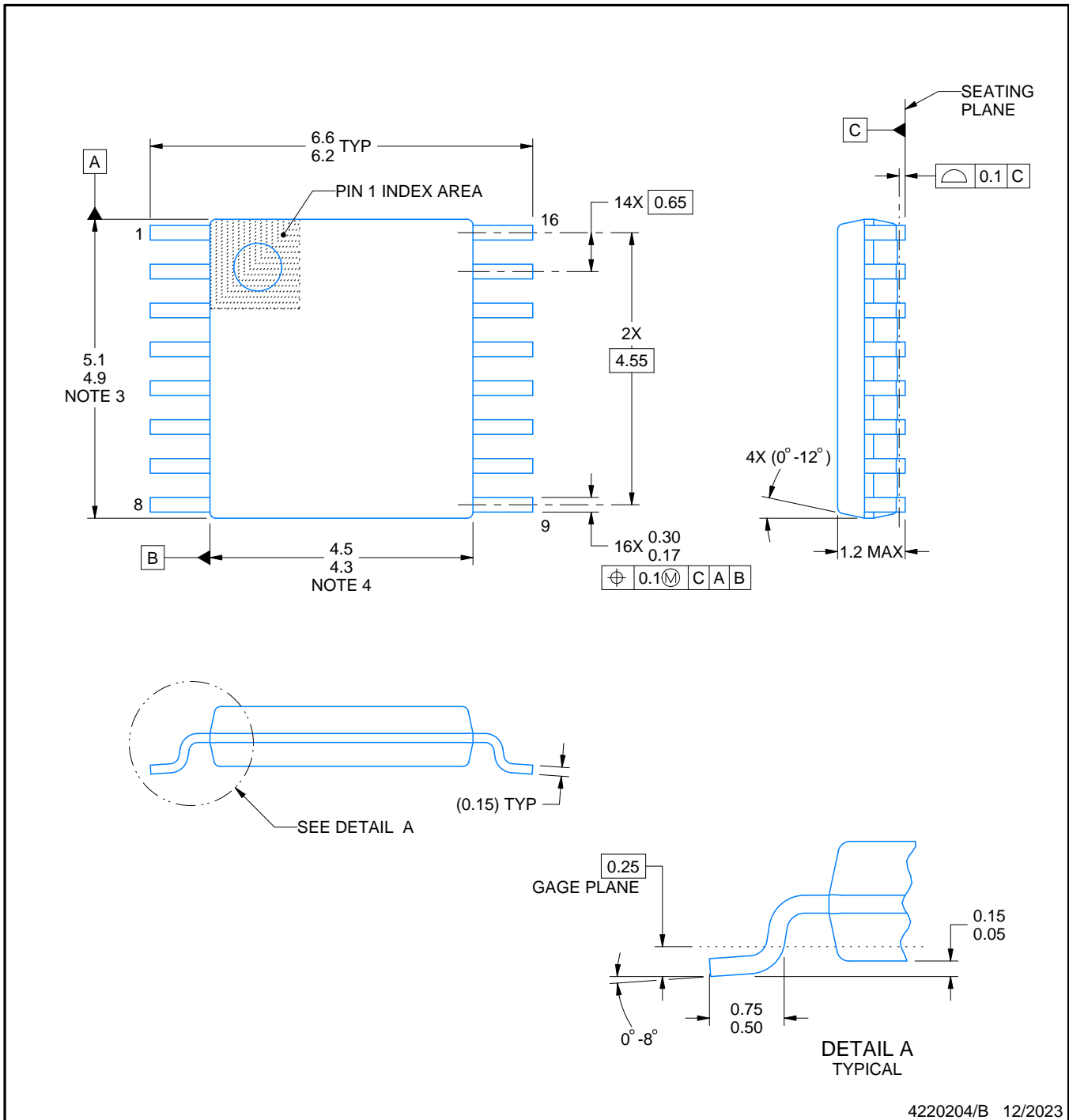
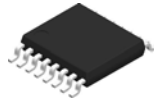
SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 85% PRINTED COVERAGE BY AREA
 SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220204/B 12/2023

NOTES:

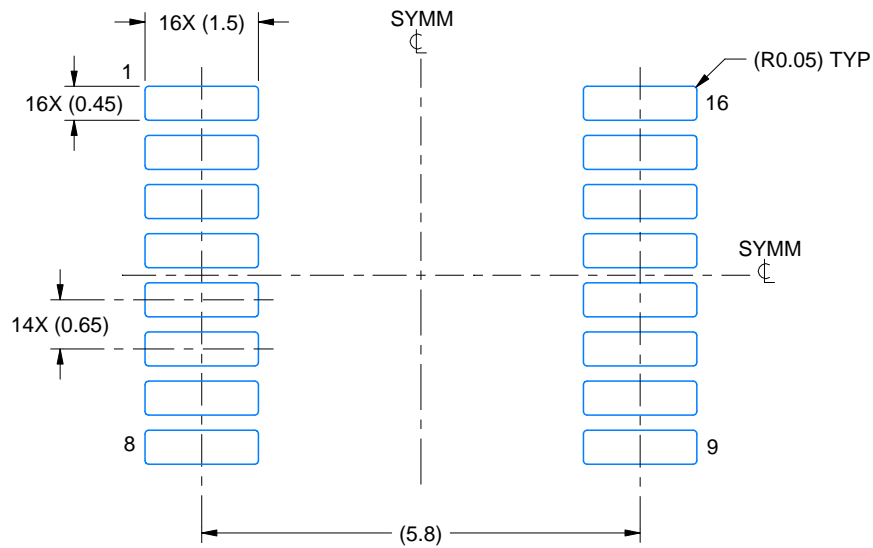
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

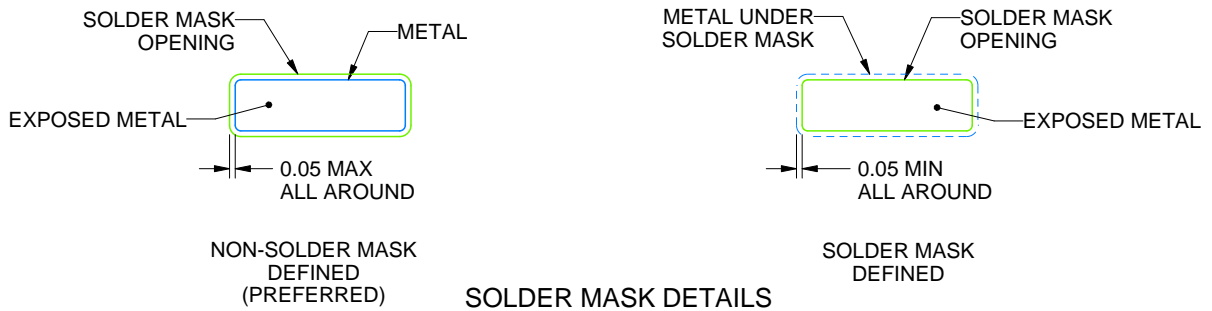
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

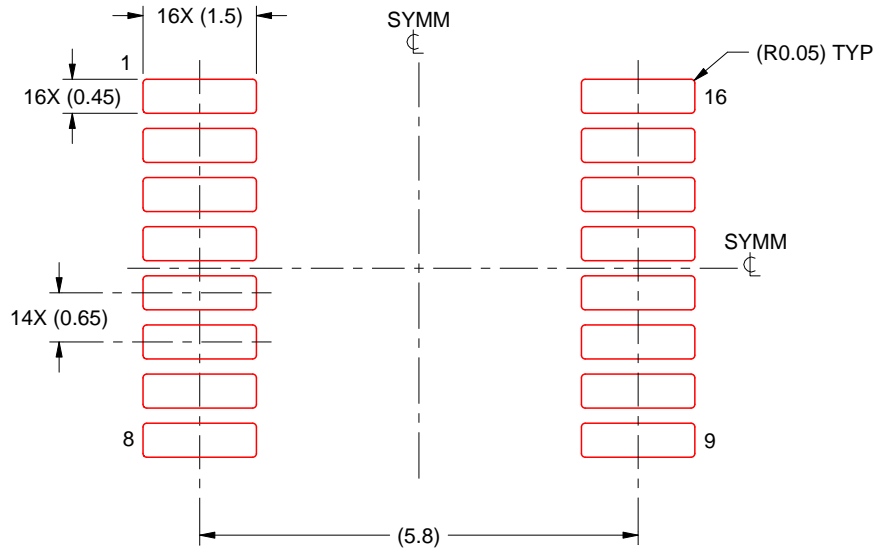
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025