

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

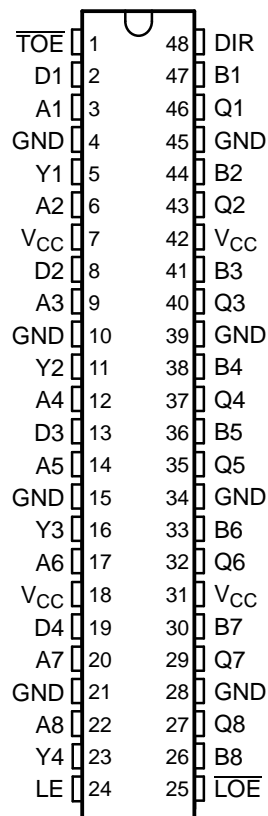
DESCRIPTION/ORDERING INFORMATION

This device contains four independent noninverting buffers and an 8-bit noninverting bus transceiver and D-type latch, designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16973 is particularly suitable for demultiplexing an address/data bus into a dedicated address bus and dedicated data bus. The device is used where there is asynchronous bidirectional communication between the A and B data bus, and the address signals are latched and buffered on the Q bus. The control-function implementation minimizes external timing requirements.

This device can be used as one 4-bit buffer, one 8-bit transceiver, or one 8-bit latch. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The transceiver output-enable (\overline{TOE}) input can be used to disable the transceivers so that the A and B buses effectively are isolated.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVCH16973DL	ALVCH16973
		Tape and reel	SN74ALVCH16973DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCH16973DGGR	ALVCH16973
	TVSOP - DGV	Tape and reel	SN74ALVCH16973DGVR	VH973

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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Widebus is a trademark of Texas Instruments.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

When the latch-enable (LE) input is high, the Q outputs follow the data (A) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the A inputs. The latch output-enable ($\overline{\text{LOE}}$) input can be used to place the nine Q outputs in either a normal logic state (high or low logic level) or the high-impedance state. In the high-impedance state, the Q outputs neither drive nor load the bus lines significantly. $\overline{\text{LOE}}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the Q outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{LOE}}$ and $\overline{\text{TOE}}$ should be tied to V_{CC} through pullup resistors; the minimum values of the resistors are determined by the current-sinking capability of the drivers.

The four independent noninverting buffers perform the Boolean function $Y = D$ and are independent of the state of DIR, $\overline{\text{TOE}}$, LE, and $\overline{\text{LOE}}$.

The A and B I/Os and D inputs have bus-hold circuitry. Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

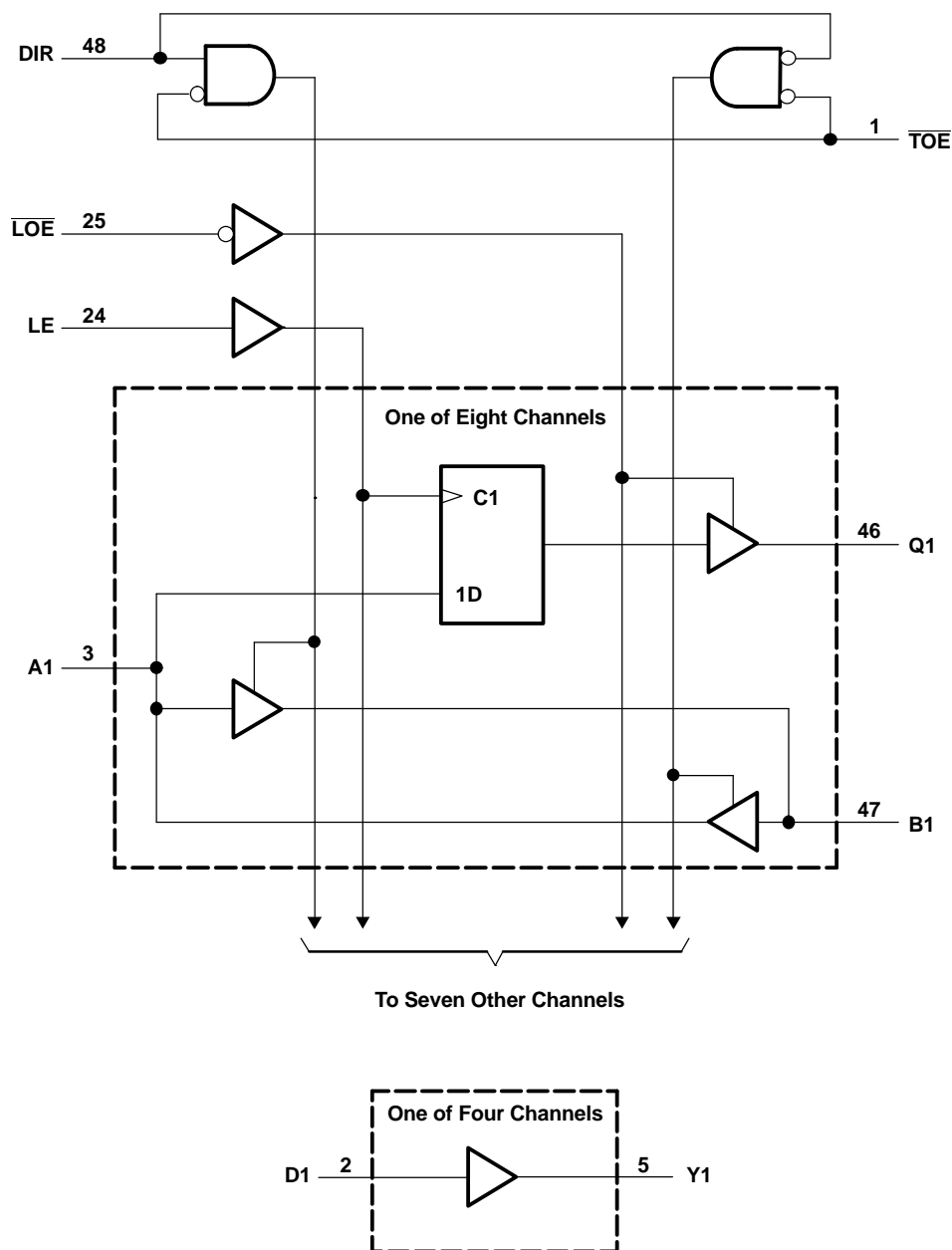
FUNCTION TABLES

INPUTS		OPERATION
$\overline{\text{TOE}}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	A bus and B bus isolation

INPUTS			OUTPUT Q
$\overline{\text{LOE}}$	LE	A	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

INPUT D	OUTPUT Y
L	L
H	H

LOGIC DIAGRAM (POSITIVE LOGIC)



SN74ALVCH16973

8-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH FOUR INDEPENDENT BUFFERS

SCES435B–APRIL 2003–REVISED SEPTEMBER 2004

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
V _I	Input voltage range	Except I/O and D input ports ⁽²⁾	-0.5	4.6	V
		I/O and D input ports ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	
V _O	Output voltage range ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through each V _{CC} or GND			±100	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DGG package		70	°C/W
		DGV package		58	
		DL package		63	
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 3 V to 3.6 V		0.8	
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		-4	mA
		V _{CC} = 2.3 V		-12	
		V _{CC} = 2.7 V		-12	
		V _{CC} = 3 V		-24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		12	
		V _{CC} = 2.7 V		12	
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN TYP ⁽¹⁾ MAX	UNIT
V _{OH}		I _{OH} = -100 µA	1.65 V to 3.6 V	V _{CC} - 0.2	V
		I _{OH} = -4 mA	1.65 V	1.2	
		I _{OH} = -6 mA	2.3 V	2	
		I _{OH} = -12 mA	2.3 V	1.7	
			2.7 V	2.2	
			3 V	2.4	
		I _{OH} = -24 mA	3 V	2	
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V		V
		I _{OL} = 4 mA	1.65 V	0.45	
		I _{OL} = 6 mA	2.3 V	0.4	
		I _{OL} = 12 mA	2.3 V	0.7	
			2.7 V	0.4	
		I _{OL} = 24 mA	3 V	0.55	
I _I		V _I = V _{CC} or GND	3.6 V		µA
I _{BHL} ⁽²⁾		V _I = 0.57 V	1.65 V	25	µA
		V _I = 0.7 V	2.3 V	45	
		V _I = 0.8 V	3 V	75	
I _{BHH} ⁽³⁾		V _I = 1.07 V	1.65 V	-25	µA
		V _I = 1.7 V	2.3 V	-45	
		V _I = 2 V	3 V	-75	
I _{BHLO} ⁽⁴⁾		V _I = 0 to V _{CC}	1.95 V	200	µA
			2.7 V	300	
			3.6 V	500	
I _{BHHO} ⁽⁵⁾		V _I = 0 to V _{CC}	1.95 V	-200	µA
			2.7 V	-300	
			3.6 V	-500	
I _{OZ} ⁽⁶⁾		V _O = V _{CC} or GND	3.6 V		µA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V	30	µA
ΔI _{CC}		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	750	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	3	pF
	D			4	
C _{io}	A ports	V _O = V _{CC} or GND	3.3 V	4.5	pF
	B ports			4.5	
C _O	Q	V _O = V _{CC} or GND	3.3 V	3	pF

- (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
- (2) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
- (3) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
- (4) An external driver must source at least I_{BHLO} to switch this node from low to high.
- (5) An external driver must sink at least I_{BHHO} to switch this node from high to low.
- (6) For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCH16973

8-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH FOUR INDEPENDENT BUFFERS

SCES435B–APRIL 2003–REVISED SEPTEMBER 2004

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	2		2		2		ns
t_{su}	Setup time, data before LE↓	0.9		0.9		0.9		ns
t_h	Hold time, data after LE↓	0.9		0.9		0.9		ns

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	
t_{pd}	D	Y	2.2	0.5	3.2	0.5	3	ns
	A	Q	2.2	0.5	3.2	0.5	3	
	LE		2.8	0.5	3.3	0.5	3	
	A or B	B or A	2.2	0.5	3.2	0.5	3	
t_{en}	\overline{LOE}	Q	2.9	0.7	4.9	0.7	4.7	ns
	\overline{TOE}	A or B	3	0.7	4.6	0.7	4.4	
	DIR		3.4	0.7	4.9	0.7	4.7	
t_{dis}	\overline{LOE}	Q	2.8	0.5	4.3	0.5	4.1	ns
	\overline{TOE}	A or B	3.2	0.5	4.3	0.5	4.1	
	DIR		3.4	0.5	4.9	0.5	4.7	

OPERATING CHARACTERISTICS⁽¹⁾

$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	
$C_{pd}^{(2)}$ (each output)	Power dissipation capacitance	A outputs enabled, Q outputs disabled, One A output switching	One $f_A = 10\text{ MHz}$, One $f_B = 10\text{ MHz}$, $\overline{TOE} = \text{GND}$, $\overline{LOE} = V_{CC}$, $\text{DIR} = \text{GND}$, $C_L = 0\text{ pF}$	12	14	19	pF
		B outputs enabled, Q outputs disabled, One B output switching	One $f_A = 10\text{ MHz}$, One $f_B = 10\text{ MHz}$, $\overline{TOE} = \text{GND}$, $\overline{LOE} = V_{CC}$, $\text{DIR} = \text{GND}$, $C_L = 0\text{ pF}$	12	14	21	
		Q outputs enabled, A and B I/Os isolated, One Q output switching	One $f_A = 10\text{ MHz}$, One $f_{LE} = 20\text{ MHz}$, One $f_Q = 10\text{ MHz}$, $\overline{TOE} = V_{CC}$, $\overline{LOE} = \text{GND}$, $C_L = 0\text{ pF}$	11	13	19	
		One Y output switching, A and B I/Os isolated, Q outputs disabled	One $f_D = 10\text{ MHz}$, One $f_Y = 10\text{ MHz}$, $\overline{TOE} = V_{CC}$, $\overline{LOE} = V_{CC}$, $C_L = 0\text{ pF}$	7	8	12	
$C_{pd}^{(2)}$	Power dissipation capacitance	A and B I/Os isolated, Q outputs disabled, One LE and one A data input switching	One $f_A = 10\text{ MHz}$, One $f_{LE} = 20\text{ MHz}$, f_Q not switching, $\overline{TOE} = V_{CC}$, $\overline{LOE} = V_{CC}$, $C_L = 0\text{ pF}$	4	5	11	pF
$C_{pd}^{(3)}$ (each LE)	Power dissipation capacitance	A and B I/Os isolated, Q outputs disabled, One LE input switching	f_A not switching, One $f_{LE} = 20\text{ MHz}$, f_Q not switching, $\overline{TOE} = V_{CC}$, $\overline{LOE} = V_{CC}$, $C_L = 0\text{ pF}$	6	7	9	pF

- (1) Total device C_{pd} for multiple (m) outputs switching and (n) LE inputs switching = $[m * C_{pd} \text{ (each output)}] + [n * C_{pd} \text{ (each LE)}]$.
 (2) C_{pd} (each output) is the C_{pd} for each data bit (input and output circuitry) when it operates at 10 MHz (Note: the LE is operating at 20 MHz in this test, but its I_{CC} component has been subtracted).
 (3) C_{pd} (each LE) is the C_{pd} for the clock circuitry only when it operates at 20 MHz.

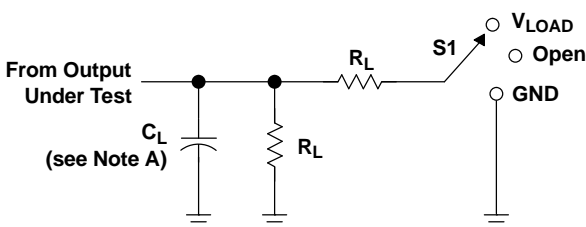
SN74ALVCH16973

8-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH

WITH FOUR INDEPENDENT BUFFERS

SCES435B–APRIL 2003–REVISED SEPTEMBER 2004

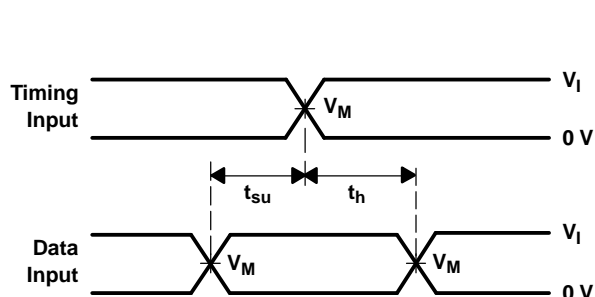
PARAMETER MEASUREMENT INFORMATION



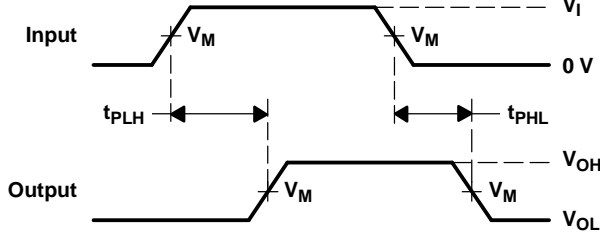
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

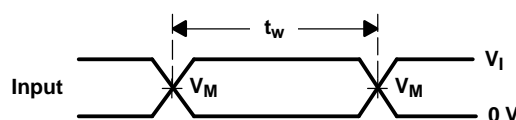
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
1.8 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



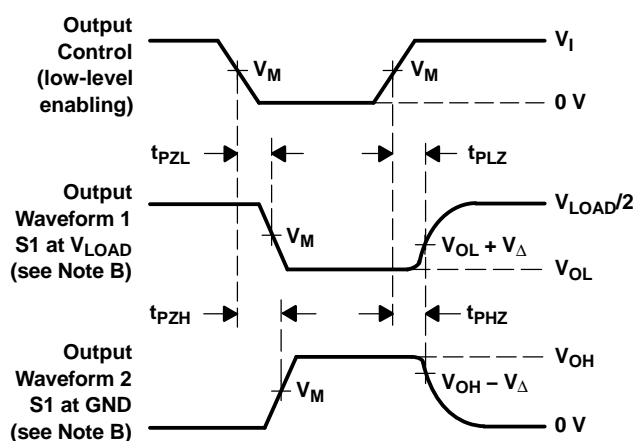
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALVCH16973DGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16973
SN74ALVCH16973DGGR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16973

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

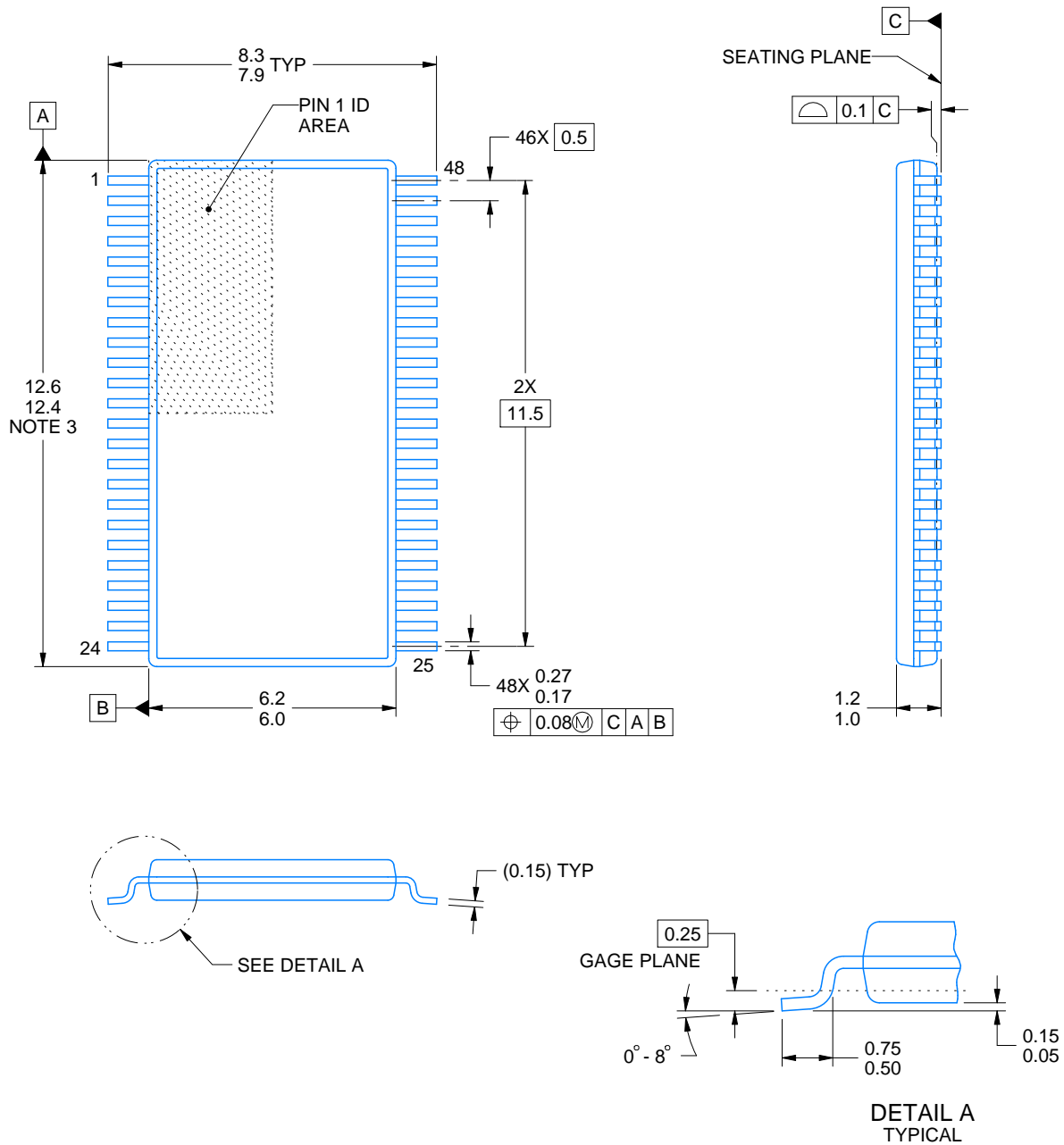
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16973DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16973DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0



4214859/B 11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

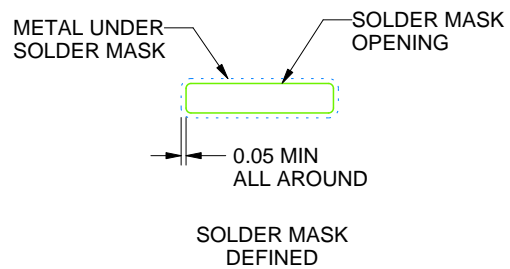
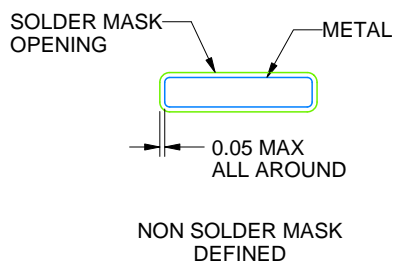
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

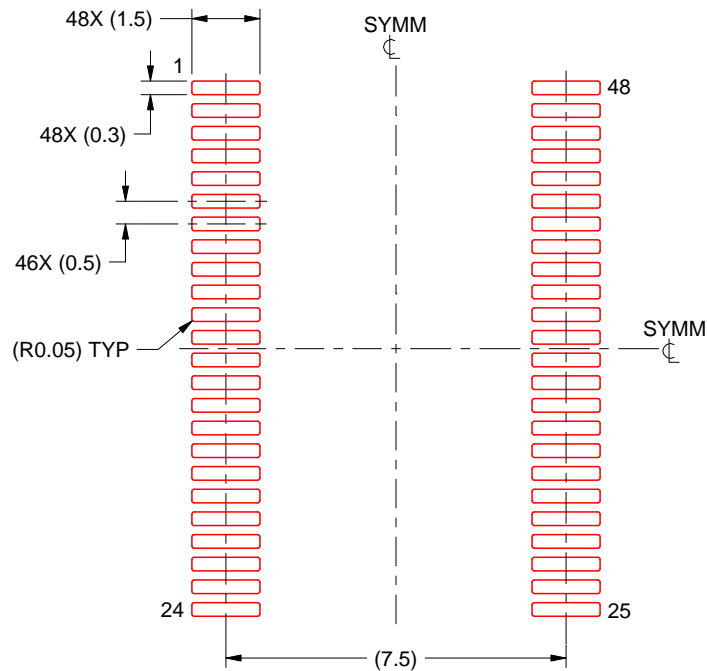
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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