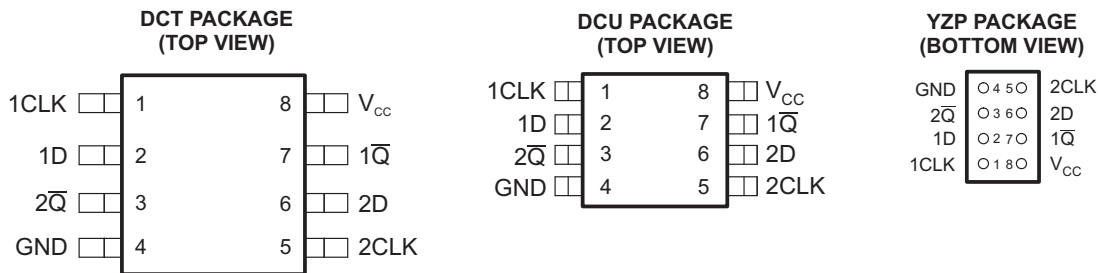


## FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max  $t_{pd}$  of 1.9 ns at 1.8 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 8$ -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

## DESCRIPTION/ORDERING INFORMATION

This dual positive-edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the  $\bar{Q}$  output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
-40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G80YZPR	___UX_
	SSOP – DCT	Reel of 3000	SN74AUC2G80DCTR	U80___
	VSSOP – DCU	Reel of 3000	SN74AUC2G80DCUR	UX_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.  
DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



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NanoFree is a trademark of Texas Instruments.

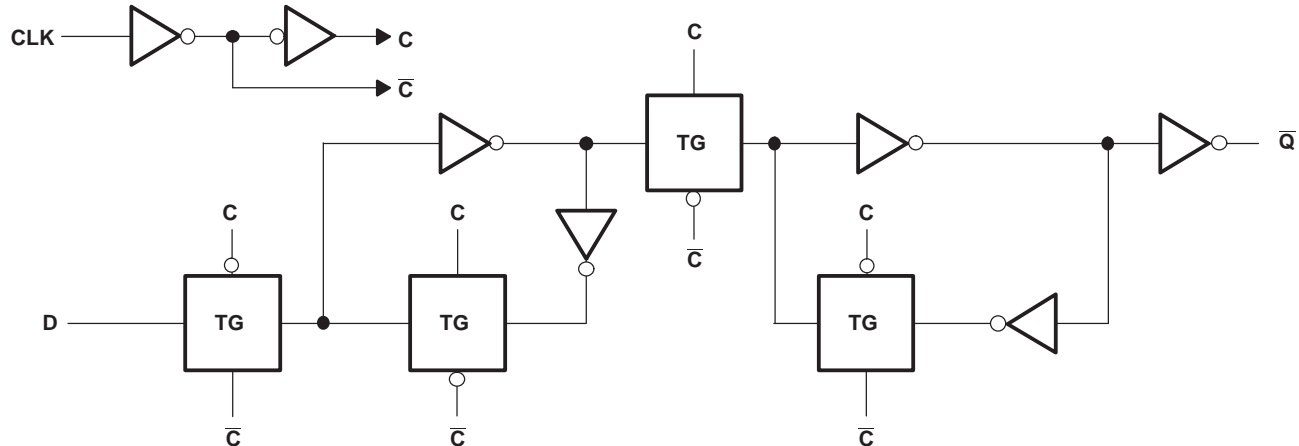
# SN74AUC2G80 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES540C—JANUARY 2004—REVISED JANUARY 2007

**FUNCTION TABLE  
(EACH FLIP-FLOP)**

INPUTS		OUTPUT Q
CLK	D	
↑	H	L
↑	L	H
L	X	Q <sub>0</sub>

**LOGIC DIAGRAM (POSITIVE LOGIC)**



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range	-0.5	3.6	V	
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	3.6	V	
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	3.6	V	
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current			±20	mA
Continuous current through V <sub>CC</sub> or GND				±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>	DCT package		220	°C/W
		DCU package		227	
		YZP package		102	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	0.8	2.7	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.1 V to 1.95 V	0.65 × V <sub>CC</sub>	
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 0.8 V	0	V
		V <sub>CC</sub> = 1.1 V to 1.95 V	0.35 × V <sub>CC</sub>	
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
V <sub>I</sub>	Input voltage	0	3.6	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 0.8 V	-0.7	mA
		V <sub>CC</sub> = 1.1 V	-3	
		V <sub>CC</sub> = 1.4 V	-5	
		V <sub>CC</sub> = 1.65 V	-8	
		V <sub>CC</sub> = 2.3 V	-9	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 0.8 V	0.7	mA
		V <sub>CC</sub> = 1.1 V	3	
		V <sub>CC</sub> = 1.4 V	5	
		V <sub>CC</sub> = 1.65 V	8	
		V <sub>CC</sub> = 2.3 V	9	
Δt/Δv	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	0.8 V to 2.7 V	V <sub>CC</sub> - 0.1		V	
	I <sub>OH</sub> = -0.7 mA	0.8 V	0.55			
	I <sub>OH</sub> = -3 mA	1.1 V	0.8			
	I <sub>OH</sub> = -5 mA	1.4 V	1			
	I <sub>OH</sub> = -8 mA	1.65 V	1.2			
	I <sub>OH</sub> = -9 mA	2.3 V	1.8			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	0.8 V to 2.7 V	0.2		V	
	I <sub>OL</sub> = 0.7 mA	0.8 V	0.25			
	I <sub>OL</sub> = 3 mA	1.1 V	0.3			
	I <sub>OL</sub> = 5 mA	1.4 V	0.4			
	I <sub>OL</sub> = 8 mA	1.65 V	0.45			
	I <sub>OL</sub> = 9 mA	2.3 V	0.6			
I <sub>I</sub>	D or CLK inputs V <sub>I</sub> = V <sub>CC</sub> or GND	0 to 2.7 V	±5		μA	
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 2.7 V	0	±5		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	0.8 V to 2.7 V	10		μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V	2.5		pF	

(1) All typical values are at T<sub>A</sub> = 25°C.

# SN74AUC2G80

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES540C—JANUARY 2004—REVISED JANUARY 2007

### Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

		$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	UNIT
		TYP	MIN MAX	MIN MAX	MIN MAX	MIN MAX	
$f_{\text{clock}}$	Clock frequency	50	200	225	250	275	MHz
$t_w$	Pulse duration, CLK high or low	2.4	1	1	1	1	ns
$t_{\text{su}}$	Setup time before CLK $\uparrow$	1	0.8	0.6	0.6	0.5	ns
$t_h$	Hold time, data after CLK $\uparrow$	0	0	0.1	0.1	0.5	ns

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 15\text{ pF}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	UNIT
			TYP	MIN MAX	MIN MAX	MIN TYP MAX	MIN MAX	
$f_{\text{max}}$			50	200	225	250	275	MHz
$t_{\text{pd}}$	CLK	$\bar{Q}$	5	1 3.9	0.8 2.5	0.3 1 1.9	0.3 1.3	ns

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 30\text{ pF}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
$f_{\text{max}}$			250			275		ns
$t_{\text{pd}}$	CLK	$\bar{Q}$	0.8	1.5	2.4	0.6	1.8	ns

### Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$	$V_{CC} = 1.5\text{ V}$	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	TYP	
$C_{\text{pd}}$	Data	$f_{\text{clock}} = 10\text{ MHz}$	16.9	17.2	18.6	21.4	29.5	pF
	CLK		1.1	1.1	1.2	1.4	2.5	
	Total		18	18.3	19.8	22.8	32	

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PZL}/t_{PZH}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$C_L$	$R_L$	$V_A$
0.8 V	15 pF	2 k $\Omega$	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k $\Omega$	0.15 V
1.8 V $\pm$ 0.15 V	30 pF	1 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 $\Omega$	0.15 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o = 50 \Omega$ , slew rate  $\geq$  1 V/ns.  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74AUC2G80DCTR</a>	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(2XE5, U80) (R, Z)
SN74AUC2G80DCTR.B	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2XE5, U80) (R, Z)
<a href="#">SN74AUC2G80DCUR</a>	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(U80Q, U80R)
SN74AUC2G80DCUR.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(U80Q, U80R)

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G80DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUC2G80DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74AUC2G80DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G80DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3

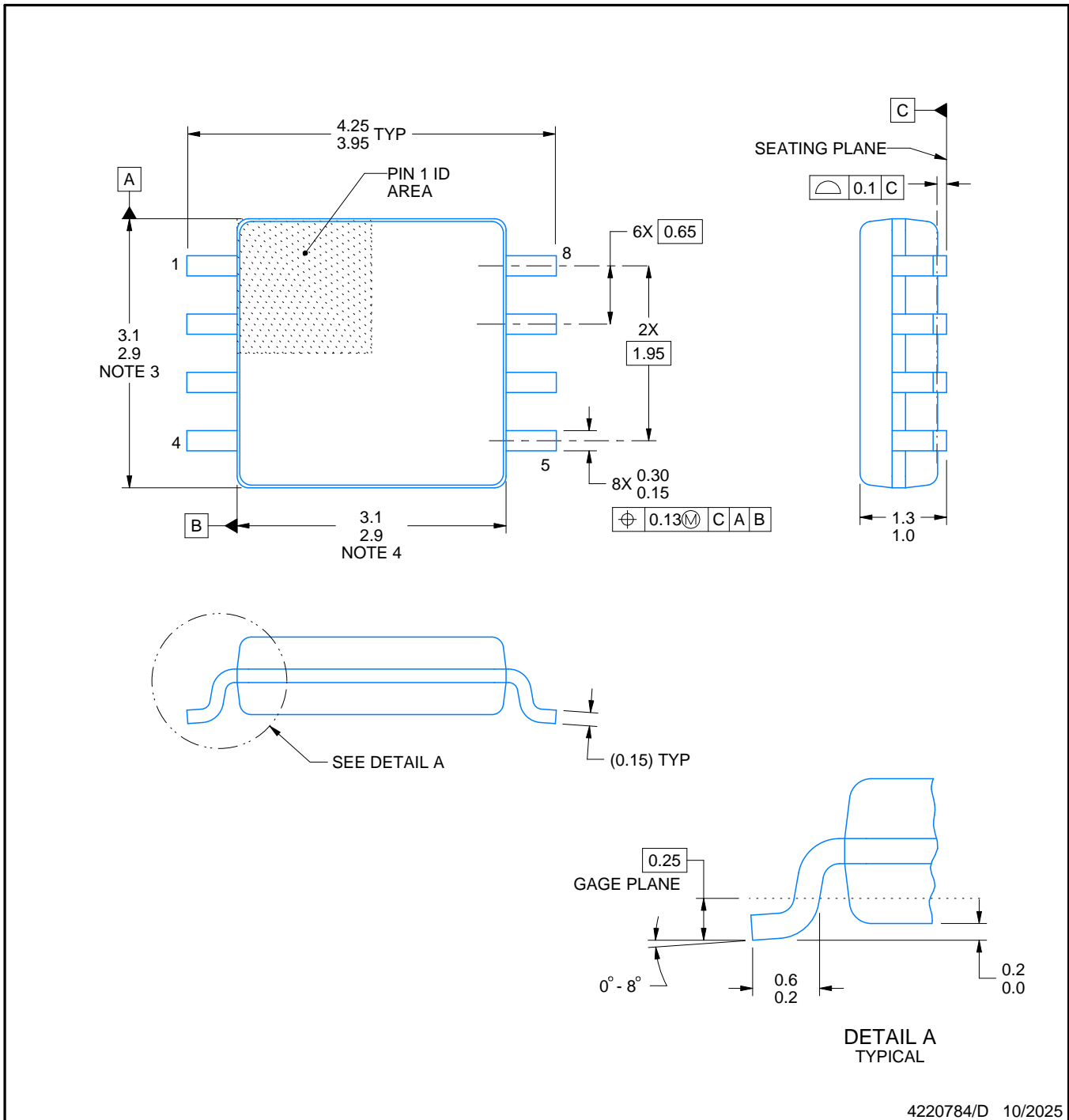
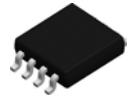
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G80DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74AUC2G80DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74AUC2G80DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G80DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0





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NOTES:

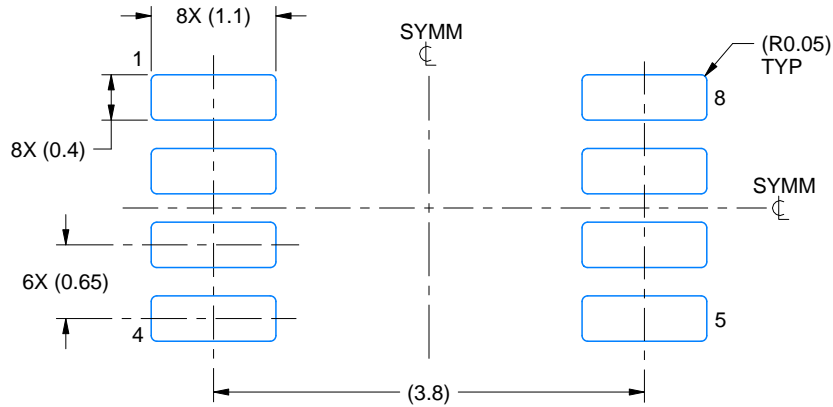
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

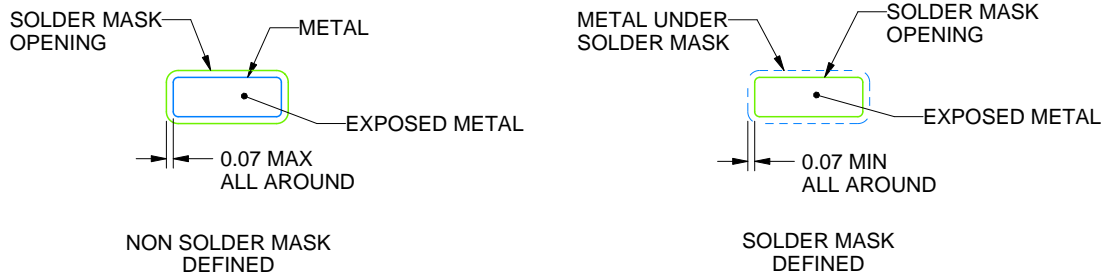
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

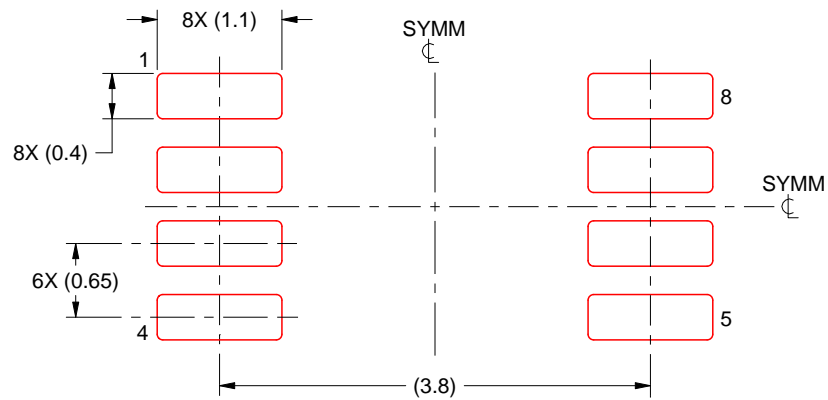
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

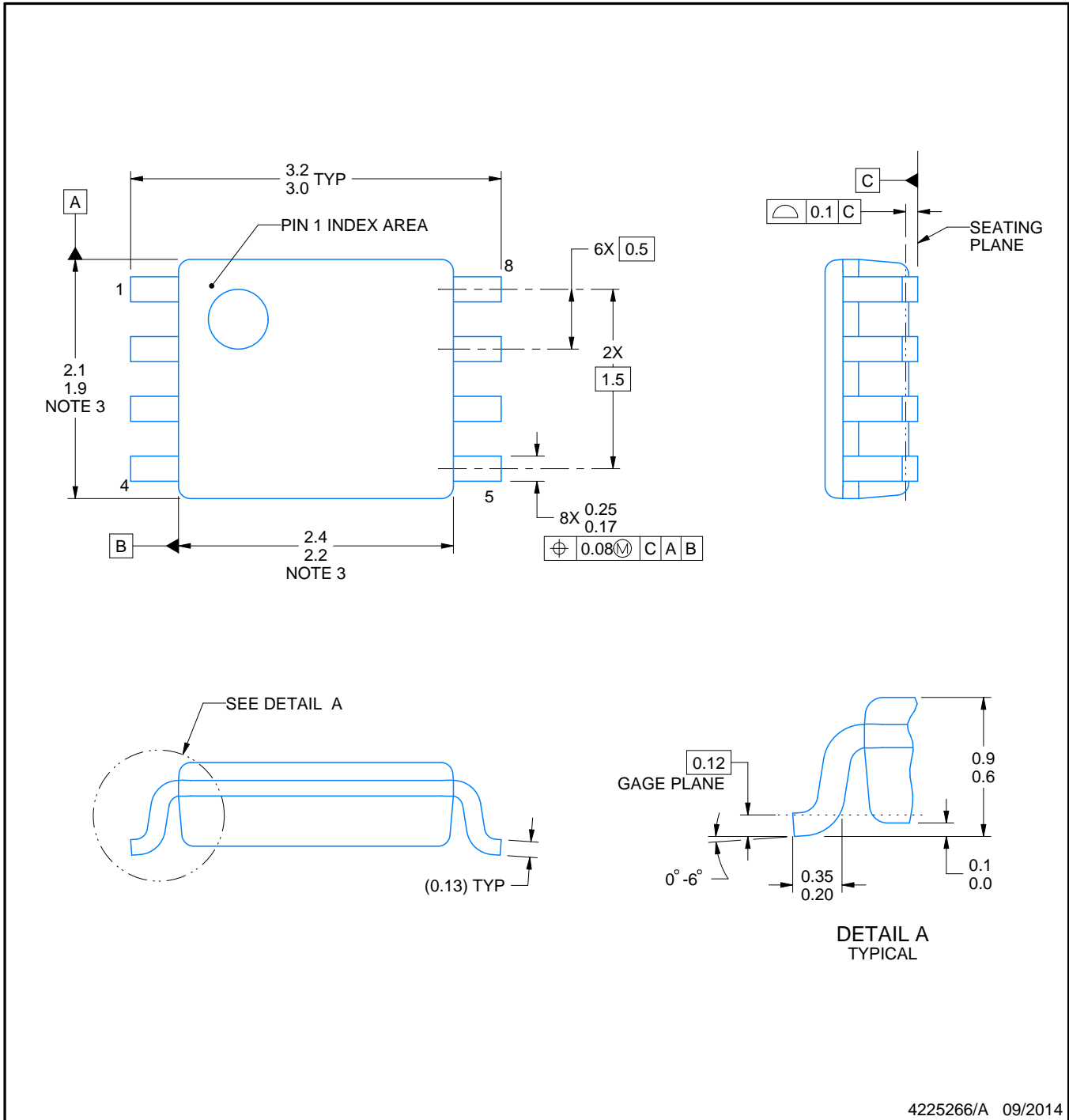
# DCU0008A



# PACKAGE OUTLINE

## VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



4225266/A 09/2014

### NOTES:

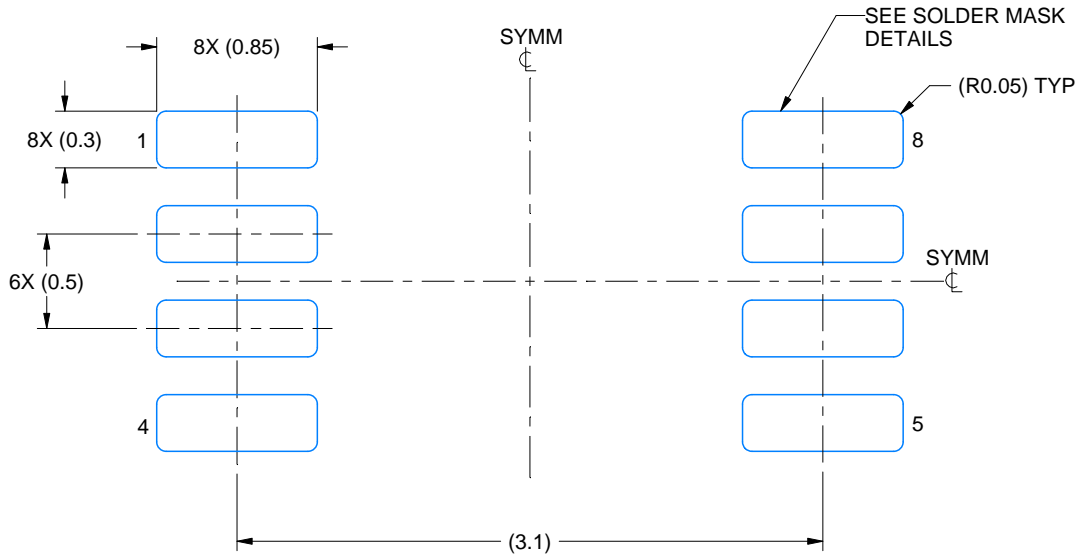
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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