SN74AUP1T34 1-Bit Unidirectional Voltage-Level Translator

1 Features

- Wide Operating VCC Range of 0.9 V to 3.6 V
- Balanced Propagation Delays: $t_{PLH} = t_{PHL}$ (1.8-V to 3.3-V Translation Typical)
- Low Static-Power Consumption: Maximum of 5-µA ICC
- ±6-mA Output Drive at 3 V
- I_{off} Supports Partial Power-Down-Mode Operation
- VCC Isolation Feature – If V_{CCA} Input Is at GND, B Port Is in the High-Impedance state
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input
- ESD Protection Exceeds JESD 22
- 5000-V Human-Body Model (A114-A)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

2 Applications

- Enterprise
- Industrial
- Personal Electronics
- Telecommunications

3 Description

The SN74AUP1T34 device is a 1-bit noninverting translator that uses two separate configurable power-supply rails. It is a uni-directional translator from A to B. The A port is designed to track V_{CCA}. V_{CCA} accepts supply voltages from 0.9 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts supply voltages from 0.9 V to 3.6 V. This allows for low-voltage translation between 1-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes. The SN74AUP1T34 is also fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

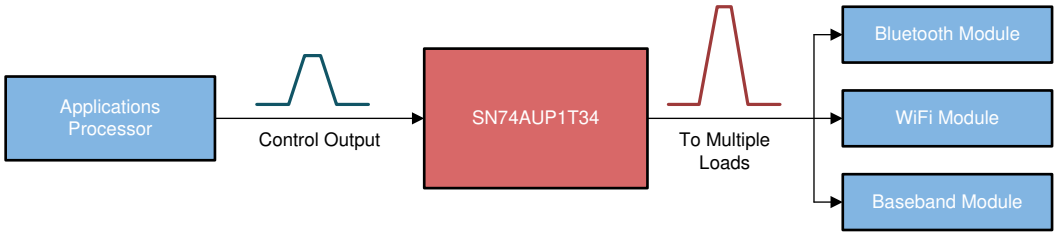
The VCC isolation feature ensures that if V_{CCA} input is at GND, the B port is in the high-impedance state. If V_{CCB} input is at GND, any input to the A side does not cause the leakage current even floating.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1T34DCK	SC70 (5)	2.00 mm × 1.25 mm
SN74AUP1T34DRY	SON (6)	1.45 mm × 1.00 mm
SN74AUP1T34DSF	SON (6)	1.00 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Example Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2016) to Revision F — **Page**

- Added operating junction temperature to *Absolute Maximum Ratings* table ... 5
- Updated *Recommended Operating Conditions* table ... 6
- Updated the V_{CCB} value for the parameter 'high-level input voltage' in the *Recommended Operating Conditions* table ... 6
- Updated the V_{CCB} value for the parameter 'low-level input voltage' in the *Recommended Operating Conditions* table ... 6
- Added *Electrical Characteristics: DC* table ... 7

Changes from Revision D (April 2016) to Revision E — **Page**

- Changed pin A number From: 3 To: 2 and GND From: 2 To: 3 for the SC70 package in the *Pin Configuration and Functions* section ... 4

Changes from Revision C (May 2013) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Removed *Ordering Information* table ... 1

Changes from Revision B (July 2012) to Revision C — **Page**

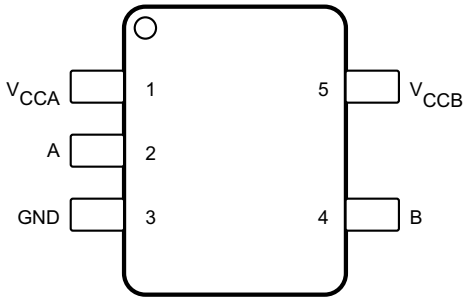
- Added Feature: VCC Isolation Feature – If V_{CCA} Input Is at GND, B Port Is in the High-Impedance state. ... 1
- Updated *Pin Functions* table. ... 4
- Deleted I_{OZ} PARAMETER from RECOMMENDED OPERATION CONDITIONS. ... 6
- Added V_{MI} and V_{MO} equations to Wavefrom 1 graphic. ... 10
- Added FUNCTION TABLE. ... 12

Changes from Revision A (June 2012) to Revision B **Page**

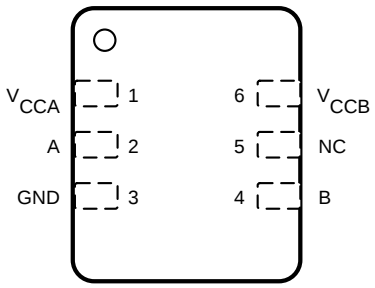
- Removed Feature: Output Enable Feature Allows User to Disable Outputs to Reduce Power Consumption. 1

5 Pin Configuration and Functions

DCK Package
5-Pin SC70
Top View



DRY or DSF Package
6-Pin SON
Top Through View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SC70	SON		
A	2	2	I	Input Port
B	4	4	O	Output Port
GND	3	3	—	Ground
V_{CCA}	1	1	—	Input Port DC Power Supply
V_{CCB}	5	6	—	Output Port DC Power Supply
NC	—	5	—	No Connect. Leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{CCA} and V_{CCB}		–0.3	4	V
Input voltage, V_I		–0.5	4.6	V
		–0.5	4.6	
		–0.5	4.6	
Voltage applied to any output in the high-impedance or power-off state, V_O		–0.5	4.6	V
		–0.5	4.6	
Voltage applied to any output in the high or low state, V_O		–0.5	4.6	V
		–0.5	4.6	
Input clamp current, I_{IK}	V_I < 0 V		–50	mA
Output clamp current, I_{OK}	V_O < 0 V		–50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CCA} or GND			±100	mA
Storage temperature, T_{stg}		–65	150	°C
Operating junction temperature, T_J			150	°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	5000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_{CCA}	Supply voltage			0.9		3.6	V
V_{CCB}	Supply voltage			0.9		3.6	V
V_{IH}	High-level input voltage	V_{CCA} = 0.9 V to 1.95 V	V_{CCB} = 0.9 V to 3.6 V	0.65 × V_{CCA}			V
		V_{CCA} = 2.3 V to 2.7 V	V_{CCB} = 0.9 V to 3.6 V	1.6			
		V_{CCA} = 3 V to 3.6 V	V_{CCB} = 0.9 V to 3.6 V	2			
V_{IH}	Low-level input voltage	V_{CCA} = 0.9 V	V_{CCB} = 0.9 V to 3.6 V			0.3 × V_{CCA}	V
		V_{CCA} = 1 V to 1.95 V	V_{CCB} = 0.9 V to 3.6 V			0.35 × V_{CCA}	
		V_{CCA} = 2.3 V to 2.7 V	V_{CCB} = 0.9 V to 3.6 V			0.7	
		V_{CCA} = 3 V to 3.6 V	V_{CCB} = 0.9 V to 3.6 V			0.9	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CCA} = 3 V to 3.6 V	V_{CCB} = 0.9 V to 3.6 V			200	ns/V
T_A	Operating free-air temperature			–40		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74AUP1T34			UNIT
		DCK (SC70)	DRY (SON)	DSF (SON)	
		5 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	300.8	338.5	367.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	141.3	240.4	188.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.3	224.6	274.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.6	86.8	24.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.5	221.4	273.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: DC

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = –100 µA	0.9 V to 3.6 V	0.9 V to 3.6 V	V_{CCB} – 0.2		V
			I_{OH} = –0.25 mA	0.9 V to 1 V	0.9 V to 1 V	0.75 × V_{CCB}		
			I_{OH} = –1.5 mA	1.2 V	1.2 V	1		
			I_{OH} = –2 mA	1.65 V	1.65 V	1.32		
			I_{OH} = –3 mA	2.3 V	2.3 V	1.9		
			I_{OH} = –6 mA	3 V	3 V	2.72		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	0.9 V to 3.6 V	0.9 V to 3.6 V		0.1	V
			I_{OL} = 0.25 mA	0.9 V to 1 V	0.9 V to 1 V		0.1	
			I_{OL} = 1.5 mA	1.2 V	1.2 V		0.3 × V_{CCB}	
			I_{OL} = 2 mA	1.65 V	1.65 V		0.31	
			I_{OL} = 3 mA	2.3 V	2.3 V		0.31	
			I_{OL} = 6 mA	3 V	3 V		0.31	
I_I	Input leakage current	V_I = VCCA or GND		0.9 V to 3.6 V	0.9 V to 3.6 V		±1	µA
I_{off}	Off-state current	A or B port: V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V		±5	µA
				0 V to 3.6 V	0 V		±5	
I_{CCA}	V_{CCA} supply current	V_I = VCCI or GND, I_O = 0 mA		0.9 V to 3.6 V	0.9 V to 3.6 V		5	µA
				0.9 V to 3.6 V	V_{CCA}		2	
				0 V	0 V to 3.6 V		1	
				0 V to 3.6 V	0 V		1	
I_{CCB}	V_{CCB} supply current	V_I = VCCI or GND, I_O = 0 mA		0.9 V to 3.6 V	0.9 V to 3.6 V		5	µA
				0.9 V to 3.6 V	V_{CCA}		2	
				0 V	0 V to 3.6 V		1	
				0 V to 3.6 V	0 V		1	
I_{CCA} + I_{CCB}	Combined supply current	V_I = VCCI or GND, I_O = 0 mA		0.9 V to 3.6 V	0.9 V to 3.6 V		5.2	µA
C_I	Input capacitance	V_I = 3.3 V or GND		3.3 V	3.3 V		4	pF
$C_{I/O}$	Input-to-output internal capacitance	A or B port: V_O = 3.3 V or GND		0 V	3.3 V		7	pF

6.6 Electrical Characteristics: AC

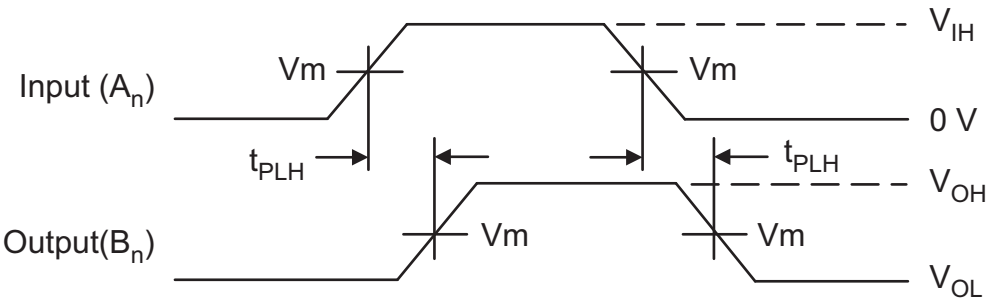
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}/t_{PHL}	Propagation delay time low-to-high output / high-to-low output	C_L = 5 pF	0.9 V	0.9 V		25		ns
				1.2 V		18		
				1.65 V		16.2		
				2.3 V		16.3		
				3 V		16.8		
		C_L = 5 pF	1.2 V	0.9 V			42.5	
				1.2 V			24.9	
				1.65 V			23.2	
				2.3 V			22.6	
				3 V			22.5	
		C_L = 5 pF	1.65 V	0.9 V			40	
				1.2 V			10.7	
				1.65 V			8.84	
				2.3 V			8.08	
				3 V			7.88	
		C_L = 5 pF	2.3 V	0.9 V			41.3	
				1.2 V			8.02	
				1.65 V			5.73	
				2.3 V			4.92	
				3 V			4.2	
		C_L = 5 pF	3 V	0.9 V			42.5	
				1.2 V			7.61	
				1.65 V			4.5	
				2.3 V			3.65	
				3 V			3.39	
t_{PLH}/t_{PHL}	Propagation delay time low-to-high output / high-to-low output	C_L = 10 pF	0.9 V	0.9 V		28.9		ns
				1.2 V		19.8		
				1.65 V		17.9		
				2.3 V		18		
				3 V		18.5		
		C_L = 10 pF	1.2 V	0.9 V			43.22	
				1.2 V			12.33	
				1.65 V			9.57	
				2.3 V			8.81	
				3 V			8.61	
		C_L = 10 pF	1.65 V	0.9 V			40.44	
				1.2 V			9.21	
				1.65 V			6.57	
				2.3 V			5.5	
				3 V			4.73	
		C_L = 10 pF	2.3 V	0.9 V			41.56	
				1.2 V			8.3	
				1.65 V			5.54	
				2.3 V			4.42	
				3 V			4.01	
		C_L = 10 pF	3 V	0.9 V			42.81	
				1.2 V			7.87	
				1.65 V			4.55	
				2.3 V			3.8	
				3 V			3.36	

Electrical Characteristics: AC (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}/t_{PHL}	Propagation delay time low-to-high output / high-to-low output	C_L = 15 pF	0.9 V	0.9 V		30.6		ns
				1.2 V		21.6		
				1.65 V		19.6		
				2.3 V		19.7		
				3 V		20.3		
		C_L = 15 pF	1.2 V	0.9 V			43.87	
				1.2 V			12.98	
				1.65 V			10.3	
				2.3 V			9.54	
				3 V			9.34	
		C_L = 15 pF	1.65 V	0.9 V			40.78	
				1.2 V			9.59	
				1.65 V			6.95	
				2.3 V			5.87	
				3 V			5.07	
		C_L = 15 pF	2.3 V	0.9 V			41.79	
				1.2 V			8.55	
				1.65 V			5.8	
				2.3 V			4.68	
				3 V			4.27	
		C_L = 15 pF	3 V	0.9 V			43.09	
				1.2 V			8.16	
				1.65 V			4.84	
				2.3 V			4.09	
				3 V			3.65	
t_{PLH}/t_{PHL}	Propagation delay time low-to-high output / high-to-low output	C_L = 30 pF	0.9 V	0.9 V		32.1		ns
				1.2 V		21.3		
				1.65 V		18.7		
				2.3 V		18		
				3 V		18.3		
		C_L = 30 pF	1.2 V	0.9 V			45.65	
				1.2 V			14.76	
				1.65 V			12.37	
				2.3 V			11.61	
				3 V			11.41	
		C_L = 30 pF	1.65 V	0.9 V			41.72	
				1.2 V			10.65	
				1.65 V			8.01	
				2.3 V			6.94	
				3 V			5.99	
		C_L = 30 pF	2.3 V	0.9 V			42.44	
				1.2 V			9.26	
				1.65 V			6.51	
				2.3 V			5.39	
				3 V			4.97	
		C_L = 30 pF	3 V	0.9 V			43.69	
				1.2 V			8.8	
				1.65 V			5.48	
				2.3 V			4.72	
				3 V			4.28	



V_{MI} =V_{IH}/2; V_{MO}= V_{CCB}/2

t_R = t_F = 2.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

Figure 1. Waveform 1 – Propagation Delays

6.7 Typical Characteristics

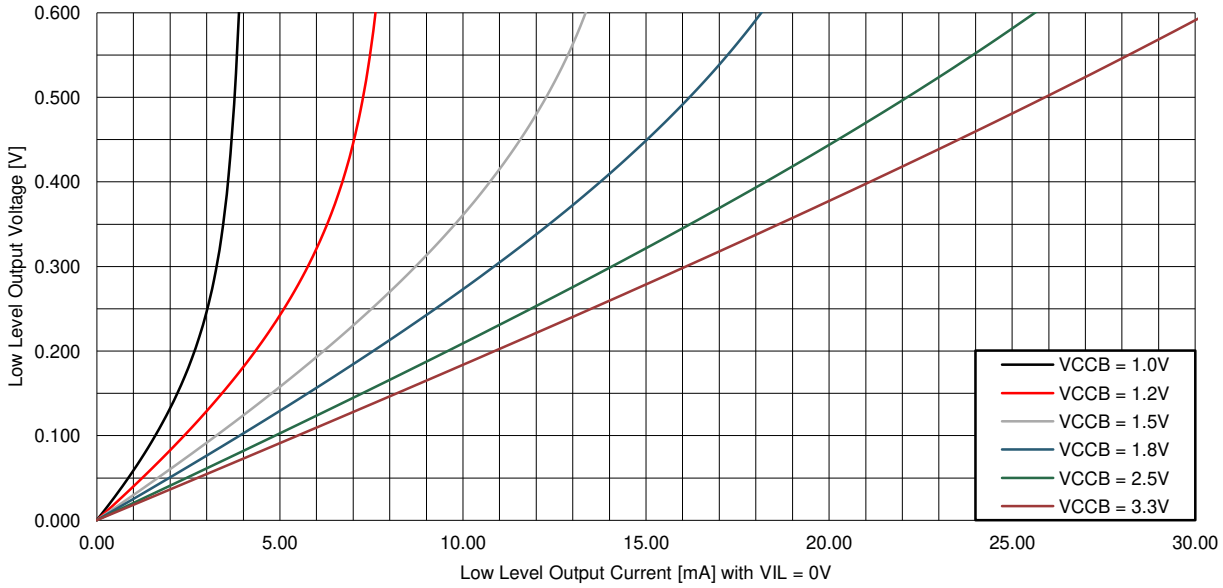
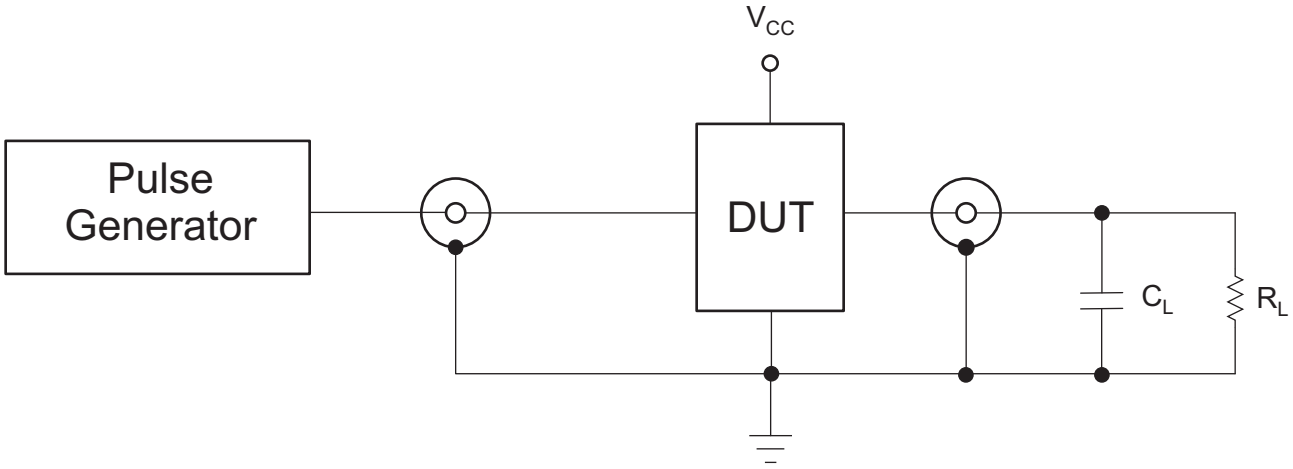


Figure 2. Low Level Output Voltage vs Low Level Output Current

7 Parameter Measurement Information



TEST

t_{PLH}, t_{PHL}

C_L = 5 pF, 10 pF, 15 pF, 30 pF or equivalent (includes probe and jig capacitance)

R_L = 1 MΩ or equivalent

Z_{OUT} of pulse generator = 50 Ω

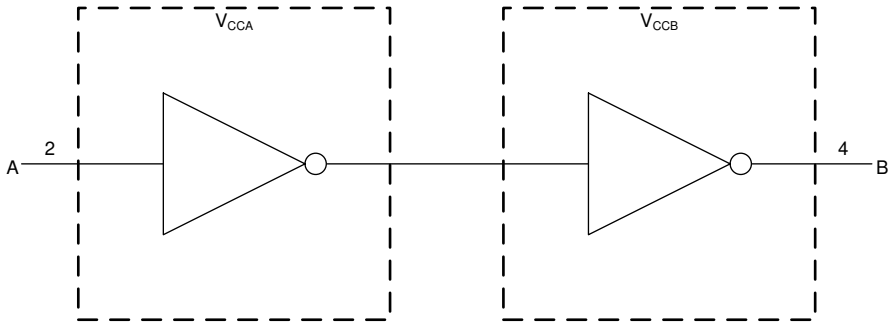
Figure 3. AC (Propagation Delay) Test Circuit

8 Detailed Description

8.1 Overview

The SN74AUP1T34 is a unidirectional, single-bit, dual-supply, noninverting voltage-level translator. Pin A, which is referenced to V_{CCA}, receives the signal that is to be level translated. Pin B, which is referenced to V_{CCB}, transmits the level translated signal. Both supply pins V_{CCA} and V_{CCB} support a voltage range from 0.9 V to 3.6 V.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design

Both V_{CCA} and V_{CCB} can be supplied at any voltage from 0.9 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (1 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

8.3.2 Partial-Power-Down Mode Operation

I_{off} circuitry disables the outputs, preventing damaging current backflow through the SN74AUP1T34 when it is powered down. This can occur in applications where subsections of a system are powered down (partial-power-down) to reduce power consumption.

8.3.3 V_{CC} Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND (or < 0.4 V), both ports A and B are set to a high-impedance state, preventing false logic levels from being presented to either bus.

8.3.4 Input Hysteresis

Input hysteresis allows the input to support slew rates as slow as 200 ns/V, improving switching noise immunity.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74AUP1T34.

Table 1. Function Table

INPUT	OUTPUT
A PORT	**B PORT**
L	L
H	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AUP1T34 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

9.2 Typical Application

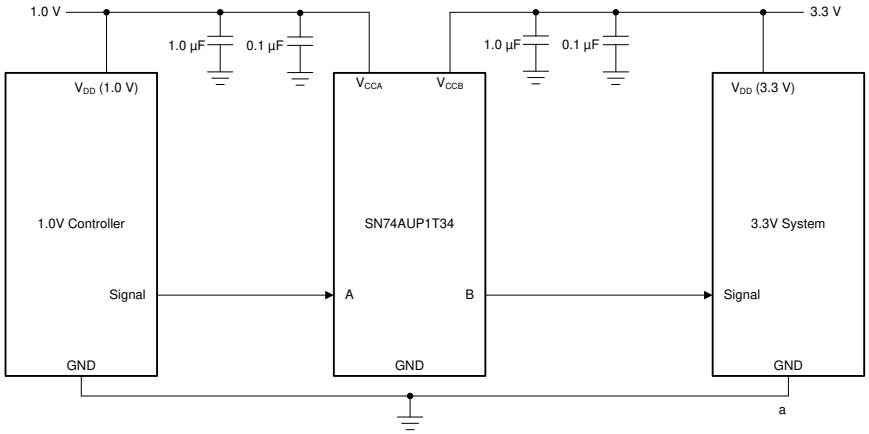


Figure 4. Typical Application Example

9.2.1 Design Requirements

Table 2 lists the design requirements of the SN74AUP1T34.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0.9 V to 3.6 V
Output Voltage Range	0.9 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AUP1T34 device to determine the input voltage range. For a valid logic-high, the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AUP1T34 device is driving to determine the output voltage range.

9.2.3 Application Curve

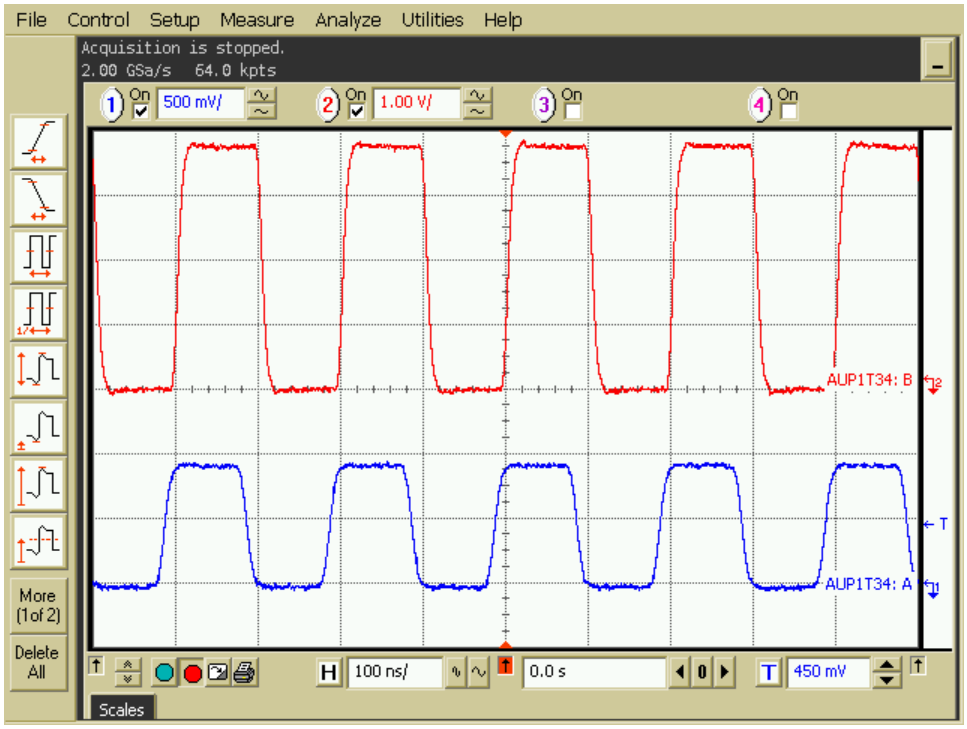


Figure 5. 10-MHz Up Translation (0.9 V to 3.6 V)

10 Power Supply Recommendations

Connect ground before applying either V_{CCA} or V_{CCB}. There is no specific power sequence requirement for the SN74AUP1T34. V_{CCA} or V_{CCB} may be powered up first, and V_{CCA} or V_{CCB} may be powered down first.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, TI recommends following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors must be used on power supplies.
- Short trace lengths must be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors helps adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

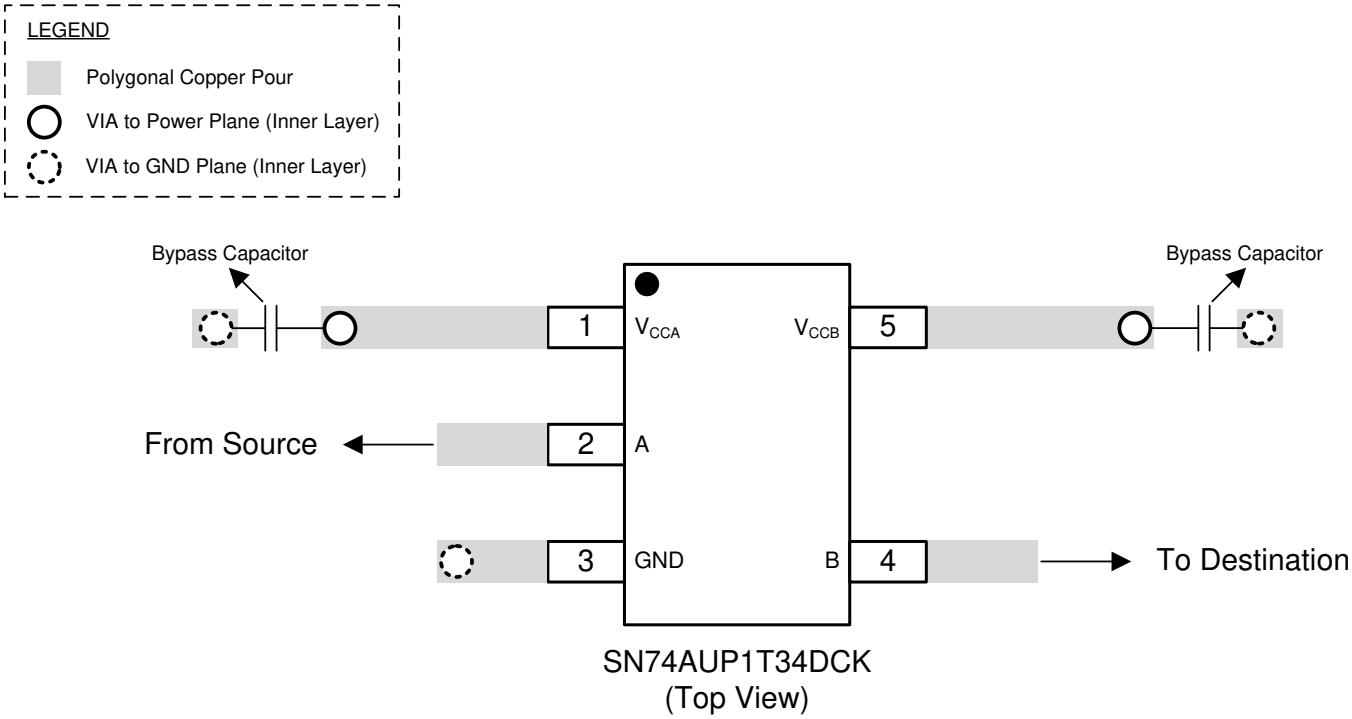


Figure 6. Example Layout

12 Device and Documentation Support

12.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
SN74AUP1T34DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	U2Q, U2E
SN74AUP1T34DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	U2
SN74AUP1T34DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	U2

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

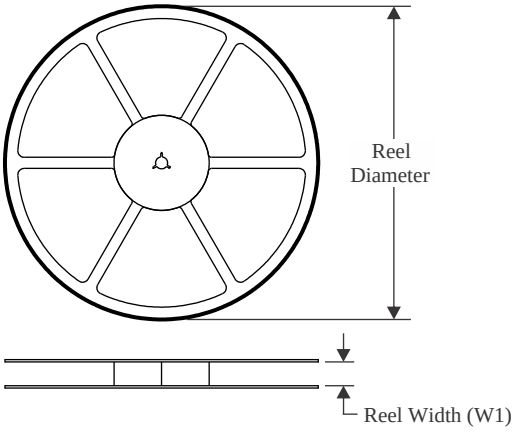
(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

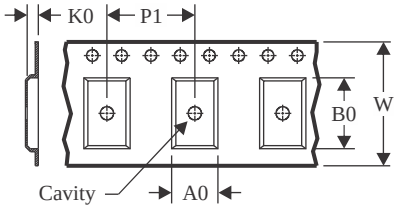
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

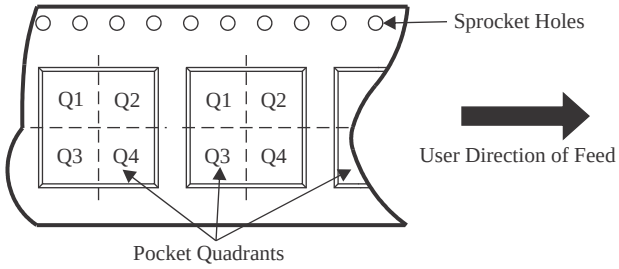


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

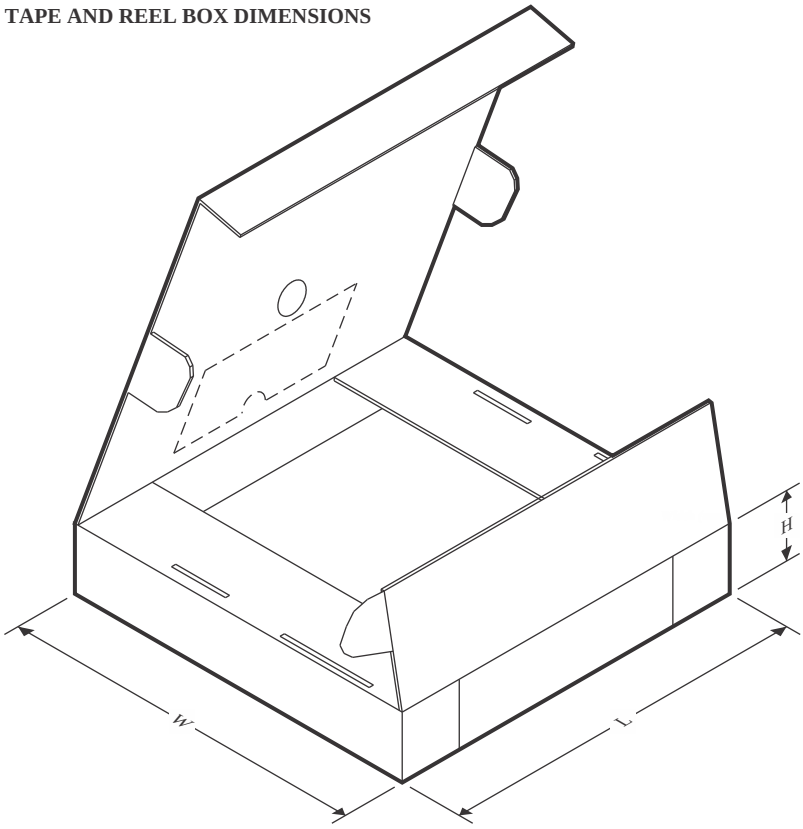
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T34DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AUP1T34DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1T34DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

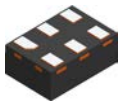
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T34DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AUP1T34DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1T34DSFR	SON	DSF	6	5000	210.0	185.0	35.0

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

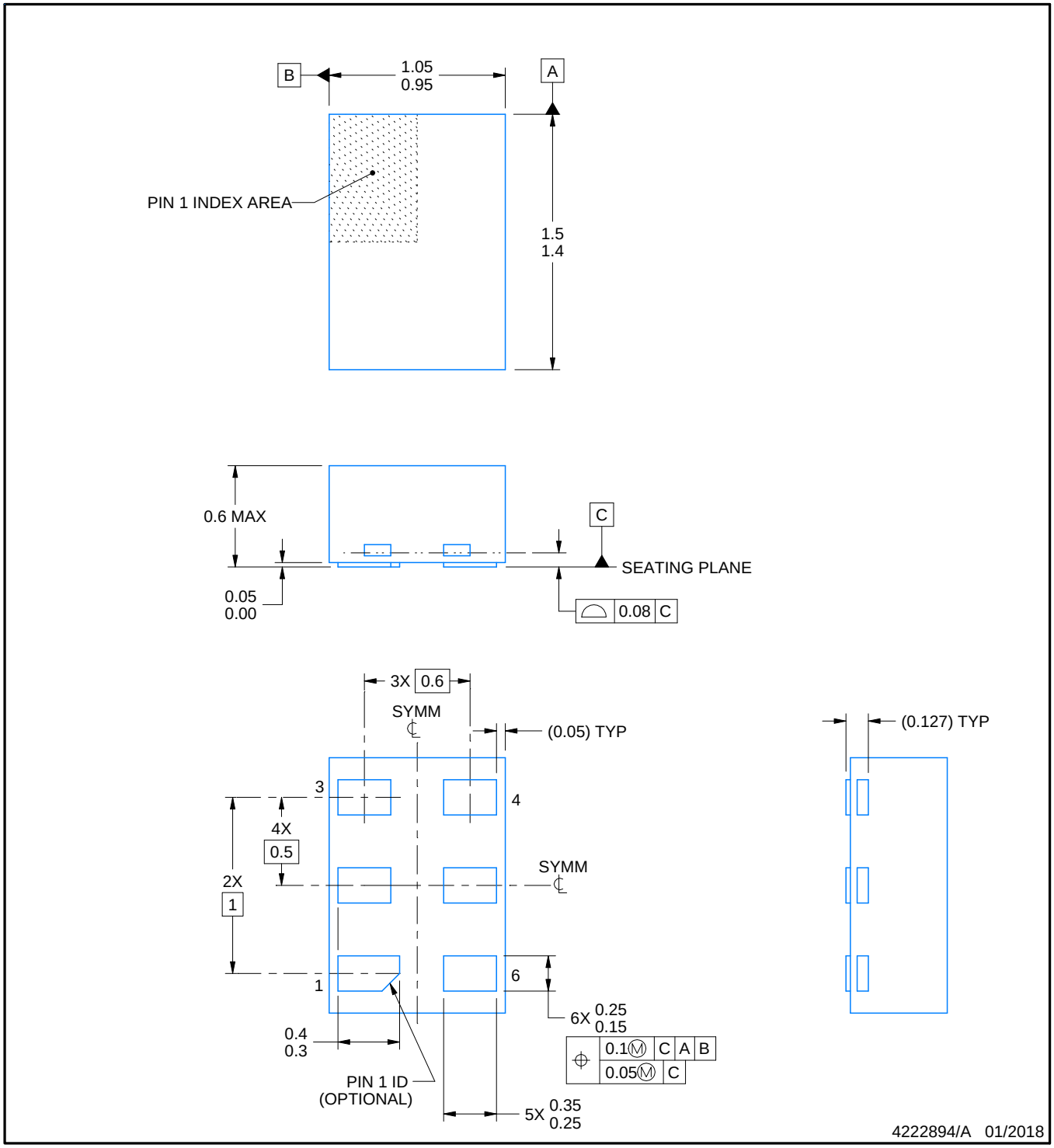
DRY0006A



PACKAGE OUTLINE

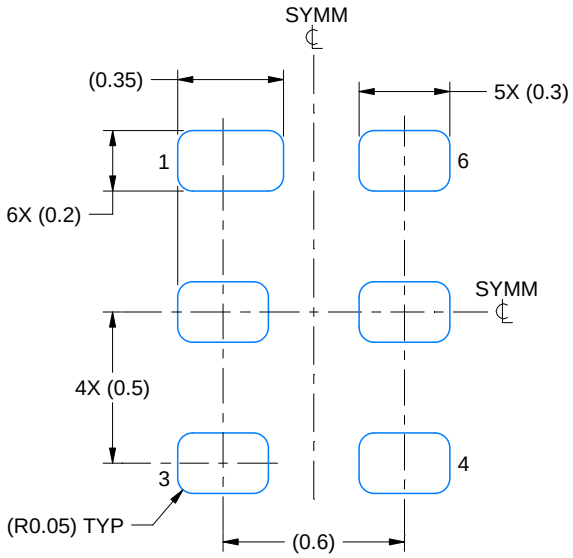
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

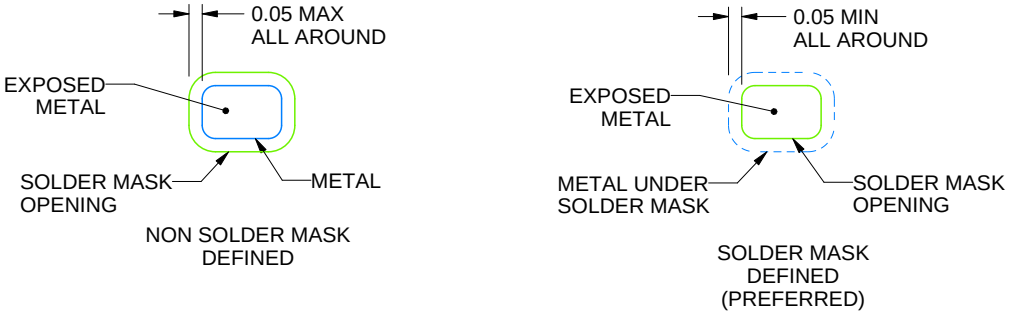


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

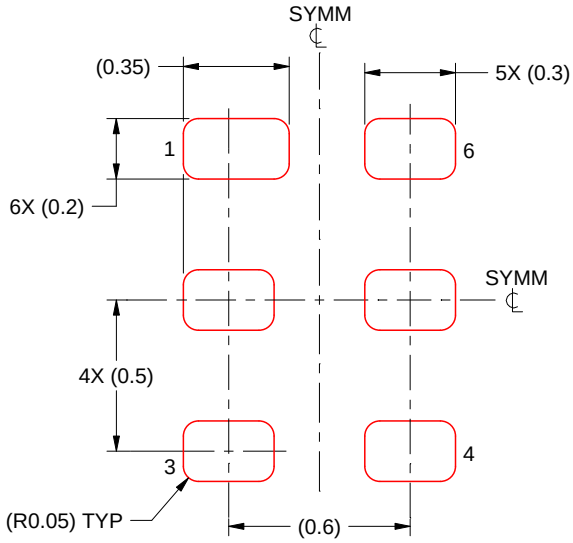
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

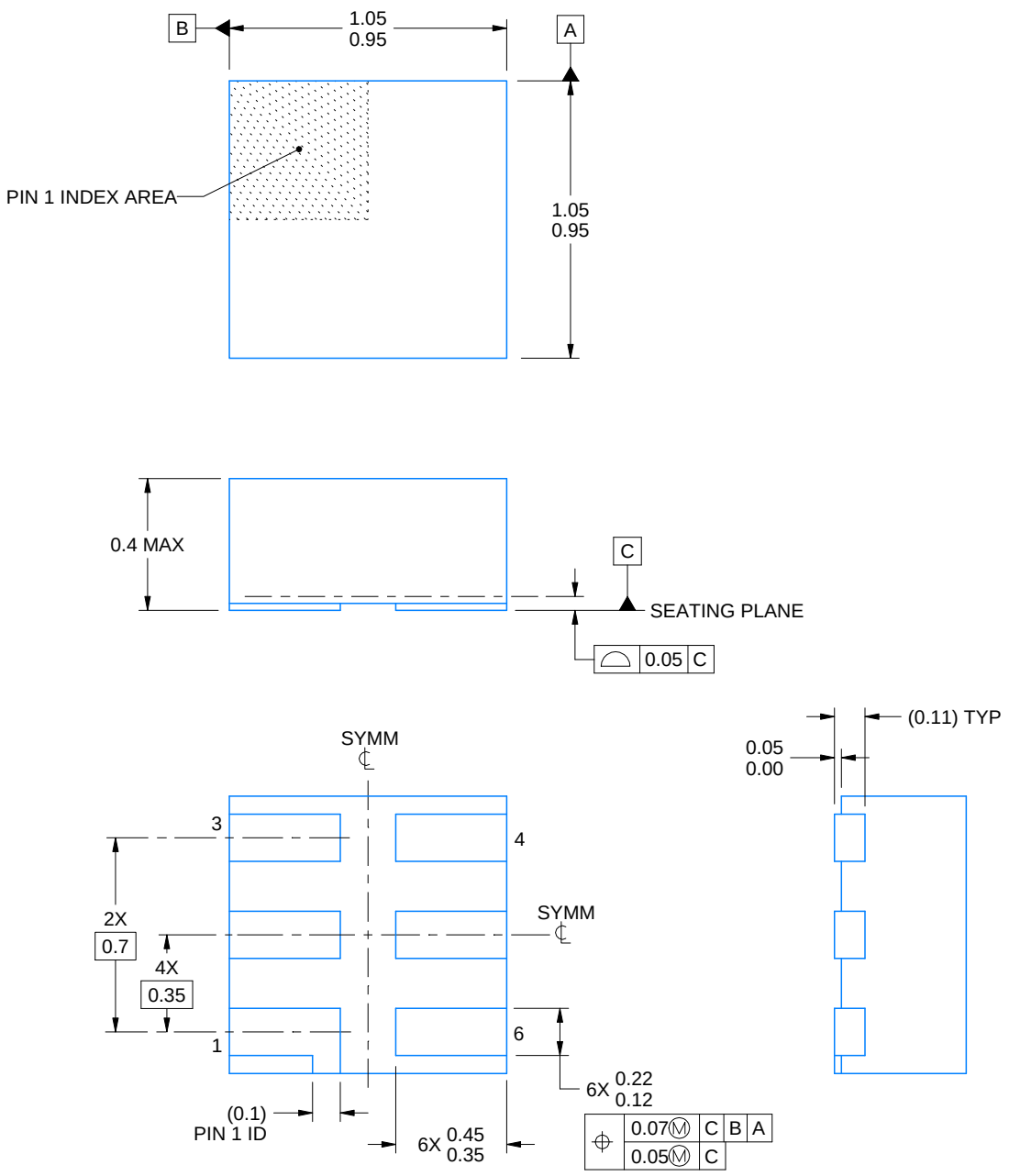
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

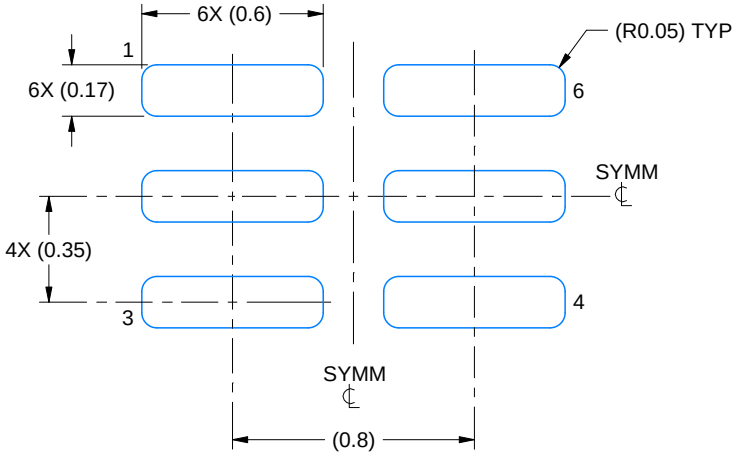
PLASTIC SMALL OUTLINE - NO LEAD



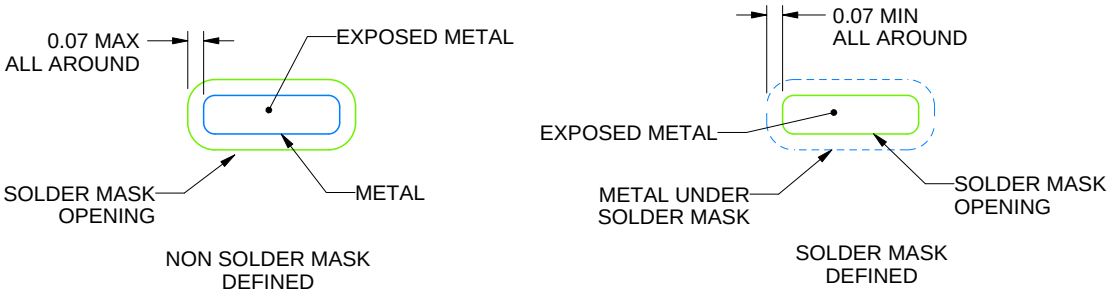
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

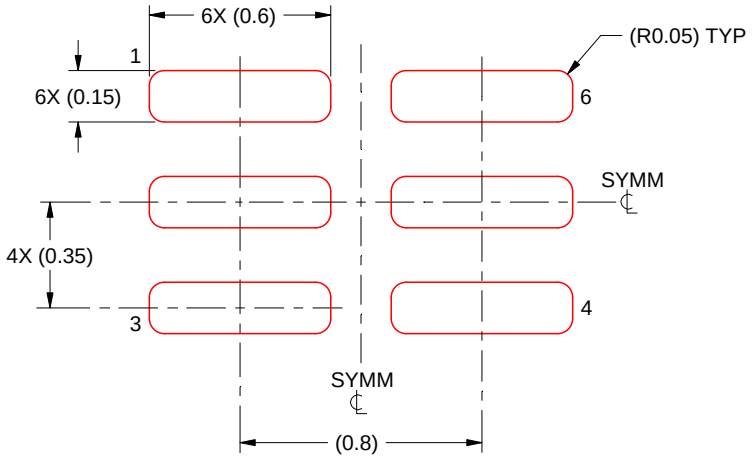
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

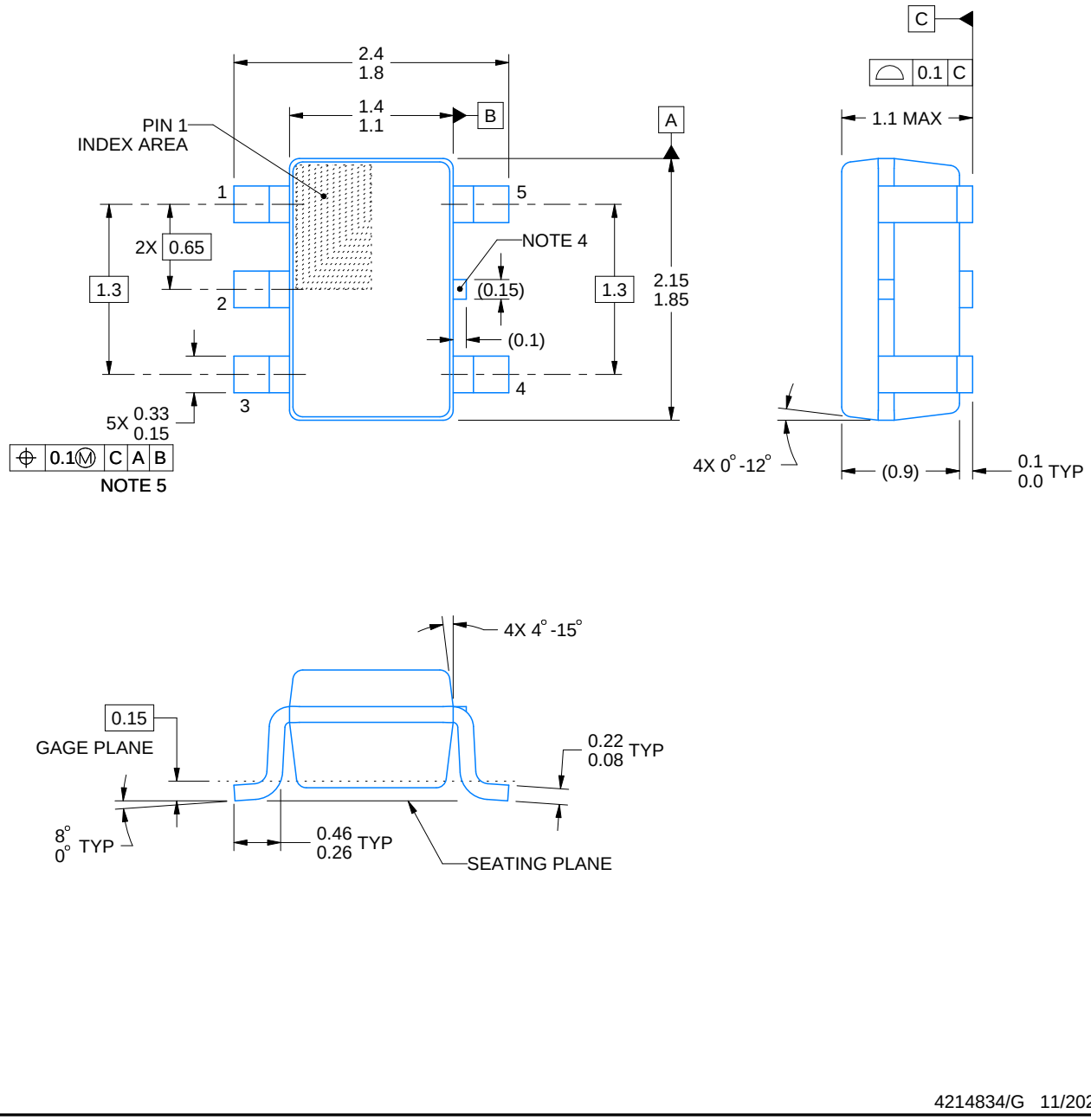
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

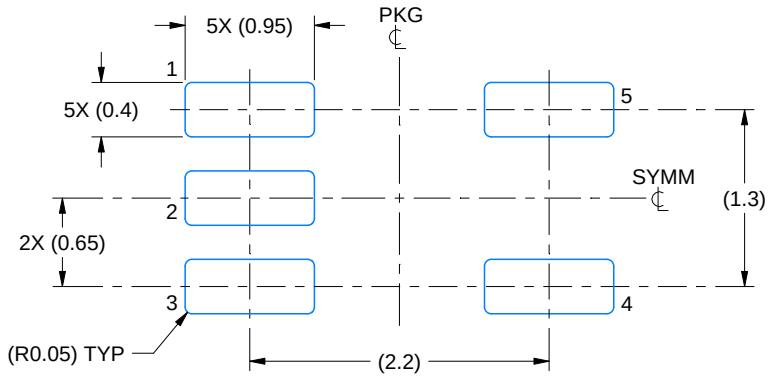
SMALL OUTLINE TRANSISTOR



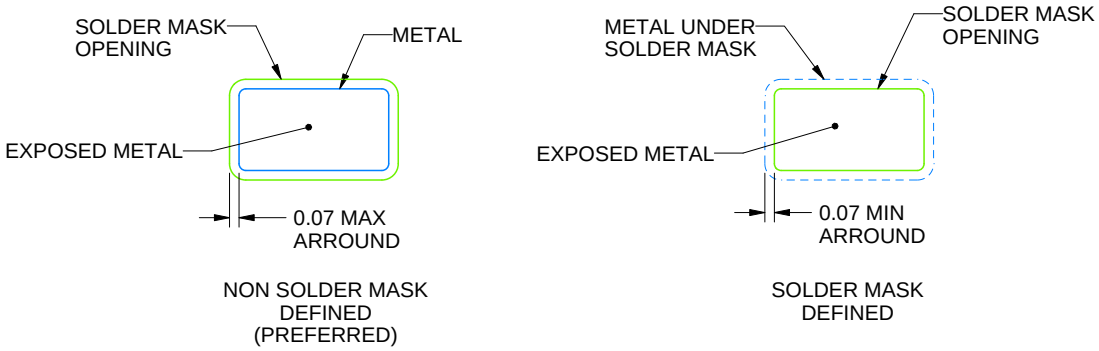
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

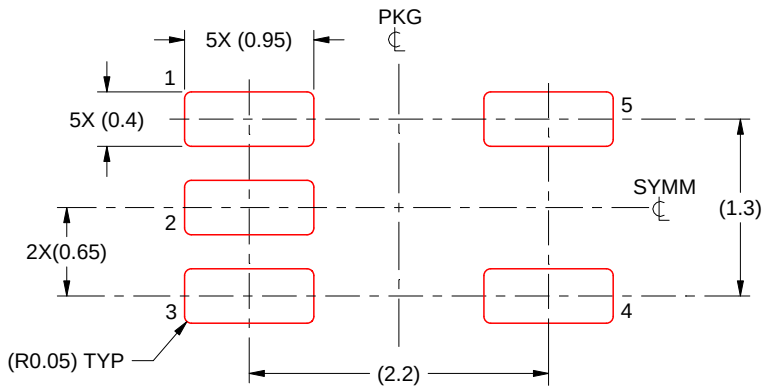


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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