

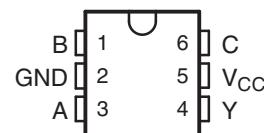
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

Check for Samples: [SN74AUP1T58](#)

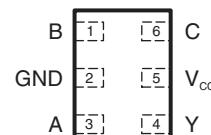
FEATURES

- Available in the Texas Instruments NanoStar™ Packages
- Single-Supply Voltage Translator
- 1.8 V to 3.3 V (at $V_{CC} = 3.3$ V)
- 2.5 V to 3.3 V (at $V_{CC} = 3.3$ V)
- 1.8 V to 2.5 V (at $V_{CC} = 2.5$ V)
- 3.3 V to 2.5 V (at $V_{CC} = 2.5$ V)
- Nine Configurable Gate Logic Functions
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity
- I_{off} Supports Partial-Power-Down Mode With Low Leakage Current (0.5 μ A)
- Very Low Static and Dynamic Power Consumption
- Pb-Free Packages Available: SON (DRY or DSF), SOT-23 (DBV), SC-70 (DCK), and NanoStar W CSP
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Related Devices: SN74AUP1T57, SN74AUP1T97, and SN74AUP1T98

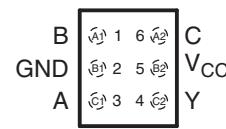
**DBV OR DCK PACKAGE
(TOP VIEW)**



**DRY OR DSF PACKAGE
(TOP VIEW)**



**YFP OR YZP PACKAGE
(TOP VIEW)**



DESCRIPTION/ORDERING INFORMATION

AUP technology is the industry's lowest-power logic technology designed for use in battery-operated or battery backed-up equipment. The SN74AUP1T58 is designed for logic-level translation applications with input switching levels that accept 1.8-V LVCMOS signals, while operating from either a single 3.3-V or 2.5-V V_{CC} supply.

The wide V_{CC} range of 2.3 V to 3.6 V allows the possibility of battery voltage drop during system operation and ensures normal operation between this range.

Schmitt-trigger inputs ($\Delta V_T = 210$ mV between positive and negative input transitions) offer improved noise immunity during switching transitions, which is especially useful on analog mixed-mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and allow for slow input signal transition.

The SN74AUP1T58 can be easily configured to perform a required gate function by connecting A, B, and C inputs to V_{CC} or ground (see Function Selection table). Up to nine commonly used logic gate functions can be performed.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar is a trademark of Texas Instruments.

I_{off} is a feature that allows for powered-down conditions ($V_{CC} = 0$ V) and is important in portable and mobile applications. When $V_{CC} = 0$ V, signals in the range from 0 V to 3.6 V can be applied to the inputs and outputs of the device. No damage occurs to the device under these conditions.

The SN74AUP1T58 is designed with optimized current-drive capability of 4 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

NanoStar package technology is a major breakthrough in IC packaging concepts, using the die as the package.

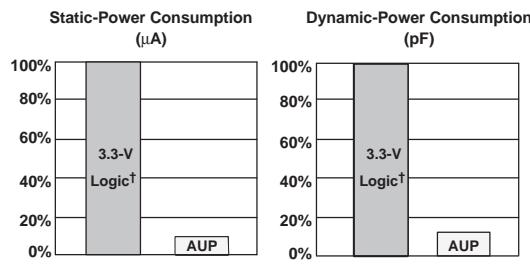
ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1T58YZPR	---TJ_
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP	Reel of 3000	SN74AUP1T58YFPR	---TJ_
	QFN – DRY	Reel of 5000	SN74AUP1T58DRYR	TJ
	uQFN – DSF	Reel of 5000	SN74AUP1T58DSFR	TJ
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1T58DBVR	HT5_
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1T58DCKR	TJ_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) DBV/DCK: The actual top-side marking has one additional character that designates the wafer fab/assembly site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

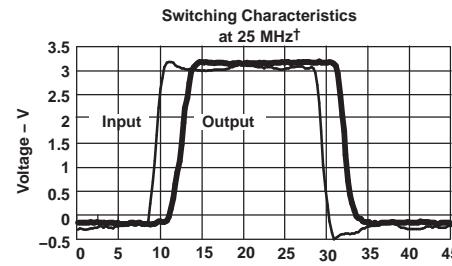
FUNCTION SELECTION TABLE

LOGIC FUNCTION	FIGURE NO.
2-input NAND gate	5
2-input OR gate with both inputs inverted	5
2-input AND gate with inverted input	6, 7
2-input NOR gate with inverted input	6, 7
2-input NAND gate with both inputs inverted	8
2-input OR gate	8
2-input XOR gate	9
Inverter	10
Noninverted buffer	11



† Single, dual, and triple gates

Figure 1. AUP – The Lowest-Power Family



† AUP1G08 data at $C_L = 15$ pF

Figure 2. Excellent Signal Integrity

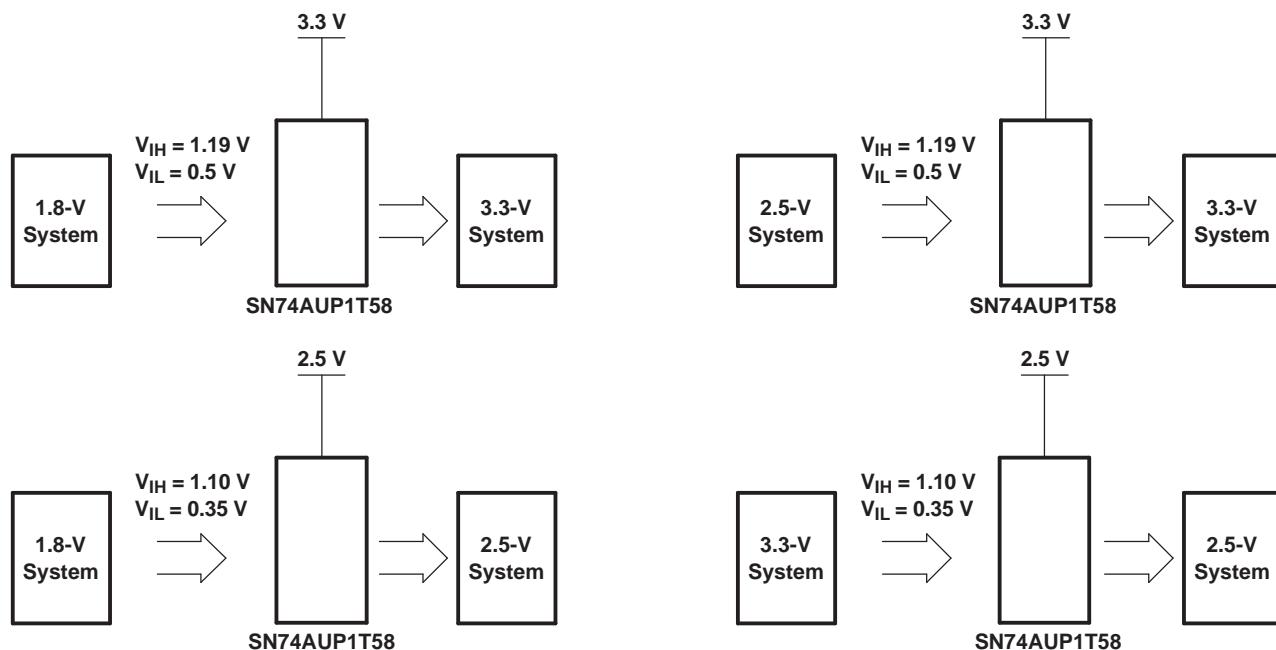


Figure 3. Possible Voltage-Translation Combinations

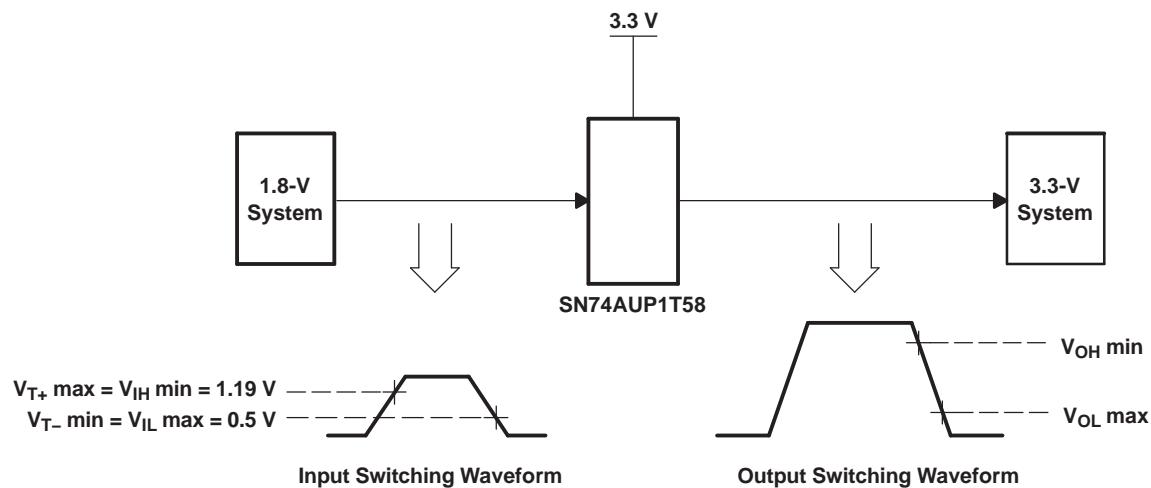
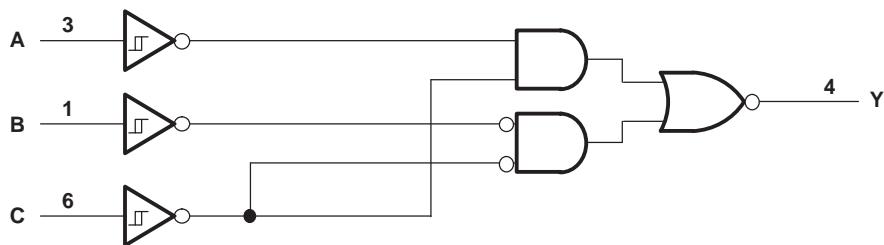


Figure 4. Switching Thresholds for 1.8-V to 3.3-V Translation

FUNCTION TABLE

INPUTS			OUTPUT
C	B	A	Y
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	L
H	H	H	L

LOGIC DIAGRAM (POSITIVE LOGIC)



LOGIC CONFIGURATIONS

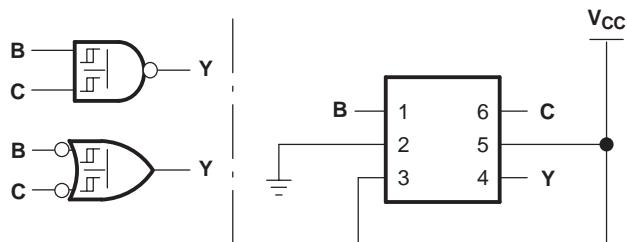
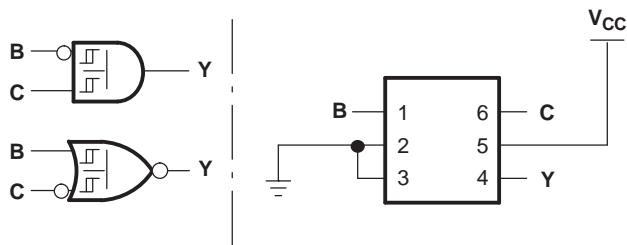
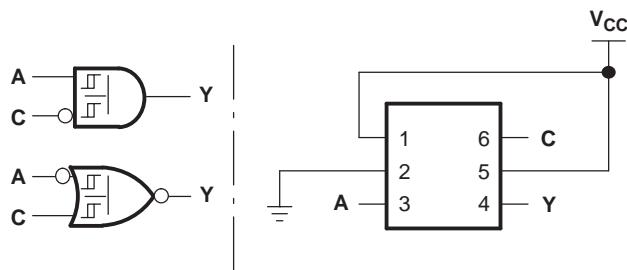


Figure 5. 00/14+32: 2-Input NAND Gate 2-Input OR Gate With Both Inputs Inverted

Figure 6. 14+08/14+02: 2-Input AND Gate With Inverted B Input
2-Input NOR Gate With Inverted Input



**Figure 7. 14+08/14+02: 2-Input AND Gate With Inverted C Input
2-Input NOR Gate With Inverted Input**

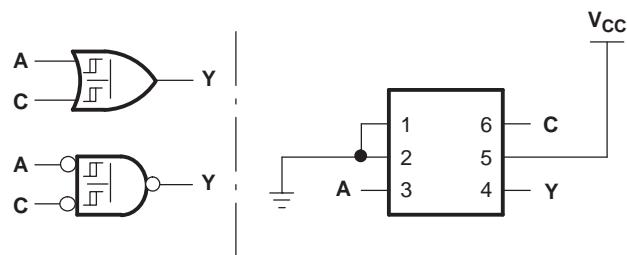


Figure 8. 32/14+00: 2-Input OR Gate 2-Input NAND Gate With Both Inputs Inverted

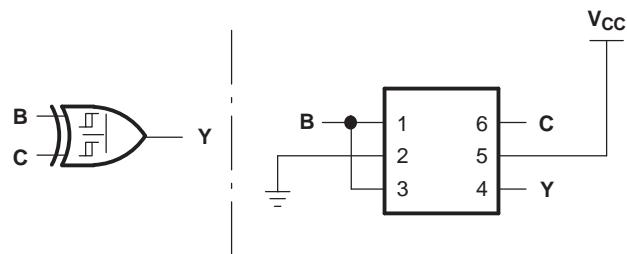


Figure 9. 86: 2-Input XOR Gate

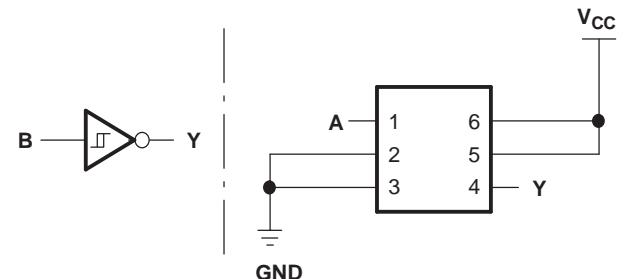


Figure 10. 04/14: Inverter

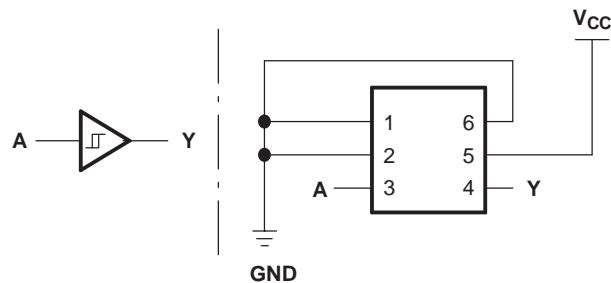


Figure 11. 17/34: Noninverted Buffer

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V
V_O	Output voltage range in the high or low state ⁽²⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		± 20	mA
	Continuous current through V_{CC} or GND		± 50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DBV package	165	°C/W
		DCK package	259	
		DRY package	340	
		DSF package	300	
		YFP package	123	
		YZP package	123	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	3.6	V
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.3$ V	-3.1	mA
		$V_{CC} = 3$ V	-4	
I_{OL}	Low-level output current	$V_{CC} = 2.3$ V	3.1	mA
		$V_{CC} = 3$ V	4	
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{T+} Positive-going input threshold voltage		2.3 V to 2.7 V	0.6	1.1		0.6	1.1	V
		3 V to 3.6 V	0.75	1.16		0.75	1.19	
V _{T-} Negative-going input threshold voltage		2.3 V to 2.7 V	0.35	0.6		0.35	0.6	V
		3 V to 3.6 V	0.5	0.85		0.5	0.85	
ΔV _T Hysteresis (V _{T+} – V _{T-})		2.3 V to 2.7 V	0.23	0.6		0.1	0.6	V
		3 V to 3.6 V	0.25	0.56		0.15	0.56	
V _{OH}	I _{OH} = -20 μA	2.3 V to 3.6 V	V _{CC} – 0.1			V _{CC} – 0.1		V
	I _{OH} = -2.3 mA	2.3 V	2.05			1.97		
	I _{OH} = -3.1 mA		1.9			1.85		
	I _{OH} = -2.7 mA	3 V	2.72			2.67		
	I _{OH} = -4 mA		2.6			2.55		
V _{OL}	I _{OL} = 20 μA	2.3 V to 3.6 V		0.1			0.1	V
	I _{OL} = 2.3 mA	2.3 V		0.31			0.33	
	I _{OL} = 3.1 mA			0.44			0.45	
	I _{OL} = 2.7 mA	3 V		0.31			0.33	
	I _{OL} = 4 mA			0.44			0.45	
I _I	All inputs	V _I = 3.6 V or GND	0 V to 3.6 V		0.1		0.5	μA
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V		0.1		0.5	μA
ΔI _{off}		V _I or V _O = 3.6 V	0 V to 0.2 V		0.2		0.5	μA
I _{CC}		V _I = 3.6 V or GND, I _O = 0	2.3 V to 3.6 V		0.5		0.9	μA
ΔI _{CC}	One input at 0.3 V or 1.1 V, Other inputs at 0 or V _{CC} , I _O = 0	2.3 V to 2.7 V					4	μA
	One input at 0.45 V or 1.2 V, Other inputs at 0 or V _{CC} , I _O = 0	3 V to 3.6 V					12	
C _i	V _I = V _{CC} or GND	3.3 V		1.5				pF
C _o	V _O = V _{CC} or GND	3.3 V		3				pF

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 1.8 V ± 0.15 V (unless otherwise noted)
(see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L	T _A = 25°C			T _A = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A, B, or C	Y	5 pF	1.8	2.3	2.9	0.5	6.8	ns
			10 pF	2.3	2.8	3.4	1	7.9	
			15 pF	2.6	3.1	3.8	1	8.7	
			30 pF	3.8	4.4	5.1	1.5	10.8	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$, $V_I = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)
(see [Figure 12](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.8	2.3	3.1	0.5	6	ns
			10 pF	2.2	2.8	3.5	1	7.1	
			15 pF	2.6	3.2	5.2	1	7.9	
			30 pF	3.7	4.4	5.2	1.5	10	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$, $V_I = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)
(see [Figure 12](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	2	2.7	3.5	0.5	5.5	ns
			10 pF	2.4	3.1	3.9	1	6.5	
			15 pF	2.8	3.5	4.3	1	7.4	
			30 pF	4	4.7	5.5	1.5	9.5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_I = 1.8 \text{ V} \pm 0.15 \text{ V}$ (unless otherwise noted)
(see [Figure 12](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	2	2.5	0.5	8	ns
			10 pF	2	2.4	2.9	1	8.5	
			15 pF	2.3	2.8	3.3	1	9.1	
			30 pF	3.4	3.9	4.4	1.5	9.8	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_I = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)
(see [Figure 12](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	1.9	2.4	0.5	5.3	ns
			10 pF	2	2.3	2.7	1	6.1	
			15 pF	2.3	2.7	3.1	1	6.8	
			30 pF	3.4	3.8	4.2	1.5	8.5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_I = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)
(see [Figure 12](#))

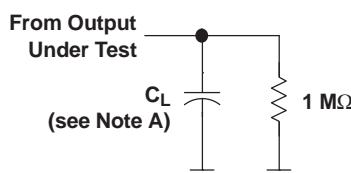
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	2.1	2.7	0.5	4.7	ns
			10 pF	2	2.4	3	1	5.7	
			15 pF	2.3	2.7	3.3	1	6.2	
			30 pF	3.4	3.8	4.4	1.5	7.8	

OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

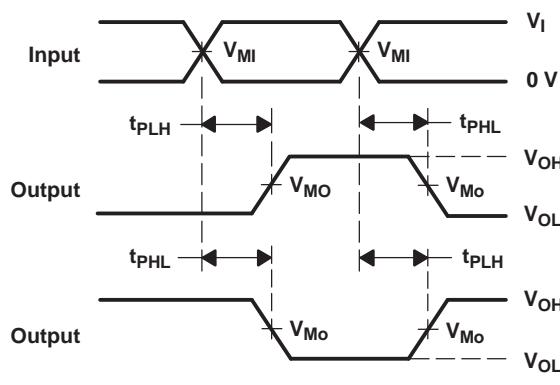
PARAMETER	TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
		TYP	TYP	
C_{pd} Power dissipation capacitance	$f = 10\text{ MHz}$	4	5	pF

PARAMETER MEASUREMENT INFORMATION



	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_{MI}	$V_I/2$	$V_I/2$
V_{MO}	$V_{CC}/2$	$V_{CC}/2$

LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

NOTES:

- C_L includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, slew rate $\geq 1 \text{ V/ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 12. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP1T58DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT5R
SN74AUP1T58DBVR.B	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT5R
SN74AUP1T58DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(TJF, TJR)
SN74AUP1T58DCKR.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(TJF, TJR)
SN74AUP1T58DCKT	Active	Production	SC70 (DCK) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TJF, TJR)
SN74AUP1T58DCKT.B	Active	Production	SC70 (DCK) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TJF, TJR)
SN74AUP1T58DCKTG4	Active	Production	SC70 (DCK) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TJR
SN74AUP1T58DCKTG4.B	Active	Production	SC70 (DCK) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TJR
SN74AUP1T58DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TJ
SN74AUP1T58DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TJ
SN74AUP1T58DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TJ
SN74AUP1T58DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TJ
SN74AUP1T58YFPR	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TJ2, TJN)
SN74AUP1T58YFPR.B	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TJ2, TJN)
SN74AUP1T58YZPR	Preview	Production	DSBGA (YZP) 6	3000 LARGE T&R	-	Call TI	Call TI	-40 to 85	

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

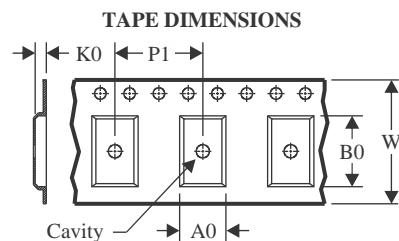
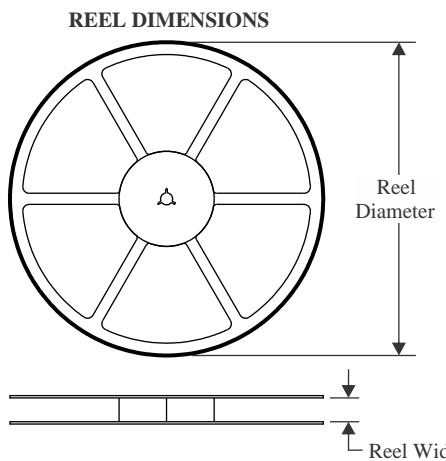
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

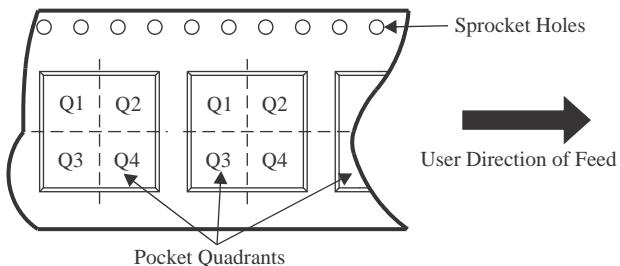
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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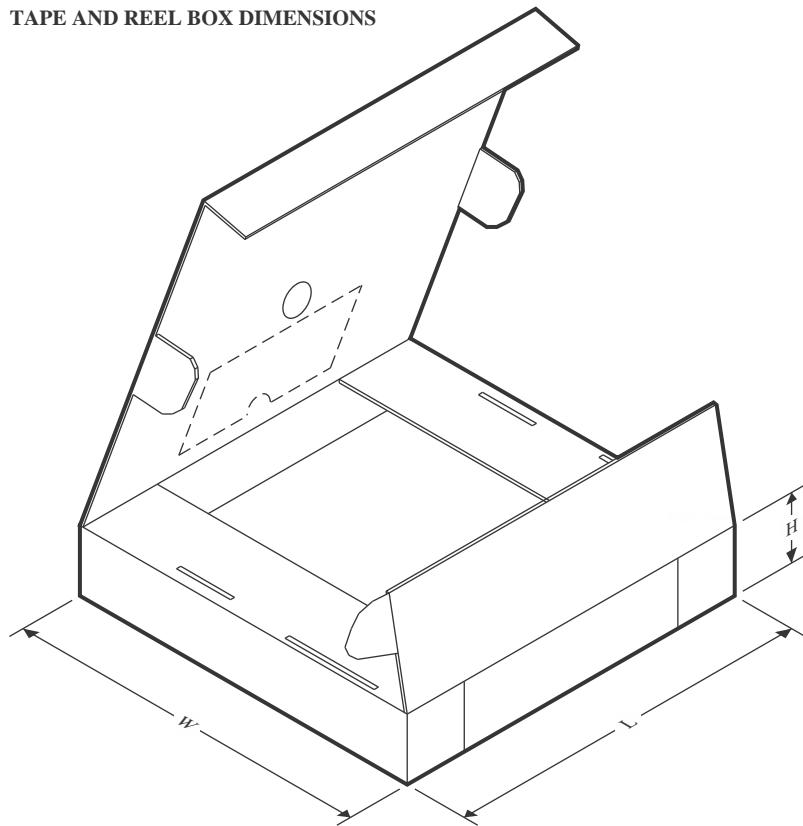
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T58DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T58DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AUP1T58DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74AUP1T58DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1T58DCKTG4	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1T58DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP1T58DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1T58YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T58DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUP1T58DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74AUP1T58DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74AUP1T58DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74AUP1T58DCKTG4	SC70	DCK	6	250	202.0	201.0	28.0
SN74AUP1T58DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP1T58DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1T58YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0

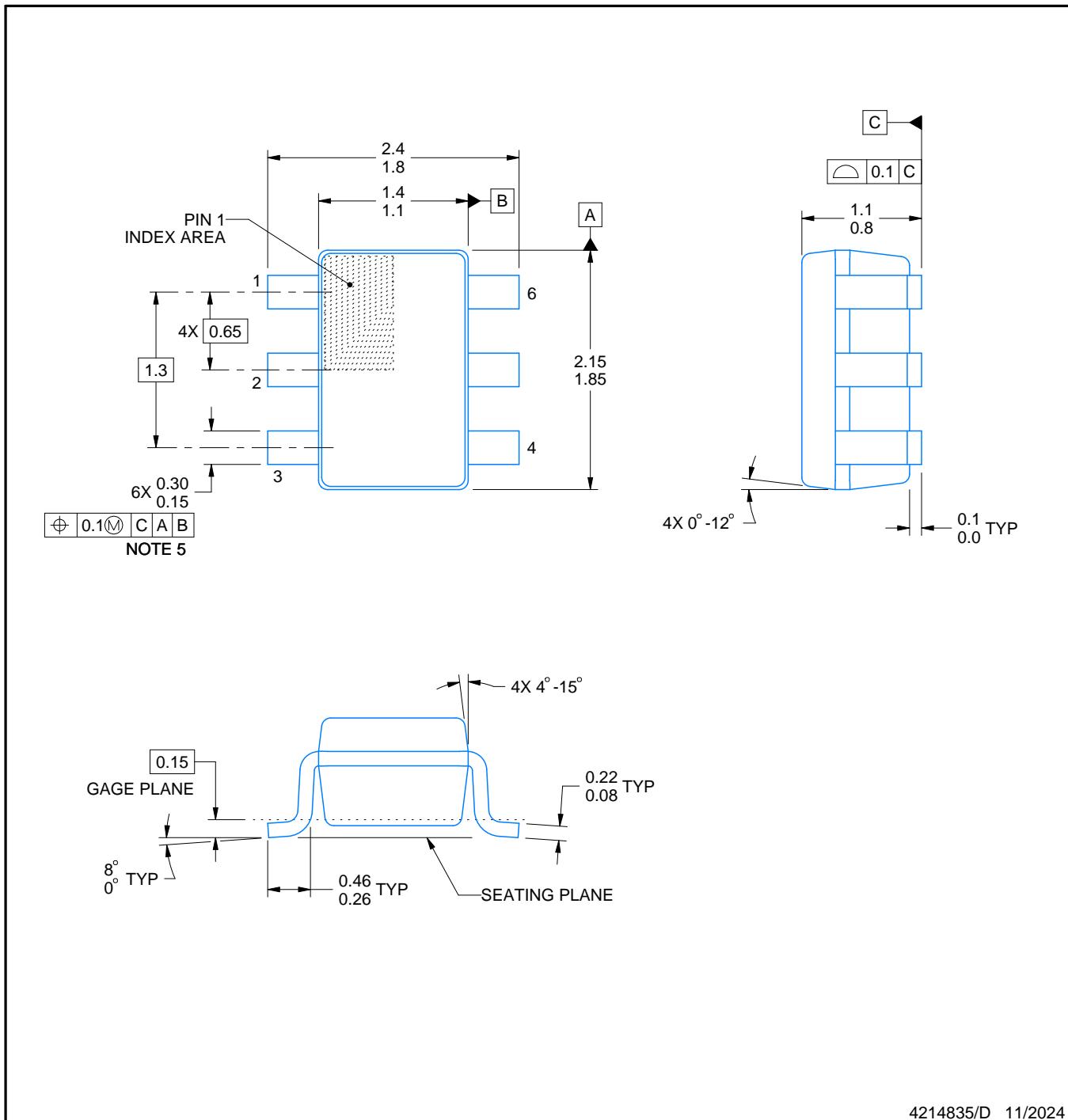
PACKAGE OUTLINE

DCK0006A



SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214835/D 11/2024

NOTES:

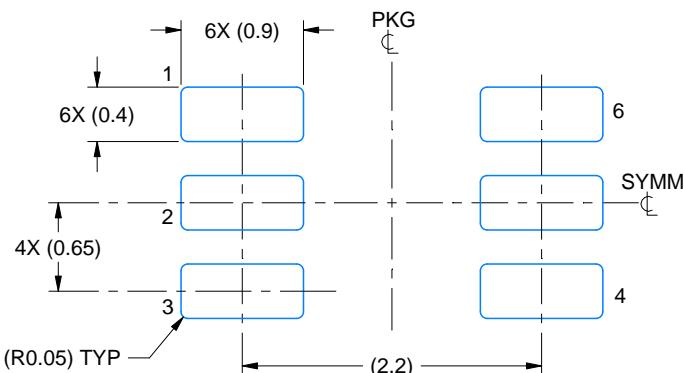
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.

EXAMPLE BOARD LAYOUT

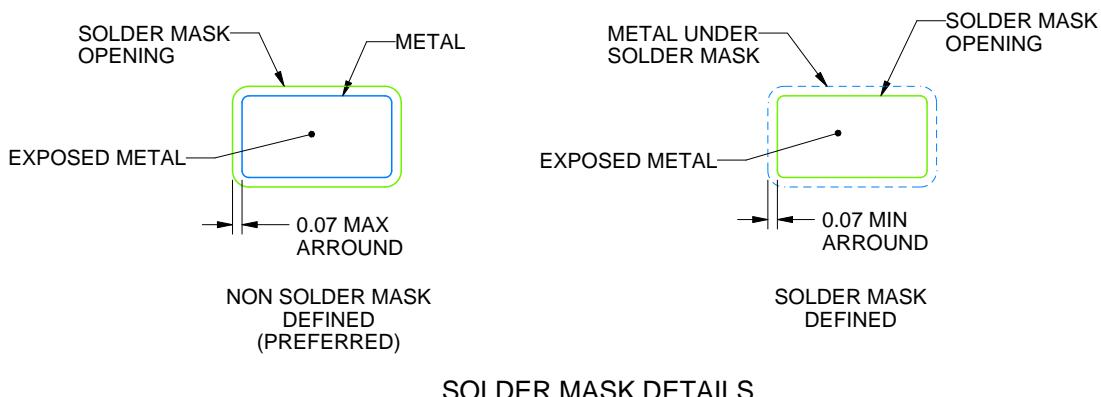
DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



4214835/D 11/2024

NOTES: (continued)

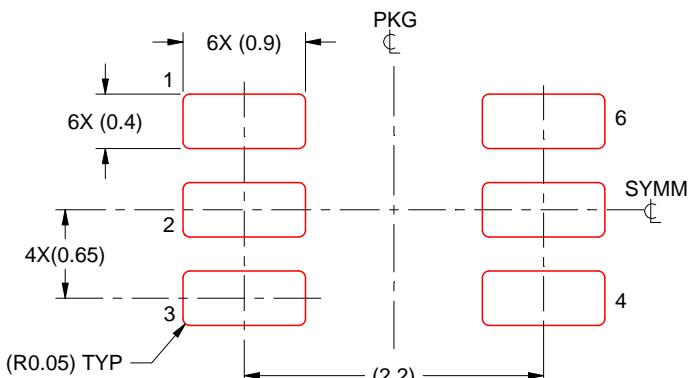
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DRY 6

GENERIC PACKAGE VIEW

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

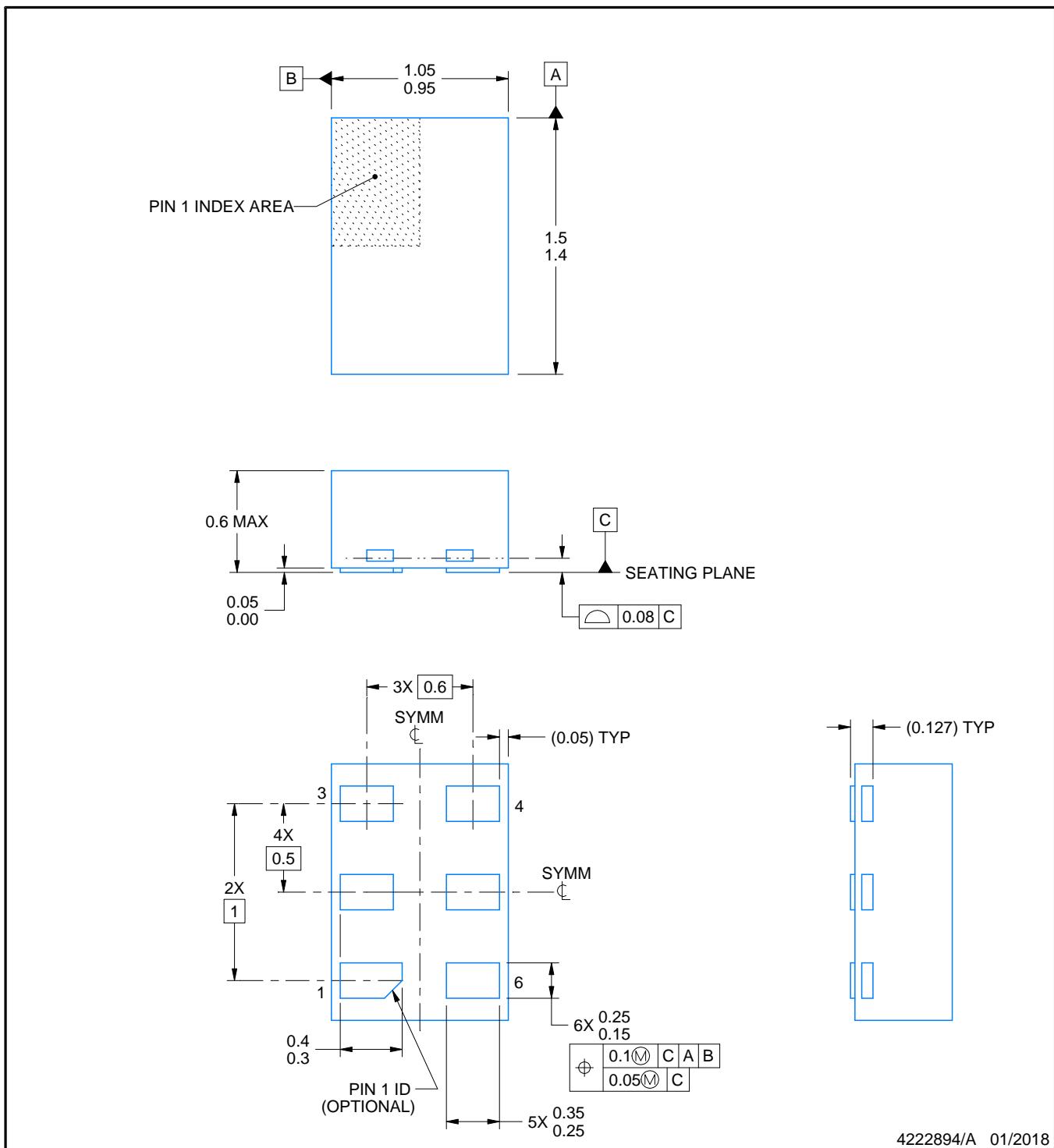
PACKAGE OUTLINE

DRY0006A



USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

NOTES:

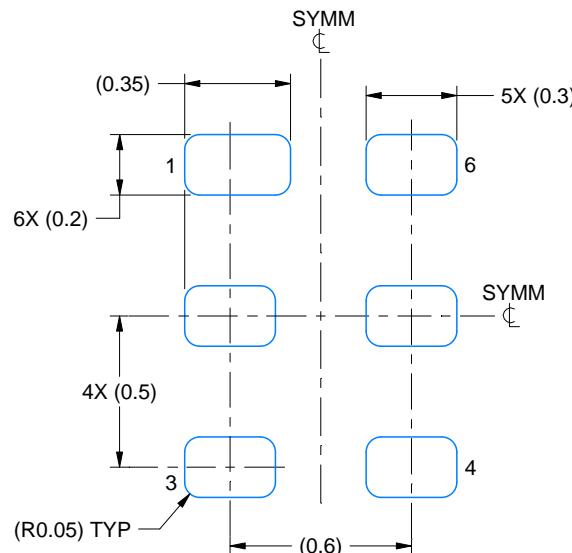
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

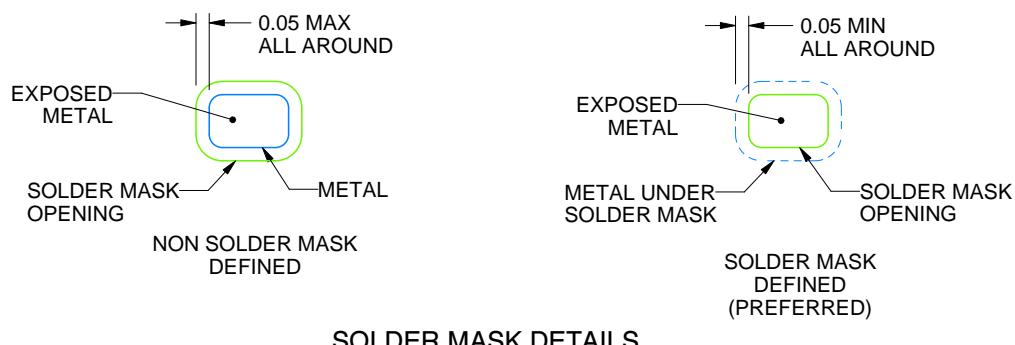
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

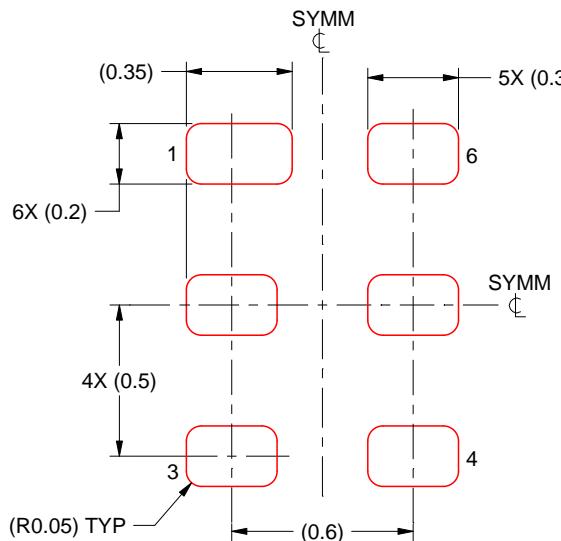
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

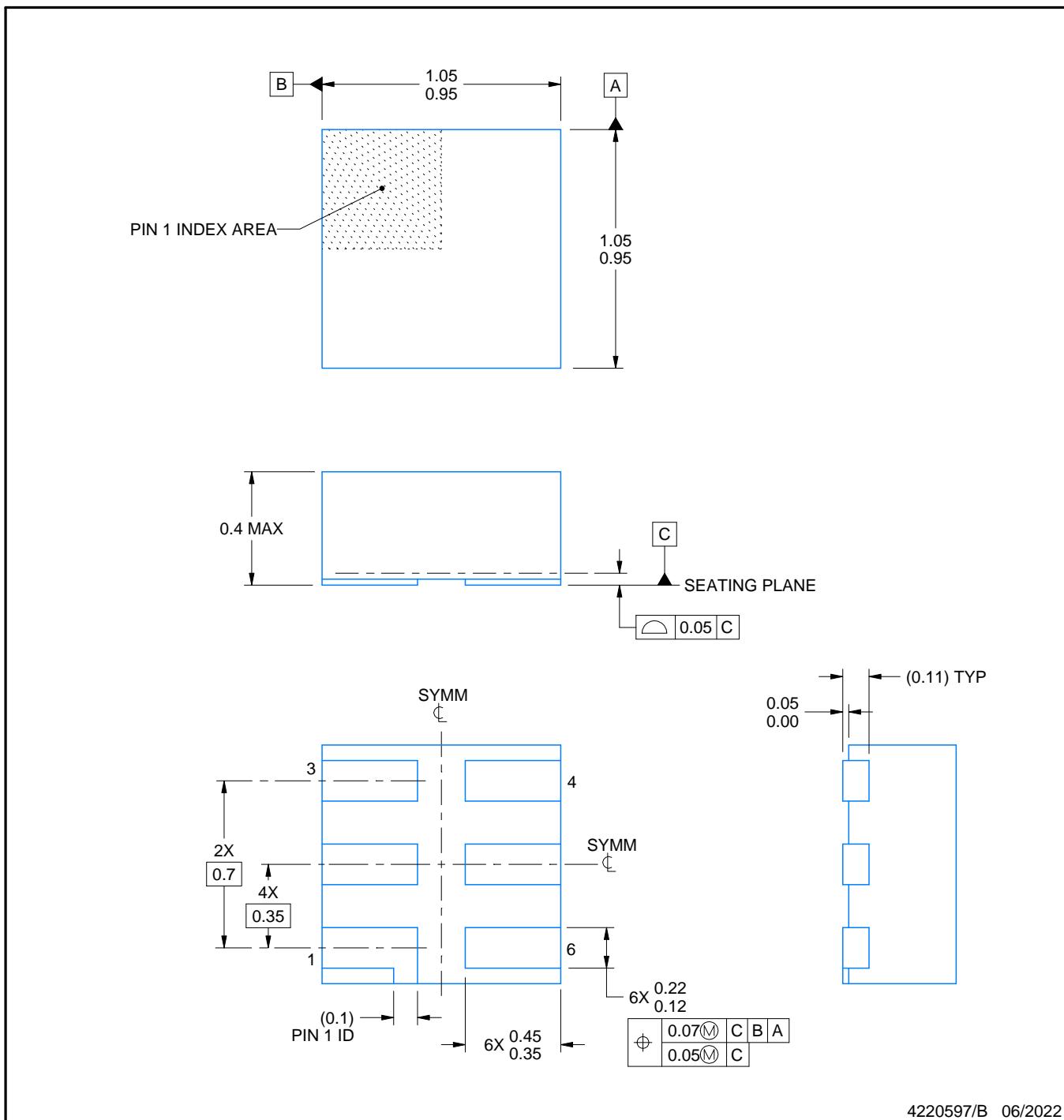


PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

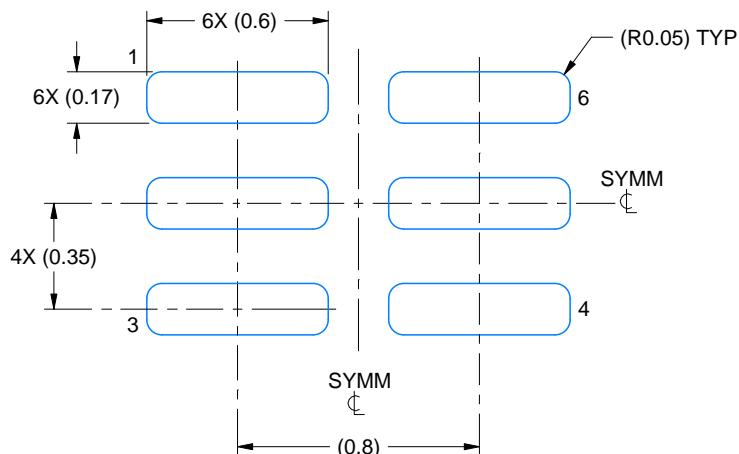
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

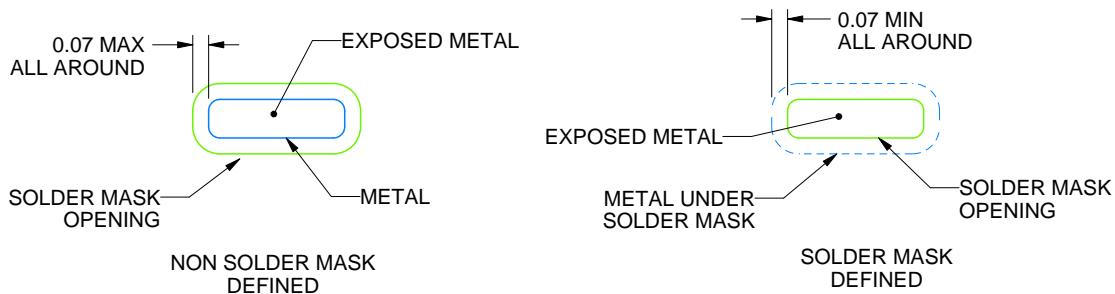
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

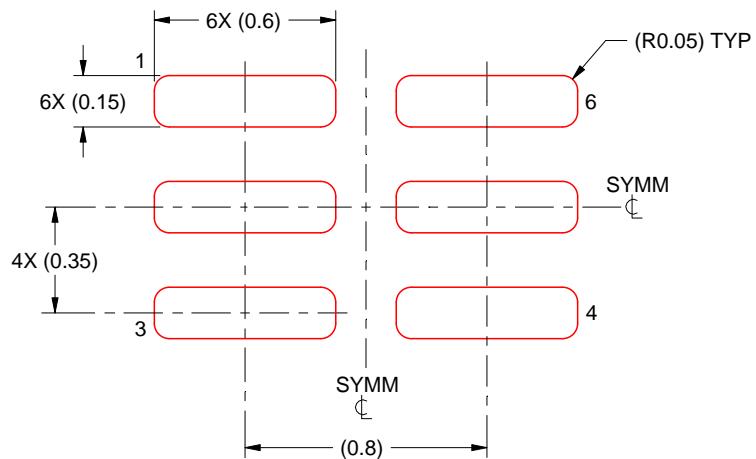
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

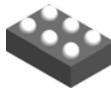
PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

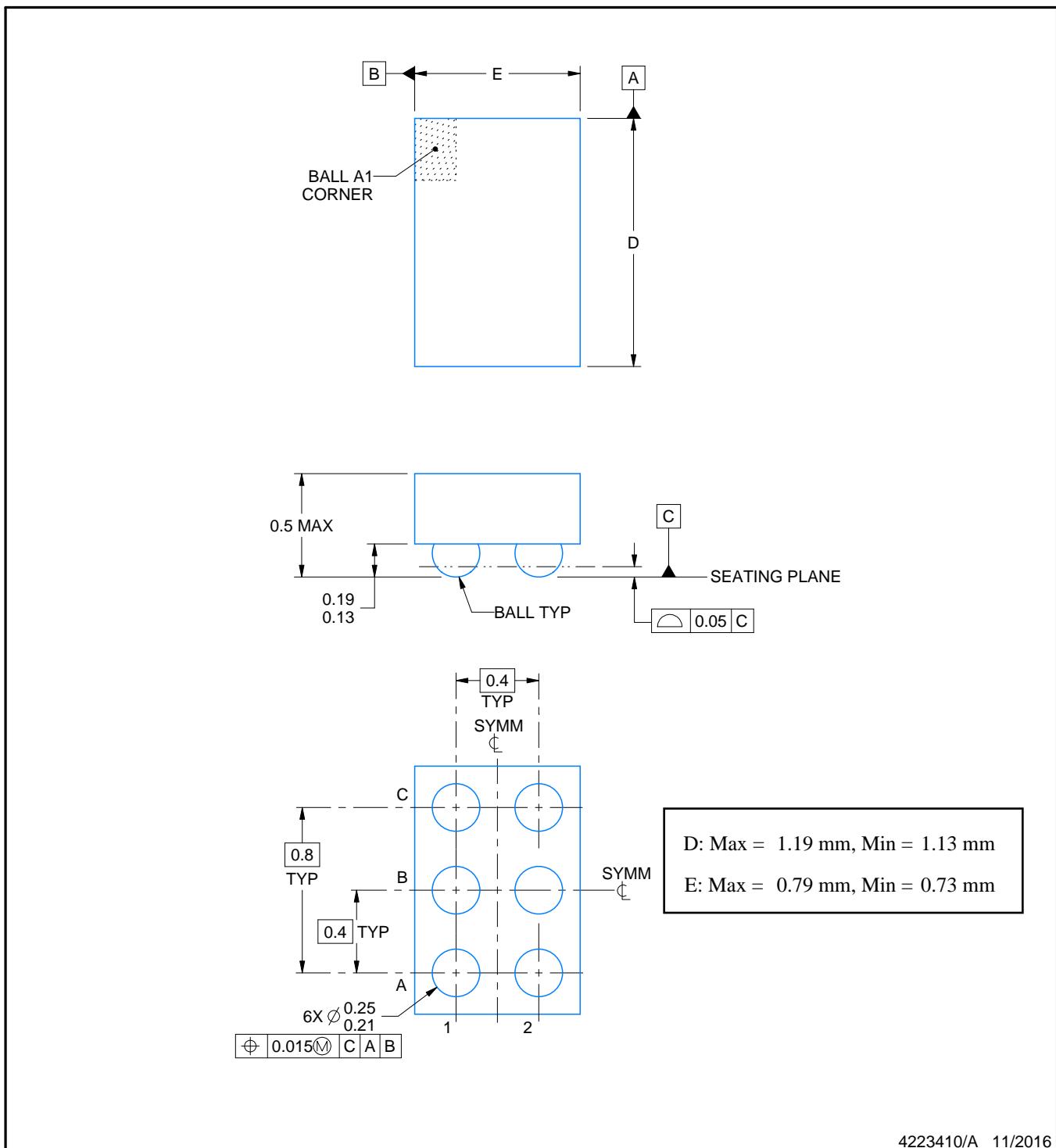
PACKAGE OUTLINE

YFP0006



DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223410/A 11/2016

NOTES:

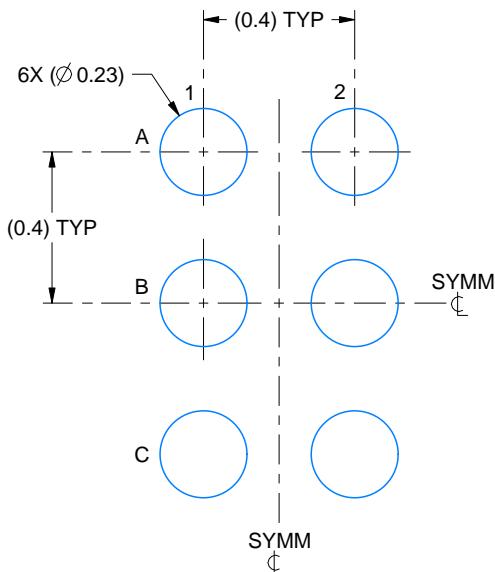
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

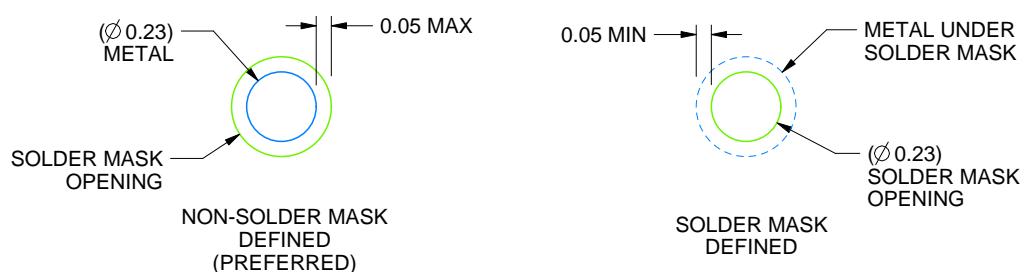
YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE



SOLDER MASK DETAILS NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

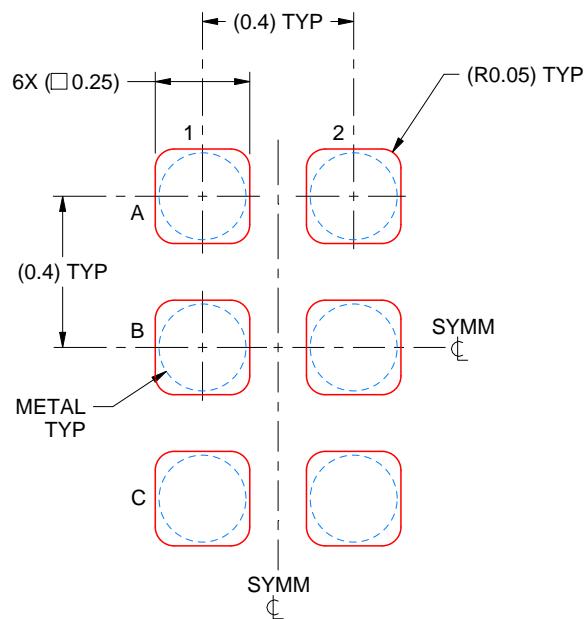
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

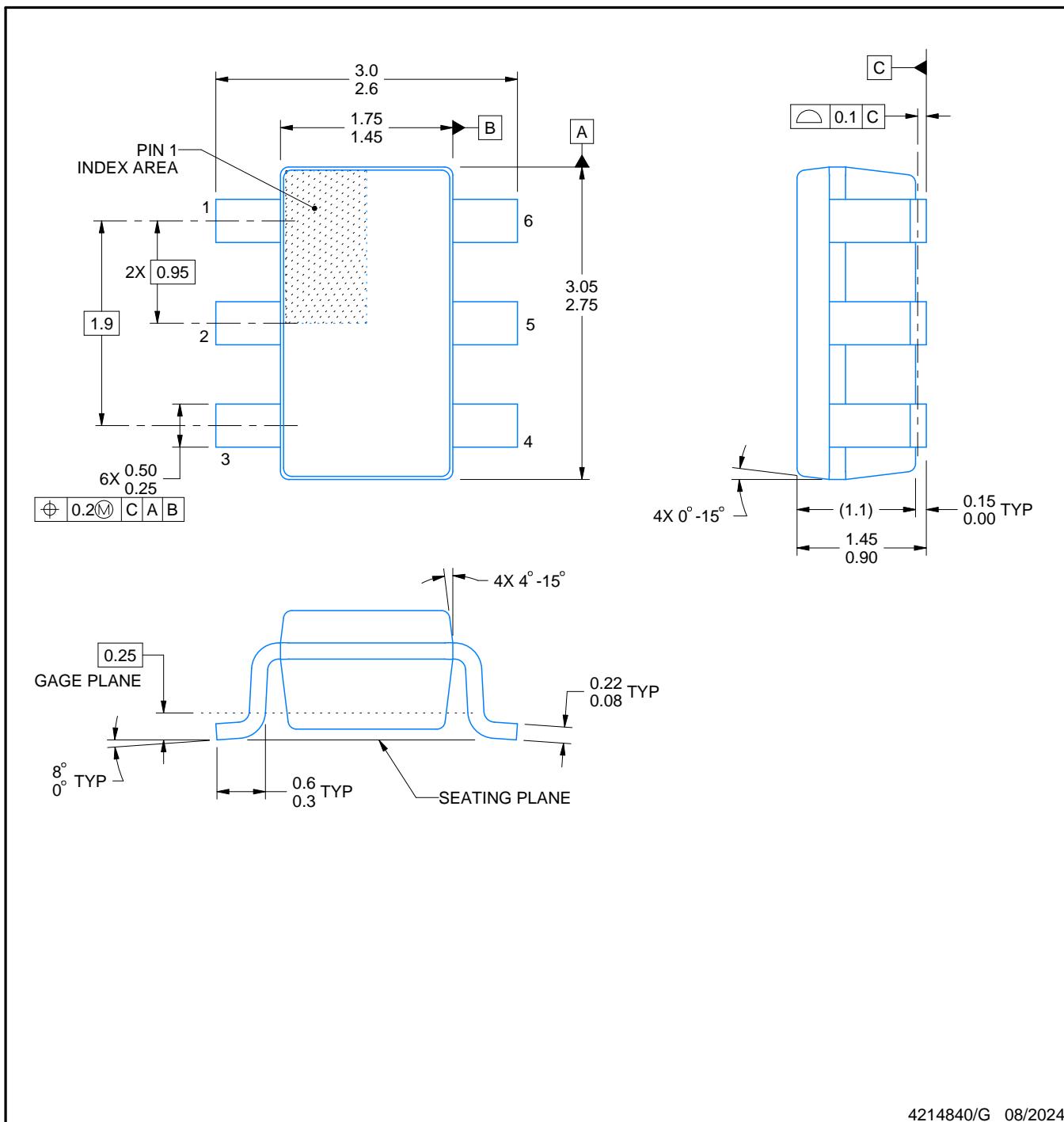
PACKAGE OUTLINE

DBV0006A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

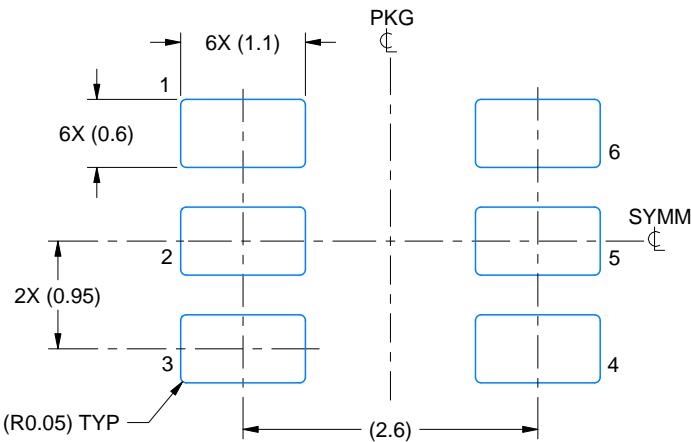
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

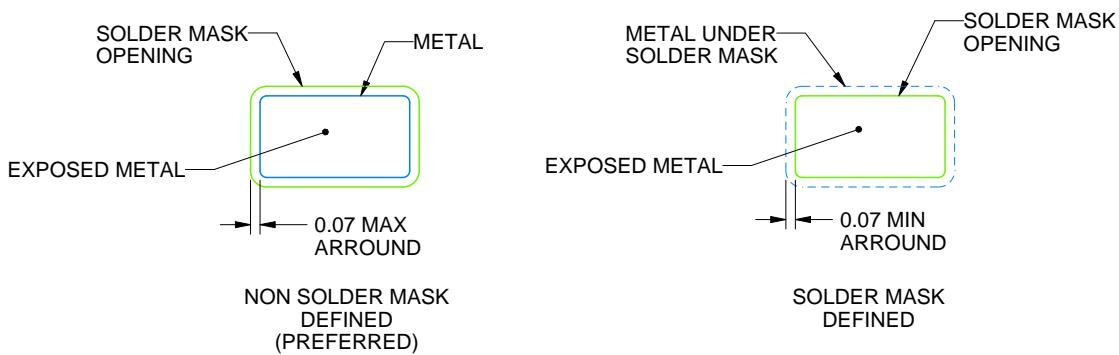
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

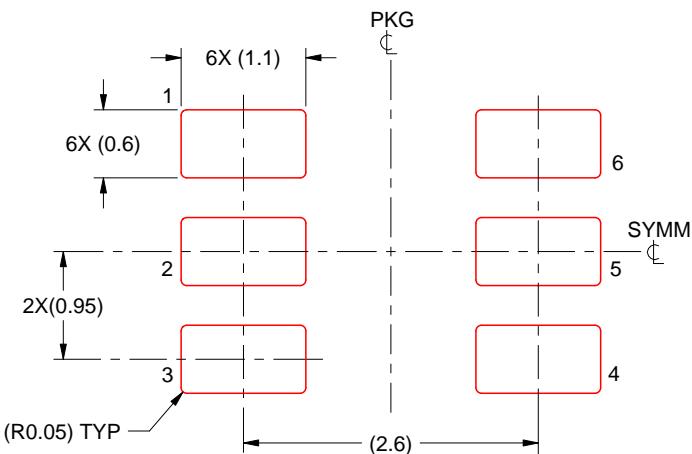
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025