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TEXAS
INSTRUMENTS

SN74CBT3244

SCDS001O −NOVEMBER 1992−REVISED SEPTEMBER 2015

SN74CBT3244 Octal FET Bus Switch

1 Features

- High-Bandwidth Data Path (Up to 200 MHz)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 5 Ω Typical)
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 6 pF Typical)
- Low Power Consumption (I_{CC} = 50 µA Maximum)
- V_{CC} Operating Range From 4.5 V to 5 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Standard '244-Type Pinout

2 Applications

- Multi-Processor Communications
- Test and Measurement Systems
- Factory Automation Control Boards
- Building Automation Control Boards

3 Description

The SN74CBT3244 device provides eight bits of high-speed TTL-compatible bus switching. The SOIC, SSOP, TSSOP, and TVSOP packages provide a standard '244 device pinout. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay. The device is organized as two 4-bit low-impedance switches with separate output-enable ($\overline{OE}$) inputs.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74CBT3244RGY	VQFN (20)	3.35 mm x 4.35 mm
SN74CBT3244DW	SOIC (20)	9.97 mm x 12.60 mm
SN74CBT3244DB	SSOP (20)	5.80 mm x 8.55 mm
SN74CBT3244DBQ	SSOP (20)	8.65 mm x 3.90 mm
SN74CBT3244PW	TSSOP (20)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
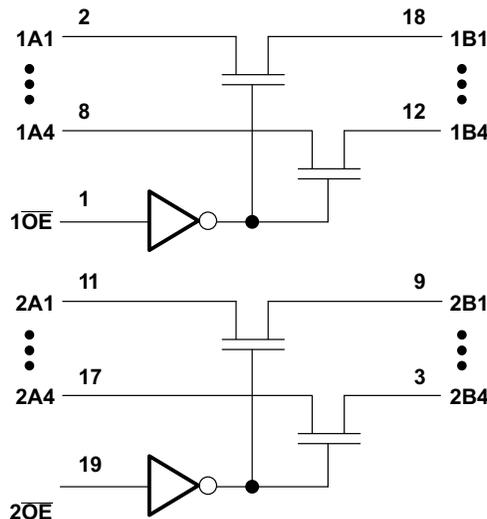
Simplified Schematic

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4 Revision History

Changes from Revision N (September 2003) to Revision O   **Page**

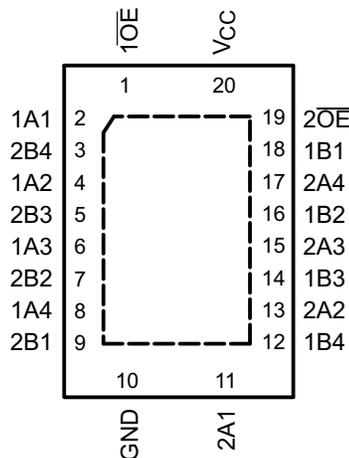- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Product Folder Links: *SN74CBT3244*

5 Pin Configuration and Functions

DB, DBQ, DGV, or PW Package
20-Pin SSOP, TVSOP, or TSSOP
Top View

```
1OE    [ 1      20 ]  VCC
1A1    [ 2      19 ]  2OE
2B4    [ 3      18 ]  1B1
1A2    [ 4      17 ]  2A4
2B3    [ 5      16 ]  1B2
1A3    [ 6      15 ]  2A3
2B2    [ 7      14 ]  1B3
1A4    [ 8      13 ]  2A2
2B1    [ 9      12 ]  1B4
GND    [ 10     11 ]  2A1
```
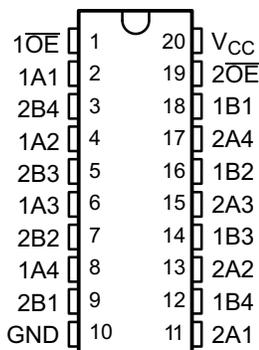
RGY Package
20-Pin VQFN
Top View

```
        1OE   VCC
         1     20
1A1   2           19   2OE
2B4   3           18   1B1
1A2   4           17   2A4
2B3   5           16   1B2
1A3   6           15   2A3
2B2   7           14   1B3
1A4   8           13   2A2
2B1   9           12   1B4
        10     11
        GND   2A1
```

Pin Functions

PIN		I/O	DESCRIPTION
NAME	DB, DBQ, DGV, PW, SSOP, TVSOP,TSSOP, VQFN		
1A1	2	I/O	Transceiver I/O pin
1A2	4	I/O	Transceiver I/O pin
1A3	6	I/O	Transceiver I/O pin
1A4	8	I/O	Transceiver I/O pin
2A1	11	I/O	Transceiver I/O pin
2A2	13	I/O	Transceiver I/O pin
2A3	15	I/O	Transceiver I/O pin
2A4	17	I/O	Transceiver I/O pin
1B1	18	I/O	Transceiver I/O pin
1B2	16	I/O	Transceiver I/O pin
1B3	14	I/O	Transceiver I/O pin
1B4	12	I/O	Transceiver I/O pin
2B1	9	I/O	Transceiver I/O pin
2B2	7	I/O	Transceiver I/O pin
2B3	5	I/O	Transceiver I/O pin
2B4	3	I/O	Transceiver I/O pin
$\overline{1OE}$	1	I	Output Enable. When high A and B are disconnected, when Low A and B are connected
$\overline{2OE}$	19	I	Output Enable. When high A and B are disconnected, when Low A and B are connected
GND	10	—	Ground
V_{CC}	20	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage, V_{CC}	−0.5	7	V
Input voltage, V_I [2]	−0.5	7	V
Continuous channel current		128	mA
Clamp current, I_K ($V_{I/O} < 0$)		−50	mA
Storage temperature, T_{stg}	−65	150	°C

(1)   Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)   The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

(1)   All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information Package

THERMAL METRIC[1][2]	SN74CBT3244					UNIT
	DB (SSOP)	DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	
	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	70	68	92	83	37	°C/W

(1)   For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2)   The package thermal impedance is calculated in accordance with JESD 51-7.

Product Folder Links: *SN74CBT3244*

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V	V_I = 5.5 V or GND				±5	µA
I_{CC}		V_{CC} = 5.5 V	I_O = 0,	V_I = V_{CC} or GND			50	µA
ΔI_{CC}[2]	Control inputs	V_{CC} = 5.5 V	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0	$\overline{OE}$ = V_{CC}			6		pF
r_{on}[3]		V_{CC} = 4.5 V	V_I = 0 V	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V	I_I = 15 mA		10	15	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(3) Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

6.6 Switching Characteristics

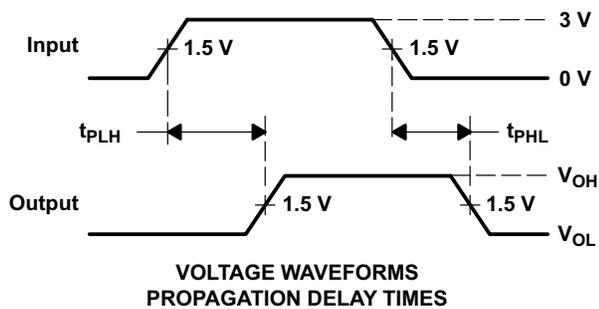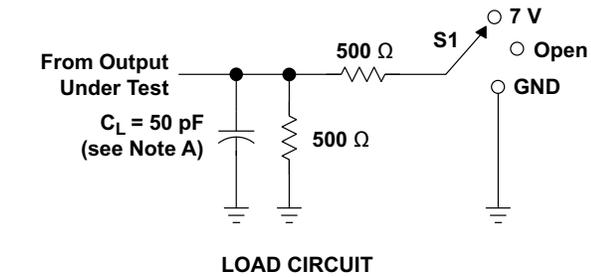over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{pd}[1]	A or B	B or A			0.25	ns
t_{en}	$\overline{OE}$	A or B	1		8.9	ns
t_{dis}	OE	A or B	1		7.4	ns

(1) This propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
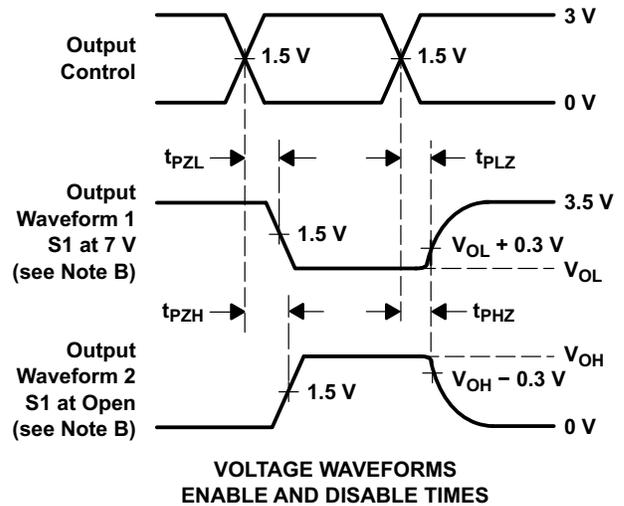
6.7 Typical Characteristics
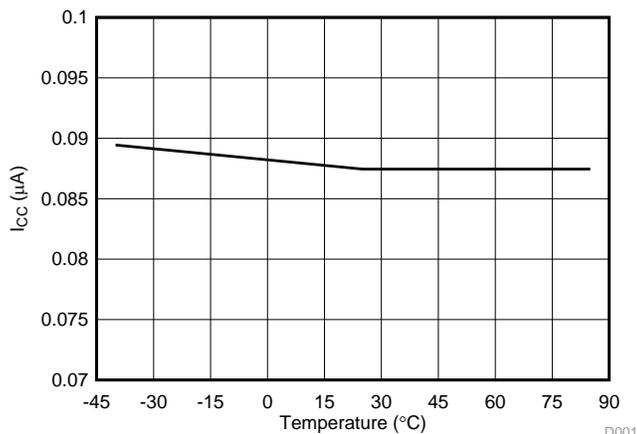
Note device variation mentioned in *Electrical Characteristics*

Figure 1. I_{CC} variation With Temperature

7 Parameter Measurement Information

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

Product Folder Links: *SN74CBT3244*

8 Detailed Description

8.1 Overview

The SN74CBT3244 has eight bits of high-speed TTL-compatible bus switching. The switches are grouped in the 2 groups of 4 bits each. Each group has output-enabled inputs to allow signals to pass between A and B ports. The signals can travel from A port to B port or vice versa.

The low ON-state resistance of the switch allows connections to be made with minimal propagation delay. The device is ideal for switching high speed digital signals between microprocessors and peripheral devices which is useful in test applications, measurement applications, and control boards for factory automation.
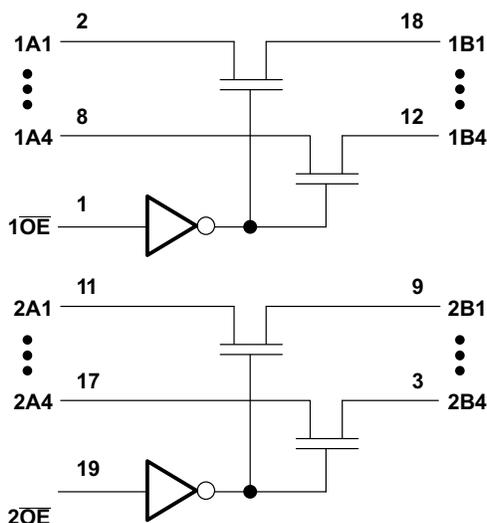
8.2 Functional Block Diagram

Figure 3. Simplified Schematic

8.3 Feature Description

The SN74CBT3244 device support same pin configuration as industry standard '244. This device has a near zero propagation delay allowing high speed signal switching up to 200 Mhz. The signals see lower distortion since the device has low ON-resistance (5 Ω) coupled with low-output capacitance (6 pF) . SN74CBT3244 has a very low power consumption in idle state consuming I_{CC} of 50 µA only allowing power-saving for the system. The device supports signal inputs any where between 0 V to 5 V.

8.4 Device Functional Modes

The device is organized as two 4-bit low-impedance switches with separate output-enable ($\overline{OE}$) inputs.The Output Enable $\overline{OE}$ is active low, implying when low A port is connected to B port. This switch is bidirectional in nature. Asserting $\overline{OE}$ high will disconnect A port from B port. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Table 1. Function Table
(Each 4-Bit Bus Switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74CBT3244 device can be used to control up to 4 bits with 2 channels simultaneously. The application shown in Figure 4 is a 8-bit bus being controlled. The $\overline{OE}$ pins are used to control the chip from the bus controller. This is a generic example and can apply to many situations. If an application requires fewer than 8 bits, ensure that the A side is tied either high or low on unused channels.
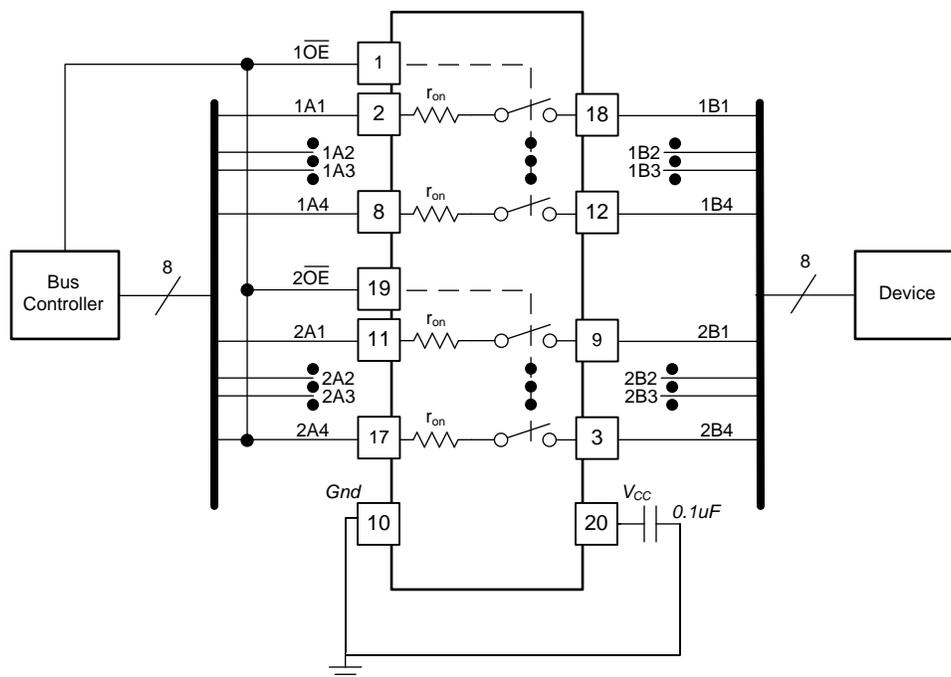
9.2 Typical Application

Figure 4. Typical Application

9.2.1 Design Requirements

A 0.1-µF bypass capacitor should be placed between each V_{CC} pin and GND. Each capacitor should be placed as close as possible to the SN74CBT3244 device.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in *Electrical Characteristics*
   - Inputs and outputs are overvoltage tolerant, which allows them to go as high as 5.5 V at any valid V_{CC}
2. Recommended output conditions:
   - Load currents must not exceed ±64 mA per channel
3. Frequency selection criterion:
   - Added trace resistance or capacitance can reduce maximum frequency capability; use layout practices as directed in *Layout Guidelines*

Product Folder Links: *SN74CBT3244*

Typical Application (continued)
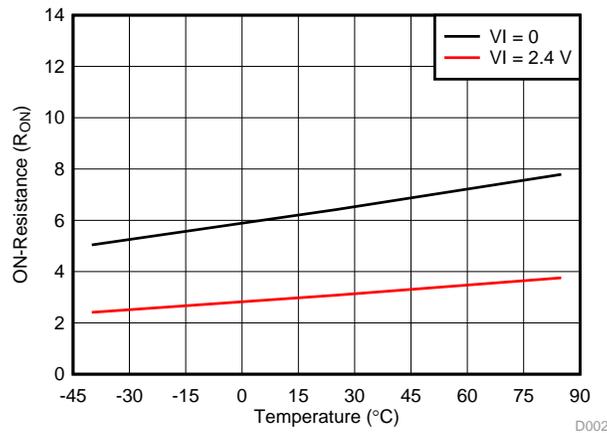
9.2.3 Application Curve

Figure 5. ON-Resistance (R_{on}) Variation vs Temperature

(1) Note device variation mentioned in *Electrical Characteristics*

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Absolute Maximum Ratings* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace, which results in the reflection. Not all PCB traces can be straight; therefore, some traces must turn corners. Figure 6 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.
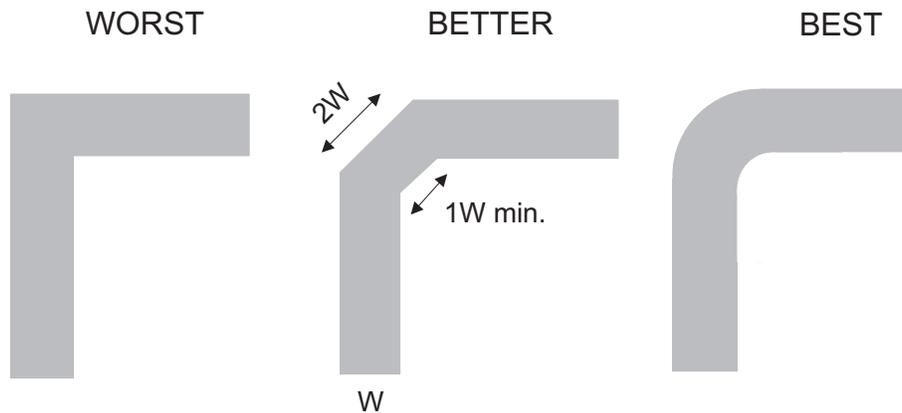
11.2 Layout Example

WORST   BETTER   BEST

2W

1W min.

W

Figure 6. Trace Example

Product Folder Links: *SN74CBT3244*

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:
- *Implications of Slow or Floating CMOS Inputs*, SCBA004
- *Selecting the Right Texas Instruments Signal Switch*, SZZA030

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

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All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CBT3244DBQR	Obsolete	Production	SSOP (DBQ) | 20	-	-	Call TI	Call TI	-40 to 85	CBT3244
SN74CBT3244DBR	NRND	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU244
SN74CBT3244DBR.A	NRND	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU244
SN74CBT3244DGVR	NRND	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU244
SN74CBT3244DGVR.A	NRND	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU244
SN74CBT3244DW	NRND	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3244
SN74CBT3244DW.A	NRND	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3244
SN74CBT3244DWR	NRND	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3244
SN74CBT3244DWR.A	NRND	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3244
SN74CBT3244PW	NRND	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU244
SN74CBT3244PW.A	NRND	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU244
SN74CBT3244PWR	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	CU244
SN74CBT3244RGYR	Obsolete	Production	VQFN (RGY) | 20	-	-	Call TI	Call TI	-40 to 85	CU244

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74CBT3244DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBT3244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3244DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74CBT3244DGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74CBT3244DWR	SOIC	DW	20	2000	356.0	356.0	45.0

PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBT3244DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CBT3244DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CBT3244PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74CBT3244PW.A	PW	TSSOP	20	70	530	10.2	3600	3.5

DBQ (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

20   11

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

Pin 1
Index Area

1   10

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.035 (0,89)
0.016 (0,40)

4073301−3/H   10/2008

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
        D. Falls within JEDEC MO−137 variation AD.

TEXAS INSTRUMENTS
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8.2 TYP
7.4

A

PIN 1 INDEX AREA

1

7.5
6.9
NOTE 3

10

18X 0.65

20

2X
5.85

11

20X 0.38
0.22

⊕ 0.1 Ⓜ C A B

B

5.6
5.0
NOTE 4

C

◠ 0.1 C

SEATING
PLANE

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0°-8°

0.95
0.55

2 MAX

0.05 MIN
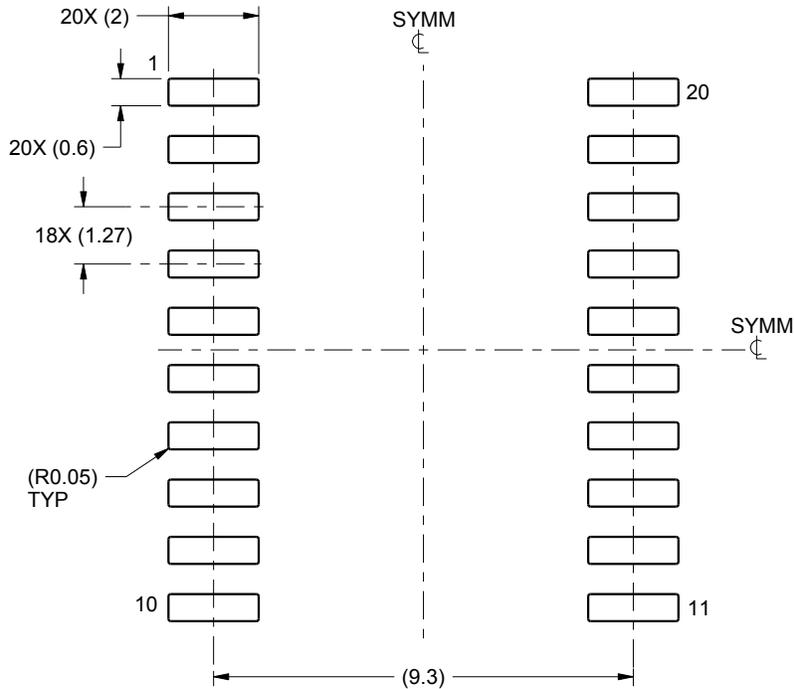
DETAIL A
TYPICAL

4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

20X (1.85)

1

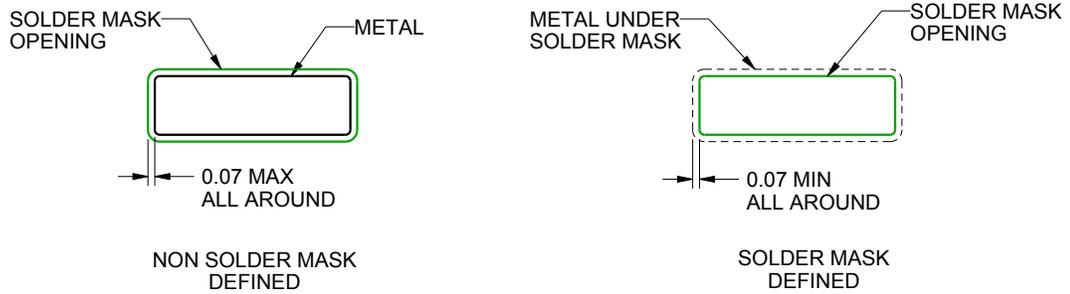20X (0.45)

(R0.05) TYP

20

SYMM

18X (0.65)

SYMM

10

11

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

**SOLDER MASK DETAILS**

4214851/B   08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DB0020A

SSOP - 2 mm max height

20X (1.85)

SYMM

(R0.05) TYP

1

20

20X (0.45)

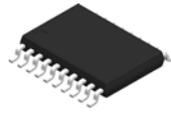SYMM

18X (0.65)

10

11

(7)
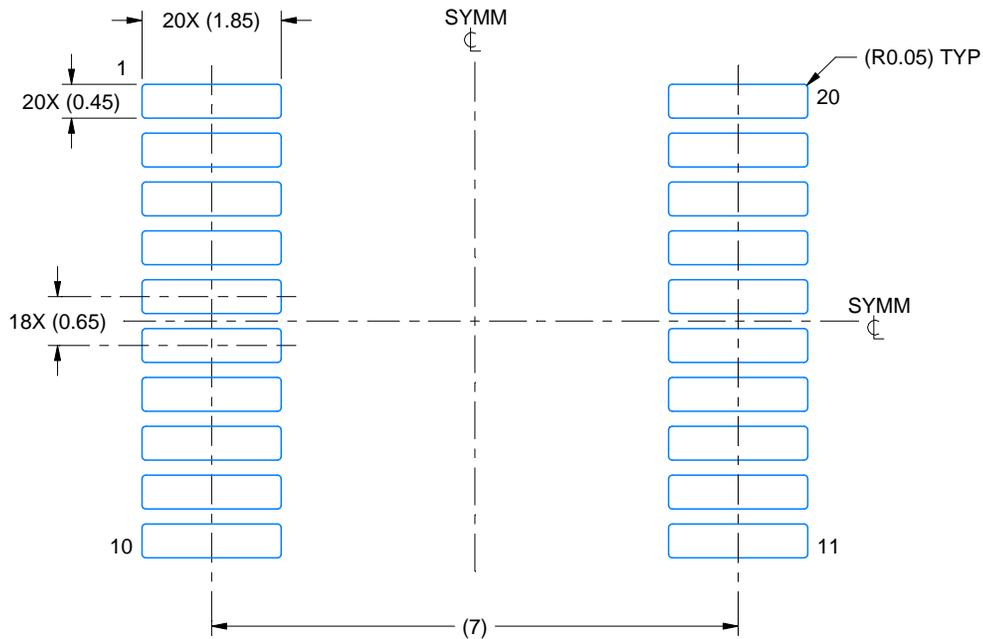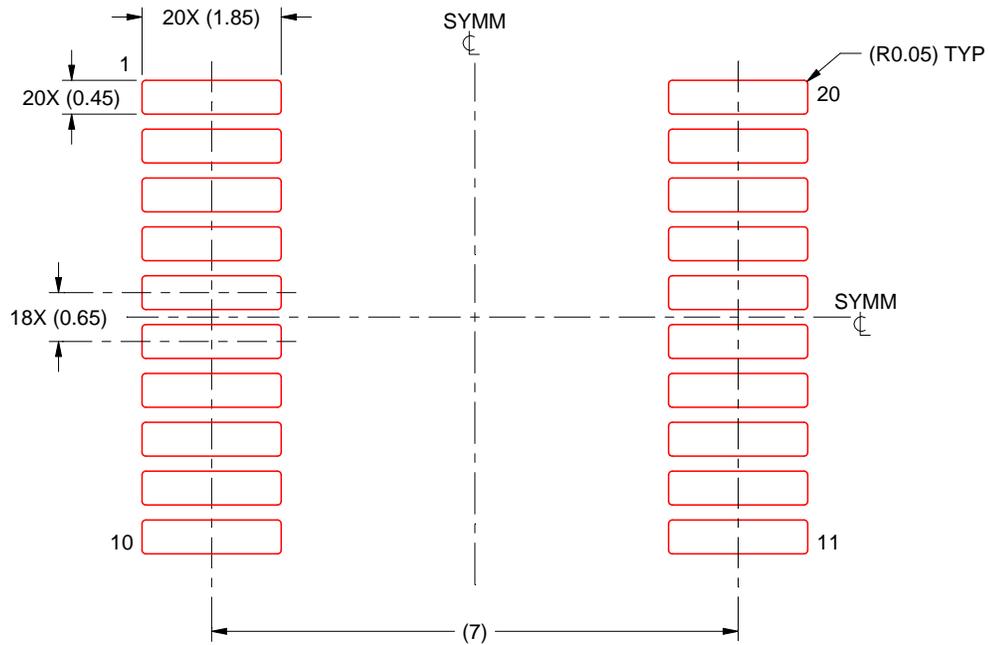
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B   08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
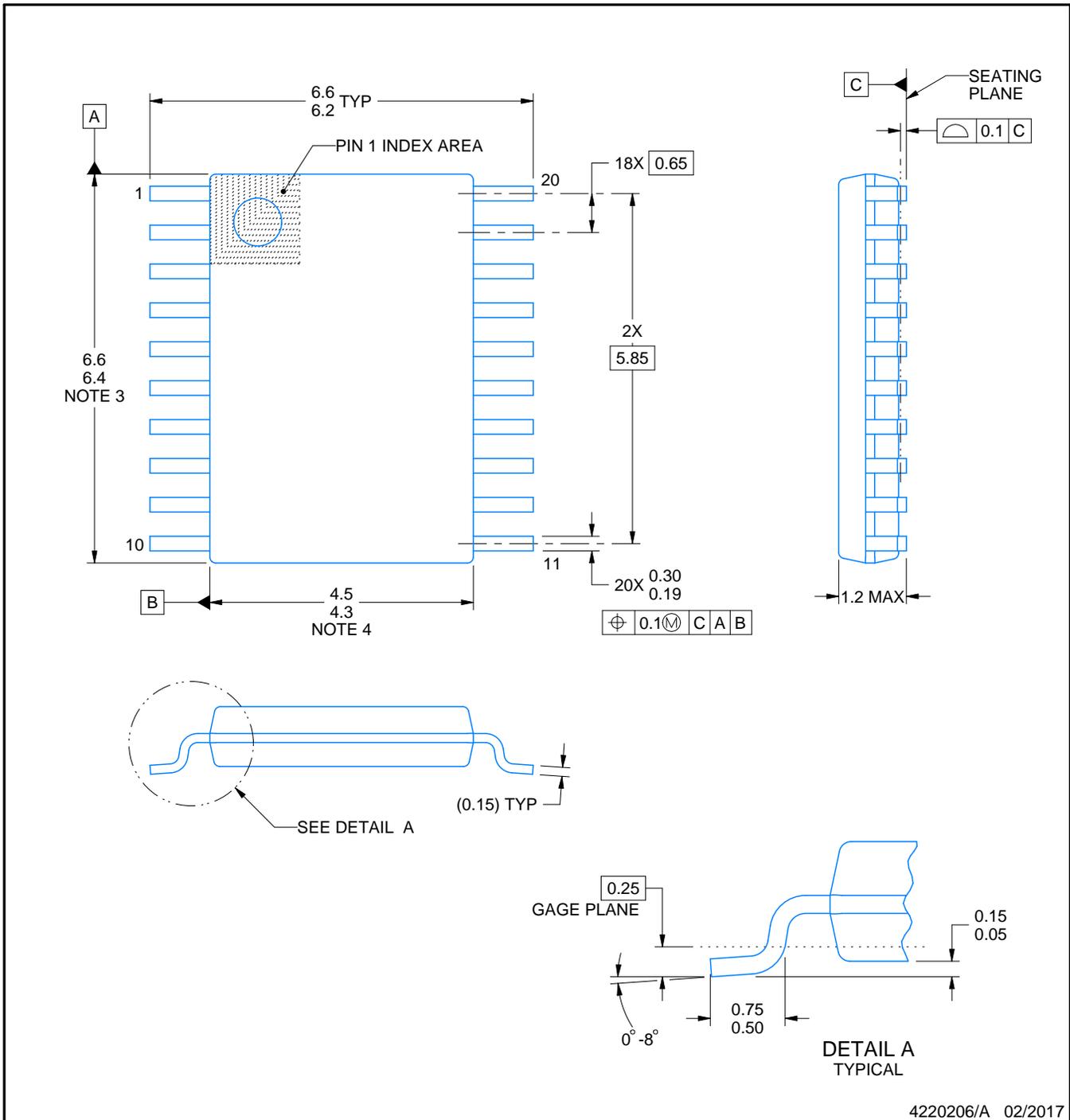
DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

0,40

0,23
0,13

⊕ | 0,07 Ⓜ

24   13

0,16 NOM

4,50   6,60
4,30   6,20

Gage Plane

0,25

0°−8°

0,75
0,50

1   12

A

Seating Plane

0,15
0,05

⌓ | 0,08

1,20 MAX

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00
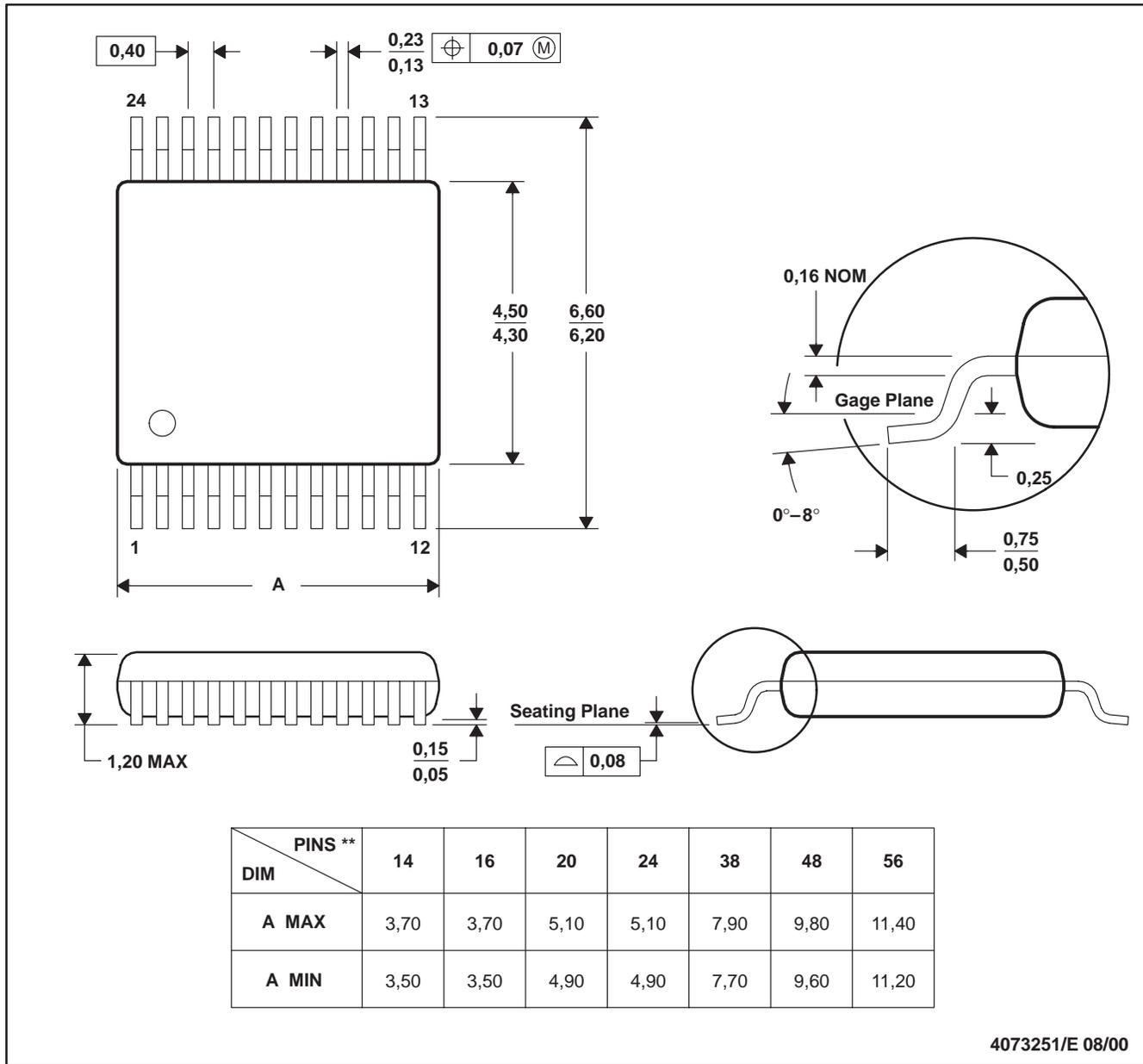
NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
        D. Falls within JEDEC: 24/48 Pins – MO-153
                                 14/16/20/56 Pins – MO-194

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4225264/A

10.63 / 9.97 TYP

A

PIN 1 ID
AREA

1

18X 1.27

20

13.0 / 12.6
NOTE 3

2X
11.43

10

11

B

7.6 / 7.4
NOTE 4

20X 0.51 / 0.31

⊕ 0.25 Ⓜ C A B

C

SEATING PLANE

⌓ 0.1 C

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

0.25
GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL
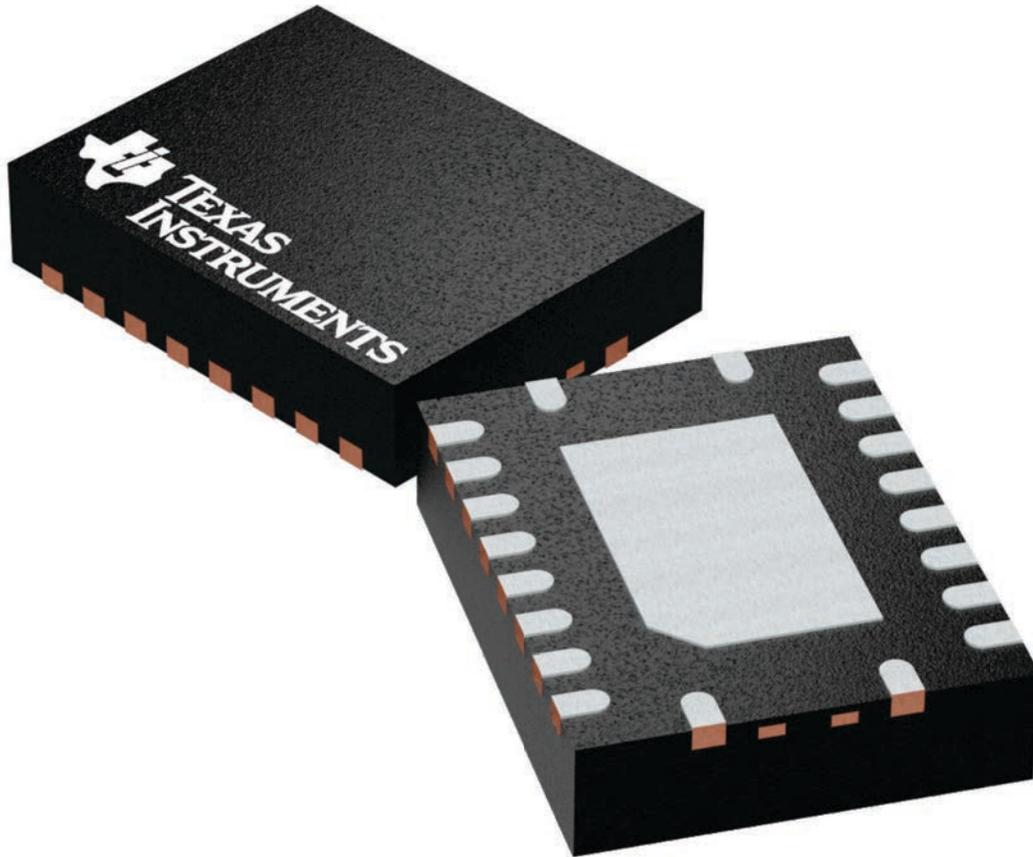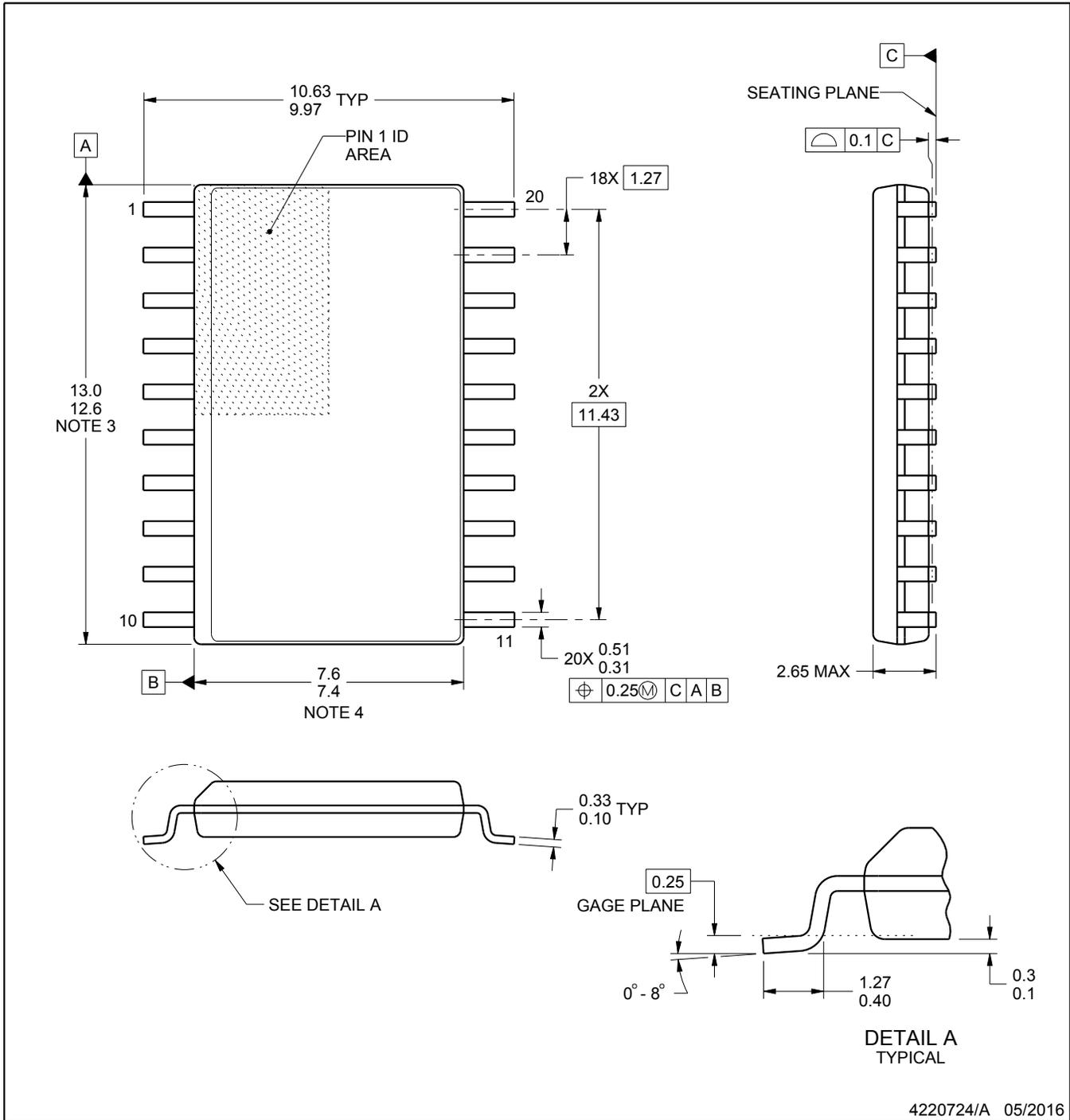
4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
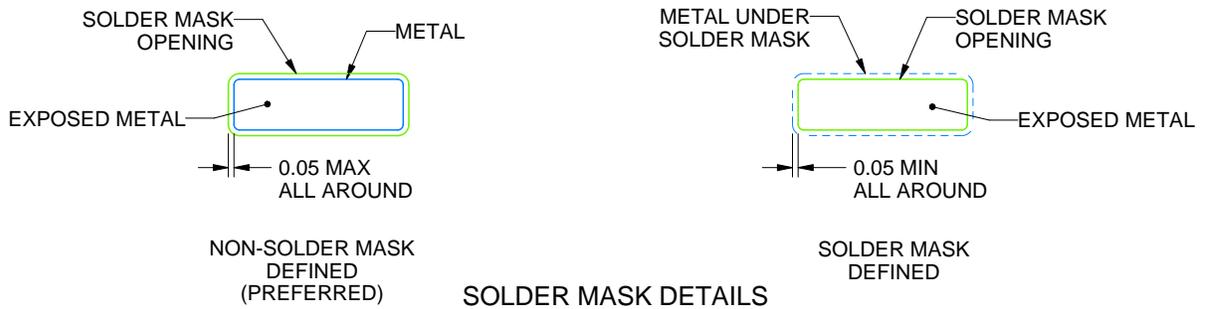5. Reference JEDEC registration MS-013.

20X (2)

SYMM

1

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

10

11

(9.3)
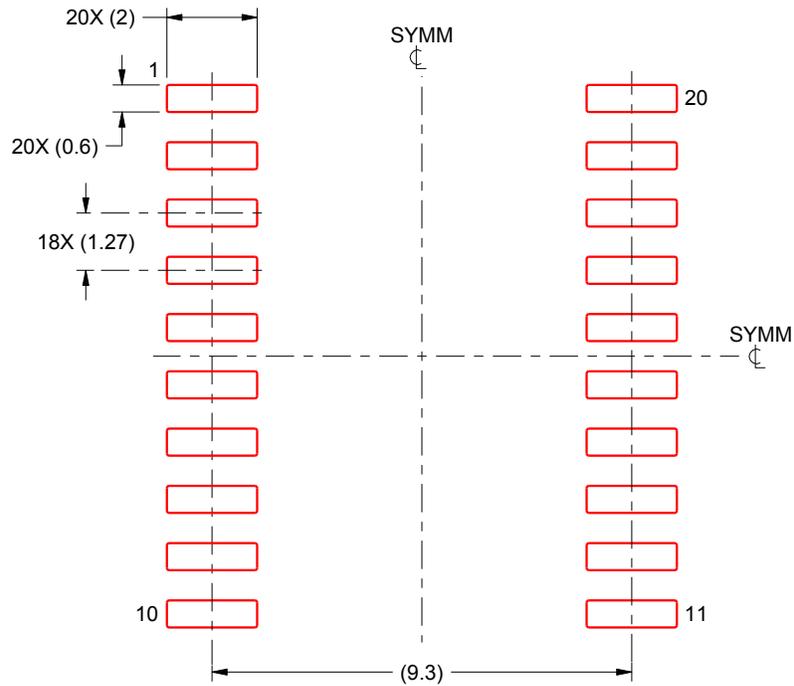
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

SMALL OUTLINE PACKAGE

A

6.6
6.2 TYP

PIN 1 INDEX AREA

1

20

18X 0.65

2X
5.85

6.6
6.4
NOTE 3

10

11

20X 0.30
0.19

B

4.5
4.3
NOTE 4

⊕ 0.1Ⓜ C A B

C

SEATING
PLANE

⬡ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0.15
0.05

0°-8°

0.75
0.50

DETAIL A
TYPICAL

4220206/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

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20X (1.5)

SYMM

(R0.05) TYP

1

20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND
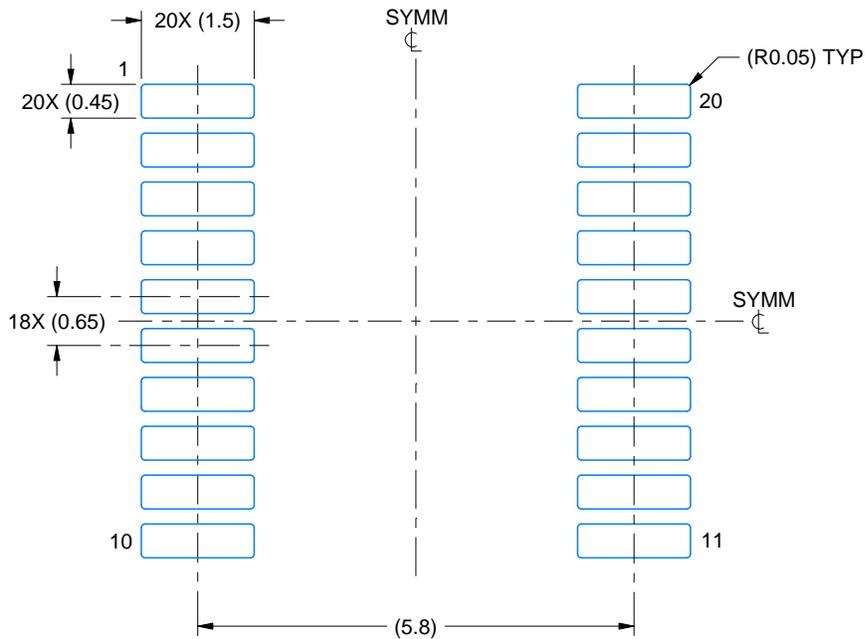
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PW0020A
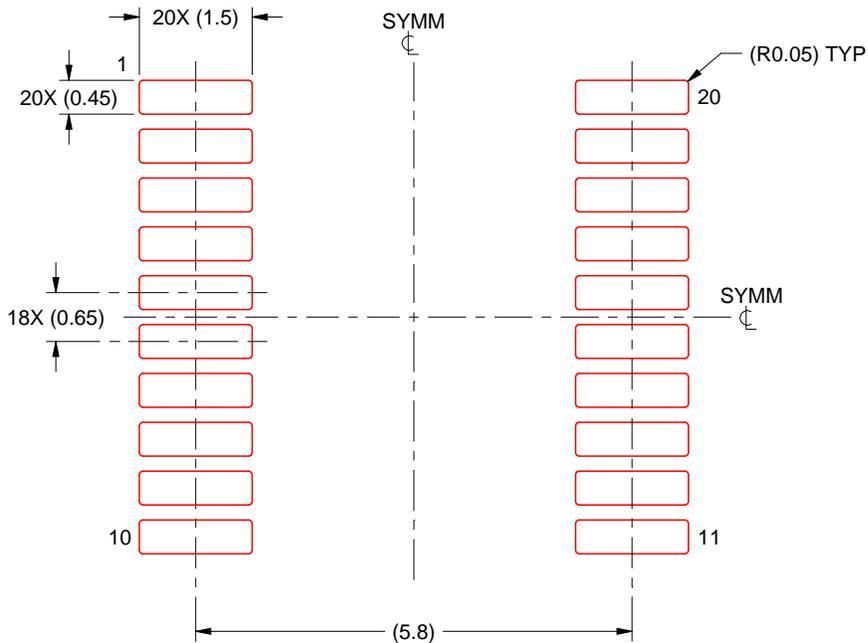
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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