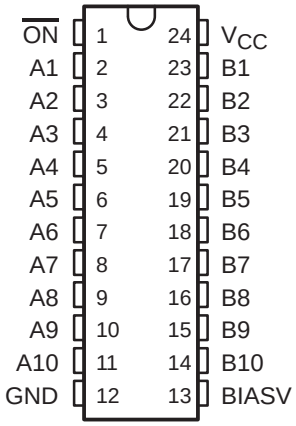
- **Member of the Texas Instruments Widebus™ Family**
- **Undershoot Protection for Off-Isolation on A and B Ports Up to −2 V**
- **B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot-Plugging**
- **Supports PCI Hot Plug**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT6800C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT6800C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

description/ordering information (continued)

The SN74CBT6800C is a 10-bit bus switch with a single output-enable ($\overline{ON}$) input. When $\overline{ON}$ is low, the 10-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{ON}$ is high, the 10-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. The B port is precharged to BIASV through the equivalent of a 10-kΩ resistor when $\overline{ON}$ is high, or if the device is powered down (V_{CC} = 0 V).

During insertion (or removal) of a card into (or from) an active bus, the card's output voltage may be close to GND. When the connector pins make contact, the card's parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method will ensure that any glitch produced by insertion (or removal) of the card will not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{ON}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

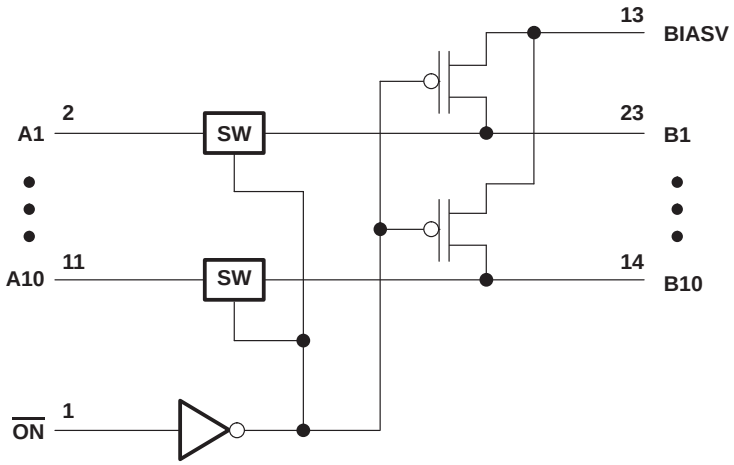
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBT6800CDW	CBT6800C
		Tape and reel	SN74CBT6800CDWR	
	SSOP − DB	Tube	SN74CBT6800CDB	CT6800C
		Tape and reel	SN74CBT6800CDBR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT6800CDBQR	CBT6800C
	TSSOP − PW	Tube	SN74CBT6800CPW	CT6800C
		Tape and reel	SN74CBT6800CPWR	
	TVSOP − DGV	Tape and reel	SN74CBT6800CDGVR	CT6800C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

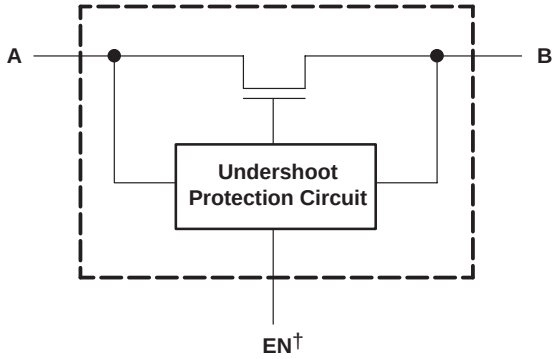
FUNCTION TABLE

INPUT $\overline{ON}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Bias supply voltage range, BIASV . . . . . −0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . . −0.5 V to 7 V
Control input clamp current, I_{IK} (V_{IN} < 0) . . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0) . . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . . ±128 mA
Continuous current through V_{CC} or GND terminals . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DB package . . . . . 63°C/W
DBQ package . . . . . 61°C/W
DGV package . . . . . 86°C/W
DW package . . . . . 46°C/W
PW package . . . . . 88°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Bias supply voltage	0	V_{CC}	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. BIASV is a supply voltage, not a control input.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
$V_{O(USP)}$‡		V_{CC} = BIASV = 5 V,	I_I = −10 mA, V_{IN} = V_{CC} or GND,	Switch OFF	3			V
V_O	B port	V_{CC} = 0 V,	BIASV = V_X,	I_O = 0	V_X−0.1		V_X	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_O	B port	V_{CC} = 4.5 V,	BIASV = 2.4 V, V_O= 0,	Switch OFF, V_{IN} = V_{CC} or GND		0.25		mA
I_{OZ}§		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}¶	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				4		pF
$C_{io(OFF)}$	A port	$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		13.5		pF
r_{on}#		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	Ω
				I_O = 30 mA		3	6	Ω
			V_I = 2.4 V,	I_O = −15 mA		5	10	Ω

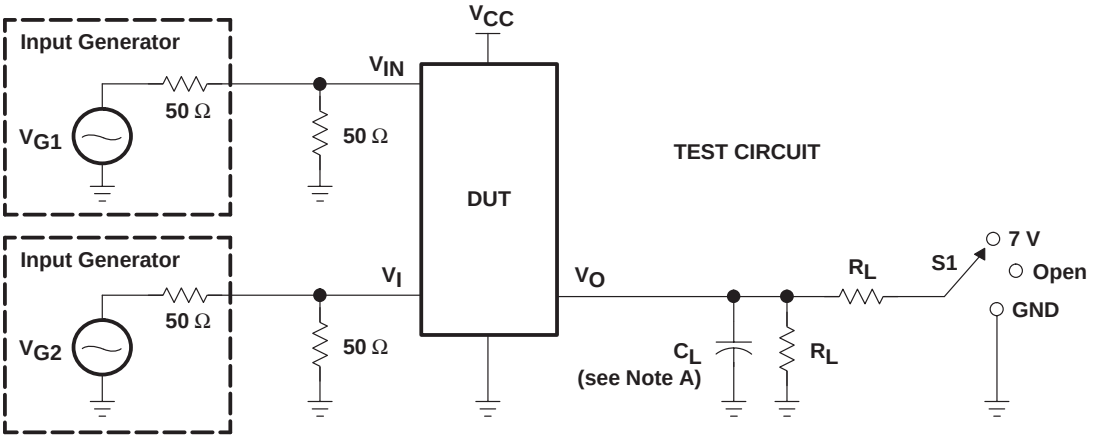
V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
‡ $V_{O(USP)}$ = A-port undershoot static protection.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.
¶ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

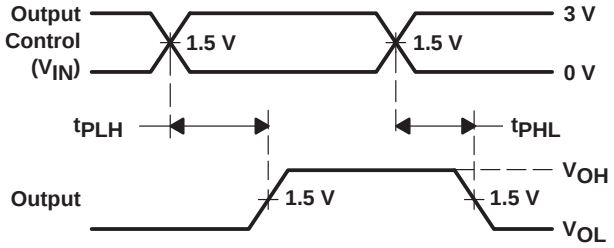
PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}‖		A or B	B or A		0.24		0.15	ns
t_{PZH}	BIASV = GND	$\overline{OE}$	A or B		6.2	1.5	5.9	ns
t_{PZL}	BIASV = 3 V				6.2	1.5	5.9	
t_{PHZ}	BIASV = GND	$\overline{OE}$	A or B		5.6	1.5	6.2	ns
t_{PLZ}	BIASV = 3 V				5.6	1.5	6.2	

‖ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

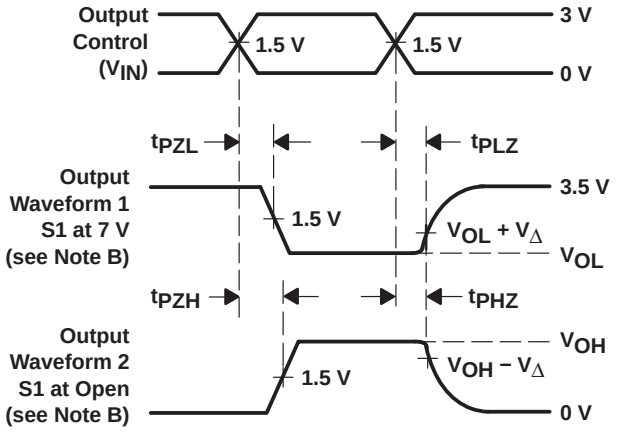
PARAMETER MEASUREMENT INFORMATION



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V	Open	500 Ω	V_{CC} or GND	50 pF	
	4 V	Open	500 Ω	V_{CC} or GND	50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V	7 V	500 Ω	GND	50 pF	0.3 V
	4 V	7 V	500 Ω	GND	50 pF	0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V	Open	500 Ω	V_{CC}	50 pF	0.3 V
	4 V	Open	500 Ω	V_{CC}	50 pF	0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT6800CDGVR	ACTIVE	TVSOP	DGV	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6800C	Samples
SN74CBT6800CDGVRE4	ACTIVE	TVSOP	DGV	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6800C	Samples
SN74CBT6800CDWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT6800C	Samples
SN74CBT6800CPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6800C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

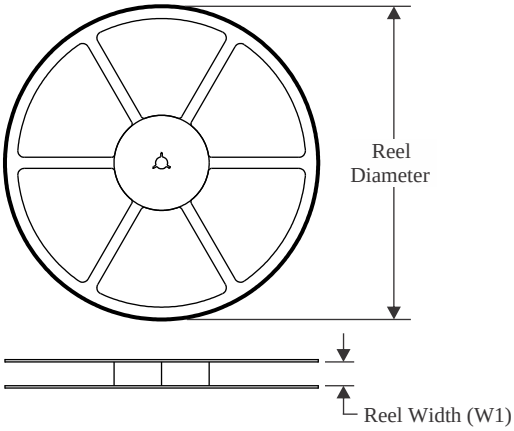
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

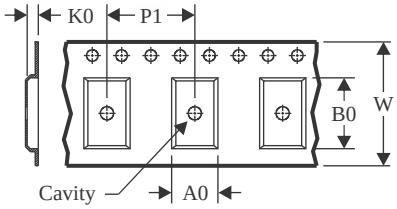
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

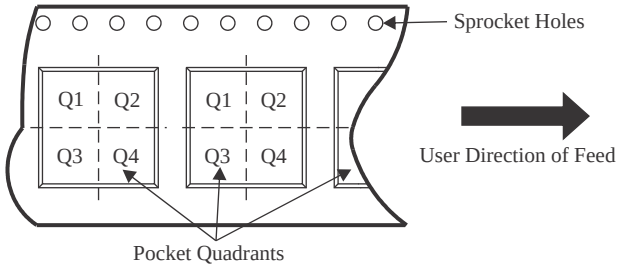


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

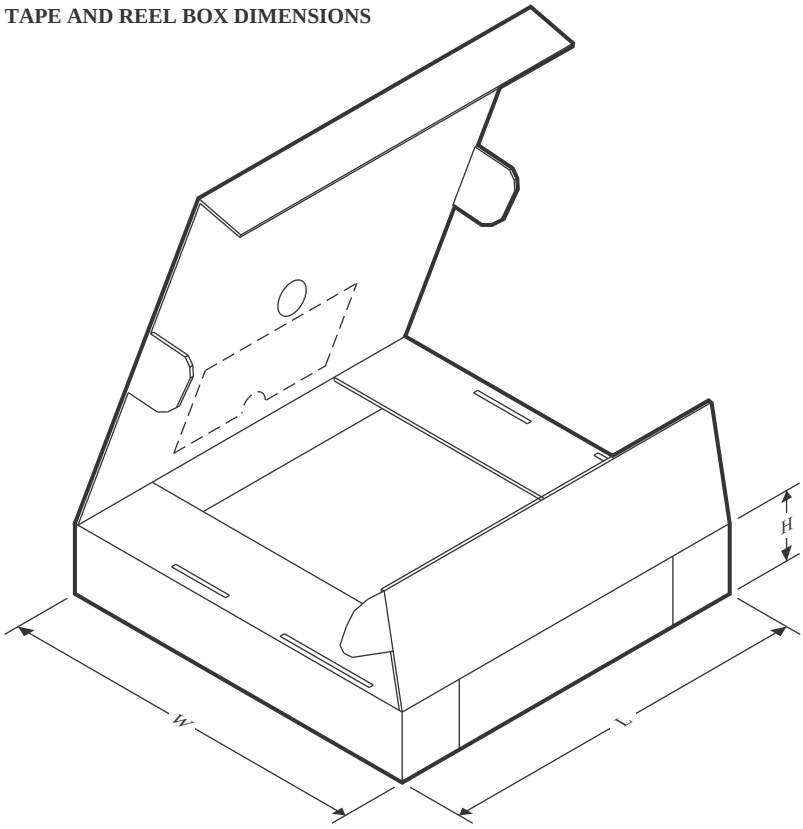
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT6800CDGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBT6800CDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBT6800CPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

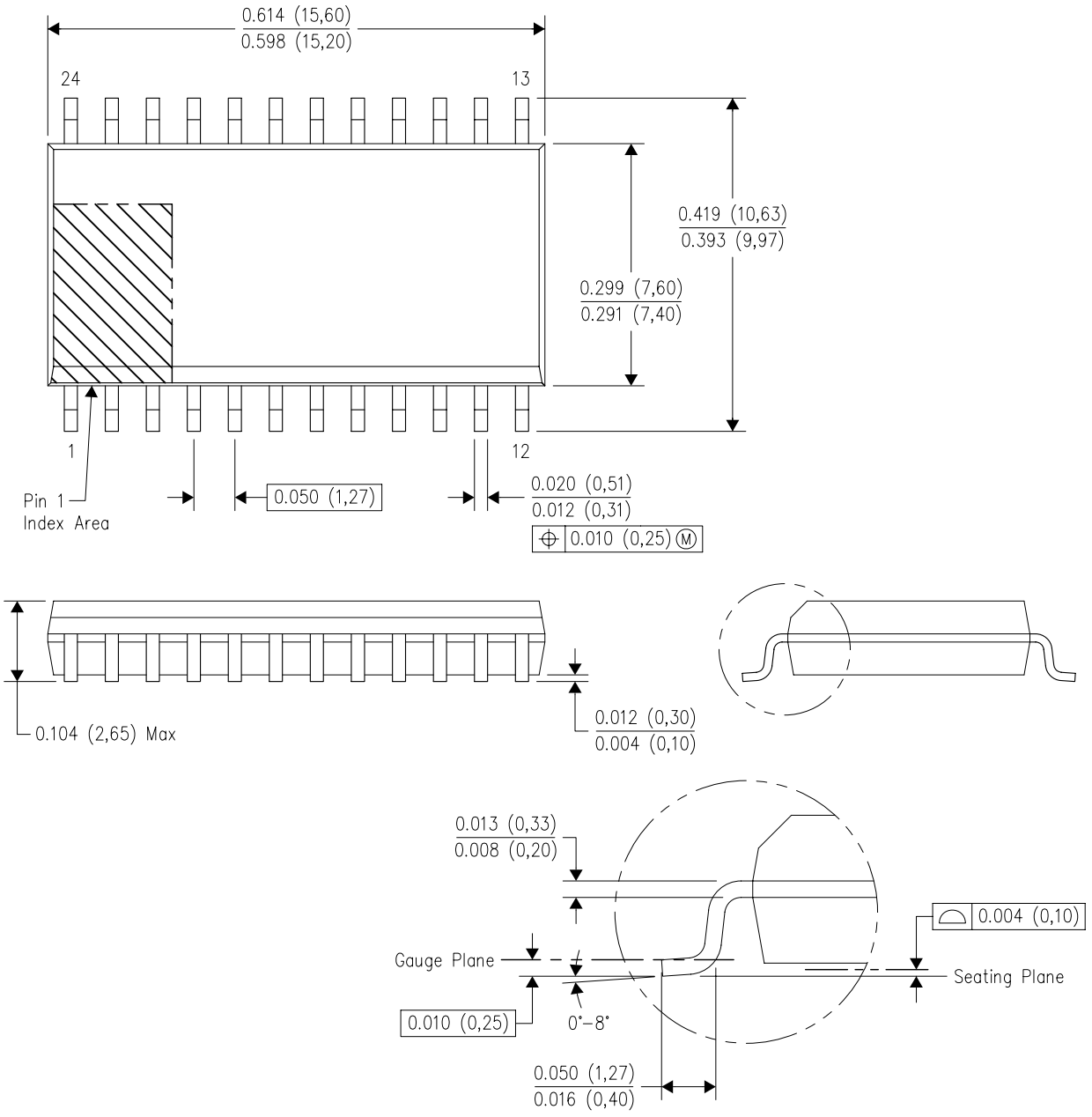
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT6800CDGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
SN74CBT6800CDWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74CBT6800CPWR	TSSOP	PW	24	2000	367.0	367.0	38.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



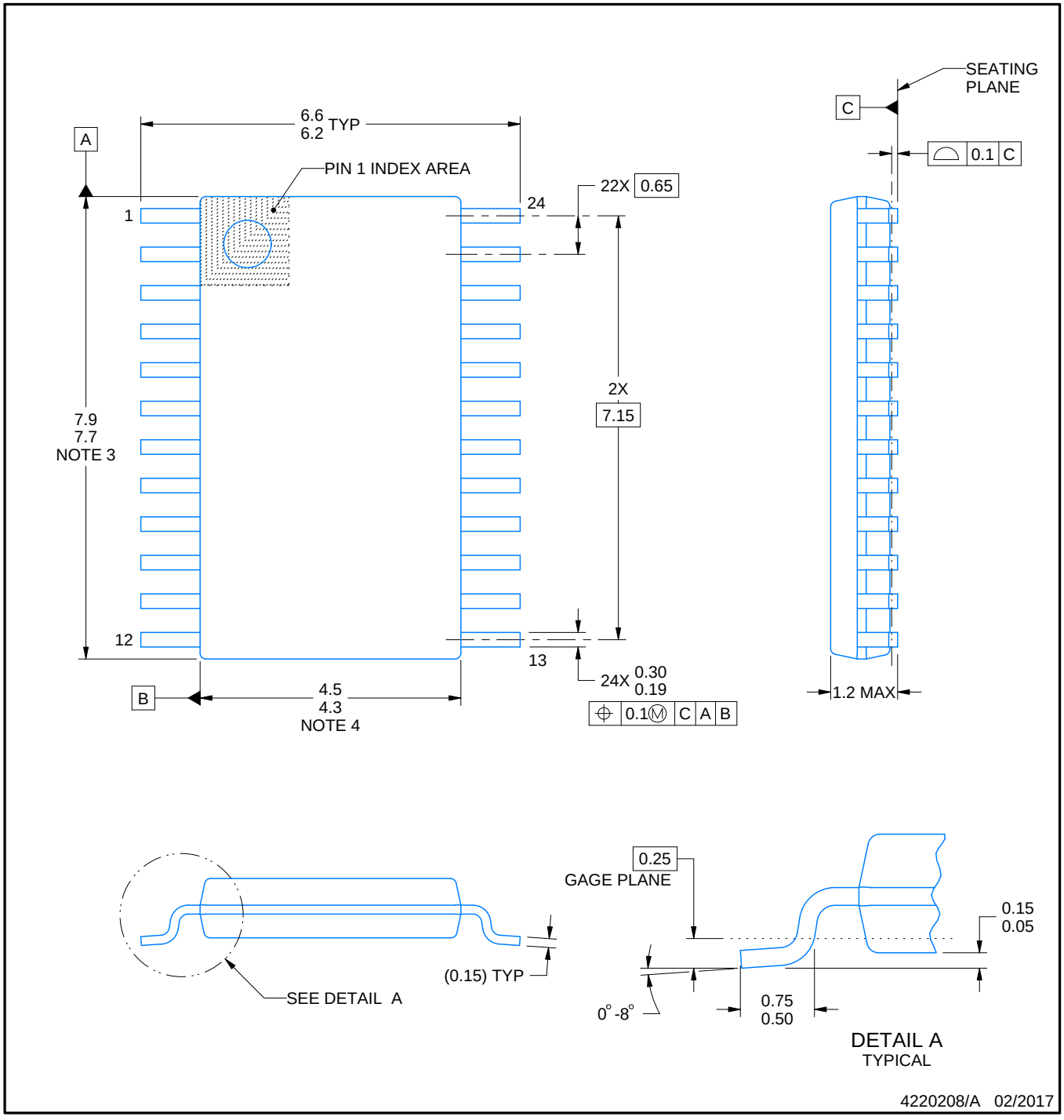
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

PACKAGE OUTLINE

PW0024A

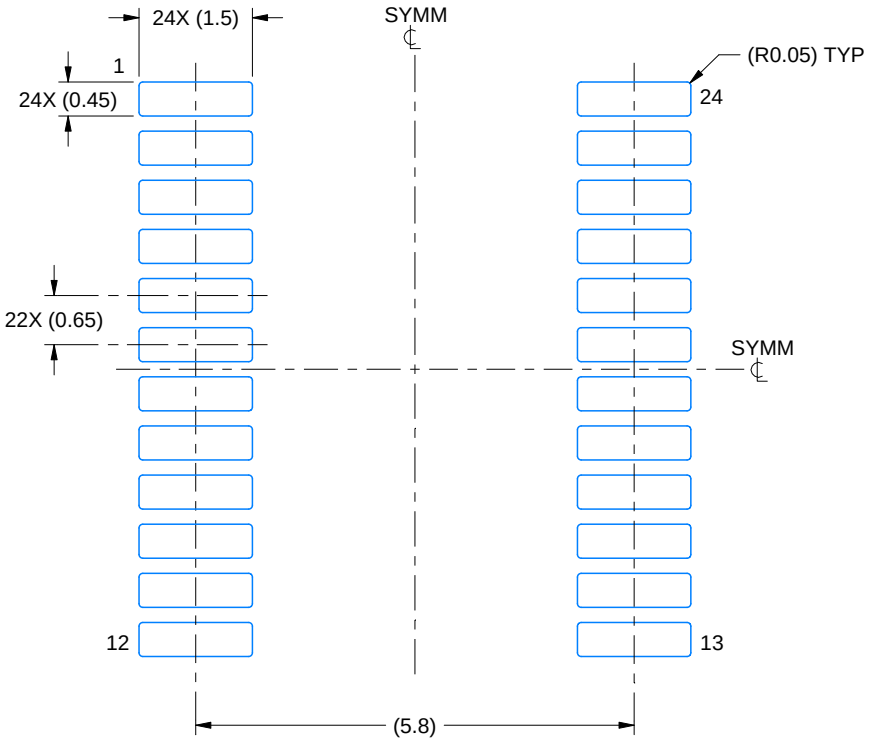
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

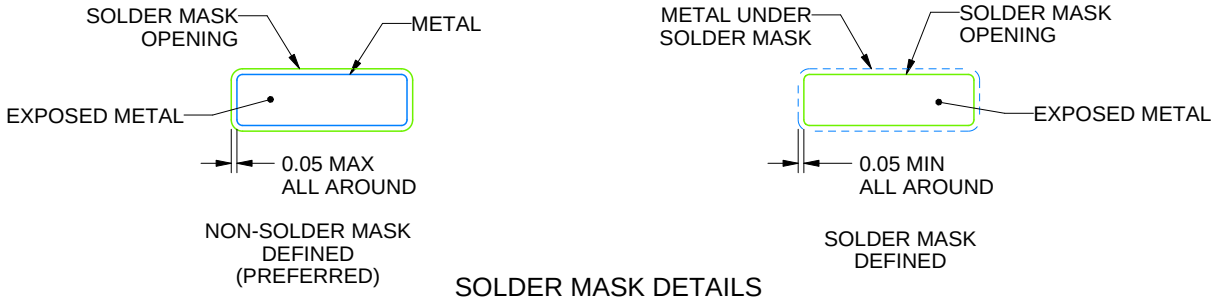


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

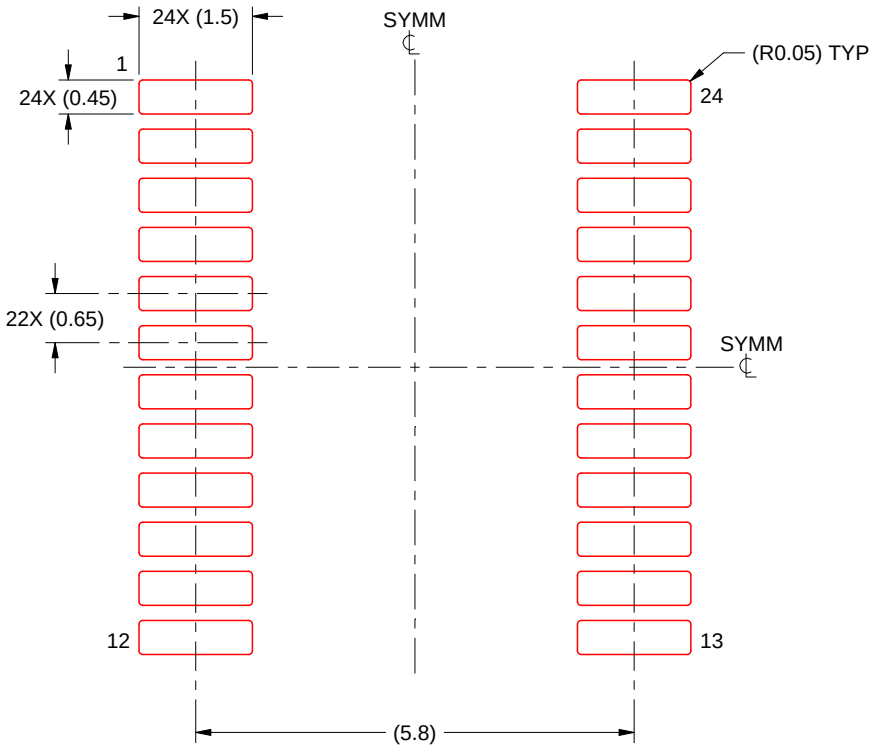


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

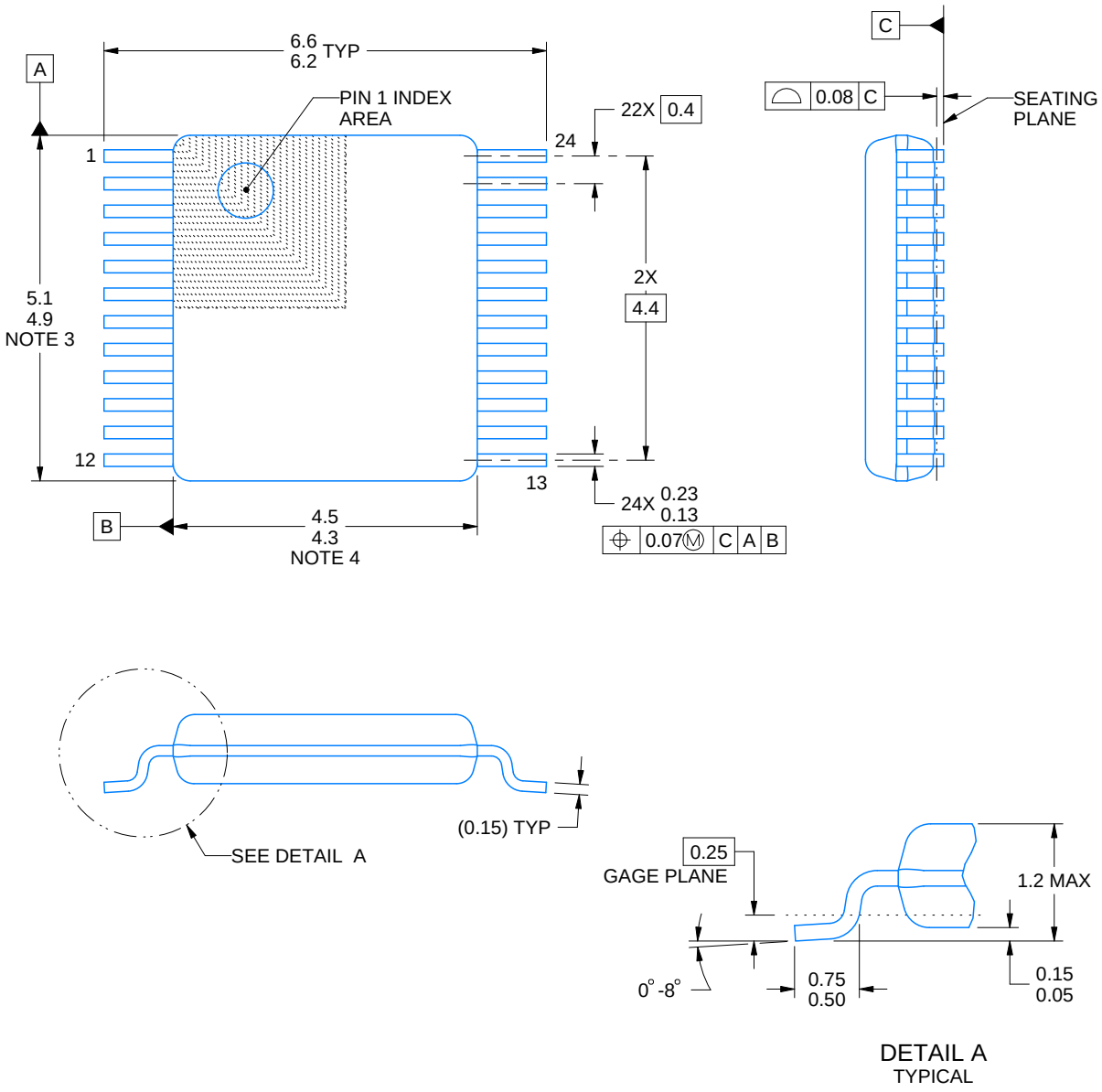
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGV0024A

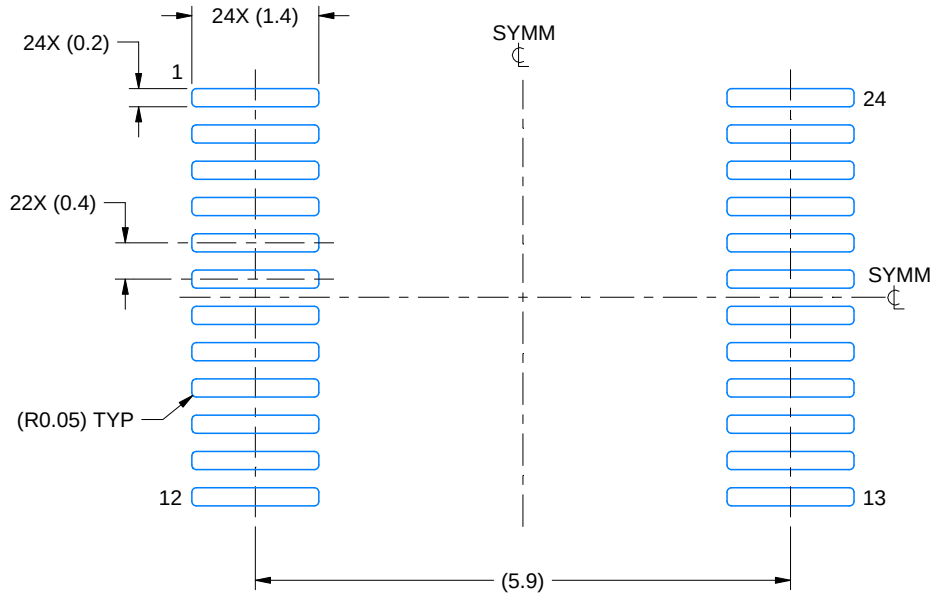
TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

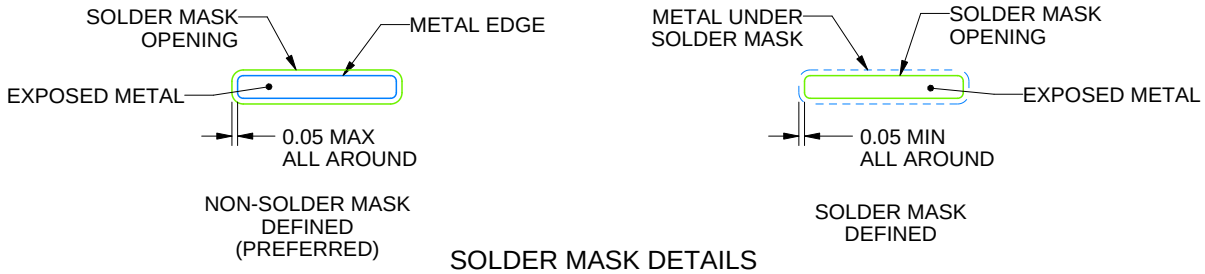


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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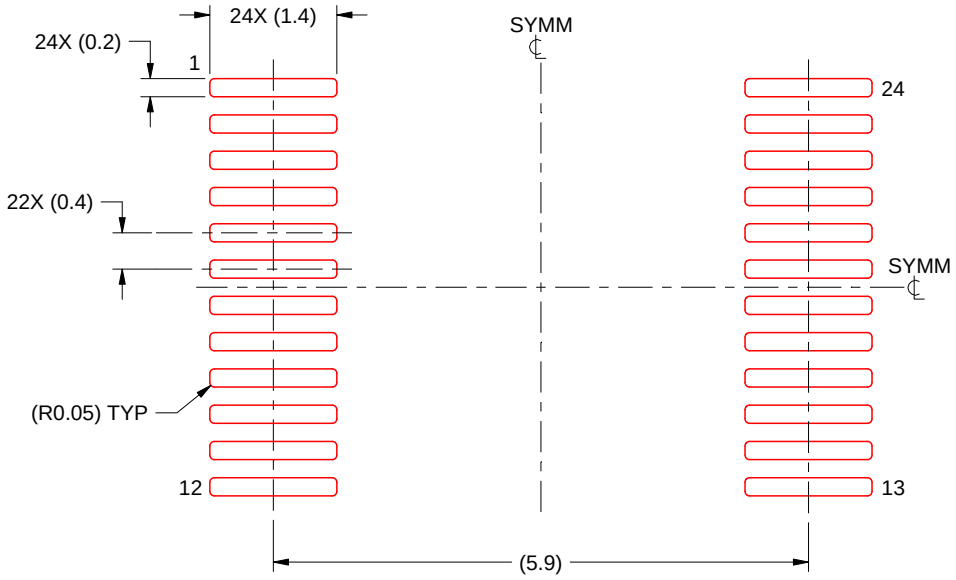
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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