

SN54F573, SN74F573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDFS011A – MARCH 1987 – REVISED OCTOBER 1993

- Eight Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

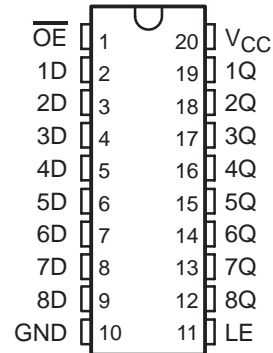
The eight latches of the 'F573 are transparent D-type latches. While the latch enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

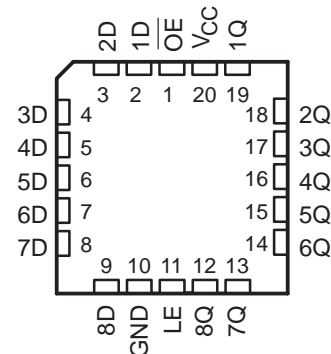
The output enable (\overline{OE}) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54F573 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74F573 is characterized for operation from 0°C to 70°C .

SN54F573 . . . J PACKAGE
SN74F573 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F573 . . . FK PACKAGE
(TOP VIEW)



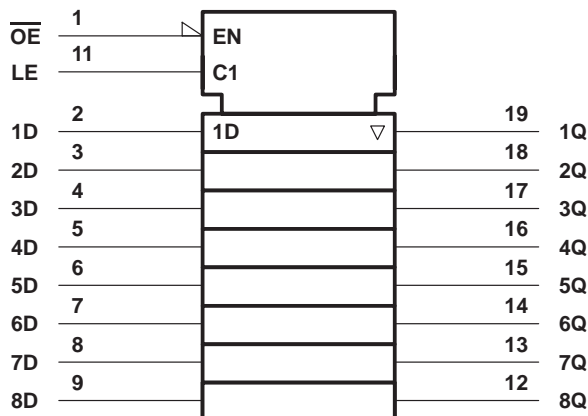
FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

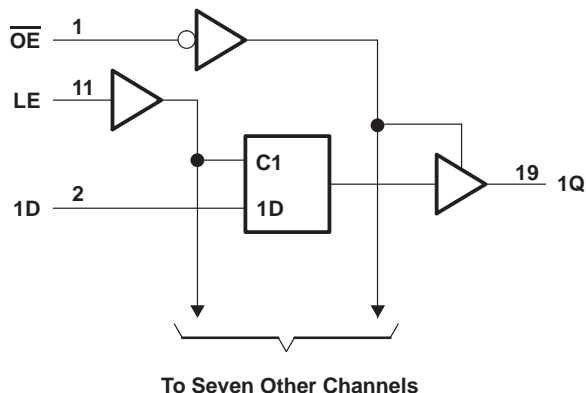
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-1.2 V to 7 V
Input current range	-30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage range applied to any output in the high state	-0.5 V to V_{CC}
Current into any output in the low state: SN54F573	40 mA
SN74F573	48 mA
Operating free-air temperature range: SN54F573	-55°C to 125°C
SN74F573	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F573			SN74F573			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current			-3			-3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F573			SN74F573			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 V$,	$I_I = -18 mA$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 V$	$I_{OH} = -1 mA$	2.5	3.4		2.5	3.4		V
		$I_{OH} = -3 mA$	2.4	3.3		2.4	3.3		
V_{OL}	$V_{CC} = 4.75 V$,	$I_{OH} = -1 mA$ to $-3 mA$				2.7			V
		$V_{CC} = 4.5 V$	$I_{OL} = 20 mA$		0.3	0.5			
		$I_{OL} = 24 mA$				0.35	0.5		
I_{OZH}	$V_{CC} = 5.5 V$,	$V_O = 2.7 V$			50			50	μA
I_{OZL}	$V_{CC} = 5.5 V$,	$V_O = 0.5 V$			-50			-50	μA
I_I	$V_{CC} = 5.5 V$,	$V_I = 7 V$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 V$,	$V_I = 2.7 V$			20			20	μA
I_{IL}	$V_{CC} = 5.5 V$,	$V_I = 0.5 V$			-0.6			-0.6	mA
I_{OS}^\ddagger	$V_{CC} = 5.5 V$,	$V_O = 0$	-60		-150	-60		-150	mA
I_{CCZ}	$V_{CC} = 5.5 V$,	See Note 2		38	55		38	55	mA

† All typical values are at $V_{CC} = 5 V$, $T_A = 25^\circ C$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CCZ} is measured with \overline{OE} at 4.5 V and all other inputs grounded.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		$V_{CC} = 5 V$, $T_A = 25^\circ C$		SN54F573		SN74F573		UNIT
		'F573						
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	6		6		6		ns
t_{su}	Setup time, data before LE↓	2		2		2		ns
t_h	Hold time, data after LE↓	3		3		3		ns

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 V$, $C_L = 50 pF$, $R_L = 500 \Omega$, $T_A = 25^\circ C$			$V_{CC} = 4.5 V$ to $5.5 V$, $C_L = 50 pF$, $R_L = 500 \Omega$, $T_A = \text{MIN to MAX}^\S$				UNIT
			'F573			SN54F573		SN74F573		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	4.9	7	1.5	9	2.2	8	ns
t_{PHL}			1.2	3.3	5	1	8	1.2	6	
t_{PLH}	LE	Q	4.2	8.6	11.5	3.7	13.5	4.2	13	ns
t_{PHL}			2.2	4.8	7	1.5	9	2.2	8	
t_{PZH}	\overline{OE}	Q	1.2	4.6	11	1	13	1.2	12	ns
t_{PZL}			1.2	5.2	7.5	1	10	1.2	8.5	
t_{PHZ}	\overline{OE}	Q	1.2	4.1	6.5	1	8.5	1.2	7.5	ns
t_{PLZ}			1.2	3.4	6	1	7	1.2	6	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74F573DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	F573	
SN74F573DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F573	Samples
SN74F573N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74F573N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

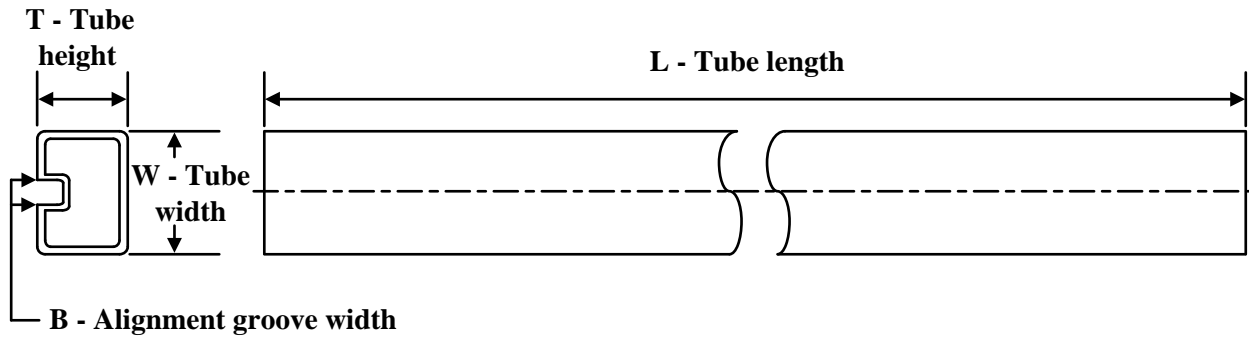

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F573DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F573DWR	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74F573N	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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