

SN74LV2T74 Dual D-Type Flip-Flop With Integrated Translation

1 Features

- Wide operating range of 1.8 V to 5.5 V
- Single-supply voltage translator (refer to LVxT Enhanced Input Voltage):
 - Up translation:
 - 1.2 V to 1.8 V
 - 1.5 V to 2.5 V
 - 1.8 V to 3.3 V
 - 3.3 V to 5.0 V
 - Down translation:
 - 5.0 V, 3.3 V, 2.5 V to 1.8 V
 - 5.0 V, 3.3 V to 2.5 V
 - 5.0 V to 3.3 V
- 5.5-V tolerant input pins
- Supports standard pinouts
- Up to 150 Mbps with 5-V or 3.3-V V_{CC}
- Latch-up performance exceeds 250 mA per JESD 17

2 Applications

- [Convert a momentary switch to a toggle switch](#)
- [Hold a signal during controller reset](#)
- [Input slow edge-rate signals](#)
- [Operate in noisy environments](#)
- Divide a clock signal by two

3 Description

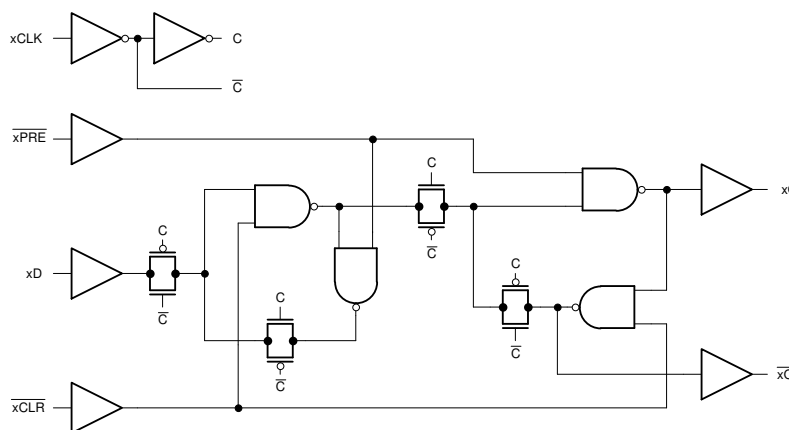
The SN74LV2T74 contains two independent D-type positive-edge-triggered flip-flops. A low level at the preset (\overline{PRE}) input sets the output high. A low level at the clear (\overline{CLR}) input resets the output low. Preset and clear functions are asynchronous and not dependent on the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs (Q, \overline{Q}) on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the input clock (CLK) signal. Following the hold-time interval, data at the data (D) input can be changed without affecting the levels at the outputs (Q, \overline{Q}). The output level is referenced to the supply voltage (V_{CC}) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

The input is designed with a lower threshold circuit to support up translation for lower voltage CMOS inputs (for example, 1.2 V input to 1.8 V output or 1.8 V input to 3.3 V output). In addition, the 5-V tolerant input pins enable down translation (for example, 3.3 V to 2.5 V output).

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE (NOM) ⁽³⁾
SN74LV2T74	BQA (WQFN, 14)	3 mm × 2.5 mm	3 mm × 2.5 mm
	PW (TSSOP, 14)	5 mm × 6.4 mm	5 mm × 4.4 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Simplified Logic Diagram (Positive Logic)



Table of Contents

1 Features	1	6.15 Typical Characteristics.....	9
2 Applications	1	7 Parameter Measurement Information	12
3 Description	1	8 Detailed Description	13
4 Revision History	2	8.1 Overview.....	13
5 Pin Configuration and Functions	3	8.2 Functional Block Diagram.....	13
6 Specifications	4	8.3 Feature Description.....	13
6.1 Absolute Maximum Ratings.....	4	8.4 Device Functional Modes.....	16
6.2 ESD Ratings.....	4	9 Application and Implementation	17
6.3 Recommended Operating Conditions.....	4	9.1 Application Information.....	17
6.4 Thermal Information.....	5	9.2 Typical Application.....	17
6.5 Electrical Characteristics.....	5	10 Power Supply Recommendations	19
6.6 Timing Characteristics 1.8-V V_{CC}	6	11 Device and Documentation Support	20
6.7 Timing Characteristics 2.5-V V_{CC}	6	11.1 Documentation Support.....	20
6.8 Timing Characteristics 3.3-V V_{CC}	6	11.2 Receiving Notification of Documentation Updates..	20
6.9 Timing Characteristics 5-V V_{CC}	6	11.3 Support Resources.....	20
6.10 Switching Characteristics 1.8-V V_{CC}	7	11.4 Trademarks.....	20
6.11 Switching Characteristics 2.5-V V_{CC}	7	11.5 Electrostatic Discharge Caution.....	20
6.12 Switching Characteristics 3.3-V V_{CC}	8	11.6 Glossary.....	20
6.13 Switching Characteristics 5-V V_{CC}	8	12 Mechanical, Packaging, and Orderable Information	20
6.14 Noise Characteristics.....	8		

4 Revision History

DATE	REVISION	NOTES
May 2023	*	Initial Release

5 Pin Configuration and Functions

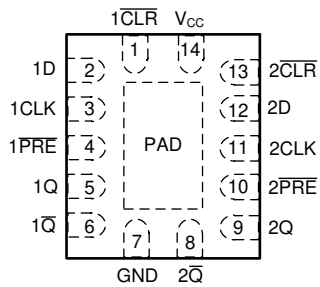


Figure 5-1. BQA Package, 14-Pin WQFN (Top View)

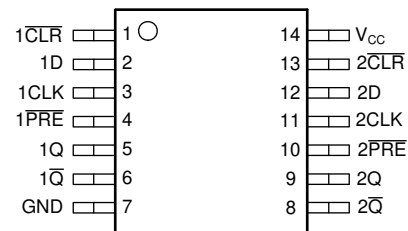


Figure 5-2. PW Package, 14-Pin TSSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1CLR	1	Input	Clear for channel 1, active low
1D	2	Input	Data for channel 1
1CLK	3	Input	Clock for channel 1, rising edge triggered
1PRE	4	Input	Preset for channel 1, active low
1Q	5	Output	Output for channel 1
1Q	6	Output	Inverted output for channel 1
GND	7	—	Ground
2Q	8	Output	Inverted output for channel 2
2Q	9	Output	Output for channel 2
2PRE	10	Input	Preset for channel 2, active low
2CLK	11	Input	Clock for channel 2, rising edge triggered
2D	12	Input	Data for channel 2
2CLR	13	Input	Clear for channel 2, active low
V _{CC}	14	—	Positive supply
Thermal Pad ⁽¹⁾		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply

(1) BQA package only.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range	-0.5	7	V	
V _I	Input voltage range ⁽²⁾	-0.5	7	V	
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	7	V	
V _O	Output voltage range ⁽²⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < -0.5 V		-20	mA
I _{OK}	Output clamp current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V		±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±25	mA
	Continuous output current through V _{CC} or GND			±50	mA
T _{stg}	Storage temperature	-65	150	°C	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	MIN	MAX	UNIT
V _{CC}	Supply voltage		1.6	5.5	V
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 2 V	1.1		V
		V _{CC} = 2.25 V to 2.75 V	1.28		
		V _{CC} = 3 V to 3.6 V	1.45		
		V _{CC} = 4.5 V to 5.5 V	2		
V _{IL}	Low-Level input voltage	V _{CC} = 1.65 V to 2 V		0.5	V
		V _{CC} = 2.25 V to 2.75 V		0.65	
		V _{CC} = 3 V to 3.6 V		0.75	
		V _{CC} = 4.5 V to 5.5 V		0.85	
I _O	Output current	V _{CC} = 1.6 V to 2 V		±3	mA
		V _{CC} = 2.25 V to 2.75 V		±7	
		V _{CC} = 3.3 V to 5.0 V		±15	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.6 V to 5.0 V		20	ns/V
T _A	Operating free-air temperature		-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV2T74		UNIT
		BQA (WQFN)	PW (TSSOP)	
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	88.3	151.0	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	90.9	80.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	56.8	94.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	9.9	28.0	°C/W
Y _{JB}	Junction-to-board characterization parameter	56.7	93.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	33.4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	1.65 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	1.65 V to 2 V	1.28	1.7 ⁽¹⁾		1.21			
	I _{OH} = -3 mA	2.25 V to 2.75 V	2	2.4 ⁽¹⁾		1.93			
	I _{OH} = -5.5 mA	3 V to 3.6 V	2.6	3.08 ⁽¹⁾		2.49			
	I _{OH} = -8 mA	4.5 V to 5.5 V	4.1	4.65 ⁽¹⁾		3.95			
V _{OL}	I _{OL} = 50 μA	1.65 V to 5.5 V			0.1			0.1	V
	I _{OL} = 2 mA	1.65 V to 2 V		0.1 ⁽¹⁾	0.2			0.25	
	I _{OL} = 3 mA	2.25 V to 2.75 V		0.1 ⁽¹⁾	0.15			0.2	
	I _{OL} = 5.5 mA	3 V to 3.6 V		0.2 ⁽¹⁾	0.2			0.25	
	I _{OL} = 8 mA	4.5 V to 5.5 V		0.3 ⁽¹⁾	0.3			0.35	
I _I	V _I = 0 V or V _{CC}	0 V to 5.5 V			±0.1			±1	μA
I _{CC}	V _I = 0 V or V _{CC} , I _O = 0; open on loading	1.65 V to 5.5 V			2			20	μA
ΔI _{CC}	One input at 0.3 V or 3.4 V, other inputs at 0 or V _{CC} , I _O = 0	5.5 V			1.35			1.5	mA
	One input at 0.3 V or 1.1 V, other inputs at 0 or V _{CC} , I _O = 0	1.8 V			10			20	μA
C _I	V _I = V _{CC} or GND	5 V			4	10		10	pF
C _O	V _O = V _{CC} or GND	5 V			3				pF
C _{PD} ^{(2) (3)}	No load, F = 1 MHz	5 V			14				pF

(1) Typical value at nearest nominal voltage (1.8 V, 2.5 V, 3.3 V, and 5 V)

(2) C_{PD} is used to determine the dynamic power consumption, per channel.

(3) P_D = V_{CC}² × F_I × (C_{PD} + C_L) where F_I = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

6.6 Timing Characteristics 1.8-V V_{CC}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	
t_W	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ LOW	8		9		nS
t_W	Pulse duration	CLK	8		9		nS
t_{SU}	Setup time before CLK \uparrow	Data	8		9		nS
t_{SU}	Setup time before CLK \uparrow	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive	7		7		nS
t_H	Hold time, data after CLK \uparrow		0.5		0.5		nS

6.7 Timing Characteristics 2.5-V V_{CC}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	
t_W	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ LOW	7		8		nS
t_W	Pulse duration	CLK	7		8		nS
t_{SU}	Setup time before CLK \uparrow	Data	7		8		nS
t_{SU}	Setup time before CLK \uparrow	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive	6		6		nS
t_H	Hold time, data after CLK \uparrow		0.5		0.5		nS

6.8 Timing Characteristics 3.3-V V_{CC}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	
t_W	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ LOW	6		7		nS
t_W	Pulse duration	CLK	6		7		nS
t_{SU}	Setup time before CLK \uparrow	Data	6		7		nS
t_{SU}	Setup time before CLK \uparrow	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive	5		5		nS
t_H	Hold time, data after CLK \uparrow		0.5		0.5		nS

6.9 Timing Characteristics 5-V V_{CC}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	
t_W	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ LOW	5		5		nS
t_W	Pulse duration	CLK	5		5		nS
t_{SU}	Setup time before CLK \uparrow	Data	5		5		nS
t_{SU}	Setup time before CLK \uparrow	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive	3		3		nS
t_H	Hold time, data after CLK \uparrow		0.5		0.5		nS

6.10 Switching Characteristics 1.8-V V_{CC}

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 125^\circ\text{C}$			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
F_{MAX}			$C_L = 15\text{ pF}$	34	53		30			MHz
			$C_L = 50\text{ pF}$	21	32		19			MHz
t_{PLH}	\overline{PRE} or \overline{CLR}	Q or \overline{Q}	$C_L = 15\text{ pF}$	14.8	24.0		1	28.3		nS
t_{PHL}				14.8	24.0		1	28.3		nS
t_{PLH}	CLK	Q or \overline{Q}		13.1	23.2		1	27.3		nS
t_{PHL}				13.1	23.2		1	27.3		nS
t_{PLH}	\overline{PRE} or \overline{CLR}	Q or \overline{Q}	$C_L = 50\text{ pF}$	19.7	30.8		1	35.1		nS
t_{PHL}				19.7	30.8		1	35.1		nS
t_{PLH}	CLK	Q or \overline{Q}		17.9	30.0		1	34.1		nS
t_{PHL}				17.9	30.0		1	34.1		nS

6.11 Switching Characteristics 2.5-V V_{CC}

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 125^\circ\text{C}$			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
F_{MAX}			$C_L = 15\text{ pF}$	52	81		46			MHz
			$C_L = 50\text{ pF}$	33	49		29			MHz
t_{PLH}	\overline{PRE} or \overline{CLR}	Q or \overline{Q}	$C_L = 15\text{ pF}$	9.9	16.0		1	18.9		nS
t_{PHL}				9.9	16.0		1	18.9		nS
t_{PLH}	CLK	Q or \overline{Q}		8.7	15.5		1	18.2		nS
t_{PHL}				8.7	15.5		1	18.2		nS
t_{PLH}	\overline{PRE} or \overline{CLR}	Q or \overline{Q}	$C_L = 50\text{ pF}$	13.1	20.5		1	23.4		nS
t_{PHL}				13.1	20.5		1	23.4		nS
t_{PLH}	CLK	Q or \overline{Q}		12.0	20.0		1	22.8		nS
t_{PHL}				12.0	20.0		1	22.8		nS

6.12 Switching Characteristics 3.3-V V_{CC}

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
F _{MAX}			C _L = 15 pF	80	125		70			MHz
			C _L = 50 pF	50	75		45			MHz
t _{PLH}	PRE or CLR	Q or Q̄	C _L = 15 pF		7.6	12.3	1	14.5		nS
t _{PHL}					7.6	12.3	1	14.5		nS
t _{PLH}	CLK	Q or Q̄			6.7	11.9	1	14		nS
t _{PHL}					6.7	11.9	1	14		nS
t _{PLH}	PRE or CLR	Q or Q̄	C _L = 50 pF		10.1	15.8	1	18		nS
t _{PHL}					10.1	15.8	1	18		nS
t _{PLH}	CLK	Q or Q̄			9.2	15.4	1	17.5		nS
t _{PHL}					9.2	15.4	1	17.5		nS

6.13 Switching Characteristics 5-V V_{CC}

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
F _{MAX}			C _L = 15 pF	130	170		110			MHz
			C _L = 50 pF	90	140		75			MHz
t _{PLH}	PRE or CLR	Q or Q̄	C _L = 15 pF		4.8	7.7	1	9		nS
t _{PHL}					4.8	7.7	1	9		nS
t _{PLH}	CLK	Q or Q̄			4.6	7.3	1	8.5		nS
t _{PHL}					4.6	7.3	1	8.5		nS
t _{PLH}	PRE or CLR	Q or Q̄	C _L = 50 pF		6.3	9.7	1	11		nS
t _{PHL}					6.3	9.7	1	11		nS
t _{PLH}	CLK	Q or Q̄			6.1	9.3	1	10		nS
t _{PHL}					6.1	9.3	1	10		nS

6.14 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.9	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}	-0.8	-0.3		V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}	4.4	5		V
V _{IH(D)}	High-level dynamic input voltage	2.1			V
V _{IL(D)}	Low-level dynamic input voltage			0.5	V

6.15 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

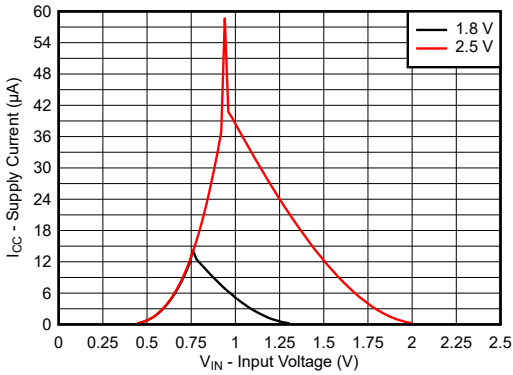


Figure 6-1. Supply Current Across Input Voltage 1.8-V and 2.5-V Supply

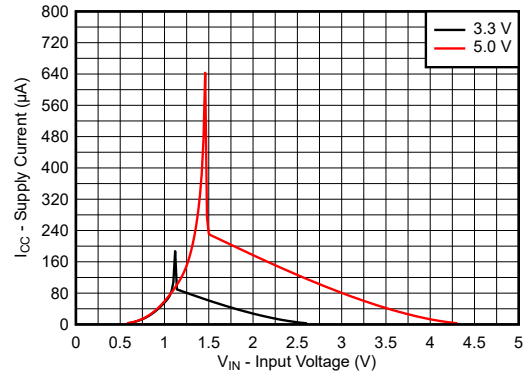


Figure 6-2. Supply Current Across Input Voltage 3.3-V and 5.0-V Supply

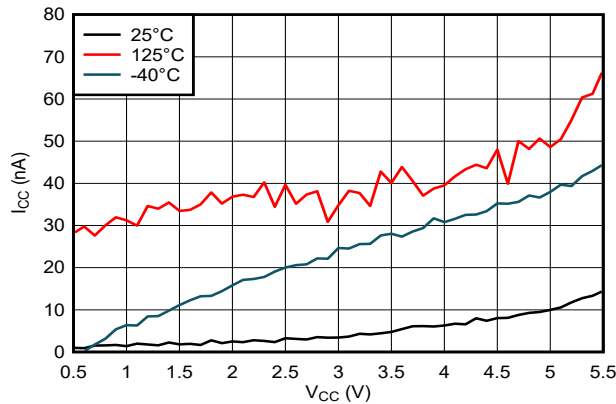


Figure 6-3. Supply Current Across Supply Voltage

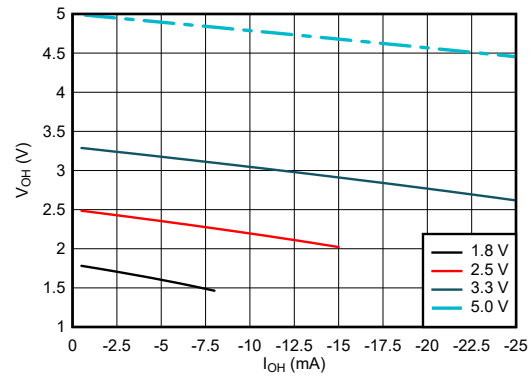


Figure 6-4. Output Voltage vs Current in HIGH State

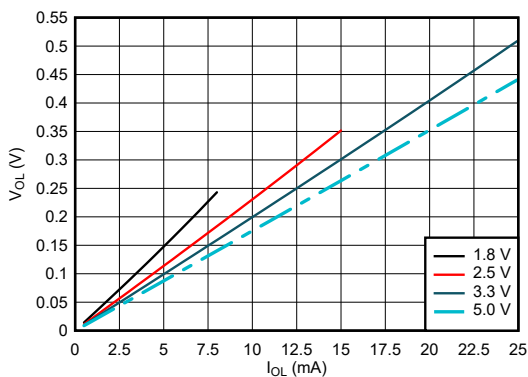


Figure 6-5. Output Voltage vs Current in LOW State

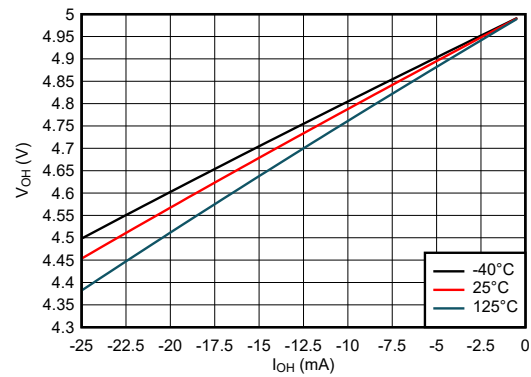


Figure 6-6. Output Voltage vs Current in HIGH State; 5-V Supply

6.15 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

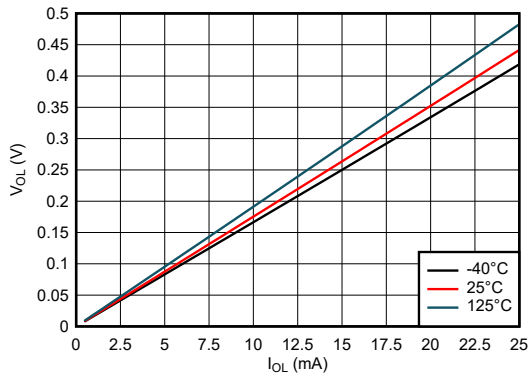


Figure 6-7. Output Voltage vs Current in LOW State; 5-V Supply

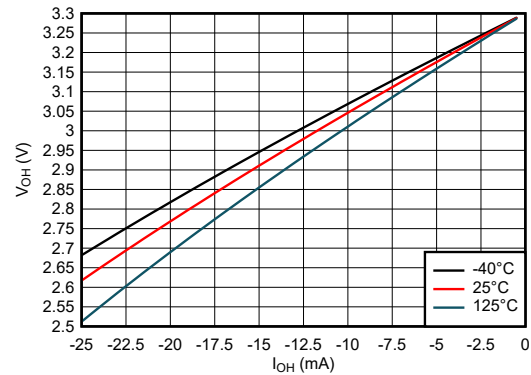


Figure 6-8. Output Voltage vs Current in HIGH State; 3.3-V Supply

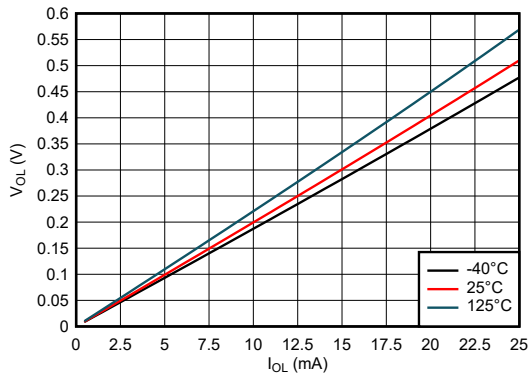


Figure 6-9. Output Voltage vs Current in LOW State; 3.3-V Supply

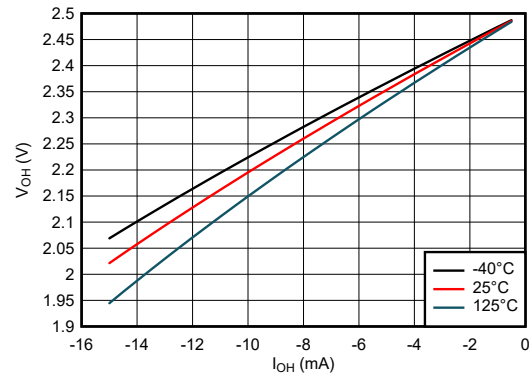


Figure 6-10. Output Voltage vs Current in HIGH State; 2.5-V Supply

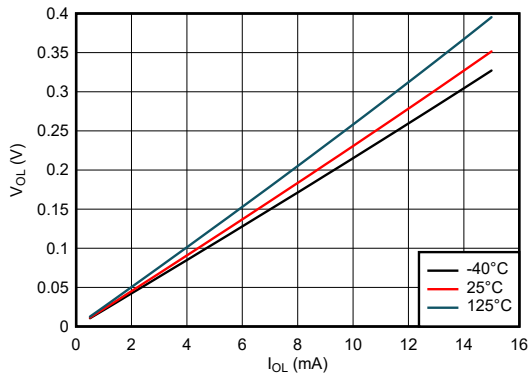


Figure 6-11. Output Voltage vs Current in LOW State; 2.5-V Supply

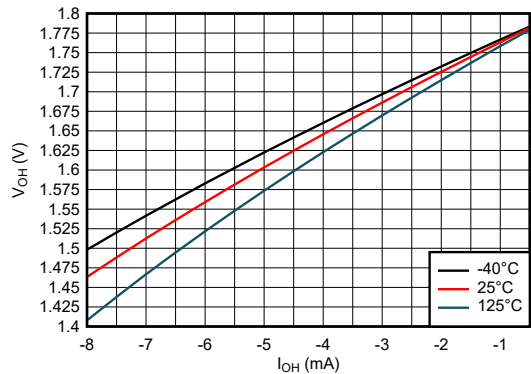


Figure 6-12. Output Voltage vs Current in HIGH State; 1.8-V Supply

6.15 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

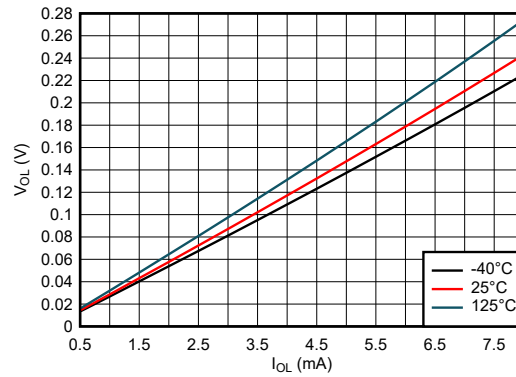


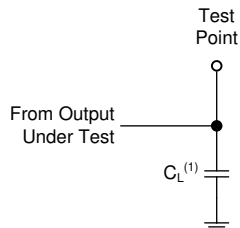
Figure 6-13. Output Voltage vs Current in LOW State; 1.8-V Supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 7-1. Load Circuit for Push-Pull Outputs

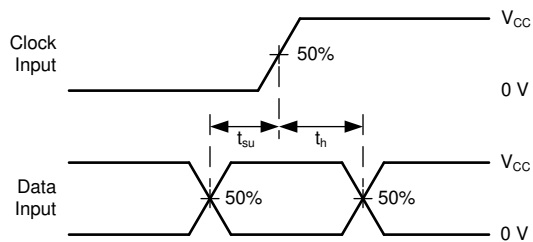


Figure 7-3. Voltage Waveforms, Setup and Hold Times

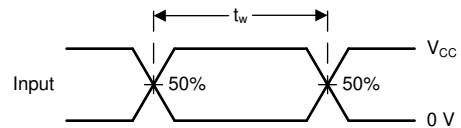
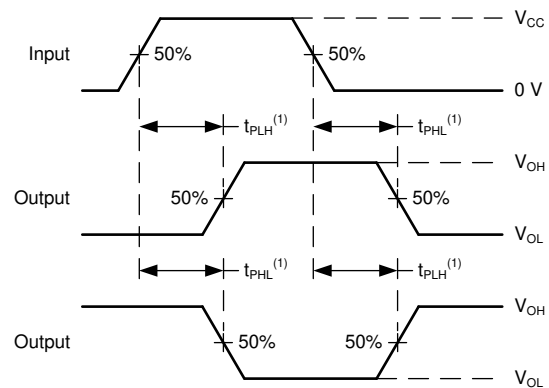
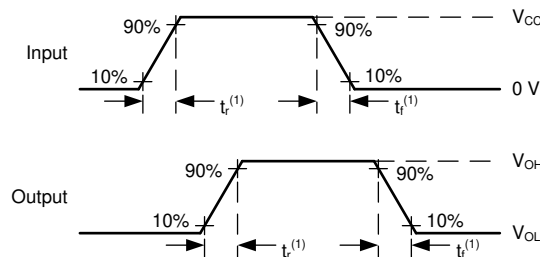


Figure 7-2. Voltage Waveforms, Pulse Duration



(1) The greater between t_{pLH} and t_{pHL} is the same as t_{pd} .

Figure 7-4. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

Figure 7-5. Voltage Waveforms, Input and Output Transition Times

8 Detailed Description

8.1 Overview

Figure 8-1 shows the SN74LV2T74. As the SN74LV2T74 is a dual D-Type positive-edge-triggered flip-flop with clear and preset, the following diagram describes one of the two device flip-flops.

8.2 Functional Block Diagram

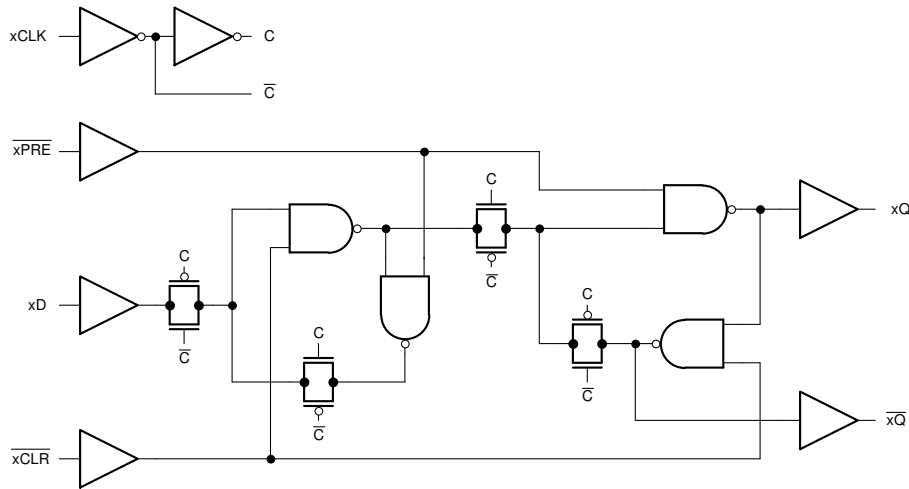


Figure 8-1. Logic Diagram (Positive Logic) for One Channel of SN74LV2T74

8.3 Feature Description

8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

8.3.2 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as shown in Figure 8-2.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

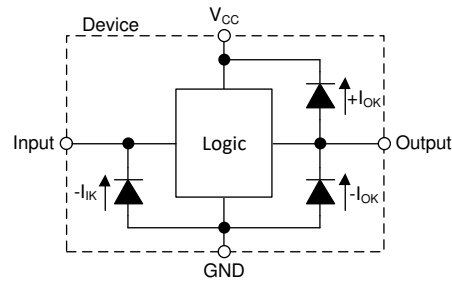


Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.3 LVxT Enhanced Input Voltage

The SN74LV2T74 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always be referenced to the supply voltage (V_{CC}), as described in the *Electrical Characteristics* table. To ensure proper functionality, input signals must remain at or below the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. Figure 8-3 shows the typical V_{IH} and V_{IL} levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the [Implications of Slow or Floating CMOS Inputs](#) application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-k Ω resistor is recommended and will typically meet all requirements.

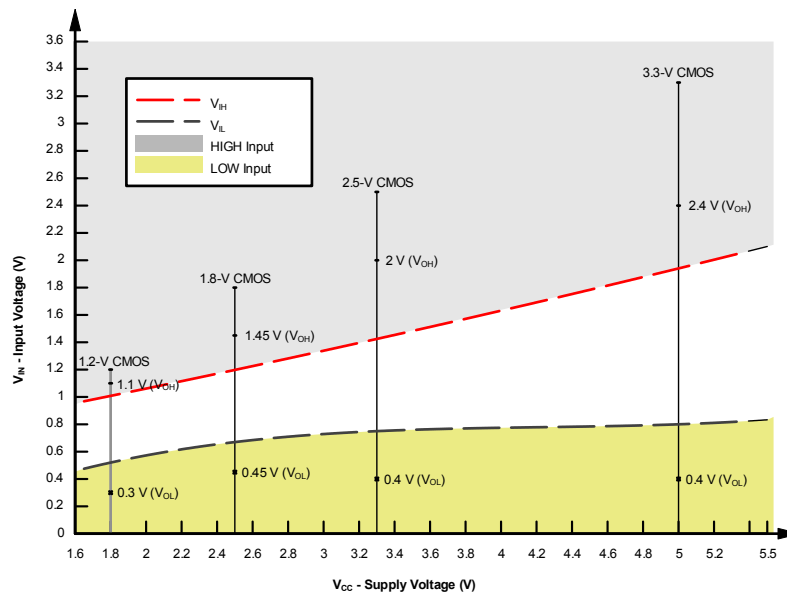


Figure 8-3. LVxT Input Voltage Levels

8.3.3.1 Down Translation

Signals can be translated down using the SN74LV2T74. The voltage applied at the V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state. As shown in [Figure 8-3](#), ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5 V, and input signals in the LOW state are lower than $V_{IL(MAX)}$.

As shown in [Figure 8-4](#) for example, the standard CMOS inputs for devices operating at 5.0 V, 3.3 V or 2.5 V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V V_{CC} .

Down Translation Combinations are as follows:

- 1.8-V V_{CC} – Inputs from 2.5 V, 3.3 V, and 5.0 V
- 2.5-V V_{CC} – Inputs from 3.3 V and 5.0 V
- 3.3-V V_{CC} – Inputs from 5.0 V

8.3.3.2 Up Translation

Input signals can be up translated using the SN74LV2T74. The voltage applied at V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a $V_{IH(MIN)}$ of 3.5 V. For the SN74LV2T74, $V_{IH(MIN)}$ with a 5-V supply is only 2 V, which would allow for up-translation from a typical 2.5-V to 5-V signals.

As shown in [Figure 8-4](#), ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$.

Up Translation Combinations are as follows:

- 1.8-V V_{CC} – Inputs from 1.2 V
- 2.5-V V_{CC} – Inputs from 1.8 V
- 3.3-V V_{CC} – Inputs from 1.8 V and 2.5 V
- 5.0-V V_{CC} – Inputs from 2.5 V and 3.3 V

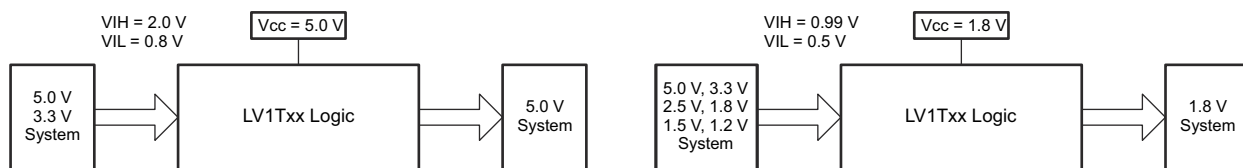


Figure 8-4. LVxT Up and Down Translation Example

8.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

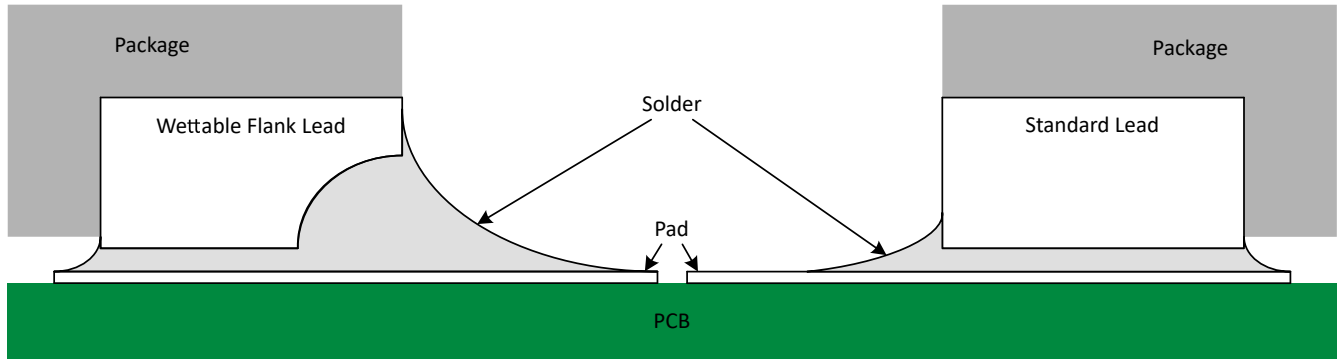


Figure 8-5. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in [Figure 8-5](#), a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

8.4 Device Functional Modes

[Table 8-1](#) lists the functional modes of the SN74LV2T74.

Table 8-1. Function Table

INPUTS				OUTPUTS ⁽¹⁾	
PRE	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	$\overline{\text{Q}}_0$

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Toggle switches are typically large, mechanically complex and relatively expensive. It is desirable to use a momentary switch instead because they are small, mechanically simple and low cost. Some systems require a toggle switch's functionality but are space or cost constrained and must use a momentary switch instead. External Schmitt-trigger buffers are used to remove noisy inputs into the (CLK) and (D) inputs.

If the data input (D) of the SN74LV2T74 is tied to the inverted output (\overline{Q}), then each clock pulse will cause the value at the output (Q) to toggle. The momentary switch can be debounced and directly connected to the clock input (CLK) to toggle the output.

9.2 Typical Application

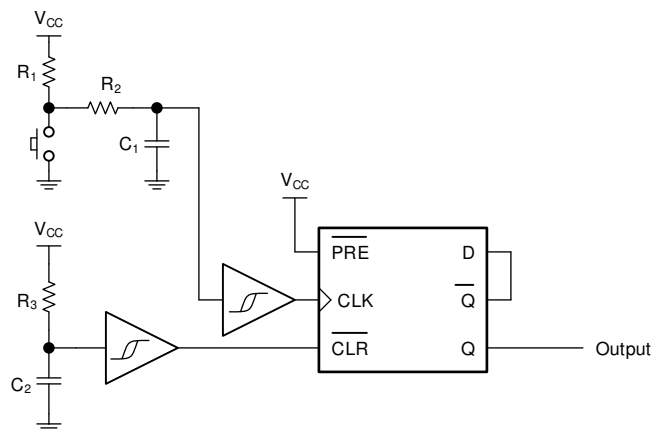


Figure 9-1. Typical Application Block Diagram

9.2.1 Design Requirements

9.2.1.1 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV2T74 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k Ω resistor value is often used due to these factors.

The SN74LV2T74 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.2 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

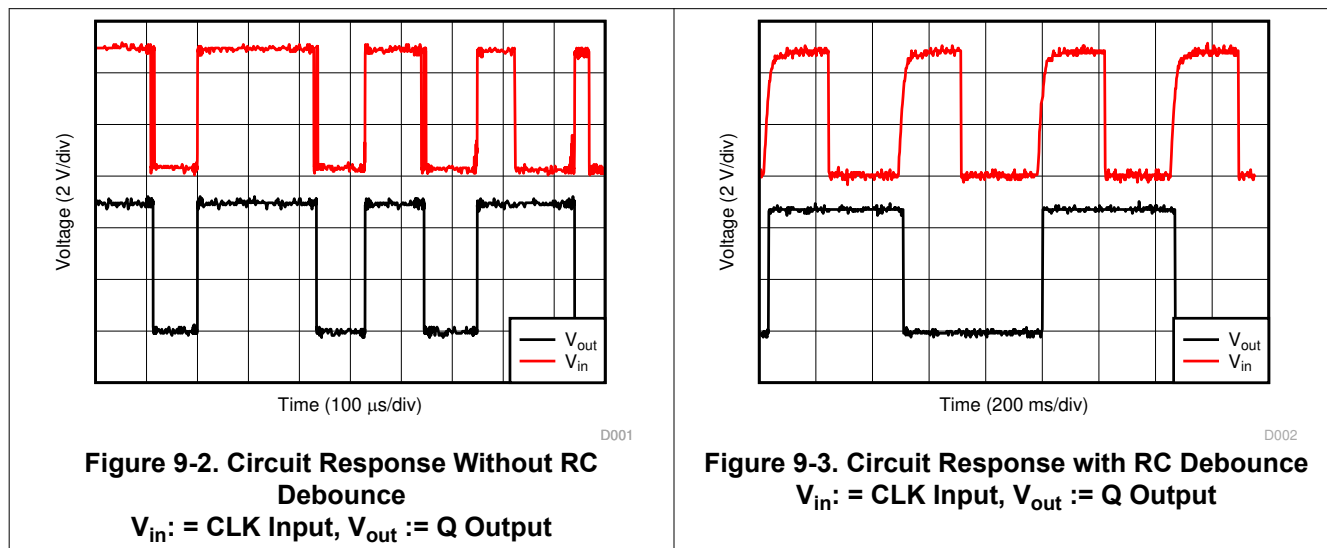
Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV2T74 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in $M\Omega$; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

9.2.3 Application Curves

Figure 9-2 shows an example of a single button press bouncing and causing the output to toggle multiple times. This will cause issues in the desired application. Figure 9-3 shows 4 button presses with an added debounce circuit, fixing the unwanted toggling and allowing for proper toggle switch operation.



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV2T74BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV2T74	Samples
SN74LV2T74PWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LV2T74	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV2T74 :

- Automotive : [SN74LV2T74-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV2T74BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LV2T74PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV2T74BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LV2T74PWR	TSSOP	PW	14	3000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

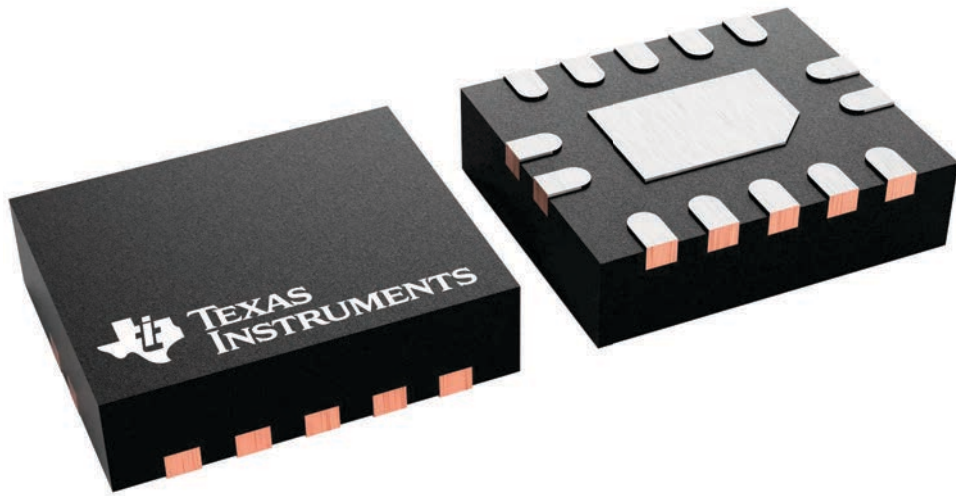
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4224636/A 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

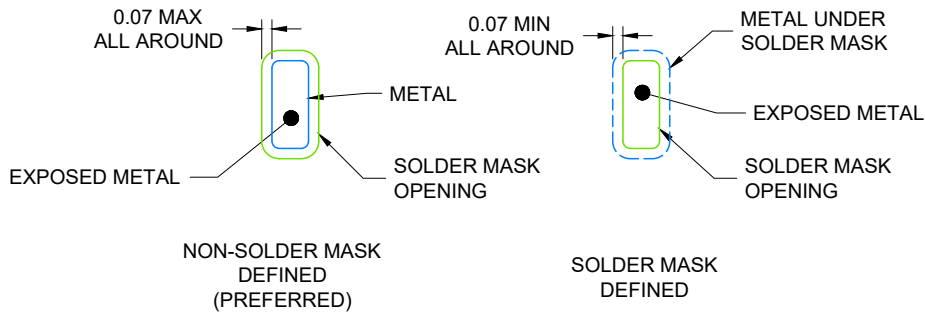
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 88% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated