SN74LV8T373-Q1 Automotive Translating Octal D-Type Flip-Flops with Clear

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Available in wettable flank QFN package
- Wide operating range of 1.65V to 5.5V
- 5.5V tolerant input pins
- Single-supply voltage translator (refer to *LVxT Enhanced Input Voltage*):
  - Up translation:
    - 1.2V to 1.8V
    - 1.5V to 2.5V
    - 1.8V to 3.3V
    - 3.3V to 5.0V
  - Down translation:
    - 5.0V, 3.3V, 2.5V to 1.8V
    - 5.0V, 3.3V to 2.5V
    - 5.0V to 3.3V
- Up to 150Mbps with 5V or 3.3V V_{CC}
- Supports standard function pinout
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Parallel data storage
- Digital bus buffer

3 Description

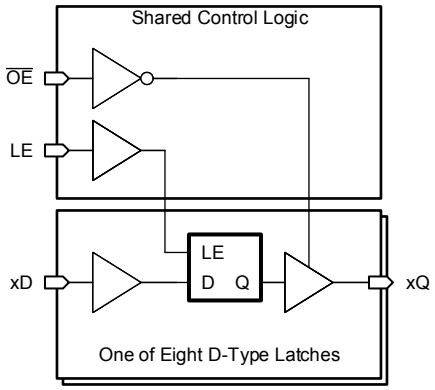
The SN74LV8T373-Q1 contains eight D-type latches. All channels share a latch enable (LE) input and output enable ($\overline{OE}$) input.

The input is designed with a reduced threshold circuit to support up translation when the supply voltage is larger than the input voltage. Additionally, the 5V tolerant input pins enable down translation when the input voltage is larger than the supply voltage. The output level is always referenced to the supply voltage (V_{CC}) and supports 1.8V, 2.5V, 3.3V, and 5V CMOS levels.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74LV8T373-Q1	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm x 4.4mm
	DGS (VSSOP, 20)	5.1mm × 4.9mm	5.1mm × 3.0mm
	RKS (VQFN, 20)	4.5mm × 2.5mm	4.5mm × 2.5mm

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

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4 Pin Configuration and Functions

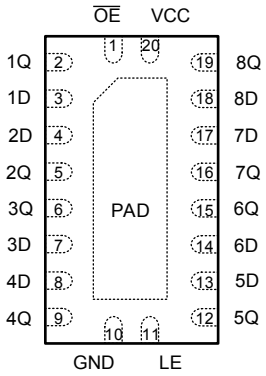


Figure 4-1. SN74LV8T373-Q1 RKS Package (Top View)

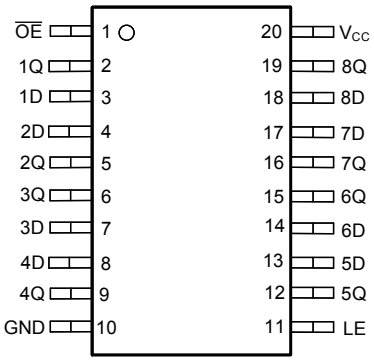


Figure 4-2. SN74LV8T373-Q1 PW , DGS Package (Top View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	I	Output enable, active low
1Q	2	O	Output for channel 1
1D	3	I	Input for channel 1
2D	4	I	Input for channel 2
2Q	5	O	Output for channel 2
3Q	6	O	Output for channel 3
3D	7	I	Input for channel 3
4D	8	I	Input for channel 4
4Q	9	O	Output for channel 4
GND	10	G	Ground
LE	11	I	Latch enable
5Q	12	O	Output for channel 5
5D	13	I	Input for channel 5
6D	14	I	Input for channel 6
6Q	15	O	Output for channel 6
7Q	16	O	Output for channel 7
7D	17	I	Input for channel 7
8D	18	I	Input for channel 8
8Q	19	O	Output for channel 8
V_{CC}	20	P	Postive supply
Thermal Pad[2]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.
(2) WRKS package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5V		-20	mA
I_{OK}	Output clamp current	V_O < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous output current through V_{CC} or GND			±75	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Spec	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
V_{IH}	High-level input voltage	V_{CC} = 1.65V to 2 V	1.1		V
		V_{CC} = 2.25V to 2.75V	1.28		
		V_{CC} = 3 V to 3.6V	1.45		
		V_{CC} = 4.5V to 5.5V	2		
V_{IL}	Low-Level input voltage	V_{CC} = 1.65V to 2 V		0.51	V
		V_{CC} = 2.25V to 2.75V		0.65	
		V_{CC} = 3 V to 3.6V		0.75	
		V_{CC} = 4.5V to 5.5V		0.8	
I_O	Output current	V_{CC} = 1.6V to 2 V		±8	mA
		V_{CC} = 2.25V to 2.75V		±15	
		V_{CC} = 3.3 V to 5.0V		±25	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.6 V to 5.0V		20	ns/V
$Δt/ΔV_{CC}$	Safe supply ramp rate for POR	V_{CC} = 1.6V to 5.5 V	6		µs/V
T_A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{θJA}$	$R_{θJC(top)}$	$R_{θJB}$	$Ψ_{JT}$	$Ψ_{JB}$	$R_{θJC(bot)}$	
DGS (VSSOP)	20	131.6	69.5	86.7	10.9	85.9	N/A	°C/W
PW (TSSOP)	20	116.8	58.5	78.7	12.6	77.9	N/A	°C/W
RKS (VQFN)	20	90.4	92.2	63.4	29	63.5	41.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH} = -50µA	1.65V to 5.5V	V_{CC}-0.1	V_{CC} - 0.01		V
	I_{OH} = -2mA	1.65V to 2V	1.21	1.7 (1)		
	I_{OH} = -3mA	2.25V to 2.75V	1.93	2.4(1)		
	I_{OH} = -5.5mA	3V to 3.6V	2.49	3.08(1)		
	I_{OH} = -8mA	4.5V to 5.5V	3.95	4.65(1)		
V_{OL}	I_{OL} = 50µA	1.65V to 5.5V		0.01	0.1	V
	I_{OL} = 2mA	1.65V to 2V		0.1(1)	0.25	
	I_{OL} = 3mA	2.25V to 2.75V		0.15(1)	0.2	
	I_{OL} = 5.5mA	3V to 3.6V		0.2(1)	0.25	
	I_{OL} = 8mA	4.5V to 5.5V		0.3(1)	0.35	
I_I	V_I = 0V or V_{CC}	0V to 5.5V		±0.001	±1	µA
I_{CC}	V_I = 0V or V_{CC}, I_O = 0; open on loading	1.65V to 5.5V		0.2	20	µA
ΔI_{CC}	One input at 0.3V or 3.4V, other inputs at 0 or V_{CC}, I_O = 0	5.5V		0.1	1.5	mA
	One input at 0.3V or 1.1V, other inputs at 0 or V_{CC}, I_O = 0	1.8V		3.4	20	µA
I_{OZ}	V_O = V_{CC} or GND and V_{CC} = 5.5V	5.5V			±2.5	µA
C_I	V_I = V_{CC} or GND	5V			10	pF
C_O	V_O = V_{CC} or GND	5V				pF
C_{PD}	No load, F = 1MHz	5V				pF
V_{POR}	V_{CC} ramp rate of 6µs/V to 100ms/V	1.65V to 5.5V			1.5	V

(1) Typical value at nearest nominal voltage (1.8V, 2.5V, 3.3V, and 5V)

5.6 Noise Characteristics

V_{CC} = 5V, C_L = 50pF, T_A = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

5.7 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	-40°C to 125°C		UNIT
				MIN	MAX	
t_W	Pulse duration	LE high	1.8V	2.7		ns
t_{SU}	Setup time	Data before LE falling edge	1.8V	1.8		ns
t_H	Hold time	Data after LE falling edge	1.8V	1.4		ns
t_W	Pulse duration	LE high	2.5V	2.7		ns
t_{SU}	Setup time	Data before LE falling edge	2.5V	1.3		ns
t_H	Hold time	Data after LE falling edge	2.5V	1.2		ns
t_W	Pulse duration	LE high	3.3V	2.7		ns
t_{SU}	Setup time	Data before LE falling edge	3.3V	1		ns
t_H	Hold time	Data after LE falling edge	3.3V	1		ns
t_W	Pulse duration	LE high	5V	2.7		ns
t_{SU}	Setup time	Data before LE falling edge	5V	0.6		ns
t_H	Hold time	Data after LE falling edge	5V	0.6		ns

5.8 Switching Characteristics

C_L = 50pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{PLH}	D	Q	C_L = 15pF	1.8V	6.4	10.8	16.4	ns
t_{PHL}				1.8V	8	14.1	21	ns
t_{PLH}	LE	Q	C_L = 15pF	1.8V	7.3	12.5	18.6	ns
t_{PHL}				1.8V	7.9	14	21	ns
t_{PZL}	$\overline{OE}$	Q	C_L = 15pF	1.8V	7.3	11.9	17.3	ns
t_{PZH}				1.8V	8.1	13.1	18.9	ns
t_{PLZ}	$\overline{OE}$	Q	C_L = 15pF	1.8V	7.1	9.4	12.3	ns
t_{PHZ}				1.8V	7.1	10.3	14.4	ns
t_{PLH}	D	Q	C_L = 15pF	2.5V	4.4	6.9	10.2	ns
t_{PHL}				2.5V	5.6	8.9	13	ns
t_{PLH}	LE	Q	C_L = 15pF	2.5V	5.1	8	11.6	ns
t_{PHL}				2.5V	5.1	8.5	12.7	ns
t_{PZL}	$\overline{OE}$	Q	C_L = 15pF	2.5V	5.2	7.8	11.1	ns
t_{PZH}				2.5V	5.9	8.7	12.2	ns
t_{PLZ}	$\overline{OE}$	Q	C_L = 15pF	2.5V	5.3	6.6	8.3	ns
t_{PHZ}				2.5V	5	6.8	9.2	ns
t_{PLH}	D	Q	C_L = 15pF	3.3V	3.9	5.8	8.4	ns
t_{PHL}				3.3V	4.9	7.4	10.6	ns
t_{PLH}	LE	Q	C_L = 15pF	3.3V	4.5	6.6	9.6	ns
t_{PHL}				3.3V	4.2	6.8	10.2	ns
t_{PZL}	$\overline{OE}$	Q	C_L = 15pF	3.3V	4.5	6.5	9.2	ns
t_{PZH}				3.3V	5.3	7.4	10.1	ns
t_{PLZ}	$\overline{OE}$	Q	C_L = 15pF	3.3V	4.6	5.6	7	ns
t_{PHZ}				3.3V	3.8	5.4	7.5	ns
t_{PLH}	D	Q	C_L = 15pF	5V	3.7	4.9	6.7	ns
t_{PHL}				5V	3.6	5.1	7.2	ns
t_{PLH}	LE	Q	C_L = 15pF	5V	4	5.5	7.5	ns
t_{PHL}				5V	3.6	5.2	7.5	ns
t_{PZL}	$\overline{OE}$	Q	C_L = 15pF	5V	3.4	4.6	6.3	ns
t_{PZH}				5V	4	5.3	7.1	ns
t_{PLZ}	$\overline{OE}$	Q	C_L = 15pF	5V	4.6	5.2	6.1	ns
t_{PHZ}				5V	3.1	4.1	5.6	ns
t_{PLH}	D	Q	C_L = 50pF	1.8V	8.3	13.9	20.7	ns
t_{PHL}				1.8V	9.9	16.7	24.9	ns
t_{PLH}	LE	Q	C_L = 50pF	1.8V	9.7	15.7	23	ns
t_{PHL}				1.8V	10.1	16.9	25.1	ns
t_{PZL}	$\overline{OE}$	Q	C_L = 50pF	1.8V	9.4	14.9	21.5	ns
t_{PZH}				1.8V	10.5	16.5	23.5	ns
t_{PLZ}	$\overline{OE}$	Q	C_L = 50pF	1.8V	13.5	16	19	ns
t_{PHZ}				1.8V	13.6	16.9	21.1	ns
t_{PLH}	D	Q	C_L = 50pF	2.5V	5.8	9	13.1	ns
t_{PHL}				2.5V	7	10.8	15.7	ns

C_L = 50pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{PLH}	LE	Q	C_L = 50pF	2.5V	6.9	10.3	14.7	ns
t_{PHL}				2.5V	6.8	10.8	15.7	ns
t_{PZL}	$\overline{OE}$	Q	C_L = 50pF	2.5V	7.1	10.1	14.1	ns
t_{PZH}				2.5V	7.8	11.2	15.5	ns
t_{PLZ}	$\overline{OE}$	Q	C_L = 50pF	2.5V	9.6	11	12.9	ns
t_{PHZ}				2.5V	9.2	11.1	13.6	ns
t_{PLH}	D	Q	C_L = 50pF	3.3V	5	7.6	10.9	ns
t_{PHL}				3.3V	6.2	9.1	12.9	ns
t_{PLH}	LE	Q	C_L = 50pF	3.3V	6	8.7	12.2	ns
t_{PHL}				3.3V	5.9	8.8	12.8	ns
t_{PZL}	$\overline{OE}$	Q	C_L = 50pF	3.3V	6.3	8.7	11.8	ns
t_{PZH}				3.3V	6.9	9.6	12.9	ns
t_{PLZ}	$\overline{OE}$	Q	C_L = 50pF	3.3V	8.2	9.2	10.6	ns
t_{PHZ}				3.3V	7.4	8.8	10.9	ns
t_{PLH}	D	Q	C_L = 50pF	5V	4.5	6.2	8.5	ns
t_{PHL}				5V	4.7	6.5	9	ns
t_{PLH}	LE	Q	C_L = 50pF	5V	5.3	7.1	9.5	ns
t_{PHL}				5V	4.9	6.9	9.6	ns
t_{PZL}	$\overline{OE}$	Q	C_L = 50pF	5V	4.7	6.3	8.4	ns
t_{PZH}				5V	5.3	7.1	9.4	ns
t_{PLZ}	$\overline{OE}$	Q	C_L = 50pF	5V	6.8	7.4	8.3	ns
t_{PHZ}				5V	5.2	6.2	7.6	ns
$t_{sk(o)}$			C_L = 50pF	1.8V		0.3	0.6	ns
$t_{sk(o)}$			C_L = 50pF	2.5V		0.3	0.4	ns
$t_{sk(o)}$			C_L = 50pF	3.3V		0.2	0.4	ns
$t_{sk(o)}$			C_L = 50pF	5V		0.2	0.3	ns

5.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

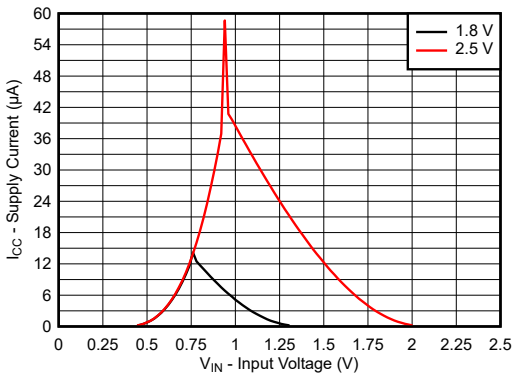


Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

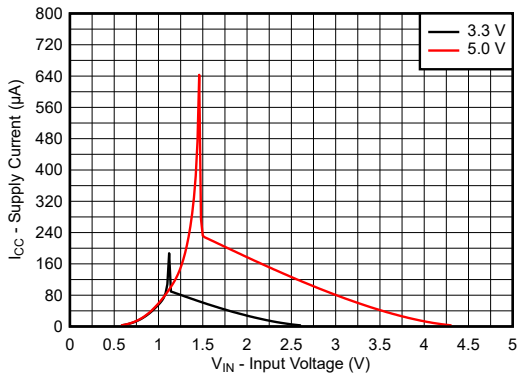


Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

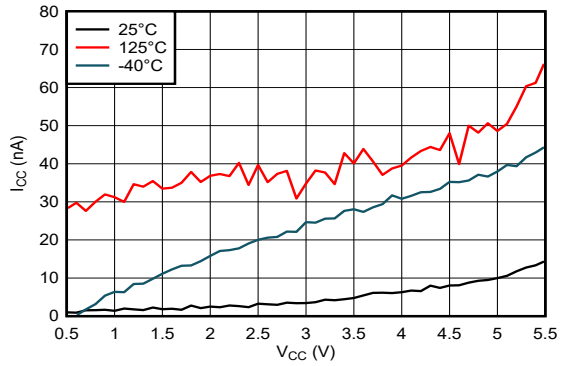


Figure 5-3. Supply Current Across Supply Voltage

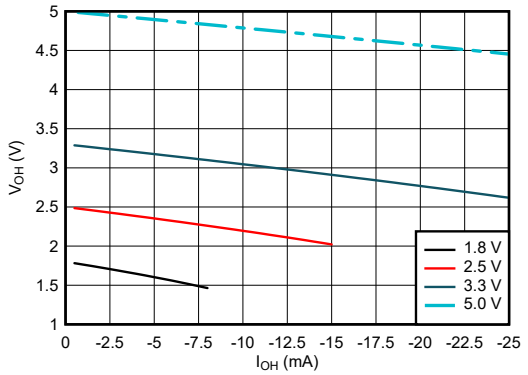


Figure 5-4. Output Voltage vs Current in HIGH State

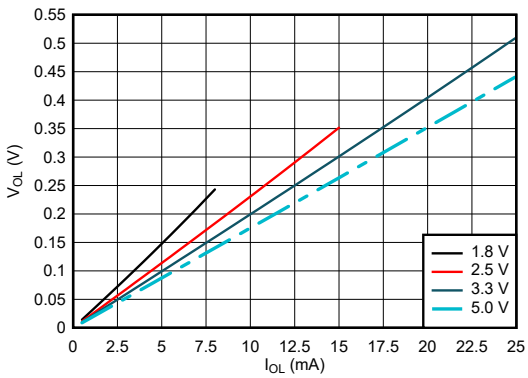


Figure 5-5. Output Voltage vs Current in LOW State

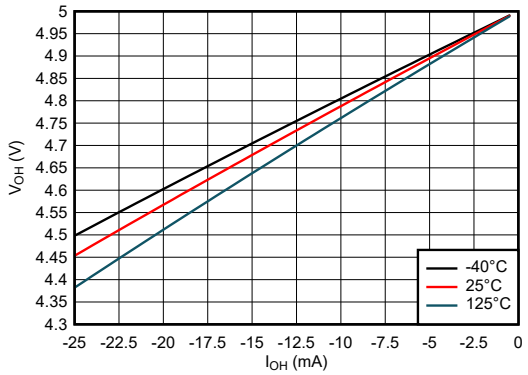


Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply

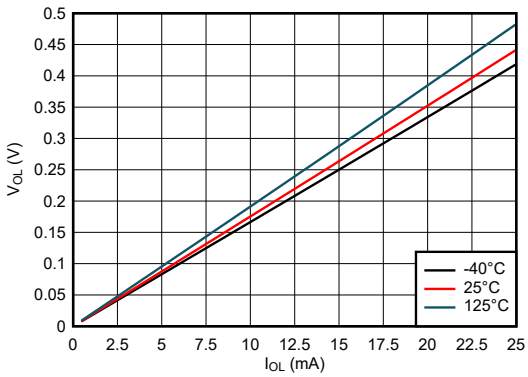


Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

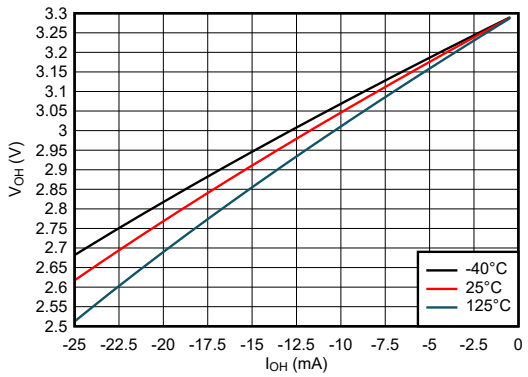


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

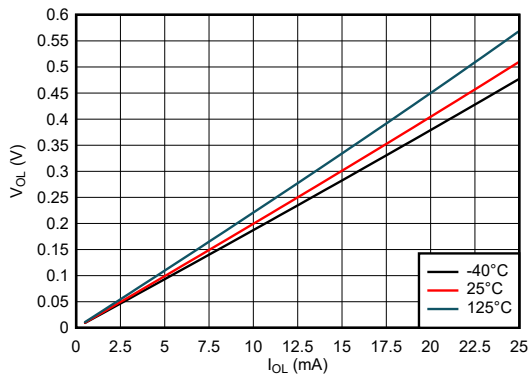


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

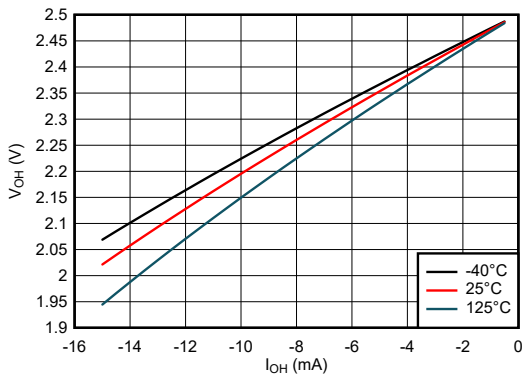


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

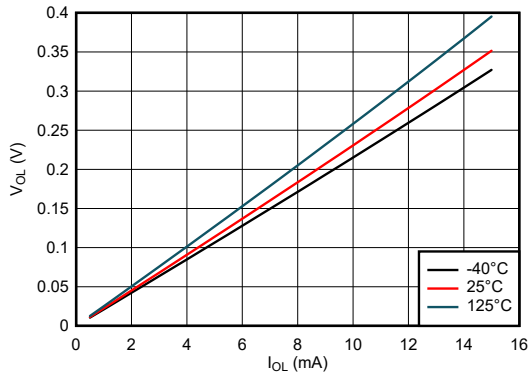


Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

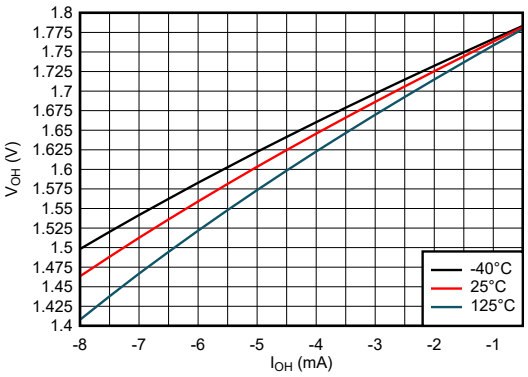


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

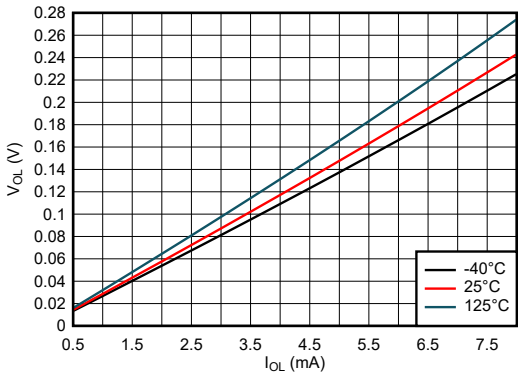


Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply

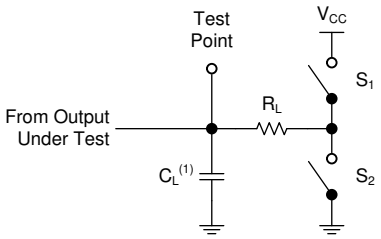
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured individually with one input transition per measurement.

TEST	S1	S2	R_L	C_L	ΔV	V_{CC}
t_{PLH}, t_{PHL}	OPEN	OPEN	—	15pF, 50pF	—	ALL
t_{PLZ}, t_{PZL}	CLOSED	OPEN	1kΩ	15pF, 50pF	0.15V	≤ 2.5V
t_{PHZ}, t_{PZH}	OPEN	CLOSED	1kΩ	15pF, 50pF	0.15V	≤ 2.5V
t_{PLZ}, t_{PZL}	CLOSED	OPEN	1kΩ	15pF, 50pF	0.3V	> 2.5V
t_{PHZ}, t_{PZH}	OPEN	CLOSED	1kΩ	15pF, 50pF	0.3V	> 2.5V



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs

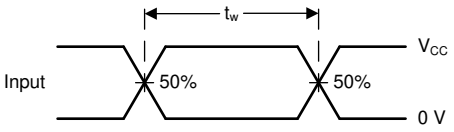


Figure 6-2. Voltage Waveforms, Pulse Duration

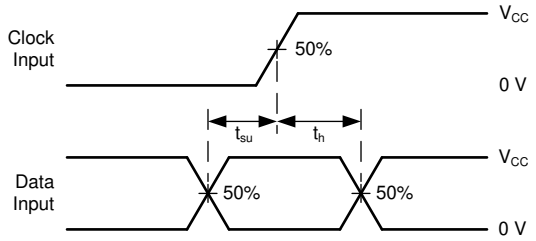
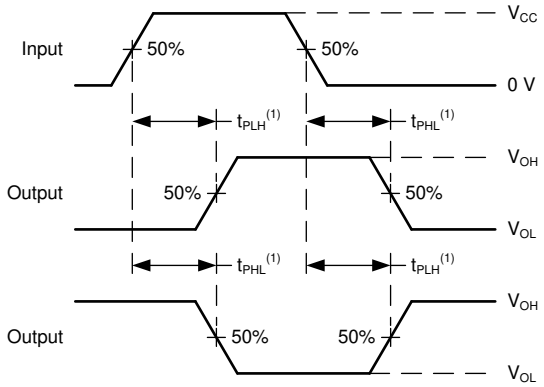
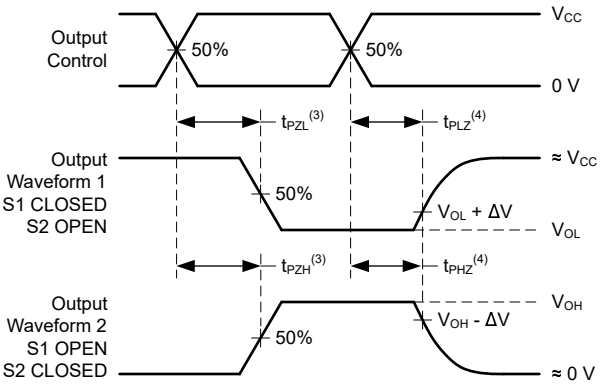


Figure 6-3. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

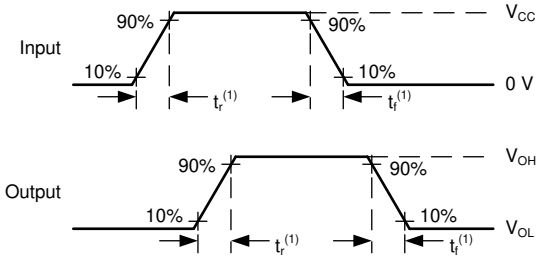
Figure 6-4. Voltage Waveforms Propagation Delays



(3) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

(4) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-5. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-6. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74LV8T373-Q1 contains eight D-type latches. All channels share a latch enable (LE) and output enable ($\overline{OE}$) input.

When the latch is enabled (LE is high), data is allowed to pass through from the D inputs to the Q outputs.

When the latch is disabled (LE is low), the Q outputs hold the last state they had regardless of changes at the D inputs.

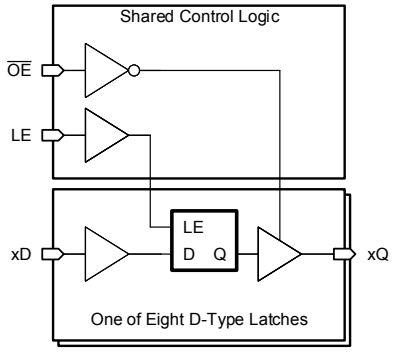
If the latch enable (LE) input is held low during startup, the output state of all channels is unknown until the latch enable (LE) input is driven high with valid input signals at all data (D) inputs.

When the outputs are enabled ($\overline{OE}$ is low), the outputs are actively driving low or high.

When the outputs are disabled ($\overline{OE}$ is high), the outputs are set into the high-impedance state.

The active low output enable ($\overline{OE}$) does not have any impact on the stored state in the latches.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.3.2 Latching Logic with Known Power-Up State

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory. In typical logic devices, the output state of each latching circuit is unknown after power is initially applied; however, this device includes an added Power On Reset (POR) circuit which sets the states of all included latching circuits during the power-up ramp prior to the device starting normal functionality.

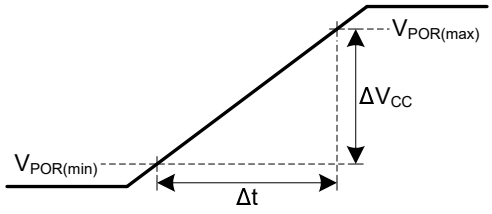


Figure 7-1. Supply (V_{CC}) Ramp Characteristics for Known Power-Up State

Figure 7-1 shows a correct supply voltage turn-on ramp and defines values used in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

Prior to starting the power-on ramp, the supply must be completely off ($V_{CC} \leq V_{POR(min)}$).

The supply voltage must ramp at a rate within the range provided in the *Recommended Operating Conditions* table.

The output state of each latching logic circuit only remains stable as long as power is applied to the device ($V_{CC} \geq V_{POR(max)}$).

Variation from these recommendations will result in the device having an unknown power-up state.

7.3.3 LVxT Enhanced Input Voltage

The SN74LV8T373-Q1 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5V levels to support down-translation. For proper functionality, input signals must remain at or above the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. Figure 7-2 shows the typical V_{IH} and V_{IL} levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Input signals must transition between valid logic states quickly, as defined by the input transition rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at a valid high or low voltage level. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and will typically meet all requirements.

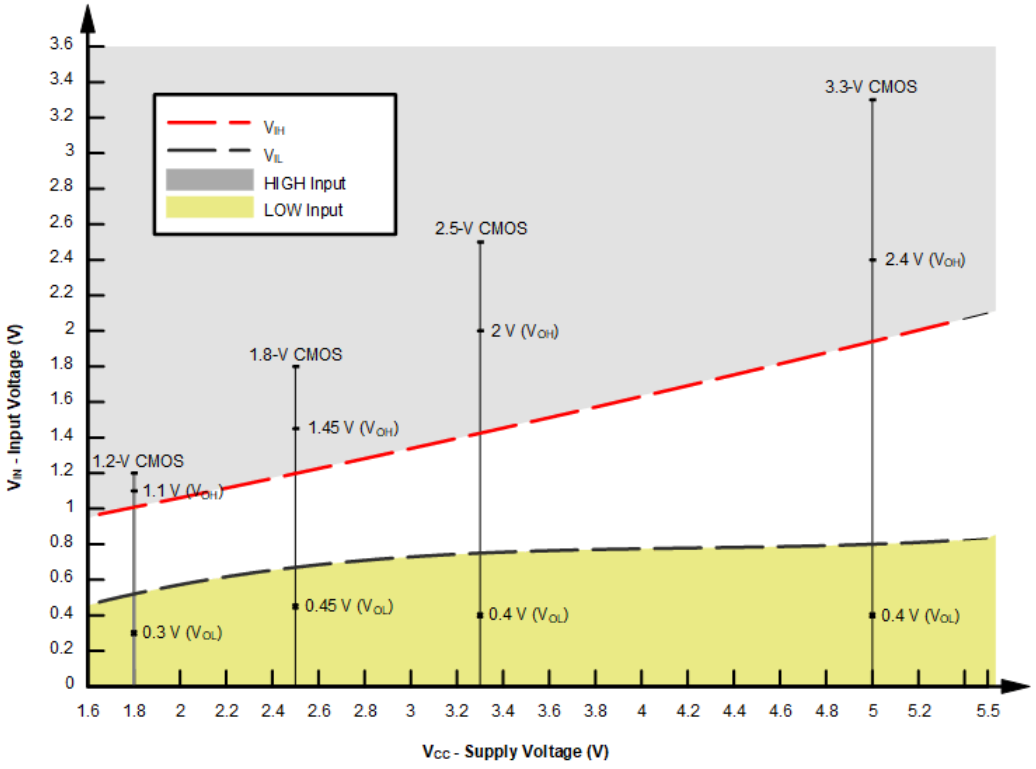


Figure 7-2. LVxT Input Voltage Levels

7.3.3.1 Up Translation

Input signals can be up translated using the SN74LV8T373-Q1. The voltage applied at V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels, which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5V supply will have a $V_{IH(MIN)}$ of 3.5V. For the SN74LV8T373-Q1, $V_{IH(MIN)}$ with a 5V supply is only 2V, which would allow for up-translation from a typical 2.5V to 5V signals.

Ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in Figure 7-3.

Up Translation Combinations are as follows:

- 1.8V V_{CC} – Inputs from 1.2V
- 2.5V V_{CC} – Inputs from 1.8V
- 3.3V V_{CC} – Inputs from 1.8V and 2.5V
- 5.0V V_{CC} – Inputs from 2.5V and 3.3V

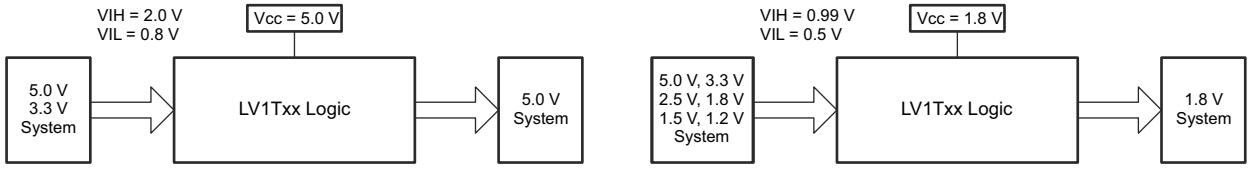


Figure 7-3. LVxT Up and Down Translation Example

7.3.3.2 Down Translation

Signals can be translated down using the SN74LV8T373-Q1. The voltage applied at the V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0V in the LOW state. Ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5V, and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in Figure 7-2.

For example, standard CMOS inputs for devices operating at 5.0V, 3.3V or 2.5V can be down-translated to match 1.8V CMOS signals when operating from 1.8V V_{CC}. See Figure 7-3.

Down Translation Combinations are as follows:

- 1.8V V_{CC} – Inputs from 2.5V, 3.3V, and 5.0V
- 2.5V V_{CC} – Inputs from 3.3V and 5.0V
- 3.3V V_{CC} – Inputs from 5.0V

7.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet where packages include this feature.

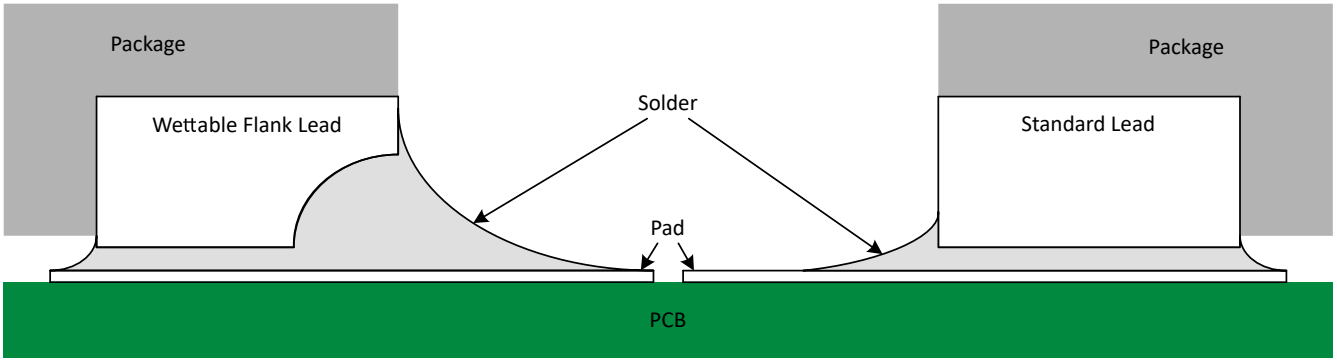


Figure 7-4. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 7-4, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

7.3.5 Clamp Diode Structure

As Figure 7-5 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

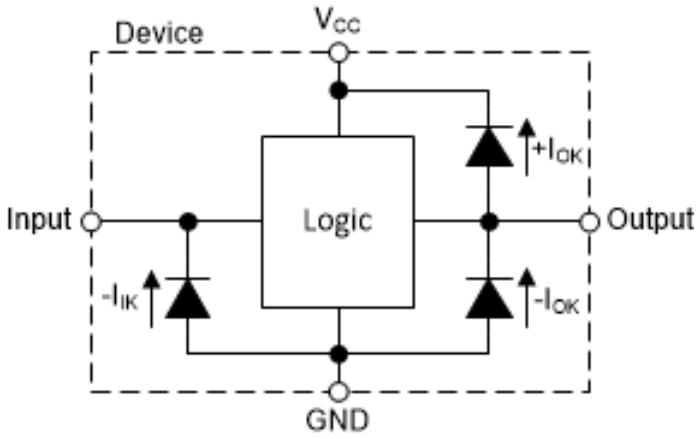


Figure 7-5. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS[1]			OUTPUT[2]
$\overline{OE}$	LE	D	Q
L	H	L	L
L	H	H	H
L	L	X	Q_0 [3]
H	X	X	Z

(1) L = input low, H = input high, ↑ = input transitioning from low to high, ↓ = input transitioning from high to low, X = don't care
(2) L = output low, H = output high, Q_0 = previous state, Z = high impedance
(3) At startup, Q_0 is low

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SN74LV8T373-Q1 is used to control an 8-bit data bus.

Outputs can be held in the high-impedance state, held in the last known state, or change together with the data inputs, depending on the control inputs at LE and $\overline{OE}$ coming from the bus controller.

8.2 Typical Application

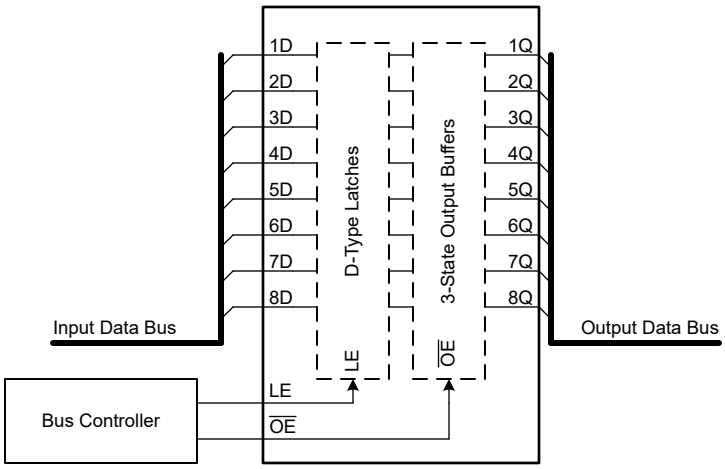


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV8T373-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV8T373-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LV8T373-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LV8T373-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV8T373-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV8T373-Q1 to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

8.2.3 Application Curves

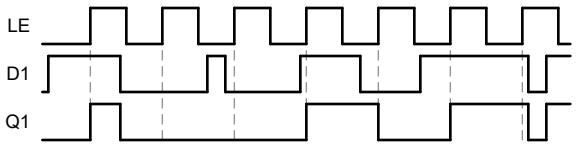


Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance.

During startup, the power supply should ramp within the provided power-up ramp rate range in the *Recommended Operating Conditions* table.

A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

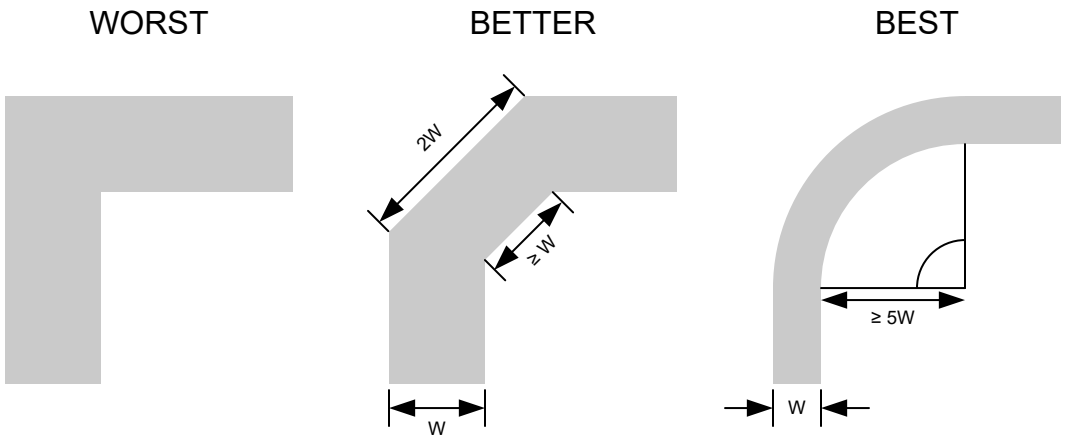


Figure 8-3. Example Trace Corners for Improved Signal Integrity

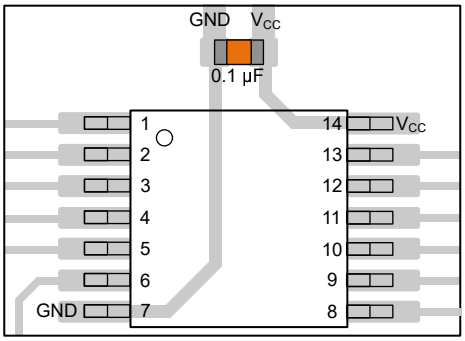


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

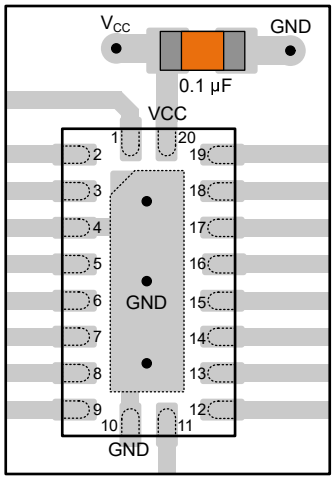


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

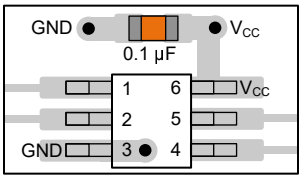


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

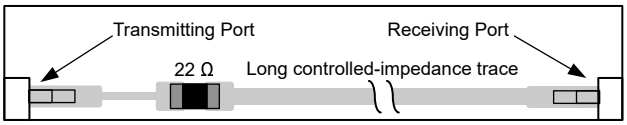


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CLV8T373QWRKSRQ1	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	LT373WQ
SN74LV8T373QDGSRQ1	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	8T373Q
SN74LV8T373QPWRQ1	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	LV8T373Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LV8T373-Q1 :

- Catalog : SN74LV8T373

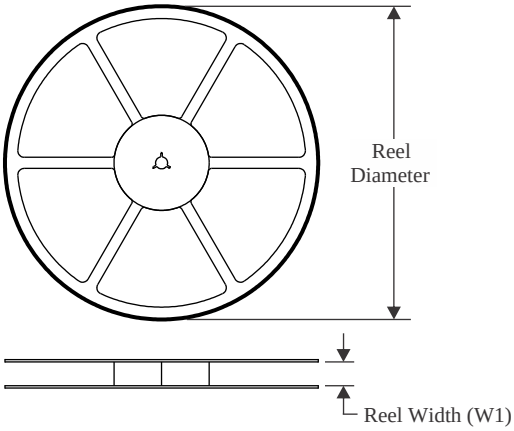
- Enhanced Product : SN74LV8T373-EP

NOTE: Qualified Version Definitions:

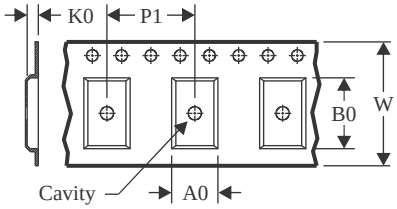
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

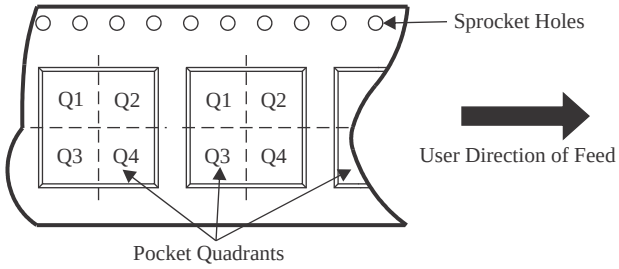


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

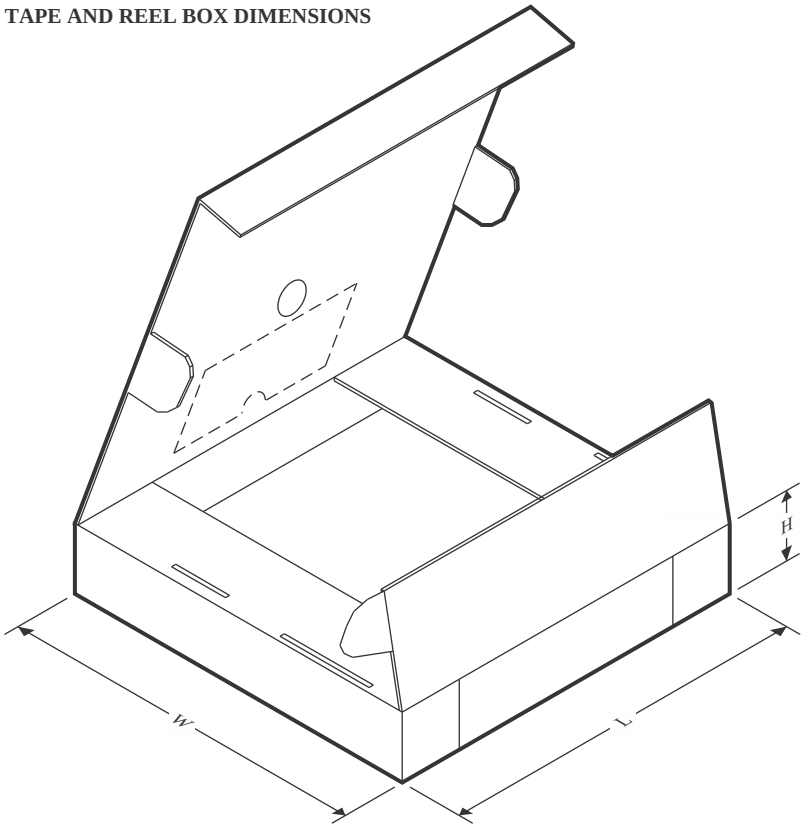
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLV8T373QWRKSRQ1	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
SN74LV8T373QDGSRQ1	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74LV8T373QPWRQ1	TSSOP	PW	20	3000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLV8T373QWRKSRQ1	VQFN	RKS	20	3000	210.0	185.0	35.0
SN74LV8T373QDGSRQ1	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74LV8T373QPWRQ1	TSSOP	PW	20	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

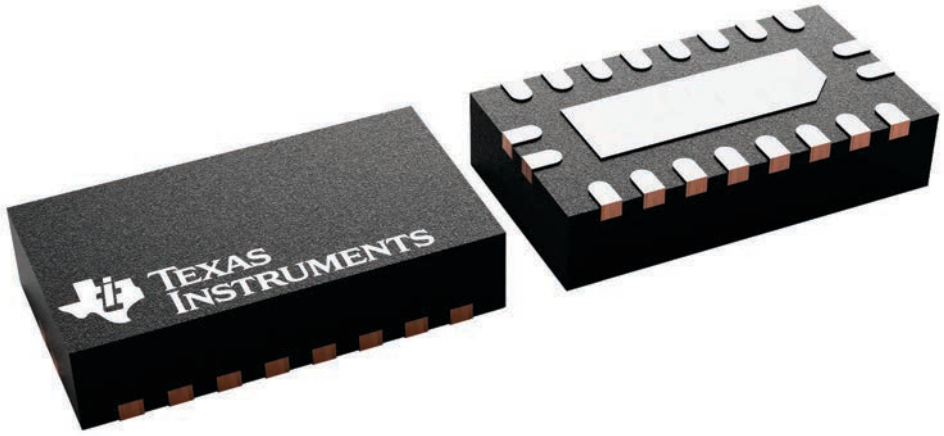
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

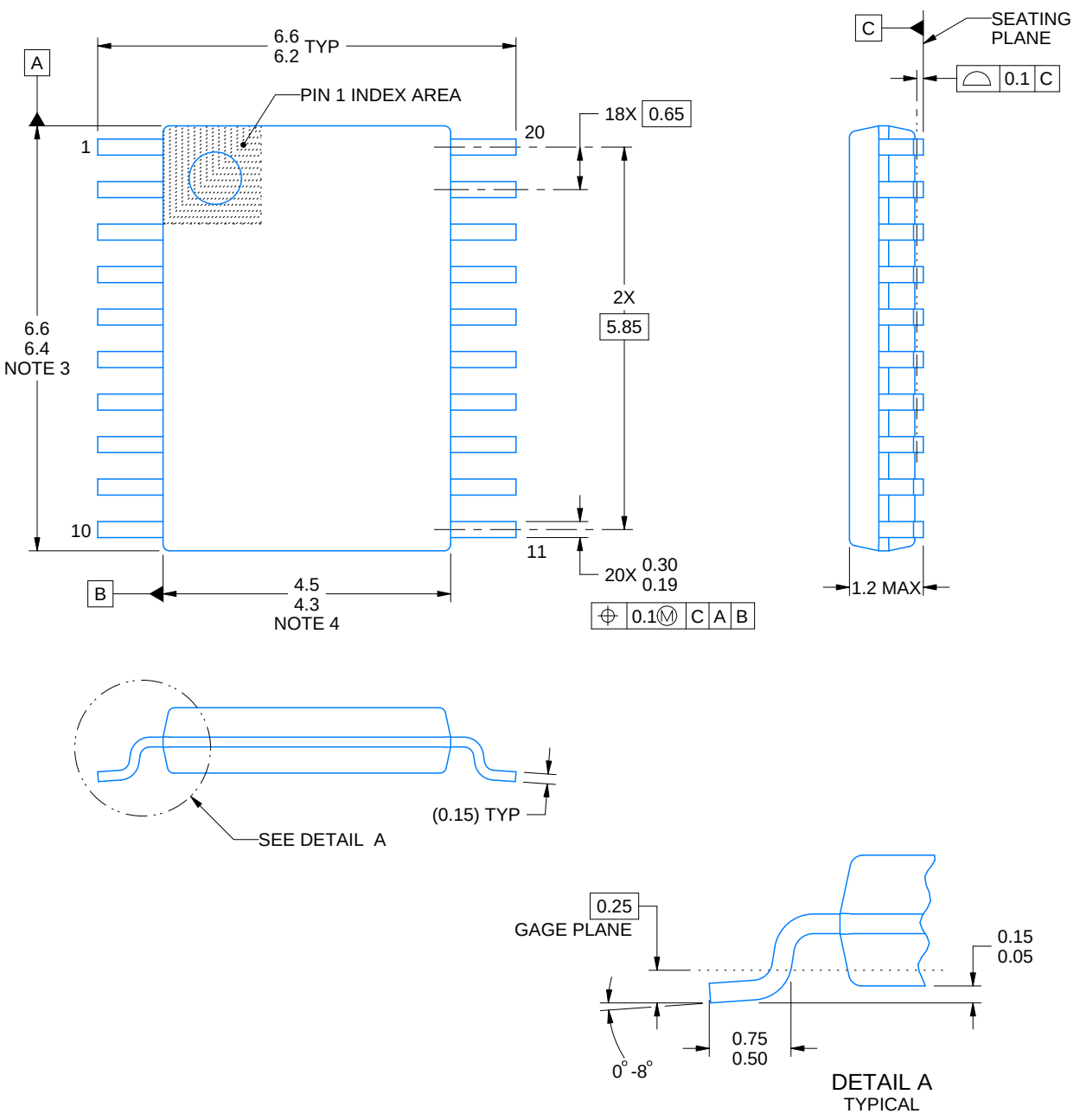


PACKAGE OUTLINE

PW0020A

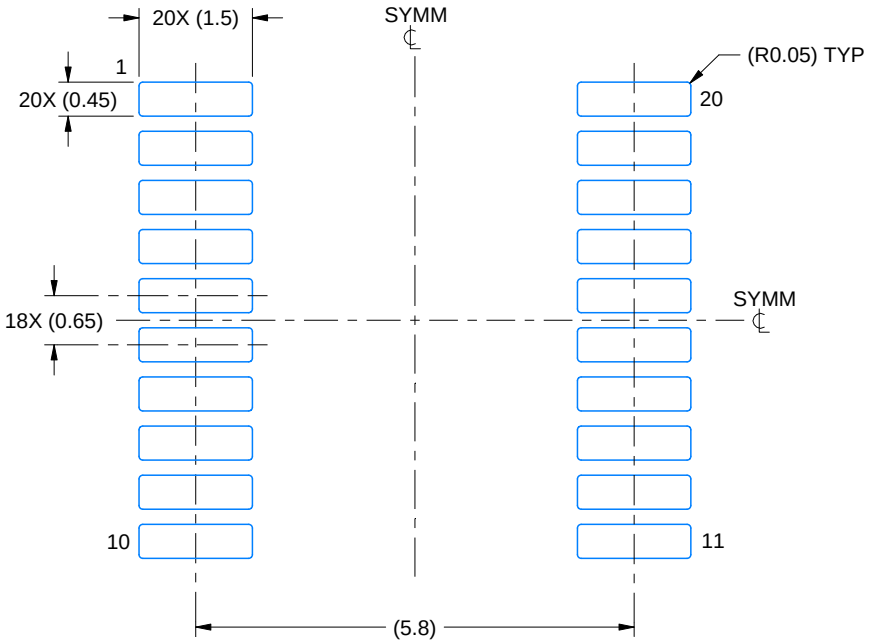
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



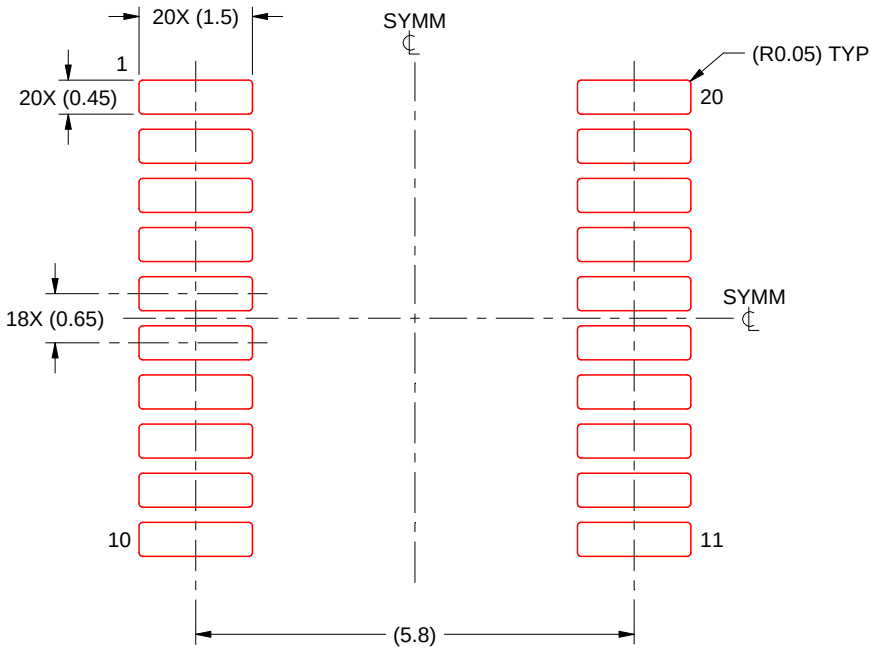
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

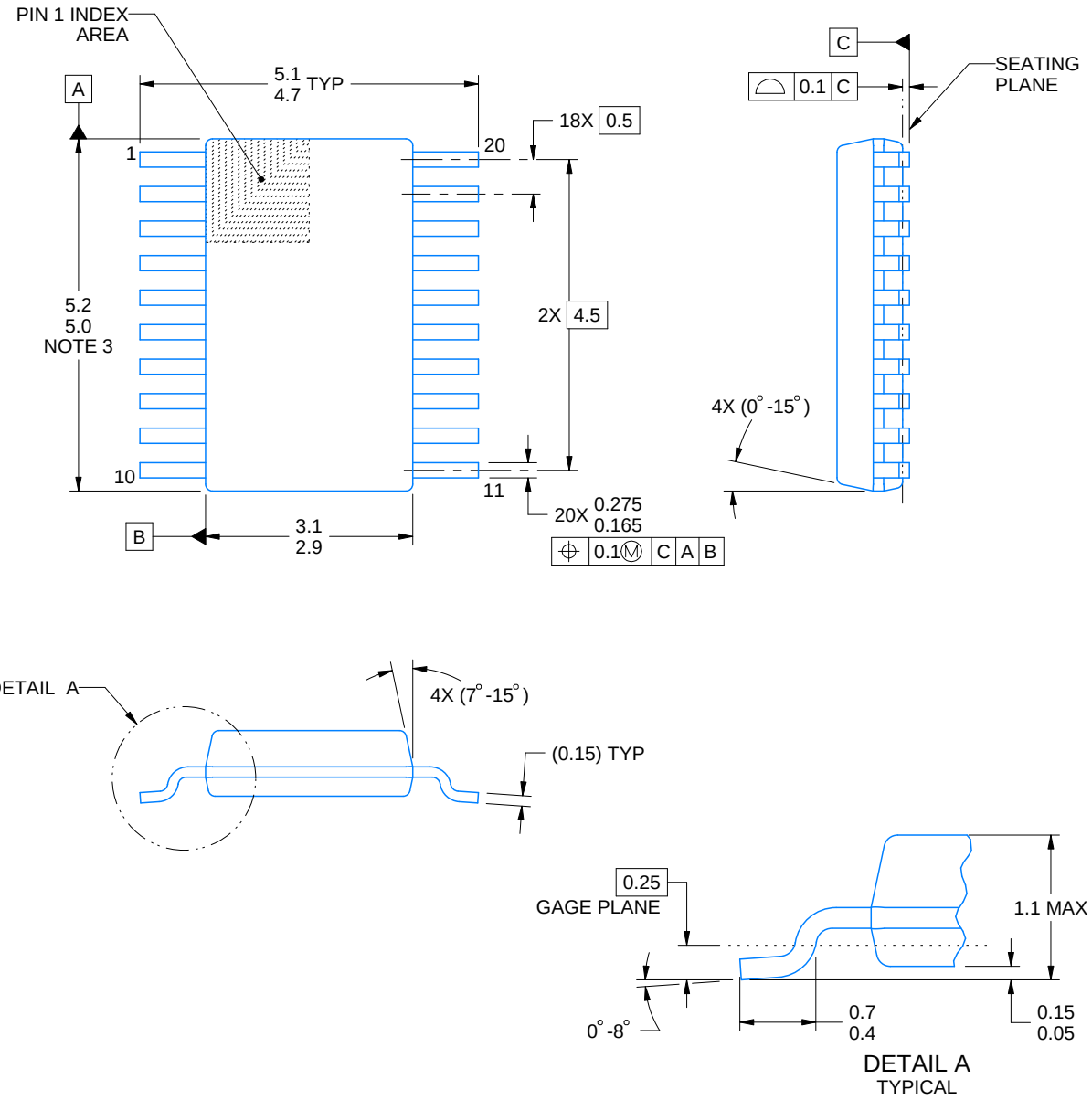
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

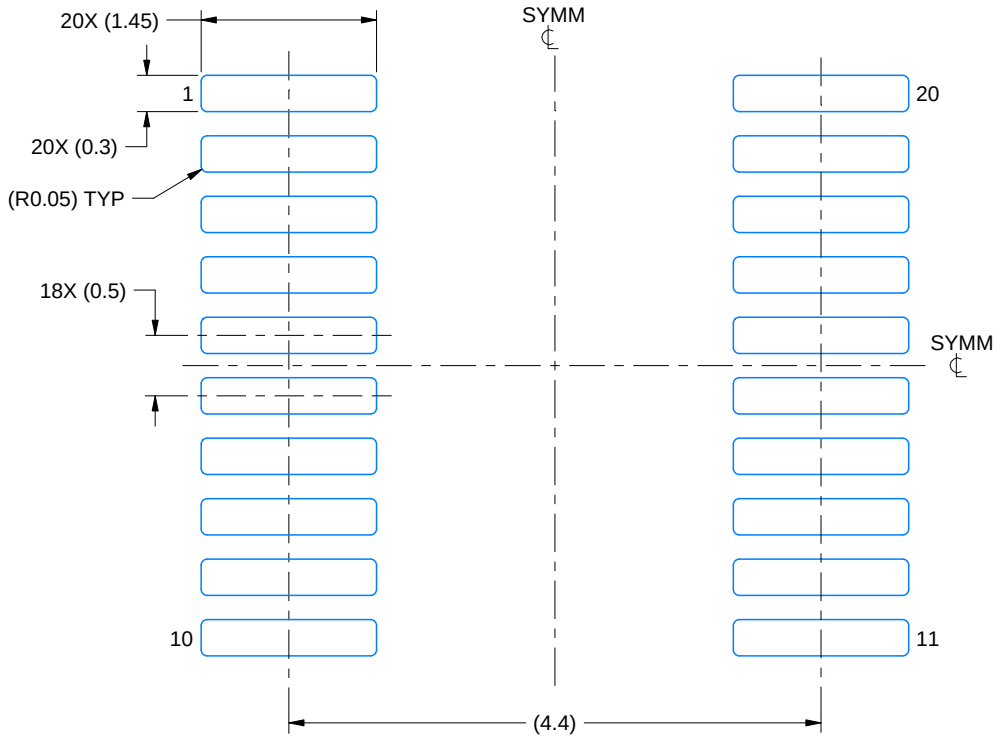
SMALL OUTLINE PACKAGE



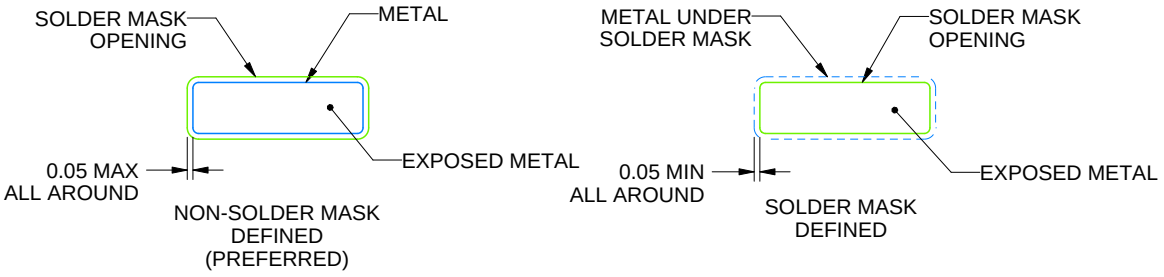
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

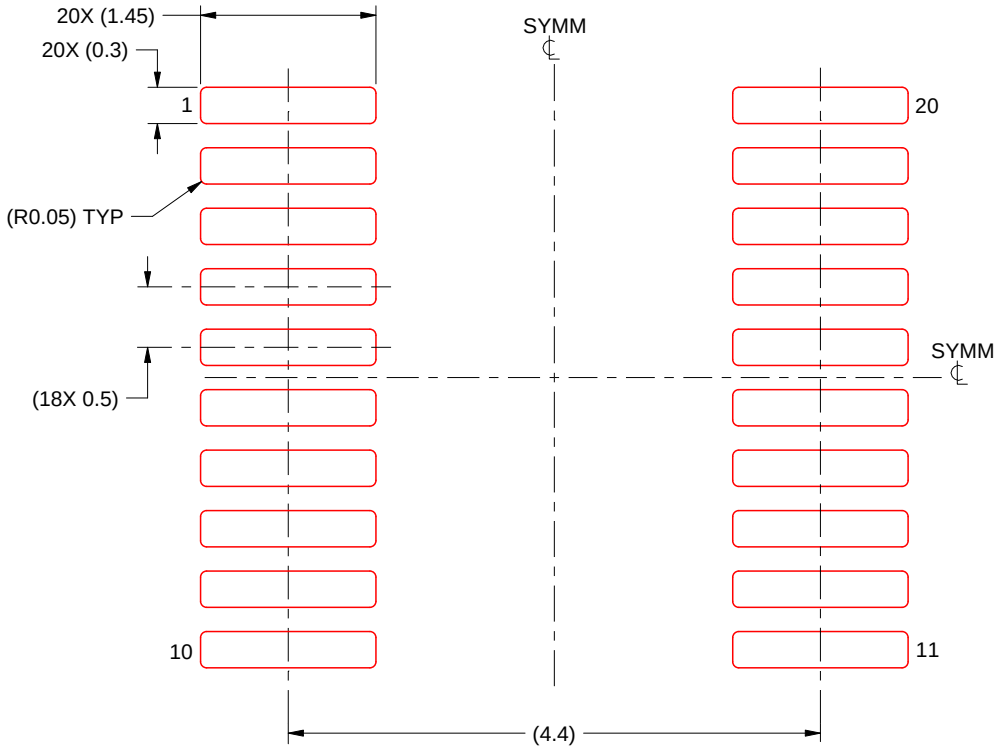


SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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