

# SN74LV8T7541-Q1 Automotive Octal Buffers With Open-Drain Outputs and Logic-Level Shifter

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Available in [Wettable Flanks](#) QFN package
- Wide operating range of 1.65V to 5.5V
- 5.5V tolerant input pins
- *LVxT enhanced inputs* combined with *open-drain outputs* provide maximum voltage translation flexibility:
  - Over 6.67Mbps operation, ( $R_{PU} = 1k\Omega$ ,  $C_L = 30pF$ )
  - Up translation from 1.2V to 5V with 1.8V supply
  - Down translation from 5V to 0.8V or even less with any valid supply
- Supports standard function pinout
- Latch-up performance exceeds 250mA per JESD 17

## 2 Applications

- [Drive an indicator LED](#)
- [Level-shift using open-drain outputs](#)

## 3 Description

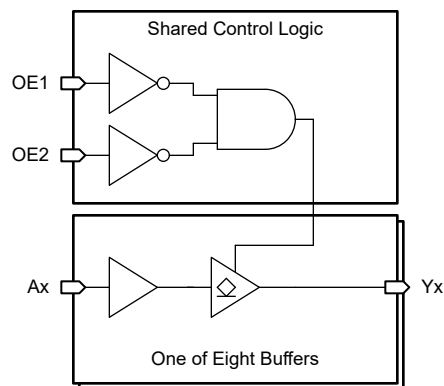
The SN74LV8T7541-Q1 is an octal buffer with open-drain outputs.

The input is designed with a reduced threshold circuit to support up translation when the supply voltage is larger than the input voltage. Additionally, the 5V tolerant input pins enable down translation when the input voltage is larger than the supply voltage. The output level is always referenced to the supply voltage ( $V_{CC}$ ) and supports 1.8V, 2.5V, 3.3V, and 5V CMOS levels.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
SN74LV8T7541-Q1	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm × 4.4mm
	DGS (VSSOP, 20)	5.1mm × 4.9mm	5.1mm × 3.0mm
	RKS (VQFN, 20)	4.5mm × 2.5mm	4.5mm × 2.5mm

- (1) For more information, see [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



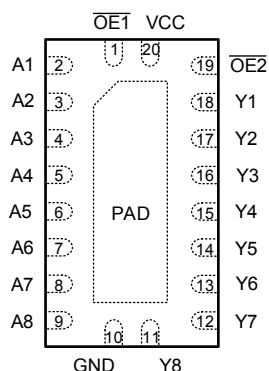
**Functional Block Diagram**



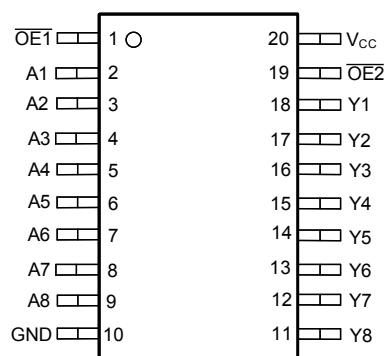
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## 4 Pin Configuration and Functions



**Figure 4-1. SN74LV8T7541-Q1 RKS Package (Top View)**



**Figure 4-2. SN74LV8T7541-Q1 PW, DGS Package (Top View)**

### Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
OE1	1	I	Output enable 1, active low
A1	2	I	Input for channel 1
A2	3	I	Input for channel 2
A3	4	I	Input for channel 3
A4	5	I	Input for channel 4
A5	6	I	Input for channel 5
A6	7	I	Input for channel 6
A7	8	I	Input for channel 7
A8	9	I	Input for channel 8
GND	10	G	Ground
Y8	11	O	Output for channel 8
Y7	12	O	Output for channel 7
Y6	13	O	Output for channel 6
Y5	14	O	Output for channel 5
Y4	15	O	Output for channel 4
Y3	16	O	Output for channel 3
Y2	17	O	Output for channel 2
Y1	18	O	Output for channel 1
OE2	19	I	Output enable 2, active low
V <sub>CC</sub>	20	P	Positive supply
Thermal Pad <sup>(2)</sup>		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.

(2) RKS package only.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>		-0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>		-0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>		-0.5	7	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < -0.5V		-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < -0.5V		-20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		25	mA
	Continuous output current through V <sub>CC</sub> or GND			±75	mA
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Spec	Description	Condition	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		1.65	5.5	V
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65V to 2V	1.1		V
		V <sub>CC</sub> = 2.25V to 2.75V	1.28		
		V <sub>CC</sub> = 3V to 3.6V	1.45		
		V <sub>CC</sub> = 4.5V to 5.5V	2		
V <sub>IL</sub>	Low-Level input voltage	V <sub>CC</sub> = 1.65V to 2 V		0.51	V
		V <sub>CC</sub> = 2.25V to 2.75V		0.65	
		V <sub>CC</sub> = 3V to 3.6V		0.75	
		V <sub>CC</sub> = 4.5V to 5.5V		0.8	
I <sub>O</sub>	Output current	V <sub>CC</sub> = 1.65V to 2 V		8	mA
		V <sub>CC</sub> = 2.25V to 2.75V		15	
		V <sub>CC</sub> = 3.3V to 5.0V		25	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.65V to 5.0V		20	ns/V
Δt/ΔV <sub>CC</sub>	Safe supply ramp rate for POR	V <sub>CC</sub> = 1.65V to 5.5V	6		μs/V

over operating free-air temperature range (unless otherwise noted)

Spec	Description	Condition	MIN	MAX	UNIT
T <sub>A</sub>	Operating free-air temperature		-40	125	°C

## 5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC <sup>(1)</sup>						UNIT
		R <sub>θJA</sub>	R <sub>θJC(top)</sub>	R <sub>θJB</sub>	Ψ <sub>JT</sub>	Ψ <sub>JB</sub>	R <sub>θJC(bot)</sub>	
DGS (VSSOP)	20	131.6	69.5	86.7	10.9	85.9	N/A	°C/W
PW (TSSOP)	20	116.8	58.5	78.7	12.6	77.9	N/A	°C/W
RKS (VQFN)	20	90.4	92.2	63.4	29	63.5	41.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OL</sub>	I <sub>OL</sub> = 50μA	1.65V to 5.5V			0.1		0.01	0.1	V
	I <sub>OL</sub> = 2mA	1.65V to 2V		0.1 <sup>(1)</sup>	0.2		0.1 <sup>(1)</sup>	0.25	
	I <sub>OL</sub> = 3mA	2.25V to 2.75V		0.15 <sup>(1)</sup>	0.17		0.15 <sup>(1)</sup>	0.2	
	I <sub>OL</sub> = 5.5mA	3V to 3.6V		0.2 <sup>(1)</sup>	0.23		0.2 <sup>(1)</sup>	0.25	
	I <sub>OL</sub> = 8mA	4.5V to 5.5V		0.3 <sup>(1)</sup>	0.3		0.3 <sup>(1)</sup>	0.35	
I <sub>I</sub>	V <sub>I</sub> = 0V or V <sub>CC</sub>	0V to 5.5V			±0.1		±0.00 1	±1	μA
I <sub>CC</sub>	V <sub>I</sub> = 0V or V <sub>CC</sub> ; I <sub>O</sub> = 0; open on loading	1.65V to 5.5V			2		0.2	20	μA
ΔI <sub>CC</sub>	One input at 0.3V or 3.4V, other inputs at 0 or V <sub>CC</sub> ; I <sub>O</sub> = 0	5.5V			1.35		0.1	1.5	mA
	One input at 0.3V or 1.1V, other inputs at 0 or V <sub>CC</sub> ; I <sub>O</sub> = 0	1.8V			10		3.4	20	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND and V <sub>CC</sub> = 5.5V	5.5V			±0.25			±2.5	μA
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5V		4	10			10	pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5V		3					pF
C <sub>PD</sub>	No load, F = 1MHz	5V		14					pF
V <sub>POR</sub>	V <sub>CC</sub> ramp rate of 6μs/V to 100ms/V	1.65V to 5.5V			1.5			1.5	V

(1) Typical value at nearest nominal voltage (1.8 V, 2.5 V, 3.3 V, and 5 V)

## 5.6 Switching Characteristics

Over operating free-air temperature range; typical values measured at T<sub>A</sub> = 25°C (unless otherwise noted). See *Parameter Measurement Information*.

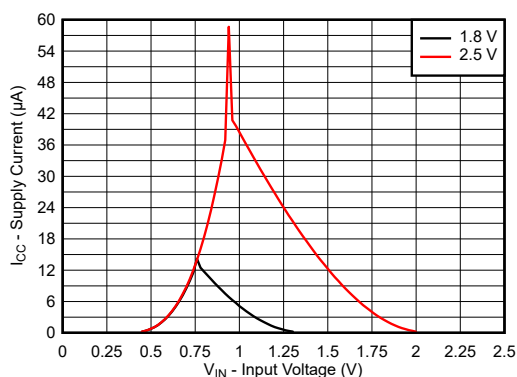
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V <sub>CC</sub>	T <sub>A</sub> = 25°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PZL</sub>	A	Y	C <sub>L</sub> = 15pF	1.8V	15.9		18.4	15.3		19.3	ns
t <sub>PLZ</sub>					8.6		16.8	7.7		18.4	ns
t <sub>PZL</sub>	OE	Y	C <sub>L</sub> = 15pF	1.8V	8.9		17.3	7.8		19.2	ns
t <sub>PLZ</sub>					7.4		10.4	6.8		11.5	ns

Over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted). See *Parameter Measurement Information*.

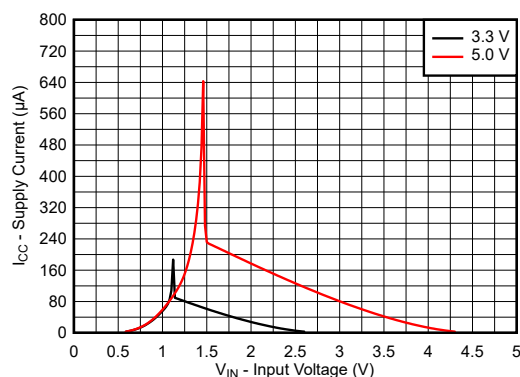
PARAMETER	FROM (INPUT)	TO (OUTPUT )	LOAD CAPACITANCE	$V_{CC}$	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 125^\circ\text{C}$			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PZL}$	A	Y	$C_L = 50\text{pF}$	1.8V	39.1		41.2	38.7		41.5	ns
$t_{PLZ}$					11.5		22.4	10.3		24.9	ns
$t_{PZL}$	$\overline{OE}$	Y	$C_L = 50\text{pF}$	1.8V	11.2		21.2	10		23.5	ns
$t_{PLZ}$					13.9		17.1	13.3		18.2	ns
$t_{sk(o)}$			$C_L = 50\text{pF}$	1.8V			1			1	ns
$t_{PZL}$	A	Y	$C_L = 15\text{pF}$	2.5V	15		16.4	14.7		17	ns
$t_{PLZ}$					6.5		10.9	5.8		12.4	ns
$t_{PZL}$	$\overline{OE}$	Y	$C_L = 15\text{pF}$	2.5V	6.4		10.5	5.5		12.1	ns
$t_{PLZ}$					5.6		7.1	5.1		7.9	ns
$t_{PZL}$	A	Y	$C_L = 50\text{pF}$	2.5V	38.2		39.4	37.9		39.7	ns
$t_{PLZ}$					9		15	7.9		17.2	ns
$t_{PZL}$	$\overline{OE}$	Y	$C_L = 50\text{pF}$	2.5V	8.3		13.3	7.4		15.2	ns
$t_{PLZ}$					9.9		11.5	9.4		12.4	ns
$t_{sk(o)}$			$C_L = 50\text{pF}$	2.5V			1			1	ns
$t_{PZL}$	A	Y	$C_L = 15\text{pF}$	3.3V	14.8		15.8	14.5		16.4	ns
$t_{PLZ}$					5.7		9.3	5.1		10.6	ns
$t_{PZL}$	$\overline{OE}$	Y	$C_L = 15\text{pF}$	3.3V	5.5		8.5	4.8		9.9	ns
$t_{PLZ}$					4.8		6	4.5		6.6	ns
$t_{PZL}$	A	Y	$C_L = 50\text{pF}$	3.3V	37.9		38.8	37.6		39.1	ns
$t_{PLZ}$					8.1		13	7.1		14.8	ns
$t_{PZL}$	$\overline{OE}$	Y	$C_L = 50\text{pF}$	3.3V	7.4		10.9	6.6		12.6	ns
$t_{PLZ}$					8.4		9.6	8.1		10.2	ns
$t_{sk(o)}$			$C_L = 50\text{pF}$	3.3V			1			1	ns
$t_{PZL}$	A	Y	$C_L = 15\text{pF}$	5V							ns
$t_{PLZ}$					4.4		6.9	4		7.9	ns
$t_{PZL}$	$\overline{OE}$	Y	$C_L = 15\text{pF}$	5V	4		5.7	3.5		6.8	ns
$t_{PLZ}$					4.7		5.4	4.5		5.8	ns
$t_{PZL}$	A	Y	$C_L = 50\text{pF}$	5V							ns
$t_{PLZ}$					6.5		9.9	5.9		11.2	ns
$t_{PZL}$	$\overline{OE}$	Y	$C_L = 50\text{pF}$	5V	5.5		7.8	5		8.9	ns
$t_{PLZ}$					6.9		7.6	6.7		8.1	ns
$t_{sk(o)}$			$C_L = 50\text{pF}$	5V			1			1	ns

## 5.7 Typical Characteristics

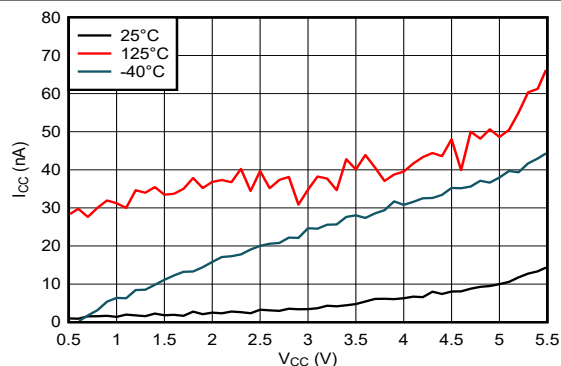
$T_A = 25^\circ\text{C}$  (unless otherwise noted)



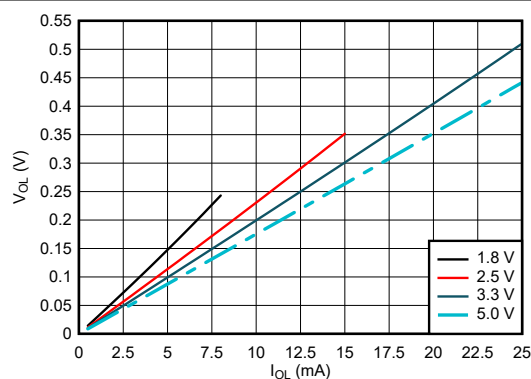
**Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply**



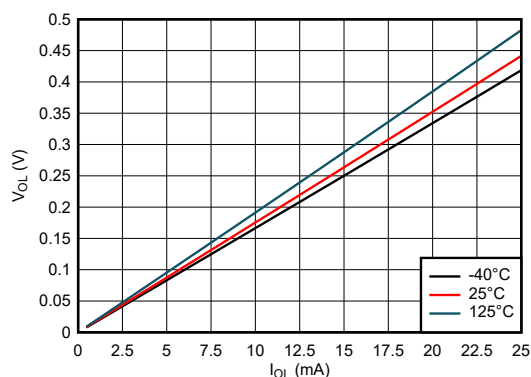
**Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply**



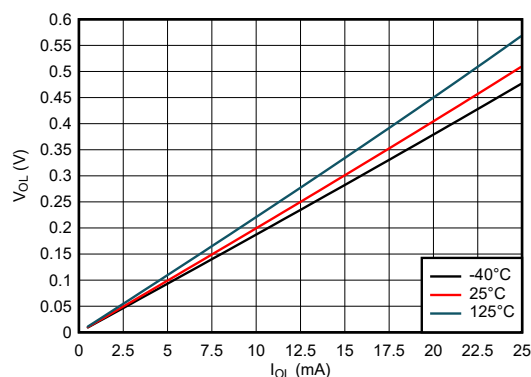
**Figure 5-3. Supply Current Across Supply Voltage**



**Figure 5-4. Output Voltage vs Current in LOW State**



**Figure 5-5. Output Voltage vs Current in LOW State; 5V Supply**



**Figure 5-6. Output Voltage vs Current in LOW State; 3.3V Supply**

## 5.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

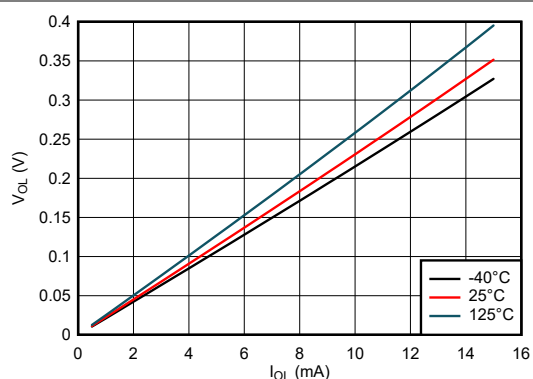


Figure 5-7. Output Voltage vs Current in LOW State; 2.5V Supply

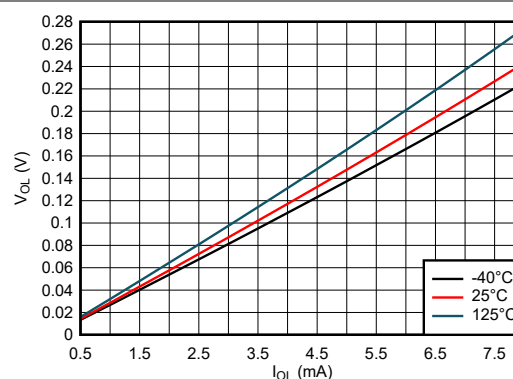


Figure 5-8. Output Voltage vs Current in LOW State; 1.8V Supply

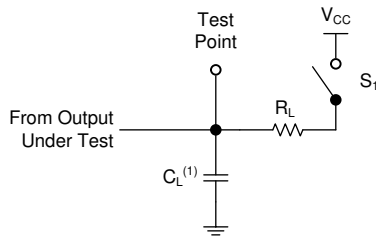


## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{MHz}$ ,  $Z_O = 50\Omega$ ,  $t_f < 2.5\text{ns}$ .

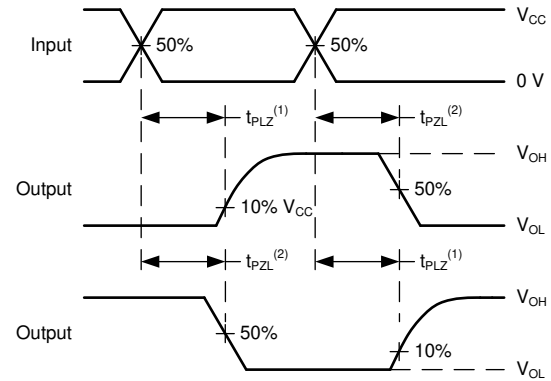
The outputs are measured individually with one input transition per measurement.

TEST	S1	$R_L$	$C_L$	$\Delta V$	$V_{CC}$
$t_{PLZ}$ , $t_{PZL}$	CLOSED	1k $\Omega$	15pF, 50pF	0.15V	$\leq 2.5\text{V}$
$t_{PLZ}$ , $t_{PZL}$	CLOSED	1k $\Omega$	15pF, 50pF	0.3V	$> 2.5\text{V}$



(1)  $C_L$  includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for Open-Drain Outputs**



(1)  $t_{PLZ}$  is the same as  $t_{dis}$ .

(2)  $t_{PZL}$  is the same as  $t_{en}$ .

**Figure 6-2. Voltage Waveforms Propagation Delays**

## 7 Detailed Description

### 7.1 Overview

The SN74LV8T7541-Q1 contains eight buffers with open-drain outputs. The active low output enable pins ( $\overline{OE1}$  and  $\overline{OE2}$ ) control all eight channels, and are configured so that both must be low for the outputs to be active.

When the outputs are enabled, the outputs are actively driven low or set into the high-impedance state.

When the outputs are disabled, the outputs are set into the high-impedance state.

### 7.2 Functional Block Diagram

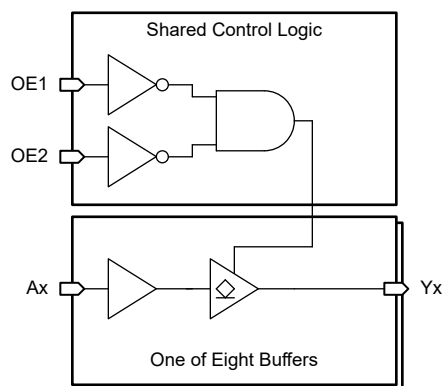


Figure 7-1. Logic Diagram (Positive Logic)

## 7.3 Feature Description

### 7.3.1 Open-Drain CMOS Outputs

This device includes open-drain CMOS outputs. Open-drain outputs can only drive the output low. When in the high logical state, open-drain outputs are in a high-impedance state. The drive capability of this device can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the device output power to avoid damage due to overcurrent. Follow the electrical and thermal limits defined in the *Absolute Maximum Ratings* at all times.

When placed into the high-impedance state, the output neither sources nor sinks current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor depends on multiple factors, including parasitic capacitance and power consumption limitations. Typically, use a 10k $\Omega$  resistor to meet these requirements.

Leave unused open-drain CMOS outputs disconnected.

### 7.3.2 LVxT Enhanced Input Voltage

The SN74LV8T7541-Q1 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5V levels to support down-translation. For proper functionality, input signals must remain at or above the specified  $V_{IH(MIN)}$  level for a HIGH input state, and at or below the specified  $V_{IL(MAX)}$  for a LOW input state. Figure 7-2 shows the typical  $V_{IH}$  and  $V_{IL}$  levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

Input signals must transition between valid logic states quickly, as defined by the input transition rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the [Implications of Slow or Floating CMOS Inputs](#) application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at a valid high or low voltage level. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and will typically meet all requirements.

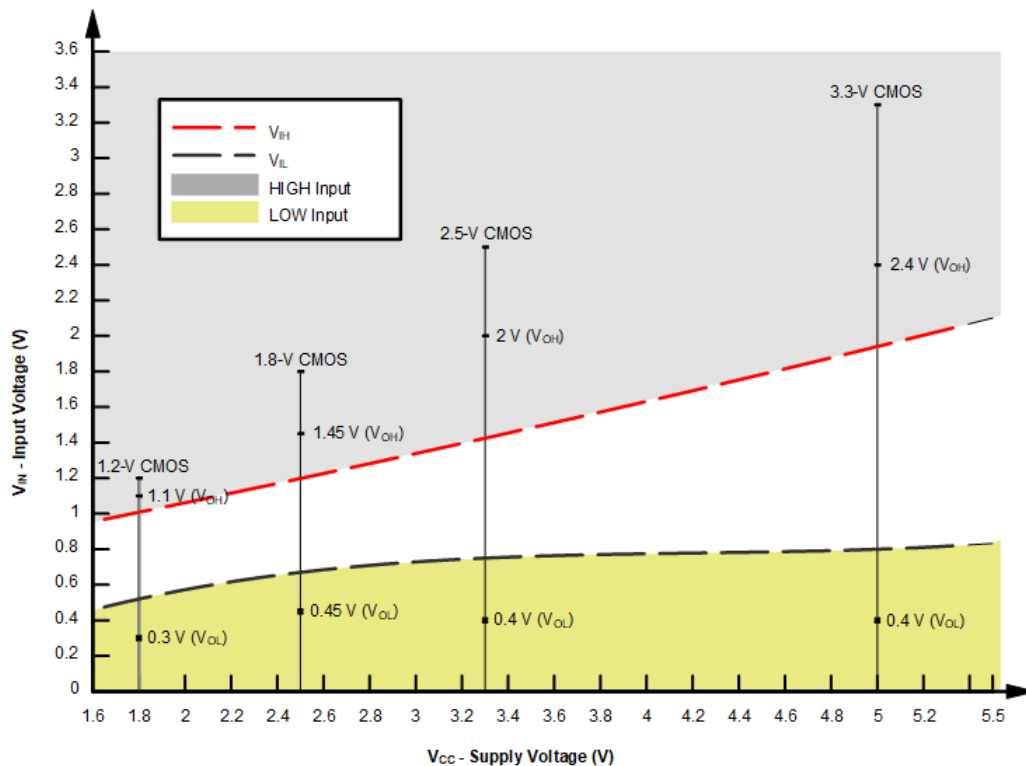


Figure 7-2. LVxT Input Voltage Levels

### 7.3.2.1 Up Translation

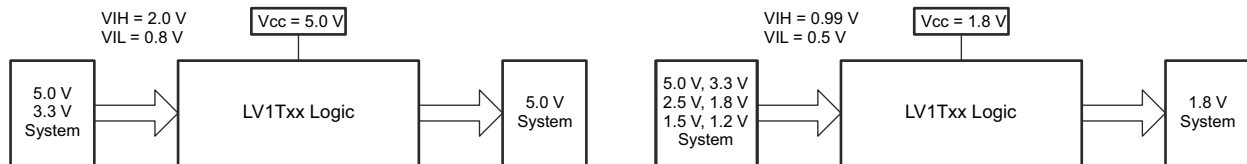
Input signals can be up translated using the SN74LV8T7541-Q1. The voltage applied at  $V_{CC}$  will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately  $V_{CC}$  in the HIGH state, and 0V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels, which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5V supply will have a  $V_{IH(MIN)}$  of 3.5V. For the SN74LV8T7541-Q1,  $V_{IH(MIN)}$  with a 5V supply is only 2V, which would allow for up-translation from a typical 2.5V to 5V signals.

Ensure that the input signals in the HIGH state are above  $V_{IH(MIN)}$  and input signals in the LOW state are lower than  $V_{IL(MAX)}$  as shown in [Figure 7-3](#).

*Up Translation Combinations* are as follows:

- 1.8V  $V_{CC}$  – Inputs from 1.2V
- 2.5V  $V_{CC}$  – Inputs from 1.8V
- 3.3V  $V_{CC}$  – Inputs from 1.8V and 2.5V
- 5.0V  $V_{CC}$  – Inputs from 2.5V and 3.3V



**Figure 7-3. LVxT Up and Down Translation Example**

### 7.3.2.2 Down Translation

Signals can be translated down using the SN74LV8T7541-Q1. The voltage applied at the  $V_{CC}$  will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately  $V_{CC}$  in the HIGH state, and 0V in the LOW state. Ensure that the input signals in the HIGH state are between  $V_{IH(MIN)}$  and 5.5V, and input signals in the LOW state are lower than  $V_{IL(MAX)}$  as shown in [Figure 7-2](#).

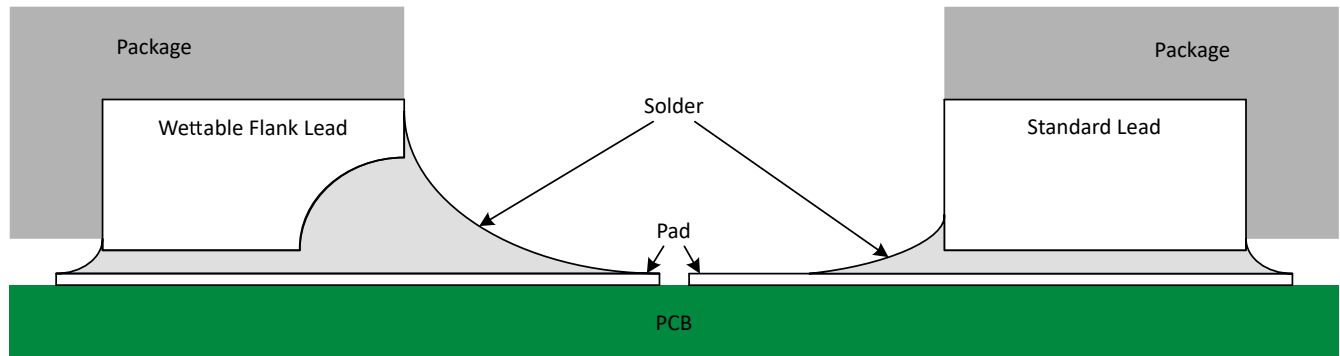
For example, standard CMOS inputs for devices operating at 5.0V, 3.3V or 2.5V can be down-translated to match 1.8V CMOS signals when operating from 1.8V  $V_{CC}$ . See [Figure 7-3](#).

*Down Translation Combinations* are as follows:

- 1.8V  $V_{CC}$  – Inputs from 2.5V, 3.3V, and 5.0V
- 2.5V  $V_{CC}$  – Inputs from 3.3V and 5.0V
- 3.3V  $V_{CC}$  – Inputs from 5.0V

### 7.3.3 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet where packages include this feature.



**Figure 7-4. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering**

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in [Figure 7-4](#), a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

### 7.3.4 Clamp Diode Structure

Figure 7-5 shows the inputs and outputs to this device have negative clamping diodes only.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

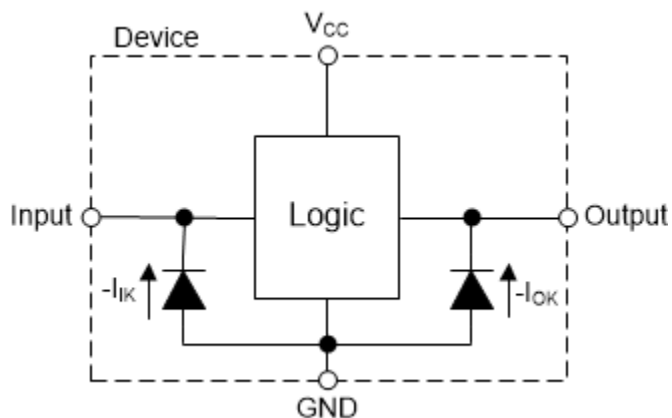


Figure 7-5. Electrical Placement of Clamping Diodes for Each Input and Output

## 7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS <sup>(1)</sup>			OUTPUT <sup>(2)</sup>
OE1	OE2	A	Y
L	L	L	L
L	L	H	Z
H	X	X	Z
X	H	X	Z

(1) L = input low, H = input high, X = do not care

(2) L = output low, Z = high impedance

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

Open-drain outputs like those available in the SN74LV8T7541-Q1 provide the ability to discharge a voltage node to ground without otherwise loading the node significantly. It is recommended to add a series resistor between the output and any capacitance larger than 50pF as shown in the *Typical Application Block Diagram* to prevent damage to the device.

The required resistor value can be determined using the maximum capacitor voltage and the maximum continuous current for the output from the equation:  $R \geq V_C / I_{O(max)}$ .

For any given RC combination, the discharge time can be determined using the discharge plot provided in the *Application Timing Diagram* and the equation  $\tau = R \times C$ . For example, to discharge a capacitor to 10% of the starting value, it takes approximately  $2.303 \times \tau = 2.303 \times R \times C$  seconds.

### 8.2 Typical Application

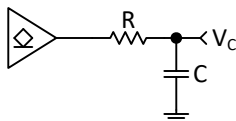


Figure 8-1. Typical Application Block Diagram



## 8.2.1 Design Requirements

### 8.2.1.1 Power Considerations

Ensure that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics of the device, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV8T7541-Q1 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LV8T7541-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LV8T7541-Q1 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#).

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 8.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV8T7541-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k $\Omega$  resistor value is often used due to these factors.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

### 8.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

## 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is  $\leq 50\text{pF}$ . This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV8T7541-Q1 to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than  $(V_{CC} / I_{O(max)})\Omega$ . Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in  $M\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

## 8.2.3 Application Curves

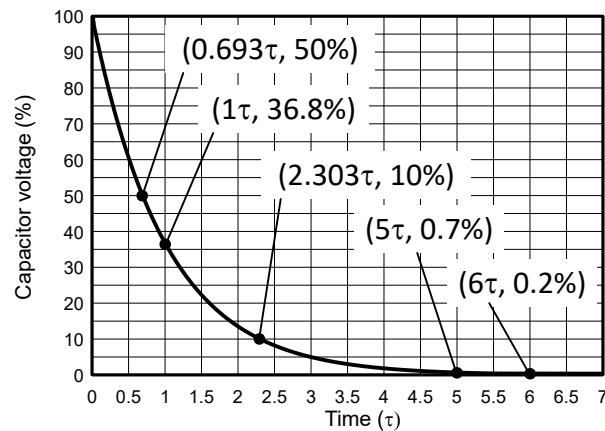


Figure 8-2. Application Timing Diagram

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance.

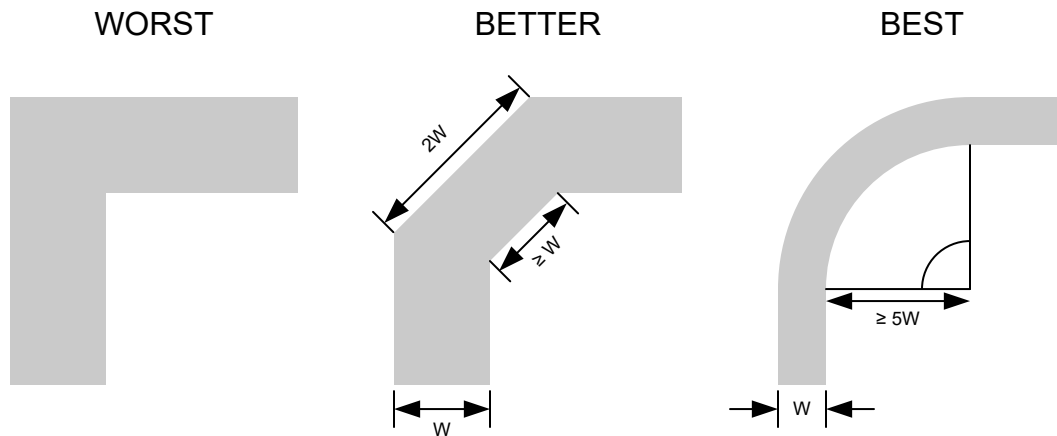
A 0.1 $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1 $\mu$ F and 1 $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 8.4 Layout

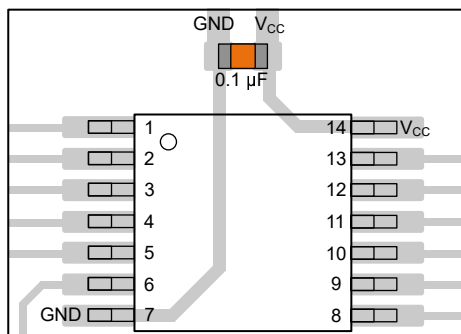
### 8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

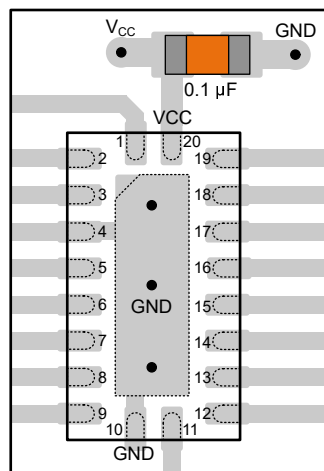
### 8.4.2 Layout Example



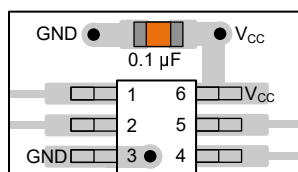
**Figure 8-3. Example Trace Corners for Improved Signal Integrity**



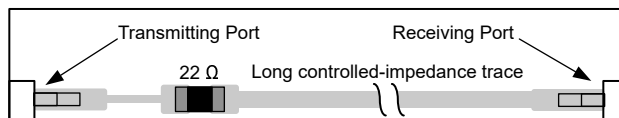
**Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages**



**Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages**



**Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**



**Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity**

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and  \$C\_{pd}\$  Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.4 Trademarks

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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2025	*	Initial Release

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CLV8T7541QDGSRQ1	Active	Production	VSSOP (DGS)   20	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T7541Q
CLV8T7541QWRKSRQ1	Active	Production	VQFN (RKS)   20	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8T7541Q
SN74LV8T7541QPWRQ1	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V8T7541Q

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### OTHER QUALIFIED VERSIONS OF SN74LV8T7541-Q1 :

- Catalog : [SN74LV8T7541](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product





## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

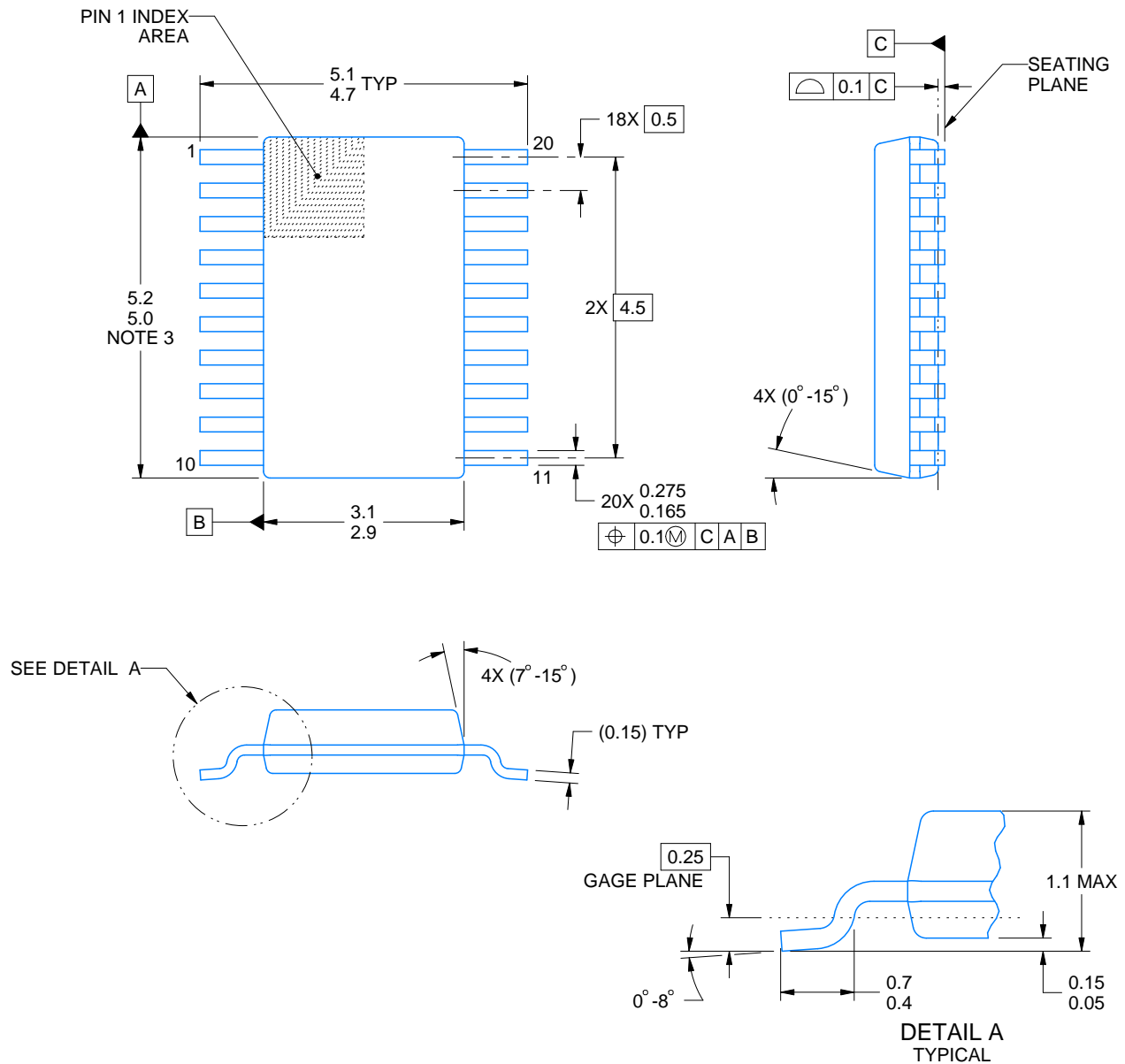
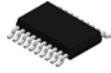


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4226367/A 10/2020

## NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES: (continued)

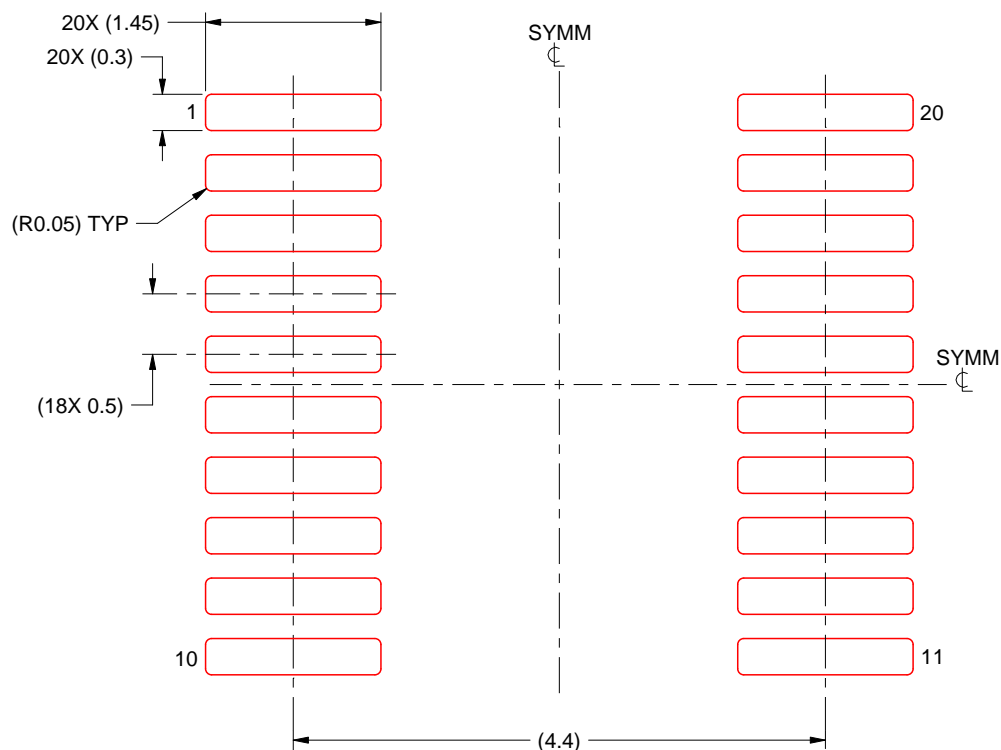
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**RKS 20**

**VQFN - 1 mm max height**

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



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Last updated 10/2025