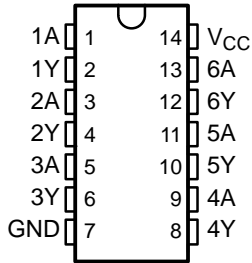


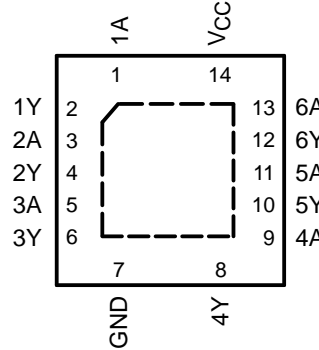
FEATURES

- Operate From 1.65 V to 3.6 V
- Specified From -40°C to 85°C , -40°C to 125°C , and -55°C to 125°C
- Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V
- Max t_{pd} of 3.7 ns at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17

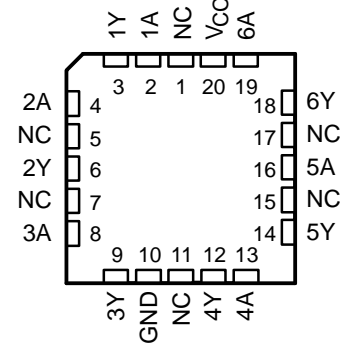
SN54LVC06A . . . J OR W PACKAGE
SN74LVC06A . . . D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVC06A . . . RGY PACKAGE
(TOP VIEW)



SN54LVC06A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

These hex inverter buffers/drivers are designed for 1.65-V to 3.6-V V_{CC} operation.

The outputs of the 'LVC06A devices are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|--|------------------------|----------------|-----------------------|------------------|
| -40°C to 85°C | QFN – RGY | Reel of 1000 | SN74LVC06ARGYR | LC06A |
| -40°C to 125°C | SOIC – D | Tube of 50 | SN74LVC06AD | LVC06A |
| | | Reel of 2500 | SN74LVC06ADR | |
| | | Reel of 250 | SN74LVC06ADT | |
| | SOP – NS | Reel of 2000 | SN74LVC06ANSR | LVC06A |
| | SSOP – DB | Reel of 2000 | SN74LVC06ADBR | LC06A |
| | TSSOP – PW | Tube of 90 | SN74LVC06APW | LC06A |
| | | Reel of 2000 | SN74LVC06APWR | |
| Reel of 250 | | SN74LVC06APWT | | |
| TVSOP – DGV | Reel of 2000 | SN74LVC06ADGVR | LC06A | |
| -55°C to 125°C | CDIP – J | Tube of 25 | SNJ54LVC06AJ | SNJ54LVC06AJ |
| | CFP – W | Tube of 150 | SNJ54LVC06AW | SNJ54LVC06AW |
| | LCCC – FK | Tube of 55 | SNJ54LVC06AFK | SNJ54LVC06AFK |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE
(EACH INVERTER)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

LOGIC DIAGRAM, EACH INVERTER (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|--|---|------|------|
| V_{CC} | Supply voltage range | -0.5 | 6.5 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 6.5 | V |
| V_O | Output voltage range | -0.5 | 6.5 | V |
| I_{IK} | Input clamp current | | -50 | mA |
| I_{OK} | Output clamp current | | -50 | mA |
| I_O | Continuous output current | | ±50 | mA |
| | Continuous current through V_{CC} or GND | | ±100 | mA |
| θ_{JA} | Package thermal impedance | D package ⁽³⁾ | 86 | °C/W |
| | | DB package ⁽³⁾ | 96 | |
| | | DGV package ⁽³⁾ | 127 | |
| | | NS package ⁽³⁾ | 76 | |
| | | PW package ⁽³⁾ | 113 | |
| | | RGY package ⁽⁴⁾ | 47 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |
| P_{tot} | Power dissipation ⁽⁵⁾⁽⁶⁾ | | 500 | mW |
| | | $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ | | |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) The package thermal impedance is calculated in accordance with JESD 51-5.
- (5) For the D package: above 70°C the value of P_{tot} derates linearly with 8 mW/K.
- (6) For the DB, DGV, NS, and PW packages: above 60°C the value of P_{tot} derates linearly with 5.5 mW/K.

Recommended Operating Conditions⁽¹⁾

| | | SN54LVC06A ⁽²⁾ | | UNIT | |
|-----------------|--------------------------|------------------------------------|------------------------|------|----|
| | | –55°C to 125°C | | | |
| | | MIN | MAX | | |
| V _{CC} | Supply voltage | Operating | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.35 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 0.8 | | |
| V _I | Input voltage | 0 | 5.5 | | V |
| V _O | Output voltage | 0 | 5.5 | | V |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | 4 | | mA |
| | | V _{CC} = 2.3 V | 8 | | |
| | | V _{CC} = 2.7 V | 12 | | |
| | | V _{CC} = 3 V | 24 | | |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Product preview

Recommended Operating Conditions⁽¹⁾

| | | SN74LVC06A | | | | | | UNIT | |
|-----------------|--------------------------|------------------------------------|------------------------|---------------|------------------------|----------------|------------------------|------|----|
| | | T _A = 25°C | | –40°C to 85°C | | –40°C to 125°C | | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| V _{CC} | Supply voltage | Operating | 1.65 | 3.6 | 1.65 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | 1.5 | | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | 0.65 × V _{CC} | | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | 1.7 | | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 2 | | 2 | | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.35 × V _{CC} | | 0.35 × V _{CC} | | 0.35 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | | 0.7 | | 0.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 0.8 | | 0.8 | | 0.8 | | |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | 0 | 5.5 | V | |
| V _O | Output voltage | 0 | 5.5 | 0 | 5.5 | 0 | 5.5 | V | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | 4 | | 4 | | 4 | | mA |
| | | V _{CC} = 2.3 V | 8 | | 8 | | 8 | | |
| | | V _{CC} = 2.7 V | 12 | | 12 | | 12 | | |
| | | V _{CC} = 3 V | 24 | | 24 | | 24 | | |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVC06A, SN74LVC06A HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

SCAS596N–OCTOBER 1997–REVISED JULY 2005

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | SN54LVC06A ⁽¹⁾ | | UNIT |
|------------------|--|-----------------|---------------------------|------------------------|------|
| | | | –55°C to 125°C | | |
| | | | MIN | TYP ⁽²⁾ MAX | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | 0.2 | | V |
| | I _{OL} = 4 mA | 1.65 V | 0.45 | | |
| | I _{OL} = 8 mA | 2.3 V | 0.7 | | |
| | I _{OL} = 12 mA | 2.7 V | 0.4 | | |
| | I _{OL} = 24 mA | 3 V | 0.55 | | |
| I _I | V _I = 5.5 V or GND | 3.6 V | ±5 | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | 10 | | μA |
| ΔI _{CC} | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | 500 | | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | 5 | | pF |

(1) Product preview

(2) T_A = 25°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | SN74LVC06A | | | | | | UNIT | |
|------------------|--|-----------------|-----------------------|-----|-----|---------------|-----|----------------|------|-----|
| | | | T _A = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | | MAX |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | 0.1 | | | 0.2 | | 0.3 | | V |
| | I _{OL} = 4 mA | 1.65 V | 0.24 | | | 0.45 | | 0.6 | | |
| | I _{OL} = 8 mA | 2.3 V | 0.3 | | | 0.7 | | 0.75 | | |
| | I _{OL} = 12 mA | 2.7 V | 0.4 | | | 0.4 | | 0.6 | | |
| | I _{OL} = 24 mA | 3 V | 0.55 | | | 0.55 | | 0.8 | | |
| I _I | V _I = 5.5 V or GND | 3.6 V | ±1 | | | ±5 | | ±20 | | μA |
| I _{off} | V _I or V _O = 5.5 V | 0 | ±1 | | | ±10 | | ±20 | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | 1 | | | 10 | | 40 | | μA |
| ΔI _{CC} | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | 500 | | | 500 | | 5000 | | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | 5 | | | | | | | pF |

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | SN54LVC06A ⁽¹⁾ | | UNIT |
|-----------------|--------------|-------------|-----------------|---------------------------|-----|------|
| | | | | –55°C to 125°C | | |
| | | | | MIN | MAX | |
| t _{pd} | A | Y | 1.8 V ± 0.15 V | 1.4 | 5.6 | ns |
| | | | 2.5 V ± 0.2 V | 1 | 3.1 | |
| | | | 2.7 V | | 3.9 | |
| | | | 3.3 V ± 0.3 V | 1 | 3.7 | |

(1) Product preview

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

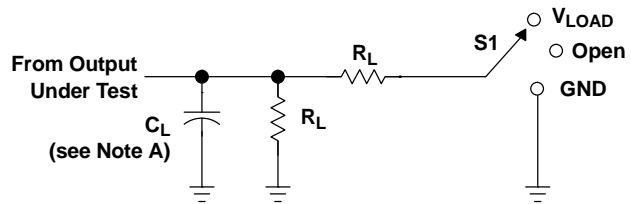
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | SN74LVC06A | | | | | | UNIT | |
|-----------------|-----------------|----------------|-----------------|-----------------------|-----|-----|---------------|-----|----------------|------|-----|
| | | | | T _A = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | | MAX |
| t _{pd} | A | Y | 1.8 V ± 0.15 V | 1.4 | 3 | 5.1 | 1.4 | 5.6 | 1.4 | 7.6 | ns |
| | | | 2.5 V ± 0.2 V | 1 | 1.9 | 2.8 | 1 | 3.1 | 1 | 4 | |
| | | | 2.7 V | 1 | 2.4 | 3.7 | 1 | 3.9 | 1 | 5 | |
| | | | 3.3 V ± 0.3 V | 1 | 2.2 | 3.5 | 1 | 3.7 | 1 | 5 | |

Operating Characteristics

T_A = 25°C

| PARAMETER | | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|-----------------|---|--------------------|-----------------|-----|------|
| C _{pd} | Power dissipation capacitance per buffer/driver | f = 10 MHz | 1.8 V | 2.1 | pF |
| | | | 2.5 V | 2.3 | |
| | | | 3.3 V | 2.5 | |

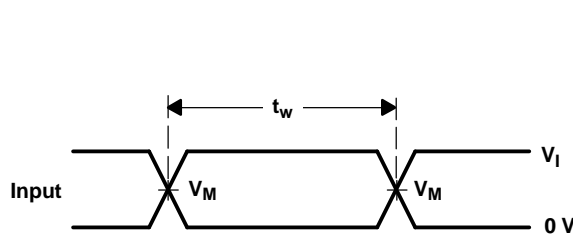
PARAMETER MEASUREMENT INFORMATION
 (OPEN DRAIN)



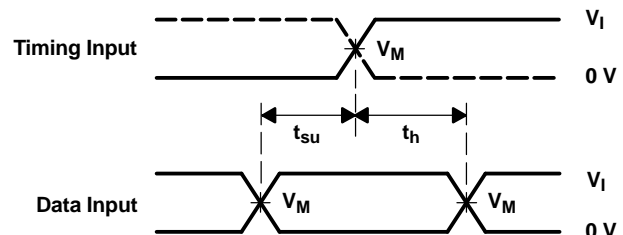
| TEST | S1 |
|-------------------------------|------------|
| t_{PZL} (see Notes E and F) | V_{LOAD} |
| t_{PLZ} (see Notes E and G) | V_{LOAD} |
| t_{PHZ}/t_{PZH} | V_{LOAD} |

LOAD CIRCUIT

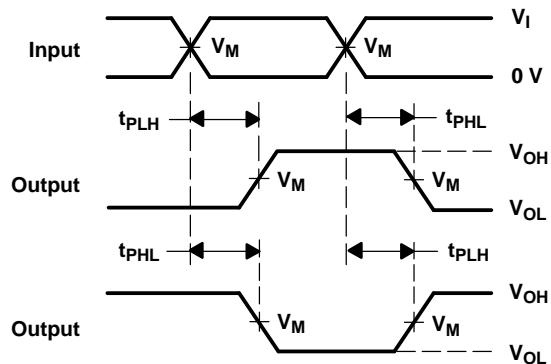
| V_{CC} | INPUT | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|--------------------|----------|---------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8 V \pm 0.15 V$ | V_{CC} | $\leq 2 ns$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5 V \pm 0.2 V$ | V_{CC} | $\leq 2 ns$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5 ns$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3 V \pm 0.3 V$ | 2.7 V | $\leq 2.5 ns$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



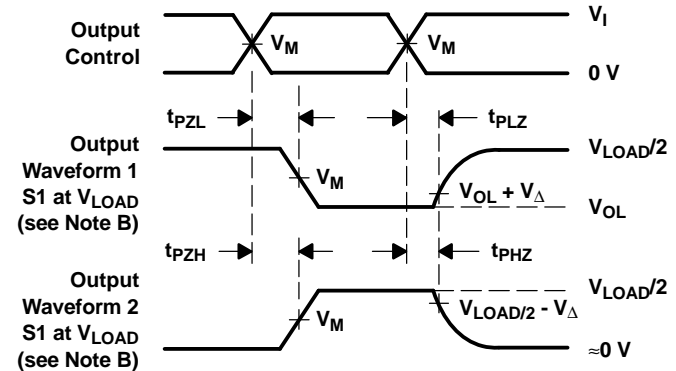
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
 F. t_{PZL} is measured at V_M .
 G. t_{PLZ} is measured at $V_{OL} + V_{\Delta}$.
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC06AD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC06A | Samples |
| SN74LVC06ADBR | ACTIVE | SSOP | DB | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC06A | Samples |
| SN74LVC06ADE4 | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC06A | Samples |
| SN74LVC06ADGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC06A | Samples |
| SN74LVC06ADR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC06A | Samples |
| SN74LVC06ADRE4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC06A | Samples |
| SN74LVC06ADT | ACTIVE | SOIC | D | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC06A | Samples |
| SN74LVC06ANSR | ACTIVE | SOP | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC06A | Samples |
| SN74LVC06APW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC06A | Samples |
| SN74LVC06APWG4 | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC06A | Samples |
| SN74LVC06APWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC06A | Samples |
| SN74LVC06APWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC06A | Samples |
| SN74LVC06APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC06A | Samples |
| SN74LVC06APWT | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC06A | Samples |
| SN74LVC06ARGYR | ACTIVE | VQFN | RGY | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC06A | Samples |
| SN74LVC06ARGYRG4 | ACTIVE | VQFN | RGY | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC06A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC06A :

- Automotive : [SN74LVC06A-Q1](#)
- Enhanced Product : [SN74LVC06A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC06ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LVC06ADGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC06ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC06ADT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC06ANSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC06APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC06APWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC06ARGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC06ADBR | SSOP | DB | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC06ADGVR | TVSOP | DGV | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC06ADR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74LVC06ADT | SOIC | D | 14 | 250 | 210.0 | 185.0 | 35.0 |
| SN74LVC06ANSR | SOP | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC06APWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC06APWT | TSSOP | PW | 14 | 250 | 356.0 | 356.0 | 35.0 |
| SN74LVC06ARGYR | VQFN | RGY | 14 | 3000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVC06AD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LVC06ADE4 | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LVC06APW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVC06APWG4 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



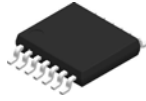
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

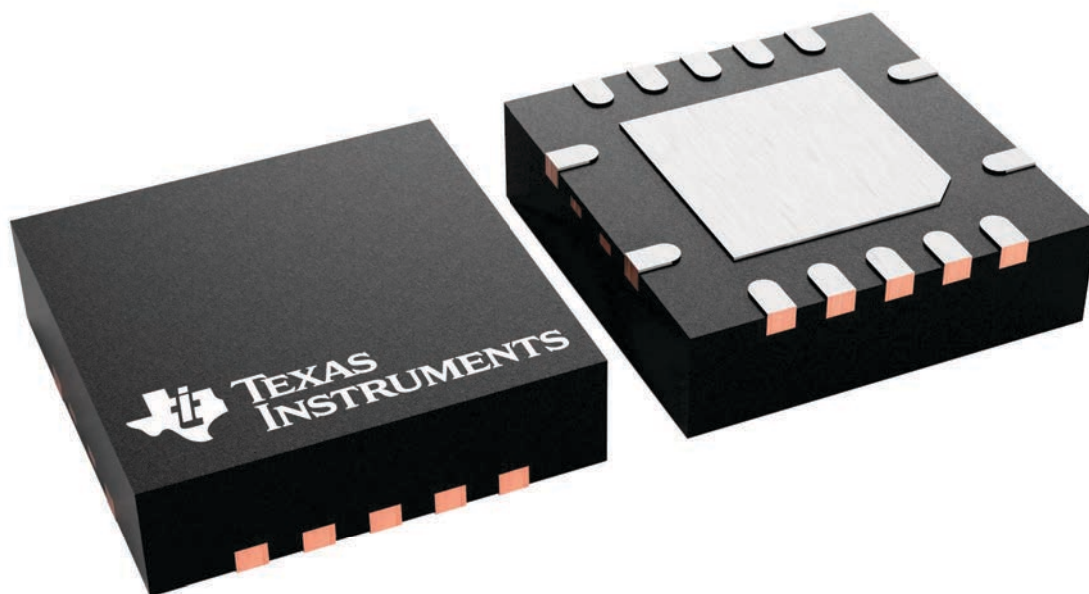
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

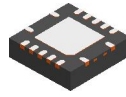
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A

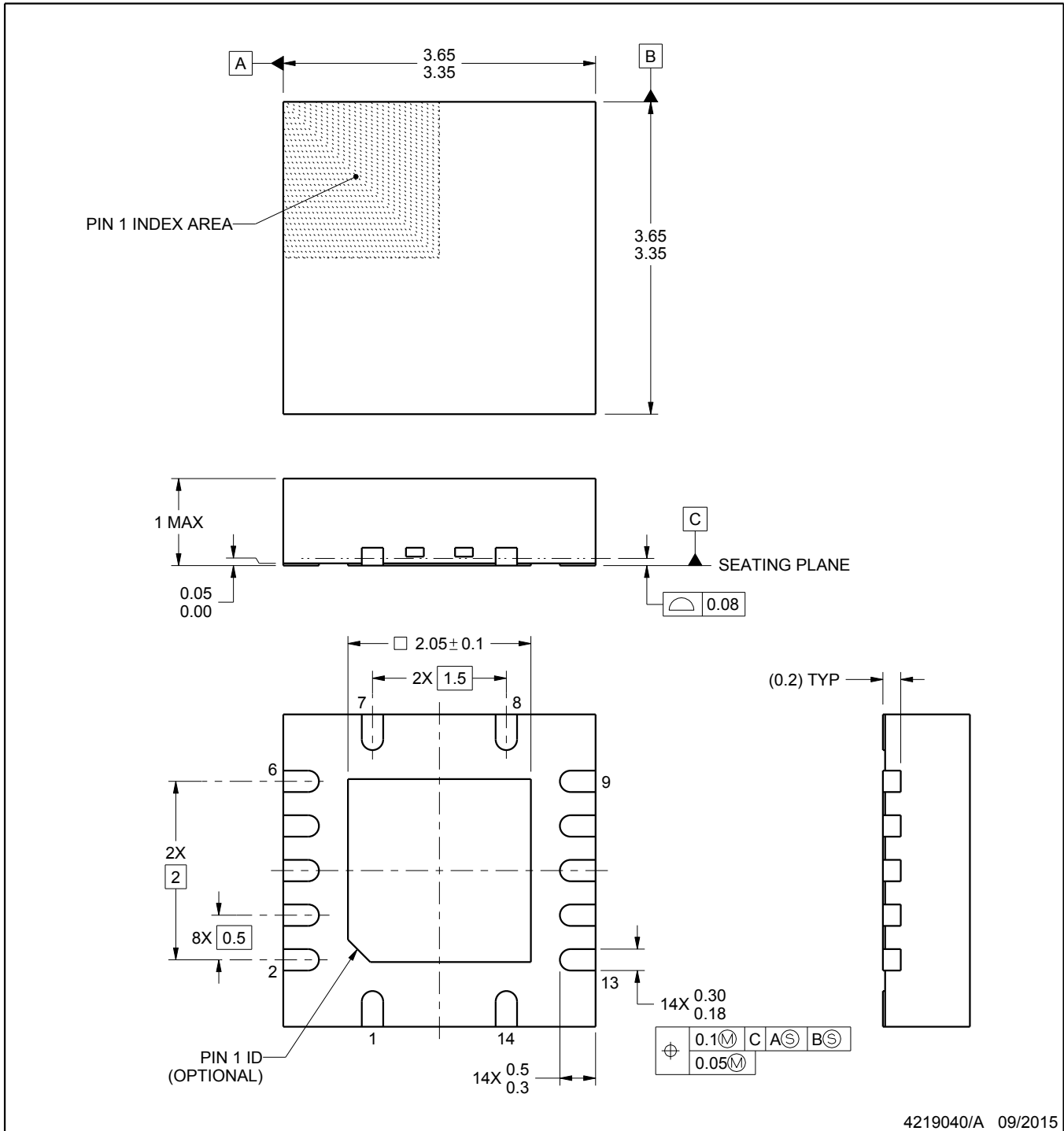
RGY0014A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

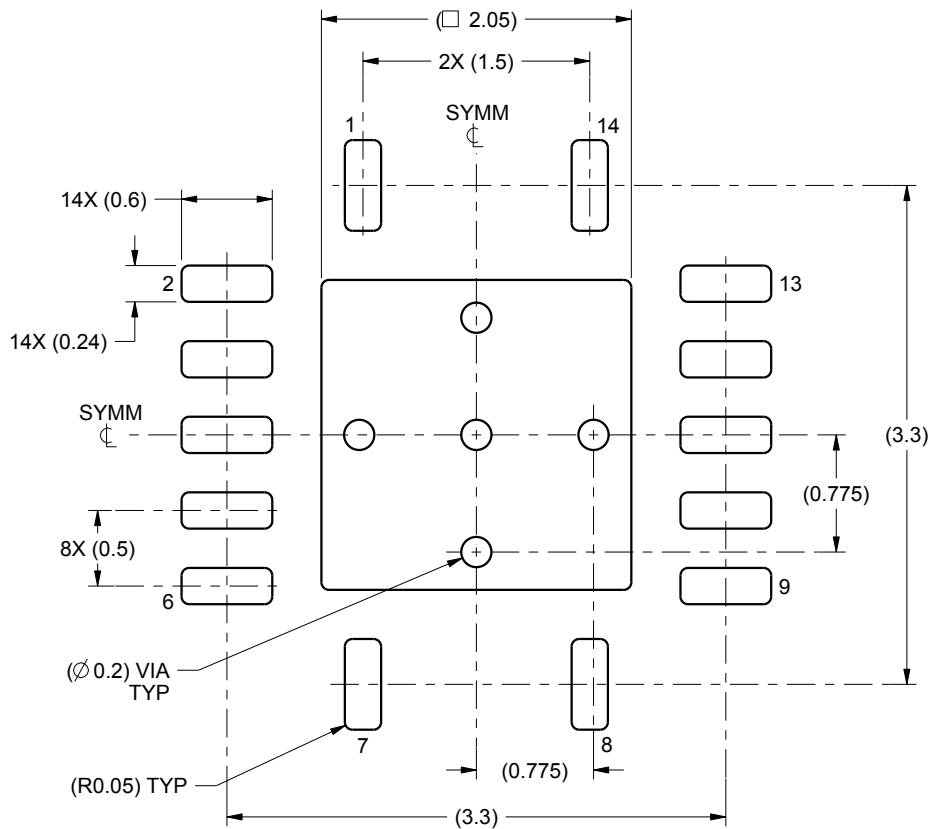
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

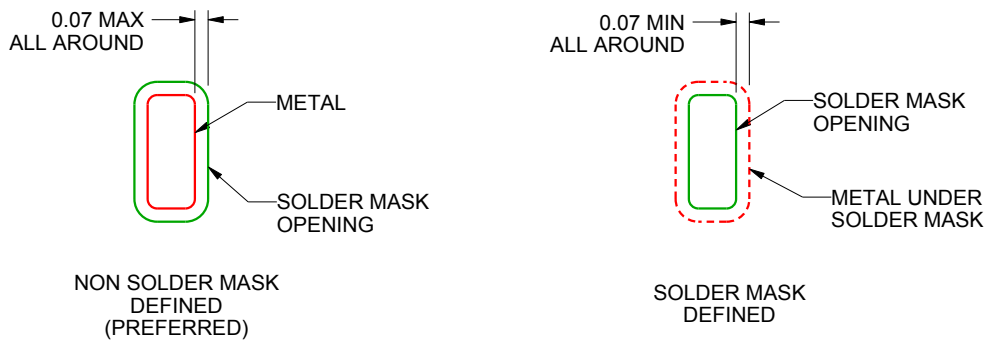
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

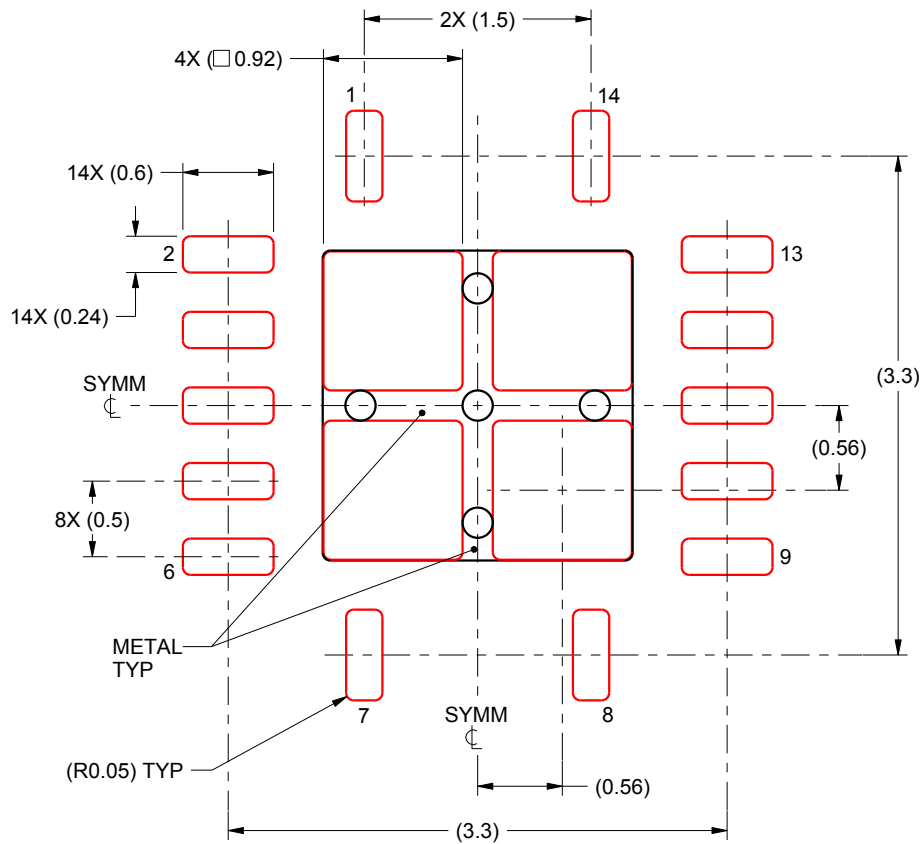
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated