# SN74LVC112A Dual Negative-Edge-Triggered J-K Flip-Flop With Clear and Preset

## 1 Features

- Operates from 1.65V to 3.6V
- Inputs accept voltages to 5.5V
- Max $t_{pd}$ of 4.8ns at 3.3V
- Typical $V_{OLP}$ (output ground bounce) < 0.8V at $V_{CC}$ = 3.3V, $T_A$ = 25°C
- Typical $V_{OHV}$ (output $V_{OH}$ undershoot) > 2V at $V_{CC}$ = 3.3V, $T_A$ = 25°C
- Latch-up performance exceeds 250mA per JESD 17

## 2 Applications

- Servers
- PCs
- Notebooks
- Network switches
- Toys
- I/O Expanders
- Electronic Points of Sale

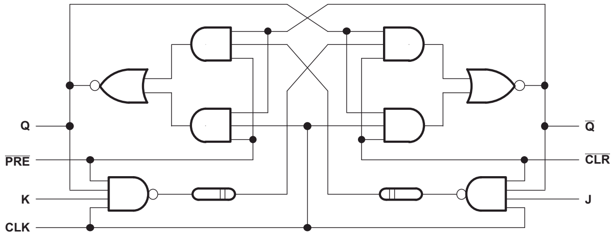
## 3 Description

This dual negative-edge-triggered J-K flip-flop is designed for 1.65V to 3.6V $V_{CC}$ operation.

**Package Information**

| PART NUMBER | PACKAGE[1] | PACKAGE SIZE[2] | BODY SIZE[3] |
|---|---|---|---|
| SN74LVC112A | DB (SSOP, 16) | 6.20mm × 7.8mm | 6.20mm × 5.30mm |
| | PW (TSSOP, 16) | 5.00mm × 6.4mm | 5.00 mm × 4.40 mm |
| | DGV (TVSOP, 16) | 3.6mm × 6.4mm | 3.60mm x 4.40mm |
| | NS (SOP, 16) | 10.2mm × 7.8mm | 10.20mm x 5.30mm |
| | D (SOIC, 16) | 9.90 mm × 6mm | 9.90mm × 3.90mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Simplified Schematic

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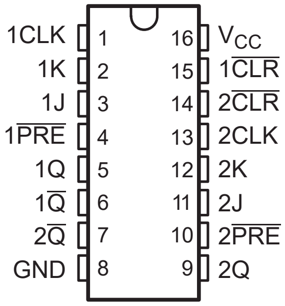
# 4 Pin Configuration and Functions

**D, DB, DGV, NS, OR PW PACKAGE**
**(TOP VIEW)**



## Pin Functions

**Table 4-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | 1CLK | I | 1 Clock |
| 2 | 1K | I | 1K Input |
| 3 | 1J | I | 1J Input |
| 4 | 1 $\overline{\text{PRE}}$ | I | 1 Preset |
| 5 | 1Q | O | 1Q Output. Pull low to set 1Q high and 1 $\overline{\text{Q}}$ low upon power-up. |
| 6 | 1 $\overline{\text{Q}}$ | O | 1 $\overline{\text{Q}}$ Output |
| 7 | 2 $\overline{\text{Q}}$ | O | 2 $\overline{\text{Q}}$ Output |
| 8 | GND | — | Ground Pin |
| 9 | 2Q | O | 2Q Output |
| 10 | 2 $\overline{\text{PRE}}$ | I | 2 Preset |
| 11 | 2J | I | 2J Input. Pull low to set 2Q high and 2 $\overline{\text{Q}}$ low upon power-up. |
| 12 | 2K | I | 2K Input |
| 13 | 2CLK | I | 2 Clock |
| 14 | 2 $\overline{\text{CLR}}$ | I | 2 Clear |
| 15 | 1 $\overline{\text{CLR}}$ | I | 1 Clear. Pull low to set 2Q low and 2 $\overline{\text{Q}}$ high upon power-up. |
| 16 | $V_{CC}$ | — | Power Pin. Pull low to set 1Q low and 1 $\overline{\text{Q}}$ high upon power-up. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage(2) | | –0.5 | 6.5 | V |
| $V_O$ | Output voltage(2) (3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_{stg}$ | Storage temperature | | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the *Recommended Operating Conditions* table.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | |
| | | $V_{CC}$ = 2.7 V | | –12 | |
| | | $V_{CC}$ = 3 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 5.4 Thermal Information

| THERMAL METRIC(1) | | SN74LVC112A | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | D (SOIC) | DB (SSOP) | DGV (TVSOP) | NS (SOP) | PW (TSSOP) | |
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 118.1 | 122.5 | 129.0 | 117.5 | 141.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 81.6 | 75.2 | 52.1 | 76 | 51.4 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 80 | 85.5 | 62.0 | 84.2 | 64.4 | |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 36.3 | 30.5 | 6.5 | 34.2 | 6.7 | |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 79.2 | 84.1 | 61.3 | 83.1 | 63.8 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | |

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C |  |  | –40°C to +85°C |  | –40°C to +125°C |  | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
|  |  |  | MIN | TYP(1) | MAX | MIN | MAX | MIN | MAX |  |
| $V_{OH}$ | $I_{OH}$ = –100 µA | 1.65 V to 3.6 V | $V_{CC}$ – 0.2 |  |  | $V_{CC}$ – 0.2 |  | $V_{CC}$ – 0.2 |  | V |
|  | $I_{OH}$ = –4 mA | 1.65 V | 1.2 |  |  | 1.2 |  | 1.2 |  |  |
|  | $I_{OH}$ = –8 mA | 2.3 V | 1.7 |  |  | 1.7 |  | 1.7 |  |  |
|  | $I_{OH}$ = –12 mA | 2.7 V | 2.2 |  |  | 2.2 |  | 2.2 |  |  |
|  |  | 3 V | 2.4 |  |  | 2.4 |  | 2.4 |  |  |
|  | $I_{OH}$ = –24 mA | 3 V | 2.2 |  |  | 2.2 |  | 2.2 |  |  |
| $V_{OL}$ | $I_{OL}$ = 100 µA | 1.65 V to 3.6 V |  |  | 0.2 |  | 0.2 |  | 0.2 | V |
|  | $I_{OL}$ = 4 mA | 1.65 V |  |  | 0.45 |  | 0.45 |  | 0.45 |  |
|  | $I_{OL}$ = 8 mA | 2.3 V |  |  | 0.7 |  | 0.7 |  | 0.7 |  |
|  | $I_{OL}$ = 12 mA | 2.7 V |  |  | 0.4 |  | 0.4 |  | 0.4 |  |
|  | $I_{OL}$ = 24 mA | 3 V |  |  | 0.55 |  | 0.55 |  | 0.55 |  |
| $I_I$ | $V_I$ = 5.5 V or GND | 3.6 V |  |  | ±5 |  | ±5 |  | ±5 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 3.6 V |  |  | 10 |  | 10 |  | 10 | µA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | 2.7 V to 3.6 V |  |  | 500 |  | 500 |  | 500 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V |  | 4.5 |  |  |  |  |  | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## 5.6 Timing Requirements, –40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

|  |  |  | $V_{CC}$ = 1.8 V ± 0.15 V |  | $V_{CC}$ = 2.5 V ± 0.2 V |  | $V_{CC}$ = 2.7 V |  | $V_{CC}$ = 3.3 V ± 0.3 V |  | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |  |
| $f_{clock}$ | Clock frequency |  |  | 120 |  | 150 |  | 150 |  | 150 | MHz |
| $t_w$ | Pulse duration, CLK high or low |  | 4.2 |  | 3.3 |  | 3.3 |  | 3.3 |  | ns |
| $t_{su}$ | Setup time | Data before CLK↓ | 5.8 |  | 3.2 |  | 3.1 |  | 2.3 |  | ns |
|  |  | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive | 5 |  | 2.8 |  | 2.4 |  | 1.1 |  |  |
| $t_h$ | Hold time, data after CLK↓ |  | 6.2 |  | 4.4 |  | 2.5 |  | 0.7 |  | ns |

## 5.7 Timing Requirements, –40°C to +125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

|  |  |  | $V_{CC}$ = 1.8 V ± 0.15 V |  | $V_{CC}$ = 2.5 V ± 0.2 V |  | $V_{CC}$ = 2.7 V |  | $V_{CC}$ = 3.3 V ± 0.3 V |  | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |  |
| $f_{clock}$ | Clock frequency |  |  | 120 |  | 150 |  | 150 |  | 150 | MHz |
| $t_w$ | Pulse duration, CLK high or low |  | 4.1 |  | 3.3 |  | 3.3 |  | 3.3 |  | ns |
| $t_{su}$ | Setup time | Data before CLK↓ | 6 |  | 3.2 |  | 3.1 |  | 2.3 |  | ns |
|  |  | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive | 5 |  | 2.8 |  | 2.4 |  | 1.1 |  |  |
| $t_h$ | Hold time, data after CLK↓ |  | 6.2 |  | 4.7 |  | 2.5 |  | 0.7 |  | ns |

## 5.8 Switching Characteristics, –40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | TYP | MAX | |
| $f_{max}$ | | | 150 | | 150 | | 150 | | 150 | | | MHz |
| $t_{pd}$ | $\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ | Q or $\overline{\text{Q}}$ | | 5.9 | | 4.1 | | 5.5 | 1 | 3.4 | 4.8 | ns |
| | CLK | | | 5.6 | | 4 | | 7.1 | 1 | 3.5 | 5.9 | |

## 5.9 Switching Characteristics, –40°C to +125°C

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | TYP | MAX | |
| $f_{max}$ | | | 120 | | 150 | | 150 | | 150 | | | MHz |
| $t_{pd}$ | $\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ | Q or $\overline{\text{Q}}$ | | 6.2 | | 4 | | 6 | 1 | 3.4 | 5.3 | ns |
| | CLK | | | 6.2 | | 4.1 | | 7.6 | 1 | 3.5 | 6.4 | |

## 5.10 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | See[1] | See[1] | 24 | pF |

(1) This information was not available at the time of publication.

## 5.11 Typical Characteristics

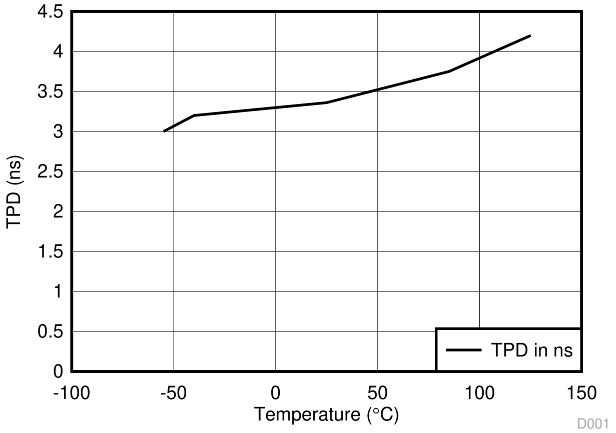


Figure 5-1. TPD vs Temperature

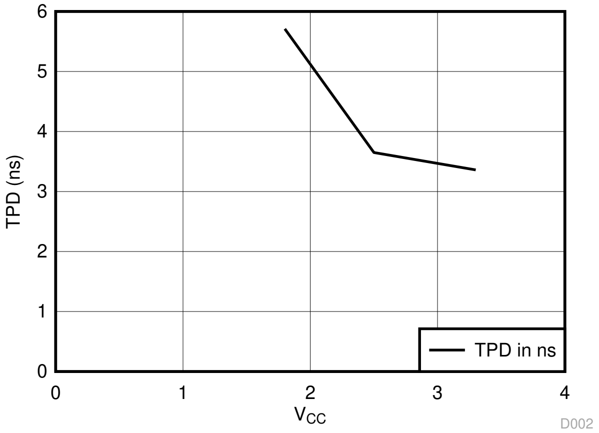
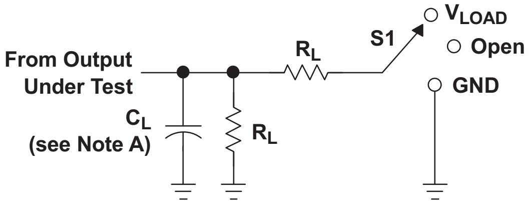


Figure 5-2. TPD vs $V_{CC}$ at 25°C

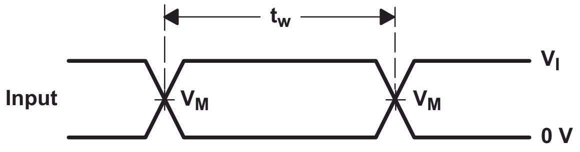
# 6 Parameter Measurement Information



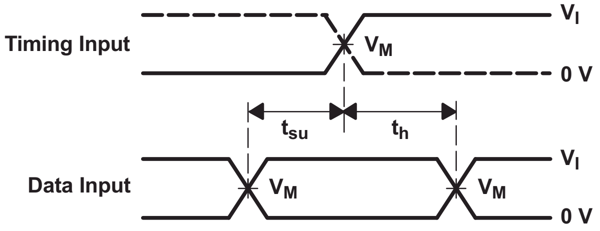
LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

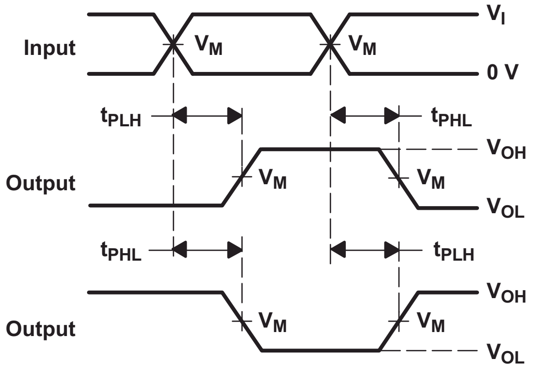
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_{\Delta}$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V ± 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



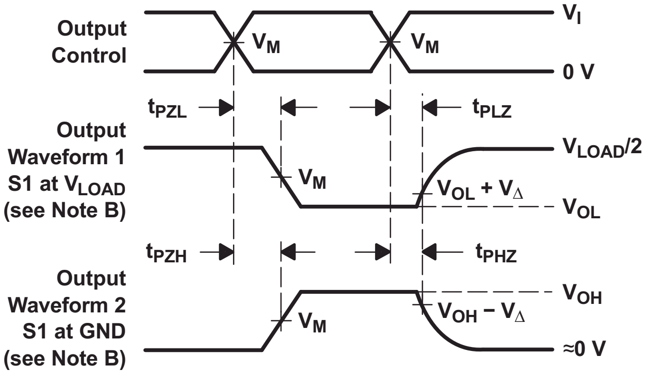
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. $C_L$ includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, $Z_O$ = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
- F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
- G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
- H. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit and Voltage Waveforms**

# 7 Detailed Description

## 7.1 Overview

This dual negative-edge-triggered J-K flip-flop is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

A low level at the preset ( $\overline{\text{PRE}}$) or clear ( $\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the J and K inputs meeting the setup-time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs can be changed without affecting the levels at the outputs. The SN74LVC112A can perform as a toggle flip-flop by tying J and K high.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

## 7.2 Functional Block Diagram

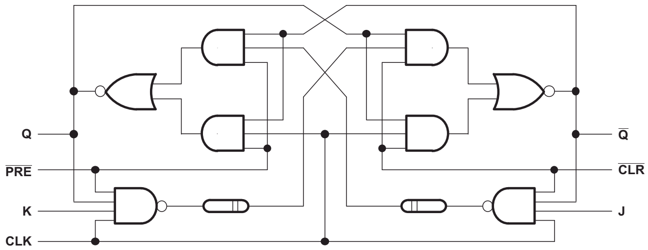


**Figure 7-1. Logic Diagram, Each Flip-Flop (Positive Logic)**

## 7.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
  - Inputs accept voltages to 5.5 V
- $I_{off}$ feature
  - Allows voltages on the inputs and outputs when $V_{CC}$ is 0 V

## 7.4 Device Functional Modes

**Table 7-1. Function Table**

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| $\overline{\text{PRE}}$ | $\overline{\text{CLR}}$ | CLK | J | K | Q | $\overline{\text{Q}}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H(1) | H(1) |
| H | H | ↓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | X | X | $Q_0$ | $\overline{Q}_0$ |

(1) The output levels in this configuration may not meet the minimum levels for $V_{OH}$. Furthermore, this configuration is nonstable; that is, it does not persist when either $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

SN74LVC112A is a high-drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be retained or latched. It can produce 24 mA of drive current at 3.3 V, making it Ideal for driving multiple outputs and good for high-speed applications up to 150 MHz. The inputs are 5.5-V tolerant allowing it to translate down to $V_{CC}$.

## 8.2 Typical Application

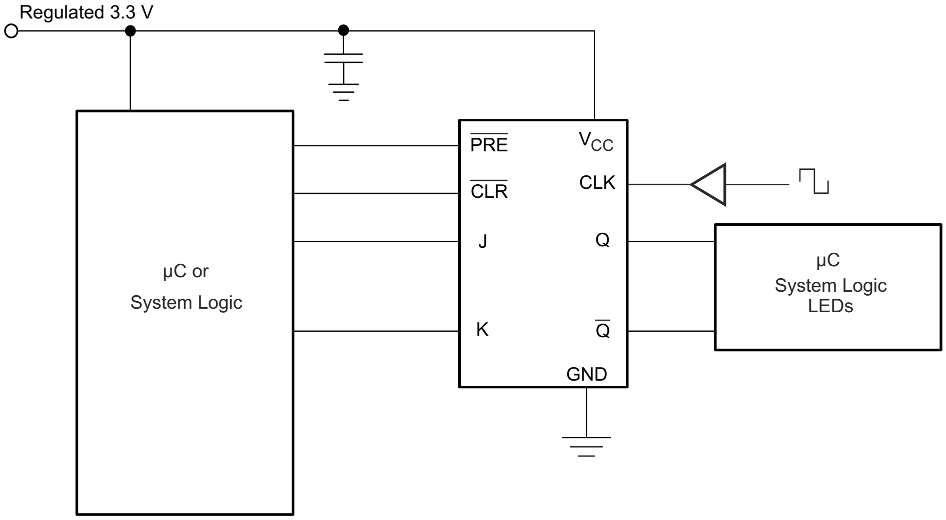


**Figure 8-1. Typical Application Schematic**

### *8.2.1 Design Requirements*

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that may exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### *8.2.2 Detailed Design Procedure*

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *Recommended Operating Conditions* table.
   - For specified High and low levels, see $V_{IH}$ and $V_{IL}$ in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$.
2. Recommend Output Conditions
   - Load currents should not exceed 50 mA per output and 100 mA total for the part.
   - Outputs should not be pulled above $V_{CC}$.

### 8.2.3 Application Curve

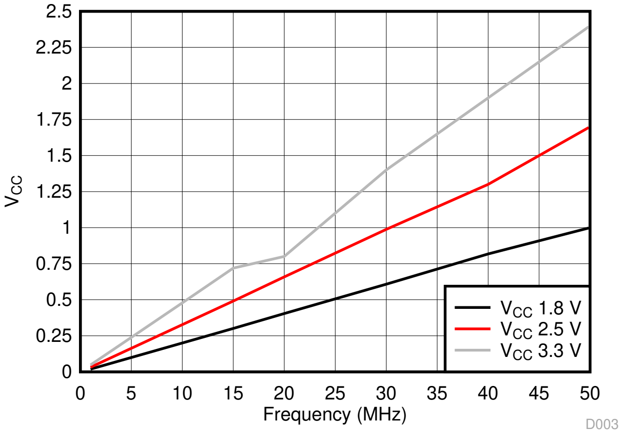


Figure 8-2. $I_{CC}$ vs Frequency

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple $V_{CC}$ pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

Inputs should not float when using multiple bit logic devices. Functions or parts of functions of digital logic devices are unused in many cases. Some examples include situations in which only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver.

### 8.4.2 Layout Example

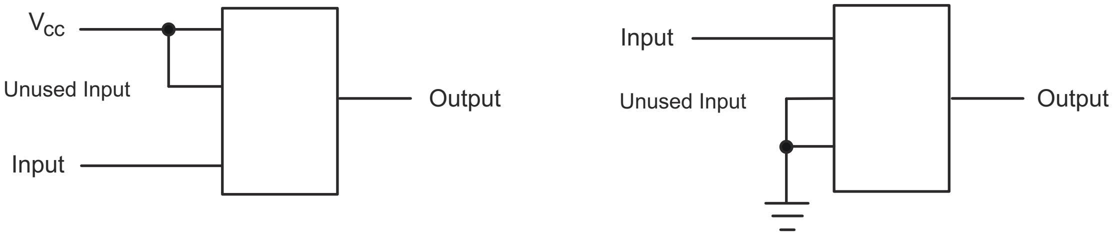


Figure 8-3. Layout Diagram

# 9 Device and Documentation Support

## 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision M (December 2014) to Revision N (December 2024)** **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Deleted references to machine model throughout the data sheet, and updated HBM and CDM values from 3000V to 2000V and 1500V to 1000V, respectively.......................................................................... 1
- Updated RθJA values: D = 90.6 to 118.1, DB = 107.1 to 122.5, NS = 90.7 to 117.5, PW = 122.6 to 141.8; updated D, DB, NS, and PW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W...5

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**Changes from Revision L (August 2004) to Revision M (December 2014)** **Page**

- Added *Applications*, *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section................... 1
- Deleted *Ordering Information* table.......................................................................................... 1
- Changed MAX operating temperature to 125°C in *Recommended Operating Conditions* table........................5
- Added –40°C to +125°C temperature range to *Electrical Specifications* table. ................................................6
- Added *Timing Requirements* table for –40°C to 125°C temperature range...................................................... 6
- Added *Switching Characteristics* table for –40°C to 125°C temperature range. .............................................. 7

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC112AD | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC112A | Samples |
| SN74LVC112ADBR | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC112A | Samples |
| SN74LVC112ADGVR | ACTIVE | TVSOP | DGV | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC112A | Samples |
| SN74LVC112ADR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC112A | Samples |
| SN74LVC112ADT | ACTIVE | SOIC | D | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC112A | Samples |
| SN74LVC112ANSR | ACTIVE | SOP | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC112A | Samples |
| SN74LVC112APW | ACTIVE | TSSOP | PW | 16 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC112A | Samples |
| SN74LVC112APWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC112A | Samples |
| SN74LVC112APWT | ACTIVE | TSSOP | PW | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC112A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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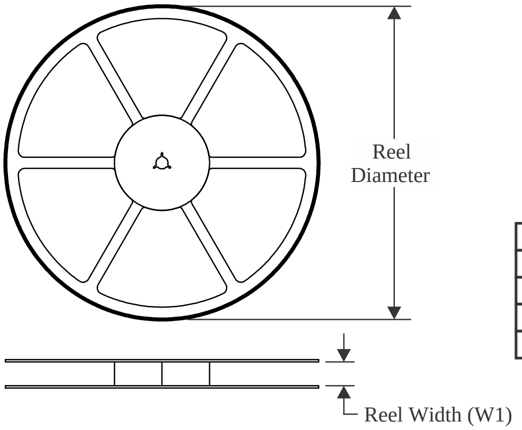
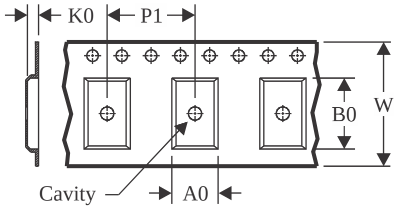
## TAPE AND REEL INFORMATION

REEL DIMENSIONS

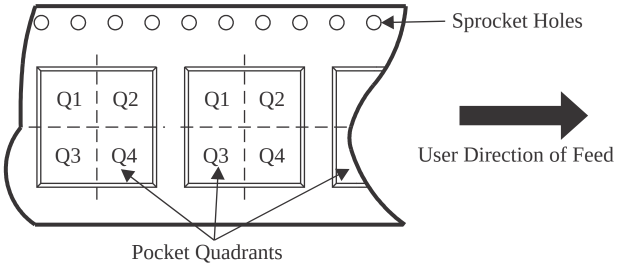


TAPE DIMENSIONS



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

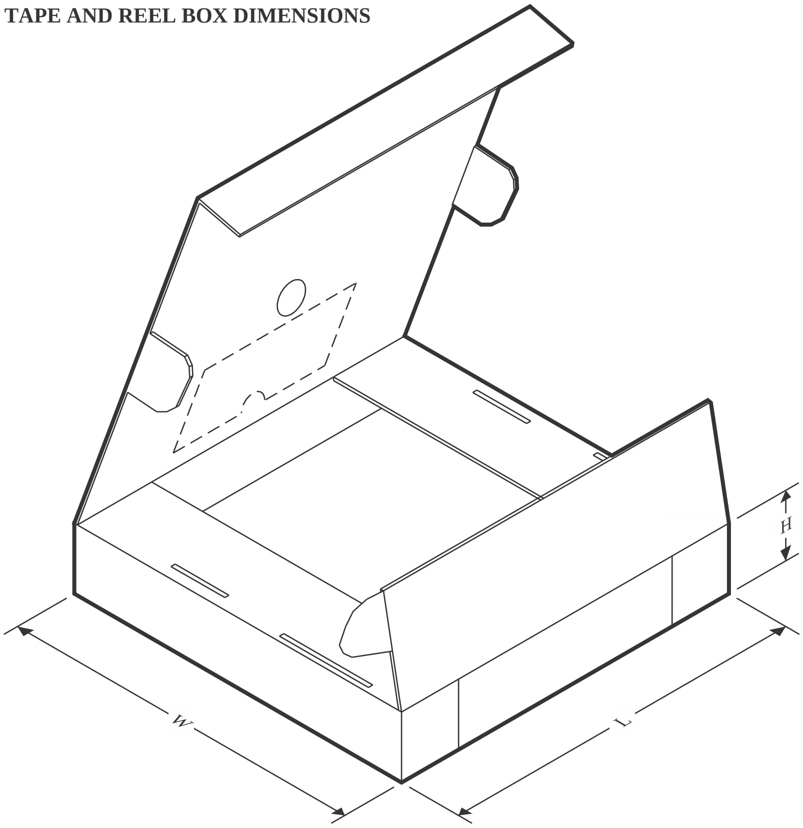
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC112ADBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LVC112ADGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC112ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC112ANSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC112APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC112APWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

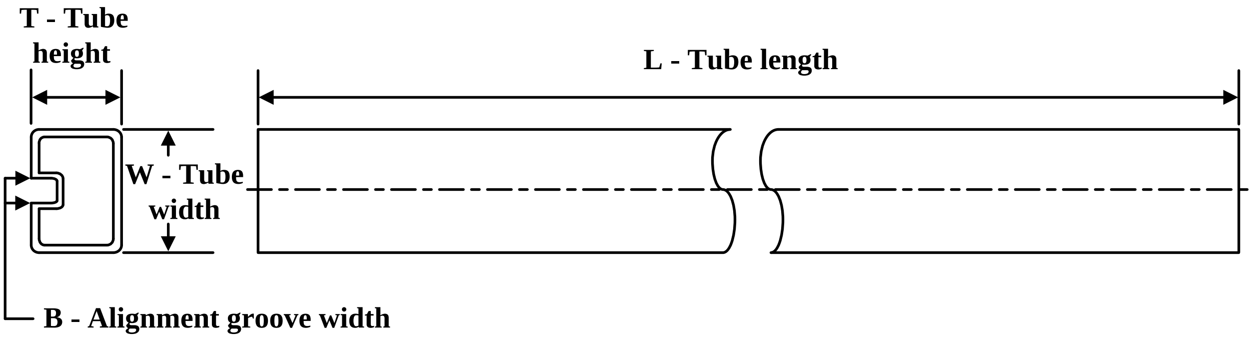
## TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

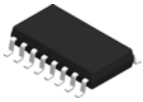
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC112ADBR | SSOP | DB | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC112ADGVR | TVSOP | DGV | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC112ADR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LVC112ANSR | SOP | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC112APWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC112APWT | TSSOP | PW | 16 | 250 | 356.0 | 356.0 | 35.0 |

## TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74LVC112AD | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74LVC112APW | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |

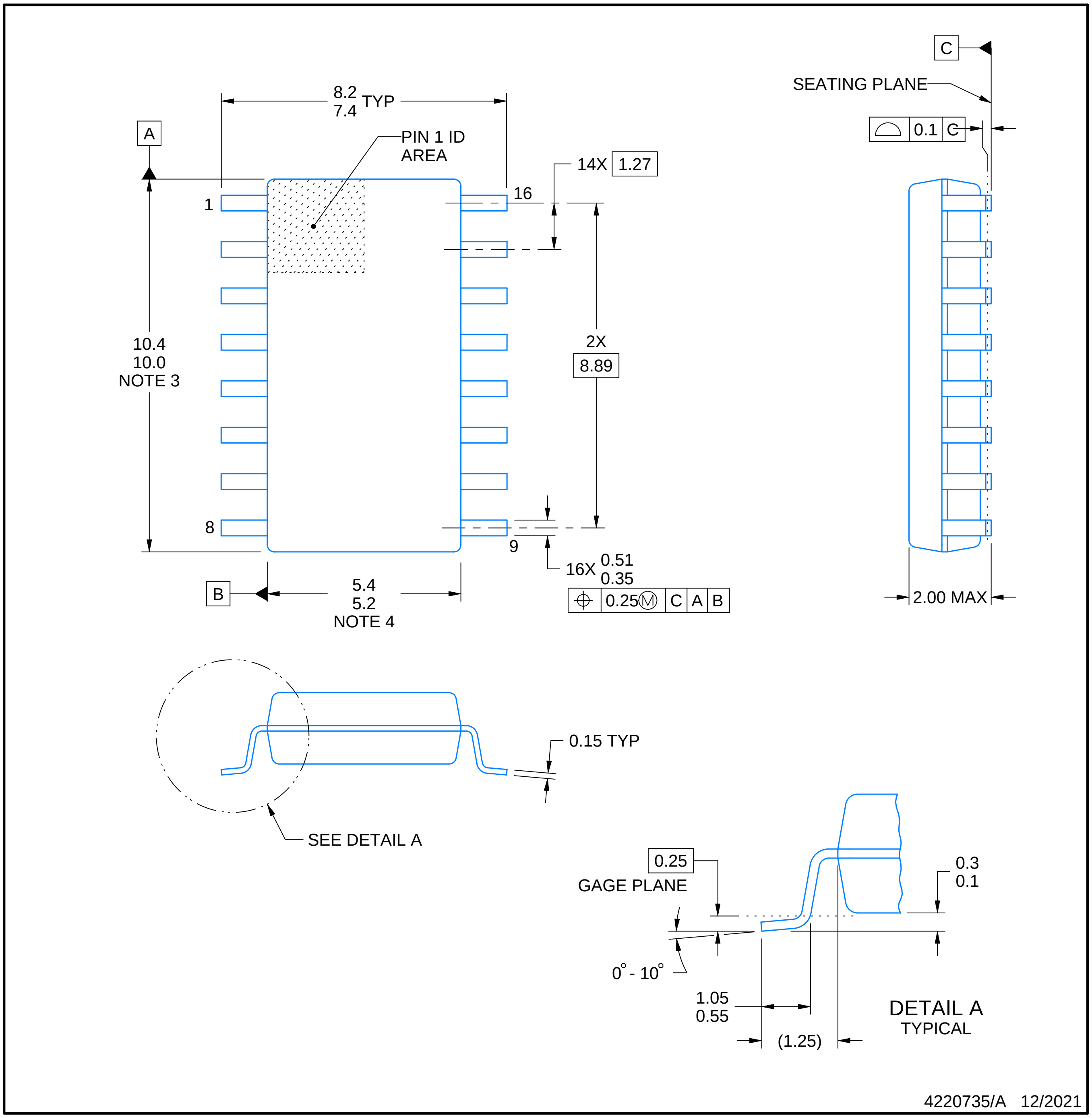


# PACKAGE OUTLINE

**NS0016A**

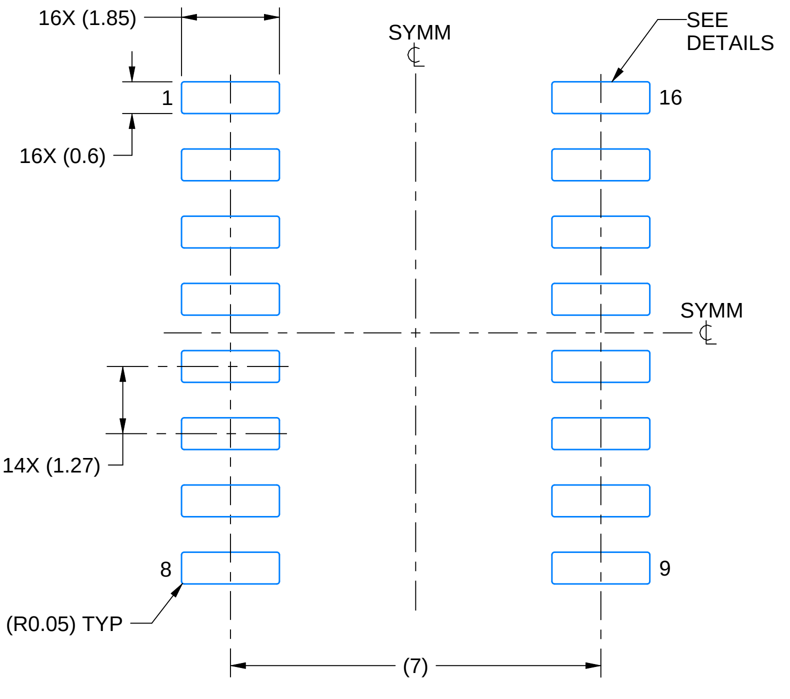
## SOP - 2.00 mm max height

SOP

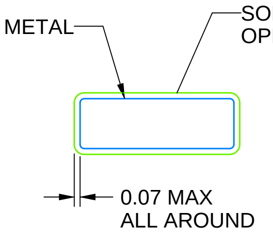


NOTES:

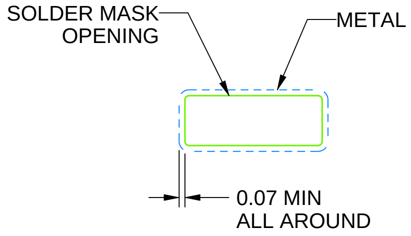
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

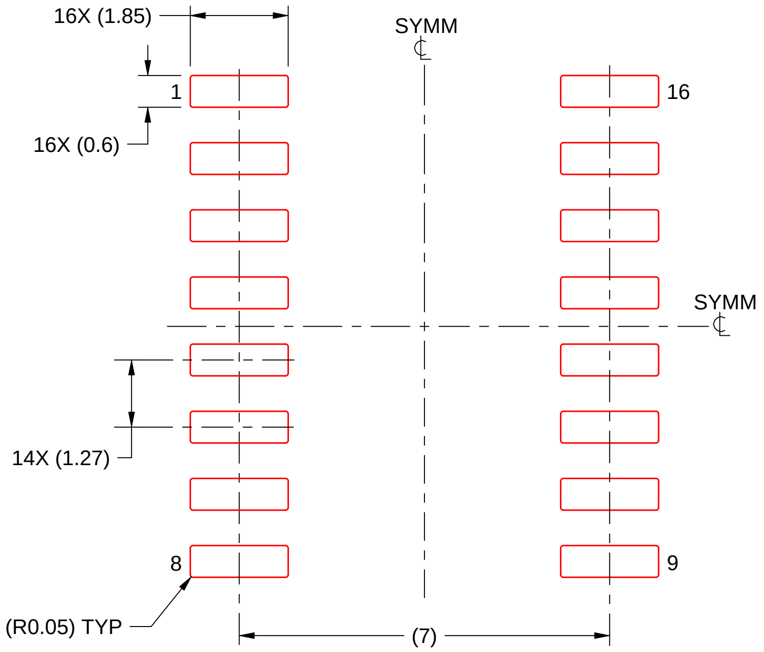
4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## SOP - 2.00 mm max height

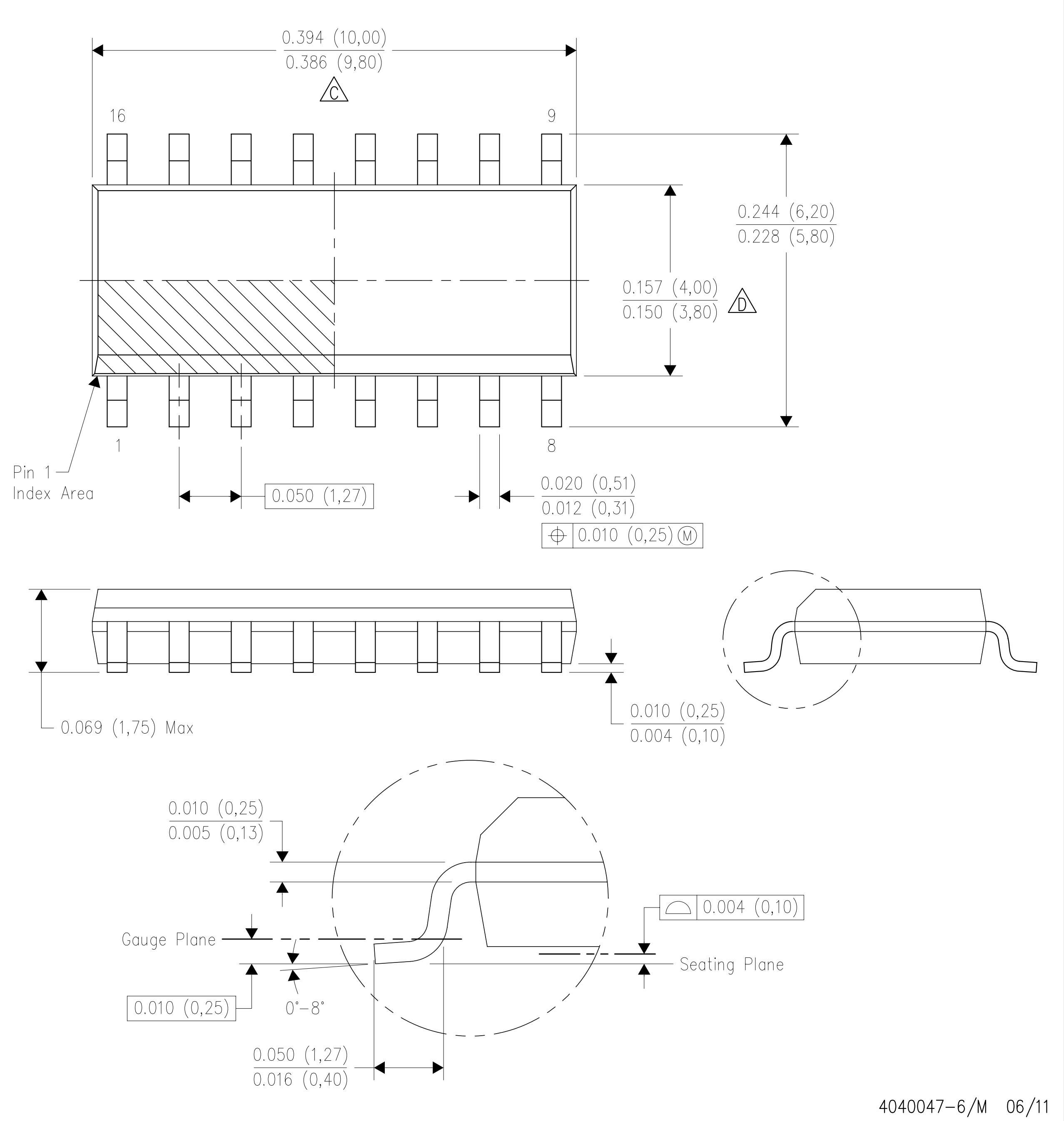


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

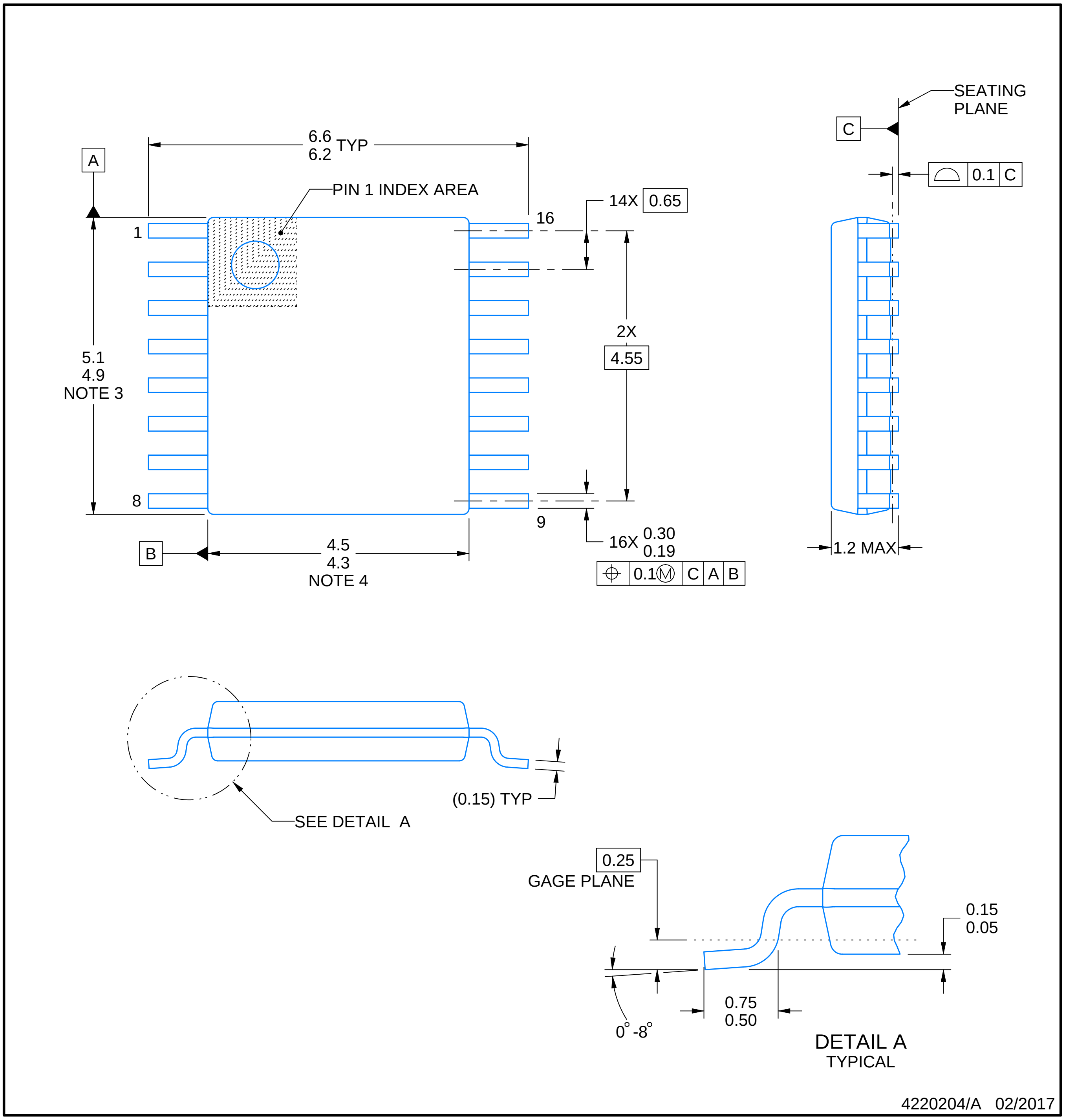
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

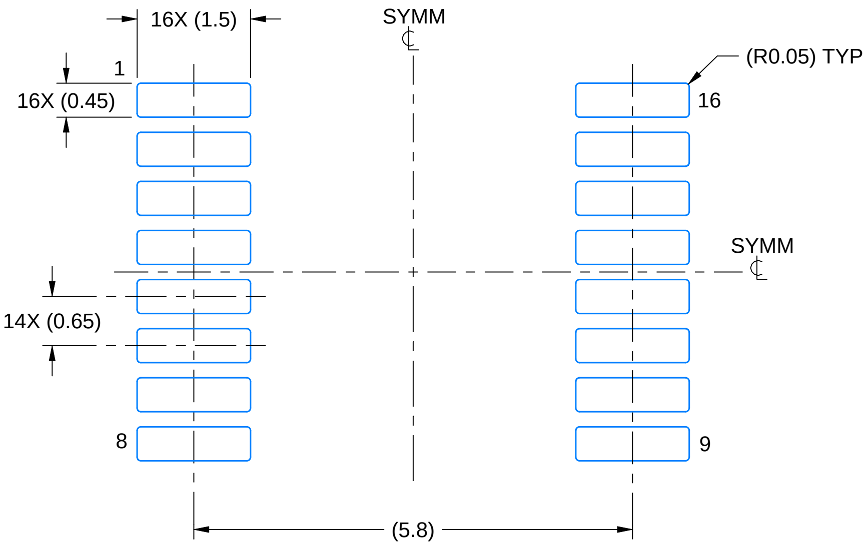


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

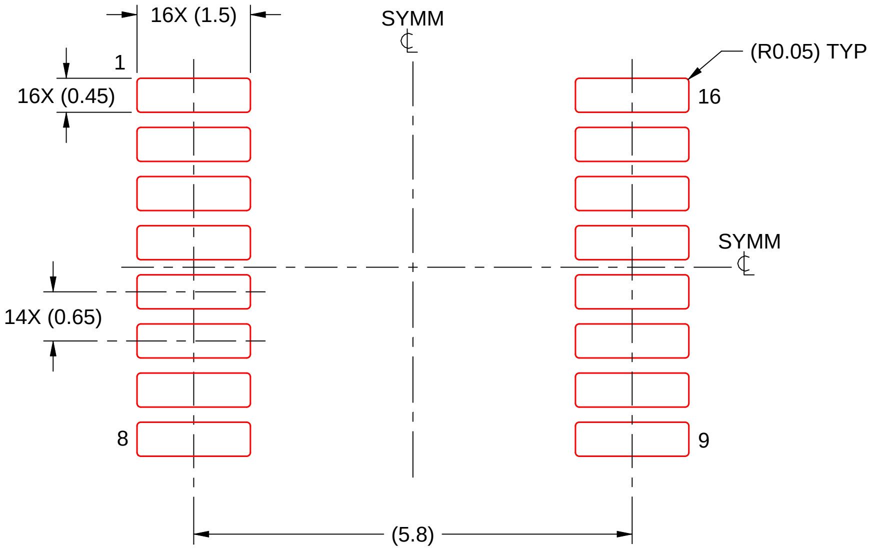
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

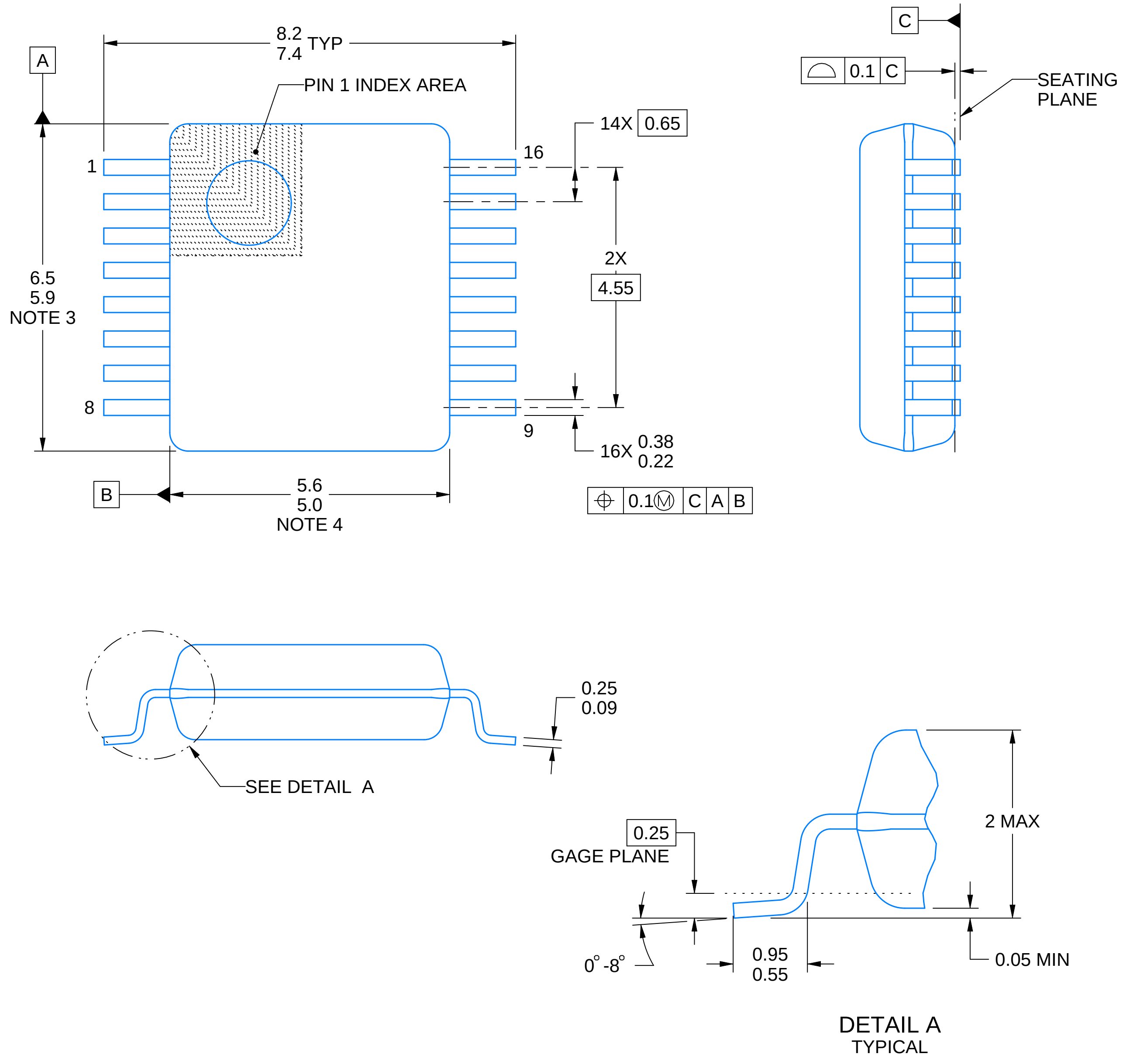


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

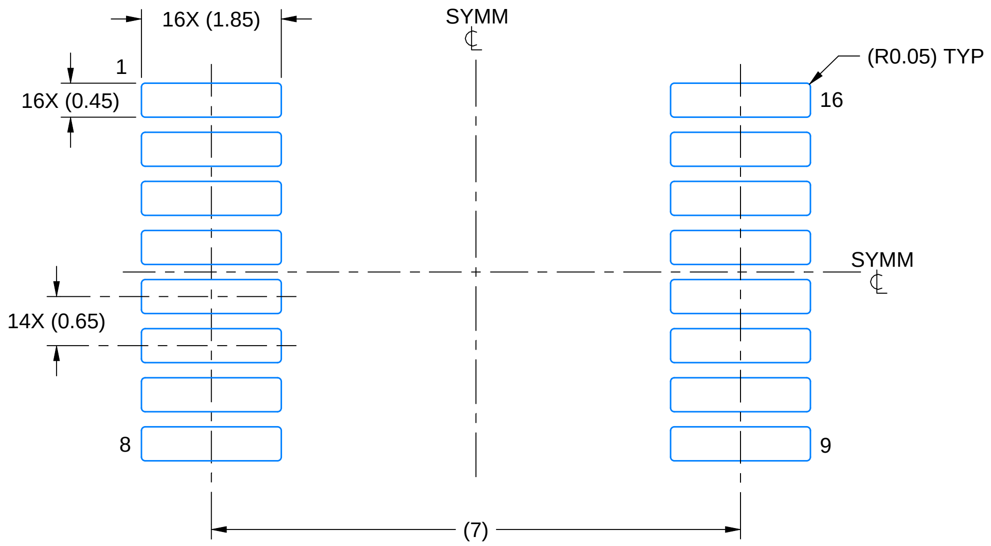
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



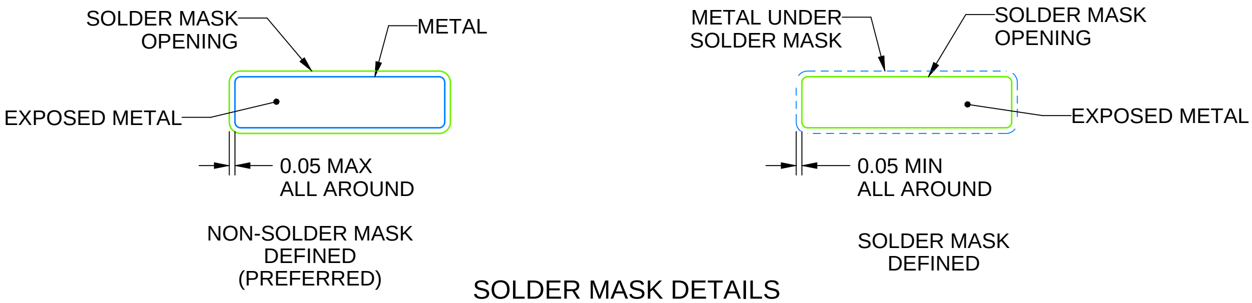
4220763/A 05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

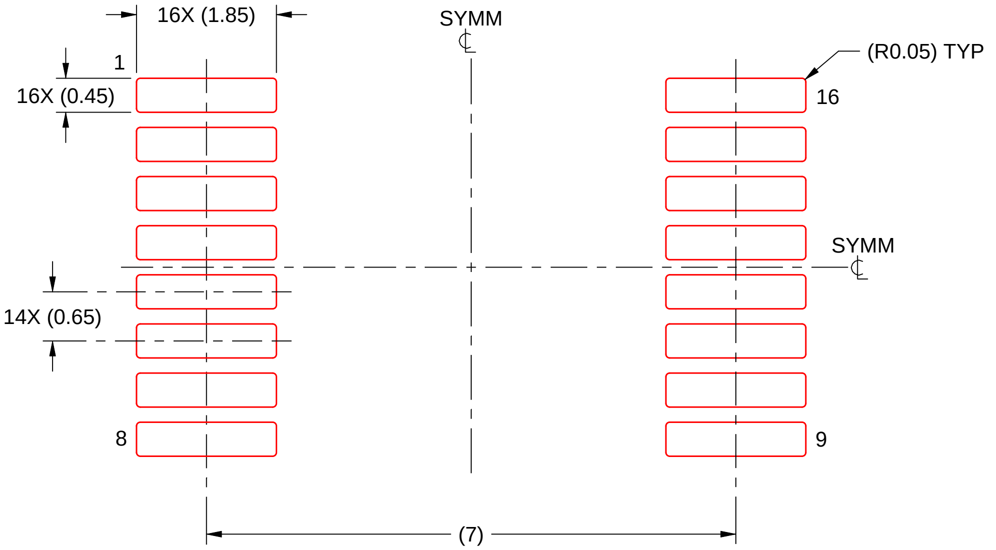


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

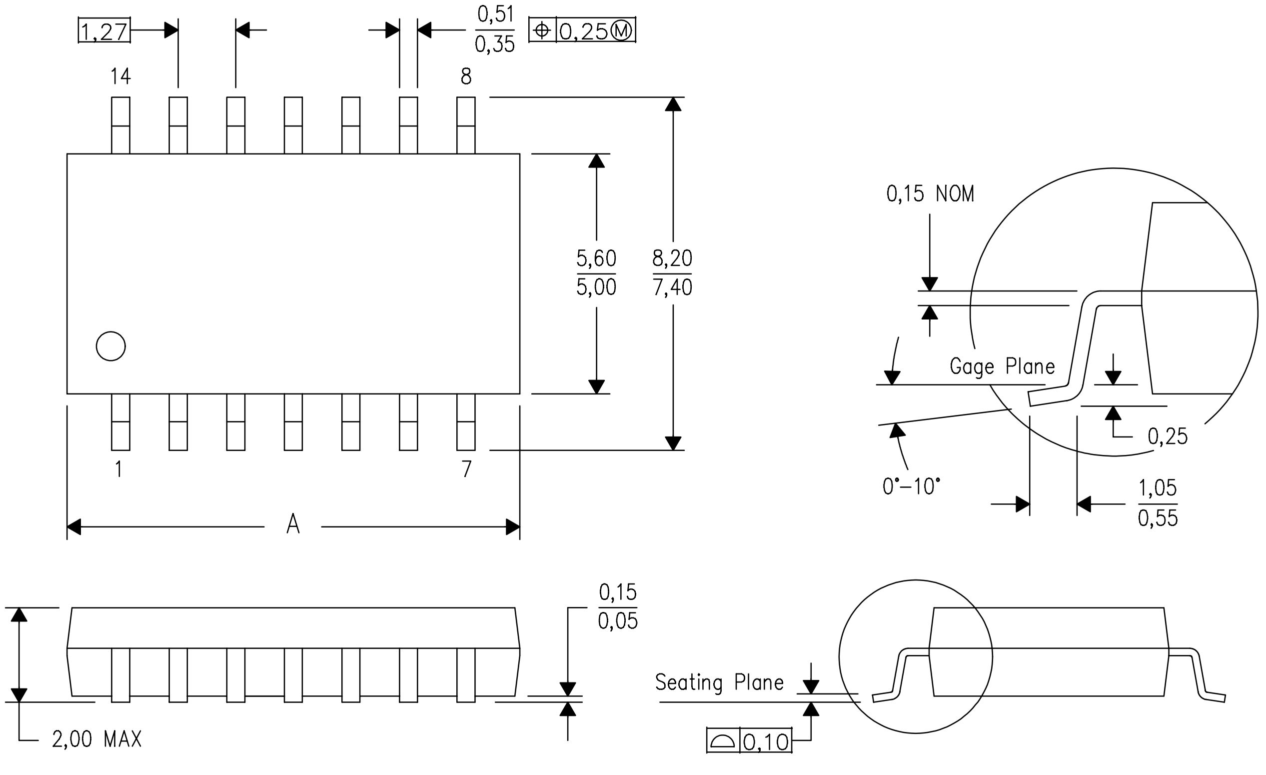
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



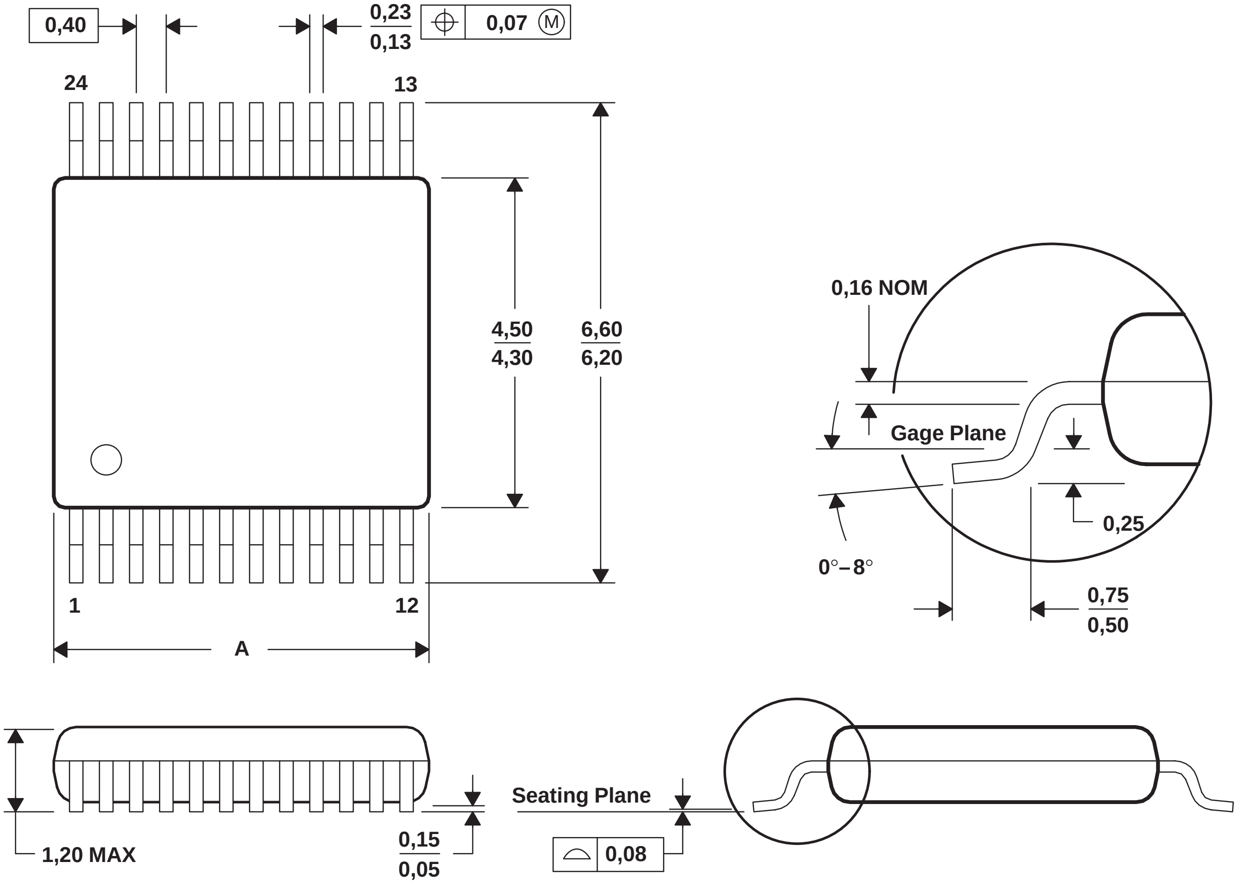
| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

**24 PINS SHOWN**



| PINS **<br>DIM | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| **A MAX** | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| **A MIN** | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

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