

## SN74LVC2G241 Dual Buffer and Driver With 3-State Outputs

### 1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.1 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Maximum  $I_{CC}$
- $\pm$ 24-mA Output Drive at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Can Be Used as a Down Translator to Translate Inputs From a Max of 5.5 V Down to the  $V_{CC}$  Level
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- AV Receivers
- Blu-ray Players and Home Theaters
- DVD Recorders and Players
- Desktop or Notebook PCs
- Digital Radio or Internet Radio Players
- Digital Video Cameras (DVC)
- Embedded PCs
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Projector Front-Ends
- Portable Media Players
- Pro Audio Mixers

### 3 Description

This dual buffer and line driver is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC2G241 device is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

The SN74LVC2G241 device is organized as two 1-bit line drivers with separate output-enable ( $1\overline{OE}$ ,  $2OE$ ) inputs. When  $1\overline{OE}$  is low and  $2OE$  is high, the device passes data from the A inputs to the Y outputs. When  $1\overline{OE}$  is high and  $2OE$  is low, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor, and  $OE$  should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking or the current-sourcing capability of the driver.

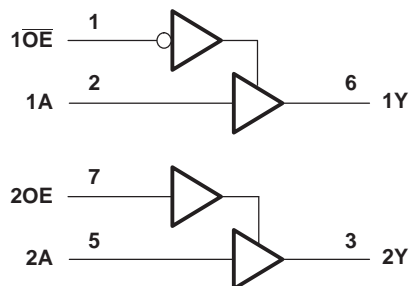
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC2G241DCT	SM8 (8)	2.95 mm x 2.80 mm
SN74LVC2G241DCU	VSOOP (8)	2.30 mm x 2.00 mm
SN74LVC2G241YZP	DSBGA (8)	1.91 mm x 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (December 2015) to Revision P	Page
• Changed Electrical Characteristics table format .....	5
• Changed Switching Characteristics tables format. ....	6

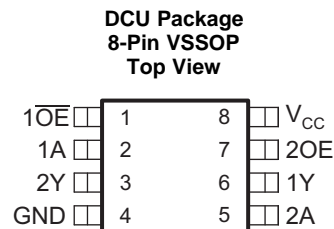
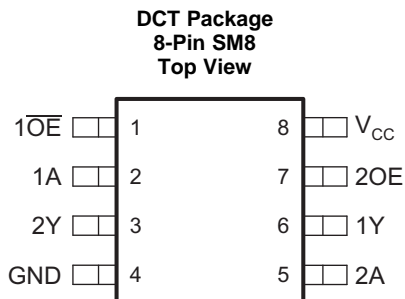
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Changes from Revision N (November 2013) to Revision O	Page
• Added <i>Applications</i> section, <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....	1

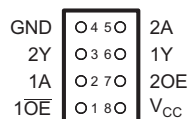
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Changes from Revision M (February 2007) to Revision N	Page
• Updated document to new TI data sheet format. ....	1
• Removed Ordering Information table. ....	1
• Updated Features. ....	1
• Updated operating temperature range. ....	4

## 5 Pin Configuration and Functions



**YZP Package**  
**8-Pin DSBGA**  
**Bottom View**



### Pin Functions<sup>(1)(2)</sup>

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	2	I	Input
$\overline{1OE}$	1	I	Output enable (Active low)
1Y	6	O	Output
2A	5	I	Input
2Y	3	O	Output
2OE	7	I	Output enable (Active high)
GND	4	—	Ground
V <sub>CC</sub>	8	—	Power pin

(1) N.C. – No internal connection

(2) See for dimensions

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	6.5	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA
T <sub>J</sub>	Maximum junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5
		Data retention only	1.5	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
		V <sub>CC</sub> = 3 V to 3.6 V	2	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
		V <sub>CC</sub> = 3 V to 3.6 V	0.8	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.3 × V <sub>CC</sub>	
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>
		3-state	0	5.5
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	-4	mA
		V <sub>CC</sub> = 2.3 V	-8	
		V <sub>CC</sub> = 3 V	-16	
		V <sub>CC</sub> = 4.5 V	-24	

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

**Recommended Operating Conditions<sup>(1)</sup> (continued)**

		MIN	MAX	UNIT
$I_{OL}$ Low-level output current	$V_{CC} = 1.65\text{ V}$		4	mA
	$V_{CC} = 2.3\text{ V}$		8	
	$V_{CC} = 3\text{ V}$		16	
			24	
	$V_{CC} = 4.5\text{ V}$		32	
$\Delta t/\Delta v$ Input transition rise or fall rate	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$		20	ns/V
	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		10	
	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		5	
$T_A$ Operating free-air temperature		-40	85	°C

**6.4 Thermal Information**

THERMAL METRIC <sup>(1)</sup>	SN74LVC2G241			UNIT
	DCT (SM8)	DCU (VSSOP)	YZP (DSBGA)	
	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	220	227	102	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

**6.5 Electrical Characteristics**

over recommended operating free-air temperature range,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	-40°C to 85°C			-40°C to 125°C (Recommended)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OH}$	$I_{OH} = -100\ \mu\text{A}$	1.65 V to 5.5 V	$V_{CC} - 0.1$			$V_{CC} - 0.1$			V
	$I_{OH} = -4\text{ mA}$	1.65 V	1.2			1.2			
	$I_{OH} = -8\text{ mA}$	2.3 V	1.9			1.9			
	$I_{OH} = -16\text{ mA}$	3 V	2.4			2.4			
	$I_{OH} = -24\text{ mA}$		2.3			2.3			
	$I_{OH} = -32\text{ mA}$	4.5 V	3.8			3.8			
$V_{OL}$	$I_{OL} = 100\ \mu\text{A}$	1.65 V to 5.5 V	0.1			0.1			V
	$I_{OL} = 4\text{ mA}$	1.65 V	0.45			0.45			
	$I_{OL} = 8\text{ mA}$	2.3 V	0.3			0.3			
	$I_{OL} = 16\text{ mA}$	3 V	0.4			0.4			
	$I_{OL} = 24\text{ mA}$		0.55			0.55			
	$I_{OL} = 32\text{ mA}$	4.5 V	0.55			0.75			
$I_i$	A or $\overline{\text{OE}}$ inputs	$V_i = 5.5\text{ V}$ or GND	0 to 5.5 V			$\pm 5$			$\mu\text{A}$
$I_{off}$	$V_i$ or $V_o = 5.5\text{ V}$	0	$\pm 10$			$\pm 10$			$\mu\text{A}$
$I_{OZ}$	$V_o = 0$ to 5.5 V	3.6 V	10			10			$\mu\text{A}$
$I_{CC}$	$V_i = 5.5\text{ V}$ or GND, $I_o = 0$	1.65 V to 5.5 V	10			10			$\mu\text{A}$
$\Delta I_{CC}$	One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND	3 V to 5.5 V	500			500			$\mu\text{A}$
$C_i$	Data Inputs	$V_i = V_{CC}$ or GND	3.5						pF
	Control Inputs		4						
$C_o$	$V_o = V_{CC}$ or GND	3.3 V	6.5						pF

## 6.6 Switching Characteristics

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	3.3	9.1	1.5	5.5	1.4	4.3	1.0	4.0	ns
$t_{en}$	$\overline{OE}$	Y	4.0	9.9	1.3	6.6	1.2	4.7	1.1	5.0	ns
$t_{dis}$	$\overline{OE}$	Y	1.5	11.6	1.0	5.7	1.4	4.6	0.5	4.2	ns

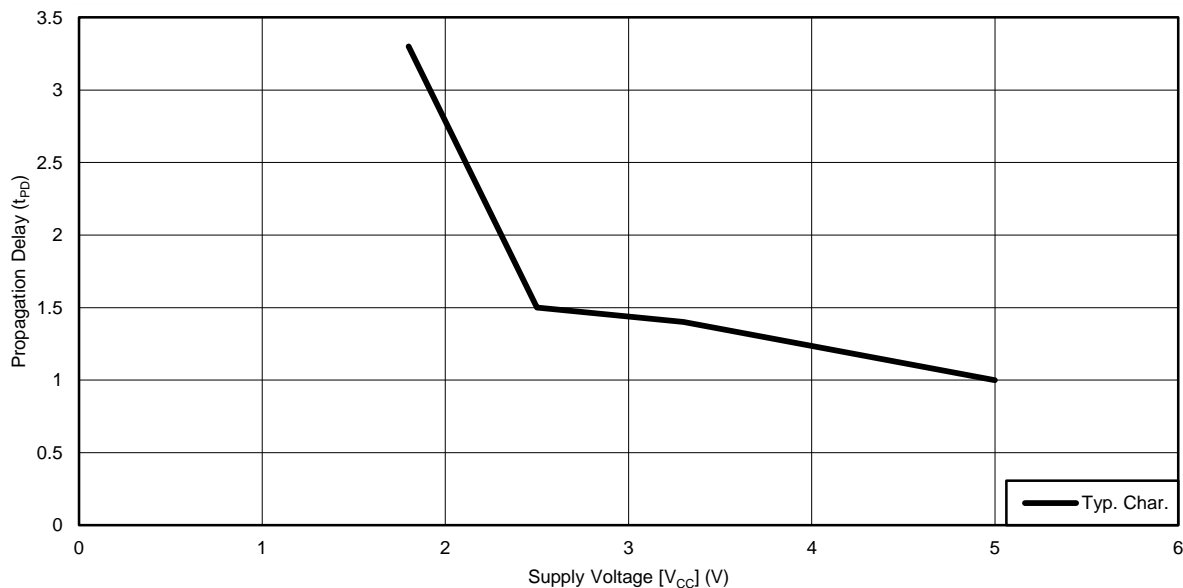
PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 125°C (Recommended)								UNIT
			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	3.3	10.1	1.5	5.6	1.4	5.3	1.0	4.2	ns
$t_{en}$	$\overline{OE}$	Y	4.0	10.9	1.3	6.6	1.2	5.7	1.2	4.3	ns
$t_{dis}$	$\overline{OE}$	Y	1.5	12.6	1.0	6.6	1.4	5.6	1.0	3.9	ns

## 6.7 Operating Characteristics

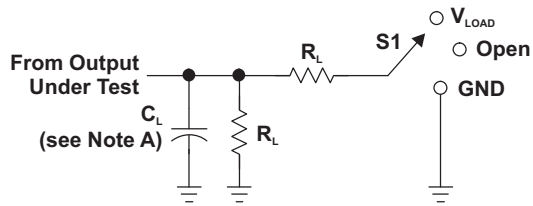
 $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT	
$C_{pd}$	Power dissipation capacitance per buffer/driver	Outputs enabled	$f = 10\text{ MHz}$	$V_{CC} = 1.8\text{ V}$	19	pF
				$V_{CC} = 2.5\text{ V}$	19	
				$V_{CC} = 3.3\text{ V}$	20	
				$V_{CC} = 5\text{ V}$	22	
	Outputs disabled	$V_{CC} = 1.8\text{ V}$	2	pF		
		$V_{CC} = 2.5\text{ V}$	2			
		$V_{CC} = 3.3\text{ V}$	2			
		$V_{CC} = 5\text{ V}$	3			

## 6.8 Typical Characteristic


**Figure 1.  $t_{pd}$  vs  $V_{CC}$  Over Full Temperature Range**

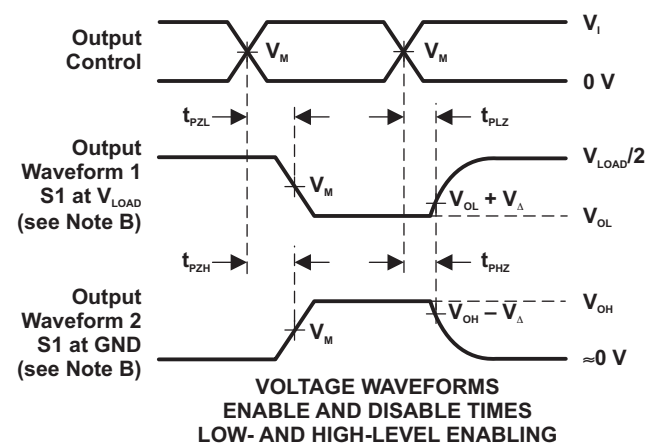
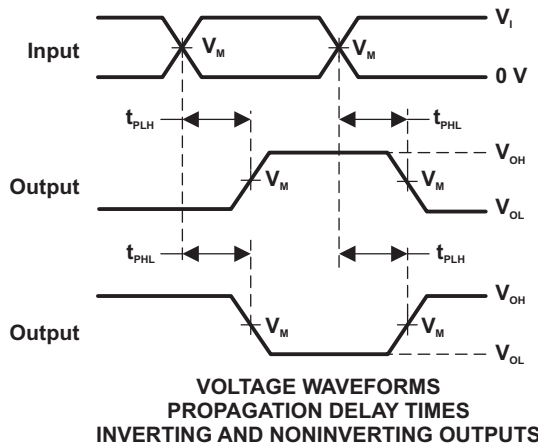
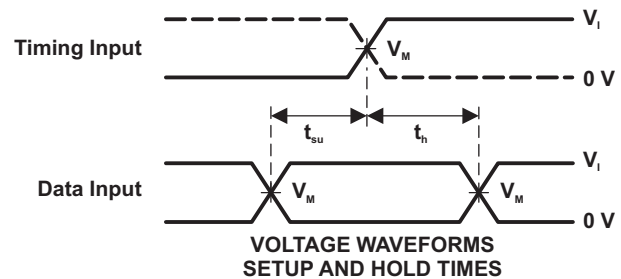
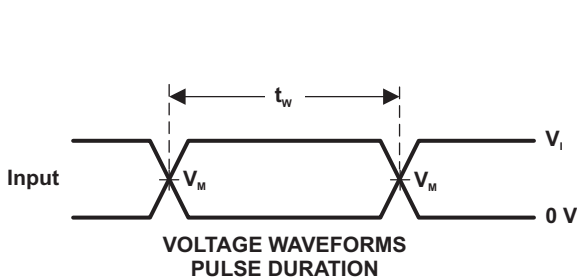
## 7 Parameter Measurement Information



LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_i$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

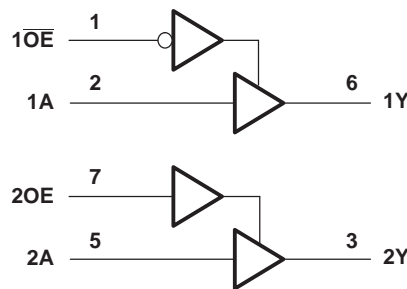
## 8 Detailed Description

### 8.1 Overview

The SN74LVC2G241 device is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters. The SN74LVC2G241 device is organized as two 1-bit line drivers with separate output-enable ( $\overline{1OE}$ , 2OE) inputs. When  $\overline{1OE}$  is low and 2OE is high, the device passes data from the A inputs to the Y outputs. When  $\overline{1OE}$  is high and 2OE is low, the outputs are in the high-impedance state.

The SN74LVC2G241 is also an effective redriver, with a maximum output current drive of 32 mA.

### 8.2 Functional Block Diagram



**Figure 3. Logic Diagram (Positive Logic)**

### 8.3 Feature Description

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor, and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking or the current-sourcing capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 8.4 Device Functional Modes

Table 1 and Table 2 list the functional modes of the SN74LVC2G241.

**Table 1. Gate 1 Functional Table**

INPUTS		OUTPUT 1Y
$\overline{1OE}$	1A	
L	H	H
L	L	L
H	X	Z

**Table 2. Gate 2 Functional Table**

INPUTS		OUTPUT 2Y
2OE	2A	
H	H	H
H	L	L
L	X	Z



## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

*Typical Application* shows a simple application where a physical push button is connected to the SN74LVC2G241. The push button is in a physical location far enough away from the processor that the input signal is weak and needs to be redriven. The SN74LVC2G241 acts as a redriver, providing a strong input signal to the processor with as little as 1 ns of propagation delay.

### 9.2 Typical Application

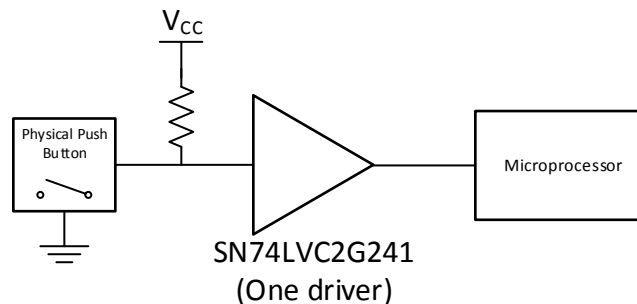


Figure 4. SN74LVC2G241 Application

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - Rise time and fall time specs. See  $(\Delta t/\Delta V)$  in *Recommended Operating Conditions*.
  - Specified high and low levels. See  $(V_{IH}$  and  $V_{IL})$  in *Recommended Operating Conditions*.
  - Inputs are overvoltage tolerant allowing them to go as high as  $(V_I \text{ max})$  in *Recommended Operating Conditions* at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents must not exceed  $(I_O \text{ max})$  per output and must not exceed (Continuous current through  $V_{CC}$  or GND) total current for the part. These limits are located in *Absolute Maximum Ratings*.
  - Outputs must not be pulled above  $V_{CC}$  during normal operation or 5.5 V in high-z state.

## Typical Application (continued)

### 9.2.3 Application Curve

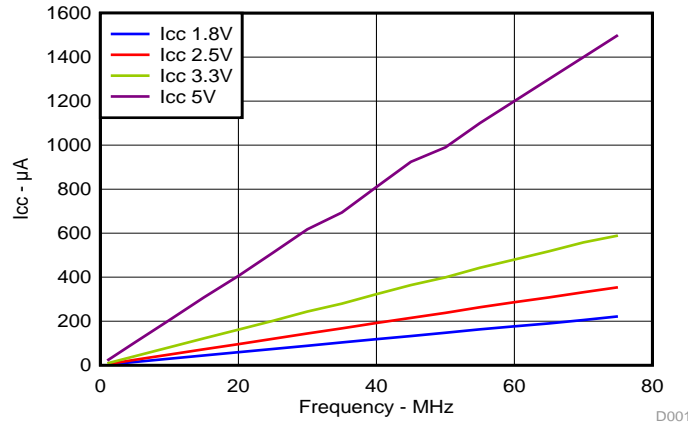


Figure 5. I<sub>CC</sub> vs Frequency

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#).

Each V<sub>CC</sub> pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple V<sub>CC</sub> pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V<sub>CC</sub>, whichever make more sense or is more convenient.

### 11.2 Layout Example

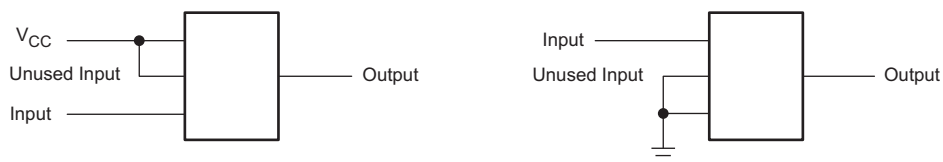


Figure 6. Layout Diagram

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

*Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC2G241DCTRE4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41 Z	<a href="#">Samples</a>
74LVC2G241DCTRG4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41 Z	<a href="#">Samples</a>
74LVC2G241DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C41R	<a href="#">Samples</a>
SN74LVC2G241DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(2WP5, C41) Z	<a href="#">Samples</a>
SN74LVC2G241DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C41J, C41Q, C41R)	<a href="#">Samples</a>
SN74LVC2G241DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C41J, C41Q, C41R)	<a href="#">Samples</a>
SN74LVC2G241YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	(C2, C27)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC2G241DCTRE4	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
74LVC2G241DCTRG4	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
74LVC2G241DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G241DCTR	SM8	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC2G241DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G241DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G241YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC2G241DCTRE4	SM8	DCT	8	3000	182.0	182.0	20.0
74LVC2G241DCTRG4	SM8	DCT	8	3000	182.0	182.0	20.0
74LVC2G241DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G241DCTR	SM8	DCT	8	3000	190.0	190.0	30.0
SN74LVC2G241DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC2G241DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC2G241YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0

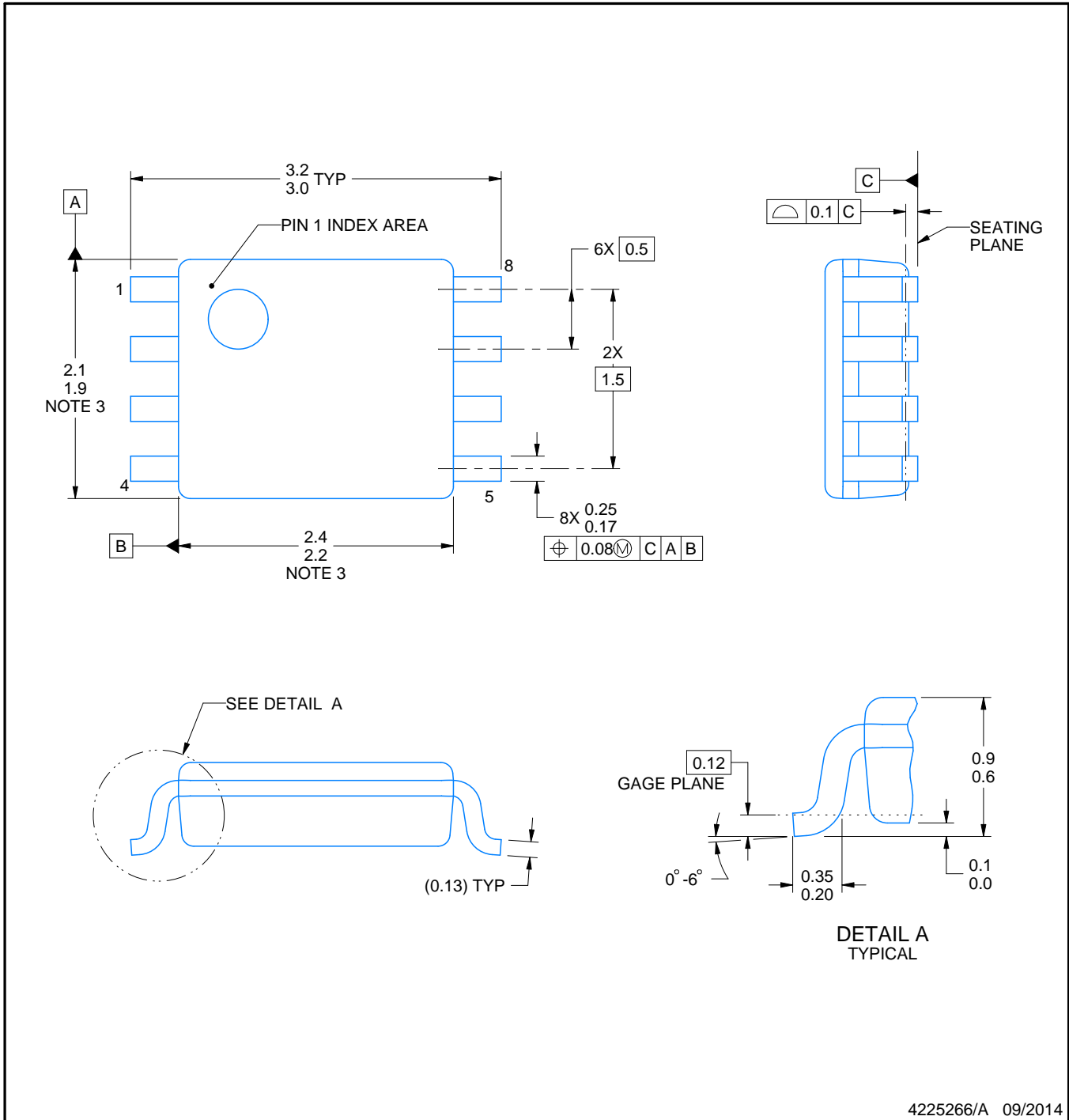
# DCU0008A



# PACKAGE OUTLINE

## VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

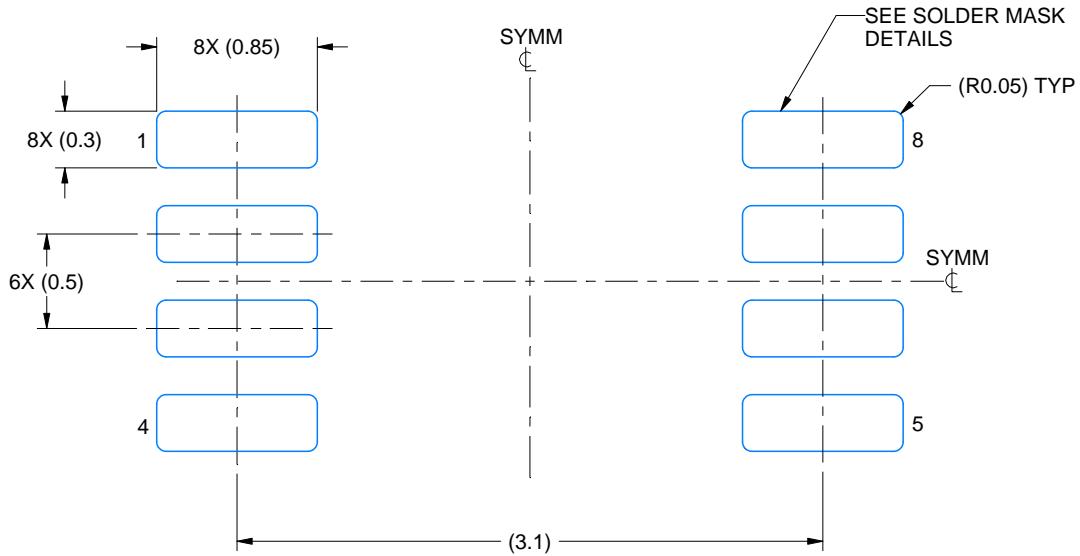


# EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

YZP0008



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

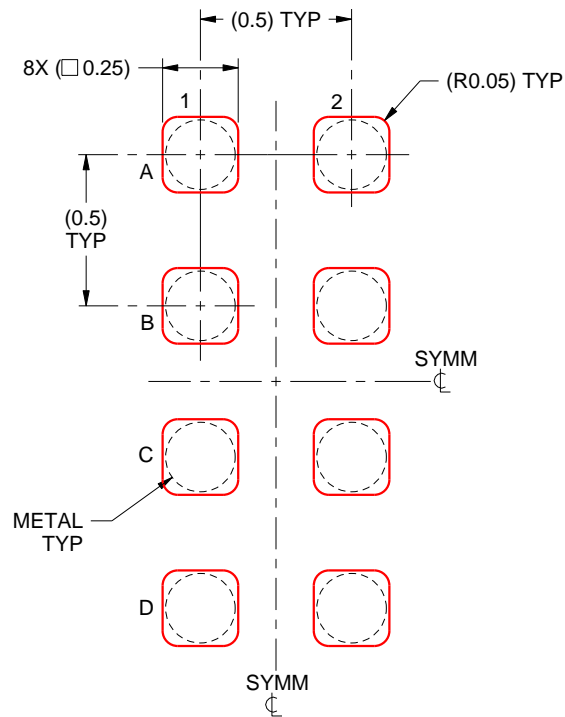
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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