

TAC5682 Full-function SoundWire Stereo Audio Codec with Universal Audio Jack, 4-Channel Digital Mic Support, Integrated DSP, and Stereo 12W Class-D Amplifier

1 Features

- Universal Audio Jack (UAJ)
 - ADC Channel
 - Performance:
 - Mono Mic, Single-ended (Jack Pins 3, 4)
 - DR: 100dB
 - Input Voltage: 0.4V_{RMS} FS
 - Stereo Mic/Line In Single-ended (Jack Pins 1, 2)
 - DR: 95dB
 - Input Voltage: 1V_{RMS} FS
 - THD+N: -85dB
 - Programmable microphone bias (2.25V or 3V)
 - Integrated MICBIAS resistor
 - DAC Channel
 - Integrated Ground Centered Stereo HP Amp
 - Performance:
 - DR: 117dB & THD+N: -90dB at 40mW
 - Output Level: 40mW at 32Ω
 - High impedance output voltage: Single-ended, 2V_{RMS} FS
 - Common Features
 - UAJ type & Button-press detection
 - Automatic OMTP/CTIA configuration
- Class-D Amplifier
 - Stereo 12W Class-D
 - 80% Efficiency (1W, 8Ω, 12.6V)
 - 30μV_{RMS} A-wt. idle channel noise
 - Wide battery range support from 5V up to 23V
 - Integrated speaker protection
- 4-Channel PDM Digital Microphone
- Common features
 - Programmable High Pass Filter (HPF) and bi-quad filters
 - Integrated Tunable DSP and Programmable PLL
- Temperature: -40°C ≤ T_A ≤ +85°C
- User Interface
 - SoundWire 1.2 and SDCA 1.0
 - I²C

- Power Supplies
 - SPKVDD: 5V to 23V
 - DRVDD: 5V
 - AVDD: 1.8V, CPVDD: 1.8V
 - IOVDD: 1.2V or 1.8V

2 Applications

- [Laptops](#)
- [Chromebooks](#) and [Tablets](#)
- [Desktop Computers](#)

3 Description

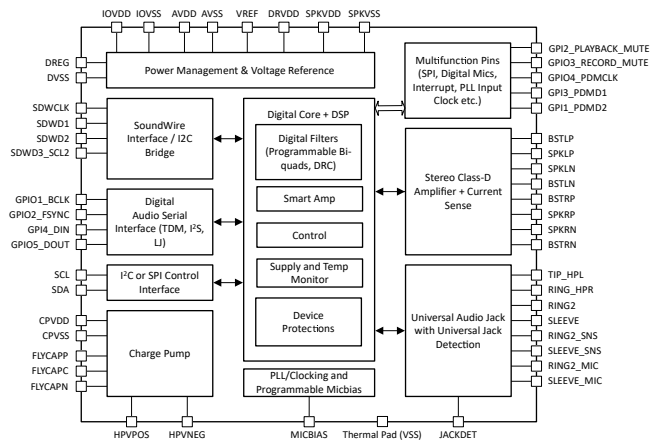
The TAC5682 is a high-performance full-function SoundWire stereo audio codec, integrating a universal audio jack (UAJ) with a stereo Ground Centered Headphone (GCHP) amplifier, 4-channel digital mic, stereo Class-D amplifier along with an integrated DSP for advanced audio processing. The UAJ supports jack and button-press detection, and the ADC and DAC have a dynamic range of 100dB and 117dB respectively. The headphone amp can drive up to 40mW ground-centered output into 32Ω headphone loads. The integrated speaker current sense provides for real-time monitoring of the speakers and the on-chip DSP supports the Texas Instruments Smart Amp speaker protection algorithm. Additionally the TAC5682 integrates programmable channel gain, digital volume control, a low-jitter PLL, programmable High Pass Filter (HPF), along with programmable DRC and bi-quad filters. The TAC5682 supports the MIPI Alliance SoundWire[®] 1.2 protocol and is SDCA 1.0 compliant. The device can be controlled with I²C. These integrated high-performance features make TAC5682 an excellent single-chip choice for PC notebooks and desktop audio applications.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TAC5682	VQFN (48)	6mm × 6mm with 0.4mm pitch

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.





Simplified Block Diagram

ADVANCE INFORMATION

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4 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

4.1 Documentation Support

4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

4.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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4.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

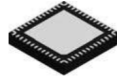
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

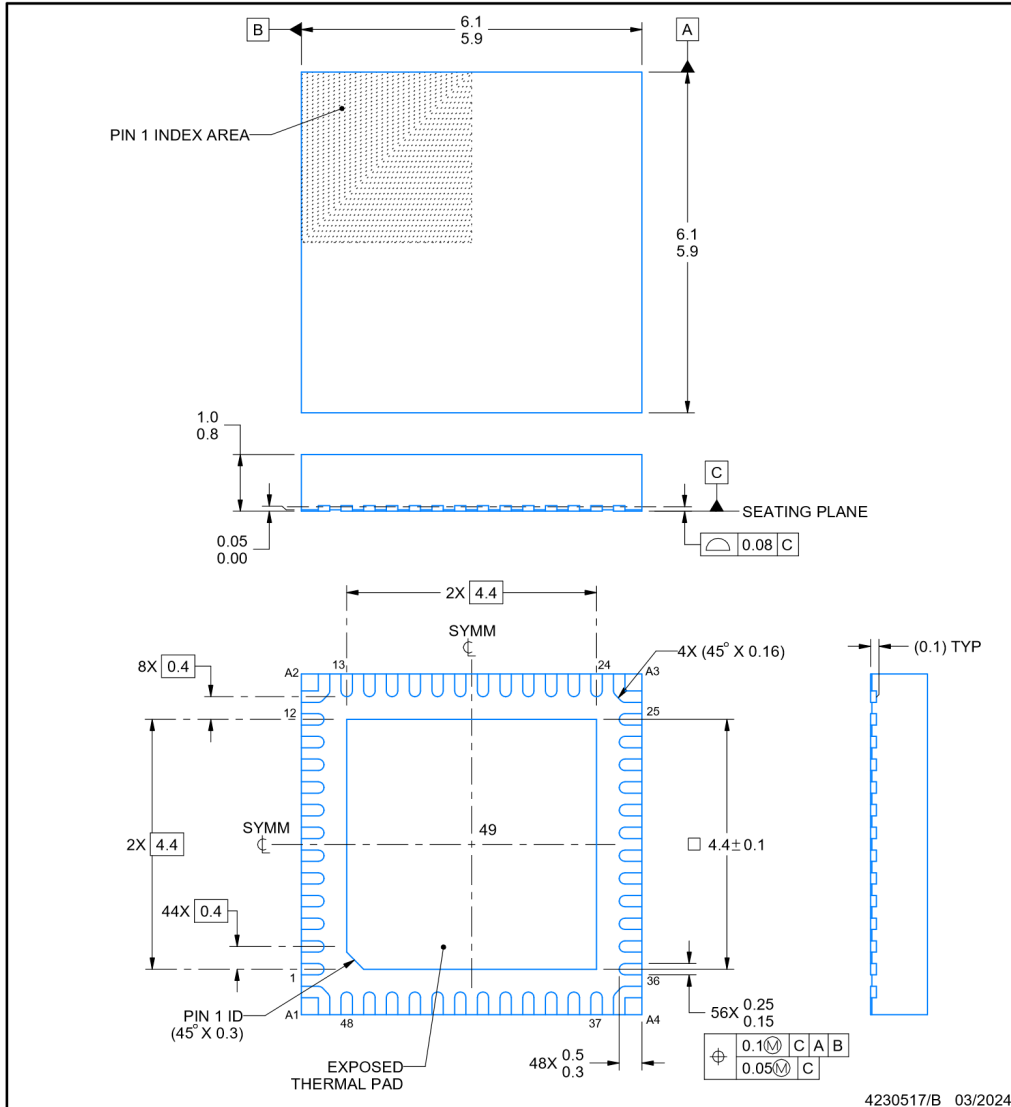


RSL0048F

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

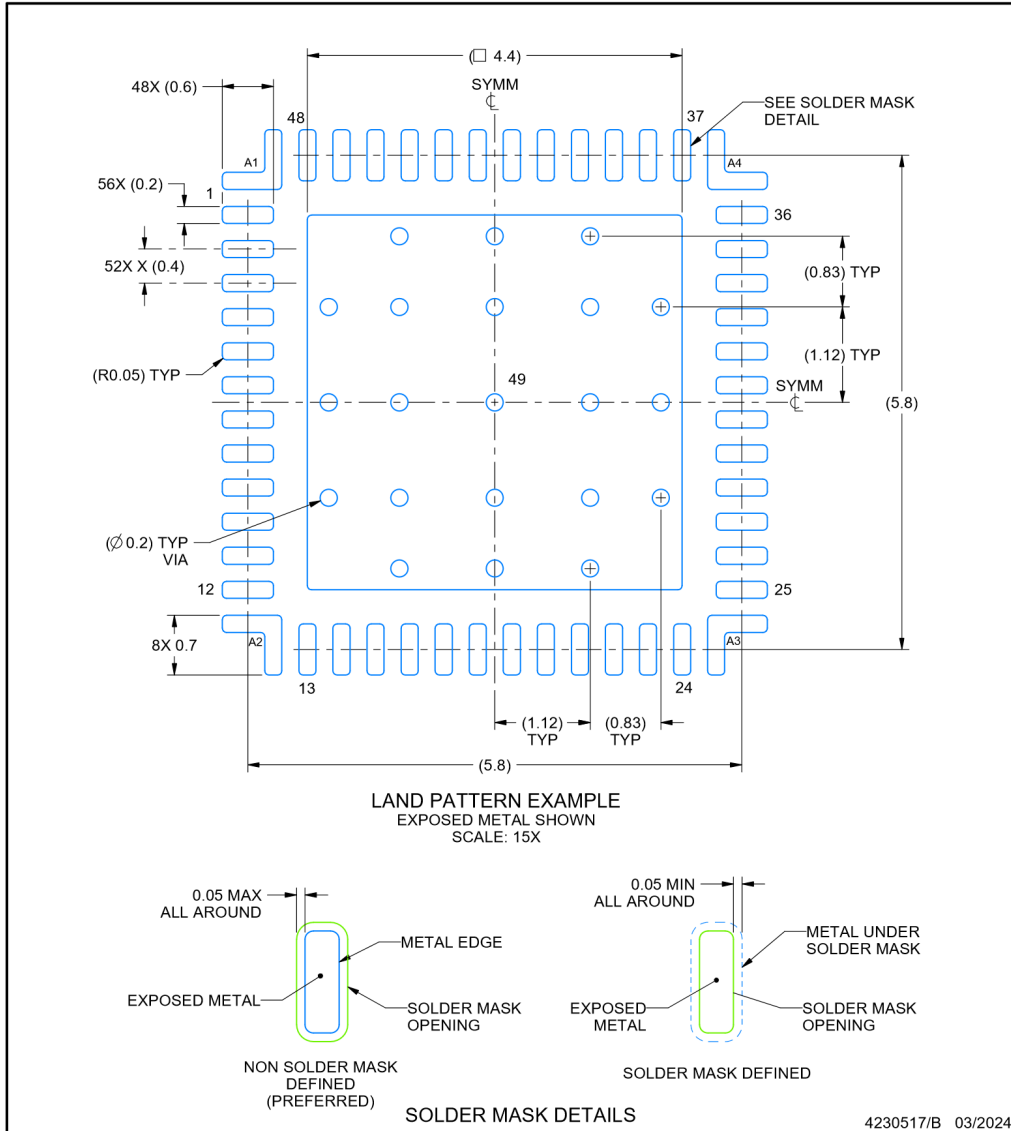
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RSL0048F

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

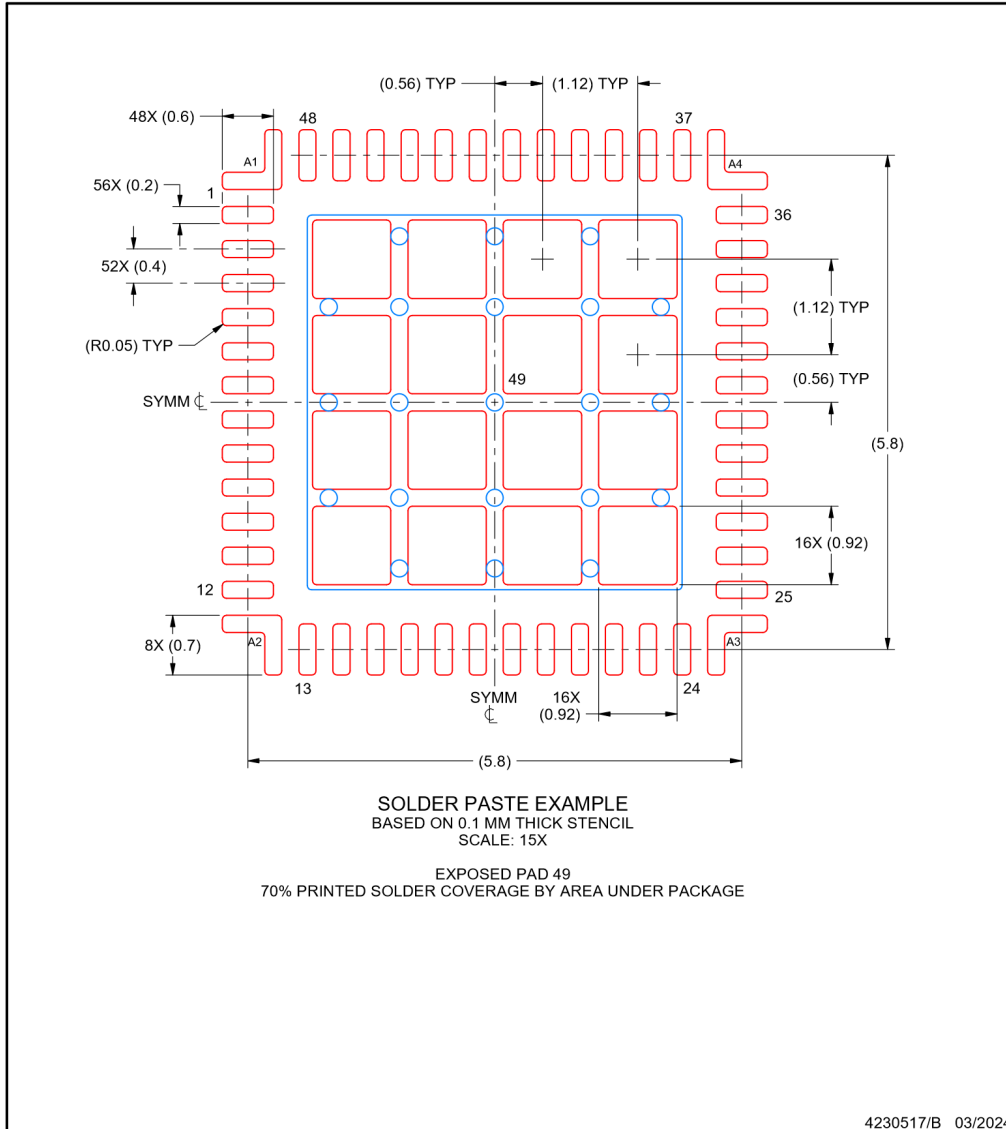
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSL0048F

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

5.1 Package Option Addendum

Packaging Information

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁶⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^{(4) (5)}
TAC5682RSLR	Contact TI	VQFN	RSL	48	3000	RoHS & Green	NiPdAu	Level-2-1YEA R-260C	-40 to 85	TAC5682

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTAC5682RSLR	Active	Preproduction	VQFN (RSL) 48	3000 LARGE T&R	-	Call TI	Call TI	-	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

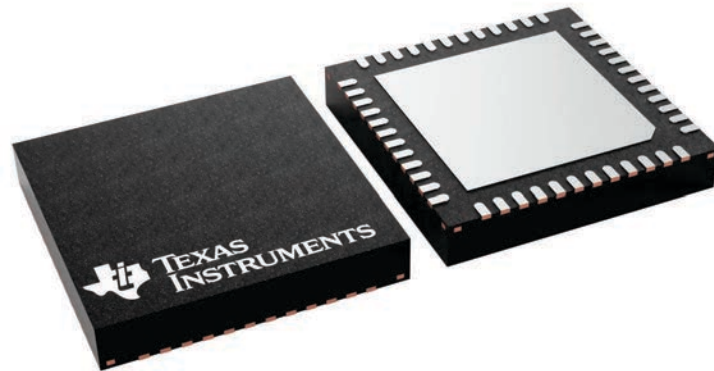
RSL 48

VQFN - 1 mm max height

6 x 6, 0.4 mm pitch

QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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