TAD5242 Hardware-control stereo audio DAC with 120dB dynamic range, and headphone/line driver

1 Features

- – Stereo audio DAC performance:
  - DAC to differential line-out dynamic range: 120dB
  - DAC to pseudo-differential headphone-out dynamic range: 110dB
  - DAC to differential line-out THD+N: –100 dB
  - Output voltage:
    - Differential Line-out/Receiver, $2V_{RMS}$ full-scale
    - Pseudo-differential Headphone, $1V_{RMS}$ full-scale
    - Single-ended Line-out, $1V_{RMS}$ full-scale
  - DAC sample rates (f_s) = 8kHz to 192kHz
- – Key Features
  - Pin or Hardware Control
  - Audio Serial Interface
    - Format: TDM, LJ or I^2S
    - Bus Controller and Target Modes
    - Daisy chain in TDM Mode
    - Word Length: Selectable 24 or 32 Bits
  - Pin-selectable digital interpolation filter options:
    - Linear-phase
    - Low-latency
  - Auto clock detection
  - Interrupt output on clock error
  - Single supply operation AVDD: 1.8V or 3.3V
  - I/O Supply Operation: 1.8V or 3.3V
  - Temperature grade 1: –40°C ≤ T_A ≤ +125°C

2 Applications

- AV Receiver
- IP Network Camera
- Soundbar
- Video Conference System

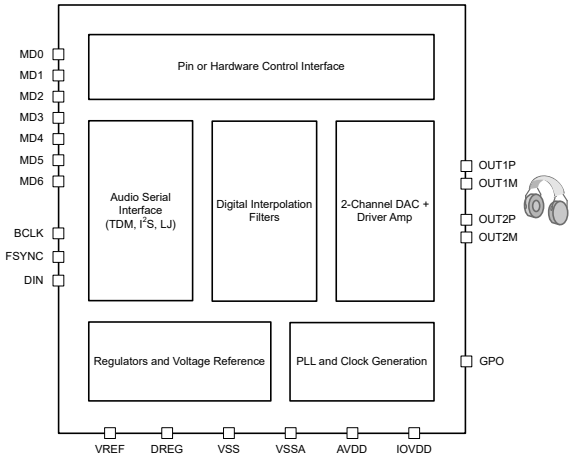
3 Description

The TAD5242 is a $2V_{RMS}$ 120dB stereo audio DAC that can be configured for either line output or headphone load and supports both single-ended and differential output options. The device integrates a phase-locked loop (PLL) and supports sample rates up to 192kHz. TAD5242 can drive upto 62.5 mW into a 16Ω headphone load. The TAD5242 supports time-division multiplexing (TDM), left-justified (LJ), or I^2S audio formats in controller and target modes, and is pin or hardware controlled. These integrated high-performance features, pin control along with a single supply operation, make TAD5242 an excellent choice for space-constrained audio applications.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (NOM)(2)
TAD5242	VQFN (24)	4mm x 4mm with 0.5mm pitch

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram

Table of Contents

4 Pin Configuration and Functions

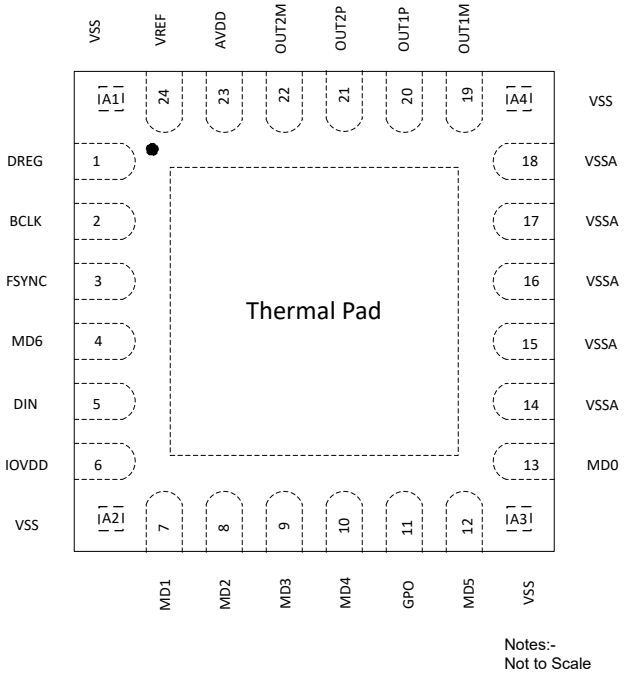


Figure 4-1. 24-Pin QFN Package with Exposed Thermal Pad and Corner Pins, Top View

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VSS	A1	Ground	Ground pin. Short directly to board ground plane.
DREG	1	Digital Supply	Digital on-chip regulator output voltage for digital supply (1.55V, nominal)
BCLK	2	Digital I/O	Audio serial data interface bus bit clock
FSYNC	3	Digital I/O	Audio serial data interface bus frame synchronization signal
MD6	4	Digital I/O	TDM mode: Daisy chain output
			I^2S/LJ mode: Mono/Stereo DAC Channels selection
DIN	5	Digital Input	Audio serial data interface bus input
IOVDD	6	Digital Supply	Digital I/O power supply (1.8V or 3.3V, nominal)
VSS	A2	Ground	Ground pin. Short directly to board ground plane.
MD1	7	Digital Input	Controller mode: Frame rate and BCLK frequency selection
			Target mode: AVDD supply, word length, and interpolation filter type selection
MD2	8	Digital Input	Controller mode: Frame rate and BCLK frequency selection
			Target mode: AVDD supply, word length, and interpolation filter type selection
MD3	9	Digital Input	Controller mode: Controller clock input
			Target mode: Short directly to board ground plane.
MD4	10	Digital Input	DAC output configuration selection
GPO	11	Digital Output	Interrupt output (latched)

Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
MD5	12	Digital Input	DAC output configuration selection
VSS	A3	Ground	Ground pin. Short directly to board ground plane.
MD0	13	Analog Input	Multi-level analog input for controller/target mode and I^2S/TDM/LJ mode selection
VSSA	14	Ground	Short directly to board ground plane
VSSA	15	Ground	Short directly to board ground plane
VSSA	16	Ground	Short directly to board ground plane
VSSA	17	Ground	Short directly to board ground plane
VSSA	18	Ground	Short directly to board ground plane
VSS	A4	Ground	Ground pin. Short directly to board ground plane.
OUT1M	19	Analog Output	Analog output 1M pin
OUT1P	20	Analog Output	Analog output 1P pin
OUT2P	21	Analog Output	Analog output 2P pin
OUT2M	22	Analog Output	Analog output 2M pin
AVDD	23	Analog Supply	Analog power supply (1.8V or 3.3V, nominal)
VREF	24	Analog	Analog reference voltage filter output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD to VSS (thermal pad)	–0.3	3.9	V
Supply voltage	IOVDD to VSS (thermal pad)	–0.3	3.9	V
Ground voltage differences	VSSA to VSS (thermal pad)	–0.3	0.3	V
Digital input voltage	Digital input pins voltage to VSS (thermal pad)	–0.3	IOVDD + 0.3	V
Temperature	Functional ambient, T_A	–55	125	°C
	Operating ambient, T_A	–40	125	
	Junction, T_J	–40	150	
	Storage, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
POWER					
AVDD(1)	Analog supply voltage to VSS (thermal pad) - AVDD 3.3V operation	3.0	3.3	3.6	V
	Analog supply voltage to VSS (thermal pad) - AVDD 1.8V operation	1.65	1.8	1.95	
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 3.3V operation	3.0	3.3	3.6	V
	IO supply voltage to VSS (thermal pad) - IOVDD 1.8V operation	1.65	1.8	1.95	
INPUTS					
IO	Digital input pins (MD1 to MD6) voltage to VSS (thermal pad)	0		IOVDD	V
MD0	MD0 pin w.r.t VSS (thermal pad)	0		AVDD	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		125	°C

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
OTHERS					
CCLK	MD3 controller mode clock frequency (CCLK) - IOVDD 3.3V operation			36.864(2)	MHz
	MD3 controller mode clock frequency (CCLK) - IOVDD 1.8V operation			24.576(2)	
C_L	Digital output load capacitance		20	50	pF

(1) VSSA and VSS (thermal pad); all ground pins must be tied together and must not differ in voltage by more than 0.2V.
(2) CCLK input rise time (V_{IL} to V_{IH}) and fall time (V_{IH} to V_{IL}) must be less than 5ns. For better audio noise performance, CCLK input must be used with low jitter.

5.4 Thermal Information

THERMAL METRIC(1)		TAD5242 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256 × f_S, TDM target mode, and linear phase interpolation filter, with 1200Ω/600Ω line-out load in differential/single-ended configuration or 32Ω receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DAC Performance for Line Output/Head Phone Playback						
	Full Scale Output Voltage	Differential output between OUTxP and OUTxM, AVDD = 3.3V		2		V_{RMS}
		Differential output between OUTxP and OUTxM, AVDD = 1.8V		1		
		Single-ended output, AVDD = 3.3V		1		
		Single-ended output, AVDD = 1.8V		0.5		
		Pseudo-differential output between OUTxP and OUT1M with external common-mode sense, AVDD = 3.3V		1		
		Pseudo-differential output between OUTxP and OUT1M with external common-mode sense, AVDD = 1.8V		0.5		
SNR	Signal-to-noise ratio, A-weighted(1) (2)	Differential output, 0dBFS Signal, AVDD = 3.3V		120		dB
		Single-ended output, 0dBFS Signal, AVDD = 3.3V		111		
		Pseudo-differential output, 0dBFS Signal, AVDD = 3.3V		110		
		Differential output, 0dBFS Signal, AVDD = 1.8V		115		
		Single-ended output, 0dBFS Signal, AVDD = 1.8V		105		
		Pseudo-differential output, 0dBFS Signal, AVDD = 1.8V		104		

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256 × f_S, TDM target mode, and linear phase interpolation filter, with 1200Ω/600Ω line-out load in differential/single-ended configuration or 32Ω receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DR	Dynamic range, A-weighted(2)	Differential output, –60dBFS Signal, AVDD = 3.3V		120		dB
		Single-ended output, –60dBFS Signal, AVDD = 3.3V		111		
		Pseudo-differential output, –60dBFS Signal, AVDD = 3.3V		110		
		Differential output, –60dBFS Signal, AVDD = 1.8V		115		
		Single-ended output, –60dBFS Signal, AVDD = 1.8V		105		
		Pseudo-differential output, –60dBFS Signal, AVDD = 1.8V		104		
THD+N	Total harmonic distortion(2)	Differential output, –1dBFS Signal, AVDD = 3.3V		–100		dB
THD+N	Total harmonic distortion(2)	Single-ended output, –1dBFS Signal, AVDD = 3.3V		–96		dB
	Headphone Load Range(3)		8	16	300	Ω
	Headphone/Line-out Cap Load		0	100	550	pF
	Line-out Load Range		600			Ω
DAC Channel OTHER PARAMETERS						
	Output Offset	0 Input, Differential Line-output		0.5		mV
	Output Common Mode	Common Mode Level for OUTxP and OUTxM, AVDD = 1.8V		0.9		V
	Output Common Mode	Common Mode Level for OUTxP and OUTxM, AVDD = 3.3V		1.65		V
	Common Mode Error	DC Error in Common Mode Voltage		±10		mV
	Output Signal Bandwidth			20		kHz
	Input data word length	Pin-selectable	24		32	Bits
	Interchannel isolation			–120		dB
	Gain Error			0.1		dB
	Interchannel gain mismatch			0.1		dB
	Interchannel phase mismatch	1kHz sinusoidal signal		0.01		Degrees
PSRR	Power-supply rejection ratio	100mV_{PP}, 1kHz sinusoidal signal on AVDD, differential input, 0dB channel gain		120		dB
P_{out}	Output Power Delivery	Receiver/Headphone R_L=16Ω, THD+N<1% in Differential or Pseudo-differential mode		62.5		mW
DIGITAL I/O						
V_{IL}	Low-level digital input logic voltage threshold	All digital pins, IOVDD 1.8V operation	–0.3		0.35 x IOVDD	V
		All digital pins, IOVDD 3.3V operation	–0.3		0.8	
V_{IH}	High-level digital input logic voltage threshold	All digital pins, IOVDD 1.8V operation	0.65 x IOVDD		IOVDD + 0.3	V
		All digital pins, IOVDD 3.3V operation	2		IOVDD + 0.3	

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256 × f_S, TDM target mode, and linear phase interpolation filter, with 1200Ω/600Ω line-out load in differential/single-ended configuration or 32Ω receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OL}	Low-level digital output voltage	All digital pins, I_{OL} = –2 mA, IOVDD 1.8V operation			0.45	V
		All digital pins, I_{OL} = –2 mA, IOVDD 3.3V operation			0.4	
V_{OH}	High-level digital output voltage	All digital pins, I_{OH} = 2 mA, IOVDD 1.8V operation	IOVDD – 0.45			V
		All digital pins, I_{OH} = 2 mA, IOVDD 3.3V operation	2.4			
I_{IL}	Input logic-low leakage for digital inputs	All digital pins, input = 0V	–5	0.1	5	µA
I_{IH}	Input logic-high leakage for digital inputs	All digital pins, input = IOVDD	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pulldown resistance for digital I/O pins when asserted on			20		kΩ
TYPICAL SUPPLY CURRENT CONSUMPTION						
I_{AVDD}	Current consumption in sleep mode or low power mode	All external clocks stopped with MD3 pin grounded, AVDD = 3.3V		0.8		mA
I_{IOVDD}		All external clocks stopped with MD3 pin grounded, IOVDD = 3.3V		0.6		µA
I_{IOVDD}		All external clocks stopped with MD3 pin grounded, IOVDD = 1.8V		0.2		
I_{AVDD}	Current consumption with DAC to Headphone 2-channel operation at f_S 16kHz, I^2S Target Mode, BCLK = 64 × f_S	AVDD = 3.3V		16.3		mA
I_{IOVDD}		IOVDD = 3.3V		0.06		
I_{IOVDD}		IOVDD = 1.8V		0.03		
I_{AVDD}	Current consumption with DAC to Headphone 2-channel operation at f_S 48kHz, I^2S Target Mode, BCLK = 64 × f_S	AVDD = 3.3V		20		mA
I_{IOVDD}		IOVDD = 3.3V		0.06		
I_{IOVDD}		IOVDD = 1.8V		0.03		
I_{AVDD}	Current consumption with DAC to Line-out 2-channel operation at f_S 16kHz, I^2S Target Mode, BCLK = 64 × f_S	AVDD = 3.3V		17		mA
I_{AVDD}	Current consumption with DAC to Line-out 2-channel operation at f_S 48kHz, I^2S Target Mode, BCLK = 64 × f_S	AVDD = 3.3V		20		mA
I_{IOVDD}		IOVDD = 3.3V		0.06		
I_{IOVDD}		IOVDD = 1.8V		0.03		

(1) Ratio of output level with 1kHz full-scale sine-wave input, to the output level with no generator input signal and input shorted to ground, measured with an A-weighted filter over a 20Hz to 20kHz bandwidth

(2) All performance measurements done with 20kHz low-pass filter and, where noted, an A-weighted filter. Failure to use such a filter can result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, can affect dynamic specification values.

(3) For headphone loads <32Ω, input signal level should be limited as per the output power delivery specifications.

5.6 Timing Requirements: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3V or 1.8V and 20pF load on all outputs (unless otherwise noted), see Figure 5-1 for timing diagram where DOUT refers to Daisy Chain Output when applicable

			MIN	NOM	MAX	UNIT
$t_{(BCLK)}$	BCLK period	IOVDD = 1.8V	80			ns
		IOVDD = 3.3V	40			
$t_{H(BCLK)}$	BCLK high pulse duration(1)	IOVDD = 1.8V	36			ns
		IOVDD = 3.3V	18			
$t_{L(BCLK)}$	BCLK low pulse duration(1)	IOVDD = 1.8V	36			ns
		IOVDD = 3.3V	18			
$t_{SU(FSYNC)}$	FSYNC setup time	IOVDD = 1.8V	8			ns
		IOVDD = 3.3V	8			
$t_{HLD(FSYNC)}$	FSYNC hold time	IOVDD = 1.8V	8			ns
		IOVDD = 3.3V	8			
$t_{SU(DIN)}$	DIN setup time	IOVDD = 1.8V	8			ns
		IOVDD = 3.3V	8			
$t_{HLD(DIN)}$	DIN hold time	IOVDD = 1.8V	16			ns
		IOVDD = 3.3V	8			
$t_{r(BCLK)}$	BCLK rise time	10% - 90% rise time, IOVDD = 1.8V			10	ns
		10% - 90% rise time, IOVDD = 3.3V			10	
$t_{f(BCLK)}$	BCLK fall time	90% - 10% fall time, IOVDD = 1.8V			10	ns
		90% - 10% fall time, IOVDD = 3.3V			10	

(1) To meet the timing specifications, the BCLK minimum high or low pulse duration must be higher than 25ns, if the DOUT data line is latched on the opposite BCLK edge polarity from the one used by the device to transmit the DOUT data at IOVDD = 3.3V.

5.7 Switching Characteristics: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3V or 1.8V and 20pF load on all outputs (unless otherwise noted); see Figure 5-1 for timing diagram where DOUT refers to Daisy Chain Output when applicable

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(DOUT-BCLK)}$	BCLK to DOUT delay	50% of BCLK to 50% of DOUT, IOVDD = 1.8V			26	ns
		50% of BCLK to 50% of DOUT, IOVDD = 3.3V			19	
$t_{d(DOUT-FSYNC)}$	FSYNC to DOUT delay in TDM mode	50% of FSYNC to 50% of DOUT, IOVDD = 1.8V			26	ns
	FSYNC to DOUT delay in TDM mode	50% of FSYNC to 50% of DOUT, IOVDD = 3.3V			19	
$f_{(BCLK)}$	BCLK output clock frequency; controller mode(1)	IOVDD = 1.8V			12.288	MHz
		IOVDD = 3.3V			24.576	
$t_{d(FSYNC)}$	BCLK to FSYNC delay; controller mode	50% of BCLK to 50% of FSYNC, IOVDD = 1.8V			26	ns
		50% of BCLK to 50% of FSYNC, IOVDD = 3.3V			19	
$t_{H(BCLK)}$	BCLK high pulse duration; controller mode	IOVDD = 1.8V	36			ns
		IOVDD = 3.3V	18			
$t_{L(BCLK)}$	BCLK low pulse duration; controller mode	IOVDD = 1.8V	36			ns
		IOVDD = 3.3V	18			
$t_{r(BCLK)}$	BCLK rise time; controller mode	10% - 90% rise time, IOVDD = 1.8V			10	ns
		10% - 90% rise time, IOVDD = 3.3V			10	

at T_A = 25°C, IOVDD = 3.3V or 1.8V and 20pF load on all outputs (unless otherwise noted); see Figure 5-1 for timing diagram where DOUT refers to Daisy Chain Output when applicable

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{f(BCLK)}$	BCLK fall time; controller mode	90% - 10% fall time, IOVDD = 1.8V			10	ns
		90% - 10% fall time, IOVDD = 3.3V			10	

(1) To meet the timing specifications, the BCLK output clock frequency must be lower than 18.5MHz, if the DOUT data line is latched on the opposite BCLK edge polarity from the one used by the device to transmit DOUT data at IOVDD = 3.3V.

5.8 Timing Diagrams

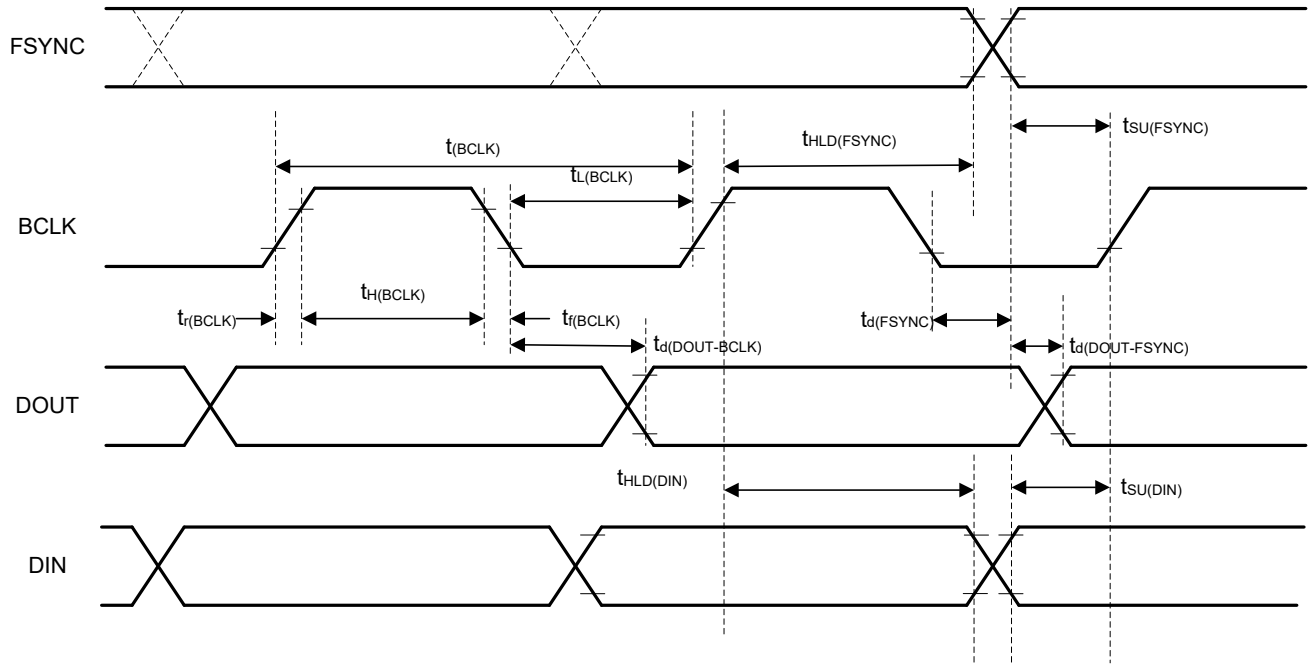
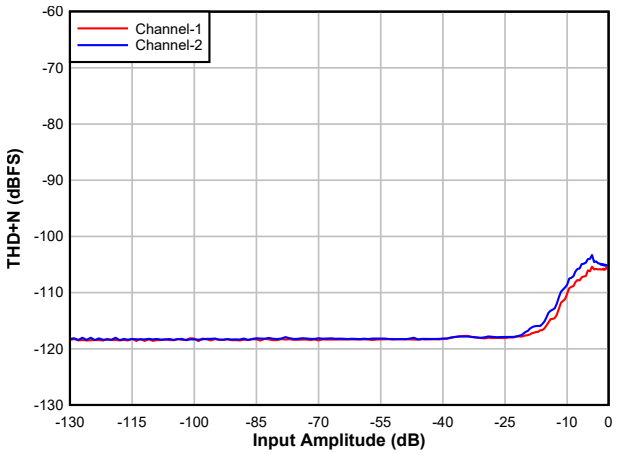


Figure 5-1. TDM, I²S, and LJ Interface Timing Diagram

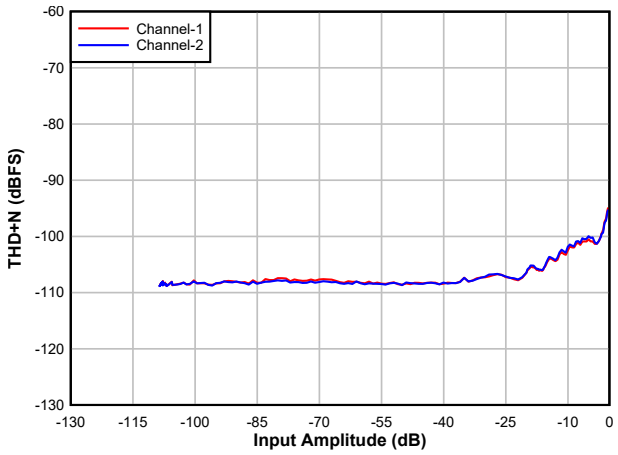
5.9 Typical Characteristics

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256×f_S, TDM target mode, and linear phase interpolation filter, with 1200Ω/600Ω line-out load in differential/ single-ended configuration or 32Ω receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted



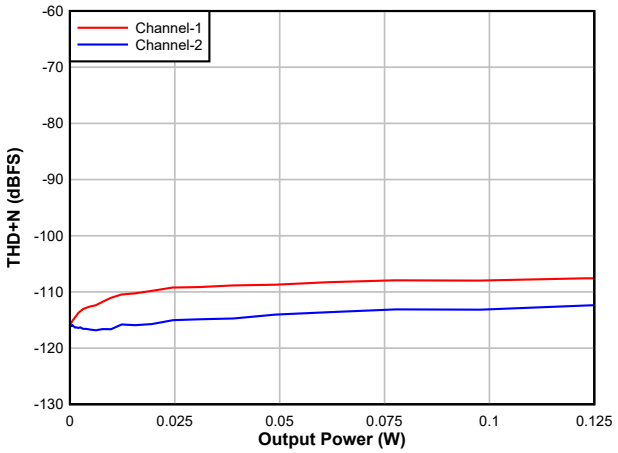
Differential output

Figure 5-2. DAC THD+N Level vs Input



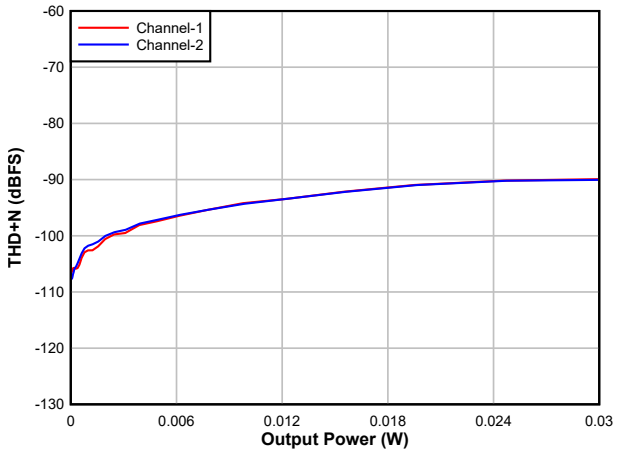
Single-ended output

Figure 5-3. DAC THD+N Level vs Input



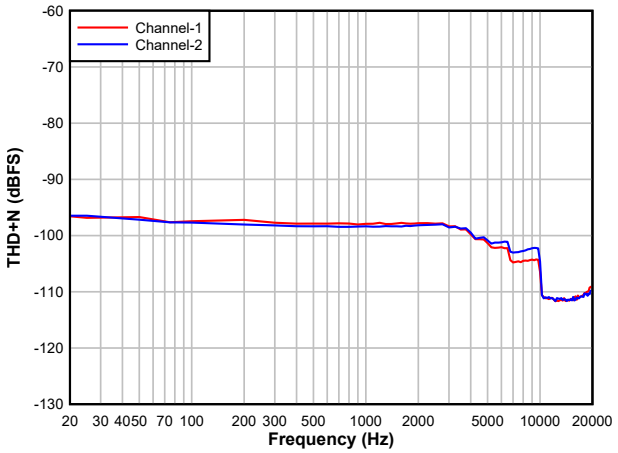
Differential receiver/headphone output, 32Ω load

Figure 5-4. DAC THD+N Level vs Output Power



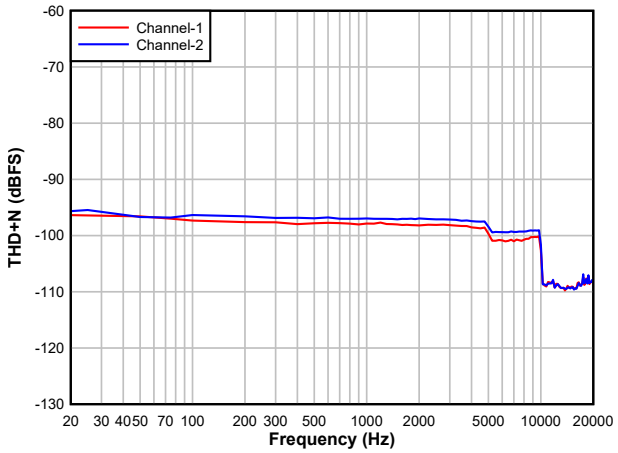
Pseudo-differential output, 32Ω headphone load

Figure 5-5. DAC THD+N Level vs Output Power



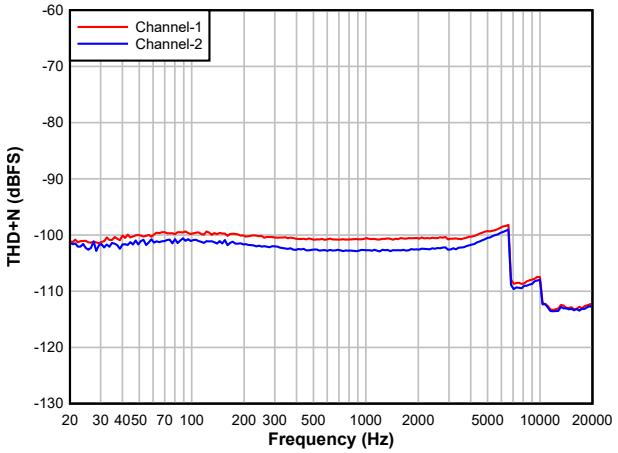
Differential output

Figure 5-6. DAC THD+N Level vs Frequency



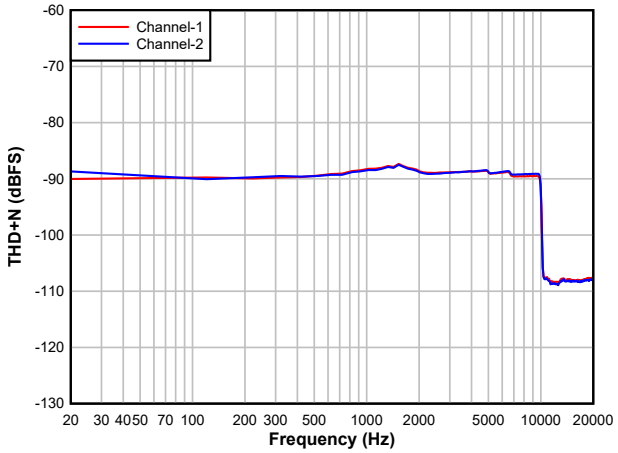
Single-ended output

Figure 5-7. DAC THD+N Level vs Frequency



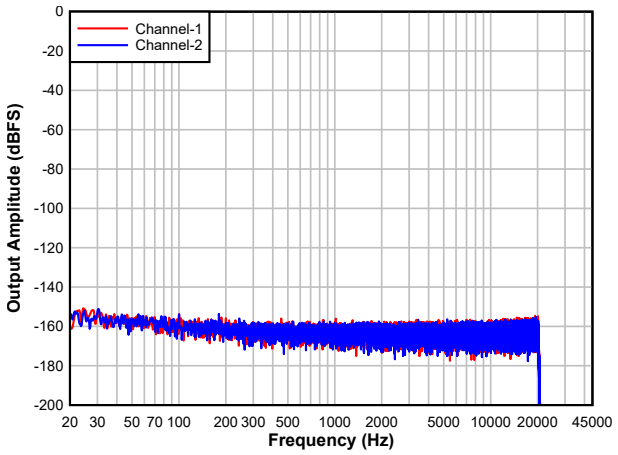
Differential receiver/headphone output, 32Ω load

Figure 5-8. DAC THD+N Level vs Frequency



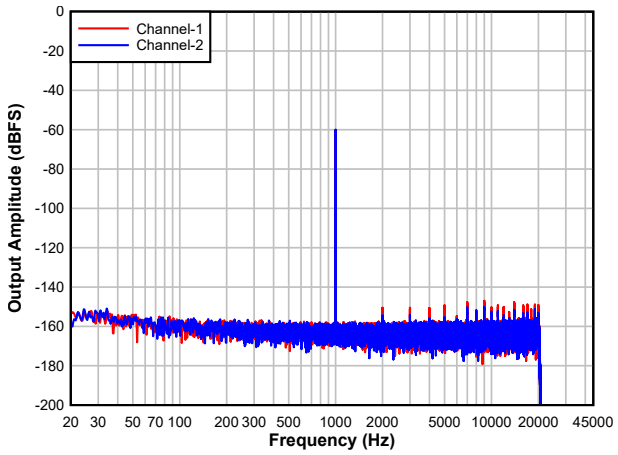
Pseudo-differential output, 32Ω headphone load

Figure 5-9. DAC THD+N Level vs Frequency



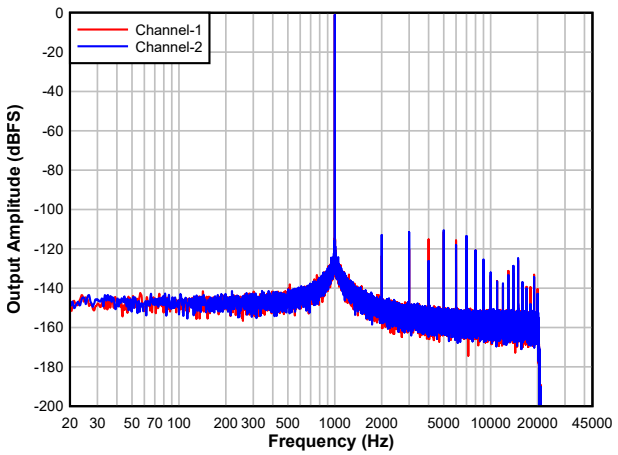
Differential output, idle-channel input

Figure 5-10. DAC FFT



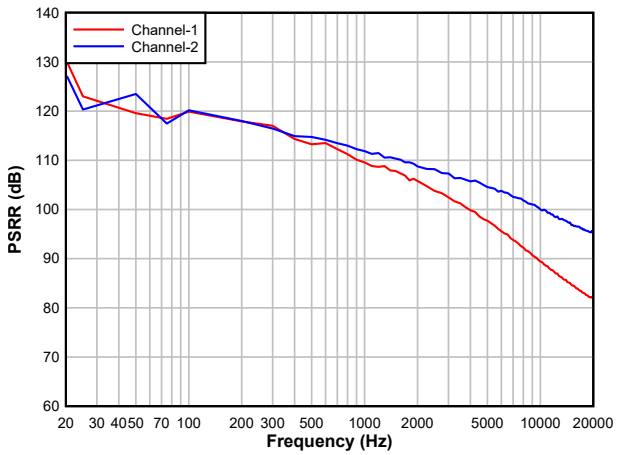
Differential output, -60dBFS input

Figure 5-11. DAC FFT



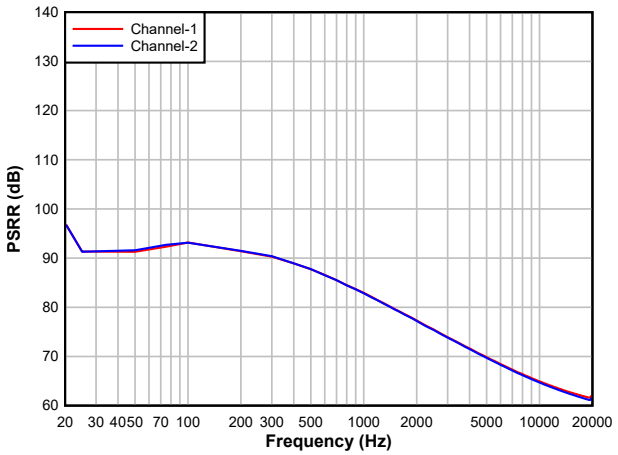
Differential output, -1dBFS input

Figure 5-12. DAC FFT



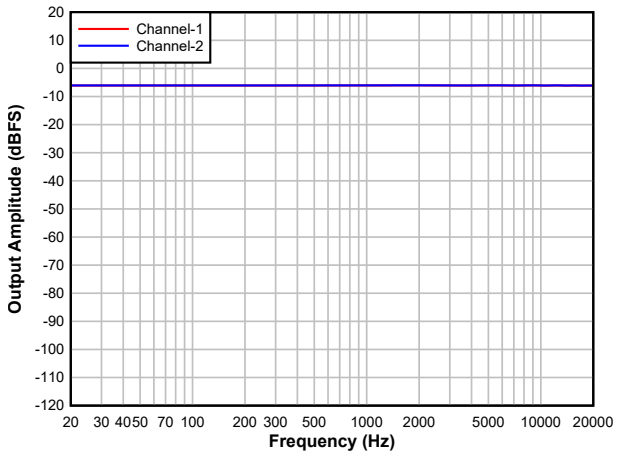
Differential output

Figure 5-13. DAC PSRR vs Frequency



Single-ended output

Figure 5-14. DAC PSRR vs Frequency



Differential output, -6dBFS input

Figure 5-15. DAC Frequency Response

6 Detailed Description

6.1 Overview

The TAD5242 is a high-performance, low-power, stereo audio digital-to-analog converter (DAC). This device is intended for broad market applications such as ruggedized communication equipment, IP network camera, professional audio and multimedia applications. This device integrates a host of features that reduce cost, board space, and power consumption in space-constrained system designs. Package, performance, and compatible configuration across an extended family makes this device well suited for scalable system designs.

The TAD5242 consists of the following features:

- 2-channel, multi-bit, high-performance delta-sigma (ΔΣ) DACs
- Pin or Hardware controlled device configurations
- Configurable single-ended, differential or pseudo-differential audio outputs
- Linear-phase or Low-latency digital interpolation filters
- Integrated low-jitter, phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

6.2 Functional Block Diagram

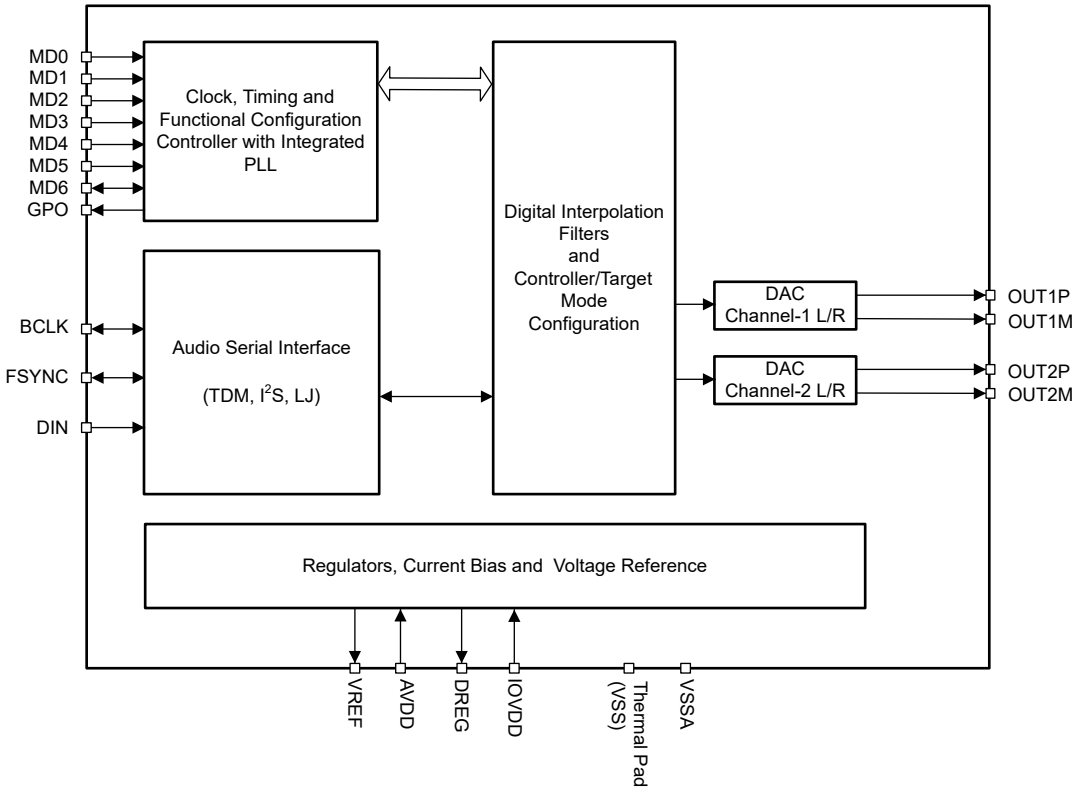


Figure 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Hardware Control

The device supports simple hardware-pin-controlled options to select a specific mode of operation and audio interface for a given system as summarized in Table 6-1. The MD1 to MD6 pins are connected to either logic low (VSS) or logic high (IOVDD), and the MD0 pin can be connected to AVDD or VSS through different pull-up or pull-down resistors.

Table 6-1. Pin Selectable Configurations Summary

PIN	TARGET MODE	CONTROLLER MODE
MD0	Multi-level analog input for controller/target mode and I²S/TDM/LJ mode selection	
MD1	AVDD supply, word length, and interpolation filter type selection	Frame rate and BCLK frequency selection
MD2		
MD3	Ground	Controller clock input
MD4	DAC output configuration selection (Differential Line-out/ Differential Receiver/Headphone/Single-ended Line-out/ Pseudo-differential Headphone)	
MD5		
MD6	TDM mode: Daisy chain output or I²S/LJ mode: Mono/Stereo selection	

6.3.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the TAD5242 on the digital audio serial interface (ASI), or audio bus. This bus can be operated in target or controller mode through pin control. The ASI supports TDM, I²S and Left-Justified bus protocols. The data is in MSB-first, two's-complement pulse code modulation (PCM) format, with pin-selectable word-length configuration.

The device supports an audio bus controller or target mode of operation using the hardware pin MD0. In target mode, FSYNC and BCLK work as input pins whereas in controller mode, FSYNC and BCLK work as output pins generated by the device. Table 6-2 shows the controller and target mode selection using the MD0 pin.

Table 6-2. Controller and Target Mode Selection

MD0	CONTROLLER AND TARGET SELECTION
Short to Ground	Target I²S Mode
Short to Ground with 4.7K Ohms	Target TDM Mode
Short to AVDD	Controller I²S Mode
Short to AVDD with 4.7K Ohms	Controller TDM Mode
Short to AVDD with 22K Ohms	Target LJ Mode

The word length for audio serial interface (ASI) in TAD5242 can be selected through MD1 and MD2 Pins in target mode of operation. The TAD5242 also supports 1.8V AVDD operation in target mode with 32-bit word length. Table 6-3 shows the configuration table for setting the word length, AVDD supply voltage and interpolation filter type applicable in Target Mode. In controller mode, AVDD supply mode is 3.3V, word length of 32-bits is supported, interpolation filter is configured in the linear-phase and the MD1 and MD2 Pins control the system clock configuration described in Table 6-8.

Table 6-3. Word Length, Supply Mode, and Interpolation Filter Selection

MD2	MD1	WORD LENGTH, SUPPLY MODE, AND INTERPOLATION FILTER SELECTION (Valid for Target Mode only)
Low	Low	AVDD=3.3V, Word Length=32, Linear-phase Filter
Low	High	AVDD=1.8V, Word Length=32, Linear-phase Filter
High	Low	AVDD=3.3V, Word Length=24, Linear-phase Filter
High	High	AVDD=3.3V, Word Length=32, Low-latency phase Filter

The TAD5242 also offers daisy chain option for TDM mode of operation. This option is auto enabled whenever device is selected to be in TDM Mode with MD0. MD6 Pin acts as a Daisy Chain output in this mode. In this case, for a TDM with N slots, the device plays the audio present on the last 2 slots, and the remaining slots are shifted to the right and sent on the MD6 pin, as shown in the block diagram in the Figure 6-2.

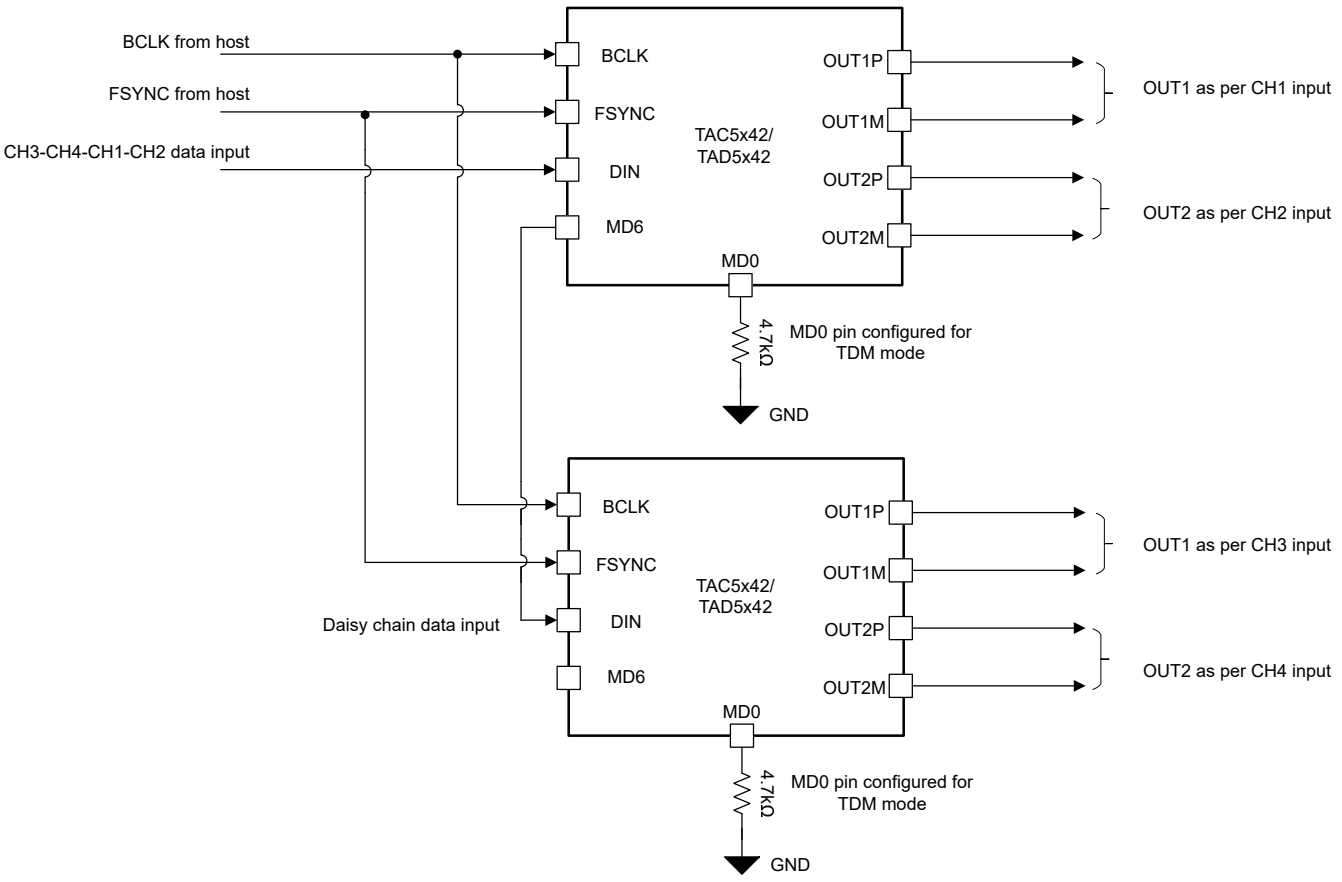


Figure 6-2. Daisy Chain in TDM Mode Block Diagram

6.3.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit is transmitted on the rising edge of BCLK and received on the falling edge of BCLK. Figure 6-3 and Figure 6-4 show the protocol timing for TDM operation with various configurations. DOUT refers to the Daisy Chain Output.

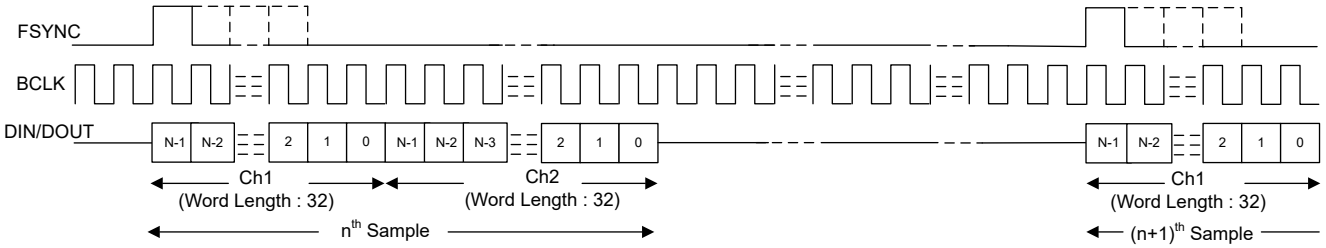


Figure 6-3. TDM Mode Protocol Timing (MD0 shorted to ground with 4.7K Ohms) in Target Mode

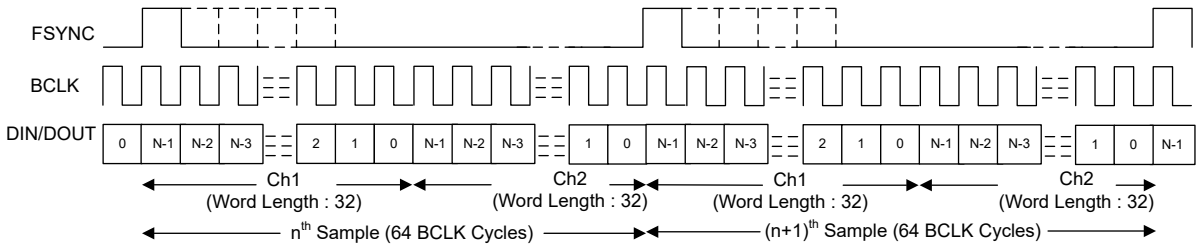


Figure 6-4. TDM Mode Protocol Timing (MD0 shorted to AVDD with 4.7K Ohms) in Controller Mode

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active input and output channels times the configured word length of the input and output channel data. The DOUT pin is in a Hi-Z state for the extra unused bit clock cycles. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock, but also supports multiples as well.

6.3.2.2 Inter IC Sound (I^2S) Interface

The standard I^2S protocol is defined for only two channels: left and right. In I^2S mode, the MSB of the left slot 0 is received on the rising edge of BCLK in the second cycle after the *falling* edge of FSYNC. The MSB of the right slot 0 is received on the rising edge of BCLK in the second cycle after the *rising* edge of FSYNC. Each subsequent data bit is received on the rising edge of BCLK. In controller mode, FSYNC is transmitted on the falling edge of BCLK. Figure 6-5 and Figure 6-6 show the protocol timing for I^2S operation in target and controller mode of operation.

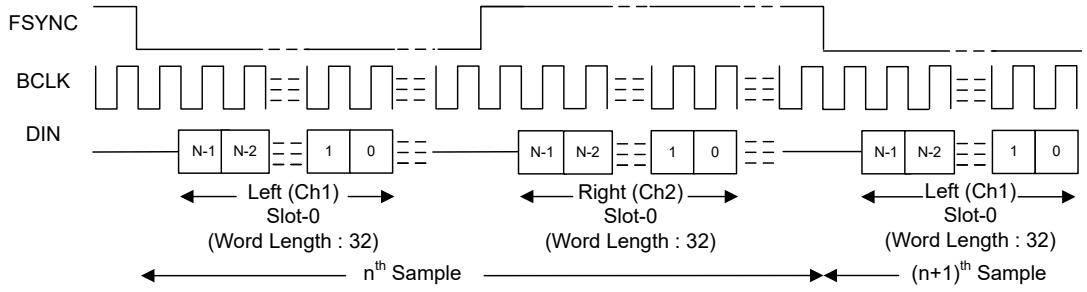


Figure 6-5. I^2S Mode Protocol Timing (MD0 shorted to ground) in Target Mode

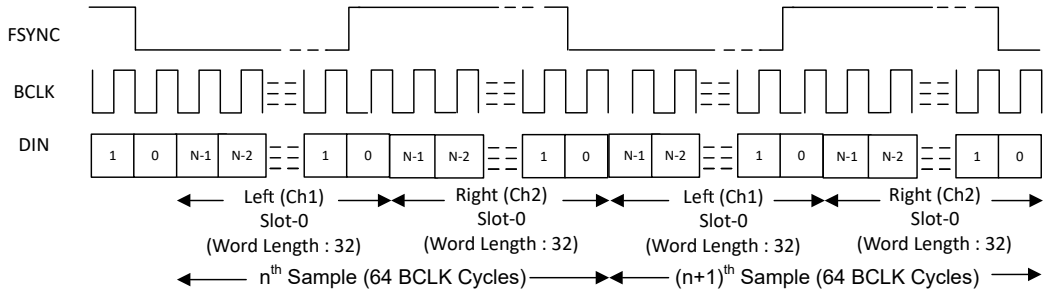


Figure 6-6. I^2S Protocol Timing (MD0 shorted to AVDD) in Controller Mode

For proper operation of the audio bus in I^2S mode, the number of bit clocks per frame must be greater than or equal to the number of active input channels (including left and right slots) times the configured word length of the input channel data.

6.3.2.3 Left-Justified (LJ) Interface

The standard LJ protocol is defined for only two channels: left and right. In LJ mode, the MSB of the left slot 0 is received in the same BCLK cycle after the *rising* edge of FSYNC. Each subsequent data bit is received on the rising edge of BCLK. The MSB of the right slot 0 is received in the same BCLK cycle after the *falling* edge of FSYNC. Figure 6-7 illustrates the protocol timing for LJ operation in target mode of coperation.

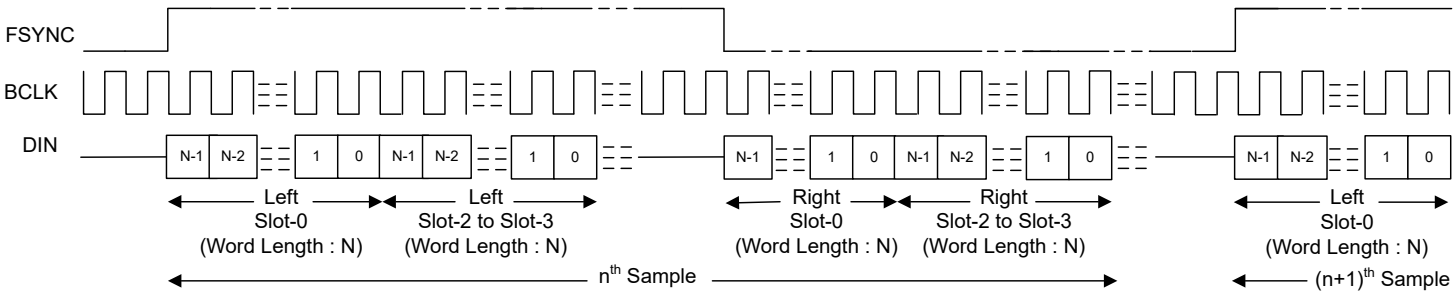


Figure 6-7. LJ Mode Standard Protocol Timing (MD0 shorted to AVDD with 22K Ohms) in Target Mode

For proper operation of the audio bus in LJ mode, the number of bit clocks per frame must be greater than or equal to the number of active input channels (including left and right slots) times the configured word length of the input channel data.

6.3.3 Phase-Locked Loop (PLL) and Clock Generation

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the DAC modulators and digital filter engine, as well as other control blocks.

In target mode of operation, the device supports the various output data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. Table 6-4 to Table 6-7 list the supported FSYNC and BCLK frequencies depending on IOVDD Supply.

Table 6-4. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies (IOVDD - 3.3V Operation)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)
16	**Reserved**	0.256	0.384	0.512	0.768	1.536	3.072
24	**Reserved**	0.384	0.576	0.768	1.152	2.304	4.608
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288
96	0.768	1.536	2.304	3.072	4.608	9.216	18.432
128	1.024	2.048	3.072	4.096	6.144	12.288	24.576
192	1.536	3.072	4.608	6.144	9.216	18.432	**Reserved**
256	2.048	4.096	6.144	8.192	12.288	24.576	**Reserved**
384	3.072	6.144	9.216	12.288	18.432	**Reserved**	**Reserved**
512	4.096	8.192	12.288	16.384	24.576	**Reserved**	**Reserved**

Table 6-5. Supported FSYNC (Multiples or Submultiples of 44.1 kHz) and BCLK Frequencies (IOVDD - 3.3V Operation)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)
16	**Reserved**	**Reserved**	0.3528	0.4704	0.7056	1.4112	2.8224
24	**Reserved**	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336
32	**Reserved**	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	16.9344
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	22.5792
192	1.4112	2.8224	4.2336	5.6448	8.4672	16.9344	**Reserved**
256	1.8816	3.7632	5.6448	7.5264	11.2896	22.5792	**Reserved**
384	2.8224	5.6448	8.4672	11.2896	16.9344	**Reserved**	**Reserved**
512	3.7632	7.5264	11.2896	15.0528	22.5792	**Reserved**	**Reserved**

Table 6-6. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies (IOVDD - 1.8V Operation)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)
16	**Reserved**	0.256	0.384	0.512	0.768	1.536	3.072
24	**Reserved**	0.384	0.576	0.768	1.152	2.304	4.608
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144

Table 6-6. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies (IOVDD - 1.8V Operation) (continued)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288
96	0.768	1.536	2.304	3.072	4.608	9.216	Reserved
128	1.024	2.048	3.072	4.096	6.144	12.288	Reserved
192	1.536	3.072	4.608	6.144	9.216	Reserved	**Reserved**
256	2.048	4.096	6.144	8.192	12.288	Reserved	**Reserved**
384	3.072	6.144	9.216	12.288	Reserved	**Reserved**	**Reserved**
512	4.096	8.192	12.288	Reserved	Reserved	**Reserved**	**Reserved**

Table 6-7. Supported FSYNC (Multiples or Submultiples of 44.1 kHz) and BCLK Frequencies (IOVDD - 1.8V Operation)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)
16	**Reserved**	**Reserved**	0.3528	0.4704	0.7056	1.4112	2.8224
24	**Reserved**	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336
32	**Reserved**	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	Reserved
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	Reserved
192	1.4112	2.8224	4.2336	5.6448	8.4672	Reserved	**Reserved**
256	1.8816	3.7632	5.6448	7.5264	11.2896	Reserved	**Reserved**
384	2.8224	5.6448	8.4672	11.2896	Reserved	**Reserved**	**Reserved**
512	3.7632	7.5264	11.2896	Reserved	Reserved	**Reserved**	**Reserved**

In the controller mode of operation, the device uses the MD3 pin, as the system clock, CCLK for the reference input clock source. In target mode of operation, the MD3 pin should be grounded.

The device provides flexibility in FSYNC selection with a supported system clock frequency option of either 256 × f_S or 128 × f_S or a fixed 48/44.1KSPS or 96/88.2KSPS as configured using the MD1 and MD2 pins.

The table Table 6-8 shows the FSYNC and BCLK selection for the controller mode using the MD1 and MD2 pins. In controller mode of operation, AVDD = 3.3V and Word-Length = 32.

Table 6-8. System Clock Selection for the Controller Mode

MD2	MD1	SYSTEM CLOCK SELECTION (Valid for Controller Mode only)		
		FSYNC	I^2S Mode	TDM Mode
Low	Low	FSYNC = CCLK/256	BCLK = 64*f_S	For FSYNC<=48KSPS, BCLK = 256*f_S, for 48KSPS<FSYNC<=96KSPS, BCLK = 128*f_S, and for FSYNC>96KSPS, BCLK = 64*f_S
Low	High	FSYNC = CCLK/128		
High	Low	FSYNC = 96/88.2KSPS		BCLK = 128*f_S
High	High	FSYNC = 48/44.1KSPS		BCLK = 256*f_S

See Table 6-2 for the MD1 and MD2 pin function in the target mode of operation.

6.3.4 Analog Output Configurations

The device supports playback of two channels using the high-performance stereo DAC. The device consists of two pairs of analog output pins (OUTxP and OUTxM) which can be configured in single-ended or differential input mode by setting MD4 and MD5 pins. The input source for these channels is from TDM/I^{2}S/LJ interface.

Table 6-9 shows the analog output configuration modes available with MD4 and MD5 pins.

Table 6-9. Analog Output Configurations

MD5	MD4	ANALOG OUTPUT CONFIGURATION
Low	Low	Differential Output; Line-out only
Low	High	Differential Output; Receiver/Headphone load or Line-out
High	Low	Single-ended output; Line-out only
High	High	Pseudo differential output with external common-mode sense; Headphone load only

Figure 6-8 to Figure 6-10 show the typical configuration diagrams for the various output modes.

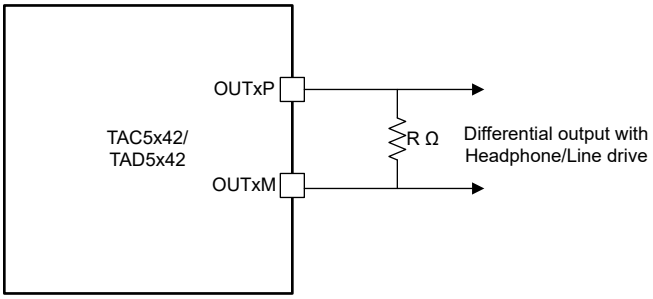


Figure 6-8. Typical Application Diagram for Differential Output Connection

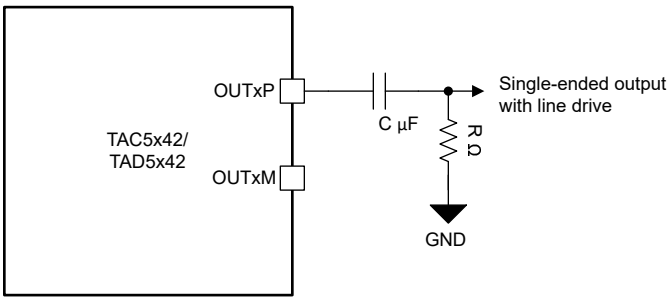


Figure 6-9. Typical Application Diagram for Single-ended Output Connection

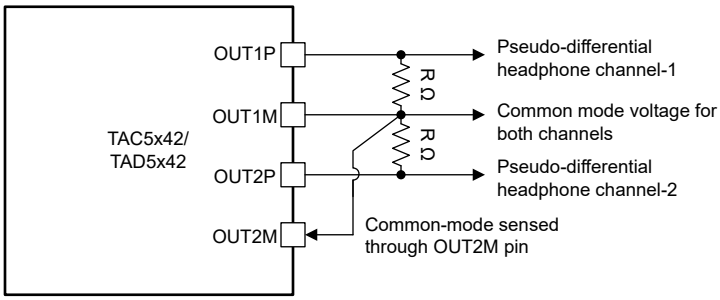


Figure 6-10. Typical Application Diagram for Pseudo-differential Output Connection with External Common-Mode Sense

The device also supports channel select configurations to enable mono or stereo outptut in I^{2}S and LJ Modes. This can be configured by setting MD6 pin. Table 6-10 shows the control for this feature with MD6 configuration.

DAC Channel-2 is disabled when MD6 pin is set to High. In TDM mode, MD6 pin function is as described in Figure 6-2.

Table 6-10. Output Channel Select configuration in I^2S and LJ Modes

MD6	ANALOG OUTPUT CONFIGURATION
Low	Stereo DAC
High	Mono 1-Channel DAC (OUT1x enabled, OUT2x disabled)

6.3.5 Reference Voltage

All audio data converters require a DC reference voltage. The TAD5242 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1µF capacitor connected from the VREF pin to the device ground (VSS). The value of this reference voltage, VREF, is set to 2.75V, which in turn supports a $2V_{RMS}$ differential full-scale output to the device. The required minimum AVDD voltage for this VREF voltage is 3V. When the device is configured for 1.8V AVDD supply voltage, the voltage on the VREF pin is 1.375V, which supports a $1V_{RMS}$ differential full-scale output to the device. Do not connect any external load to the VREF pin.

6.3.6 DAC Signal-Chain

Figure 6-11 shows the key components of the playback signal chain.

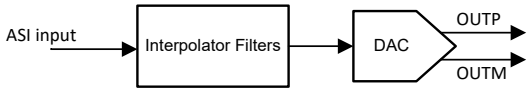


Figure 6-11. DAC Signal-Chain Processing Flowchart

The DAC signal chain offers a highly flexible low-noise playback path for low-noise and high-fidelity audio applications. This low-noise and low-distortion, multi-bit, delta-sigma DAC enables the TAD5242 to achieve a high dynamic range in very low power. Moreover, the DAC architecture has inherent anti-alias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band. The TAD5242 also integrates, high-performance multi-stage digital interpolation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

6.3.6.1 Digital Interpolation Filters

The device playback channel includes a high dynamic range, built-in digital interpolation filter to process the input data stream to generate digital data stream for multibit delta-sigma (ΔΣ) modulator. The interpolation filters in the device can be selected to linear phase or low-latency filters based on the state of the MD2 and MD1 pins according to Table 6-3. This makes them suitable for a wide variety of audio applications. Following section describes the filter response for different samples rates.

6.3.6.1.1 Linear-phase filters

The linear-phase interpolation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

6.3.6.1.1.1 Sampling Rate: 8kHz or 7.35kHz

Figure 6-12 and Figure 6-13 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 8kHz or 7.35kHz, and Table 6-11 lists its specifications.

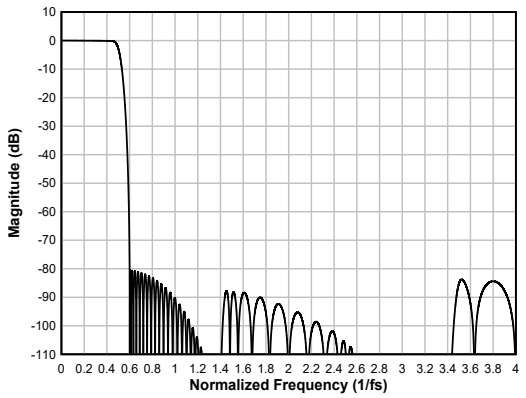


Figure 6-12. Linear-phase Interpolation Filter Magnitude Response

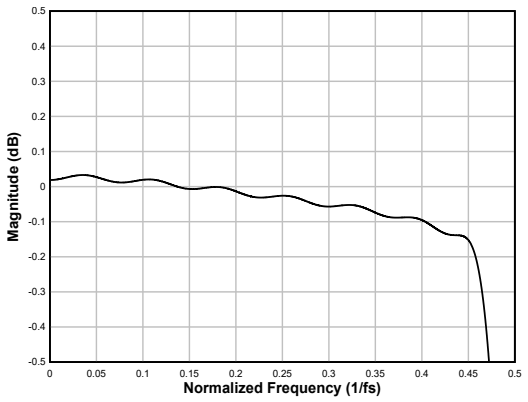


Figure 6-13. Linear-phase Interpolation Filter Pass-Band Ripple

Table 6-11. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.17		0.03	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.4			dB
	Frequency range is 4 × f_S to 7.431 × f_S	86.9			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		16		1/f_S

6.3.6.1.1.2 Sampling Rate: 16kHz or 14.7kHz

Figure 6-14 and Figure 6-15 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 16kHz or 14.7kHz, and Table 6-12 lists its specifications.

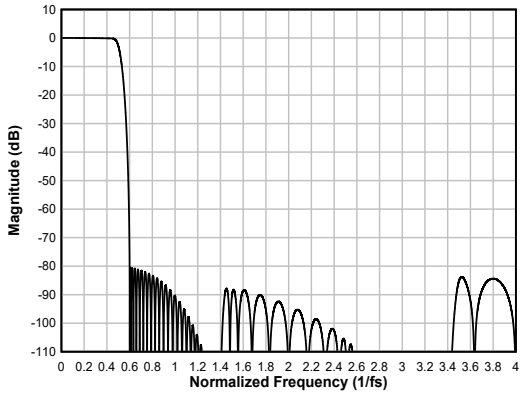


Figure 6-14. Linear-phase Interpolation Filter Magnitude Response

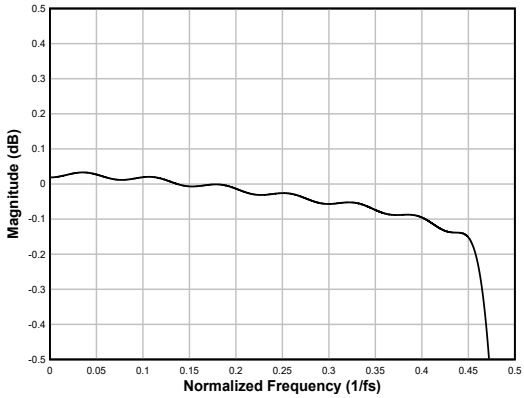


Figure 6-15. Linear-phase Interpolation Filter Pass-Band Ripple

Table 6-12. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.17		0.03	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.4			dB
	Frequency range is 4 × f_S to 7.431 × f_S	86.9			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		16		$1/f_S$

6.3.6.1.1.3 Sampling Rate: 24kHz or 22.05kHz

Figure 6-16 and Figure 6-17 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 24kHz or 22.05kHz, and Table 6-13 lists its specifications.

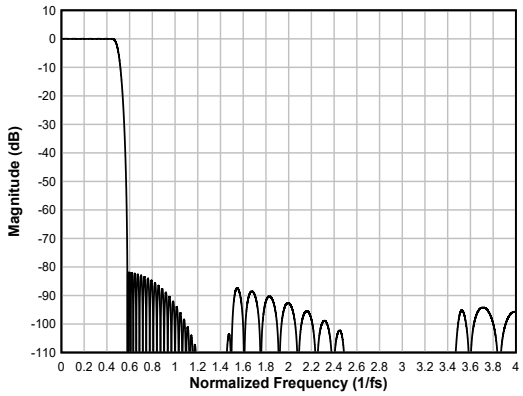


Figure 6-16. Linear-phase Interpolation Filter Magnitude Response

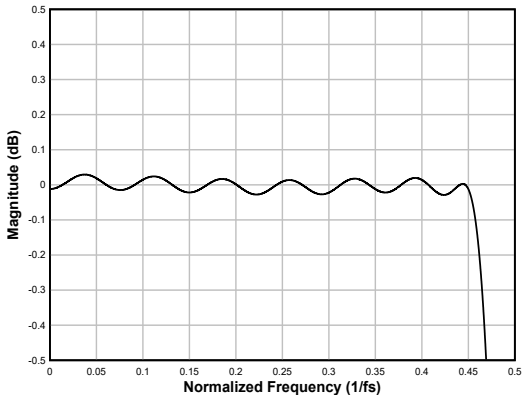


Figure 6-17. Linear-phase Interpolation Filter Pass-Band Ripple

Table 6-13. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.05		0.03	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	81.9			dB
	Frequency range is 4 × f_S to 8 × f_S	87.7			

Table 6-13. Linear-phase Interpolation Filter Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Group delay or latency	Frequency range is 0 to 0.455 × f_S		17.6		$1/f_S$

6.3.6.1.1.4 Sampling Rate: 32kHz or 29.4kHz

Figure 6-18 and Figure 6-19 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 32kHz or 29.4kHz, and Table 6-14 lists its specifications.

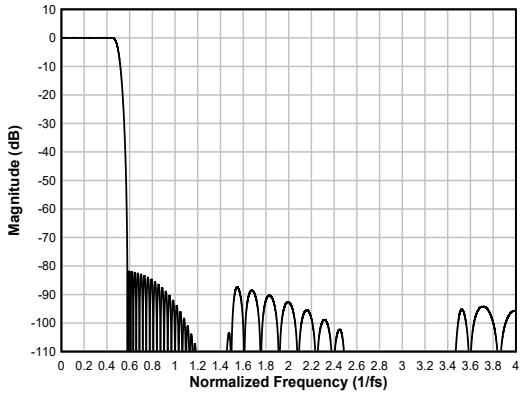


Figure 6-18. Linear-phase Interpolation Filter Magnitude Response

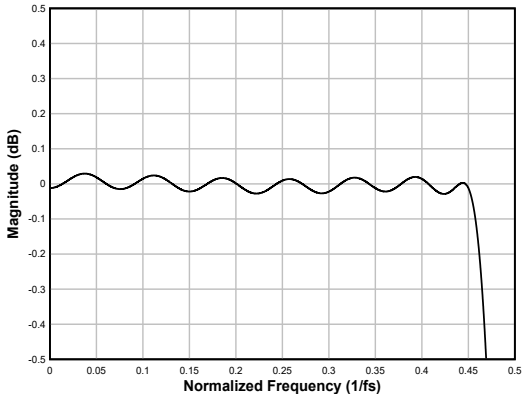


Figure 6-19. Linear-phase Interpolation Filter Pass-Band Ripple

Table 6-14. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.05		0.03	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	81.9			dB
	Frequency range is 4 × f_S to 8 × f_S	87.6			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		17.6		$1/f_S$

6.3.6.1.1.5 Sampling Rate: 48kHz or 44.1kHz

Figure 6-20 and Figure 6-21 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 48kHz or 44.1kHz, and Table 6-15 lists its specifications.

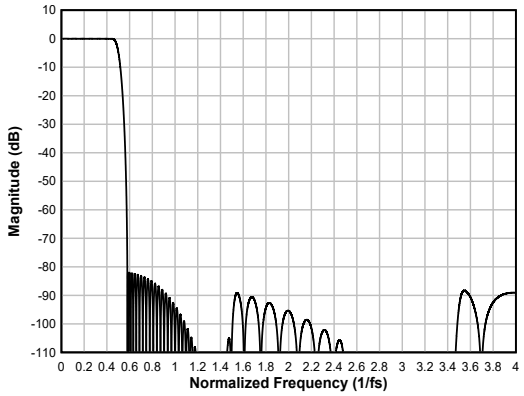


Figure 6-20. Linear-phase Interpolation Filter Magnitude Response

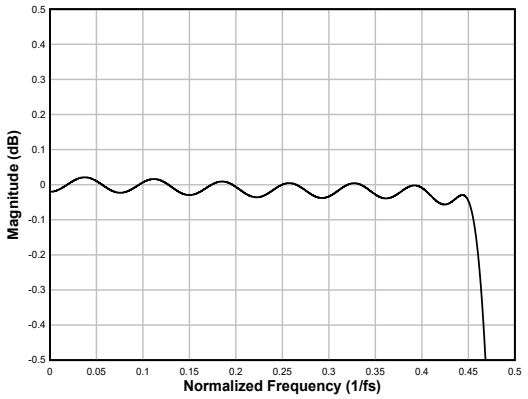


Figure 6-21. Linear-phase Interpolation Filter Pass-Band Ripple

Table 6-15. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.09		0.02	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	82			dB
	Frequency range is 4 × f_S to 7.423 × f_S	89.1			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		17.3		1/f_S

6.3.6.1.1.6 Sampling Rate: 96kHz or 88.2kHz

Figure 6-22 and Figure 6-23 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 96kHz or 88.2kHz, and Table 6-16 lists its specifications.

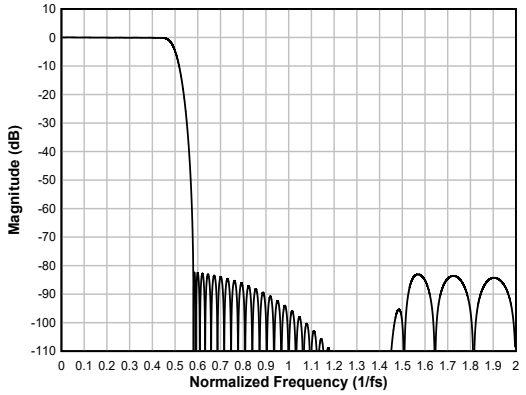


Figure 6-22. Linear-phase Interpolation Filter Magnitude Response

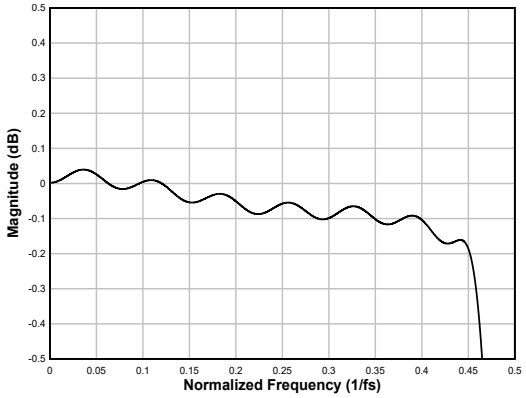


Figure 6-23. Linear-phase Interpolation Filter Pass-Band Ripple

Table 6-16. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.23		0.04	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 2 × f_S	82.4			dB
	Frequency range is 2 × f_S to 3.422 × f_S	85.1			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		16.7		1/f_S

6.3.6.1.1.7 Sampling Rate: 192kHz or 176.4kHz

Figure 6-24 and Figure 6-25 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 192kHz or 176.4kHz, and Table 6-17 lists its specifications.

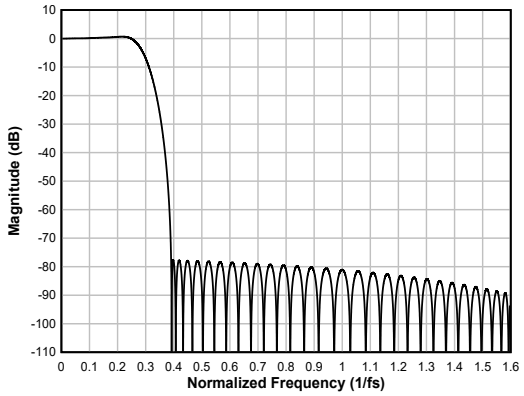


Figure 6-24. Linear-phase Interpolation Filter Magnitude Response

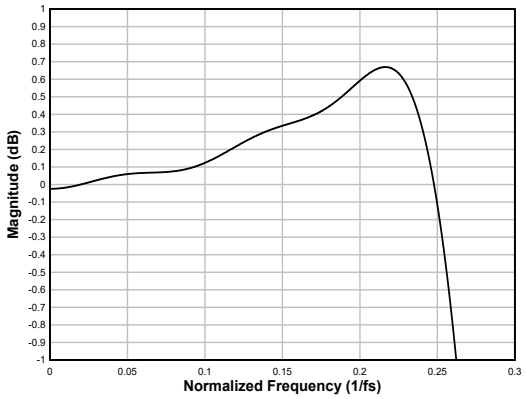


Figure 6-25. Linear-phase Interpolation Filter Pass-Band Ripple

Table 6-17. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.258 × f_S	–0.67		0.67	dB
Stop-band attenuation	Frequency range is 0.391 × f_S to 1 × f_S	77.7			dB
	Frequency range is 1 × f_S to 1.612 × f_S	81.1			
Group delay or latency	Frequency range is 0 to 0.258 × f_S		10.7		$1/f_S$

6.3.6.1.2 Low-latency Filters

For applications where low latency with minimal phase deviation (within the audio band) is critical, the low-latency interpolation filters on the TAD5242 can be used. The device supports these filters with a group delay of approximately seven samples with an almost linear phase response within the 0.376 × f_S frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the low-latency filters.

6.3.6.1.2.1 Sampling Rate: 24kHz or 22.05kHz

Figure 6-26 shows the magnitude response and Figure 6-27 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 24kHz or 22.05kHz. Table 6-18 lists its specifications.

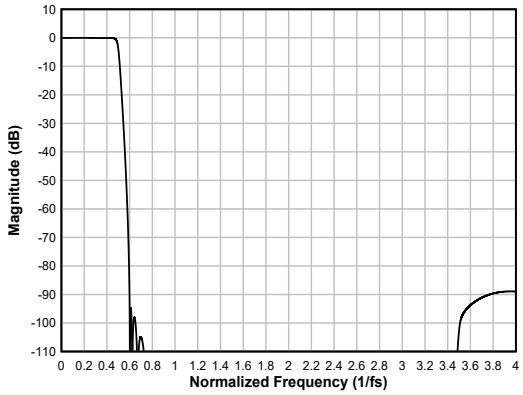


Figure 6-26. Low-latency Interpolation Filter Magnitude Response

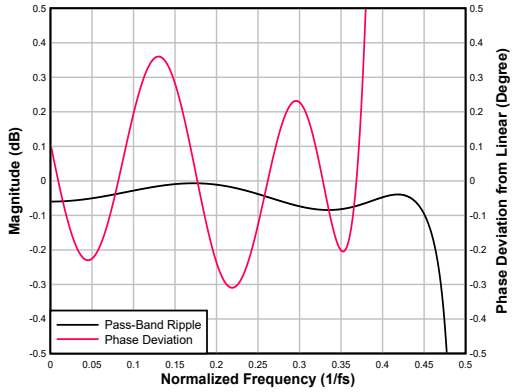


Figure 6-27. Low-latency Interpolation Filter Pass-Band Ripple and Phase Deviation

Table 6-18. Low-latency Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.12		–0.01	dB
Stop-band attenuation	Frequency range is 0.599 × f_S to 4 × f_S	88.9			dB
	Frequency range is 4 × f_S to 7.414 × f_S	89			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		7.19		1/f_S
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.088		0.088	1/f_S
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.31		0.36	Degrees

6.3.6.1.2.2 Sampling Rate: 32kHz or 29.4kHz

Figure 6-28 shows the magnitude response and Figure 6-29 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 32kHz or 29.4kHz. Table 6-19 lists its specifications.

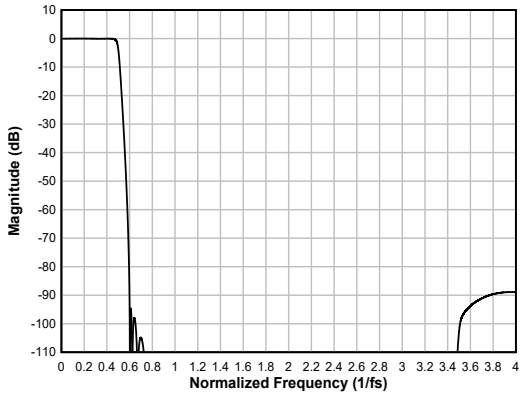


Figure 6-28. Low-latency Interpolation Filter Magnitude Response

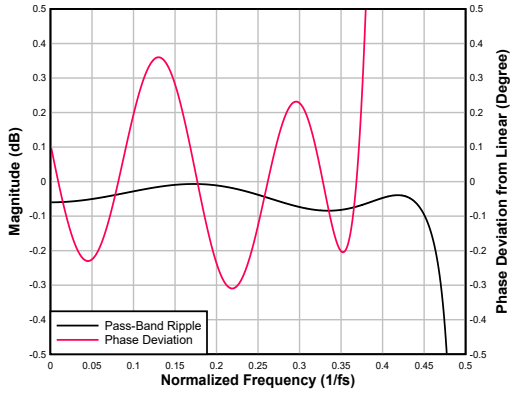


Figure 6-29. Low-latency Interpolation Filter Pass-Band Ripple and Phase Deviation

Table 6-19. Low-latency Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.12		–0.01	dB
Stop-band attenuation	Frequency range is 0.599 × f_S to 4 × f_S	88.9			dB
	Frequency range is 4 × f_S to 7.414 × f_S	89			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		7.19		1/f_S
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.088		0.088	1/f_S
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.31		0.36	Degrees

6.3.6.1.2.3 Sampling Rate: 48kHz or 44.1kHz

Figure 6-30 shows the magnitude response and Figure 6-31 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 48kHz or 44.1kHz. Table 6-20 lists its specifications.

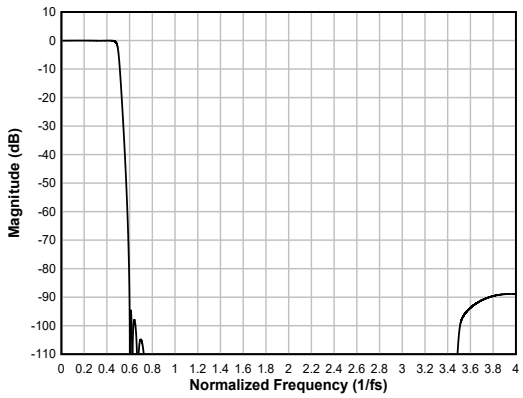


Figure 6-30. Low-latency Interpolation Filter Magnitude Response

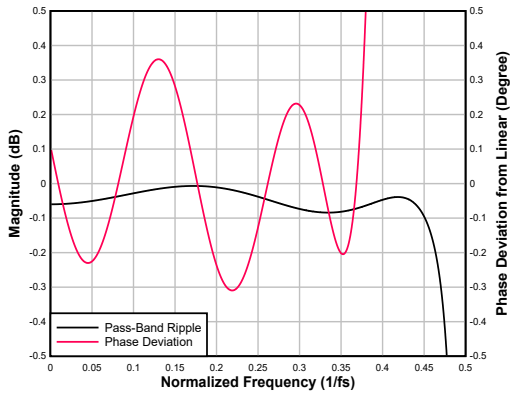


Figure 6-31. Low-latency Interpolation Filter Pass-Band Ripple and Phase Deviation

Table 6-20. Low-latency Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.12		–0.01	dB
Stop-band attenuation	Frequency range is 0.599 × f_S to 4 × f_S	88.9			dB
	Frequency range is 4 × f_S to 7.414 × f_S	89			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		7.19		1/f_S
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.088		0.088	1/f_S

Table 6-20. Low-latency Interpolation Filter Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.31		0.36	Degrees

6.3.6.1.2.4 Sampling Rate: 96kHz or 88.2kHz

Figure 6-32 shows the magnitude response and Figure 6-33 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 96kHz or 88.2kHz. Table 6-21 lists its specifications.

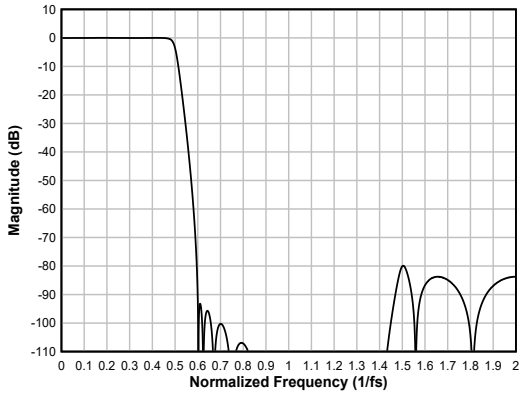


Figure 6-32. Low-latency Interpolation Filter Magnitude Response

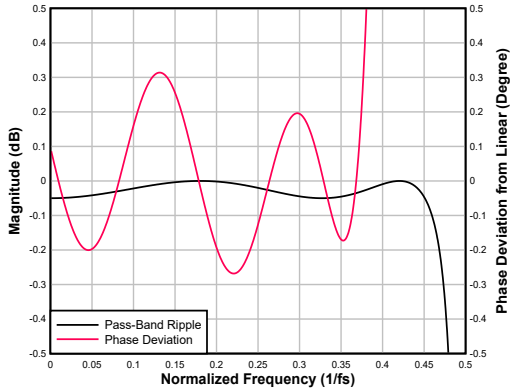


Figure 6-33. Low-latency Interpolation Filter Pass-Band Ripple and Phase Deviation

Table 6-21. Low-latency Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.456 × f_S	–0.07		0	dB
Stop-band attenuation	Frequency range is 0.595 × f_S to 2 × f_S	79.9			dB
	Frequency range is 2 × f_S to 3.405 × f_S	79.9			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		6.39		1/f_S
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.078		0.022	1/f_S
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.268		0.022	Degrees

6.3.6.1.2.5 Sampling Rate: 192kHz or 176.4kHz

Figure 6-34 shows the magnitude response and Figure 6-35 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 192kHz or 176.4kHz. Table 6-22 lists its specifications.

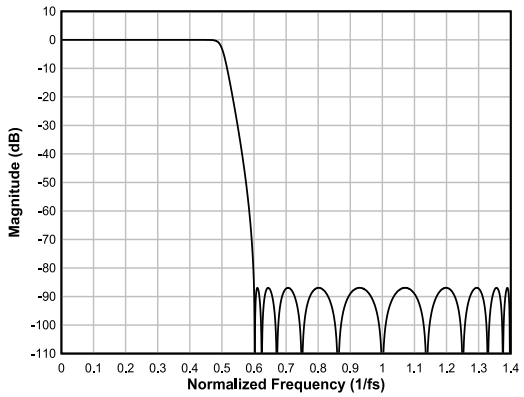


Figure 6-34. Low-latency Interpolation Filter Magnitude Response

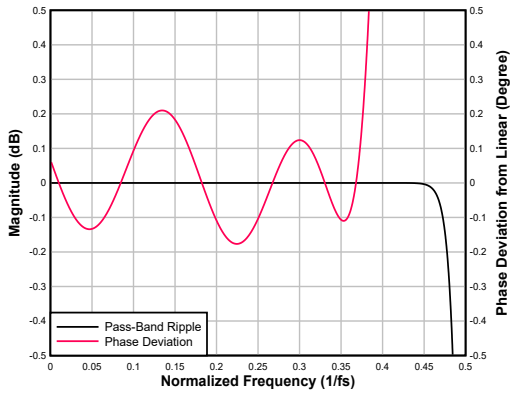


Figure 6-35. Low-latency Interpolation Filter Pass-Band Ripple and Phase Deviation

Table 6-22. Low-latency Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.452 × f_S	–0.005		0	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 1 × f_S	86.9			dB
	Frequency range is 1 × f_S to 1.401 × f_S	86.9			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		5.41		1/f_S
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.055		0.055	1/f_S
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.177		0.21	Degrees

6.4 Device Functional Modes

6.4.1 Active Mode

The device wakes up in active mode when AVDD and IOVDD are available. MD0 pin sets the type of audio serial interface and should be configured along with the supplies. Further, configure all other hardware control mode pins (MD1, MD2, MD3, MD4,MD5 and MD6) for the desired mode of operation before enabling the clocks for the device.

In active mode, when the audio clocks are available, the device automatically powers up the DAC channels and starts transmitting and playing data over the audio serial interface as per the configurations. If the clocks are stopped, then the device auto powers down the DAC channels.

Stopping the clocks or clock-error triggers an interrupt on the GPO pin. This is a latched interrupt that can be cleared by power-cycling the device supplies.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TAD5242 is a pin or hardware controlled stereo, high-performance audio DAC that supports sample rates of up to 192kHz. The device can be configured by controlling the Mode pins MD0 to MD6 and can support 1.8V or 3.3V AVDD analog power supply along with flexible digital audio serial interfaces of I²S/TDM/LJ. The device also supports various output configurations like 2-channel differential, single-ended or psuedo-differential with external common-mode sense outputs with options for headphone and line-out drive capabilities.

7.2 Typical Application

7.2.1 Application

Figure 7-1 shows a typical configuration of the TAD5242 for an application using a 2-channel differential line-out operation with a Target Mode I²S audio serial data interface.

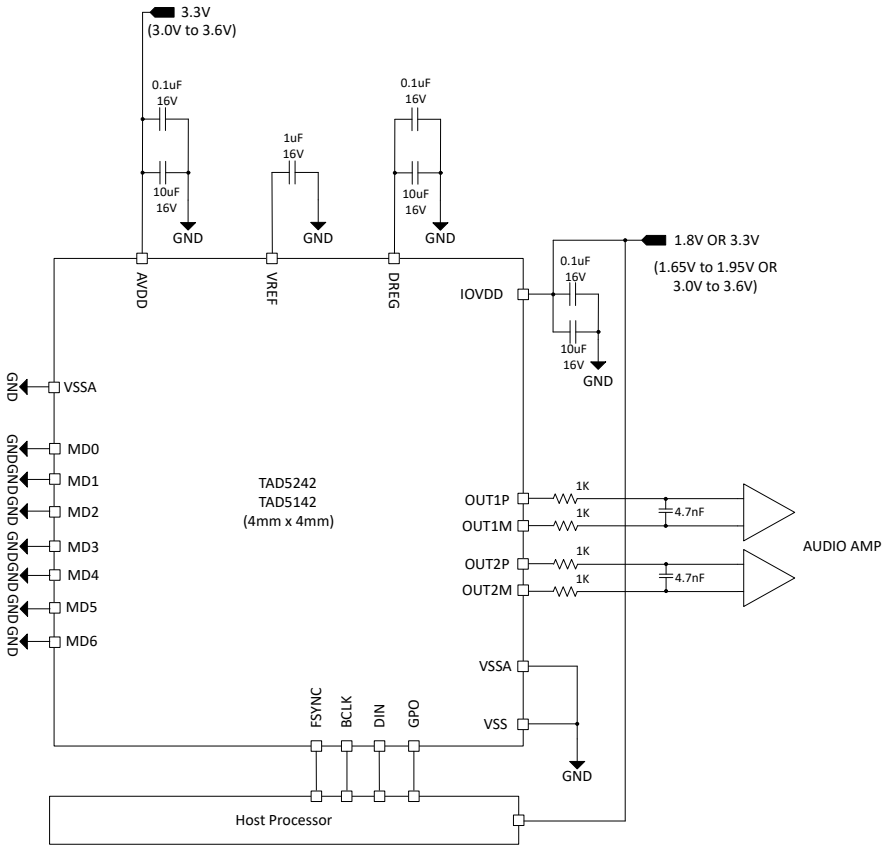


Figure 7-1. Stereo Differential Line-out in Target I²S Mode, Block Diagram

7.2.2 Design Requirements

Table 7-1 lists the typical design parameters for this application.

Table 7-1. Design Parameters

PARAMETER	VALUE
AVDD	1.8V or 3.3V
IOVDD	1.8V or 3.3V
AVDD supply current consumption	17mA, with AVDD = 3.3V
IOVDD supply current consumption	0.06mA, with IOVDD = 3.3V
Load on OUT1M, OUT1P, OUT2M, OUT2P	>600 ohms

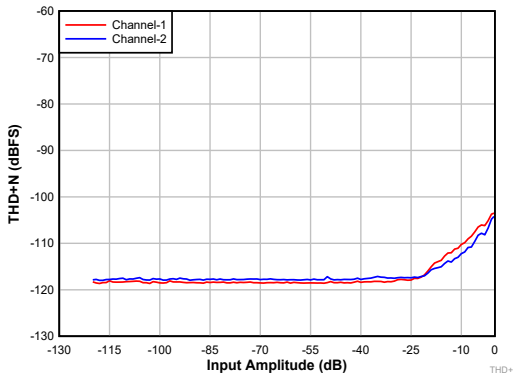
7.2.3 Detailed Design Procedure

This section describes the necessary steps to configure the TAD5242 for this specific application.

1. Audio serial interface (ASI) Mode is configured based on the MD0 pin setting which needs to be provided along with the power-supplies. Configure MD0 to be either pulled up to AVDD or down to VSS with appropriate resistor value. MD0 is configured to be grounded for this use case.
2. Apply power to the device:
   a. Power up the IOVDD and AVDD power supplies.
   b. Ensure that MD0 pin setting is stable as soon as power supplies are up and wait for at least 2ms to allow the device to initialize the internal registers for this mode of operation.
   c. The device now is in sleep mode (low-power mode <1mA).
3. Configure the Mode pins MD1 to MD6 as per the system requirements:
   a. Pull up to IOVDD or pull down to VSS on MD1 to MD6 pins as per the required configuration. All the pins are grounded for this use case.
4. Apply the ASI Clocks (BCLK and FSYNC) to wake up the device.
5. To put the device back in sleep mode, stop the clocks:
   a. Wait at least 100ms to allow the device to complete the shutdown sequence.
   b. Change the device mode configurations by changing MD1 to MD6 as per requirement.
6. To change the ASI mode, re-configure MD0 pin and power-cycle the device.
7. Repeat steps 1-6 as required for mode transitions.

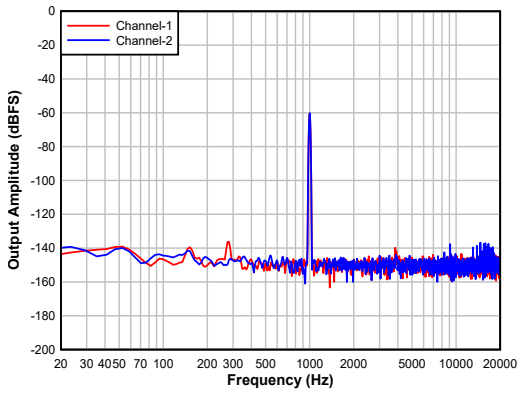
7.2.4 Application Performance Plots

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256×f_S, TDM target mode, and linear phase interpolation filter, with 1200Ω line-out load in differential configuration; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted



Differential output

Figure 7-2. DAC THD+N Level vs Input



Differential output, -60dBFS input

Figure 7-3. DAC FFT

7.3 Power Supply Recommendations

The power supply sequence between the IOVDD and AVDD rails can be applied in any order. MD0 pin should be provided along with the power supplies and should be stable as soon as the supplies are settled to the recommended operating voltage levels. Only initiate the clocks to initialize the device after all the other Mode pins (MD1 to MD6) are also stable.

For the supply power-up requirement, t_1, t_2 and t_3 must be at least 2ms to allow the device to initialize the internal registers. See the *Section 6.3.1* section for details on how the device operates in various modes after the device power supplies are settled to the recommended operating voltage levels. For the supply power-down requirement, t_4, t_5 and t_6 must be at least 10ms. This timing (as shown in the *Figure 7-4*) allows the device to ramp down the volume on the playback data, power down the analog and digital blocks, and put the device into a low power mode.

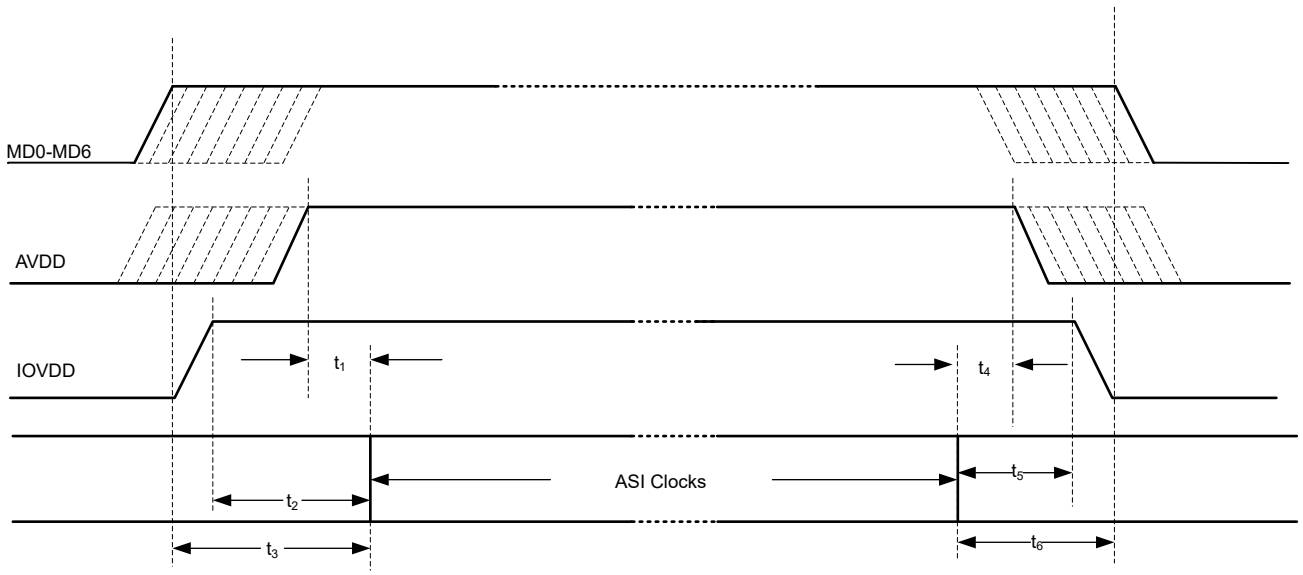


Figure 7-4. Power Supply Sequencing Requirement Timing Diagram

Make sure that the supply ramp rate is slower than 0.1V/µs and that the wait time between a power-down and a power-up event is at least 100ms.

The TAD5242 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG and integrated internal analog regulator.

7.4 Layout

7.4.1 Layout Guidelines

Each system design and printed circuit board (PCB) layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the device performance:

- Connect the thermal pad to ground. Use a via pattern to connect the device thermal pad, which is the area directly under the device, to the ground planes. This connection helps dissipate heat from the device.
- Use the same ground between VSS and VSSA to avoid any potential voltage difference between them.
- The decoupling capacitors for the power supplies must be placed close to the device pins.
- Route the analog differential audio signals differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to prevent undesirable crosstalk.
- Avoid running high-frequency clock and control signals near OUTxx pins where possible.
- The device internal voltage references must be filtered using external capacitors. Place the filter capacitors near the VREF pin for good performance.
- Provide a direct connection from the VREF external capacitor ground terminal to the VSS pin.

- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. Treat the area directly under the device as a central ground area for the device, and all device grounds must be connected directly to that area.

7.4.2 Layout Example

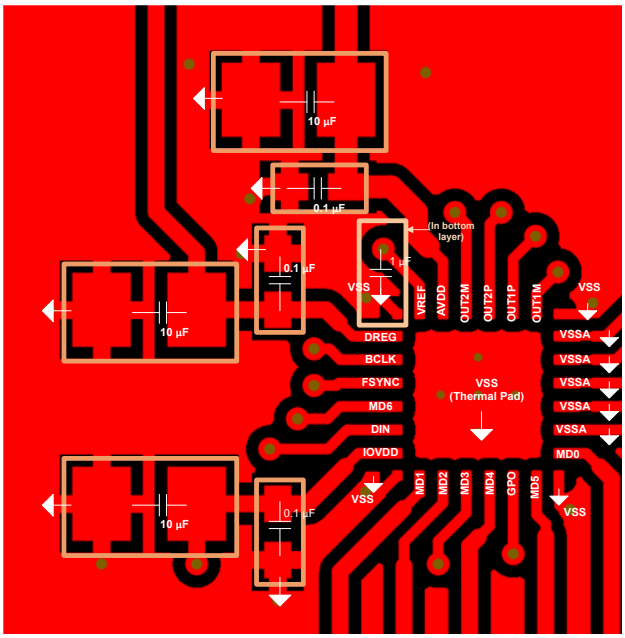


Figure 7-5. Example Layout

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TAx5x42EVM-K Hardware Control Evaluation Module* User's Guide

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2024) to Revision A (October 2024)	Page
• Updated device status to production data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAD5242IRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TAD5242	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

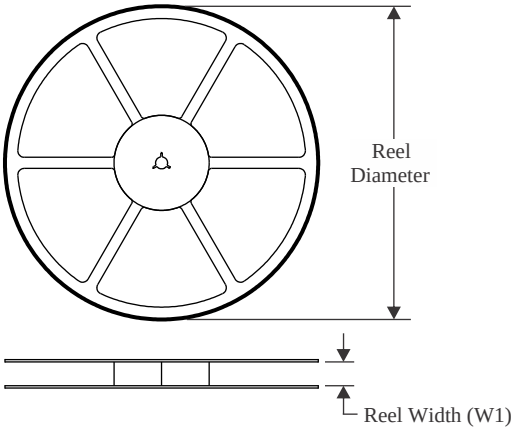
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

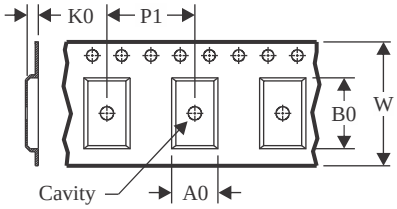
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

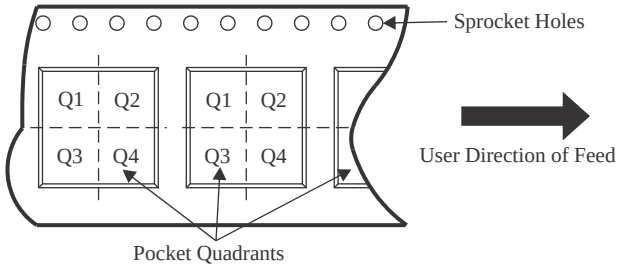


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

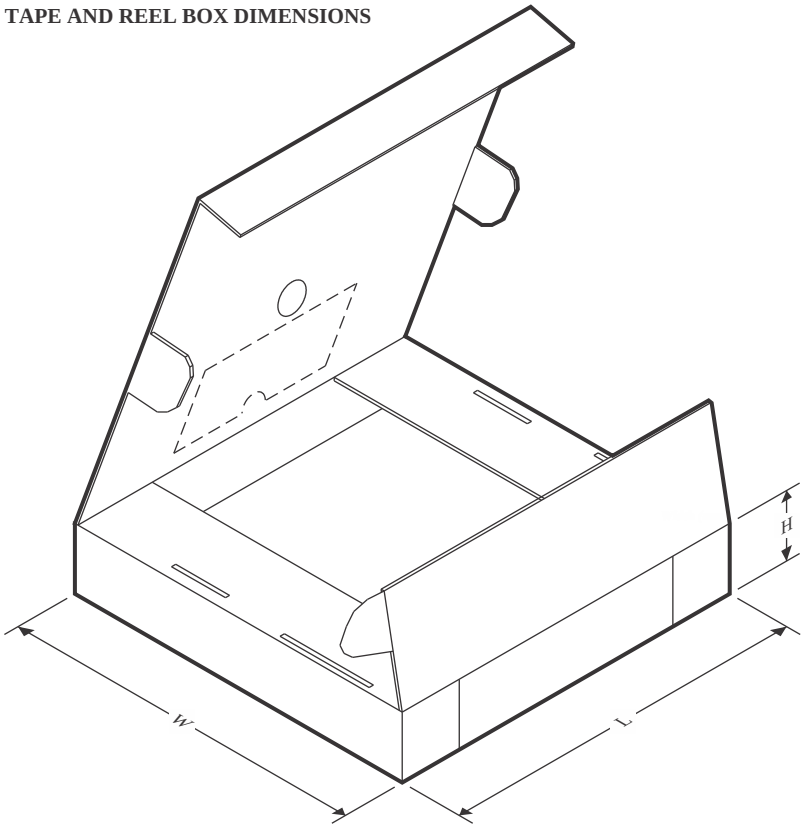
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAD5242IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



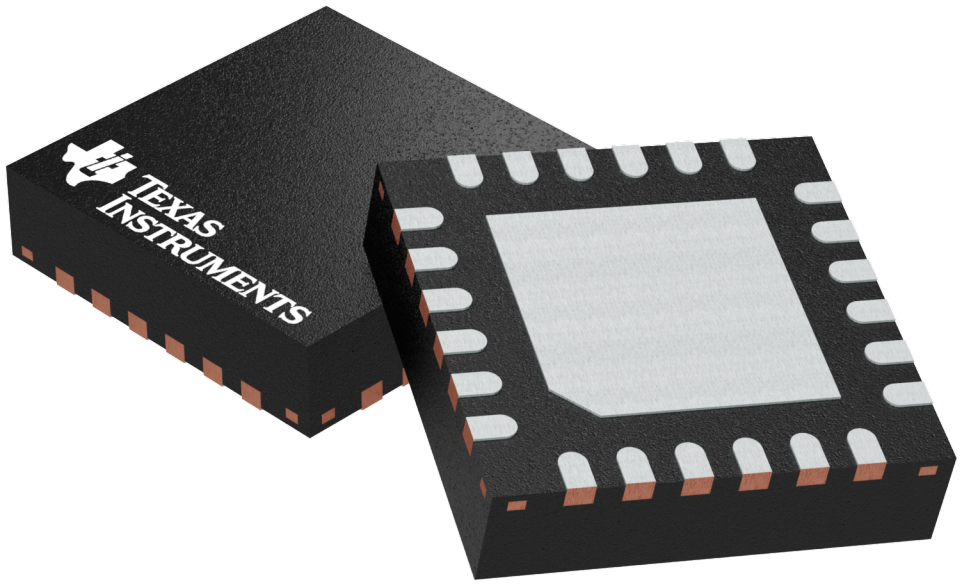
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAD5242IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

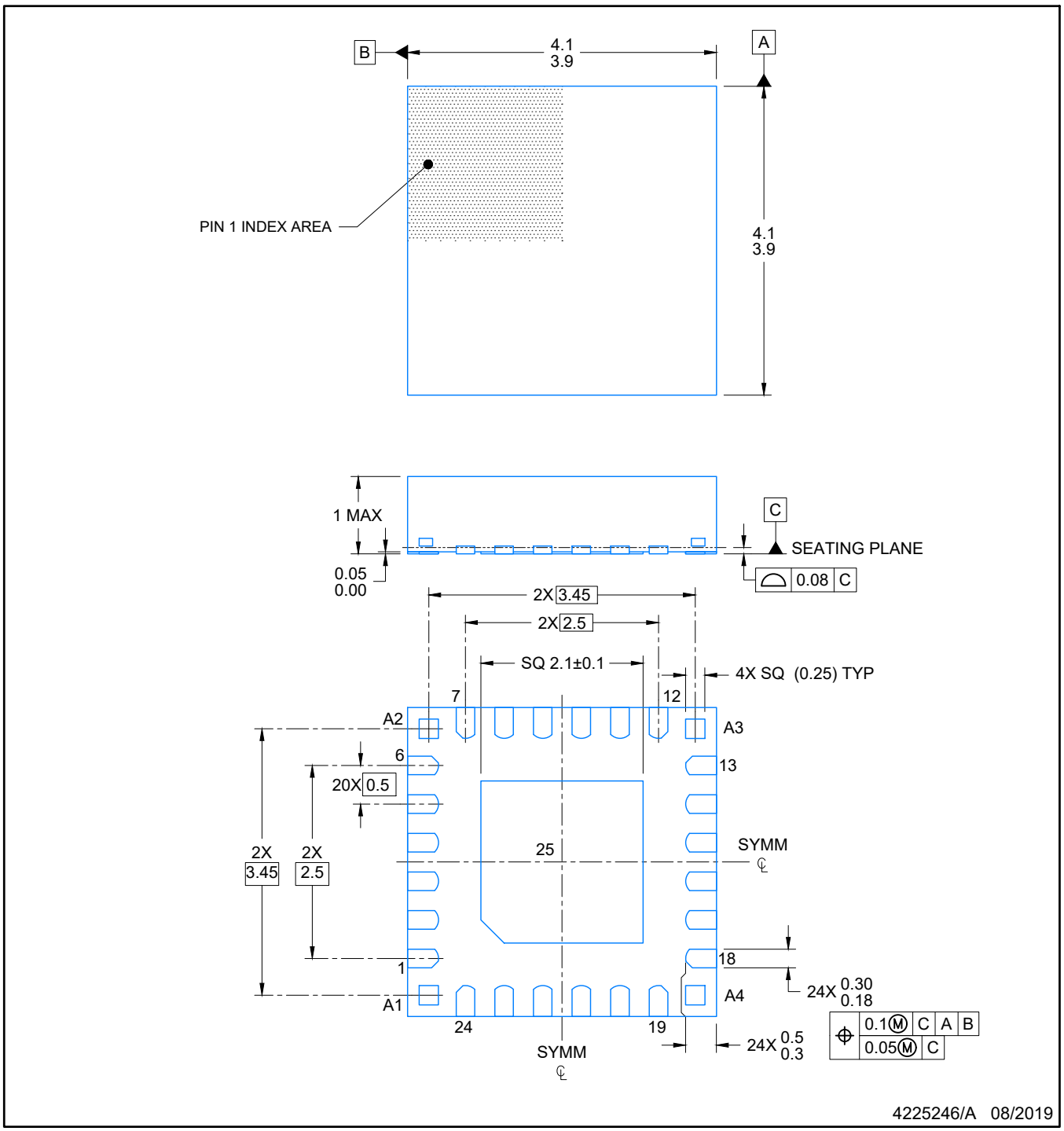
4204104/H

PACKAGE OUTLINE

RGE0024R

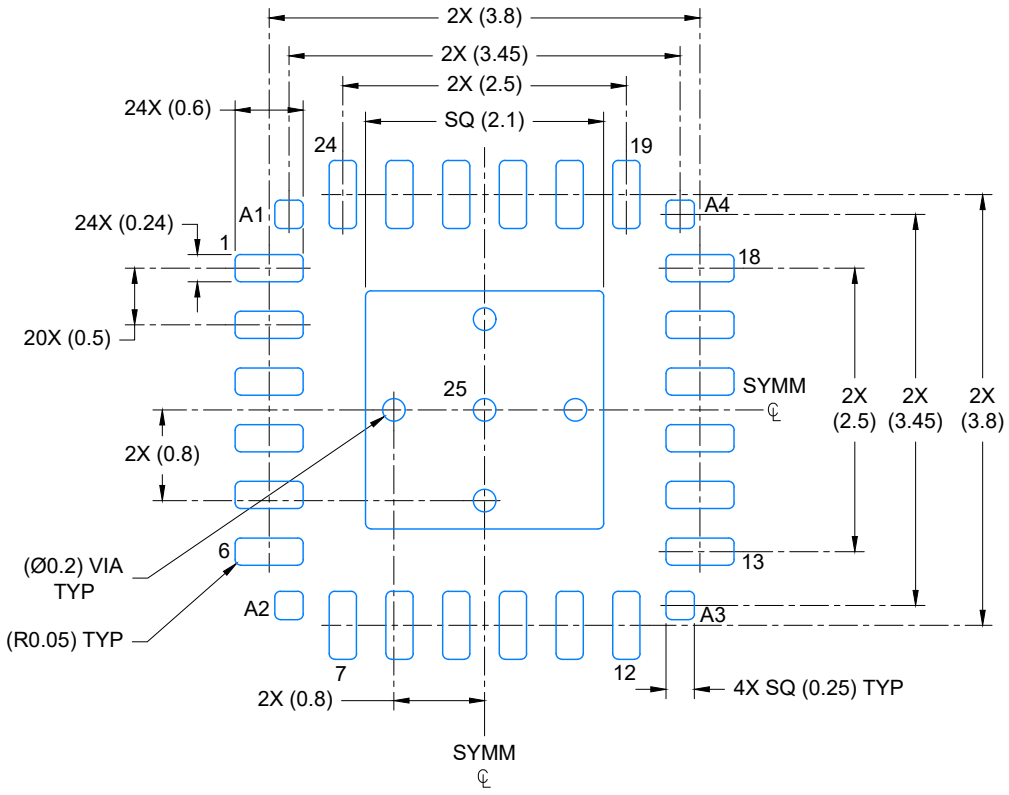
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

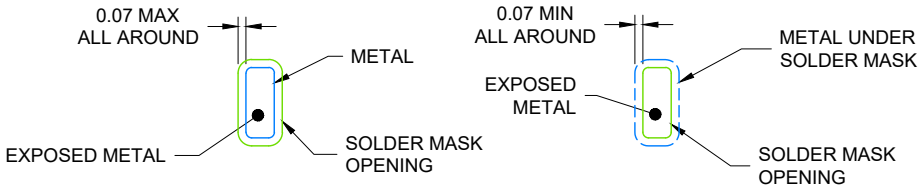


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

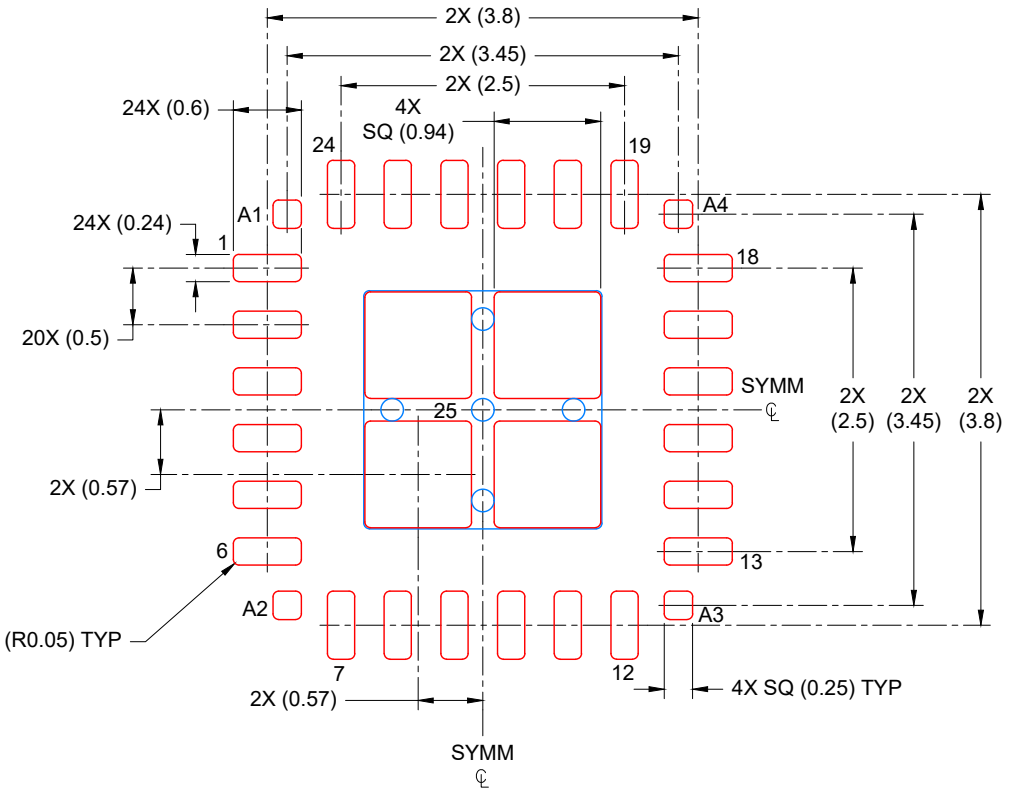
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4225246/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 15X

4225246/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265