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TEXAS INSTRUMENTS

TAS2320 15W Mono Digital Input Class-D Speaker Amp with 15V Support

1 Features

- Powerful Class-D amplifier
  - 15W 1% THD+N
  - 15V external PVDD supply
- Best in class efficiency
  - Upto 89% efficiency at system level for 8Ω load
  - 14.2mW idle channel power, noise gate off
  - 5mW idle channel power, noise gate on
  - Integrated 1.8V Y-bridge
- High performance audio channel
  - 17.2µV A-wt. idle channel noise
  - 109dB Dynamic Range
  - -89dB THD+N
  - Low EMI performance with ERC and SSM
  - < 1µs chip to chip group delay matching
- Advanced integrated features
  - Signal detection high efficiency modes
  - High accuracy voltage monitor & temp sensor
- Ease of use features
  - Hardware pin control or I^2C control
  - External PVDD supply
  - Clock based power up/down
  - Auto clock rate detection: 16 to 192kHz
  - MCLK free operation
  - Thermal and over current protection
- Power Supplies and user interface
  - VBAT: 2.5V to 5.5V
  - VDD: 1.65V to 1.95V
  - IOVDD: 1.8V or 3.3V
  - PVDD: 2.5V to 15V
  - I^2S/TDM: 8 channels
  - HW pin control or I^2C based control
- 26-Pin, 0.4mm Pitch, QFN package

2 Applications

- Smart Speakers with Voice Assistance
- Bluetooth and Wireless speakers
- Tablets, Wearables
- Laptop, Desktop Computers

3 Description

The TAS2320 is a mono, digital input Class-D audio amplifier designed for efficiently driving high peak power into loudspeakers.

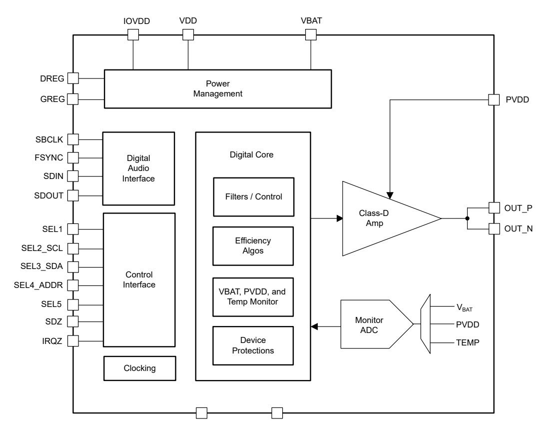
Device is optimized to deliver best battery life for real-use cases of music playback and voice calls. Advanced efficiency optimization features like Y-bridge, and algorithms enable the device to produce best-in-class efficiency across all power regions of operation. The Class-D amplifier is capable of delivering 15W output power using external PVDD supply.

Up to four devices can share a common bus via I^2S/TDM + I^2C interfaces. The device also supports five HW Control pins that can configure the device for the desired mode of operation.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (2)
TAS2320	QFN	4mm × 3.5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional block diagram

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4 Pin Configuration and Functions

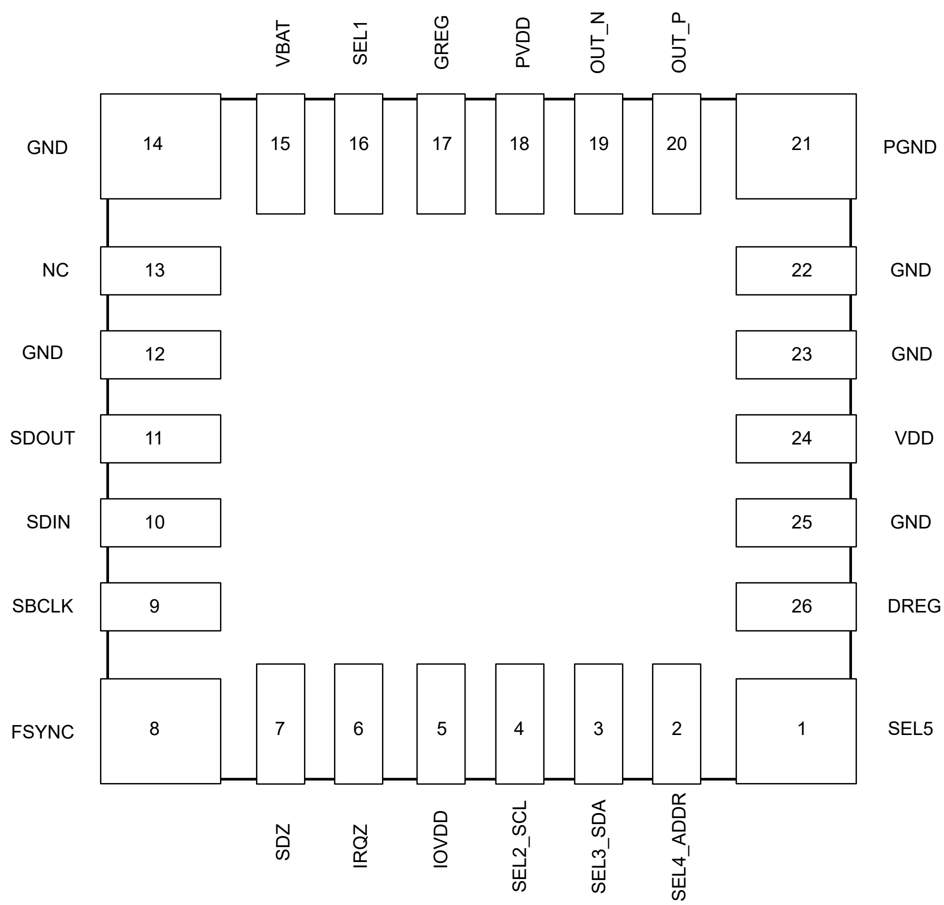

Figure 4-1. QFN Package Bottom View

Pin Functions

PIN NAME	PIN NO.	Type(1)	DESCRIPTION
DREG	26	P	Digital core voltage regulator output. Bypass to GND with a capacitor. Do not connect to an external load.
FSYNC	8	I	I^2S word clock or TDM frame sync.
GREG	17	P	High-side gate CP regulator output. Do not connect to an external load.
GND	12, 14, 22, 23, 25	P	Connect to PCB GND plane. Strong connection to ground plane required through multiple vias.
IOVDD	5	P	1.8V or 3.3V Digital IO supply. Decouple to GND with capacitor.
IRQZ	6	O	Open drain, active low interrupt pin. Pull up to IOVDD with resistor if optional internal pullup is not used.
NC	13	-	No connect. Keep floating.
OUT_N	19	O	Class-D negative output.
OUT_P	20	O	Class-D positive output.
PGND	21	P	Class-D Power stage ground. Connect to PCB GND plane strongly through multiple vias.
PVDD	18	P	Class-D power stage supply.
SBCLK	9	I	I^2S/TDM serial bit clock.
SDIN	10	I	I^2S or TDM serial data input.
SDOUT	11	I/O	I^2S or TDM serial data output.
SDZ	7	I	Active low hardware shutdown.
SEL1	16	I	HW Mode: Select 1 Pin. Amplifier gain level selection with volume ramp enable and disable options. I^2C Mode: Short to GND for I^2C mode selection.
SEL2_SCL	4	I	HW Mode: Select 2 Pin. I^2S, TDM, Left justified selection. I^2C Mode: Clock Pin. Pull up to IOVDD with a resistor.
SEL3_SDA	3	I/O	HW Mode: Select 3 Pin. Data valid rising edge and falling edge selection. I^2C Mode: Data Pin. Pull up to IOVDD with a resistor.
SEL4_ADDR	2	I	HW Mode: Select 4 Pin.Y-bridge threshold configuration setting. I^2C Mode: I^2C address pin.
SEL5	1	I/O	HW Mode: Connect to IOVDD for external PVDD selection.
VBAT	15	P	Battery power supply input. Connect to a 2.5 to 5.5V supply and decouple with a capacitor.
VDD	24	P	Connect to 1.8V supply and decouple to GND with capacitor.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply Voltage	PVDD	–0.3	19	V
Supply Voltage	VBAT	–0.3	6	V
Supply Voltage	VDD	–0.3	2	V
Supply Voltage	IOVDD	–0.3	6	V
Class-D Output	OUTP, OUTM	–0.7	19	V
High Side Drive Regulator	GREG	–0.3	PVDD + 6	V
Digital Supply Regulator	DREG	–0.3	1.65	V
Digital IO Pins	Digital pins referenced to IOVDD supply	–0.3	6	V
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{PVDD}	Amplifier Supply (External PVDD Mode)	V_{BAT}	12	15	V
V_{VDD}	Supply Voltage	1.65	1.8	1.95	V
V_{IOVDD}	IO Supply Voltage 1.8V	1.62	1.8	1.98	V
V_{IOVDD}	IO Supply Voltage 3.3V	3.0	3.3	3.6	V
R_{SPK}	Speaker resistance	3.2	8	38.4	Ω
L_{SPK}	Speaker inductance	5	33	100	μH
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		150	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		Standard JEDEC[(2)] HR-QFN 26 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.2	°C/W

5.4 Thermal Information (continued)

THERMAL METRIC[1]		Standard JEDEC[2] HR-QFN 26 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) JEDEC Standard 4 Layer PCB

5.5 Electrical Characteristics

TA = 25 °C, VBAT = 3.6 V, PVDD = 12 V (External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V, RL = 8Ω + 33μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, SDZ = 1, Noise gate disabled, Measured filter free with an Audio Precision using 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AMPLIFIER PERFORMANCE - EXTERNAL PVDD Mode						
$P_{OUT\_EXT\_PVDD}$	Maximum Continuous Output Power - 1% THDN	R_L = 8 Ω + 33 μH		8.3		W
		R_L = 4 Ω + 33 μH		14.9		W
$P_{OUT\_EXT\_PVDD}$	Maximum Continuous Output Power - 1% THDN	R_L = 8 Ω + 33 μH, HW pin control mode		8.3		W
$P_{OUT\_EXT\_PVDD}$	Maximum Continuous Output Power - 10% THDN	RL = 8 Ω + 33 μH		10.3		W
		RL = 4 Ω + 33 μH		18.4		W
		RL = 4 Ω + 33 μH, PVDD=14V		24.5		W
$\eta_{SYSTEM\_EXT\_0.5W}$	System Efficiency at P_{OUT} = 0.5W	R_L = 8 Ω + 33 μH		83.9		%
		R_L = 4 Ω + 33 μH		80.0		%
$\eta_{SYSTEM\_\_EXT\_1W}$	System Efficiency at P_{OUT} = 1.0W	R_L = 8 Ω + 33 μH		88.1		%
		R_L = 4 Ω + 33 μH		84.2		%
$\eta_{SYSTEM\_\_EXT\_1W}$	System Efficiency at P_{OUT} = 1.0W	R_L = 8 Ω + 33 μH, HW pin control mode		88.1		%
$\eta_{SYSTEM\_EXT\_MAX\_POUT}$	System Efficiency at 1% THD+N power Level	R_L = 8 Ω + 33 μH		93.2		%
		R_L = 4 Ω + 33 μH		88.5		%
$\eta_{SYSTEM\_EXT\_MAX\_POUT}$	System Efficiency at 1% THD+N power Level	R_L = 8 Ω + 33 μH, HW pin control mode		93.2		%
V_{N_EXT}	Idle channel Noise	A-Weighted, Gain = 21dBV (Speaker Mode), DAC-Running		14.4		µV
DNR_EXT	Dynamic Range	A-Weighted, -60 dBFS Method, RL = 8 Ω + 33 μH		114.4		dB
THD+N_EXT	Total Harmonic distortion + Noise	P_{OUT} = 1 W, R_L = 8 Ω + 33 μH, f_{in} = 1 kHz		0.003		%
		P_{OUT} = 1 W, R_L = 4 Ω + 33 μH, f_{in} = 1 kHz		0.004		%
K_{CP}_EXT	Click and pop performance	All dynamic power up/downs of audio channel except for faults. Includes In/Out of Mute, Power Up and power Down, Noise Gate mode entry and Exit. Measured at Peak A-weighted Voltage. RL = 8 Ω + 33 μH, Input = Digital Silience		–68		dBV
V_{OS}_EXT	Output Offset Voltage	Idle channel	–1		1	mV

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5.5 Electrical Characteristics (continued)

TA = 25 °C, VBAT = 3.6 V, PVDD = 12 V (External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V, RL = 8Ω + 33μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, SDZ = 1, Noise gate disabled, Measured filter free with an Audio Precision using 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$PSRR_{PVDD\_EXT}$	PVDD power-supply rejection ratio	PVDD = 12 V + 200 mVpp, fripple = 217 Hz		115		dB
		PVDD = 12 V + 200 mVpp, fripple = 1 kHz		115		dB
		PVDD = 12 V + 200 mVpp, fripple = 20 kHz		95		dB
$PSRR_{VBAT\_EXT}$	VBAT power-supply rejection ratio	VBAT = 3.6 V + 200 mV_{pp}, f_{ripple} = 217 Hz		115		dB
		VBAT = 3.6 V + 200 mV_{pp}, f_{ripple} = 1 kHz		115		dB
		VBAT = 3.6 V + 200 mV_{pp}, f_{ripple} = 20 kHz		90		dB
$PSRR_{VDD\_EXT}$	VDD power-supply rejection ratio	VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 217 Hz		110		dB
		VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 1 kHz		110		dB
		VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 20 kHz		90		dB
TDM Serial Port						
	PCM Sample Rates and FSYNC Input Frequency		16		192	kHz
	SBCLK Input Frequency	I^2S/TDM Operation	0.512		24.57	MHz
	SBCLK Maximum Input Jitter	RMS Jitter below 40 kHz that can be tolerated without performance degradation			0.5	ns
		RMS Jitter above 40 kHz that can be tolerated without performance degradation			5	ns
	SBCLK Cycles per FSYNC in I^2S and TDM Modes	Values: 64, 96, 128, 192, 256, 384 and 512	64		512	Cycles
PCM Playback Characteristics to fs ≤ 48 kHz						
fs	Sample Rates		16		48	kHz
	Audio Channel Passband LPF Corner	Ripple < pass-band ripple		0.454		fs
	Audio Channel Passband Ripple	20 Hz to LPF cutoff		± 0.1		dB
	Audio Channel Stop Band Attenuation	≥ 0.55 fs		60		dB
		≥ 1 fs		65		dB
	Audio Channel Group Delay	Fin = 1kHz, Class-H mode		31.5		1/fs
		Fin = 1kHz, Class-H bypassed		6.5		1/fs
		DC to 20kHz, HPF bypassed, Class-H bypassed		11.0		1/fs
		DC to 20kHz, HPF bypassed, Class-H mode		37.0		1/fs
PCM Playback Characteristics to fs > 48 kHz						
fs	Sample Rates		88.2		192	kHz
	Audio Channel Passband LPF Corner	fs = 96 kHz		0.469		fs
		fs = 192 kHz		0.234		fs
	Audio Channel Passband Ripple	20 Hz to LPF cutoff		± 0.2		dB
	Audio Channel Stop Band Attenuation	fs = 96 kHz, fin ≥ 0.55 fs		60		dB
		fs = 96 kHz, fin ≥ 1 fs		65		dB
		fs = 192 kHz, 0.55 fs ≥ fin ≥ 0.275 fs		60		dB

5.5 Electrical Characteristics (continued)

TA = 25 °C, VBAT = 3.6 V, PVDD = 12 V (External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V, RL = 8Ω + 33µH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, SDZ = 1, Noise gate disabled, Measured filter free with an Audio Precision using 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Audio Channel Group Delay	fin=1kHz, fs=96 kHz, Class-H mode		56.7		1/fs
		DC to 40kHz, fs=96 kHz, HPF Bypassed, Class-H bypassed		8.6		1/fs
		DC to 40kHz, fs=192 kHz, HPF Bypassed, Class-H Mode		117.8		1/fs
Protection Circuits						
	Thermal shutdown temperature			140		°C
	Thermal shutdown retry time			1.5		s
	VBAT undervoltage lockout threshold (UVLO)	UVLO is asserted	1.9			V
		UVLO is released			2.3	V
	VDD undervoltage lockout threshold (UVLO)	UVLO is asserted	1.4			V
		UVLO is released			1.6	V
	PVDD undervoltage lockout threshold (UVLO)	UVLO is asserted, external PVDD mode only	2.6			V
		UVLO is released, external PVDD mode only			2.8	V
	PVDD overvoltage lockout threshold (OVLO)	OVLO is asserted, OVLO protection enabled.		16		V
	Output Short circuit protection	Output to Output, Output to GND, Output to PVDD, Output to VBAT, H-bridge mode		4.1		A
Power up/down Time						
T_{STDBY}	Turn ON time from SDZ Asserted to device ready for i2c Command				300	us
T_{ACTIVE}	Turn ON time from release of Software Shutdown to Amplifier output Active	Volume ramping disabled		1.6		ms
		Volume ramping enabled		3.9		ms
$T_{TURNOFF}$	Turn OFF time from assertion of Software Shutdown to Amplifier output Hi-Z	Volume ramping disabled		0.2		ms
		Volume ramping enabled		13.9		ms
Current Consumption - External PVDD Mode						
$I_{Q\_HW\_SD}$	Current consumption in Hardware Shutdown	PVDD, SDZ=0		1		uA
		VBAT, SDZ=0		0.1		uA
		VDD, SDZ=0		0.2		uA
		IOVDD, SDZ=0		0.1		uA
$I_{Q\_SW\_SD}$	Current consumption in Software Shutdown	PVDD, All clocks Stopped		1		uA
		VBAT, All clocks Stopped		0.1		uA
		VDD, All clocks Stopped		12		uA
		IOVDD, All clocks Stopped		0.1		uA
I_{Q_NG}	Current consumption in Idle channel	PVDD, P_{OUT} = 0, Noise gate enabled		0.1		mA
		VBAT, P_{OUT} = 0, Noise gate enabled		0.15		mA
		VDD, P_{OUT} = 0, Noise gate enabled		2.2		mA
		IOVDD, P_{OUT} = 0, Noise gate enabled		0.1		mA
		Total Power, P_{OUT} = 0, Noise gate enabled		5.3		mW

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5.5 Electrical Characteristics (continued)

TA = 25 °C, VBAT = 3.6 V, PVDD = 12 V (External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V, RL = 8Ω + 33µH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, SDZ = 1, Noise gate disabled, Measured filter free with an Audio Precision using 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{Q_IDLE}	Current consumption in Idle channel	PVDD, P_{OUT} = 0, Noise gate disabled		0.2		mA
		VBAT, P_{OUT} = 0, Noise gate disabled		0.5		mA
		VDD, P_{OUT} = 0, Noise gate disabled		5.6		mA
		IOVDD, P_{OUT} = 0, Noise gate disabled		0.1		mA
		Total Power, P_{OUT} = 0, Noise gate disabled		14.0		mW
I_{Q_IDLE}	Current consumption in Idle channel, , HW pin control mode	PVDD, P_{OUT} = 0, Noise gate disabled				mA
		VBAT, P_{OUT} = 0, Noise gate disabled				mA
		VDD, P_{OUT} = 0, Noise gate disabled				mA
		IOVDD, P_{OUT} = 0, Noise gate disabled				mA
		Total Power, P_{OUT} = 0, Noise gate disabled				mW
DIGITAL IOs						
V_{IH}	High-level digital input logic voltage threshold	All digital pins	0.7 x IOVDD			V
V_{IL}	Low-level digital input logic voltage threshold	All digital pins			0.3 x IOVDD	V
V_{OH}	High-level digital output voltage	All digital pins except SDA, SCL and IRQZ; I_{OH} = 100µA	IOVDD - 0.2 V			V
V_{OL}	Low-level digital output voltage	All digital pins except SDA, SCL and IRQZ; I_{OL} = -100µA			0.2	V
$V_{OL(I2C)}$	Low-level digital output voltage	SDA and SCL; I_{OL} = -1mA			0.2 x IOVDD	V
$V_{OL(IRQZ)}$	Low-level digital output voltage for open drain output	IRQZ pin; I_{OL} = -1mA			0.2	V
I_{IH}	Input logic-high leakage for digital inputs	All digital pins; Input = IOVDD.	-1		1	µA
I_{IL}	Input logic-low leakage for digital inputs	All digital pins; Input = GND	-1		1	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pull down resistance for digital input/IO pins when asserted on	All digital pins. Pull down resistance option enabled		18		kΩ

5.6 Timing Requirements

T_A = 25 °C, VDD = IOVDD = 1.8 V (unless other wise noted)

		MIN	NOM	MAX	UNIT
I2C - Standard-Mode					
f_{SCL}	SCL clock frequency	0		100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			µs
t_{LOW}	LOW period of the SCL clock	4.7			µs
t_{HIGH}	HIGH period of the SCL clock	4			µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7			µs
$t_{HD;DAT}$	Data hold time: For I^2C bus devices	0		3.45	µs
$t_{SU;DAT}$	Data set-up time	250			ns
t_r	SDA and SCL rise time			1000	ns
t_f	SDA and SCL fall time			300	ns

5.6 Timing Requirements (continued)

T_A = 25 °C, VDD = IOVDD = 1.8 V (unless other wise noted)

		MIN	NOM	MAX	UNIT
$t_{SU;STO}$	Set-up time for STOP condition	4			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
C_b	Capacitive load for each bus line			400	pF
I2C - Fast-Mode					
f_{SCL}	SCL clock frequency	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6			µs
t_{LOW}	LOW period of the SCL clock	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.6			µs
$t_{HD;DAT}$	Data hold time: For I^2C bus devices	0		0.9	µs
$t_{SU;DAT}$	Data set-up time	100			ns
t_r	SDA and SCL rise time	20 + 0.1 × Cb		300	ns
t_f	SDA and SCL fall time	20 + 0.1 × Cb		300	ns
$t_{SU;STO}$	Set-up time for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
C_b	Capacitive load for each bus line			400	pF
TDM Port					
t_H(SBCLK)	SBCLK high period	20			ns
t_L(SBCLK)	SBCLK low period	20			ns
t_{SU}(FSYNC)	FSYNC setup time	8			ns
t_{HLD}(FSYNC)	FSYNC hold time	8			ns
t_{SU}(SDIN/ICC)	SDIN/ICC setup time	8			ns
t_{HLD}(SDIN/ICC)	SDIN/ICC hold time	8			ns
t_d(SDO/ICC-SBCLK)	SBCLK to SDOUT/ICC delay : 50% of SBCLK to 50% of SDOUT IOVDD=1.8V			13	ns
t_d(SDO/ICC-SBCLK)	SBCLK to SDOUT/ICC delay : 50% of SBCLK to 50% of SDOUT IOVDD=3.3V			30	ns
t_r(SBCLK)	SBCLK rise time : 10 % - 90 % Rise Time			8	ns
t_f(SBCLK)	SBCLK fall time : 90 % - 10 % Rise Time			8	ns

5.7 Typical Characteristics

T_A = 25℃, VBAT = 3.6V, PVDD = 12V (External PVDD mode enabled) , VDD=1.8 V, IOVDD=1.8 V, Load = 8Ω + 33µH, F_{IN} = 1kHz, Fs = 48kHz, Gain = 21dBV, SDZ=1, Noise gate mode disabled, Measured filter free with an Audio Precision with a 22Hz to 20kHz un-weighted bandwidth, unless otherwise noted.

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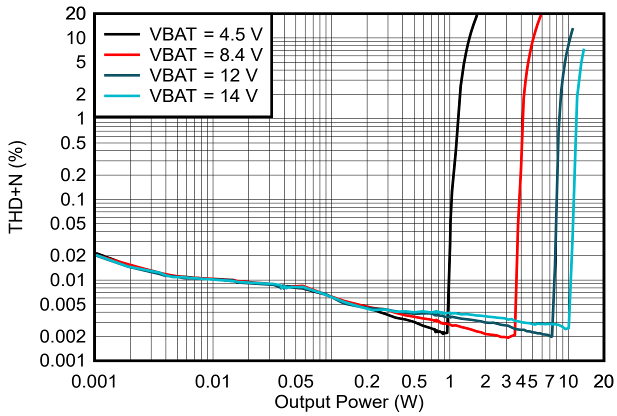
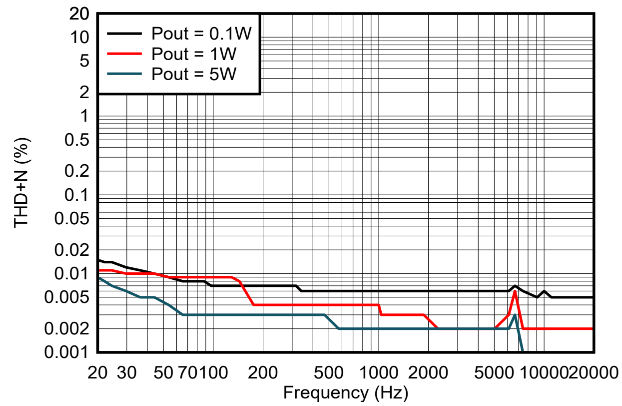


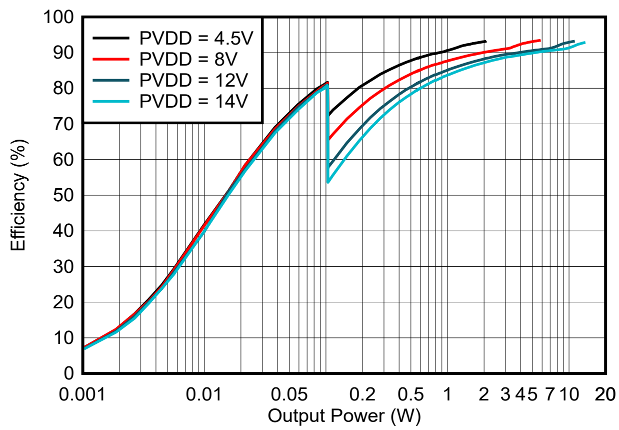
R_L = 8 Ω External PVDD mode

Figure 5-1. THD+N vs Output Power



R_L = 8 Ω PVDD = 12 V External PVDD mode

Figure 5-2. THD+N vs Frequency



R_L = 8 Ω External PVDD mode

Figure 5-3. Efficiency vs Output Power

6 Detailed Description

6.1 Overview

The TAS2320 is a mono digital input Class-D amplifier optimized for delivering the highest efficiency across all powers for longer battery life operation. It comes with a small solution size for board space-constrained applications. It integrates battery/temperature sensors for system-level protection features.

6.2 Functional Block Diagram

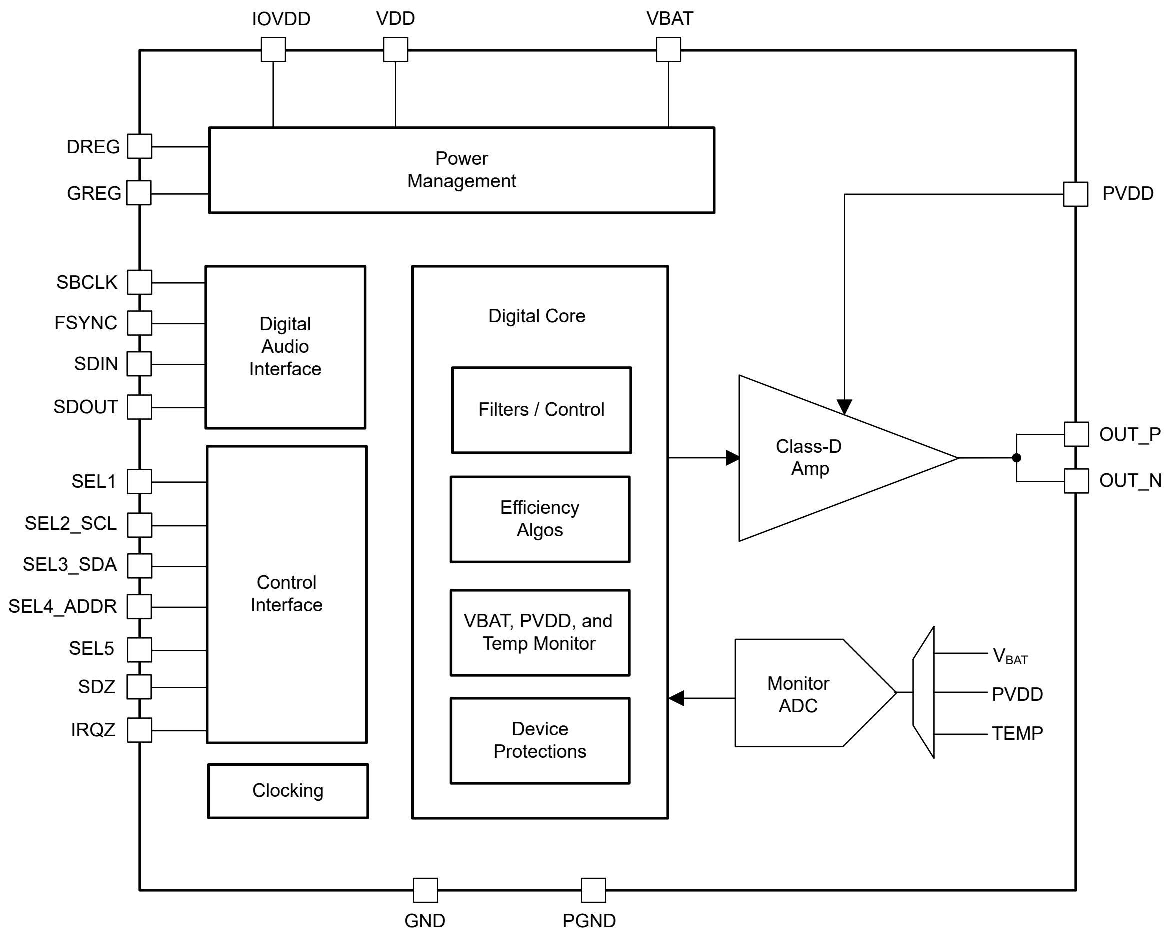


Figure 6-1. Top Level Functional block diagram

6.3 Device Functional Modes

6.3.1 Operational Modes

6.3.1.1 Hardware Shutdown

The device can be powered down by asserting SDZ pin low. The shutdown behavior of the device when SDZ pin is pulled low is controlled by SDZ_MODE register settings.

In Hardware Shutdown mode (SDZ_MODE[1:0] = 00 or 01) if the SDZ pin is asserted low, the device consumes the minimum quiescent current from VDD and VBAT supplies. All registers lose state in this mode and go back to default settings, and I^2C communication is disabled.

If configured in SDZ_MODE[1:0] = 00, when the SDZ pin is asserted low while audio is playing, the device will follow the normal power down sequencing like volume ramp down on the audio (if enabled), stop the Class-D

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switching, power down analog and digital blocks to ensure no power down pop and finally put the device into Hardware Shutdown mode. I2C communication is disabled while the SDZ pin is asserted low in this mode.

If configured in SDZ_MODE[1:0] = 01, when the SDZ pin is asserted low the device will immediately enter the hardware shutdown and will not go through any power-down sequencing routine. It is recommended to ensure that the audio input signal is ramped down to the idle channel before asserting the SDZ pin low in this mode (device software mute mode can be used to realize this). I2C communication is disabled while the SDZ pin is asserted low in this mode.

Finally, the device can be configured to Software shutdown mode by setting SDZ_MODE[1:0] = 10. In this mode, when the SDZ pin is pulled low, the device will follow normal power-down sequencing and enter software shutdown mode. All the device register configuration programmed is retained as is from the state the device was in before the SDZ pin was pulled low. I2C communication is still available while the SDZ pin is asserted low in this mode.

Table 6-1. Shutdown Control

SDZ_MODE[1:0]	Configuration
00 (default)	Hardware shutdown mode with power-down sequencing
01	Hardware shutdown mode - immediate
10	Software shutdown mode (All register values retained)
11	Reserved

When SDZ_MODE[1:0] is 00 or 10, the device goes through shutdown sequencing and the SDZ pin must be held low for the entire duration of the shutdown time. The shutdown time is specified in the Power up/down Time section of the Electrical Characteristics section. When SDZ is released, the device will sample the AD1 and AD2 pins and enter the software shutdown mode.

6.3.1.2 Hardware Config Modes

The device can operate in a pre-configured HW Mode depending on the resistor terminations used for Select pin1 to Select Pin5. HW Mode behavior of the device is designed to simplify device configuration without using any software based configurations through I^2C communication.

Table 6-2. SEL1 HW Mode configuration

SEL1 Connection	Configuration
Direct Short to GND	I^2C Mode selection
1.2k to GND	6dBV Amp Gain, Volume ramp disabled
1.2k to VBAT	12dBV Amp Gain, Volume ramp disabled
5k to GND	18dBV Amp Gain, Volume ramp disabled
330 to VBAT	21dBV Amp Gain, Volume ramp disabled
4.7k to VBAT	6dBV Amp Gain, Volume ramp enabled
24k to GND	12dBV Amp Gain, Volume ramp enabled
24k to VBAT	18dBV Amp Gain, Volume ramp enabled
Direct Short to VBAT	21dBV Amp Gain, Volume ramp enabled

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Table 6-3. SEL2 HW Mode configuration

SEL2_SCL Connection	Configuration
Direct Short to GND	I^2S L or TDM0
470 to IOVDD	I^2S R or TDM1
Direct Short to IOVDD	I^2S (L+R)/2 or TDM2
1.2k to GND	Left-Justified L or TDM3
1.2k to IOVDD	Left-Justified R or TDM4
4.7k to GND	Left-Justified (L+R)/2 or TDM5
4.7k to IOVDD	I^2S L+Tx or TDM6
24k to GND	I^2S R+Tx or TDM7
24k to IOVDD	Reserved

Table 6-4. SEL3 HW Mode configuration

SEL3_SDA Connection	Configuration
Direct Short to GND	Data valid on rising edge
Direct Short to IOVDD	Data valid on falling edge

Table 6-5. SEL4 HW Mode configuration

SEL4_ADDR Connection	Configuration
Direct Short to GND	Y-bridge threshold of 80mW
Direct Short to IOVDD	Y-bridge threshold of 40mW
24k to IOVDD	Y-bridge threshold of 1mW

Table 6-6. SEL5 HW Mode configuration

SEL5 Connection	Configuration
Direct Short to IOVDD	External PVDD Mode

6.3.1.3 Software Power Modes Control and Software Reset

The TAS2320 power state can be controlled using the register MODE[1:0]. Change in any of the MODE settings will not cause the device to lose any of the existing device configuration register settings.

Active state: When MODE[1:0] is configured as '00', the device enters an active mode of operation with proper power-up sequencing to minimize the click and pop.

Software shutdown state: When MODE[1:0] is configured as '10', the device enters software shutdown mode. This mode powers down all analog blocks required to playback audio but does not cause the device to lose register state. If audio is playing when Software Shutdown is asserted, the Class-D will volume ramp down before shutting down. When de-asserted, the Class-D will begin switching and volume ramp back to the programmed digital volume setting.

Clock based Active and shutdown state: When MODE[1:0] is configured as '11' the device toggles between Active and Shutdown state based on valid ASI clock signals applied on the ASI input pins, BCLK and FSYNC. When clocks are applied, the device will automatically detect the clock signals and follow proper power-up sequencing to avoid any power-up click and pop. When the audio channels are powered up and the ASI clock is removed, the device will automatically start power-down sequencing and avoid any click and pop. It is recommended to do a volume ramp-down in the input data stream before stopping the clocks for the best pop & click experience (device software mute mode can be used to realize this).

Table 6-7. Software Mode Control

MODE[1:0]	Configuration
00	Device in active mode of operation

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Table 6-7. Software Mode Control (continued)

MODE[1:0]	Configuration
01	Reserved
10 (default)	Device in software shutdown mode
11	Device in Clock based Active and shutdown mode

TAS2320 can be reset to its default configuration by setting the SW_RESET register to '1'. If the device is powered up, when the SW_RESET bit is set high, all the channels are powered down immediately. All the registers are restored to the default state when SW_RESET is set high. This bit is self-clearing and goes back to '0' once the reset is complete.

The device can also signal to the host once the status of the device reaches Active mode of operation using the *INT_LTCH0[1]* bit (Section 6.3.2). This bit is a live device status bit and reflects the device status in real-time. This bit is set high when the device is in Active mode and set low when the device is in shutdown mode.

6.3.1.4 Efficiency and power saving modes

TAS2320 has multiple power-saving modes of operation designed to achieve the highest system level efficiency under all operating conditions. The device transitions from one mode to the next based on the configured mode and the signal condition. The transitions from one mode to another are automatic and designed to ensure high-performance audio levels during the transition of the modes.

6.3.1.4.1 Noise Gate

When the Noise gate feature is enabled, the device automatically detects periods of silence during active playback mode and reduces the idle channel power consumption significantly to extend the battery life. This feature is useful for signals playback having long periods of silence, eg voice calls, movie tracks, etc.

The device monitors the input audio signal level against the programmed Noise gate threshold configured by the *NG_TH_LVL[2:0]* register. When the audio signal falls below the threshold, an internal Hysteresis timer is enabled. If the signal level remains below the configured *NG_TH_LVL[2:0]* for the entire duration of the *NG_HYST_TIMER[1:0]*, the device enters into the Noise gate mode and reduces the idle channel power consumption. In the Noise gate mode of operation, the high switching blocks like class-D PWM output are turned OFF and outputs are pulled low. The output impedance of class-D can be controlled when the Noise gate mode is active using the *CLASSD_HIZ_MODE* register. While the Noise gate mode is active, class-D outputs are not switching and the device does not produce any audio output signal. When the device is in Noise gate mode, the *NG_STATUS* bit is set as high and when the device comes out of noise gate mode, the status bit is set to low.

When the signal level increases above the NG_TH_LVL[1:0], the device automatically wakes up the blocks in low IQ mode and starts playing out the audio input signals. The wake up from Noise gate maintains the signal fidelity by buffering the input signal data during the transition time from noise gate mode to active playback mode. The device does not lose any audio input samples while transitioning from noise gate to active playback.

The transition into noise gate mode and recovery out of noise gate mode is designed to be click and pop-free by following the proper shutdown and power up sequencing.

Table 6-8. Noise gate threshold

NG_TH_LVL[2:0]	Configuration
000	-85 dBFs
001	-90 dBFs
010	-95 dBFs
011	-100 dBFs

Table 6-8. Noise gate threshold (continued)

NG_TH_LVL[2:0]	Configuration
100 (default)	-105 dBFs
101	-110 dBFs
110	-115 dBFs
111	-120 dBFs

Table 6-9. Noise gate hysteresis timer

NG_HYST_TIMER[1:0]	Configuration
00	10 ms
01 (default)	50 ms
10	100 ms
11	1000 ms

6.3.1.4.2 Music Efficiency Mode

When the Music efficiency mode feature is enabled, the device automatically detects low-power signal states during active playback mode and reduces the overall I_Q power consumption to extend the battery life. This feature is useful for dynamic audio signals with varying signal levels for example music tracks, voice calls movie tracks, and so forth.

The device monitors the input audio signal level against the programmed Music efficiency threshold configured by the *MUSIC_EFF_MODE_THR[23:0]* register. When the audio signal falls below the threshold, an internal hysteresis timer is enabled. If the signal level remains below the configured *MUSIC_EFF_MODE_THR[23:0]* for the entire duration of the *MUSIC_EFF_MODE_TIMER[23:0]*, the device enters into the Music efficiency mode. When the device is in Music efficiency mode, the *MUSIC_EFF_STATUS* bit is set as high and when the device comes out of music efficiency mode, the status bit is set low.

When the signal level increases above the *MUSIC_EFF_MODE_THR[23:0]*, the device automatically wakes up the blocks in low I_Q mode and continues playing out the audio input signals. The transition from Music efficiency mode to normal operation occurs with minimal click and pop. While the device is in Music efficiency mode, the audio channel performance is maintained and doesn't impact the output signal level or noise.

The *MUSIC_EFF_MODE_THR[23:0]* and *MUSIC_EFF_MODE_TIMER[23:0]* registers can be configured using the PPC3 Software Section 6.4.1.

6.3.2 Faults and Status

During power-up sequencing, the power-on-reset circuit (POR) monitors the VDD and IOVDD pins and holds device in reset (including all the configuration registers) until the supplies are valid. Any supply voltage dip on VDD or IOVDD below the UVLO voltage thresholds resets the device immediately along with all the register configurations.

During operation modes, the device monitors internal device status and fault conditions and can notify the host of error and status conditions using the IRQZ interrupt pin and internal I^2C based interrupt registers. The interrupt generation in IRQZ pin can be masked by configuring the corresponding Interrupt mask register bit.

Table 6-10 lists the different faults and interrupts that the device monitors and the corresponding configuration bits to enable/disable the interrupt generation and reading the I2C interrupt status

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Table 6-10. Faults and Interrupts

Category	Interrupt	Interrupt Mask register bit	Default Mask status	Interrupt Latched status bit
Limiter & Brown out protection Section 6.4.2.4	Brownout detected	*INT_MASK0[3]*	Not Masked	*INT_LTCH0[3]*
	BOP Active	*INT_MASK0[2]*	Not Masked	*INT_LTCH0[2]*
	BOP infinite hold	*INT_MASK0[7]*	Not Masked	*INT_LTCH0[7]*
	Limiter Active	*INT_MASK0[4]*	Not Masked	*INT_LTCH0[4]*
	Limiter attenuation	*INT_MASK0[6]*	Not Masked	*INT_LTCH0[6]*
	Supply below inflection point	*INT_MASK0[5]*	Not Masked	*INT_LTCH0[5]*
Supply Voltage Monitors Section 6.4.4	PVDD Over voltage	*INT_MASK3[2]*	Not Masked	*INT_LTCH3[2]*
	PVDD Under voltage	*INT_MASK1[7]*	Not Masked	*INT_LTCH1[7]*
	VBAT2S supply under voltage	*INT_MASK1[6]*	Not Masked	*INT_LTCH1[6]*
	VBAT supply under voltage	*INT_MASK4[7]*	Not Masked	*INT_LTCH4[7]*
Thermal protection Section 6.4.5	Thermal warning at 135C	*INT_MASK1[4]*	Masked	*INT_LTCH1[4]*
	Thermal warning at 125C	*INT_MASK1[3]*	Masked	*INT_LTCH1[3]*
	Thermal warning at 115C	*INT_MASK1[2]*	Masked	*INT_LTCH1[2]*
	Thermal warning at 105C	*INT_MASK1[1]*	Masked	*INT_LTCH1[1]*
	Over temperature error	*INT_MASK3[7]*	Not Masked	*INT_LTCH3[7]*
Clock protection Section 6.4.6.1	Clock error	*INT_MASK2[3]*	Not Masked	*INT_LTCH2[3]*
	Pre-Power-up Clock error	*INT_MASK4[2]*	Not Masked	*INT_LTCH4[2]*
	Clock ratio change error	*INT_MASK2[2]*	Not Masked	*INT_LTCH2[2]*
	Fs change error	*INT_MASK2[1]*	Not Masked	*INT_LTCH2[1]*
	Fs invalid error	*INT_MASK2[0]*	Not Masked	*INT_LTCH2[0]*
	Frame out of sync	*INT_MASK2[5]*	Not Masked	*INT_LTCH2[5]*
	Internal PLL Clock error	*INT_MASK2[4]*	Not Masked	*INT_LTCH2[4]*
	Digital watchdog	*INT_MASK2[7]*	Not Masked	*INT_LTCH2[7]*
Other Protections & Status	Class-D Over current error	*INT_MASK3[3]*	Not Masked	*INT_LTCH3[3]*
	Device Active	*INT_MASK0[1]*	Masked	*INT_LTCH0[1]*

6.3.2.1 Interrupt generation and clearing

The IRQZ is an open drain output that asserts low during unmasked fault conditions and therefore must be pulled up with a resistor to IOVDD. An internal pull up resistor (18kΩ) is provided in the device and can be assessed by setting the *IRQZ_PU* register bit.

The interrupt generation on IRQZ pin can be configured using *IRQZ_PIN_CFG[1:0]* register. For the interrupts that have auto retry feature, the retry timer can be configured using *RETRY_WAIT_TIME* register. The interrupt pin polarity can be changed from the default case of Active Low to Active high by setting the *IRQZ_POL* register bit high.

Any latched interrupt can be cleared by setting INT_CLR_LTCH bit high. This is self clearing bit and automatically gets updated to low once the interrupt is cleared. Interrupts can also be cleared by hardware shutdown by pulling the SDZ pin low, or by software reset using SW_RESET bit.

Table 6-11. IRQZ pin configuration

IRQZ_PIN_CFG[1:0]	Configuration
00	Reserved
01(default)	Interrupt generated on any unmasked latched interrupt
10	Reserved

Table 6-11. IRQZ pin configuration (continued)

IRQZ_PIN_CFG[1:0]	Configuration
11	Interrupt generated for 2 to 4 ms every 4 ms on any unmasked latched interrupt

Table 6-12. Retry wait timer

RETRY_WAIT_TIME	Configuration
0 (default)	Retry every 1.5sec
1	Retry every 100ms

6.4 Feature Description

6.4.1 PurePath™ Console 3 Software

The TAS2320's advanced features and device configuration can be performed using PurePath Console 3(PPC3) software. The base software PPC3 is downloaded and installed from the TI website. Once installed the TAS2320 application can be downloaded from with-in PPC3. The PCC3 tool calculates necessary register coefficients that are described in the following sections. The device performance is optimized using registers named *TUNING* based on the options for system configuration selected in the GUI. This is the recommended method to configure the device. Once the TAS2320 application calculates and updates the device, the registers values can be read back using the PPC3 tool for final system integration.

6.4.2 Playback Signal Path

6.4.2.1 Digital Volume Control and Amplifier Output Level

The gain from audio input to speaker terminals is controlled by setting the amplifier's analog gain level (A_{AMP}) and digital volume control (A_{DVC}). Equation 1 calculates the amplifiers output voltage. Amplifier analog gain setting should be set before powering up the playback channel and shouldn't be changed while the channel is active. The digital volume control can be modified while the channel is active and also allows for soft volume ramp up/down feature to allow for smooth transition of output voltage from one level to another.

$$V_{AMP} = \text{Input} + A_{dvc} + A_{AMP} \;\; \text{dBV} \quad (1)$$

where

- V_{AMP} is the amplifier output voltage in dBV
- Input is the digital input amplitude in dB with respect to 0 dBFS
- A_{DVC} is the digital volume control setting, 6 dB to -110 dB in 0.5 dB steps
- A_{AMP} is the amplifier output level setting, -0.071dBV to 21.0dBV in 0.5017dBV steps.

Amplifier output level settings are presented in dBV (dB relative to 1 V_{rms}) with a full scale digital audio input (0 dBFS) and the digital volume control set to 0 dB. It should be noted that these levels may not be achievable because of analog clipping in the amplifier, so they should be used to convey gain only.

Table below shows gain settings that can be programmed via the *AMP_LVL* register. When AMP_LVL is set to less than 9dBV settings, the playback channel is automatically configured to low noise mode or receiver mode of operation.

Table 6-13. Amplifier Output Level Settings

AMP_LVL[5:0]	FULL SCALE OUTPUT	
	dBV	V_{PEAK} (V)
0x00	21.000	15.9
0x01	20.498	15.0
0x02	19.997	14.1
0x03	19.495	13.3

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Table 6-13. Amplifier Output Level Settings (continued)

AMP_LVL[5:0]	FULL SCALE OUTPUT	
	dBV	V_{PEAK} (V)
0x04	18.993	12.6
...	...	...
0x27	1.434	1.7
0x28	0.932	1.6
0x29	0.430	1.5
0x2A	-0.071	1.4
0x2B-0x3F	Reserved	Reserved

When a change in digital volume control occurs, the device ramps the volume to the new setting based on the *DVC_SLEW_RATE* register bits. If *DVC_SLEW_RATE* is set to 0x7FFFFF, volume ramp is disabled. This can be used to speed up start up, shutdown and digital volume changes when volume ramp is handled by the system host. When volume ramp is disabled, the input audio data stream should be held at digital silence during shutdown and power up of the device to avoid any clicks and pops.

The device can be put in software based mute by setting DVC_LEVEL to 0x000000 setting.

The digital voltage control registers *DVC_LEVEL* and DVC_SLEW_RATE registers can be configured using the PPC3 Software Section 6.4.1.

Table 6-14. Digital Volume Control

DVC_LEVEL[23:0]	VOLUME (dB)
0x000000	Software MUTE
0x00000D (MIN)	-110
...	...
0x400000	0 (default)
...	...
0x7FB261 (MAX)	6

Table 6-15. Digital Volume Ramp Rate

DVC_SLEW_RATE[23:0]	RAMP RATE @ 48kHz (s)
0x00036A	1000ms
...	
0x034A51	4ms (default)
...	
0x7FFFFF	0 - Ramp disabled

6.4.2.2 High Pass Filter

Excessive DC and low frequency content in audio playback signal can damage loudspeakers. The playback path employs a high-pass filter (HPF) to prevent this from occurring. The HPF is a 1st order filter and can be changed from the default 2 Hz for 48ksps fs using the *AUDIO_HPF_N0*, *AUDIO_HPF_N1*, *AUDIO_HPF_D1* registers. The HPF filter frequency scales with change in the FSYNC clock and can be re-configured to achieve the required cutoff frequency for different FSYNC clock frequencies. The coefficients can also be changed to disable the HPF coefficients appropriately. These coefficients should be calculated and set using PPC3 Software Section 6.4.1.

6.4.2.3 Class-D Amplifier

TAS2320 has integrated high performance class-D amplifier with low idle channel noise, low distortion and high PSRR. The Class-D amplifier switches on a clock frequency derived from the SBCLK frequency and is always synchronized to the input clock source. The *SAMP_RATE_CFG* register enables selection between input clock source based out of multiple of 44.1kHz vs 48kHz multiples.

Table 6-16. Sample rate configuration

SAMP_RATE_CFG	Configuration
0 (default)	Audio data rate is multiple/sub-multiple of 48ksps
1	Audio data rate is multiple/sub-multiple of 44.1ksps

For improvements in EMI performance the class-D amplifier supports programmable Edge rate control (ERC) and class-D clock spread spectrum modulation (SSM).

The edge rate of class-D can be controlled using *CLASSD_OUTPUT_EDGERATE_CTRL[1:0]* register. By default the class-D output edge rate is configured to fastest setting to enable high efficiency in the system. The class-D output edge rate can be slowed down using other configuration settings to reduce the EMI energy at high frequency with reduction in efficiency. The exact rate of change of output edge rate varies based on output load conditions, and the values mentioned in the tables below are approximate edge rate levels for default loading conditions.

Table 6-17. Class-D output edge rate control

CLASSD_OUTPUT_EDGERATE_CTRL[1:0]	Configuration
00	Class-D output edge rate of 0.5 V/ns
01	Class-D output edge rate of 1.0 V/ns
10	Reserved
11(default)	Class-D output edge rate of 2 V/ns

The class-D amplifier has over current protection on each of the output power FETs, including the PVDD High side and the ground power FETs.

The class-D amplifier output impedance can be controlled when the outputs stop switching during Noise gate mode using *CLASSD_HIZ_MODE* control register.

Table 6-18. Class-D high-Z mode control

CLASSD_HIZ_MODE	Configuration
0 (default)	Output pulled down with 2.5kΩ
1	Output pulled down with >13kΩ

6.4.2.4 Supply Tracking Limiters with Brown Out Prevention

TAS2320 monitors class-D supply voltage (VBAT or PVDD) along with the audio signal to automatically decrease gain when the audio signal peaks exceed a programmable threshold. This helps prevent clipping and extends playback time through end of charge battery conditions. The limiter and brown out module calculates the signal attenuation required based on the condition of the signal level, channel gain and the selected supply voltage.

The Brown Out Prevention (BOP) module provides a priority input to provide a fast response to transient dips in the battery supply. The BOP feature can be enabled by configuring the register bit *BOP_EN* high. The supply voltage that is tracked to determine Brown out conditions can be configured as V_{BAT} or PVDD based on system configuration needs by using *BOP_SRC* register bit. When the selected supply dips below the brown-out

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threshold configured by setting register *BOP_THR_LVL[23:0]*, the BOP will begin reducing gain. The rate of gain reduction (db/sample) can be configured by setting the *BOP_ATK_RATE[23:0]* registers . When the VBAT supply rises above the brownout threshold, the BOP will begin to release the gain after the programmed hold timer, *BOP_HLD_COUNT[23:0]*. The BOP feature uses the *LIM_RLS_RATE[23:0]* register setting to release after a brown out event. The release rate is rate of gain increase in db/sample ratio. During a BOP event the limiter updates will be paused. This is to prevent a limiter from releasing during a BOP event.

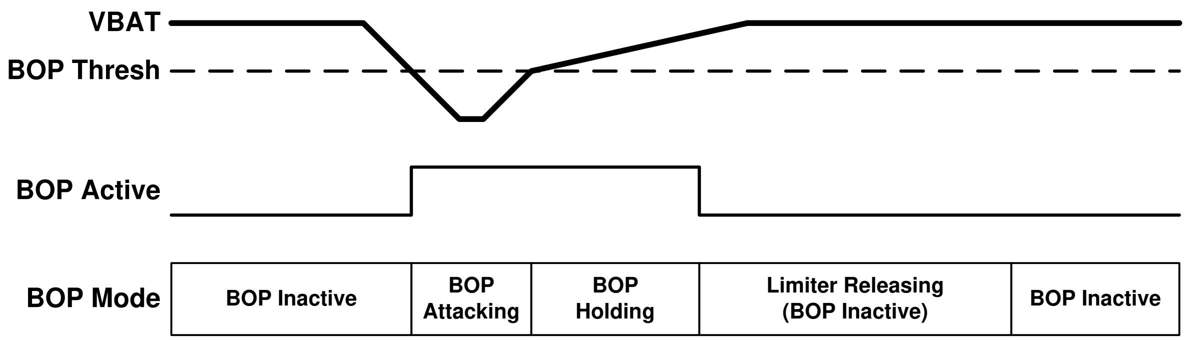

Figure 6-2. Brown Out Prevention Event

The device can be configured to hold the gain attenuation once a BOP event is detected by setting the register bit *BOP_INF_HLD* high. When the bit is programmed high, the Limiter and BOP module does not release the gain attenuation and holds the device in the programmed min gain attenuation level until the infinite hold is cleared by setting the register bit *BOP_HLD_CLR* high. The hold clearing bit is self clearing and will automatically reset to low state once the hold is cleared.

A hard brownout level can be set to shutdown the device if the BOP gain attenuation cannot mitigate the drop in battery voltage. The brown out based shutdown of the device is enabled when *BOPSD_EN* bit is set high and shuts down when the battery voltage falls below the voltage threshold set by *BOSD_THR_LVL[23:0]* register bits.

A maximum level of attenuation applied by the limiters and brown out prevention feature is configurable via the *LIM_MAX_ATN* register. This attenuation limit is shared between the features. For instance, if the maximum attenuation is set to 6 dB and the limiters have reduced gain by 4 dB, the brown out prevention feature will only be able to reduce the gain further by another 2 dB. If the limiter or brown out prevention feature is attacking and it reaches the maximum attenuation, gain will not be reduced any further.

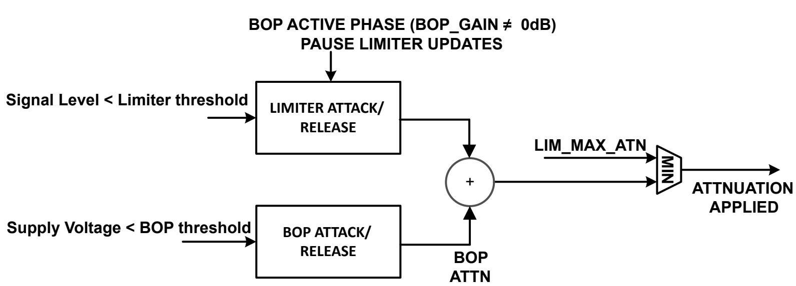

Figure 6-3. Limiter and Brown out gain attenuation

6.4.2.4.1 Voltage Limiter and Clipping protection

The supply tracking limiter can be configured using *LIM_MODE[1:0]* register. In the VBAT voltage mode, the limiter tracks the VBAT supply voltage for voltage limiter and in PVDD voltage mode, the limiter tracks the PVDD voltage for external PVDD mode of use case.

Table 6-19. Limiter mode selection

LIM_MODE[1:0]	Configuration
00 (default)	Disabled

Table 6-19. Limiter mode selection (continued)

LIM_MODE[1:0]	Configuration
01	VBAT voltage based limiter
10	PVDD voltage based limiter
11	Reserved

The limiter can be configured to reduce the output signal based on fixed signal threshold level, or it can attenuate signal based on a dynamic threshold which tracks the selected supply voltage. The register bit *SUPPLY_HEADROOM_LIM_MODE* enables the dynamic supply tracking and can be used to limit the clipping distortion when the supply voltage is varying in the system.

Table 6-20. Limiter dynamic supply headroom tracking mode

SUPPLY_HEADROOM_LIM_MODE	Configuration
0(default)	Disabled
1	Enabled. Limiter threshold is dynamically changed based as a fixed percentage of monitored supply voltage.

When *SUPPLY_HEADROOM_LIM_MODE* is set high, the limiter sets the threshold as a fixed percentage of the monitored supply voltage. The limiter begins reducing gain when the output signal level is greater than the threshold configured. For eg, if voltage limiting is desired to be 10% below the supply voltage, then *LIM_SLOPE[23:0]* is configured as 0.9 and the threshold is calculated as monitored supply voltage multiplied by 1.1. Similarly if the *LIM_SLOPE[23:0]* is configured at > 1.0, the limiter threshold is set at higher than the supply voltage, and a small amount of controlled clipping occurs.

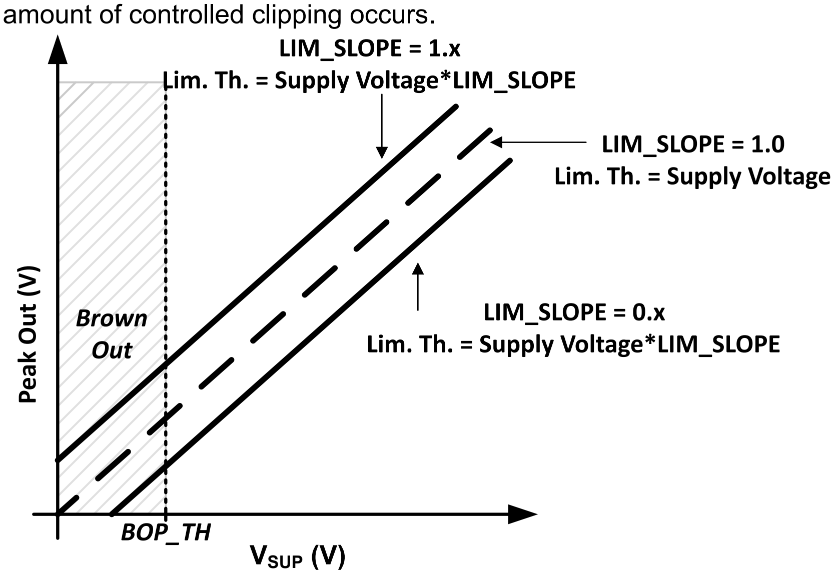

Figure 6-4. Limiter with dynamic supply headroom

When *SUPPLY_HEADROOM_LIM_MODE* is set low, the limiter begins reducing gain when the output signal level is greater than the limiter threshold. The limiter can be configured to track selected supply below a programmable inflection point with a minimum threshold value. Figure 6-5below shows the limiter configured to limit to a constant level regardless of the selected supply level. To achieve this behavior, set the limiter maximum threshold to the desired level using *LIM_TH_MAX[23:0]*. Set the limiter inflection point using *LIM_INF_PT[23:0]*

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below the minimum allowable supply setting. The limiter minimum threshold register *LIM_TH_MIN[23:0]* does not impact limiter behavior in this use case.

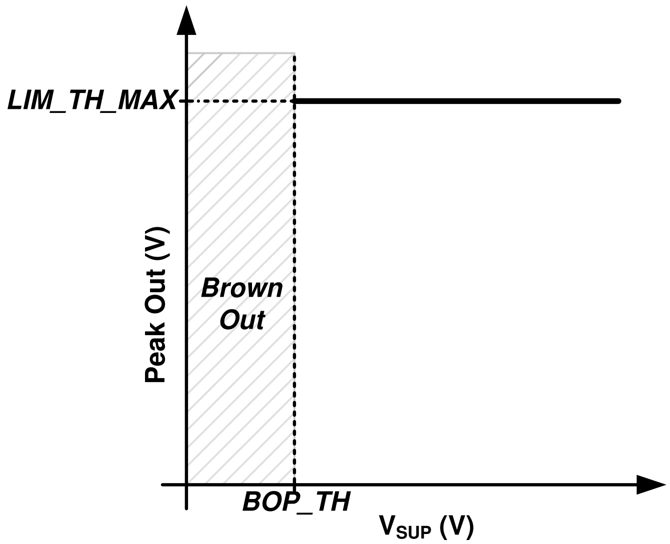

Figure 6-5. Limiter with Fixed Threshold

Figure 6-6 shows how to configure the limiter to track selected supply below a threshold without a minimum threshold. Set the *LIM_TH_MAX[23:0]* register to the desired threshold and *LIM_INF_PT[23:0]* register to the desired inflection point where the limiter begins to reduce the threshold with the selected supply. The *LIM_SLOPE[23:0]* register bits can be used to change the slope of the limiter tracking the supply voltage in V/V. For example, a slope value of 1 V/V reduces the limiter threshold 1 V for every 1 V of drop in the supply voltage. Program the *LIM_TH_MIN[23:0]* below the minimum of the selected supply to prevent the limiter from having a minimum threshold reduction when tracking the selected supply.

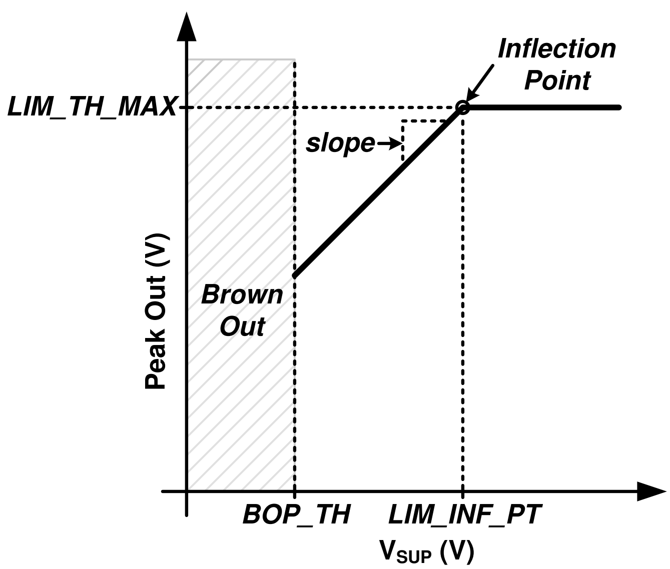

Figure 6-6. Limiter with Inflection Point

To achieve a limiter that tracks the selected supply below a threshold, configure the limiter as explained in the previous example, except program the *LIM_TH_MIN[23:0]* register to the desired minimum threshold. This is shown in Figure 6-7 below.

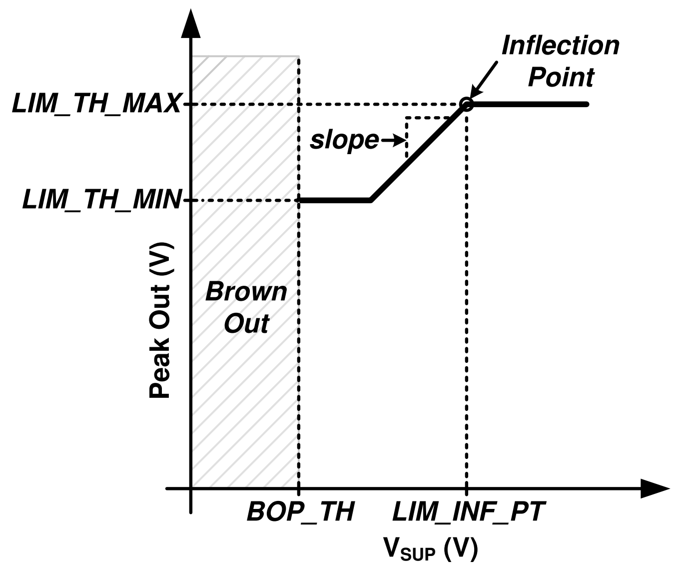

Figure 6-7. Limiter with Inflection Point and Minimum Threshold

The limiter has a configurable attack rate (dB/Sample), hold time (no of samples) and release rate (db/Sample), which are available via the *LIM_ATK_RATE[23:0]*, *LIM_HLD_COUNT[23:0]*, *LIM_RLS_RATE[23:0]* register bits.

6.4.2.5 Tone Generator

TAS2320 can generate internally a sine tone using an integrated tone generator. This feature can be enabled by configuring the register bit *INTERNAL_TONE_GEN_ENZ* to low. The tone signal will start playing back on the output by configuring the *INTERNAL_TONE_PLAYBACK_EN* bit high. When set high, the device will start generating a sine tone based on the programmed *TONE_GEN_CNTRL_xx* registers. The tone generator can generate any frequency from 16Hz to a maximum frequency of 0.45*Fs, where Fs is the sampling rate of the input digital clocks. The amplitude of the tone signal can also be controlled using the *TONE_GEN_CNTRL_xx* registers. It is recommended to program the tone frequency and amplitude using the PPC3 Software.

The internally generated tone can be mixed with incoming audio stream, or can replace the input audio stream and only tone signal is generated using *INTERNAL_TONE_MIXING_EN* register.

Table 6-21. Internal tone generator mixing options

INTERNAL_TONE_MIXING_EN	Configuration
0	Only internal tone is generated.
1(default)	Internally generated tone is mixed with input audio data and played together.

The tone generator can use external clock source like BCLK, or it can be generated using internal oscillator to generate tone signals even with no external clock sources using *INTERNAL_TONE_CLK_SEL* register.

Table 6-22. Internal tone clock source selection

INTERNAL_TONE_CLK_SEL	Configuration
0 (default)	Tone generator uses external clocks
1	Tone generator uses internal oscillator

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6.4.3 Digital Audio Serial Interface

The device provides a flexible Audio Serial Interface (ASI) port. The port can be configured to support a variety of formats including stereo I^2S, Left Justified, and TDM. Mono audio playback is available via the SDIN pin. The SDOUT pin is used to transmit sample streams including PVDD voltage, VBAT voltage, die temperature, status and audio for echo reference.

The TDM serial audio port supports up to 16 32-bit time slots at 44.1/48 kHz, 8 32-bit time slots at a 88.2/96 kHz sample rate and 4 32-bit time slots at a 176.4/192 kHz sample rate. The device supports 2 time slots at 32 bits in width and 4 or 8 time slots at 16, 24 or 32 bits in width. The device automatically detects the number of time slots and this does not need to be programmed. PCM data sampling rate and SBCLK to FSYNC ratio detected on the TDM bus is reported back on the read-only register bits *FS_RATE_DETECTED[2:0]* and *FS_RATIO_DETECTED[3:0]* respectively.

Table 6-23. PCM Data Sample Rate Detected

FS_RATE_DETECTED[2:0] (Read Only)	Setting
000	Reserved
001	14.7kHz / 16kHz
010	22.05kHz / 24kHz
011	29.4kHz / 32kHz
100 (default)	44.1kHz / 48kHz
101	88.2 kHz / 96 kHz
110	176.4 kHz / 192 kHz
111	Error condition

A frame begins with the transition of FSYNC from either high to low or low to high (set by the *FRAME_START* register bit). FSYNC and SDIN are sampled by SBCLK using either the rising or falling edge set by the *RX_EDGE* register bit. The *RX_OFFSET[4:0]* register bits define the number of SBCLK cycles from the transition of FSYNC until the beginning of time slot 0. This is typically set to a value of 0 for Left Justified format and 1 for an I^2S format.

The *RX_SLEN[1:0]* register bits set the length of the RX time slot to 16, 24 or 32 (default) bits. The length of the audio sample word within the time slot is configured by the *RX_WLEN[1:0]* register bits. The RX port will left justify the audio sample within the time slot by default, but this can be changed to right justification via the *RX_JUSTIFY* register bit. The device supports mono and stereo down mix playback ([L+R]/2). By default the device will playback mono from the time slot equal to the I^2C base address offset (set by the AD1 and AD2 pins) for playback. The *RX_SCFG[1:0]* register bits can be used to override the playback source to the left time slot, right time slot or stereo down mix set by the *RX_SLOT_R[3:0]* and *RX_SLOT_L[3:0]* register bits.

If time slot selection places reception either partially or fully beyond the frame boundary, the receiver returns a null sample equivalent to a digitally muted sample.

The TDM port can transmit a number of sample streams on the SDOUT pin including interrupts and status, PVDD voltage, VBAT voltage and die temperature.

Either the rising or falling edge of SBCLK can be used to transmit data on the SDOUT pin. This can be configured by setting the *TX_EDGE* register bit. The *TX_OFFSET[2:0]* register bits define the number SBCLK cycles between the start of a frame and the beginning of time slot 0. This is programmed to 0 for Left Justified format and 1 for I^2S format. The TDM TX can either transmit logic 0 or Hi-Z depending on the setting of the *TX_FILL* register bit. An optional bus keeper can weakly hold the state of SDOUT pin when all devices are driving Hi-Z. Since only one bus keeper is required on SDOUT, this feature can be disabled via the *TX_KEEPEN* register bit. The bus keeper can be configured to hold the bus for only 1 LSB or Always (permanent) using *TX_KEEPLN* register bit. Additionally, the keeper LSB can be driven for a full cycle or half of cycle using *TX_KEEPCY* register bit.

The device also support monitoring and TDM transmit of PVDD and VBAT input voltages. For PVDD slot, enable and length settings *PVDD_SLOT[5:0]*, *PVDD_TX* and *PVDD_SLEN* register bits can be use. Similarly for VBAT slot, enable and length settings *VBAT_SLOT[5:0]*, *VBAT_TX* and *VBAT_SLEN* register bits can be used. Die temperature can also be transmitted from the device in same manner. Enable and slot settings for Die temperature are done using *TEMP_TX* and *TEMP_SLOT [5:0]* register bits.

Information about status of slots can be found in *STATUS_SLOT[5:0]* register bits. *STATUS_TX* register bit set high enables the status transmit. If time slot selections place transmission beyond the frame boundary, the transmitter will truncate transmission at the frame boundary.

6.4.3.1 Digital Loopback

The device supports loop back feature to loop SDIN data to SDOUT at two levels. When this feature is enabled through *TDM_LOOPBACK* register bit, loop back is done at the IO Pin level without any ASI data decoding within the device. Other option is to enable the loop back feature through *TDM_DESER_LOOPBACK* register bit in which case SDIN data first goes through ASI protocol decoding within the device and then sent back via SDOUT. These SDIN to SDOUT loop back options can be useful for board level debug of an audio system.

Device can also loop back echo reference digital audio data at the end of the internal signal processing blocks like Limiter, BOP etc. through SDOUT signal. This allows audio system to perform noise and echo cancellation algorithms in a host processor that is connected to the device. The echo reference can be enabled by configuring AUDIO_TX register bit. The slot length and the time slot can be selected using AUDIO_SLEN and AUDIO_SLOT[5:0] register bits.

6.4.4 Supply Voltage Monitors

TAS2320 has integrated SAR ADC to monitor the supply voltage pins VBAT and PVDD. The sensed voltages are used for internal device features, protections and can also be streamed out over digital data bus or read through i2c registers.

The monitor ADC samples the VBAT pin at higher rate compared to PVDD pin voltage. This sampling speed can be swapped to prioritize PVDD pin sampling rate over VBAT, for example in case of external PVDD mode of operation.

Table 6-24. Supply monitor sampling rate

SUPPLY_SAMPLING_RATE	Configuration
0(default)	VBAT Sampling rate is higher than PVDD
1	PVDD Sampling rate is higher than VBAT

The VBAT and PVDD monitored voltages are stored in the register *VBAT_CNV* and *PVDD_CNV* registers and can be read using i2c commands.

The supply monitors are also used for voltage protection like VBAT under voltage, PVDD over voltage and under voltage. The voltage protection features monitors the supply voltages, and shuts down the device when the voltage crosses the protection threshold levels. The device also sets the corresponding fault register and can generate an interrupt on IRQZ pin based on configured interrupt Mask register as described in Section 6.3.2. Once the device is shutdown, the device can be re-powered up using the *MODE[1:0]* register bits.

PVDD over voltage protection is based on the monitored PVDD voltage compared against a programmable threshold which can be controlled using *PVDD_OVLO_TH_SEL_EXT* in the external PVDD mode of operation. The PVDD Over voltage protection is enabled by default and can be disabled by setting *PVDD_OV_DET_DIS* bit high.

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Table 6-25. PVDD Over voltage protection threshold, External PVDD mode

PVDD_OVLO_TH_SEL_EXT[1:0]	Configuration
00	Over voltage threshold is 13.5V
01 (default)	Over voltage threshold is 14V
10	Over voltage threshold is 15V
11	Over voltage threshold is 16V

6.4.5 Thermal Protection

TAS2320 has internal device junction temperature monitor which protects the device against over temperature. When the internal temperature rises above the Over temperature threshold, the device automatically shuts down and sets the Over temperature flag in the corresponding Interrupt registers. The device can automatically retry to power up if *OTE_RETRY* bit is set high. When set high, the device attempts to re-power up after every *RETRY_WAIT_TIME* setting (default 1.5 seconds of retry)

Along with over temperature protection, the device has thermal warning thresholds to allow for system to raise interrupts or flags as the junction temperature is approaching the shutdown. There are four thermal warning flags available at the internal temperature of 105C, 115C, 125C and 135C. Each thermal warning flag can be independently set to control the Interrupt generation on the IRQZ pad. The minimum temperature and the step size of the temperature warning flag can be programmed using the registers *THERMAL_WARN_MIN_TEMP[23:0]* and *THERMAL_WARN_TEMP_STEP[23:0]*

The real time internal junction temperature is monitored are stored in the register *TMP_CNV* and can be read using i2c commands.

6.4.6 Clocks and PLL

In TDM/I^{2}S Mode, the device operates from SBCLK. Table 6-26 below shows the valid SBCLK frequencies for each sample rate and SBCLK to FSYNC ratio. For 44.1kHz based clocking, the same table is applicable with the associated ratio change between 48ksps to 44.1ksps.

While the sampling rate of 192kHz is supported, data is internally down-sampled to 96kHz. Therefore audio content greater than 40kHz should not be applied to prevent aliasing. This additionally affects all processing blocks like BOP and limiter which should use 96 kHz fs when accepting 192 kHz audio.

If the sample rate is properly configured via the *SAMPLE_RATE_CFG* bits, no additional configuration is required as long as the SBCLK to FSYNC ratio is valid. The device automatically detects the input PCM FSYNC and BCLK frequency and auto configures itself to playback audio signal. The detected clock rates can be read using the read only registers *FS_RATIO_DETECTED* and *FS_RATE_DETECTED*. The device will detect improper SBCLK frequencies and SBCLK to FSYNC ratios and volume ramp down the playback path to minimize audible artifacts.

Table 6-26. Supported SBCLK Frequencies (MHz) (48 kHz based sample rates)

Sample Rate (kHz)	SBCLK to FSYNC Ratio													
	16	24	32	48	64	96	128	192	256	384	512	125	250	500
16 kHz	NA	0.384	0.512	0.768	1.024	1.536	2.048	3.072	4.096	6.144	8.192	2	4	8
24 kHz	0.384	0.576	0.768	1.152	1.536	2.304	3.072	4.608	6.144	9.216	12.288	3	6	12
32 kHz	0.512	0.768	1.024	1.536	2.048	3.072	4.096	6.144	8.192	12.288	16.384	4	8	16
48 kHz	0.768	1.152	1.536	2.304	3.072	4.608	6.144	9.216	12.288	18.432	24.576	6	12	24
96 kHz	1.536	2.304	3.072	4.608	6.144	9.216	12.288	18.432	24.576	NA	NA	12	24	NA
192 kHz	3.027	4.608	6.144	9.216	12.288	18.432	24.576	NA	NA	NA	NA	24	NA	NA

6.4.6.1 Auto clock based wakeup and clock errors

TAS2320 supports flexible operating mode transition from active to shutdown and vice-verse using ASI clock auto detection feature. When MODE[1:0] is configured as '11' the device toggles between Active and Software shutdown state based on valid ASI clock signals applied on the ASI input pins, ie BCLK and FSYNC. If no ASI clocks are detected in this mode, the device remains in software shutdown, with software shutdown mode I_Q on VDD pin, until a valid BCLK and FSYNC clock is detected. Once a valid clock is detected, the device is powered up in active state until the clocks are valid or device is shutdown using software or hardware shutdown commands.

The device can detect and raise interrupt flags on detection of incorrect clock configurations based on status of *CLK_ERR_PWR_EN*. When this bit is set high, the device monitors for activity on the clock pins and flags any error using the latched interrupts status register. The device can also raise interrupts using IRQZ pin based on status of the corresponding interrupt MASK registers. When the error protection bit is enabled, if a clock error is detected, the device will automatically shutdown with proper shutdown sequencing and minimize any clicks and pops due to invalid clocks.

When the device is in shutdown state, the clock error detection can be delayed to provide system with time required to settle the input clocks. This power up delay in clock error detection is controlled using an internal pre-power up clock error detection timer configured by *CLK_HALT_TIMER*. If device doesn't detect a valid clock at the end of the *CLK_HALT_TIMER* expiry, the Pre-Power-up Clock error is flagged on *INT_LTCH4[2]* bit, and corresponding interrupt can be generated on IRQZ pin based on status of *INT_MASK4[2]* bit. When MODE[1:0] is configured as '11' (Wake-up on ASI mode), CLK_HALT_TIMER of '000' is not recommended and it stops the device from entering the software shutdown and increases the VDD I_Q while the device is shutdown.

Once the device is powered up, the external and internally generated clocks are constantly monitored based on status of *CLK_ERR_PWR_EN* bit. If enabled, any error in external or internal clock is flagged using the clock error status register *INT_LTCH2[3]* bit, and corresponding interrupt can be generated on IRQZ pin based on status of *INT_MASK2[3].*

For system flexibility, the device will also set the error status for the type of detected clock error. The device can also be configured to raise an interrupt on IRQZ pin for any specific type of clock error, instead of using the generic clock error interrupt generation. Table 6-29 below explains the different type of clock errors and corresponding status bits and interrupt MASK register bits. One or more register bits in the table below can be set based on the type of clock error detected.

If the device shuts down due to any type of clock error, it can attempt to re-power itself automatically when *MODE[1:0]* is set to '11'.

Table 6-27. Clock Error detection control

CLK_ERR_PWR_EN	Setting
0	Disabled
1	Enabled (default)

Table 6-28. Clock Halt Timer

CLK_HALT_TIMER[2:0]	Setting
000	Disabled (infinite time).
001	0.8 ms (default)
010	3.2 ms
011	34.1 ms
100	68.3 ms
101	256 ms
110	768 ms
111	1.3 s

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Table 6-29. Clock error type description

Clock error type	Description	Status flag register bit	IRQZ generation Mask bit
Clock error	Clock error for any internal or external clocking configuration errors. This bit will be set along with specific clock errors detected in the rest of the table below except for Pre-Power-up Clock errors.	*INT_LTCH2[3]*	*INT_MASK2[3]*
Pre-Power-up Clock error	Clock error detected during shutdown mode after clock error is detected at end of CLK_HALT_TIMER.	*INT_LTCH4[2]*	*INT_MASK4[2]*
Clock ratio change error	Clock error detected due to on the fly change in FSYNC to SBCLK ratio.	*INT_LTCH2[2]*	*INT_MASK2[2]*
Fs change error	Clock error detected due to on the fly change in FSYNC clock frequency	*INT_LTCH2[1]*	*INT_MASK2[1]*
Fs invalid error	Clock error detected due to incorrect FSYNC clock frequency	*INT_LTCH2[0]*	*INT_MASK2[0]*
Frame out of sync	Clock error detected due to Frame out of sync	*INT_LTCH2[5]*	*INT_MASK2[5]*
Internal PLL Clock error	Clock error detected due to internally generated clock frequency error.	*INT_LTCH2[4]*	*INT_MASK2[4]*

The device also has a digital watchdog timer which monitors for errors in the internal digital state machine and shuts down the device on detection of such errors. This error can also raise an interrupt on IRQZ pin and flag to the host device of the error state.

6.4.7 Digital IO pins

TAS2320 supports 1.8V and 3.3V IO voltage supply based on the voltage applied on the IOVDD pin.

I2S digital input pin has an optional weak pull down to prevent the pin from floating. Pull downs are not enabled during HW shutdown. The pull downs are disabled by default and can be enabled by setting the corresponding Pull down enable bit high.

Table 6-30. Digital pin weak pull down

Pin Name	Pull down control register name
SDOUT	*SDOUT_PD_EN*
SDIN	*SDIN_PD_EN*
FSYNC	*FSYNC_PD_EN*
SBCLK	*SBCLK_PD_EN*

6.5 Programming

The device contains configuration registers and programming coefficients that can be set to the desired values for a specific system and application use. These registers are called device control registers and are each eight bits in width, mapped using a page scheme.

Each page contains 128 configuration registers. All key device configuration registers are stored in page 0, which is the default page setting at power up and after a software reset. All programmable coefficient registers are located in page 2, page 3 and later pages. The current page of the device can be switched to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

6.5.1 I^{2}C Control Interface

The device supports the I^{2}C control protocol as a target device, and is capable of operating in standard mode, fast mode, and fast mode plus. Device configuration and status are provided via the SDA and SCL pins using the I^{2}C protocol.

6.5.2 I^2C Address Selection

The TAS2320 can operate using one of four selectable device addresses. I^2C target addresses is defined as the 7 MSBs followed by read/write bit. Table 6-31 below illustrates how to select the device I^2C address and the address corresponds to R/W bit set to 0 (ie ADDR[6:0],1b'0). The I^2C address is detected by sampling the address pins when SDZ pin is released or when device is reset using software reset bit.

Table 6-31. I^2C Mode Address Selection

I^2C TARGET ADDRESS	AD2 PIN	AD1 PIN
0x80 (global address)	NA	NA
0x90	GND	GND
0x92	GND	IOVDD
0x94	IOVDD	GND
0x96	IOVDD	IOVDD

The TAS2320 has a global 7-bit I^2C address 0x40 (0x80 in 8-bit format with R/W bit set to 0). When enabled the device will additionally respond to I^2C commands at this address regardless of the address pins selected . This is used to speed up device configuration when using multiple TAS2320 devices and programming similar settings across all devices. The I^2C ACK / NACK cannot be used during the multi-device writes since multiple devices are responding to the I^2C command. The I^2C CRC function should be used to ensure each device properly received the I^2C commands. At the completion of writing multiple devices using the global address, the CRC at *I2C_CKSUM* register should be checked on each device using the local address for a proper value. The global I^2C address can be disabled using *I2C_GBL_EN* register.

Table 6-32. I^2C Global Address Enable

I2C_GBL_EN	SETTING
0	Disabled
1	Enabled (default)

6.5.3 General I^2C Operation

The I^2C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred MSB first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the controller device driving a start condition on the bus and ends with the controller device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The controller device drives a start condition followed by the 7-bit target address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledgment condition. The target device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the controller device transmits the next byte of the sequence. Each target device is addressed by a unique 7-bit target address plus the R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

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There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the controller device generates a stop condition to release the bus. Figure 6-8 shows a generic data transfer sequence.

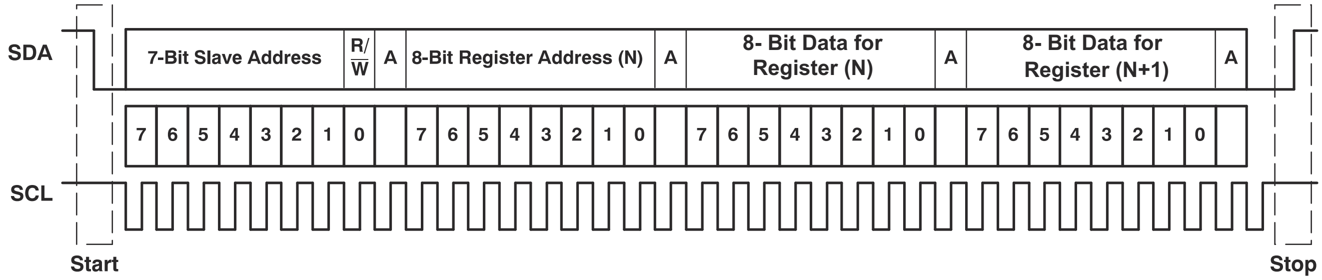

Figure 6-8. Typical I²C Sequence

In the system, use external pullup resistors for the SDA and SCL signals to set the logic high level for the bus. The SDA and SCL voltages must not exceed the device supply voltage, IOVDD.

6.5.4 I²C Single-Byte and Multiple-Byte Transfers

The device I²C interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the device responds with data, a byte at a time, starting at the register assigned, as long as the controller device continues to respond with acknowledges.

The device supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction takes place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many registers are written.

6.5.5 I²C Single-Byte Write

As shown in Figure 6-9, a single-byte data write transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I²C target address and the read/write bit, the device responds with an acknowledge bit (ACK). Next, the controller device transmits the register byte corresponding to the device internal register address being accessed. After receiving the register byte, the device again responds with an acknowledge bit (ACK). Then, the controller transmits the byte of data to be written to the specified register. When finished, the target device responds with an acknowledge bit (ACK). Finally, the controller device transmits a stop condition to complete the single-byte data write transfer.

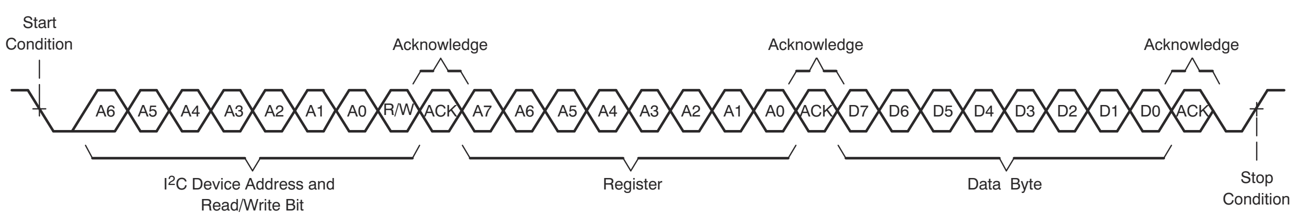

Figure 6-9. I²C Single-Byte Write Transfer

6.5.6 I^{2}C Multiple-Byte Write

As shown in Figure 6-10, a multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the controller device to the target device. After receiving each data byte, the device responds with an acknowledge bit (ACK). Finally, the controller device transmits a stop condition after the last data-byte write transfer.

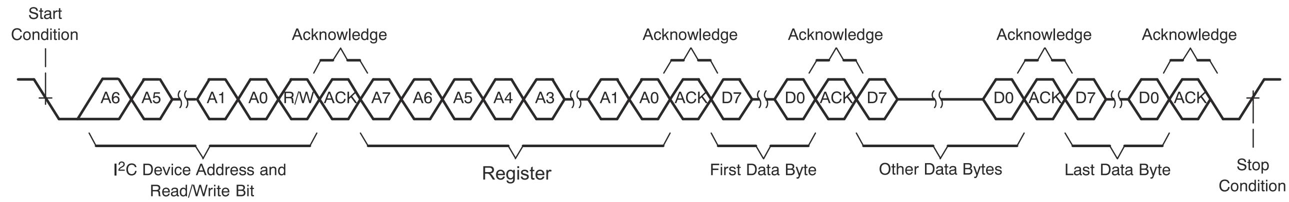

Figure 6-10. I^{2}C Multiple-Byte Write Transfer

6.5.7 I^{2}C Single-Byte Read

As shown in Figure 6-11, a single-byte data read transfer begins with the controller device transmitting a start condition followed by the I^{2}C target address and the read/write bit. For the data read transfer, both a write followed by a read are done. Initially, a write is done to transfer the address byte of the internal register address to be read. As a result, the read/write bit is set to 0.

After receiving the target address and the read/write bit, the device responds with an acknowledge bit (ACK). The controller device then sends the internal register address byte, after which the device issues an acknowledge bit (ACK). The controller device transmits another start condition followed by the target address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the device transmits the data byte from the register address being read. After receiving the data byte, the controller device transmits a not-acknowledge (NACK) followed by a stop condition to complete the single-byte data read transfer.

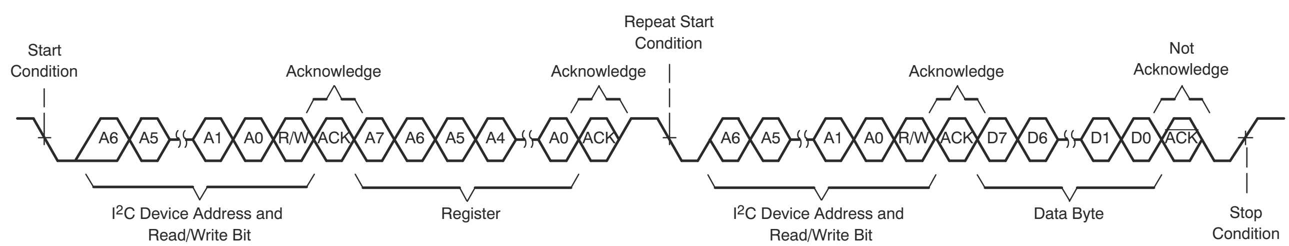

Figure 6-11. I^{2}C Single-Byte Read Transfer

6.5.8 I^{2}C Multiple-Byte Read

As shown in Figure 6-12, a multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the device to the controller device. With the exception of the last data byte, the controller device responds with an acknowledge bit after receiving each data byte. After receiving the last data byte, the controller device transmits a not-acknowledge (NACK) followed by a stop condition to complete the data read transfer.

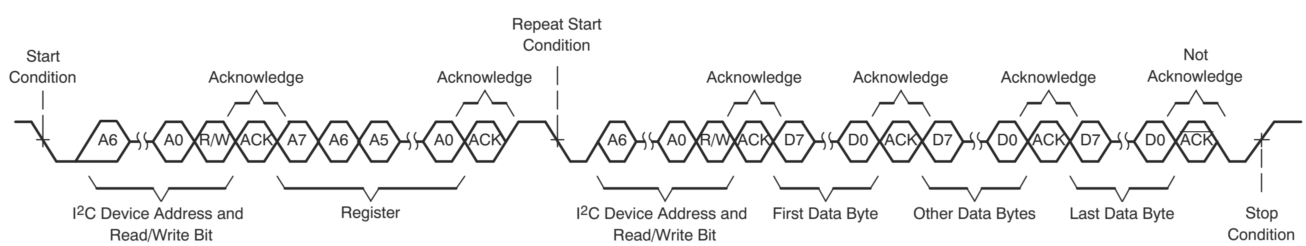

Figure 6-12. I^{2}C Multiple-Byte Read Transfer

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

TAS2320 is a mono channel digital-in Class-D amplifier with battery voltage and temperature monitoring capabilities. I^2S audio data is supplied by host processor via SDIN data port along with the bit clock and frame sync signals. I^2C bus is used for configuration and control.

The device needs external power supply voltage rails of VBAT: 2.5V to 5.5V, VDD : 1.65V to 1.95V and IOVDD: 1.8V or 3.3V for operation.

PurePath^{TM} Console 3 (PPC3) software is the recommended tool to configure the device, and it enables optimization of device performance parameters depending on different application scenarios.

7.2 Typical Application

Diagrams below shows the typical application connections for Li-Ion battery and for the external PVDD or 3S Battery connection. SEL1 is used for HW Mode selection or I^2C Mode selection of the Device.

System can use same 1.8V supply source to power the IOVDD and VDD if required. The decoupling caps C2 and C3 should still be placed close to the device pins.

VBAT, VDD, PVDD power rails are critical for device performance and wide trace should be used from the source PMIC to these pins to minimize parasitic inductance. Supply ripple should be kept at minimum for these rails and should be connected to common supply planes.

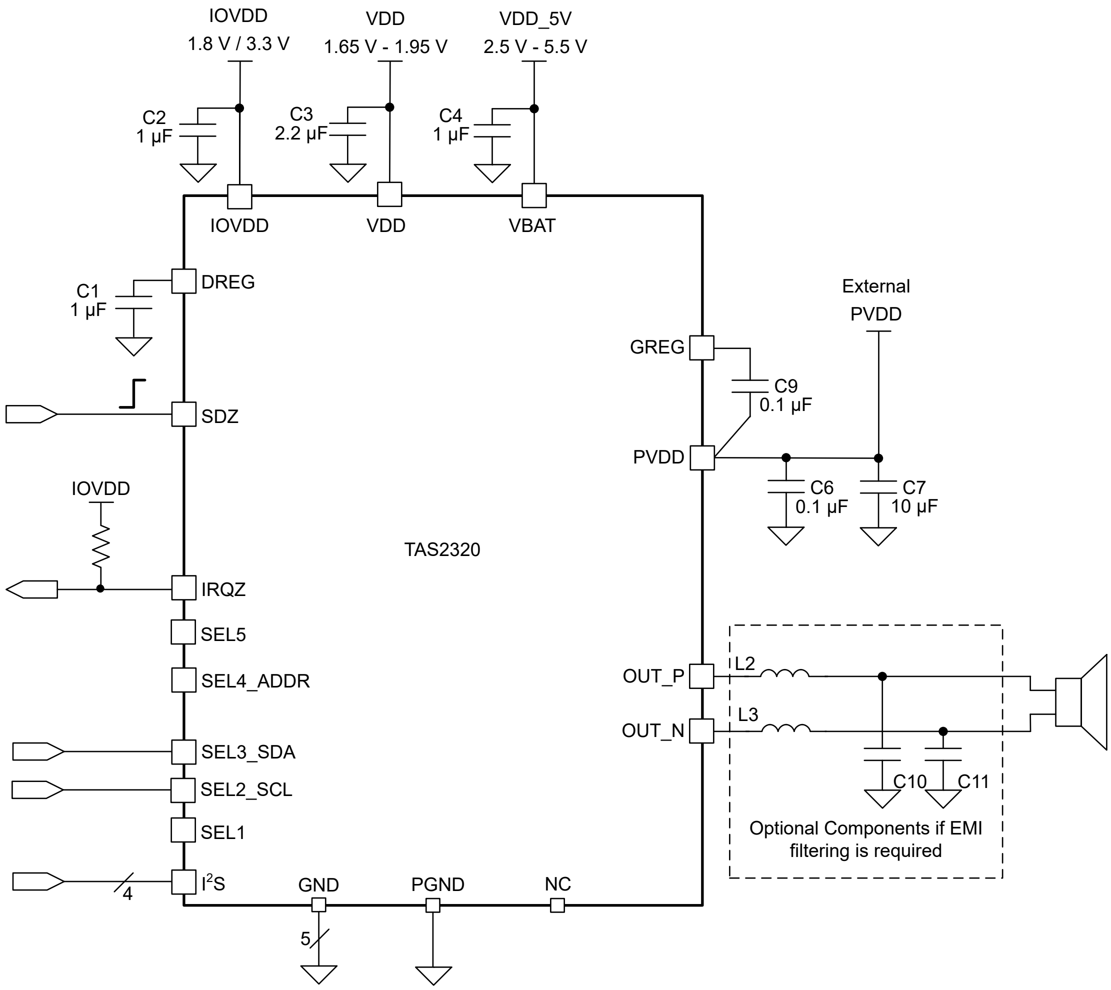

Figure 7-1. Application Diagram for External PVDD or 3S Battery system

ADVANCE INFORMATION

ADVANCE INFORMATION

Table 7-1. Recommended External Components

Component	Description	Specification	Min	Typ	Max	Unit
L2, L3	Optional EMI Filter Inductors (must use C10, C11 if L2, L3 are used)	DC Current	2			A
C1, C2	DREG, IOVDD decap	Capacitance, 20% tolerance		1		µF
		Voltage rating	2	6.3		V
C3	VDD decap	Capacitance, 20% tolerance		2.2		µF
		Voltage rating	2	6.3		V
C4	VBAT decap	Capacitance, 20% tolerance		1		µF
		Voltage rating	6.3	10		V
C6	PVDD Low ESL decap	Capacitance, 20% tolerance		0.1		µF
		Voltage rating	16	25		V
C7	PVDD Power decap	Capacitance, 20% tolerance		10		µF
		Voltage rating	16	25		V
C9	GREG decap	Capacitance, 20% tolerance		0.1		µF
		Voltage rating	6.3	10		V
C10, C11	Optional EMI Filter capacitors (must use L2, L3 if C10, C11 are used)	Voltage rating	2xPVDD			V

7.2.1 Design Requirements

Table 7-1 lists the BOM components required for the application. Table 7-2 lists other requirements for the application.

Table 7-2. Design Parameters

PARAMETER	CONDITION	SPECIFICATION
VDD supply current(1)	VDD Y-bridge disabled, 48ksps mode, all blocks enabled	< 15mA
	VDD Y-bridge disabled, 96ksps mode, all blocks enabled	< 20mA
IOVDD supply current	1.8V mode	< 1mA
	3.3V mode	< 1mA
VBAT supply current	< 10mA	

(1) When VDD Y-bridge is enabled, additional power taken from VDD supply based on the selected switchover threshold voltage and the output load impedance.

7.2.2 Detailed Design Procedure

(2)

7.2.2.1 Mono/Stereo Configuration

In this application, the device is assumed to be operating in mono mode. See Section 6.5.2 for information on changing the I^2C address of the TAS2320 to support stereo or multi-channel operation. Mono or stereo configuration does not impact the device performance.

7.2.2.2 EMI Passive Devices

The TAS2320 supports edge-rate control to minimize EMI, but the system designer may want to include passive devices on the Class-D output for further reduction in EMI . These passive devices that are labeled L2, L3, C10 and C11 in Section 7.2. If C10 and C11 are used, L2 and L3 must also be installed, and C10 and C11 must be placed after L2 and L3 respectively to maintain the stability of the output stage.

The component value selection for the EMI filters depends on the application need on the frequency band that needs to be suppressed using these filters. Higher cutoff frequency helps in reducing the BOM size and reduces the switching power loss associated with the filters. Application should select the highest cutoff frequency filter which will meet the system's frequency suppression target to get better efficiency performance.

The DC resistance of the inductors or ferrite beads used in the EMI filters also plays a critical role in system efficiency. Lower resistance reduces power loss and helps in improving overall system efficiency. Based on available board space, smallest DC resistance components which meet the application needs will give better efficiency performance.

7.2.2.3 Miscellaneous Passive Devices

The GREG Capacitor requires 100 nF to meet Class-D power delivery and efficiency specs. For device functionality, the GREG capacitor should be kelvin/star connected to PVDD pin of the device.

In order to maintain the device performance and keep the supply ripple within the device specification, minimizing the parasitic inductance on supply/ground paths for decoupling capacitors is required. All supply decapacitors should be selected as smallest package footprint to minimize the ESL of the capacitors. The layout placement and routing of the capacitors is critical for minimizing the trace parasitic inductance. Refer to Layout section (Section 9.1) to get detailed recommendations.

7.2.3 Application Performance Plots

T_A = 25 °C, VBAT = 3.6 V, VDD=1.8 V, IOVDD=1.8 V, Load = 8 Ω + 33 μH, F_{IN} = 1kHz, Fs = 48 kHz, Gain = 21dBV, SDZ=1, Noise gate mode disabled, Measured on EVM with typical application use case (Section 7.2). Measured filter free with an Audio Precision with a 22Hz to 20kHz un-weighted bandwidth, unless otherwise noted.

ADVANCE INFORMATION

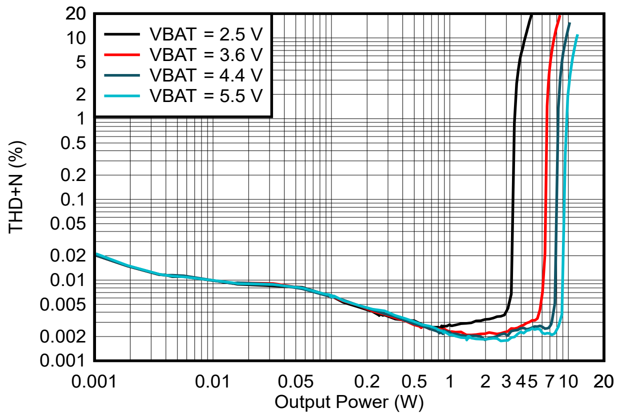

Figure 7-2. THDN vs Output Power

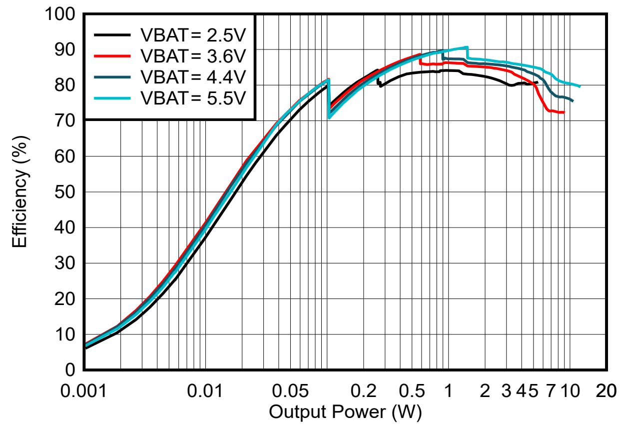

Figure 7-3. Efficiency vs Output Power

ADVANCE INFORMATION

8 Power Supply Recommendations

TAS2320 supports supply voltages to ramp up/down in any order of sequence for the externally supplied voltages on VDD, IOVDD, VBAT and PVDD(for external PVDD mode).

SDZ pin must be held low when supplies are not in stable operating condition. Once all the supplies are stable, SDZ pin can be asserted high for device to start operating. SDZ pin must be pulled low before any supply is ramped down below its recommended operating voltage.

If using the device in external PVDD mode, the SW pad must be kept floating.

Once all the supplies are valid and SDZ pin is released to high, the digital core voltage regulator powers up, and starts the internal initialization sequence. After a hardware or software reset, additional i2c commands to the device should be delayed by at-least 300us to allow the device internal blocks to be initialized.

9 Layout

9.1 Layout Guidelines

- Use wide traces for signals that carry high current and avoid VIAs wherever possible. If VIAs can't be avoided, multiple VIAs should be added to enable low parasitic inductance and high current capability. These include traces for PVDD, VBAT, VDD, PGND, GND, OUT_P and OUT_N.
- PGND and BGND signals should be directly connected and shorted to the ground plane of board to minimize parasitic inductance. Common inductance between ground pins (eg GND and PGND common routing) before connecting to ground plane should be avoided.
- The coupling between high switching signal traces like OUT_P, OUT_N, SW, should be avoided from sensitive low voltage signals.
- Minimize capacitance between high switching lines like OUT_P, OUT_N, SW, to ground/static nodes. Larger capacitance will result in efficiency drop. Coupling between OUT_P and OUT_N will also cause degraded efficiency.
- Decoupling capacitors should be placed close to the device. Smallest possible package size is recommended for the decaps to achieve best performance from device. DREG, VDD, IOVDD, VBAT (C4 cap), PVDD low ESL (C6 cap) are recommended to be 0201 case size or lower. VIAs between decapacitors and device pins should be avoided, or multiple VIAs added to minimize parasitic inductances.
- All decoupling capacitor's ground terminal should be strongly connected to the ground plane with multiple ground VIAs. The ground routing loop between the cap ground and the device ground pins should be minimized.
- For VDD Y-bridge functionality, the routing from the host PMIC to the device VDD should be wide supply plane trace with minimal routing parasitic inductance.
- For the capacitor between GREG-PVDD (C9 cap), PVDD side of capacitor should not be connected directly to the PVDD decoupling capacitors (C6, C7 and C8), and should be connected as close as possible to the device PVDD pin.

9.2 Layout Example

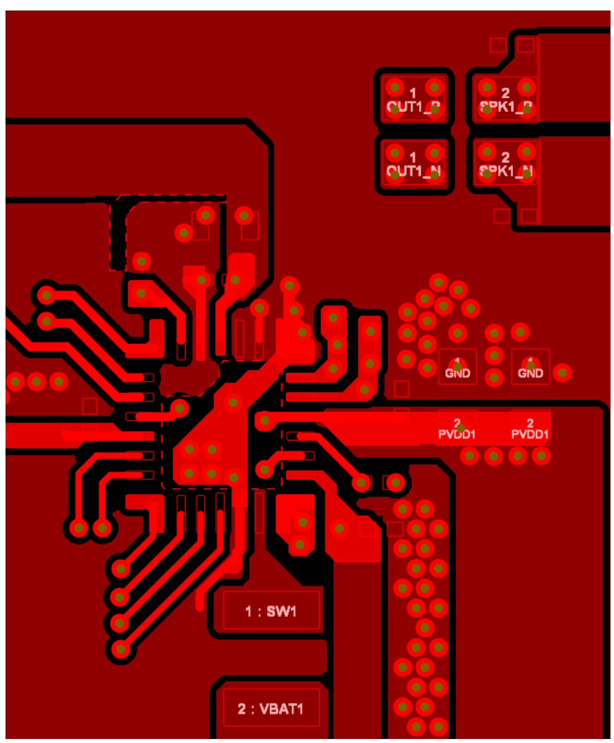

Figure 9-1. Example Layout Top

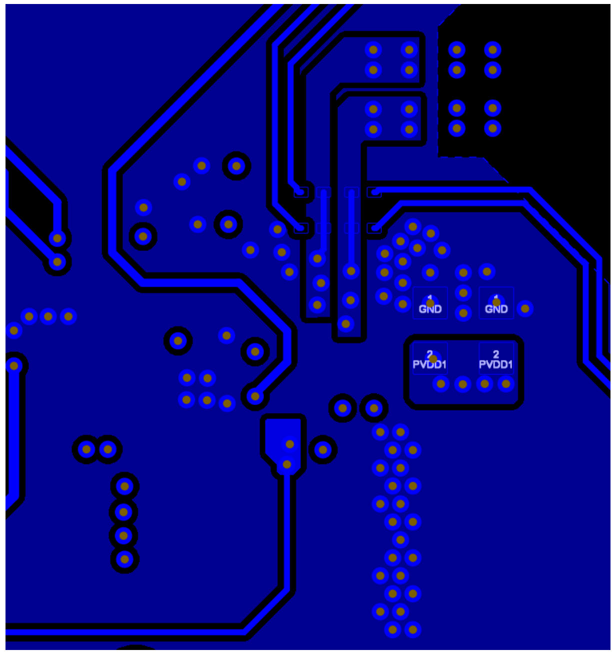

Figure 9-2. Example Layout Bottom

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documents see the following

- Texas Instruments, Purepath Console 3 (PPC3) Software

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

12.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PTAS2320RBGR	ACTIVE	VQFN-HR	RBG	26	3000	RoHS & Green	NiPdAu	Level-1-260C -UNLIM	-40 to 85	PTS2X20

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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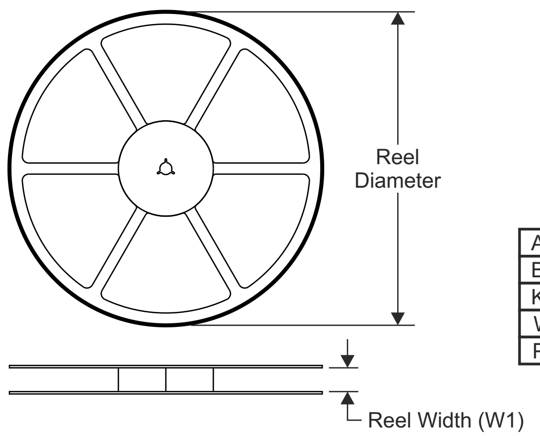
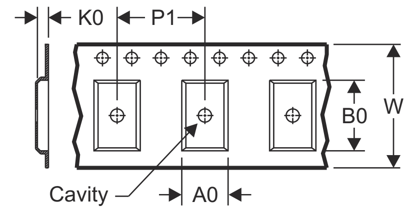
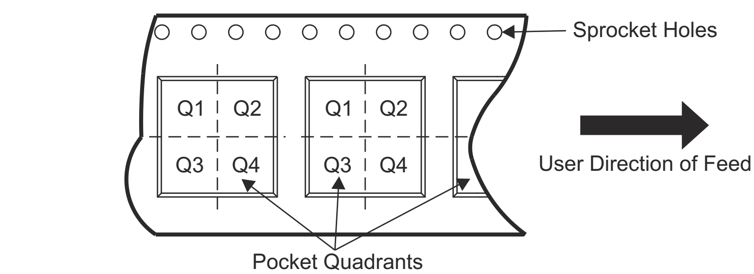
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

12.2 Tape and Reel Information



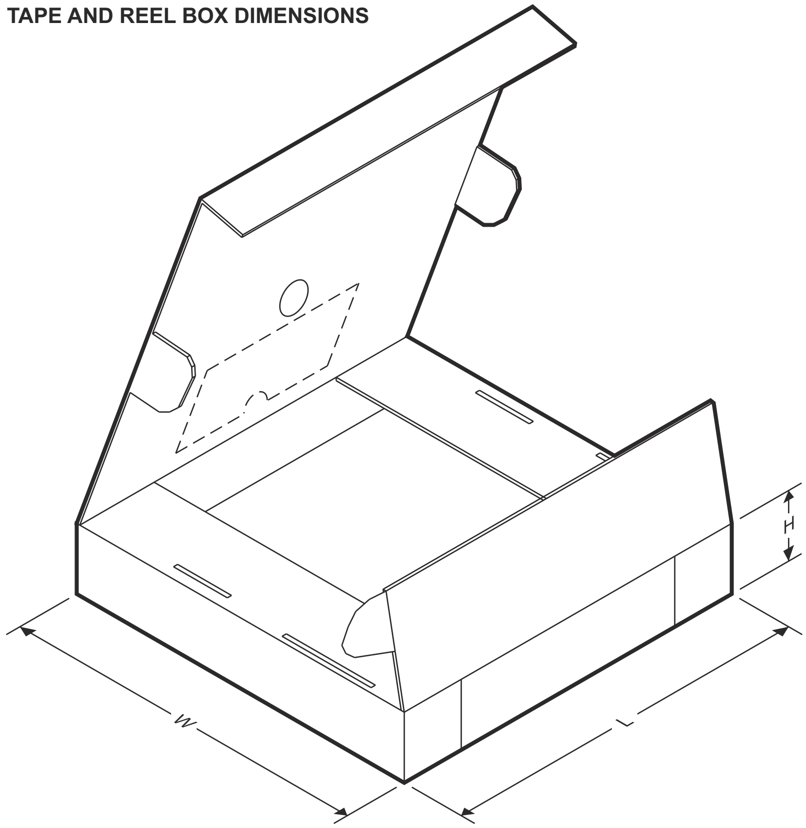


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTAS2320RBGR	VQFN-HR	RBG	26	3000	330	12.4	3.8	4.3	1.5	8	12	Q1

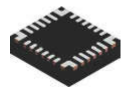
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTAS2320RBGR	VQFN-HR	RGB	26	3000	360.0	360.0	35

ADVANCE INFORMATION

ADVANCE INFORMATION

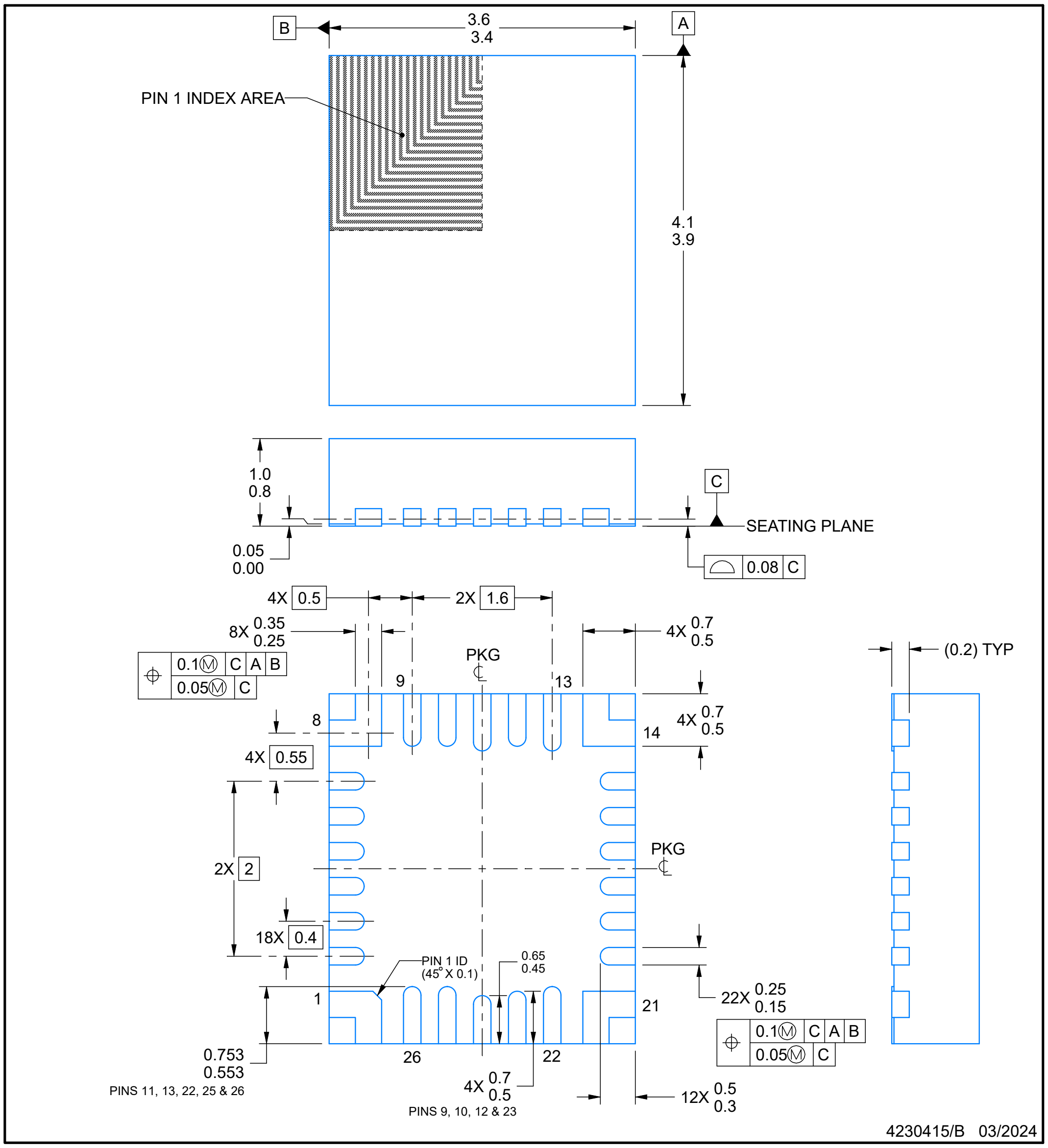


PACKAGE OUTLINE

RBG0026A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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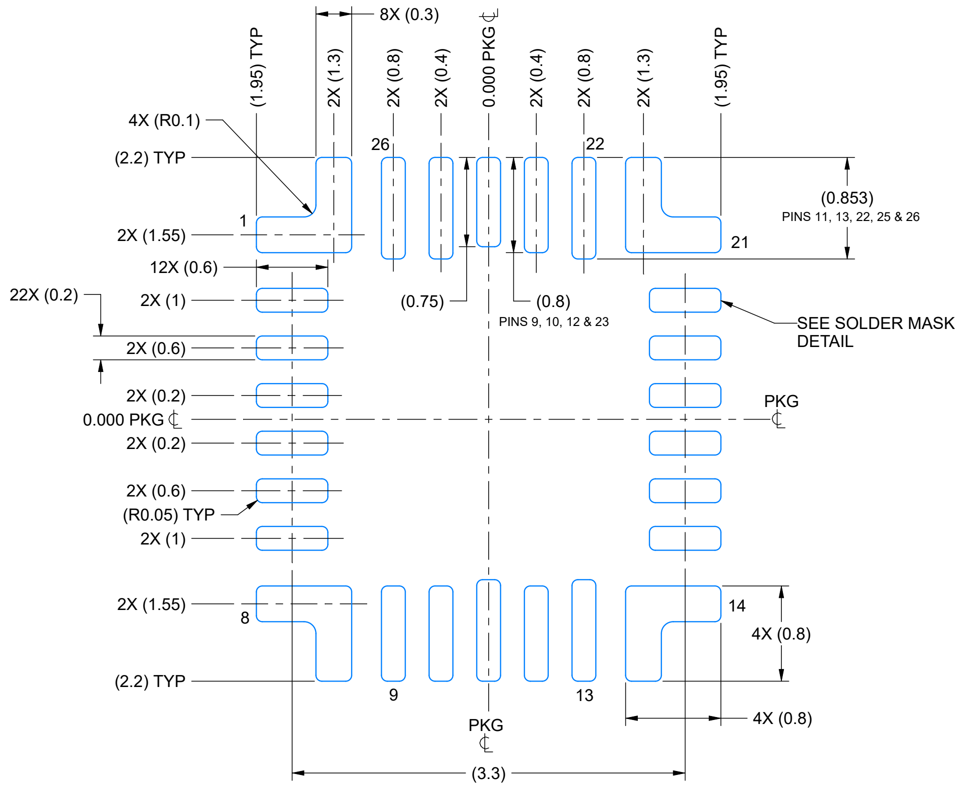
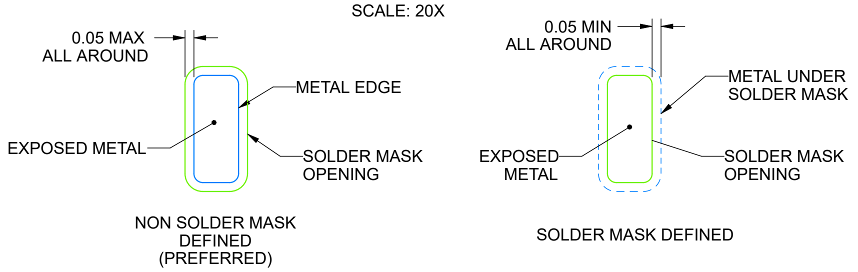
EXAMPLE BOARD LAYOUT

RBG0026A **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4230415/B 03/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

TEXAS INSTRUMENTS
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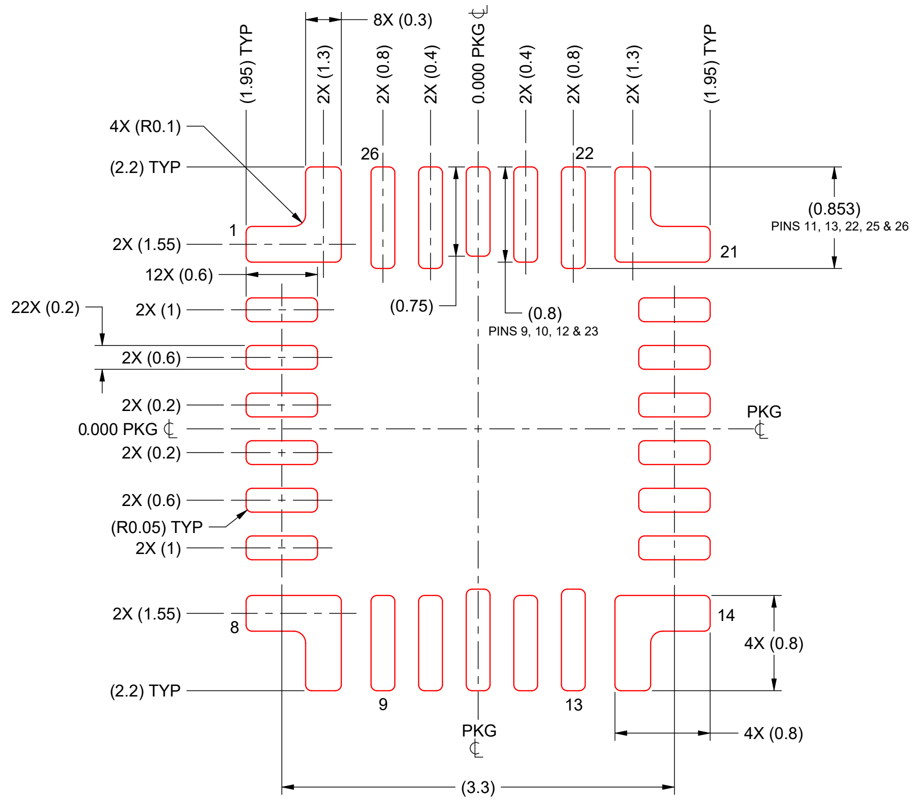
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RBG0026A **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 20X

4230415/B 03/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTAS2320RBGR	ACTIVE	VQFN-HR	RBG	26	3000	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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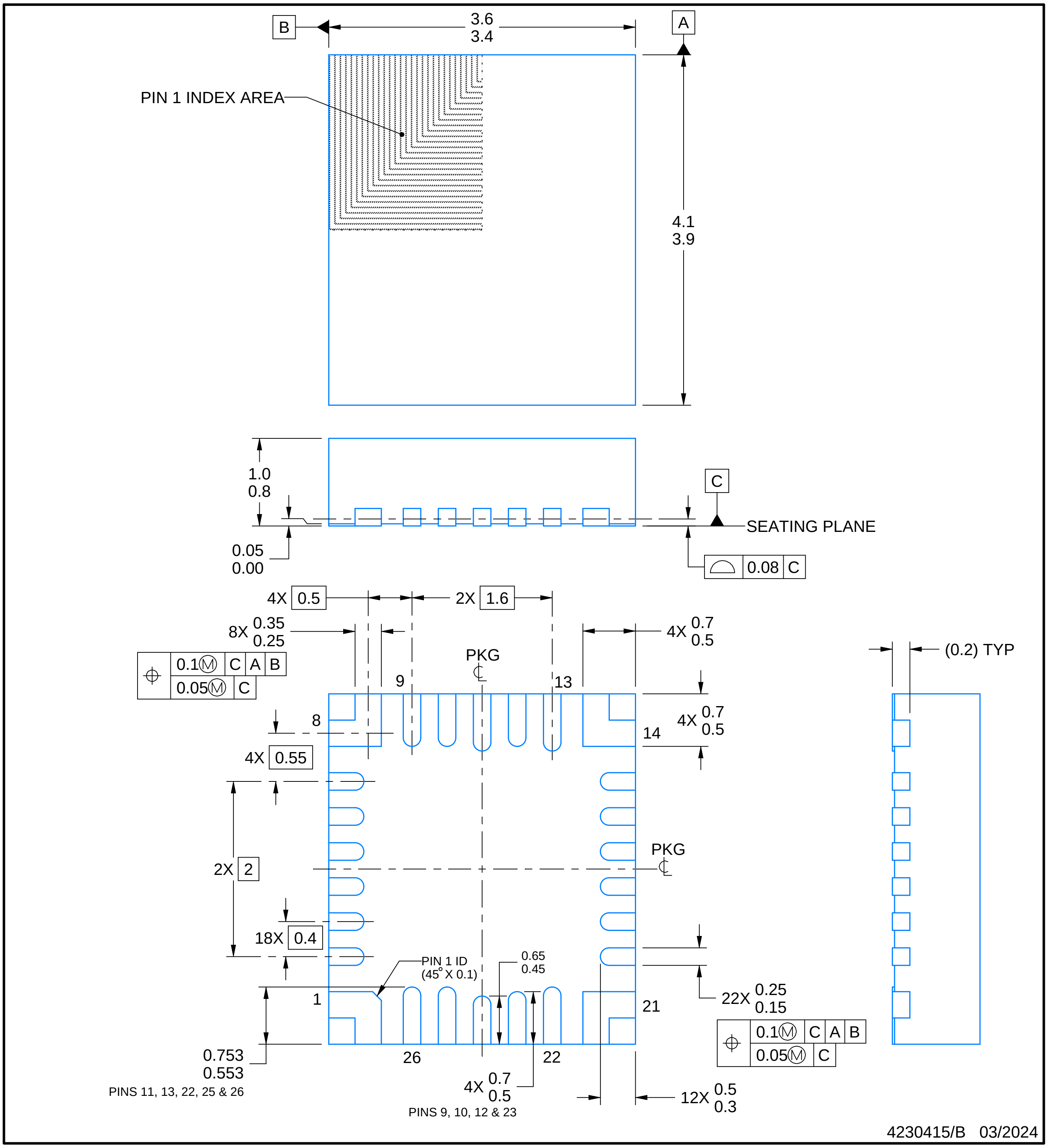
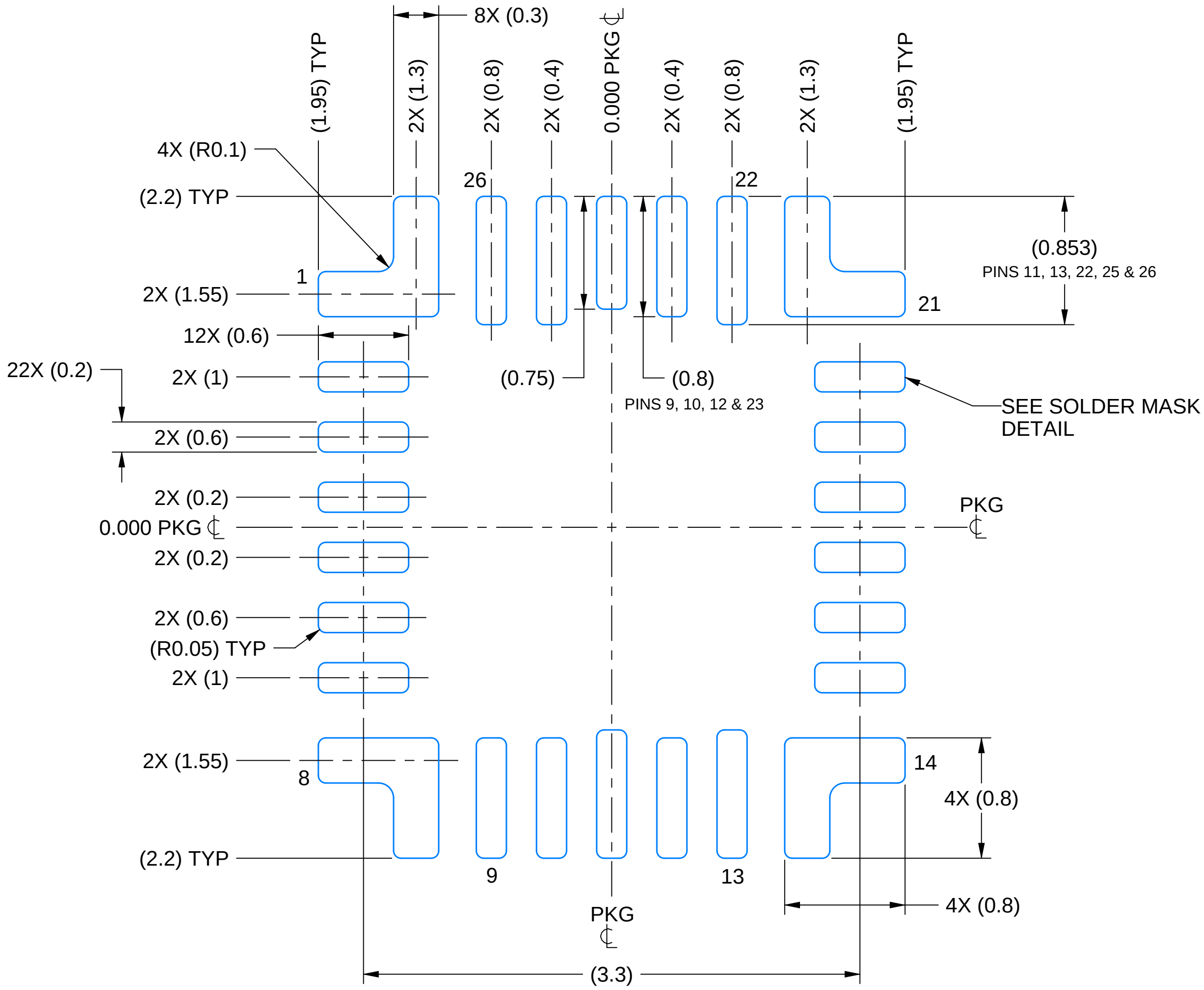
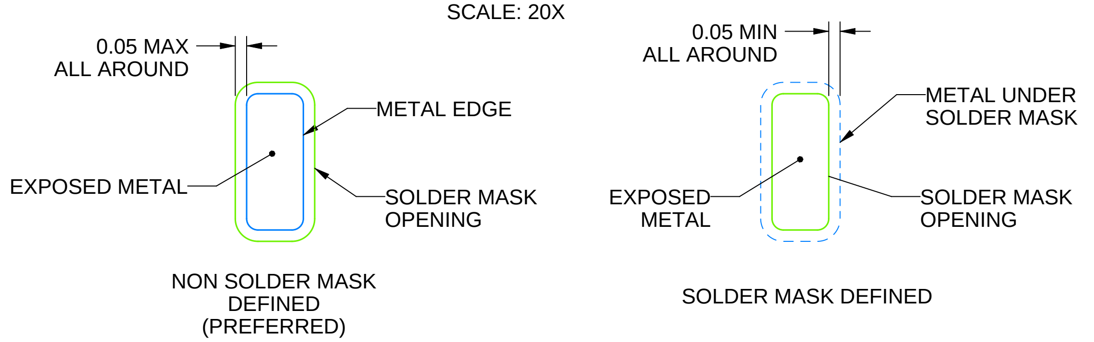


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

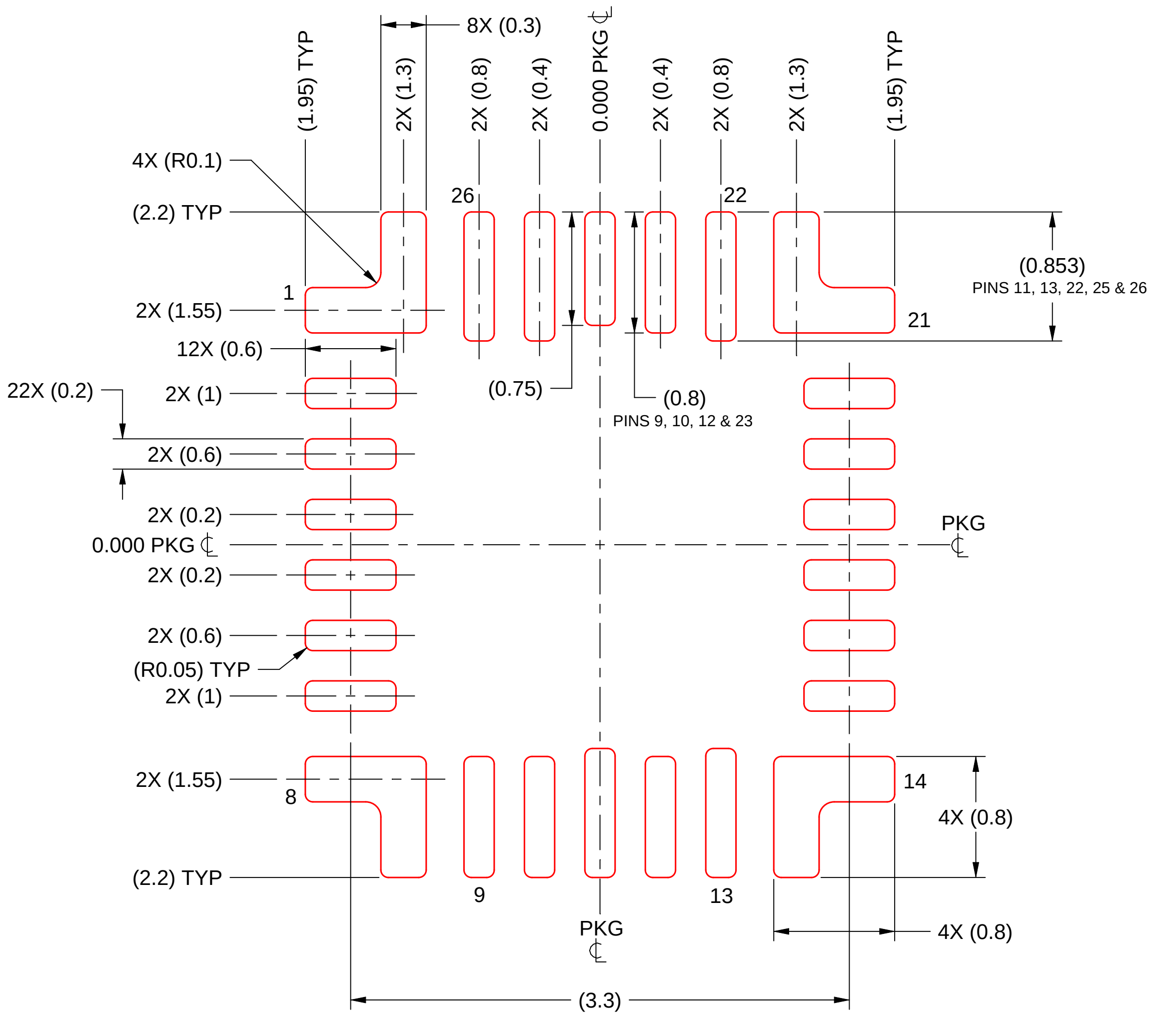


SOLDER MASK DETAILS

4230415/B 03/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 20X

4230415/B 03/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.