

TAS5802 22W Stereo, Inductor-Less, Digital Input, Closed-Loop Class-D Audio Amplifier with 96Khz Extended Processing and Low Idle Power Dissipation

1 Features

- Supports multiple output configurations
 - 2 × 22.7W, BTL mode(8Ω, 20V, THD+N=1%)
 - 2 × 28W, BTL mode(6Ω, 20V, THD+N=1%)
- Excellent audio performance:
 - 65uVrms Idle noise (typical)
 - THD+N ≤ 0.06% at 1W, 1kHz, PVDD = 12V
 - SNR ≥ 108dB (A-weighted)
- High-efficiency class-D and better thermal performance:
 - > 90% Power efficiency, 120mΩ R_{DS(on)}
- Flexible audio I/O:
 - I²S, LJ, RJ, TDM
 - Supports 32, 44.1, 48, 88.2, 96kHz sample rates
 - SDOUT for Audio monitoring, sub-channel, echo cancellation
 - Supports stereo bridge-tied (BTL)
- Enhanced audio processing
 - Multi-band advanced DRC+AGL
 - 2×15 BQs with smart EQ
 - Dynamic EQ and smart bass
 - DC Blocking
- Excellent power consumption profile:
 - Non-latching over-current error (OCE)
 - Enhanced over-temperature protection
 - Over-temperature warn (OTW)
 - Over-temperature error (OTE)
 - Under/over-voltage lock-out (UVLO/OVLO)
- Easy system integration
 - Flexible control strategy
 - Software control (full features)
 - Reduced solution size
 - Fewer passives required compare with open loop devices
 - Inductor-less operation (ferrite bead) for most cases where PVDD ≤ 12V

2 Applications

- [Sounds bars, PC audio](#)
- [Wireless, Bluetooth speakers](#)
- [DTV, HDTV, UHD and multi-purpose monitors](#)

3 Description

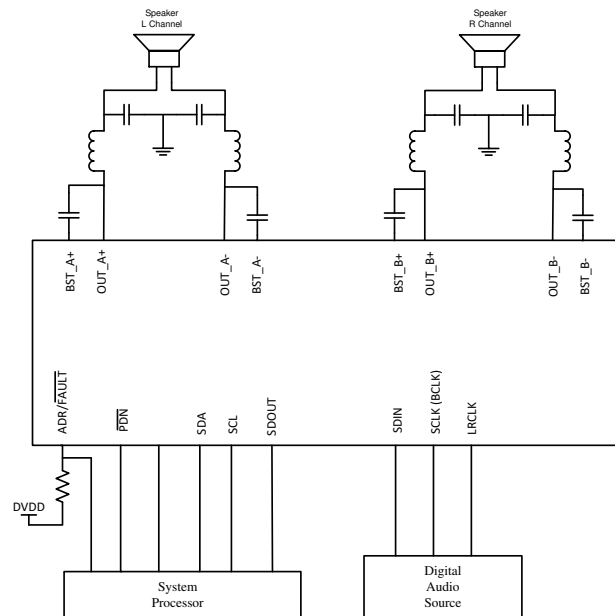
The TAS5802 is a 2×22 W digital input Class-D audio amplifier for driving loudspeakers used in consumer, commercial, and industrial electronics. The device is highly flexible, allowing operation with a range of control methods, power supply configurations, and audio I/O arrangements.

The TAS5802 high-performance closed-loop architecture and wide-switching frequency range reduce the solution size by reducing passive components and eliminating the inductor + capacitor (LC) filters in most applications. Advanced electromagnetic interference (EMI) reduction techniques allow excellent electromagnetic compliance (EMC) performance, even when used with ferrite bead + capacitor (BC) filters. Several power consumption methods have been implemented to minimize idle power consumption (IPC).

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TAS5802PWP	TSSOP (28) PWP	9.7mm × 6.4mm

- (1) For all available packages, see [Section 11.2](#)
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



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Device Comparison Table

Part Number	Recommended PVDD Range	R _{DS(ON)} Option	Package	Class-H Algorithm Integrated
TAS5802	4.5V to 20V	120mΩ	TSSOP28(PWP)	No
TAS5815	4.5V to 26.4V	120mΩ	TSSOP28(PWP)	Yes
TAS5827	4.5V to 26.4V	70mΩ	QFN32(RHB)	Yes
TAS5825P	4.5V to 26.4V	90mΩ	QFN32(RHB)	Yes
TAS5828M	4.5V to 26.4V	90mΩ	TSSOP32(DAD)	Yes
TAS5822M	4.5V to 26.4V	90mΩ	HTSSOP38(DCP)	No
TAS5806M	4.5V to 26.4V	180mΩ	TSSOP38(DCP)	No
TAS5805M	4.5V to 26.4V	180mΩ	TSSOP28(PWP)	No

4 Pin Configuration and Functions

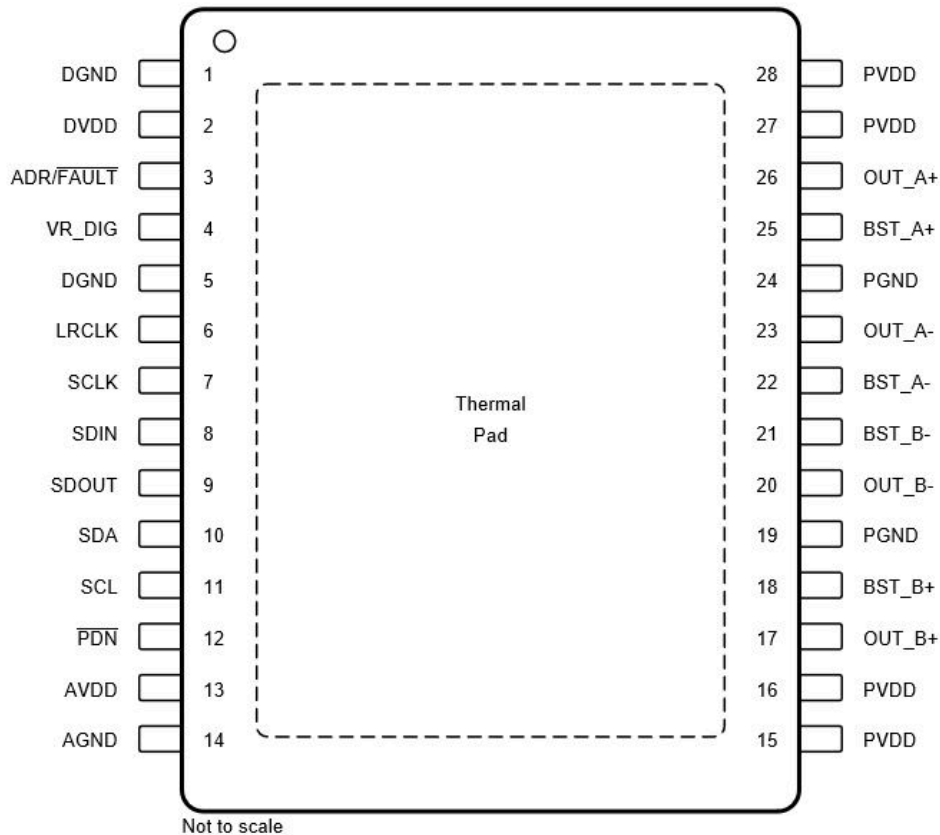


Figure 4-1. PWP (TSSOP) Package, 28-Pin PadDown, Top View

Table 4-1. Pin Functions For TSSOP28 Package

PIN NO.	NAME	TYPE ⁽¹⁾	DESCRIPTION
1	DGND	P	Digital ground
2	DVDD	P	3.3-V/1.8-V digital power supply
3	ADR/FAULT	DI/O	A table of resistor value (Pull up/Down to DVDD/GND) will decide device I2C address. After power up, this pin can be programmed by writing 1 to a register bit after Power up bit. In this mode, ADR/ FAULT is redefine as FAULT.

Table 4-1. Pin Functions For TSSOP28 Package (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
4	VR_DIG	P	Internally regulated 1.5-V digital supply voltage. This pin must not be used to drive external devices
5	DGND	P	Digital ground
6	LRCLK	DI	Input serial audio data left/right clock (sample rate clock)
7	SCLK	DI	Serial audio data clock (shift clock). SCLK is the serial audio port input data bit clock.
8	SDIN	DI	Serial audio data input. SDIN supports three discrete (stereo) data formats
9	SDOUT	DO	Serial audio data output, the source data can select as Pre-DSP or Post-DSP.
10	SDA	DI/O	I2C serial control data interface input/output
11	SCL	DI	I2C serial control clock input
12	PDN	DI	Power down, active-low. PDN sets the amplifier in Shutdown, turn off all internal regulators.
13	AVDD	P	Internally regulated 5 V analog power voltage. This pin must not be used to drive external devices.
14	AGND	G	Analog ground
15	PVDD	P	PVDD voltage input
16	PVDD	P	PVDD voltage input
17	OUT_B+	PO	Positive pin for differential speaker amplifier output B+
18	BST_B+	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+
19	PGND	G	Ground reference for power device circuitry. Connect this pin to system ground
20	OUT_B-	NO	Negative pin for differential speaker amplifier output B-
21	BST_B-	P	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-
22	BST_A-	P	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-
23	OUT_A-	NO	Negative pin for differential speaker amplifier output A-
24	PGND	G	Ground reference for power device circuitry. Connect this pin to system ground
25	BST_A+	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+
26	OUT_A+	PO	Positive pin for differential speaker amplifier output A+
27	PVDD	P	PVDD voltage input
28	PVDD	P	PVDD voltage input
	PowerPAD™	G	Ground, connect to grounded heat sink for best system performance.

- (1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), PO = Positive output, NO = Negative output, P = Power, G = Ground (0 V)

5 Specifications

5.1 Absolute Maximum Ratings

Free-air room temperature 25°C (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
DVDD	Low-voltage digital supply	-0.3	3.9	V
PVDD	PVDD supply	-0.3	23	V
V _{I(DigIn)}	DVDD referenced digital inputs ⁽²⁾	-0.5	V _{DVDD} + 0.5	V
V _{I(SPK_OUTxx)}	Voltage at speaker output pins	-0.3	25	V
T _A	Ambient operating temperature,	-40	85	°C
T _J	Operating junction temperature	-40	160	°C
T _{stg}	Storage temperature	-40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) DVDD referenced digital pins include: ADR/~~FAULT~~, LRCLK, SCLK, SDIN, SDOUT, SCL, SDA, ~~PDN~~

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted) see ⁽¹⁾

			MIN	NOM	MAX	UNIT
V _(POWER)	Power supply inputs	DVDD	1.62		3.63	V
		PVDD	4.5		20	
V _{IH(DigIn)}	Input logic high for DVDD referenced digital inputs		0.9 × V _{DVDD}		DVDD	V
V _{IL(DigIn)}	Input logic low for DVDD referenced digital inputs				0.1 × V _{DVDD}	V
L _{OUT}	Minimum inductor value in LC filter under short-circuit condition		1			μH

- (1) The Max Recommended PVDD value is limited by OCE_{THRES}.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TAS5802 TSSOP28 (PWP) 28 PINS	UNIT
		JEDEC STANDARD 4-LAYER PCB	
R _{θJA}	Junction-to-ambient thermal resistance	27.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	19.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	7.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	7.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	1.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

Free-air room temperature 25°C, 1SPW Mode, LC filter=4.7uH+0.68uF, Fsw=768kHz, Class D Bandwidth=175kHz, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
Digital I/O							
V(DVDD_DigON)	Input DVDD voltage to start I/O logic and digital core block ⁽¹⁾	VPDN > 0.7 x DVDD, PVDD > 4.5V		1.1	1.5	V	
IIH	Input logic high current level for DVDD referenced digital input pins	VIN(DigIn) = VD _{VDD}			10	uA	
IIL	Input logic low current level for DVDD referenced digital input pins	VIN(DigIn) = 0 V			-10	uA	
VIH(DigIn)	Input logic high threshold for DVDD referenced digital inputs			70%		VD _{VDD}	
VIL(DigIn)	Input logic low threshold for DVDD referenced digital inputs				30%	VD _{VDD}	
VOH(DigIn)	Output logic high voltage level	IOH = 4 mA		80%		VD _{VDD}	
VOL(DigIn)	Output logic low voltage level	IOH = -4 mA			20%	VD _{VDD}	
I²C CONTROL PORT							
CL(I2C)	Allowable load capacitance for each I ² C Line				400	pF	
fSCL(fast)	Support SCL frequency	No wait states, fast mode			400	kHz	
fSCL(slow)	Support SCL frequency	No wait states, slow mode			100	kHz	
SERIAL AUDIO PORT							
tDLY	Required LRCLK/FS to SCLK rising edge delay			5		ns	
DSCLK	Allowable SCLK duty cycle			40%	60%		
fS	Supported input sample rates			32	96	kHz	
fSCLK	Supported SCLK frequencies			32	64	f _s	
fSCLK	SCLK frequency				24.576	MHz	
AMPLIFIER OPERATING MODE AND DC PRAMETERS							
t _{off}	Turn-off Time	Excluding volume ramp			10	ms	
AV(SPK_AMP)	Programmable Gain	Value represents the "peak voltage" disregarding clipping due to lower PVDD Measured at 0 dB input(1FS)			29.4	dBV	
ΔAV(SPK_AMP)	Amplifier gain error	Gain = 26.4dBV			0.5	dB	
RDS(on)	Drain-to-source on resistance of the individual output MOSFETs	FET + Metallization. VPVDD=24V, I(OUT)=500mA, Tj=25°C			120	mΩ	
PROTECTION							
OCE _{THRES}	Over-Current Error Threshold	OUTxx Overcurrent Error Threshold			5	A	
UVE _{THRES} (PVDD)	PVDD under voltage error threshold condition 2			3.7	4	4.2	V
DCE _{THRES}	Output DC Error protection threshold	Class D Amplifier's output DC voltage cross speaker load to trigger Output DC Fault protection			1.9	V	
T _{DCDET}	Output DC Detect time	Class D Amplifier's output remain at or above DCE _{THRES}			570	ms	
OTE _{THRES}	Over temperature error threshold				160	°C	
OTE _{Hystersis}	Over temperature error hysteresis				10	°C	
OTW _{THRES}	Over temperature warning level	Read by register 0x73 bit3			135	°C	
AUDIO PERFORMACNE (STEREO BTL)							

Free-air room temperature 25°C, 1SPW Mode, LC filter=4.7uH+0.68uF, Fsw=768kHz, Class D Bandwidth=175kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OS}	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.4dBV analog gain, V _{PVDD} = 13.5 V	-6.5		6.5	mV
P _{O(SPK)}	Output Power (Per Channel)	V _{PVDD} = 13.5 V, R _{SPK} = 6 Ω, f = 1 kHz, THD+N = 10%		16		W
P _{O(SPK)}	Output Power (Per Channel)	V _{PVDD} = 13.5 V, R _{SPK} = 6 Ω, f = 1 kHz, THD+N = 1%		13		W
P _{O(SPK)}	Output Power (Per Channel)	V _{PVDD} = 18 V, R _{SPK} = 6 Ω, f = 1 kHz, THD+N = 10%		30		W
P _{O(SPK)}	Output Power (Per Channel)	V _{PVDD} = 18 V, R _{SPK} = 6 Ω, f = 1 kHz, THD+N = 1%		25		W
P _{O(SPK)}	Output Power (Per Channel)	V _{PVDD} = 20 V, R _{SPK} = 6 Ω, f = 1 kHz, THD+N = 10%		35		W
P _{O(SPK)}	Output Power (Per Channel)	V _{PVDD} = 20 V, R _{SPK} = 6 Ω, f = 1 kHz, THD+N = 1%		28		W
THD+N _{SPK}	Total harmonic distortion and noise (P _O = 1 W, f = 1 KHz, R _{SPK} = 6 Ω)	V _{PVDD} = 18 V		0.03		%
THD+N _{SPK}	Total harmonic distortion and noise (P _O = 1 W, f = 1 KHz, R _{SPK} = 6 Ω)	V _{PVDD} = 13.5 V		0.03		%
ICN _(SPK)	Idle channel noise(Aweighted, AES17)	V _{PVDD} = 13.5 V, LC-filter, Load=6 Ω		50		μVrms
		V _{PVDD} = 18 V, LC-filter, Load=6 Ω		60		μVrms
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, V _{PVDD} =18 V		109		dB
		A-Weighted, referenced to 1% THD+N Output Level, V _{PVDD} =13.5 V		106		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 kHz, 1 Vrms, V _{PVDD} = 13.5 V, input audio signal = digital zero		72		dB
X-talk _{SPK}	Cross-talk (worst case between left-to-right and right-to-left coupling)	f = 1 kHz, based on Inductor (DFEG7030D-4R7) from Murata		100		dB

- (1) For stable device operation, it is recommended to follow the given operating voltages and procedures outlined in “Startup Procedures” section.

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT	
Serial Audio Port Timing - Target Mode						
f_{SCLK}	SCLK frequency	1.024			MHz	
t_{SCLK}	SCLK period	40			ns	
t_{SCLKL}	SCLK pulse width, low	16			ns	
t_{SCLKH}	SCLK pulse width, high	16			ns	
t_{SL}	SCLK rising to LRCLK/FS edge	8			ns	
t_{LS}	LRCK/FS Edge to SCLK rising edge	8			ns	
t_{SU}	Data setup time, before SCLK rising edge	8			ns	
t_{DH}	Data hold time, after SCLK rising edge	8			ns	
t_{DFS}	Data delay time from SCLK falling edge	15			ns	
I²C Bus Timing – Standard						
f_{SCL}	SCL clock frequency	100			kHz	
t_{BUF}	Bus free time between a STOP and START condition	4.7			μ s	
t_{LOW}	Low period of the SCL clock	4.7			μ s	
t_{HI}	High period of the SCL clock	4			μ s	
t_{RS-SU}	Setup time for (repeated) START condition	4.7			μ s	
t_{S-HD}	Hold time for (repeated) START condition	4			μ s	
t_{D-SU}	Data setup time	250			ns	
t_{D-HD}	Data hold time	0			3450	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$			1000	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$			1000	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$			1000	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$			1000	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$			1000	ns
t_{P-SU}	Setup time for STOP condition	4			μ s	
C_B	Capacitive load for each bus line	400			pf	
I²C Bus Timing – Fast						
f_{SCL}	SCL clock frequency	400			kHz	
t_{BUF}	Bus free time between a STOP and START condition	1.3			μ s	
t_{LOW}	Low period of the SCL clock	1.3			μ s	
t_{HI}	High period of the SCL clock	600			ns	
t_{RS-SU}	Setup time for (repeated)START condition	600			ns	
t_{RS-HD}	Hold time for (repeated)START condition	600			ns	
t_{D-SU}	Data setup time	100			ns	
t_{D-HD}	Data hold time	0			900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$			300	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$			300	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$			300	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$			300	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$			300	ns
t_{P-SU}	Setup time for STOP condition	600			ns	
t_{SP}	Pulse width of spike suppressed	50			ns	
C_B	Capacitive load for each bus line	400			pf	

5.7 Typical Characteristics

5.7.1 Bridge Tied Load (BTL) Configuration Curves with 1SPW Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, 80 kHz Class D Loop Bandwidth, the LC filter used was 10 µH / 0.68 µF, unless otherwise noted.

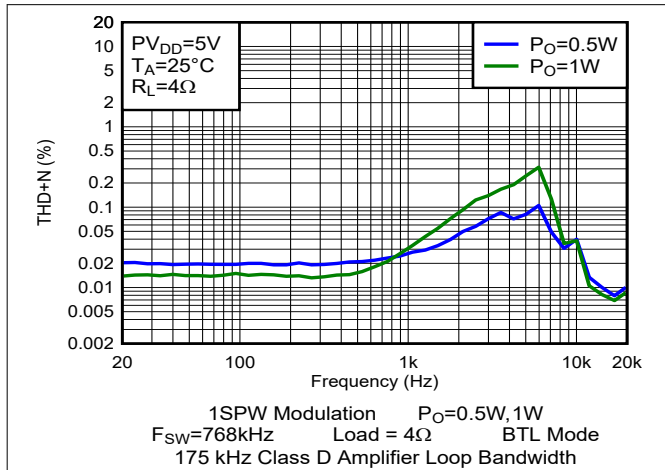


Figure 5-1. THD+N vs Frequency

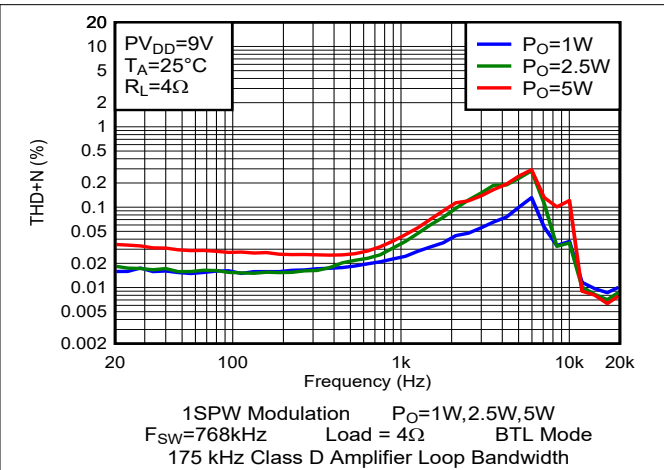


Figure 5-2. THD+N vs Frequency

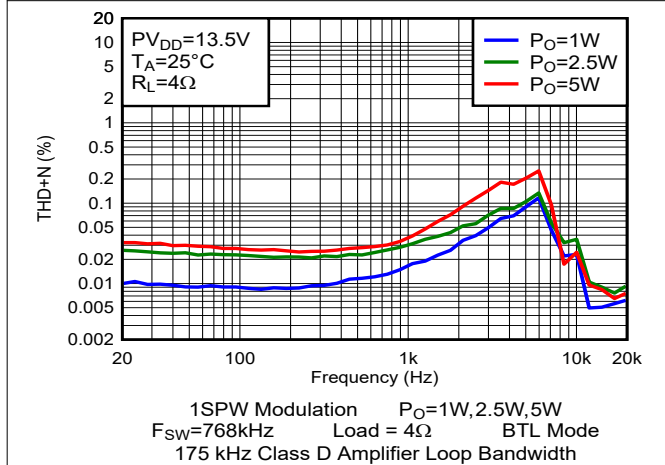


Figure 5-3. THD+N vs Frequency

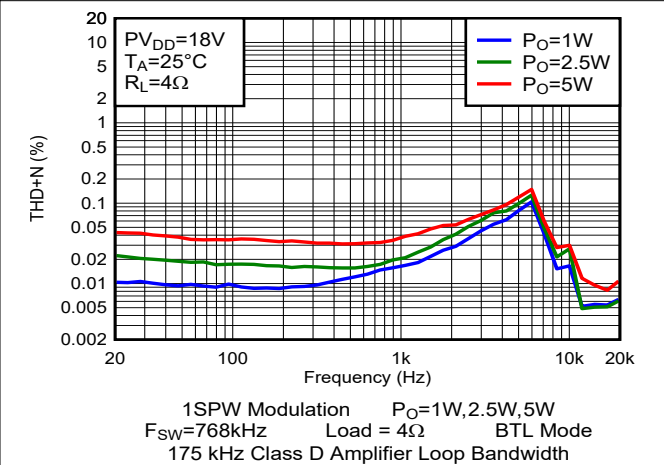


Figure 5-4. THD+N vs Frequency

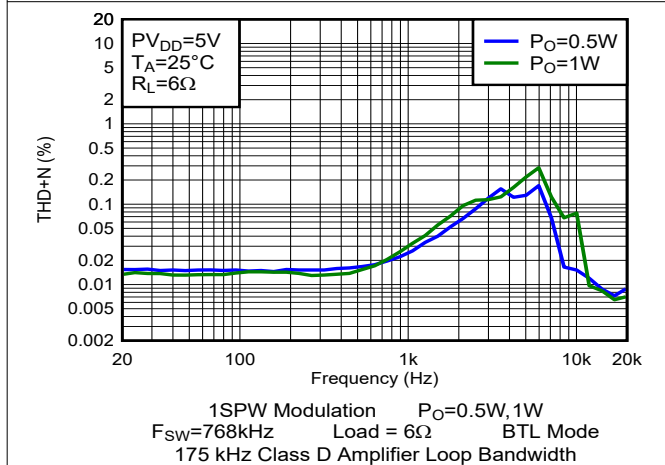


Figure 5-5. THD+N vs Frequency

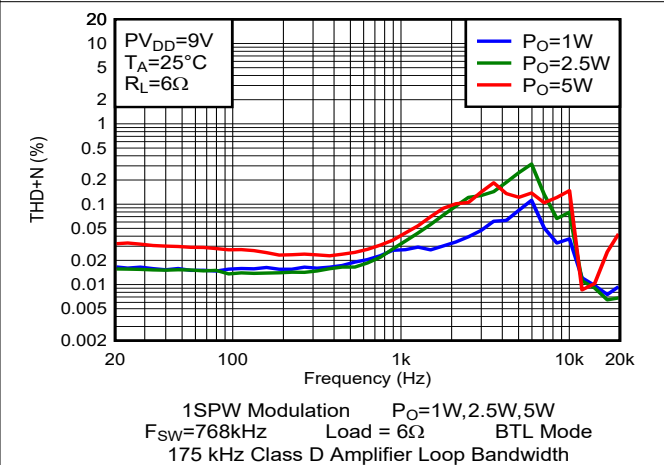


Figure 5-6. THD+N vs Frequency

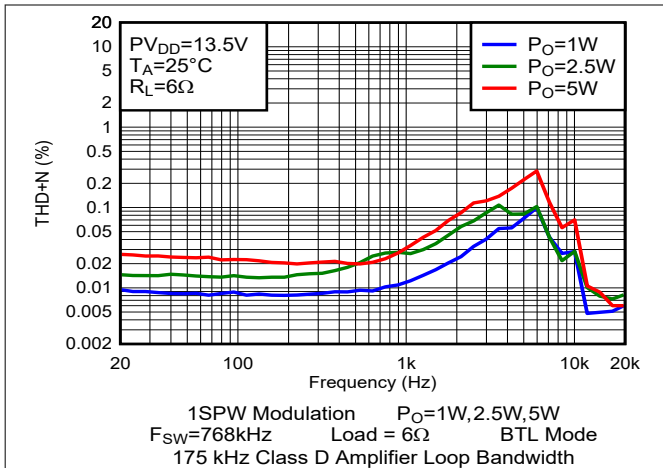


Figure 5-7. THD+N vs Frequency

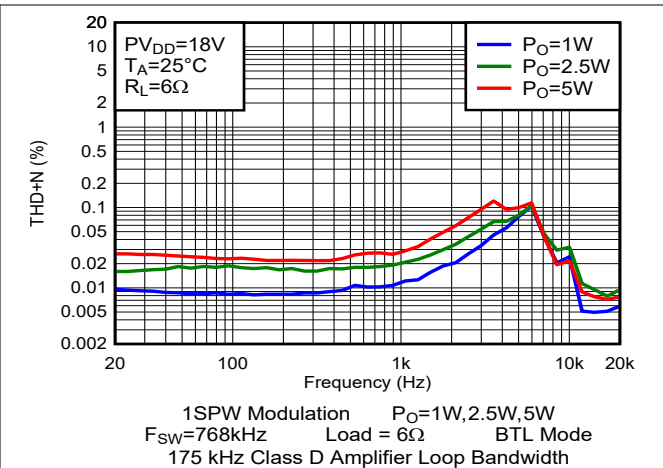


Figure 5-8. THD+N vs Frequency

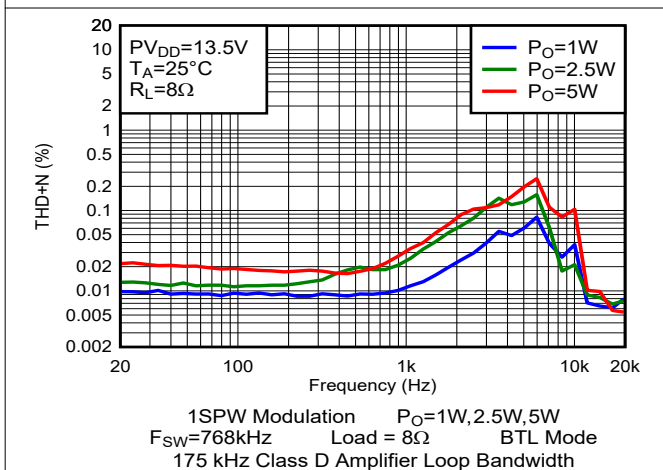


Figure 5-9. THD+N vs Frequency

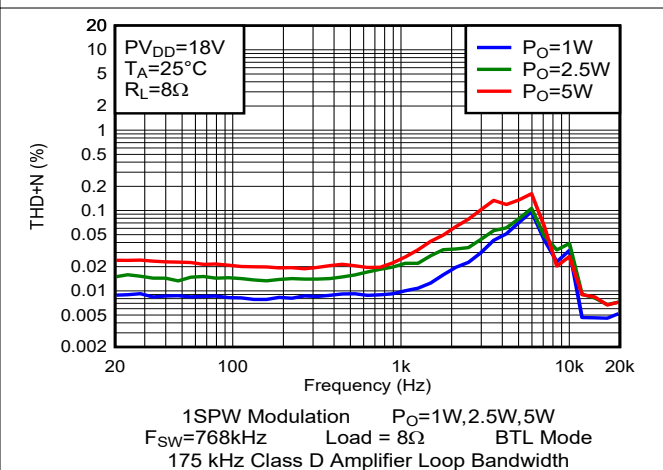


Figure 5-10. THD+N vs Frequency

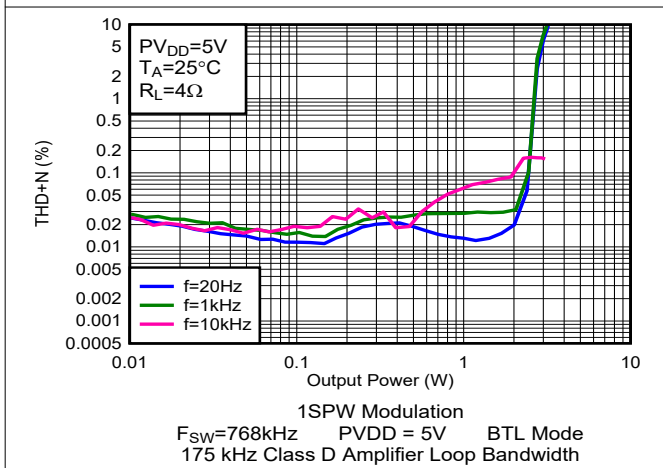


Figure 5-11. THD+N vs Output Power

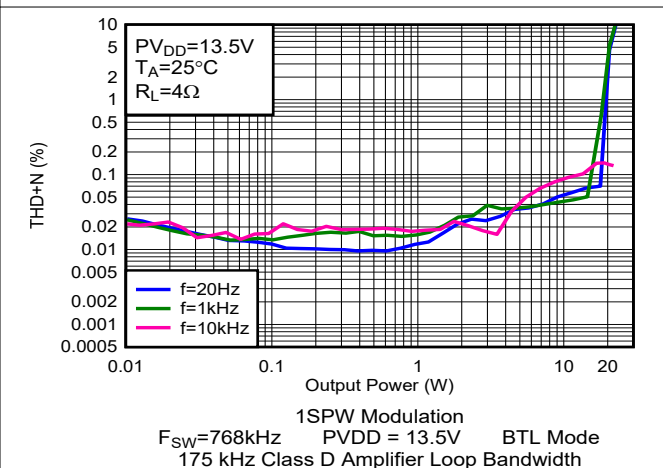


Figure 5-12. THD+N vs Output Power

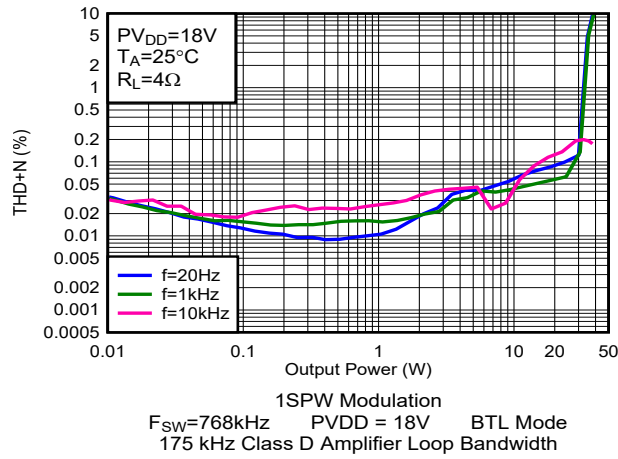


Figure 5-13. THD+N vs Output Power

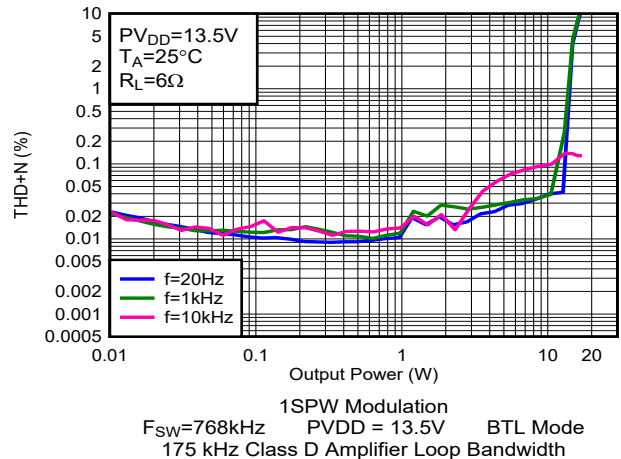


Figure 5-14. THD+N vs Output Power

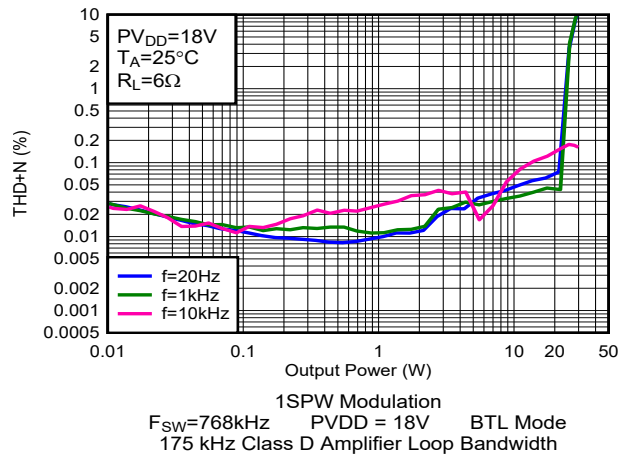


Figure 5-15. THD+N vs Output Power

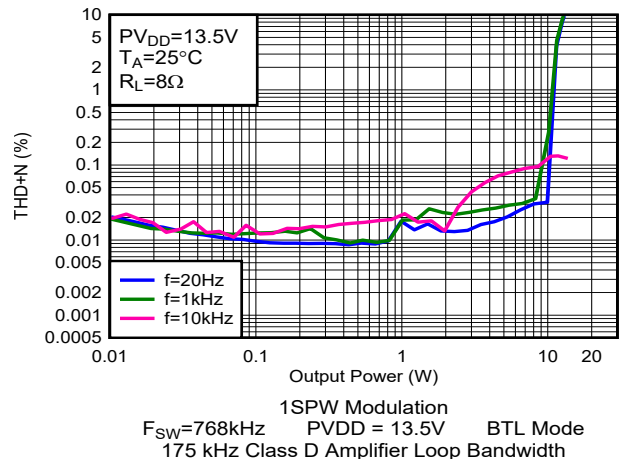


Figure 5-16. THD+N vs Output Power

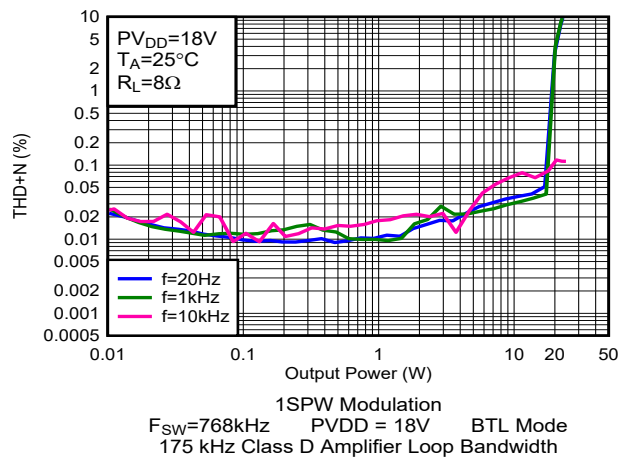


Figure 5-17. THD+N vs Output Power

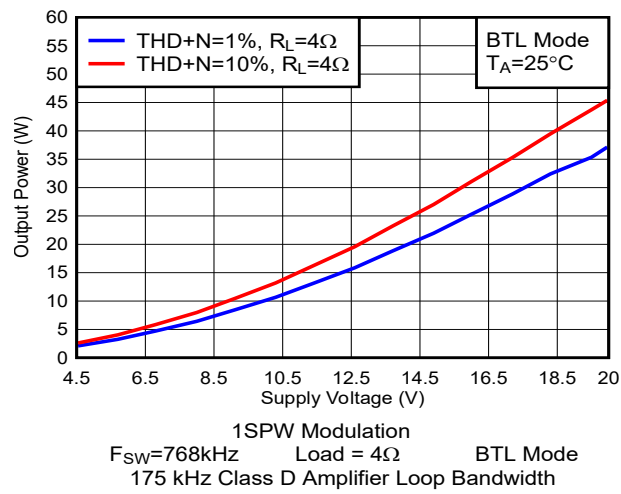
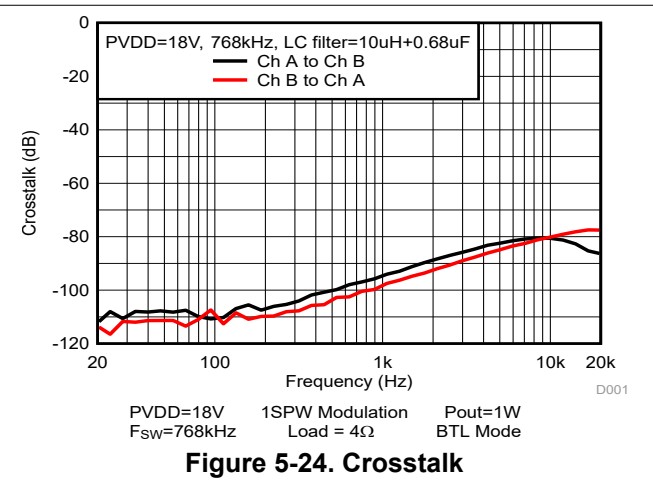
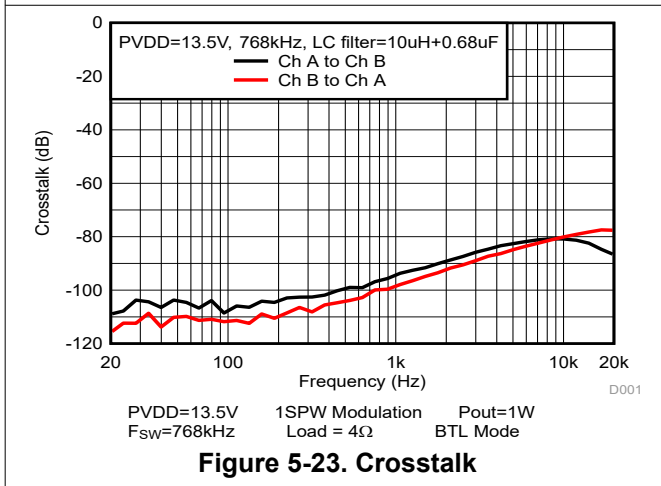
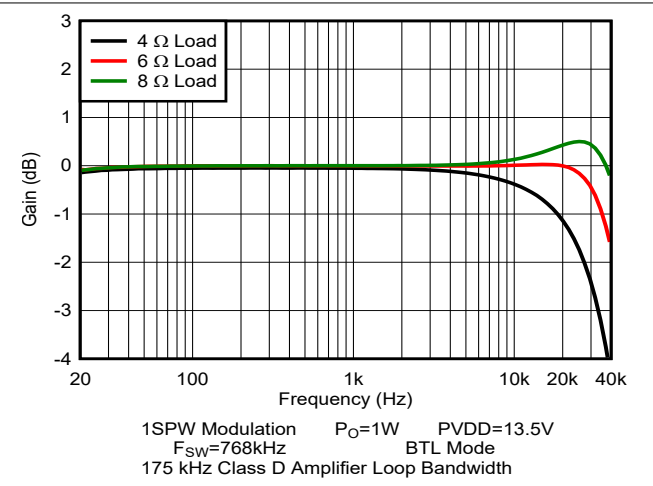
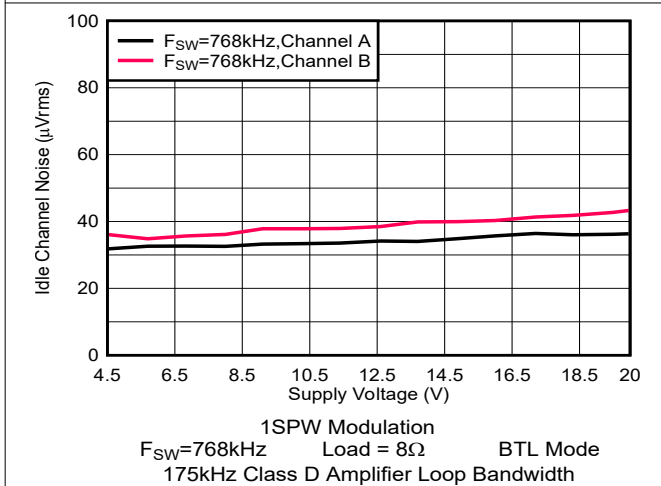
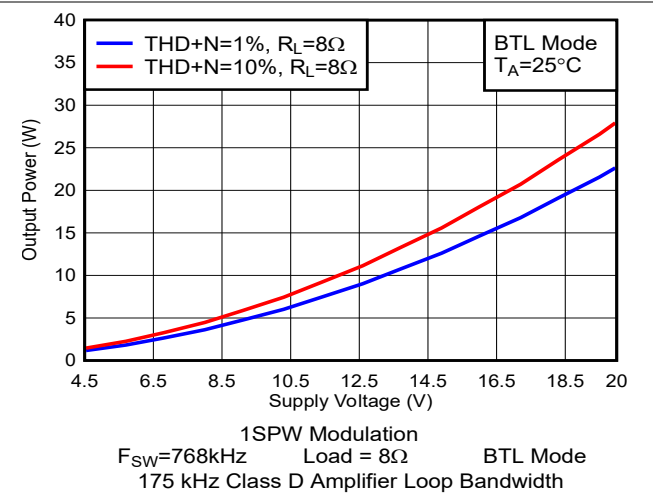
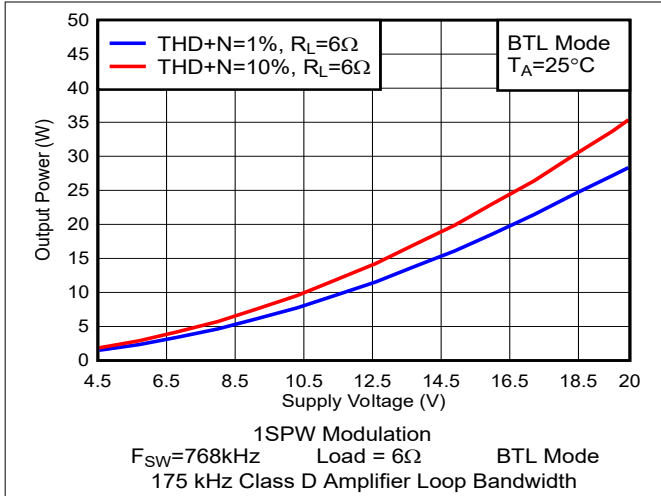
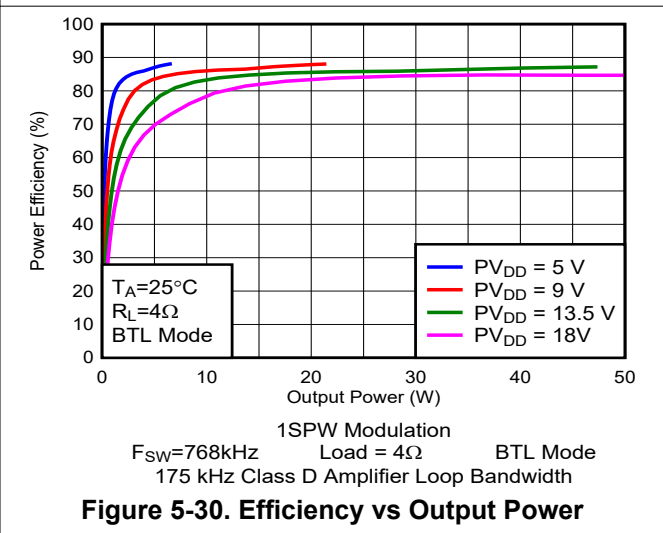
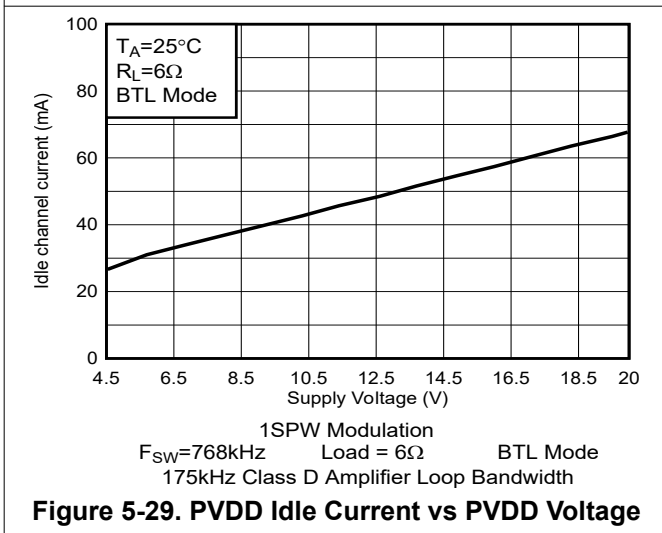
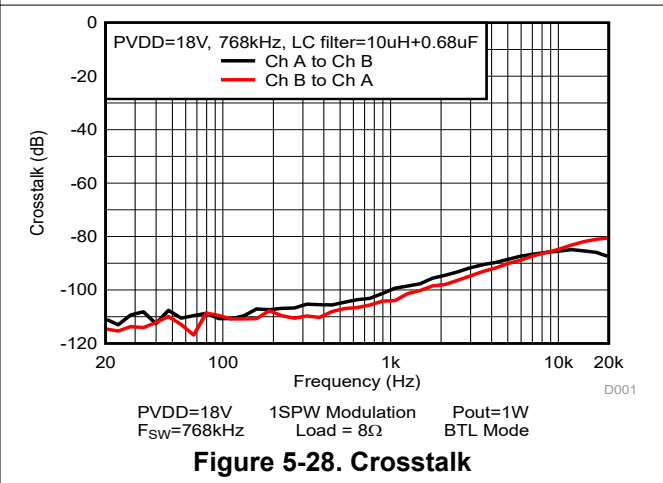
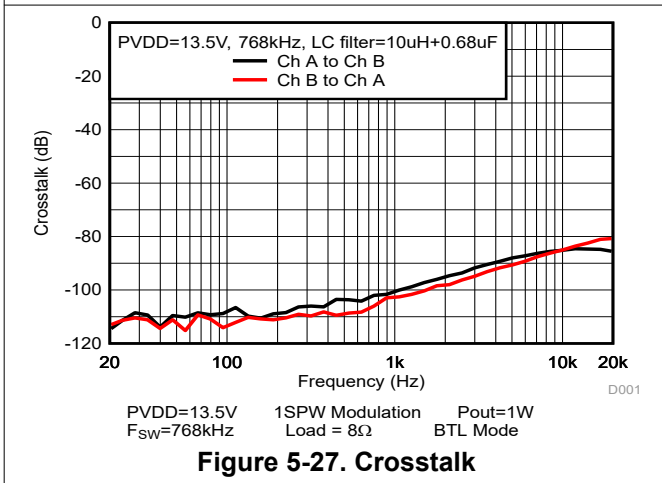
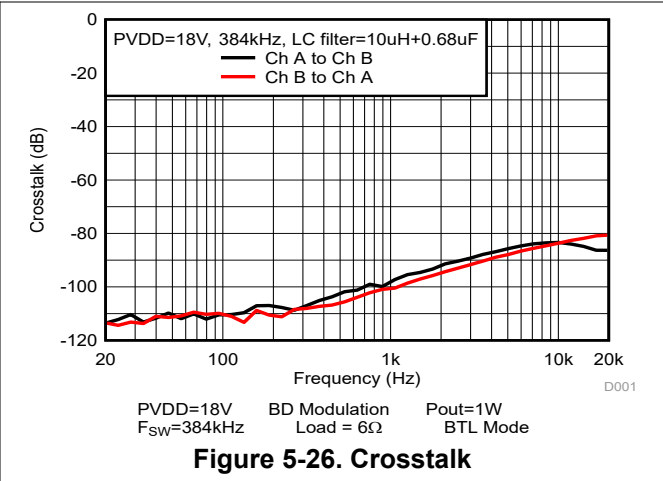
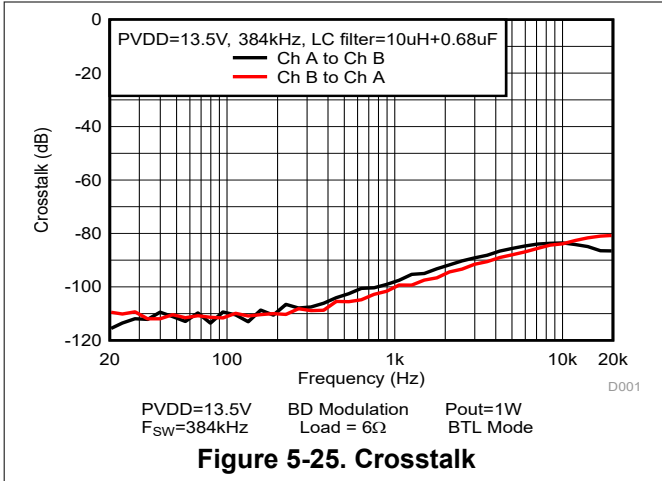
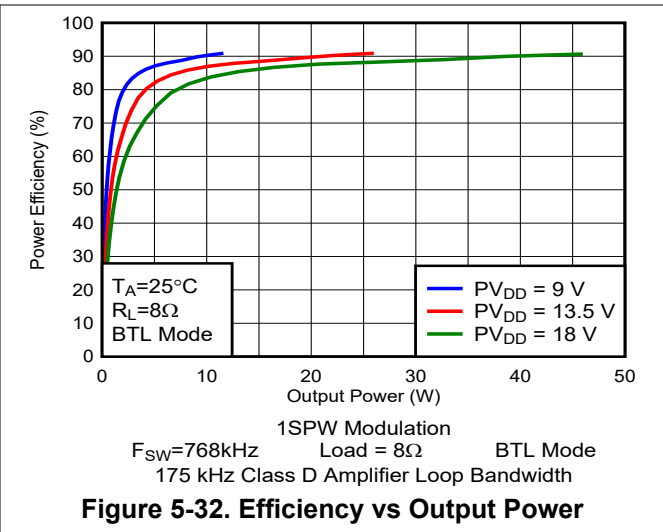
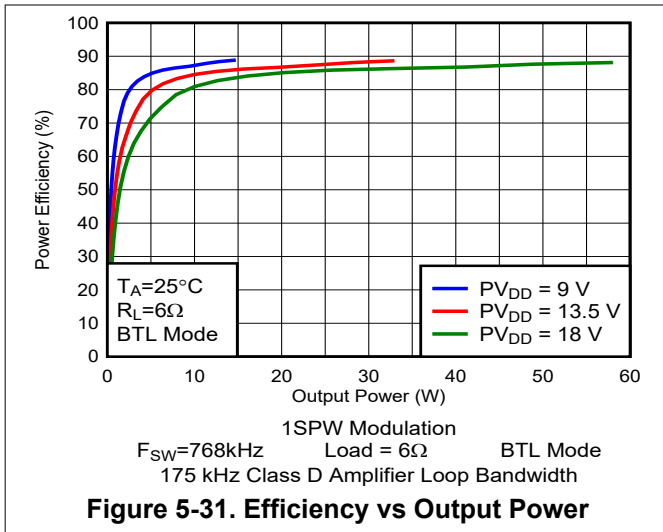


Figure 5-18. Output Power vs Supply Voltage

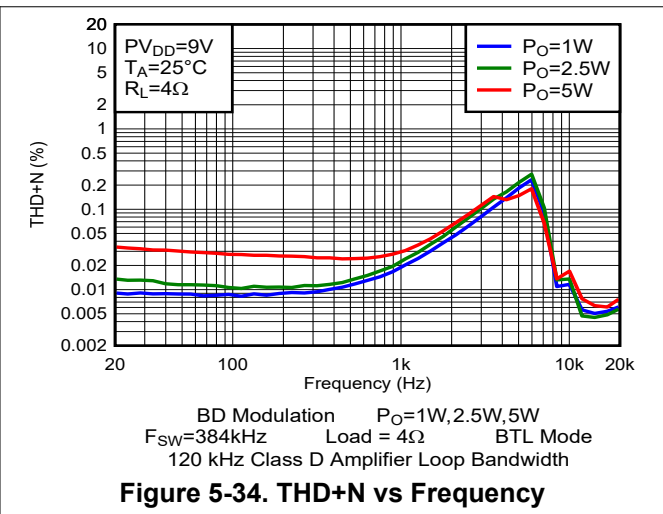
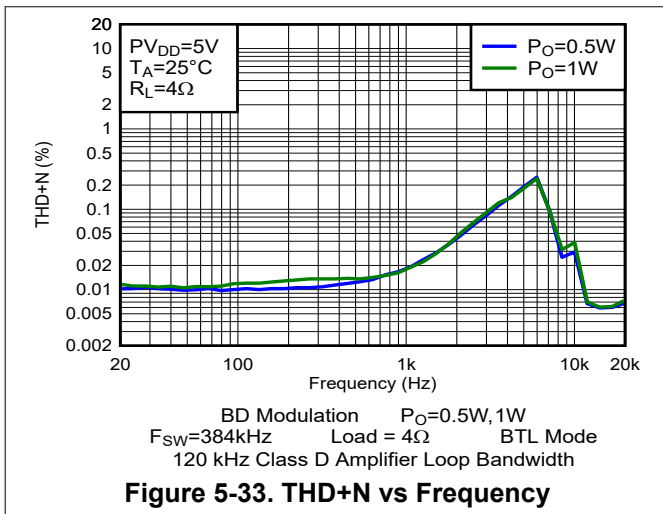


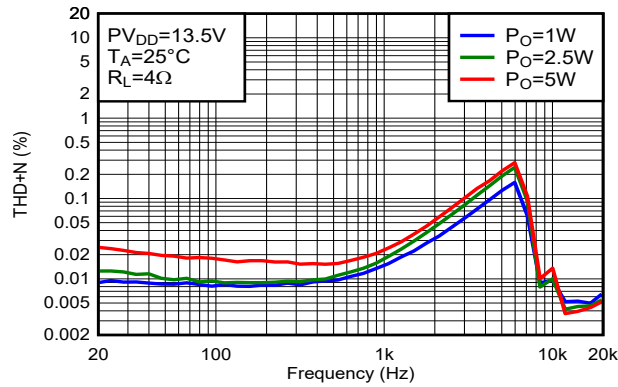




5.7.2 Bridge Tied Load (BTL) Configuration Curves with BD Modulation

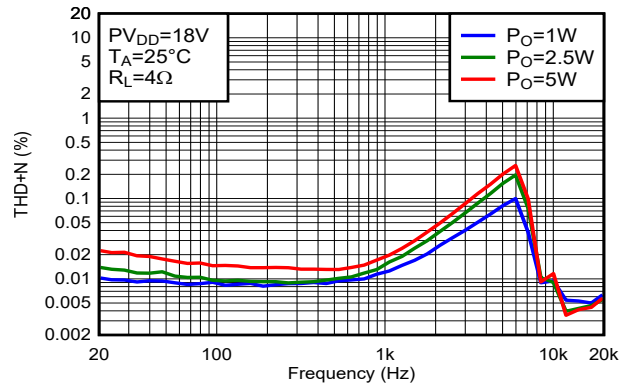
Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 576kHz, 175 kHz Class D Amplifier Loop Bandwidth, LC filter with 10μH / 0.68 μF, unless otherwise noted.





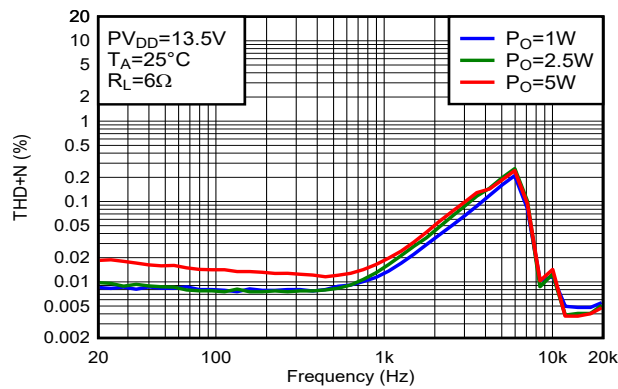
BD Modulation $P_O=1W, 2.5W, 5W$
 $F_{SW}=384kHz$ Load = 4Ω BTL Mode
 120 kHz Class D Amplifier Loop Bandwidth

Figure 5-35. THD+N vs Frequency



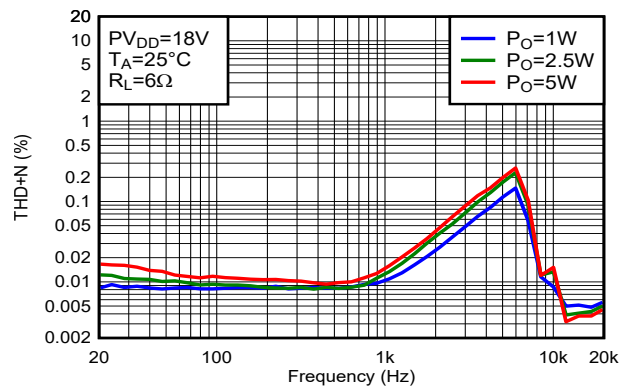
BD Modulation $P_O=1W, 2.5W, 5W$
 $F_{SW}=384kHz$ Load = 4Ω BTL Mode
 120 kHz Class D Amplifier Loop Bandwidth

Figure 5-36. THD+N vs Frequency



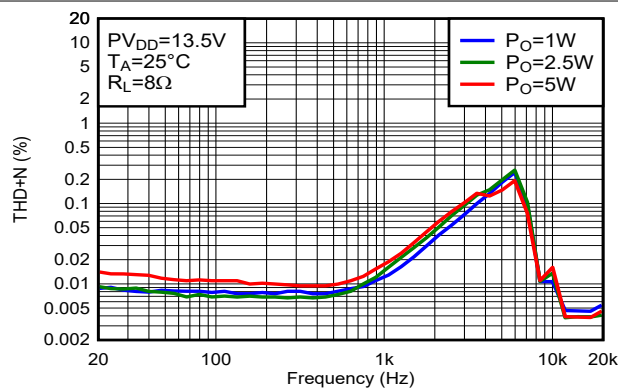
1SPW Modulation $P_O=1W, 2.5W, 5W$
 $F_{SW}=384kHz$ Load = 6Ω BTL Mode
 120 kHz Class D Amplifier Loop Bandwidth

Figure 5-37. THD+N vs Frequency



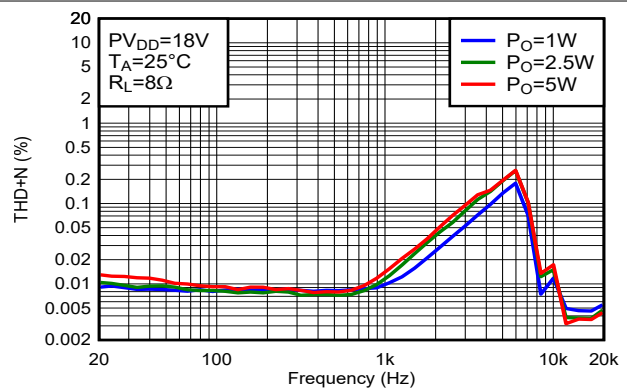
BD Modulation $P_O=1W, 2.5W, 5W$
 $F_{SW}=384kHz$ Load = 6Ω BTL Mode
 120 kHz Class D Amplifier Loop Bandwidth

Figure 5-38. THD+N vs Frequency



BD Modulation $P_O=1W, 2.5W, 5W$
 $F_{SW}=384kHz$ Load = 8Ω BTL Mode
 120 kHz Class D Amplifier Loop Bandwidth

Figure 5-39. THD+N vs Frequency



BD Modulation $P_O=1W, 2.5W, 5W$
 $F_{SW}=384kHz$ Load = 8Ω BTL Mode
 120 kHz Class D Amplifier Loop Bandwidth

Figure 5-40. THD+N vs Frequency

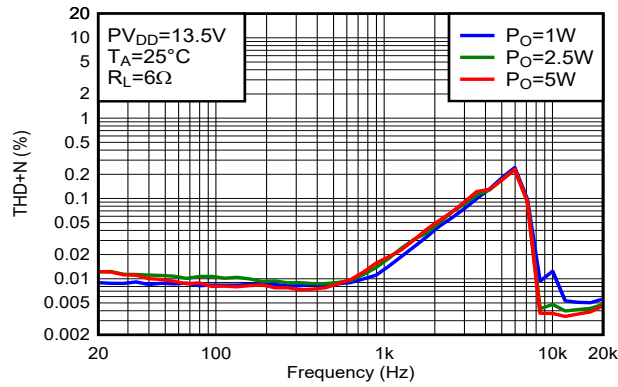


Figure 5-41. THD+N vs Frequency

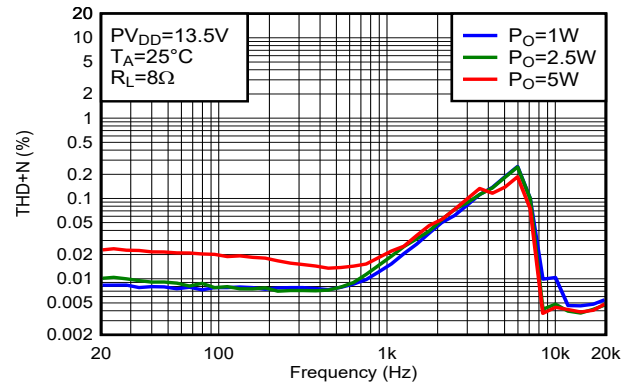


Figure 5-42. THD+N vs Frequency

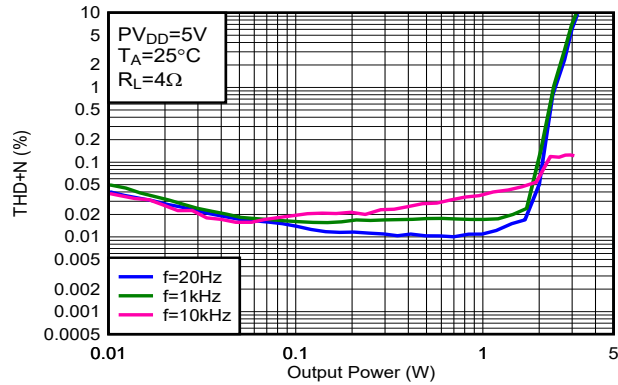


Figure 5-43. THD+N vs Output Power

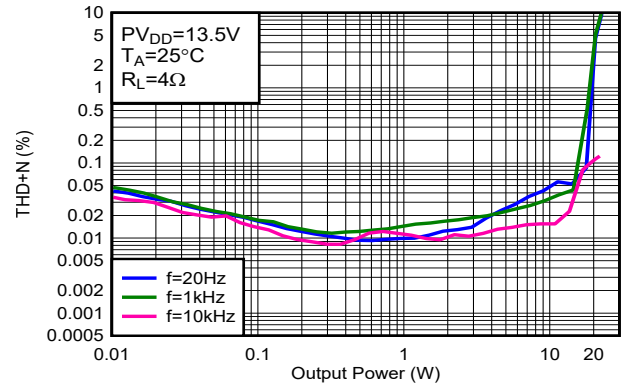


Figure 5-44. THD+N vs Output Power

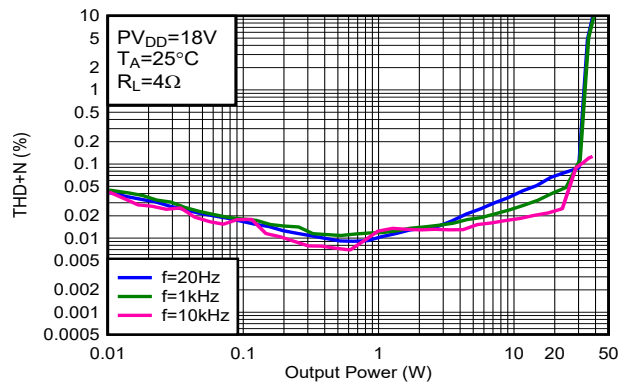


Figure 5-45. THD+N vs Output Power

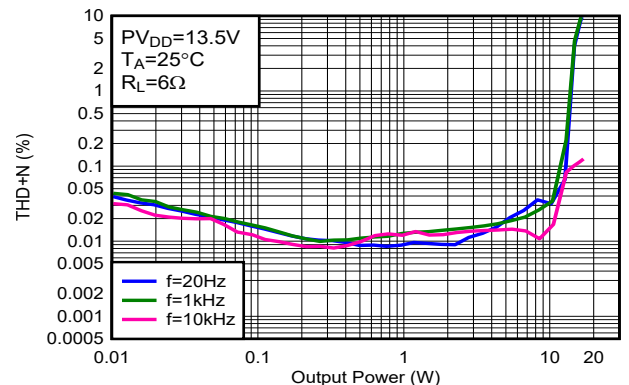


Figure 5-46. THD+N vs Output Power

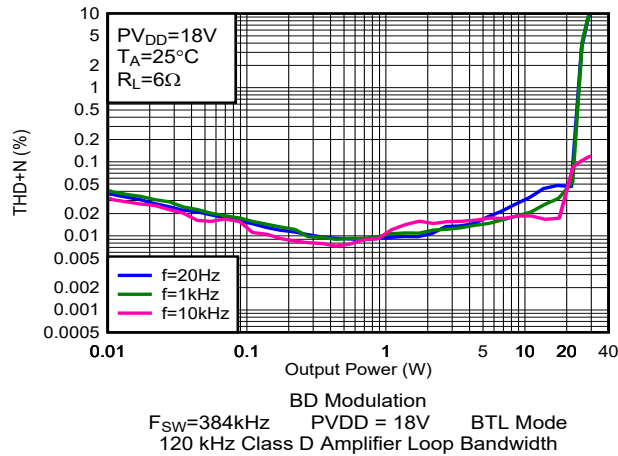


Figure 5-47. THD+N vs Output Power

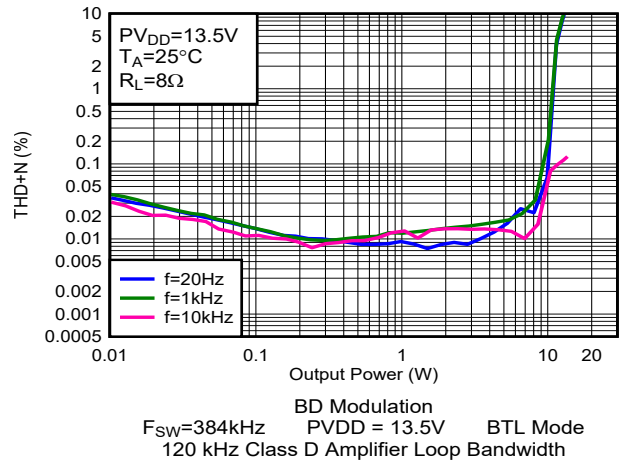


Figure 5-48. THD+N vs Output Power

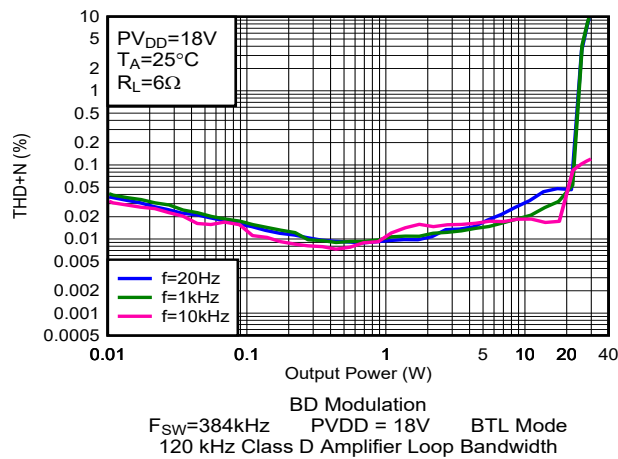


Figure 5-49. THD+N vs Output Power

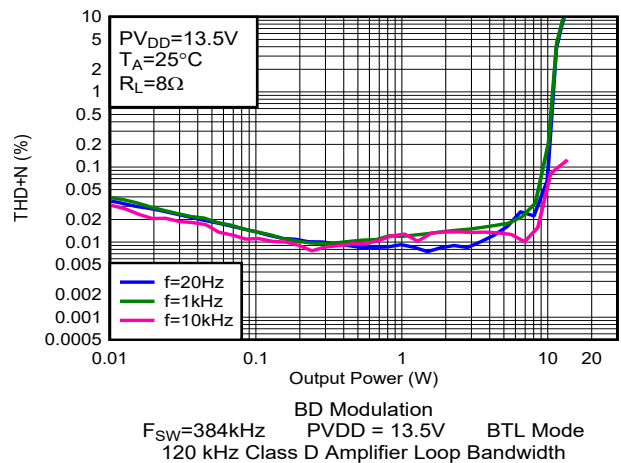


Figure 5-50. THD+N vs Output Power

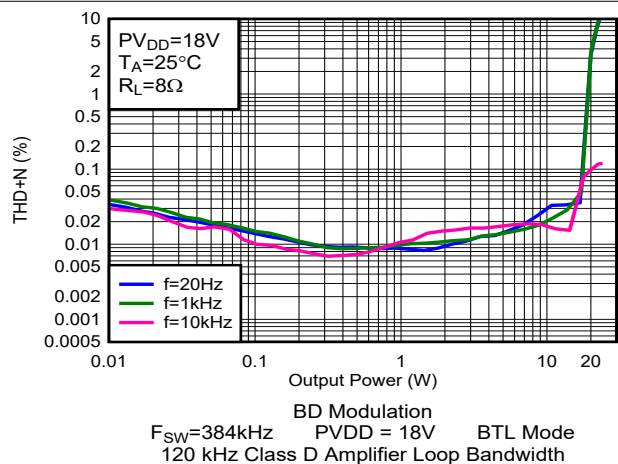


Figure 5-51. THD+N vs Output Power

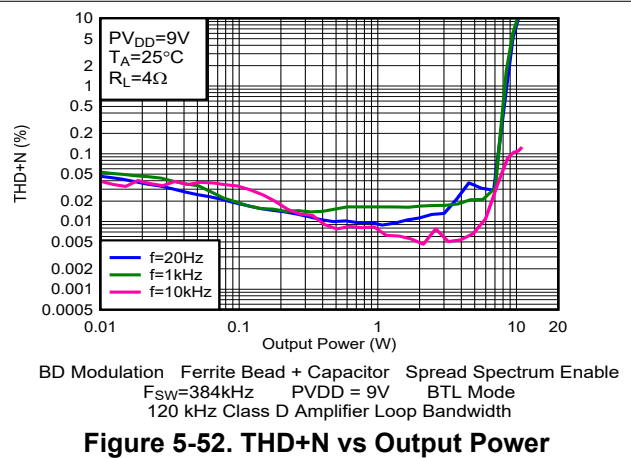
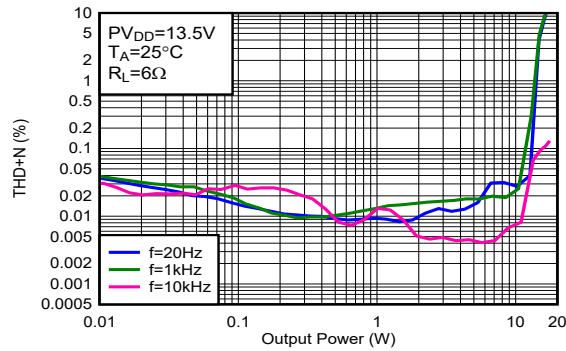
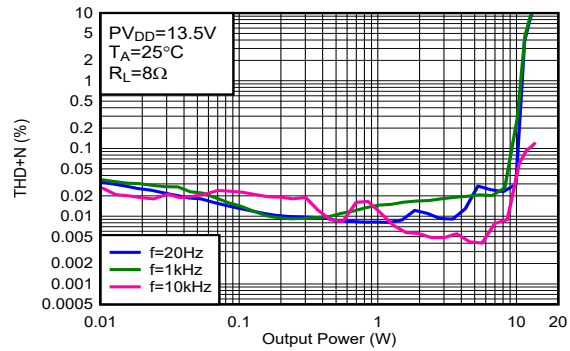


Figure 5-52. THD+N vs Output Power



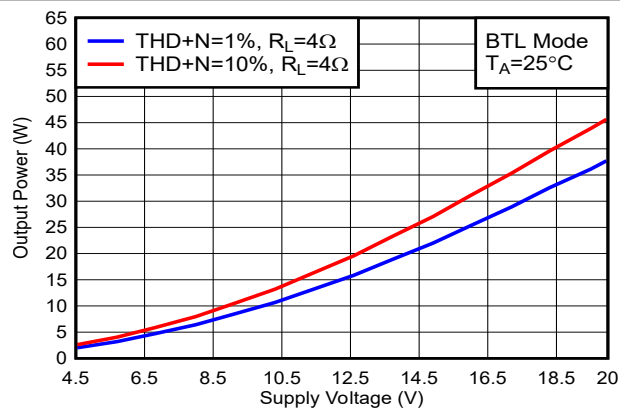
BD Modulation Ferrite Bead + Capacitor Spread Spectrum Enable
 $F_{SW}=384\text{kHz}$ PVDD = 13.5V BTL Mode
 120 kHz Class D Amplifier Loop Bandwidth

Figure 5-53. THD+N vs Output Power



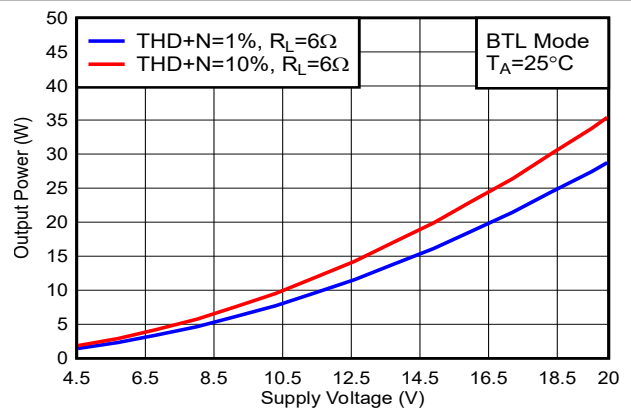
BD Modulation Ferrite Bead + Capacitor Spread Spectrum Enable
 $F_{SW}=384\text{kHz}$ PVDD = 13.5V BTL Mode
 120 kHz Class D Amplifier Loop Bandwidth

Figure 5-54. THD+N vs Output Power



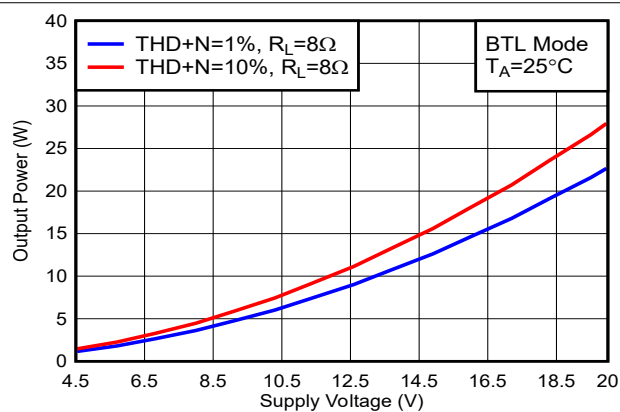
BD Modulation
 $F_{SW}=384\text{kHz}$ Load = 4Ω BTL Mode
 120 kHz Class D Amplifier Loop Bandwidth

Figure 5-55. Output Power vs Supply Voltage



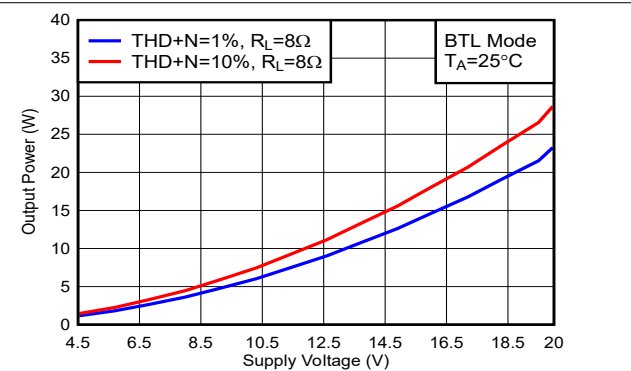
BD Modulation
 $F_{SW}=384\text{kHz}$ Load = 6Ω BTL Mode
 120 kHz Class D Amplifier Loop Bandwidth

Figure 5-56. Output Power vs Supply Voltage



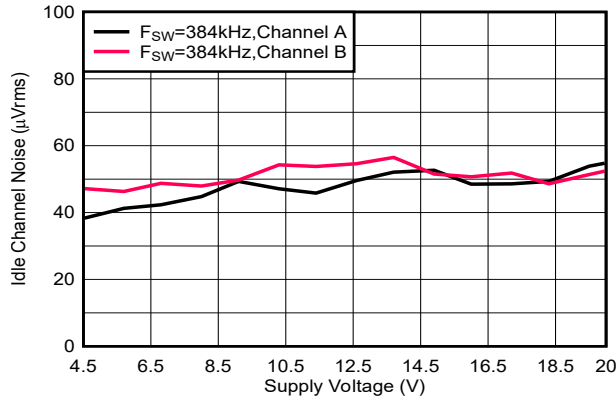
BD Modulation
 $F_{SW}=384\text{kHz}$ Load = 8Ω BTL Mode
 120 kHz Class D Amplifier Loop Bandwidth

Figure 5-57. Output Power vs Supply Voltage



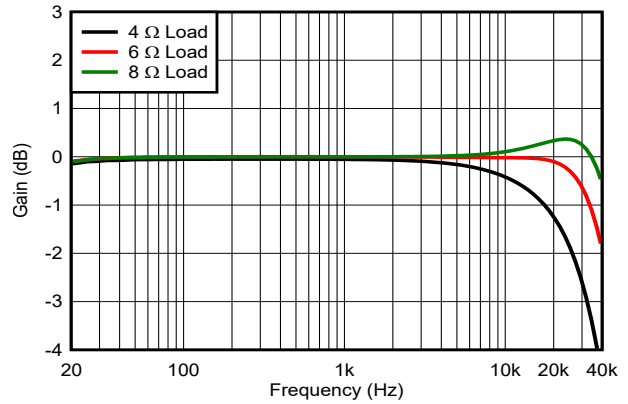
BD Modulation Ferrite Bead + Capacitor Spread Spectrum Enable
 $F_{SW}=384\text{kHz}$ Load = 8Ω BTL Mode
 120 kHz Class D Amplifier Loop Bandwidth

Figure 5-58. Output Power vs Supply Voltage



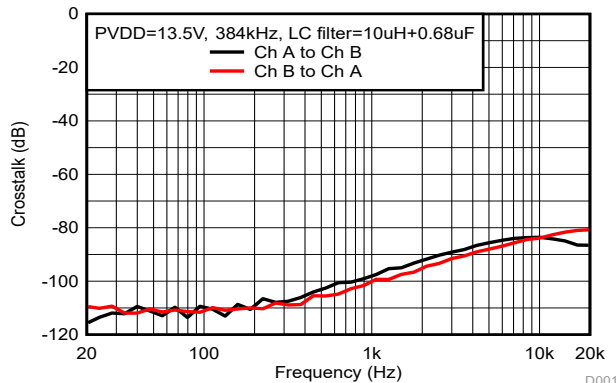
BD Modulation
F_{SW}=384kHz Load = 8Ω BTL Mode
120kHz Class D Amplifier Loop Bandwidth

Figure 5-59. Idle Channel Noise vs Supply Voltage



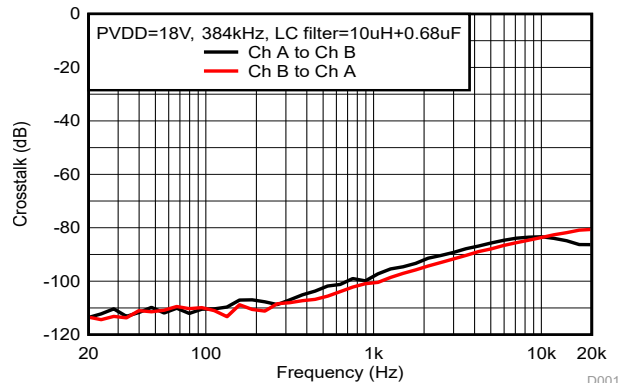
BD Modulation P_O=1W PVDD=13.5V
F_{SW}=384kHz BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

Figure 5-60. Gain vs Frequency



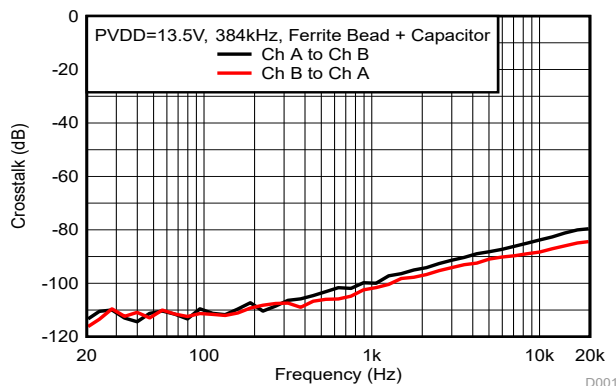
PVDD=13.5V, 384kHz, LC filter=10uH+0.68uF
PVDD=13.5V BD Modulation Pout=1W
F_{SW}=384kHz Load = 6Ω BTL Mode

Figure 5-61. Crosstalk



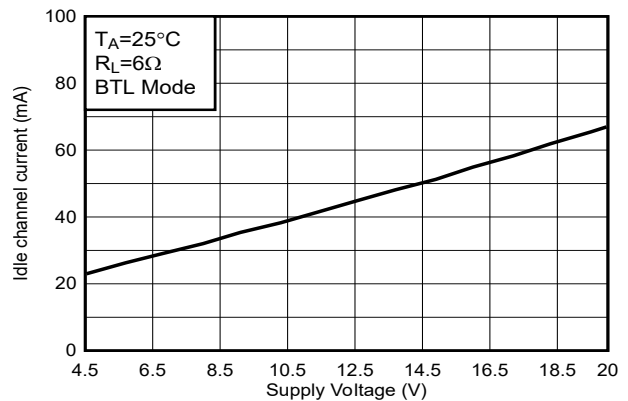
PVDD=18V, 384kHz, LC filter=10uH+0.68uF
PVDD=18V BD Modulation Pout=1W
F_{SW}=384kHz Load = 6Ω BTL Mode

Figure 5-62. Crosstalk



PVDD=13.5V, 384kHz, Ferrite Bead + Capacitor
Spread Spectrum BD Modulation Pout=1W
Enable Load = 6Ω BTL Mode

Figure 5-63. Crosstalk



T_A=25°C
R_L=6Ω
BTL Mode
F_{SW}=384kHz Load = 6Ω BTL Mode
120 kHz Class D Amplifier Loop Bandwidth

Figure 5-64. PVDD Idle Current vs PVDD Voltage

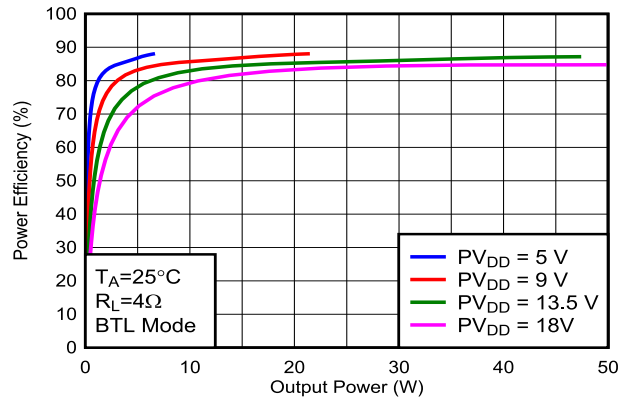


Figure 5-65. Efficiency vs Output Power

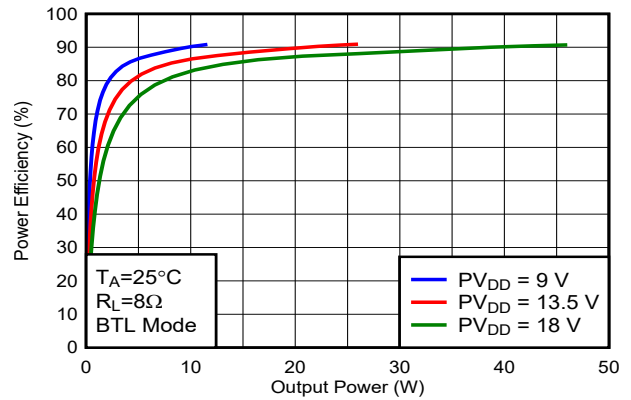


Figure 5-66. Efficiency vs Output Power

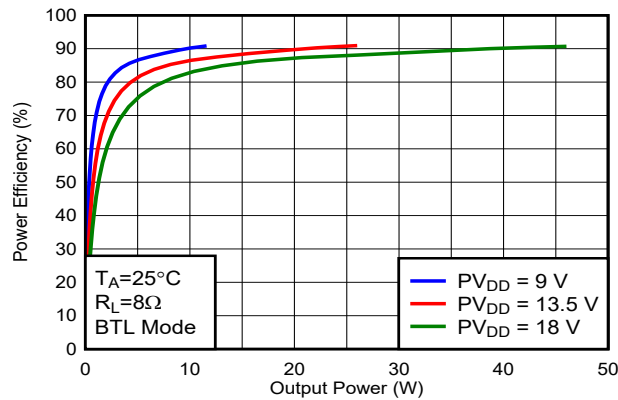


Figure 5-67. Efficiency vs Output Power

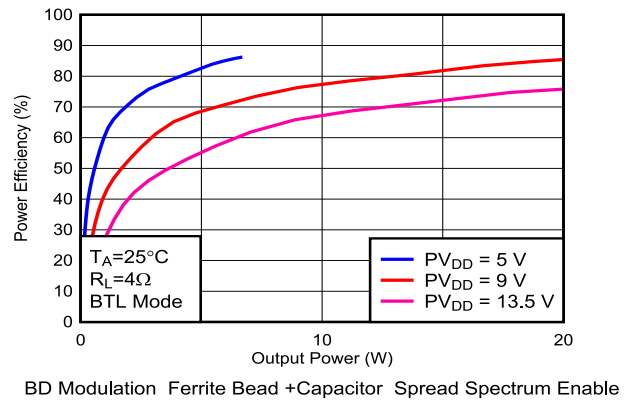


Figure 5-68. Efficiency vs Output Power (with FB)

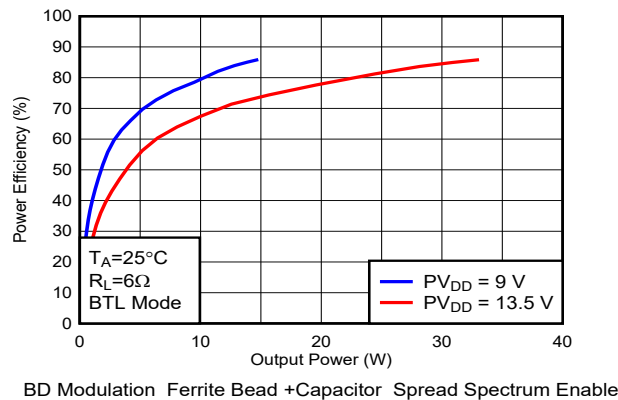


Figure 5-69. Efficiency vs Output Power

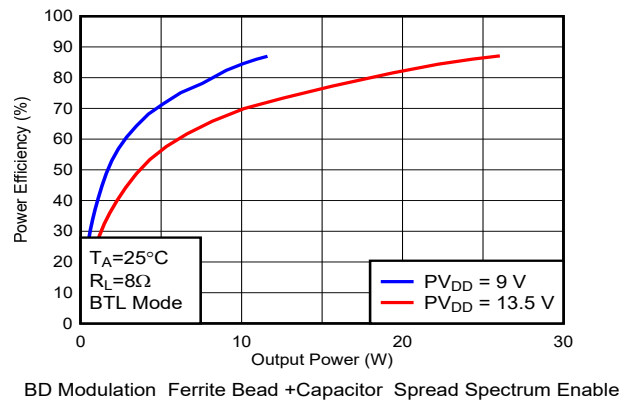


Figure 5-70. Efficiency vs Output Power

6 Detailed Description

6.1 Overview

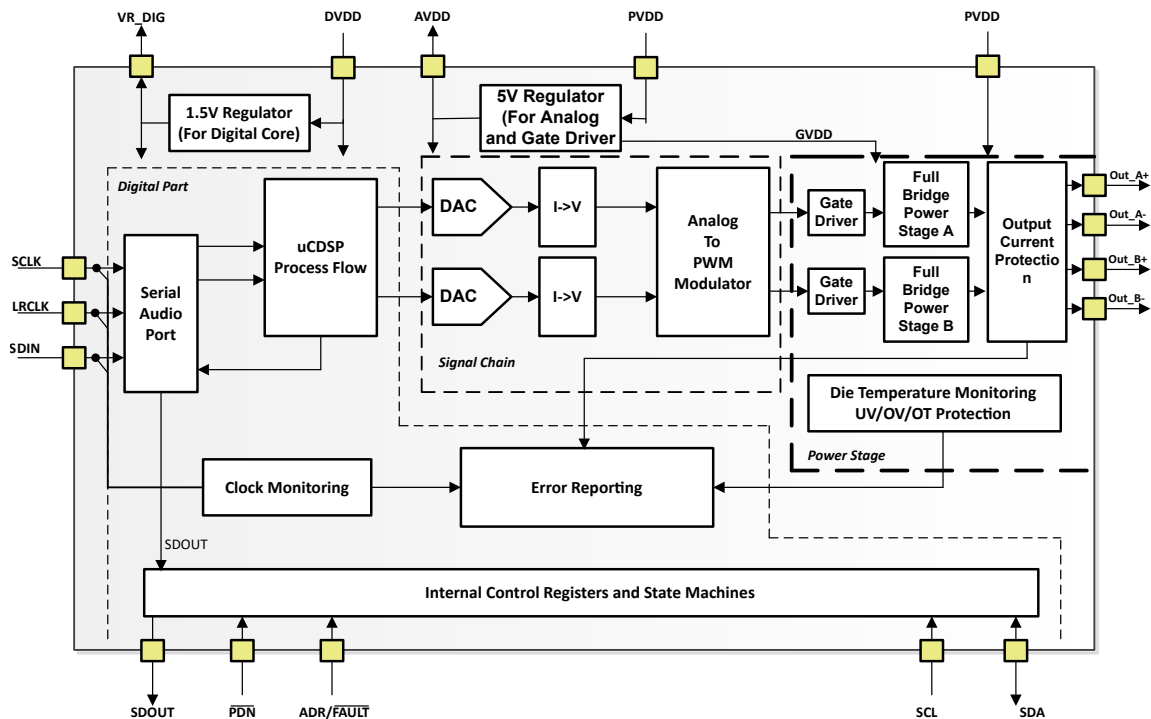
The TAS5802 device integrates 4 main building blocks into a single cohesive device that maximizes sound quality, flexibility, and ease of use. The 4 main building blocks are listed as follows:

- A stereo audio DAC.
- An Audio DSP subsystem.
- A flexible close-loop amplifier capable of operating in stereo or mono, at several different switching frequencies, and with a variety of output voltages and loads.
- An I²C control port for communication with the device

The device requires only two power supplies for proper operation. A DVDD supply is required to power the low-voltage digital circuitry. Another supply, called PVDD, is required to provide power to the output stage of the audio amplifier. One internal LDO convert PVDD to 5 V for GVDD and AVDD.

TAS5802 implements a dynamic range boost to minimize the idle channel noise, while maintaining the same dynamic range.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Power Supplies

To facilitate system design, TAS5802 needs only a 3.3-V or 1.8-V supply in addition to the (typical) 12-V or 20-V power-stage supply. Two internal voltage regulators provide suitable voltage levels for the gate drive circuitry and internal circuitry. The external pins (DVDD and AVDD) are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors. To provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_x). The gate drive voltages (GVDD) are derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, the inductance between the power-supply pins and decoupling capacitors must be avoided. For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (GVDD) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver.

6.3.2 Device Clocking

The TAS5802 devices have flexible systems for clocking. Internally, the device requires several clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface.

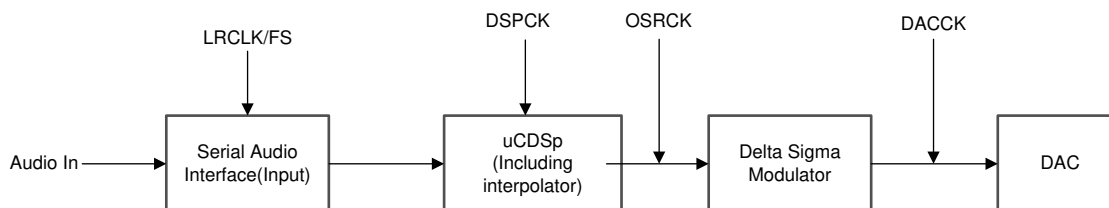


Figure 6-1. Audio Flow with Respective Clocks

Figure 6-1 shows the basic data flow and clock Distribution.

The Serial Audio Interface typically has 4 connection pins which are listed as follows:

- SCLK (Bit Clock)
- LRCK/FS (Left Right Word Clock and Frame Sync)
- SDIN (Input Data)
- SDOUT (Output Data)

The device has an internal PLL that is used to take SCLK and create the higher-rate clocks required by the DSP and the DAC clock.

The TAS5802 device has an audio sampling rate detection circuit that automatically senses which frequency the sampling rate is operating. Common audio sampling frequencies of 32kHz, 44.1kHz – 48kHz, 88.2kHz – 96kHz with $\pm 5\%$ tolerance are supported. The sampling frequency detector sets the clock for DAC and DSP automatically.

6.3.3 Serial Audio Port – Clock Rates

The serial audio interface port is a 3-wire serial port with the signals LRCLK/FS, SCLK, and SDIN. SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the TAS5802 device on the rising edge of SCLK. The LRCK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

Table 6-1. Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	SCLK RATE (f _s)
I ² S/LJ/RJ	32, 24, 20, 16	32 to 96	64, 32
TDM	32, 24, 20, 16	32	128
		44.1, 48	128, 256, 512
		96	128, 256

Before DSP registers initialize with I²C during the start-up, TAS5802 requires a stable I²S signal. When Clock halt, non-supported SCLK to LRCLK(FS) ratio is detected, the device reports Clock Error in GLOBAL_FAULT1 Register (Offset = 71h) [Reset = 00h] - D[2].

6.3.4 Serial Audio Port (SAP)

The serial audio interface port is a 3-wire serial port with the signals LRCK/FS, SCK, and SDIN. SCK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the device on the rising edge of SCK. The LRCK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

The device supports industry-standard audio data formats, including standard I2S, left-justified, right-justified, and TDM/DSP data. Data formats are selected via Register (SAP_CTRL1 Register (Offset = 33h) [Reset = 02h] - D[5:4]). If the high width of LRCK/FS in TDM/DSP mode is less than 8 cycles of SCK, the register (SAP_CTRL1 Register (Offset = 33h) [Reset = 02h] - D[3:2]) should be set to 01. All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. All the data formats, word length, and clock rate supported by this device are shown in Table 1. The data formats are detailed in Figure 1 through Figure 6. The word length are selected via Register (SAP_CTRL1 Register (Offset = 33h) [Reset = 02h] - D[1:0]). The offsets of data are selected via Register (SAP_CTRL1 Register (Offset = 33h) [Reset = 02h] - D[7]) and Register (SAP_CTRL2 Register (Offset = 34h) [Reset = 00h] - D[7:0]). The default setting is I2S and 24-bit word length.

Table 6-2. Audio Data Formats, Word Lengths, and Clock Rates

FORMAT	DATA BITS	LRCK/FS FREQUENCY (kHz)	SCK RATE (f _s)
I2S/LJ/RJ	32, 24, 20, 16	16, 32, 44.1/48, 96	32, 64
TDM/DSP	32, 24, 20, 16	16, 32, 44.1/48, 96	128, 256, 512

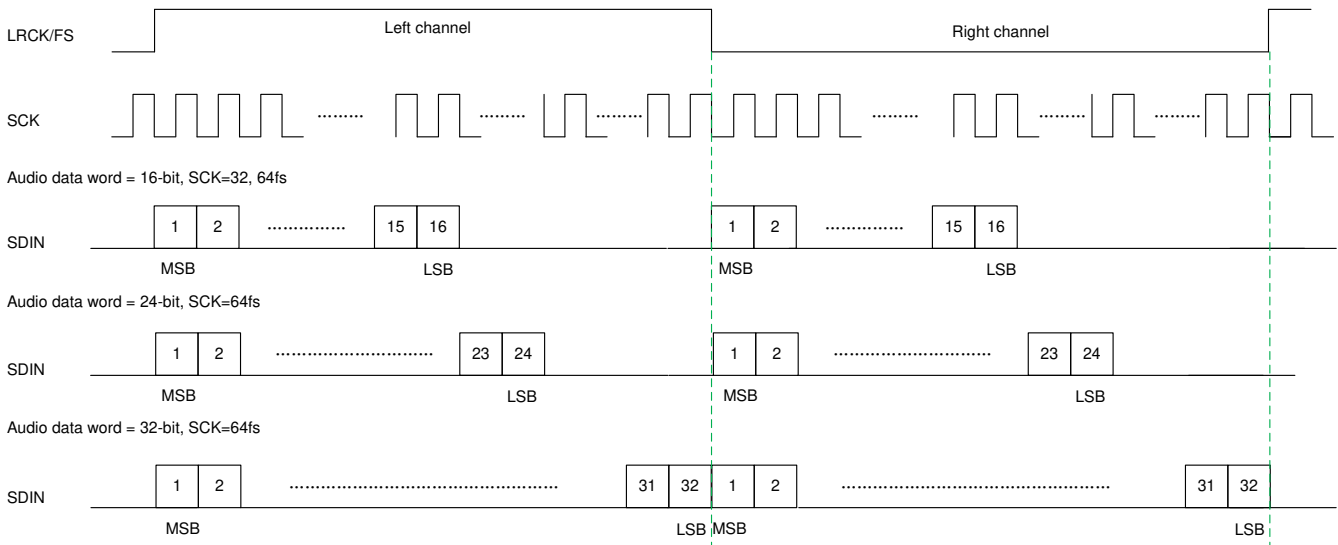
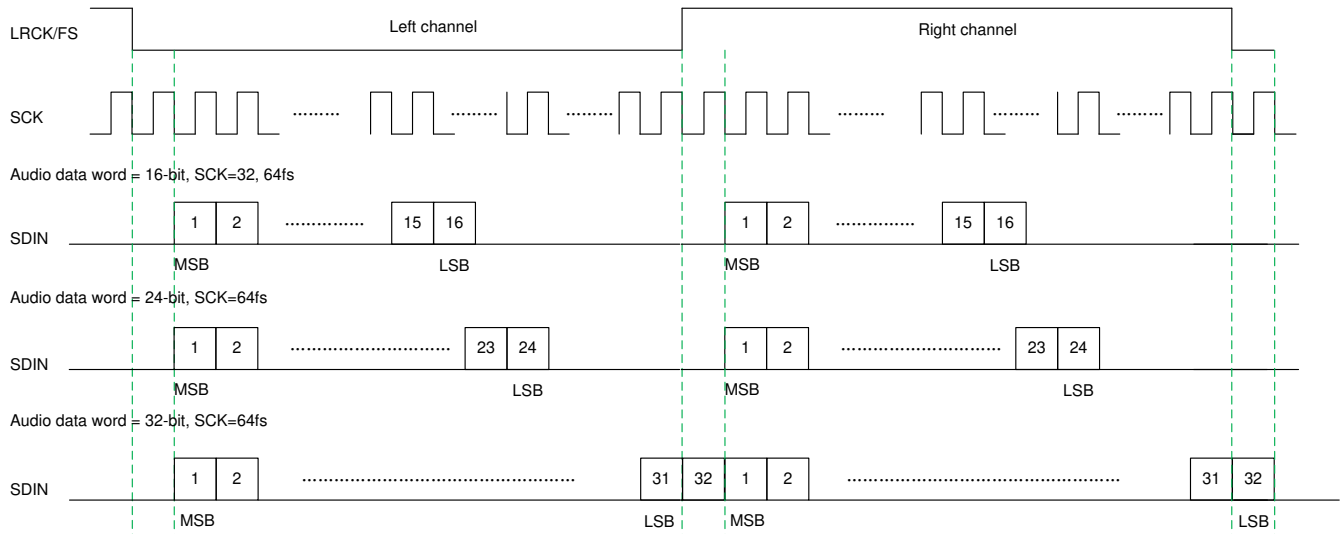
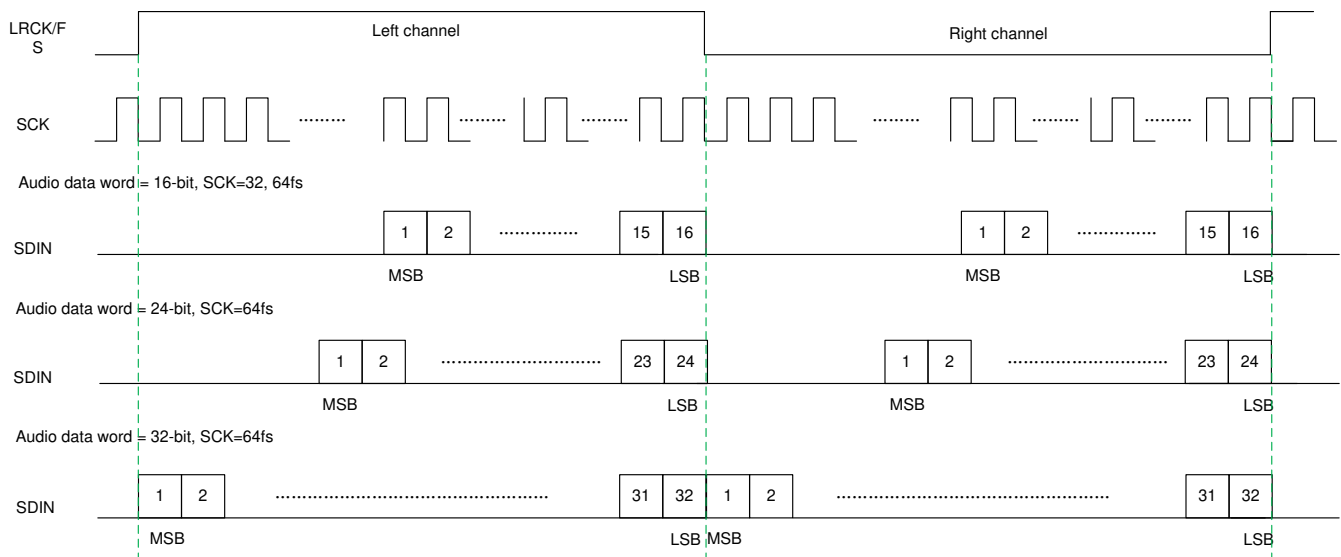


Figure 6-2. Left Justified Audio Data Format



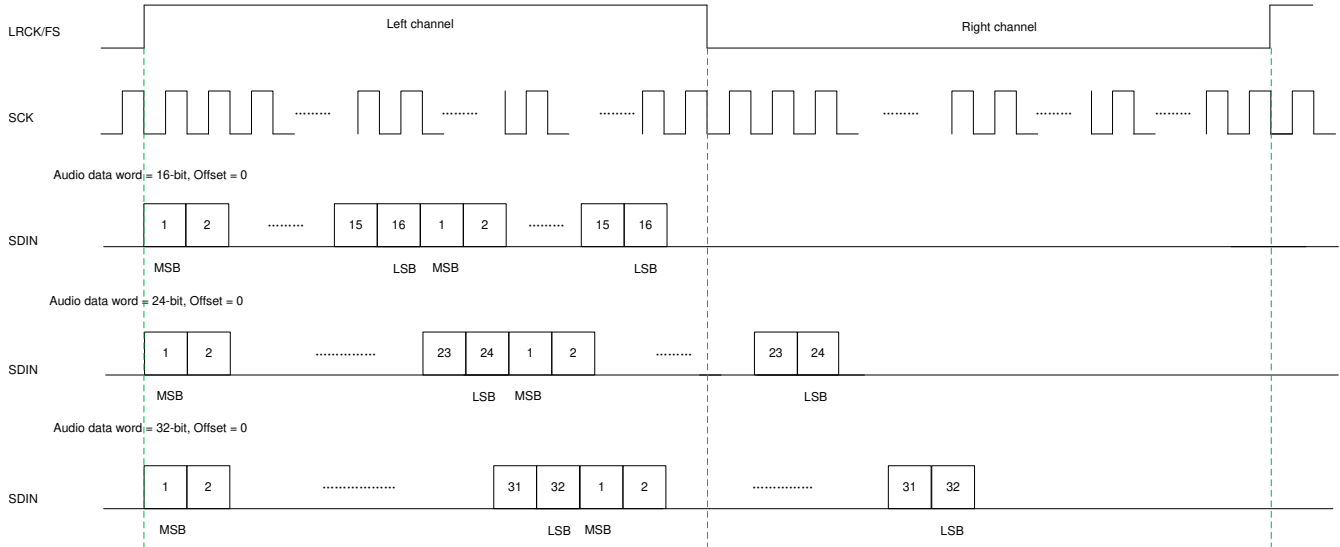
I²S Data Format; L-channel = LOW, R-channel = HIGH

Figure 6-3. I²S Audio Data Format



Right Justified Data Format; L-channel = HIGH, R-channel = LOW

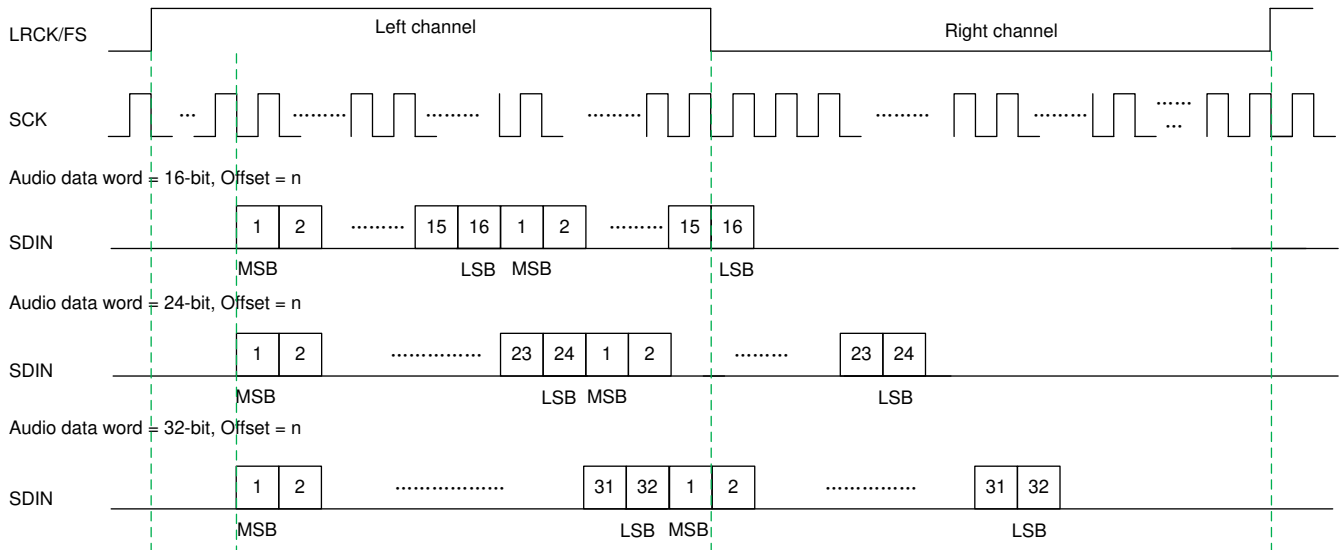
Figure 6-4. Right Justified Audio Data Format



TDM Data Format with OFFSET = 0

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 6-5. TDM Audio Data Format



TDM Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 6-6. TDM 2 Audio Data Format

The I2S target timing is shown in [Figure 6-7](#).

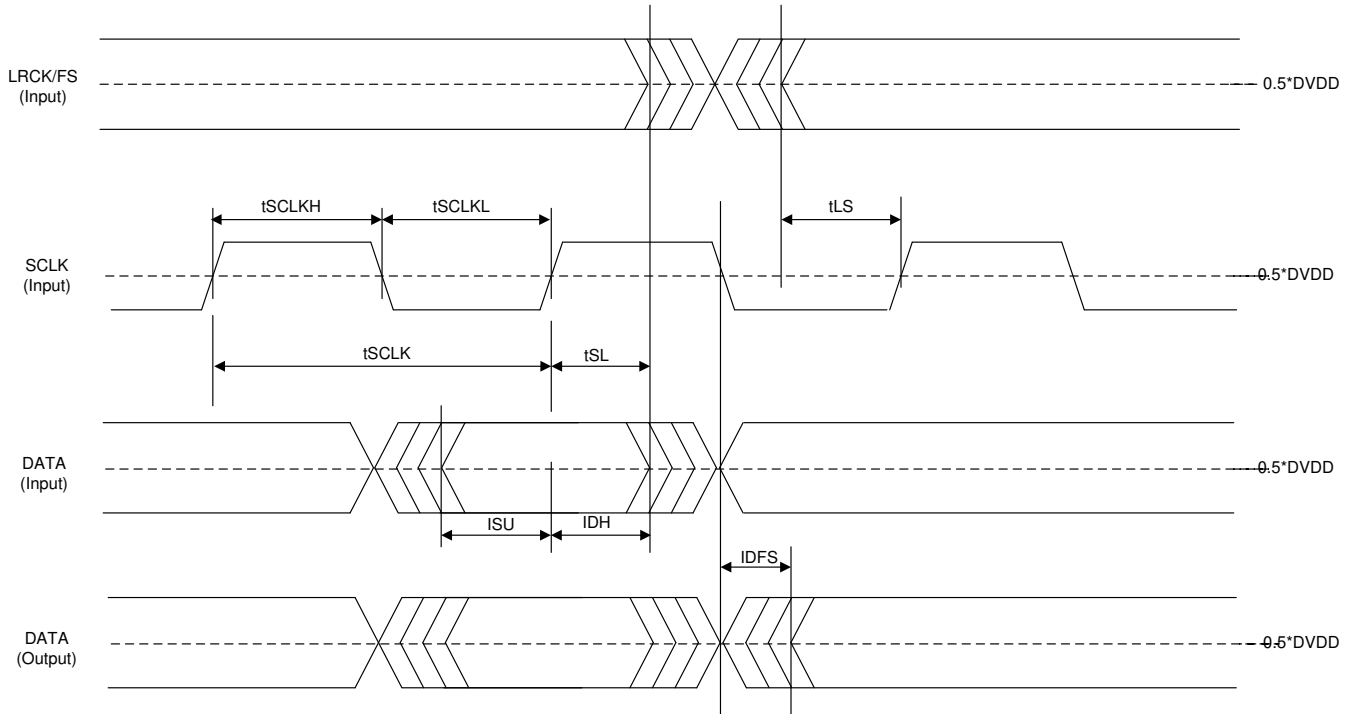


Figure 6-7. Serial Audio Timing - Target

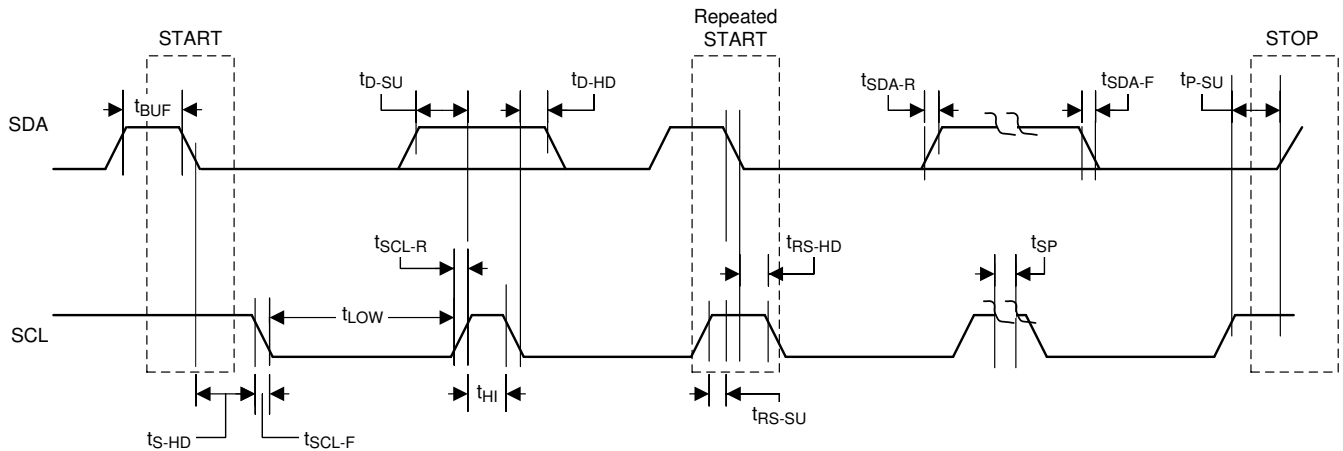


Figure 6-8. I²C Communication Timing - Target

6.3.5 Digital Audio Processing

TAS5802 DSP has a flexible process flows for different applications, refer to application note, TAS5815 and TAS5802 Process Flows for details.

6.3.6 Class D Audio Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC ensure constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device. The switching rate of the amplifier is configurable via I²C interface. In this case, the PWM switching frequency is a multiple of the sample rate.

6.3.6.1 Speaker Amplifier Gain Select

A combination of digital gain and analog gain is used to provide the overall gain of the speaker amplifier. As seen in Figure 6-9, the audio path of the TAS5802 consists of a digital audio input port, a digital audio path, a digital to PWM converter (DPC), a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the DPC block to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown as GDIG in the digital audio path and the analog gain from the input of the analog modulator GANA to the output of the speaker amplifier power stage.

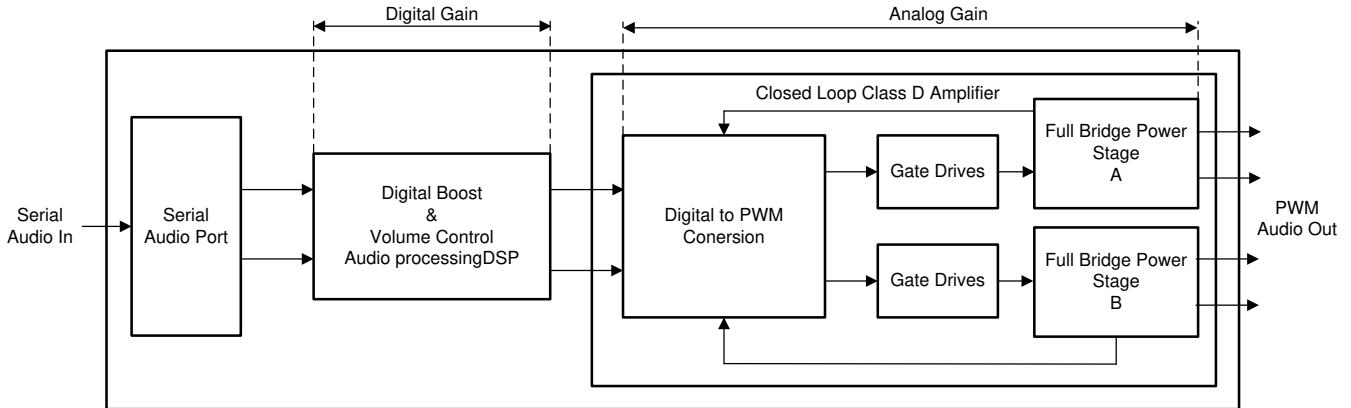


Figure 6-9. Speaker Amplifier Gain

As shown in Figure 6-9, the first gain stage for the speaker amplifier is present in the digital audio path. It consists of the volume control and the digital boost block. The volume control is set to -3 dB by default, it does not change. For all settings of the Register **AGAIN Register (Offset = 54h) [Reset = 06h]**, **AGAIN[4:0]**, the digital boost block remains at -3 dB. These gain settings ensure that the output signal is not clipping at different PVDD levels. -3 dBFS output is 20.9-V peak output voltage, which is suggested for TAS5802 maximum gain setting.

Note

Considering the register setting is compatible with other devices of TAS58xx series, the default value of the **AGAIN<4:0>** is b'00000, the analog gain at this time is 0dBFS and peak voltage is 29.5V. Because the maximum PVDD voltage of TAS5802 supports up to 20V, it should be noted in the application that the recommended maximum gain level is -3dBFS with 20.9V peak voltage, which means the **AGAIN<4:0>** is configured as b'00110.

Table 6-3. Analog Gain Setting

AGAIN <4:0>	GAIN (dBFS)	AMPLIFIER OUTPUT PEAK VOLTAGE (V)
00000	0	29.5
.....
00110	-3.0	20.9
.....
11111	-15.5	4.87

6.4 Device Functional Modes

6.4.1 Software Control

The TAS5802 device is configured via an I²C communication port.

The I²C Communication Protocol is detailed in the I²C Communication Port section. The I²C timing requirements are described in the I²C Bus Timing – Standard and I²C Bus Timing – Fast sections.

6.4.2 Speaker Amplifier Operating Modes

The TAS5802 device can only be configured in BTL Mode.

6.4.2.1 BTL Mode

In BTL mode, the TAS5802 amplifies two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on differential output pair shown as OUT_A+ and OUT_A-, the amplified right signal is presented on differential output pair shown as OUT_B+ and OUT_B-.

6.4.3 Low EMI Modes

TAS5802 employs several modes to minimize EMI during playing audio, and they can be used based on different applications.

6.4.3.1 Spread Spectrum

Spread spectrum is used in some inductor free case to minimize EMI noise. The TAS5802 supports Spread Spectrum with triangle mode.

User needs to configure register RAMP_SS_CTRL0 (0x6B) to enable Spread Spectrum with triangle mode, and select spread spectrum frequency and range with RAMP_SS_CTRL1 (0x6C). For 384kHz F_{SW} which configured by DEVICE_CTRL1 (0x02), the Spread Spectrum frequency and range are described in [Table 6-4](#)

Table 6-4. Triangle Mode Spread Spectrum Frequency and Range Selection

TRI_CTRL[3:0]	0	1	2	3	4	5	6	7
Triangle Freq	24k				48k			
Spread Spectrum Range	5%	10%	20%	25%	5%	10%	20%	25%

User Application example-Central Switching Frequency is 384kHz, Triangle Frequency is 24kHz:

w A8 6B 01 //RAMP_SS_CTRL0[0]=1, Enable Triangle Spread Spectrum

w A8 6C 03 //RAMP_SS_CTRL1[3:0]=0011, Triangle Frequency = 24kHz, Spread Spectrum Range should be 25% (336kHz~432kHz)

6.4.3.2 Channel to Channel Phase Shift

This device supports channel to channel 180-degree PWM phase shift to minimize the EMI.

6.4.3.3 Multi-Devices PWM Phase Synchronization

This device supports up to 4 phase selections for multiple device application systems. For example, when a system integrated 4 pieces of TAS5802 devices, user can select phase 0/1/2/3 for each device with register RAMP_PHASE_CTRL (0x6A), which means there is a 45-degree phase shift between each device to minimize the EMI.

Recommend to do the Phase Synchronization with I²S clock during the Startup Phase:

1. Halt I²S clock.
2. Configure each device phase selection and enable the phase synchronization. For example: Register 0x6A = 0x00 for device 0; Register 0x6A = 0x03 for device 1; Register 0x6A = 0x08 for device 2; Register 0x6A = 0x0C for device 3. There should be a 45-degree PWM phase shift between each device to minimize the EMI.

3. Configure each device into Hi-Z mode.
4. Provide I²S to each device. Phase synchronization for all 4 devices will be automatically done by internal sequence.
5. Initialize the DSP code. (This step can be skipped if only need to do the PWM Phase Synchronization).
6. Device to Device PWM phase shift should be fixed with 45 degree.

6.4.4 Thermal Foldback

The Thermal Foldback (TFB), is designed to protect TAS5802 from excessive die temperature increases, in case the device operates beyond the recommended temperature/power limit, or with a weaker thermal system design than recommended. It allows the TAS5802 to play as loud as possible without triggering unexpected thermal shutdown. When the die temperature triggers the over-temperature warning (OTW) level (135C typ), an internal AGL (Automatic Gain Limiter) will reduce the digital gain automatically. Once the die temperature drops below the OTW, the device's digital gain gradually returns to the former setting.

6.4.5 Device State Control

TAS5802 has 5 states with different power dissipation which listed in the *Electrical Characteristics* Table.

- Shutdown Mode. With $\overline{\text{PDN}}$ pin pull down to GND. All internal LDOs (1.5V for digital core, 5V for analog) are disabled, all registers will be cleared to default value.

Note

Exit from Shutdown Mode and re-enter into Play mode, need reload all register configurations (which generated by PurePath Console3) again.

- Deep Sleep Mode. Register 0x68h [1:0]=00, device stays in Deep Sleep Mode. In this mode, I2C block and 1.5V LDO for digital core still working, but internal 5V LDO (For AVDD and MOSFET gate driver) is disabled for low power dissipation. This mode can be used to extend the battery life in some portable speaker applications. If the host processor stops playing audio for a long time, TAS5802 can be set to Deep Sleep Mode to minimize power dissipation until host processor starts playing audio again. Unlike the Shutdown Mode (Pulling $\overline{\text{PDN}}$ Low), entering or exiting Deep Sleep Mode, the DSP keeps active.

Note

As in Deep Sleep Mode, the internal 5V LDO (For AVDD and internal MOSFET gate driver) is disabled. To exit from Deep Sleep Mode and re-enter into play mode, the below sequence is required for internal Finite-state machine fast setting (Take TAS5802 I²C device address = 0xA8 as example).

```
w A8 00 00 #Go to page 0
w A8 7f 00 #Change the book to 0x00
w A8 68 02 #Change the device into Hiz Mode
w A8 68 00 #Change the device into Deep Sleep Mode
w A8 00 00 #Go to page 0
w A8 7f 00 #Change the book to 0x00
w A8 68 02 #Change the device into Hiz Mode
w A8 68 03 #Change the device into Play Mode
```

- Sleep Mode. Register 0x68h [1:0]=01, device stays in Sleep Mode. In this mode, I²C block, Digital core, DSP Memory, 5V Analog LDO are stilling working. Unlike the Shutdown Mode (Pull $\overline{\text{PDN}}$ Low), enter or exit Sleep Mode, DSP is kept active. To exit from this mode and re-enter into play mode, set Register 0x68h [1:0]=11.
- Output Hi-Z Mode. Register 0x68h [1:0]=10, device stays in Hi-Z Mode. In this mode, only output driver is set to be Hi-Z state, all other block operate normally. To exit from this mode and re-enter into play mode, set Register 0x68h [1:0]=11.

- Play Mode. Register 0x68h [1:0]=11, device stays in Play Mode.

6.4.6 Device Modulation

TAS5802 has 3 modulation schemes: BD Modulation, 1SPW modulation and Hybrid modulation. Select modulation schemes for TAS5802 with Register 0x02 [1:0]-DEVICE_CTRL1.

6.4.6.1 BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

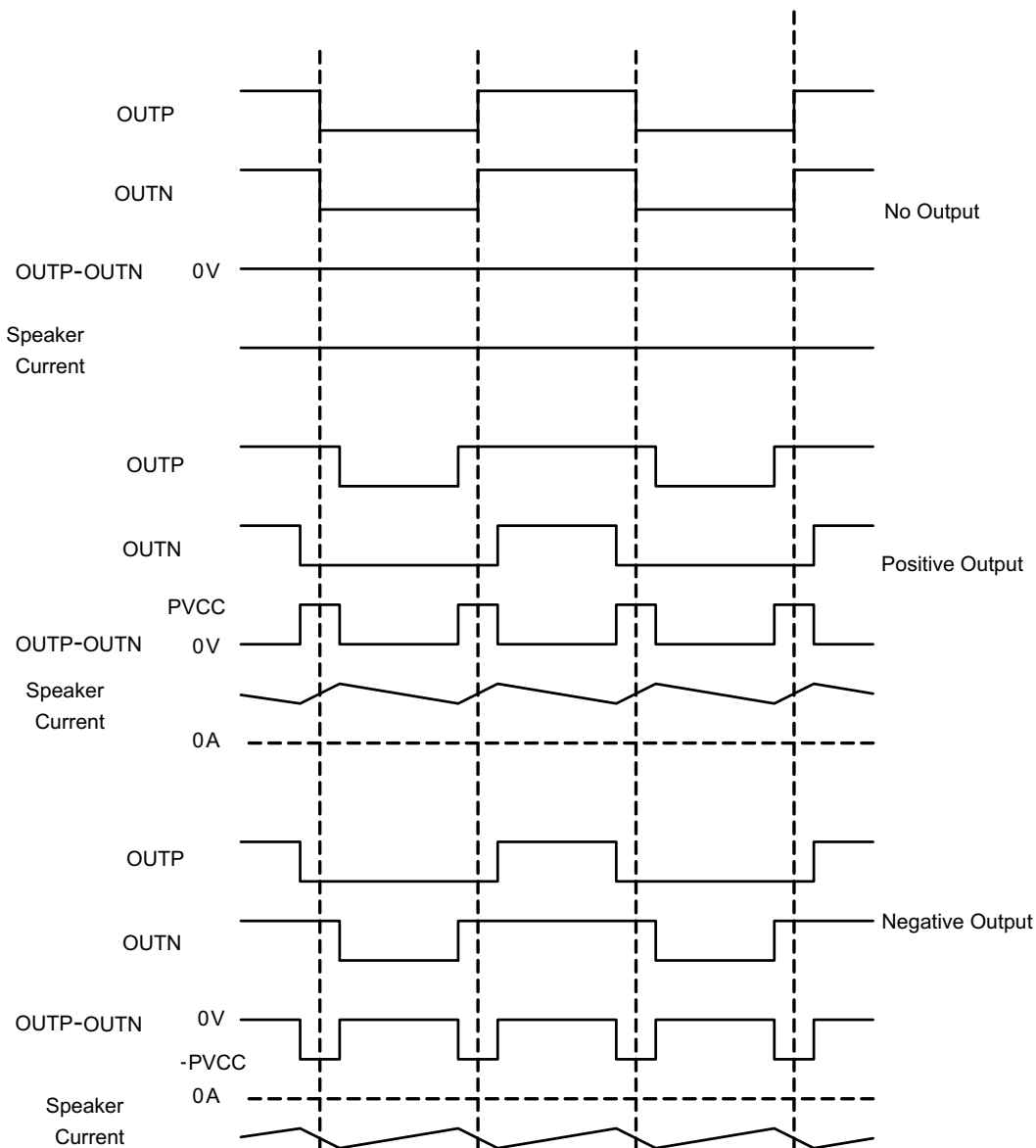


Figure 6-10. BD Mode Modulation

6.4.6.2 1SPW Modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low Idle Current mode the outputs operate at ~14% modulation during idle conditions. When an audio signal is applied one output will decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.

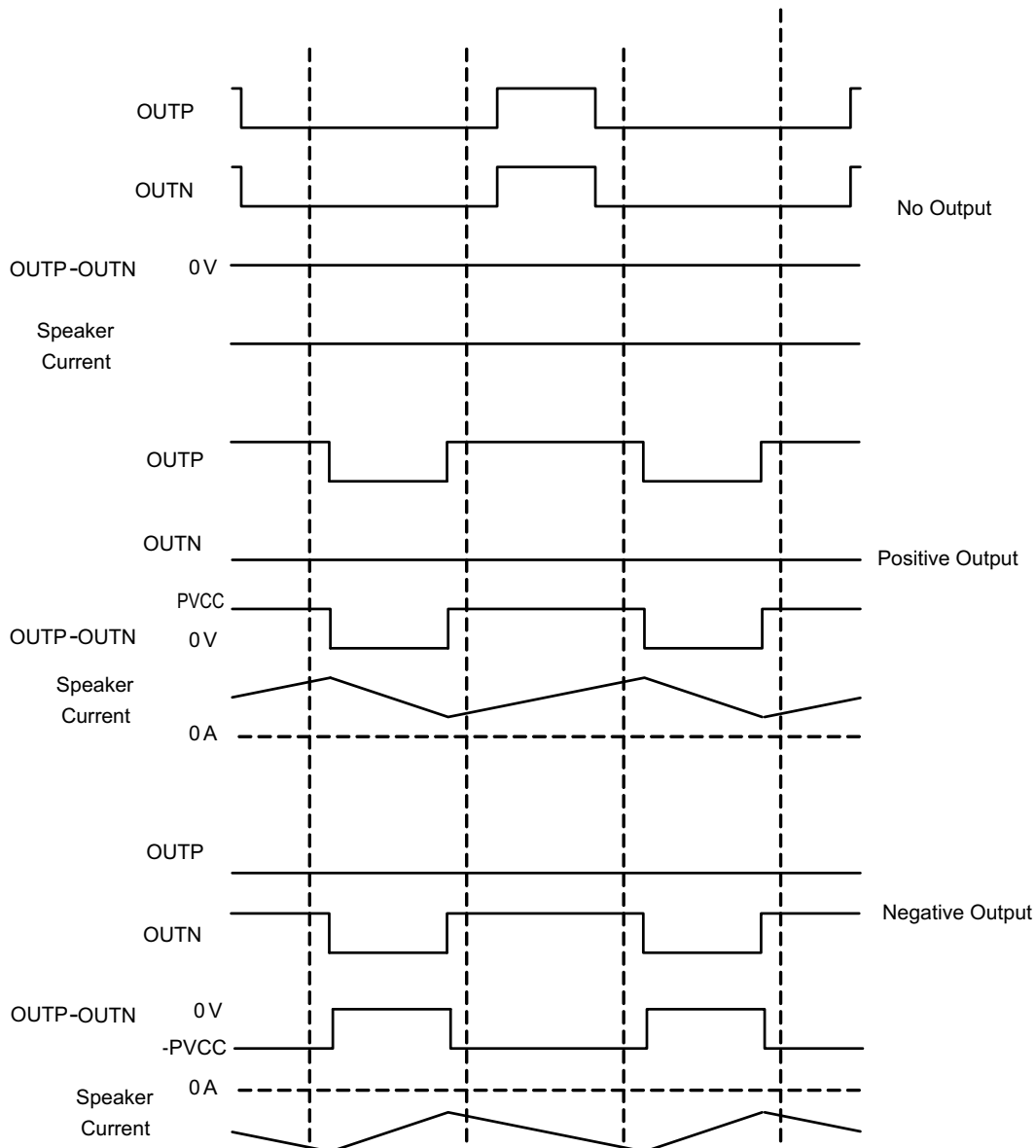


Figure 6-11. 1SPW Mode Modulation

6.4.6.3 Hybrid Modulation

Hybrid Modulation is designed to minimize power loss without compromising the THD+N performance, and is optimized for battery-powered applications. With Hybrid modulation enabled, the device detects the input signal level and adjusts the PWM duty cycle dynamically based on PVDD. Hybrid modulation achieves ultra-low idle current and maintains the same audio performance level as the BD Modulation. In order to minimize power dissipation,

low switching frequency (For example, $F_{sw} = 384 \text{ kHz}$) with proper LC filter ($15 \mu\text{H} + 0.68 \mu\text{F}$ or $22 \mu\text{H} + 0.68 \mu\text{F}$) is recommended. Follow these steps when using Hybrid Modulation:

- 1) With Hybrid Modulation, users need to input the system's PVDD value via device development application.
- 2) With Hybrid Modulation, Change device state from Deep Sleep Mode to Play Mode, specific sequence is required:
 1. Set device's PWM Modulation to BD or 1SPW mode via Register (Book0/Page0/Register0x02h, Bit [1:0]).
 2. Set device to Hi-Z state via Register (Book0/Page0/Register0x03h, Bit [1:0]).
 3. Delay 2ms.
 4. Set device's PWM Modulation to Hybrid mode via Register (Book0/Page0/Register0x02h, Bit [1:0]).
 5. Delay 15ms.
 6. Set device to Play state via Register (Book0/Page0/Register0x03h, Bit [1:0]).

6.5 Programming and Control

6.5.1 I²C Serial Communication Bus

The device has a bidirectional serial control interface that is compatible with the Inter IC (I²C) bus protocol and supports 100 and 400-kbps data transfer rates for random and sequential write and read operations as a target device. Because the TAS5802 register map and DSP memory spans multiple pages and books, the user should change from page to page or book to book before writing individual register or DSP memory. Changing from book to book is accomplished via register 0x7F on page 0x00 of each book. Changing from page to page is accomplished via register 0x00 on each page. This register value selects the page address, from 0 to 255.

6.5.2 Target Address

The TAS5802 device has 7 bits for the target address. The first five bits (MSBs) of the target address are factory preset to 10101(0xAx). The next two bits of address byte are the device select bits which can be user-defined by ADR pin in [I²C Target Address Configuration](#).

Table 6-5. I²C Target Address Configuration

ADR/FAULT PIN Configuration	MSBs					User Define		LSB
4.7kΩ to DVDD	1	0	1	0	1	0	0	R/ \bar{W}
15kΩ to DVDD	1	0	1	0	1	0	1	R/ \bar{W}
47kΩ to DVDD	1	0	1	0	1	1	0	R/ \bar{W}
120kΩ to DVDD	1	0	1	0	1	1	1	R/ \bar{W}

6.5.2.1 Random Write

As shown in [Figure 6-12](#), a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the device responds with an acknowledge bit. Next, the master transmits the address byte corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

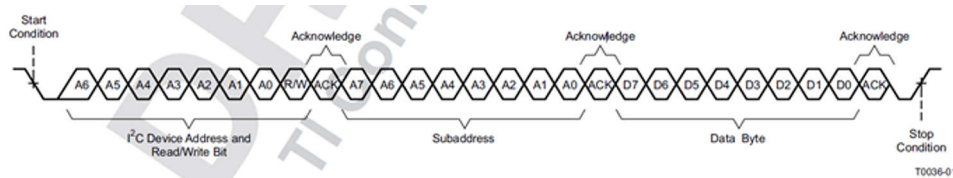


Figure 6-12. Random Write Transfer

6.5.2.2 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master to the device as shown in Figure 6-13. After receiving each data byte, the device responds with an acknowledge bit and the I²C subaddress is automatically incremented by one.

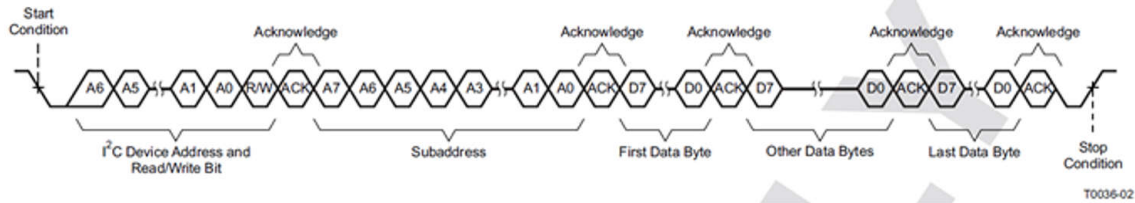


Figure 6-13. Sequential Write Transfer

6.5.2.3 Random Read

As shown in Figure 6-14, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte, the master device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

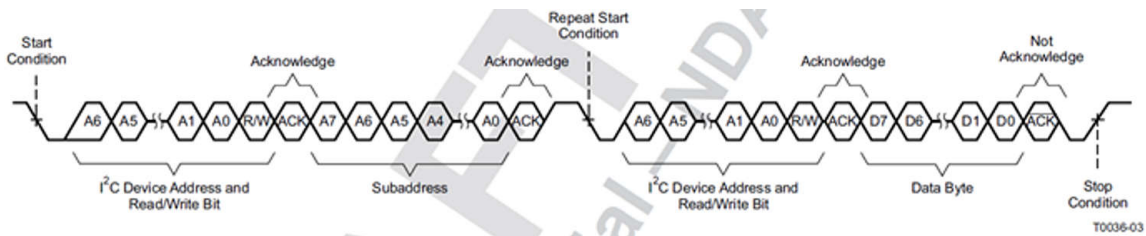


Figure 6-14. Random Read Transfer

6.5.2.4 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the master device as shown in Figure 6-15. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I²C subaddress by one. After receiving the last data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the transfer.

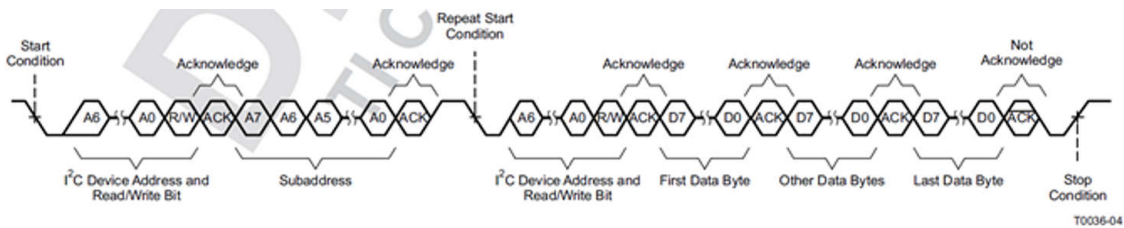


Figure 6-15. Sequential Read Transfer

6.5.2.5 DSP Memory Book, Page and BQ update

On page 0x00 of each book, register 0x7f is used to change the book. Register 0x00 of each page is used to change the page. To change a book first write 0x00 to register 0x00 to switch to page 0 then write the book number to register 0x7f on page 0. To change between pages in a book, simply write the page number to register 0x00.

All the Biquad Filters coefficients are addressed in book 0xAA. The five coefficients of every Biquad Filter should be written entirely and sequentially from the lowest address to the highest address. The address of all Biquad Filters can be found in [CONTROL PORT Registers](#).

6.5.2.6 Checksum

This device supports two different check sum schemes, a cyclic redundancy check (CRC) checksum and an Exclusive (XOR) checksum. Register reads do not change checksum, but writes to even nonexistent registers will change the checksum. Both checksums are 8-bit checksums and both are available together simultaneously. The checksums can be reset by writing a starting value (eg. 0x 00 00 00 00) to their respective 4-byte register locations.

6.5.2.6.1 Cyclic Redundancy Check (CRC) Checksum

The 8-bit CRC checksum used is the 0x7 polynomial (CRC-8-CCITT I.432.1; ATM HEC, ISDN HEC and cell delineation, $(1 + x^1 + x^2 + x^8)$). A major advantage of the CRC checksum is that it is input order sensitive. The CRC supports all I² transactions, excluding book and page switching. The CRC checksum is read from register 0x7E on page0 of any book (B_x, Page_0, Reg_126). The CRC checksum can be reset by writing 0x00 to the same register locations where the CRC checksum is valid.

6.5.2.6.2 Exclusive or (XOR) Checksum

The Xor checksum is a simpler checksum scheme. It performs sequential XOR of each register byte write with the previous 8-bit checksum register value. XOR supports only Book 0x8C, and excludes page switching and all registers in Page 0x00 of Book 0x8C. XOR checksum is read from location register 0x7D on page 0x00 of book 0x8C (B_140, Page_0, Reg_125). The XOR Checksum can be reset by writing 0x00 to the same register location where it is read.

6.5.3 Control via Software

- Startup Procedures
- Shutdown Procedures

6.5.3.1 Startup Procedures

1. Configure ADR/ $\overline{\text{FAULT}}$ pin with proper setting for I²C device address.
2. Bring up power supplies (it does not matter if PVDD or DVDD comes up first).
 - a. Ramp up DVDD to 1.8V or 3.3V
 - b. Ramp up PVDD as per recommended operating conditions
3. After stable DVDD and PVDD, wait ~1ms, bring up the $\overline{\text{PDN}}$ from LOW to HIGH.
4. After $\overline{\text{PDN}}$ High wait 5ms, then start SCLK, LRCLK.
5. Configure the device via the I²C control port based on the user cases (Make sure the $\overline{\text{PDN}}$ pin = HIGH before I²C control port operating).
6. The device is now in normal operation.

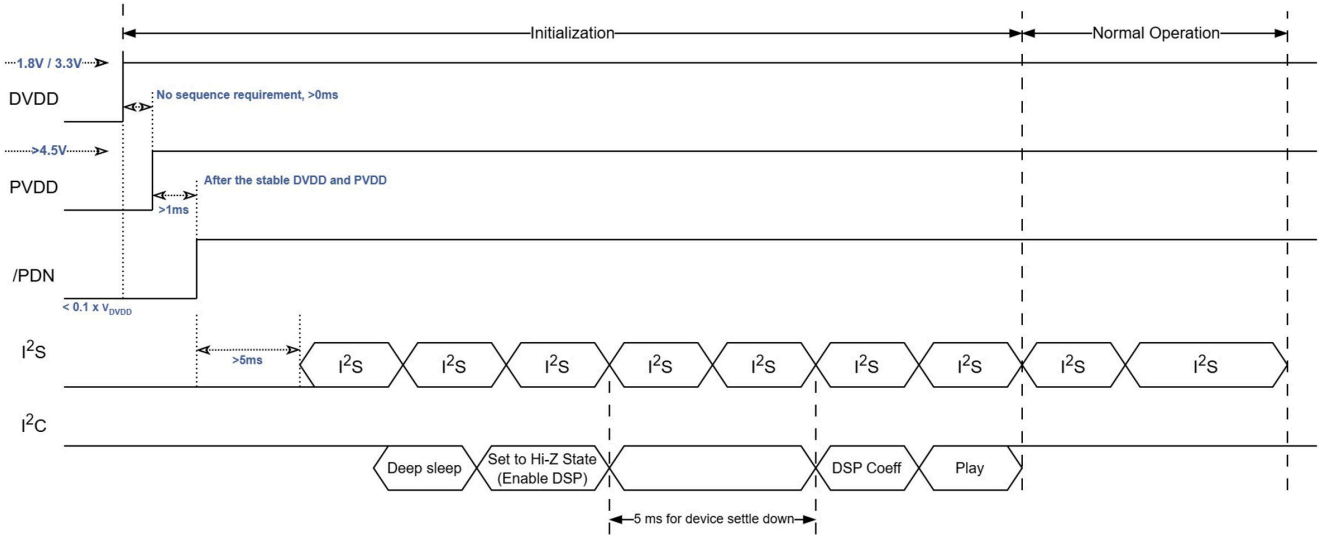
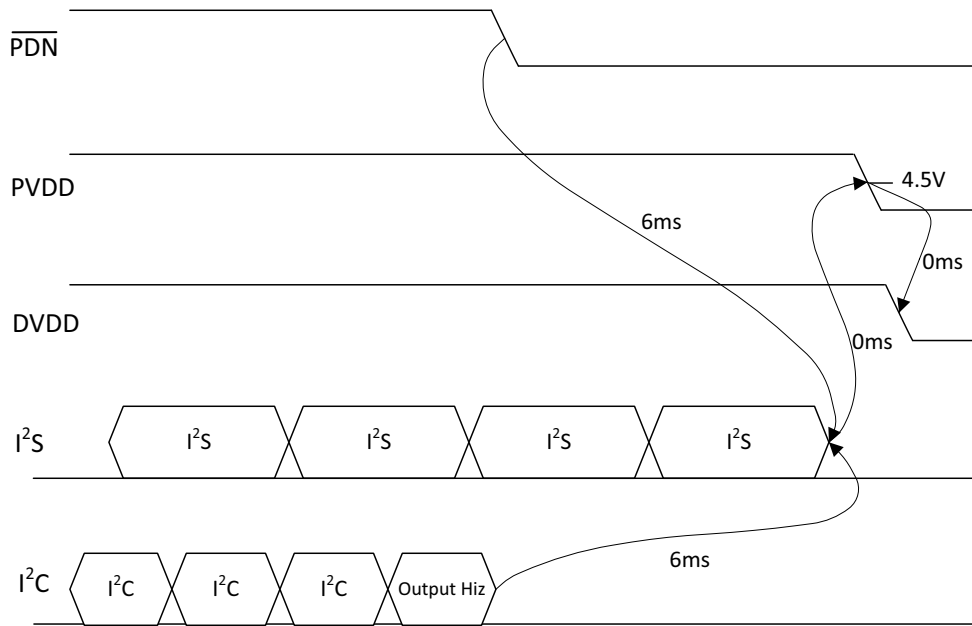


Figure 6-16. Startup sequence

6.5.3.2 Shutdown Procedures

1. The device is in normal operation.
2. Configure the Register `DEVICE_CTRL2` Register [1:0]=00 (DEEP SLEEP) via the I²C control port or Pull $\overline{\text{PDN}}$ low.
3. The clocks can now be stopped and the power supplies brought down.
4. The device is now fully shutdown and powered off.



- A. Before PVDD/DVDD power down, Class D Output driver needs to be disabled by $\overline{\text{PDN}}$ or by I²C.
- B. At least 6ms delay needed based on: LRCLK (Fs) = 48kHz, digital volume = 24dB, digital volume ramp down by 0.5dB every sample period. Changing the value of `DIG_VOL_CTRL2` or `DIG_VOL_CTRL3` registers or changing the or change the LRCLK rate will change the delay time.

Figure 6-17. Power down sequence

6.5.3.3 Protection and Monitoring

6.5.3.3.1 Overcurrent Shutdown (OCSD)

Under severe short-circuit event, such as a short to PVDD or ground, the device uses a peak-current detector, and the affected channel shuts down in < 100 ns if the peak current are enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. The user may restart the affected channel via I²C. An OCSD event activates the fault pin, and the I²C fault register saves a record. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OCSD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.

6.5.3.3.2 DC Detect

If the TAS5802 device measures a DC offset in the output voltage, the `FAULTZ` line is pulled low and the `OUTxx` outputs transition to high impedance, signifying a fault.

6.5.3.3.3 Device Over Temperature Protection

Once the die temperature exceed 160°C (Typical), device will set the output driver from Play mode to Hi-Z Mode. Over temperature shutdown fault reported by [GLOBAL_FAULT2 Register \(Offset = 72h\) \[Reset = 00h\]](#) in Book0/Page0. Set this fault's behavior to Auto-recovery mode, device will come back to play mode automatically once the die temperature drop down to 150°C or device needs re-enter into play mode by clearing fault with [FAULT_CLEAR Register \(Offset = 78h\) \[Reset = 00h\]](#) in Book0/Page0.

6.5.3.3.4 Over Voltage Protection

Once the PVDD voltage exceeds the $OVE_{THRES(PVDD)}$, device will set the output driver from Play mode to Hi-Z mode. Over voltage fault reported by [GLOBAL_FAULT1 Register \(Offset = 71h\) \[Reset = 00h\]](#) in Book0/Page0. Once PVDD voltage returns to normal, device will come back to Play mode. But this bit still keeps 1 unless clear it by [FAULT_CLEAR Register \(Offset = 78h\) \[Reset = 00h\]](#) in Book0/Page0 manually.

6.5.3.3.5 Under Voltage Protection

Once the PVDD voltage drop below the $UVE_{THRES(PVDD)}$ (4 V Typical), device will set the output driver from Play mode to Hi-Z mode. Under voltage fault reported by [GLOBAL_FAULT1 Register \(Offset = 71h\) \[Reset = 00h\]](#) in Book0/Page0. Once PVDD rise above 4.25 V (Typical), device will come back to Play mode. But this bit still keeps 1 unless clear it by [FAULT_CLEAR Register \(Offset = 78h\) \[Reset = 00h\]](#) in Book0/Page0 manually.

6.5.3.3.6 Clock Fault

Once there has any Clock error occurs (Clock Halt, SCLK/LRCLK Ratio Error, PII unlock, FS error) , [FS_MON Register \(Offset = 37h\) \[Reset = 00h\]](#) and [CLKDET_STATUS Register \(Offset = 39h\) \[Reset = 00h\]](#) monitor these errors and real-time report with details, device will enter into Hi-Z mode. Clock Fault reported in [GLOBAL_FAULT1 Register \(Offset = 71h\) \[Reset = 00h\]](#) in Book0/Page0. Once the clock error been removed, device will come back to play mode automatically. But this bit still keeps 1 unless clear it by [FAULT_CLEAR Register \(Offset = 78h\) \[Reset = 00h\]](#) in Book0/Page0 manually.

7 Register Maps

7.1 CONTROL PORT Registers

Table 7-1 lists the memory-mapped registers for the CONTROL_PORT registers. All register offset addresses not listed in Table 7-1 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. CONTROL PORT Registers

Offset	Acronym	Register Name	Section
1h	RESET_CTRL	Reset control	Go
2h	DEVICE_CTRL1	Device control 1	Go
3h	DEVICE_CTRL2	Device control 2	Go
Fh	I2C_PAGE_AUTO_INC	I2C DSP memory access page auto increment	Go
28h	SIG_CH_CTRL	Signal chain control	Go
29h	CLOCK_DET_CTRL	Clock detection control	Go
30h	SDOUT_SEL	SDOUT selection	Go
31h	I2S_CTRL	I2S control 0	Go
33h	SAP_CTRL1	I2S control 1	Go
34h	SAP_CTRL2	I2S control 2	Go
35h	SAP_CTRL3	I2S control 3	Go
37h	FS_MON	FS monitor	Go
38h	BCLK_MON	Bclk monitor	Go
39h	CLKDET_STATUS	Clock detection status	Go
40h	DSP_PGM_MODE	DSP program mode	Go
46h	DSP_CTRL	DSP control	Go
4Ch	DAC_GAIN_LEFT	Left digital volume	Go
4Dh	DAC_GAIN_RIGHT	Right digital volume	Go
4Eh	DIG_VOL_CTRL2	Digital volume control 2	Go
4Fh	DIG_VOL_CTRL3	Digital volume control 3	Go
50h	AUTO_MUTE_CTRL	Auto mute control	Go
51h	AUTO_MUTE_TIME	Auto mute time	Go
53h	ANA_CTRL	Analog control	Go
54h	AGAIN	Analog gain	Go
60h	ADR_CTRL	ADR control	Go
61h	ADR_SEL	ADR output selection	Go
67h	DIE_ID	DIE ID	Go
68h	POWER_STATE	Power State	Go
69h	AUTOMUTE_STATE	Auto mute state	Go
6Ah	RAMP_PHASE_CTRL	Switching clock phase control	Go
6Bh	RAMP_SS_CTRL0	Spread spectrum control 0	Go
6Ch	RAMP_SS_CTRL1	Spread spectrum control 1	Go
70h	CHAN_FAULT	Channel fault	Go
71h	GLOBAL_FAULT1	Global fault 1	Go
72h	GLOBAL_FAULT2	Global fault 2	Go
73h	OT_WARNING	OT Warning	Go
74h	PIN_CONTROL1	Pin control 1	Go
75h	PIN_CONTROL2	Pin control 2	Go
76h	MISC_CONTROL	Miscellaneous control	Go
78h	FAULT_CLEAR	Fault clear	Go

Complex bit access types are encoded to fit into small table cells. [Table 7-2](#) shows the codes that are used for access types in this section.

Table 7-2. CONTROL PORT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.1.1 RESET_CTRL Register (Offset = 1h) [Reset = 00h]

RESET_CTRL is shown in [Figure 7-1](#) and described in [Table 7-3](#).

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Reset control

Figure 7-1. RESET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			RST_MOD	RESERVED			RST_REG
W-0h			W-0h	W-0h			W-0h

Table 7-3. RESET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	W	0h	
4	RST_MOD	W	0h	WRITE CLEAR BIT Reset Modules This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coefficient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in hiz mode. 0: Normal 1: Reset modules
3-1	RESERVED	W	0h	
0	RST_REG	W	0h	WRITE CLEAR BIT Reset Registers This bit resets the mode registers back to their initial values. The RAM content is not cleared. This bit is auto cleared and must be set only when the DAC is in hiz mode (resetting registers when the DAC is running is prohibited and not supported) 0: Normal 1: Reset mode registers

7.1.2 DEVICE_CTRL1 Register (Offset = 2h) [Reset = 00h]

DEVICE_CTRL1 is shown in [Figure 7-2](#) and described in [Table 7-4](#).

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Device control 1

Figure 7-2. DEVICE_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	FSW_SEL			RESERVED		MODULATION	
R/W-0h	R/W-0h			R/W-0h		R/W-0h	

Table 7-4. DEVICE_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	FSW_SEL	R/W	0h	Select PWM switching frequency(Fsw) 3'b 000:768kHz 3'b 001:384kHz Others reserved
3-2	RESERVED	R/W	0h	
1-0	MODULATION	R/W	0h	00:BD mode 01:1SPW mode 10:Hybrid mode 11: Reserved

7.1.3 DEVICE_CTRL2 Register (Offset = 3h) [Reset = 10h]

DEVICE_CTRL2 is shown in [Figure 7-3](#) and described in [Table 7-5](#).

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Device control 2

Figure 7-3. DEVICE_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED			DSP_RST	CH1_MUTE	CH2_MUTE	STATE_CTL	
R/W-0h			R/W-1h	R/W-0h	R/W-0h	R/W-0h	

Table 7-5. DEVICE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	DSP_RST	R/W	1h	DSP reset When the bit is made 0, DSP will start powering up and send out data. This needs to be made 0 only after all the input clocks are settled so that DMA channels do not go out of sync. 0: Normal operation 1: Reset the DSP
3	CH1_MUTE	R/W	0h	Mute Channel 1 This bit issues soft mute request for the ch1. The volume will be smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute
2	CH2_MUTE	R/W	0h	Mute Channel 2 This bit issues soft mute request for the ch2. The volume will be smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute
1-0	STATE_CTL	R/W	0h	Device state control register 00: Deep Sleep 01: Sleep 10: Hi-Z 11: PLAY

7.1.4 I2C_PAGE_AUTO_INC Register (Offset = Fh) [Reset = 00h]

I2C_PAGE_AUTO_INC is shown in [Figure 7-4](#) and described in [Table 7-6](#).

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I2C DSP memory access page auto increment

Figure 7-4. I2C_PAGE_AUTO_INC Register

7	6	5	4	3	2	1	0
RESERVED				PAGE_INC	RESERVED		
R/W-0h				R/W-0h	R/W-0h		

Table 7-6. I2C_PAGE_AUTO_INC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	PAGE_INC	R/W	0h	Page auto increment disable Disable page auto increment mode. for non-zero books. When end of page is reached it goes back to 8th address location of next page when this bit is 0. When this bit is 1 it goes to 0 th location of current page itself like in older part. 0: Enable Page auto increment 1: Disable Page auto increment
2-0	RESERVED	R/W	0h	

7.1.5 SIG_CH_CTRL Register (Offset = 28h) [Reset = 00h]

SIG_CH_CTRL is shown in [Figure 7-5](#) and described in [Table 7-7](#).

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Signal chain control

Figure 7-5. SIG_CH_CTRL Register

7	6	5	4	3	2	1	0
BCLK_RATIO				FS_MODE			
R/W-0h				R/W-0h			

Table 7-7. SIG_CH_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BCLK_RATIO	R/W	0h	These bits indicate the configured BCLK ratio, the number of BCLK clocks in one audio frame. 4'b0000: Auto detection 4'b0011:32FS 4'b0101:64FS 4'b0111:128FS 4'b1001:256FS 4'b1011:512FS Others reserved.
3-0	FS_MODE	R/W	0h	FS Speed Mode These bits select the FS operation mode, which must be set according to the current audio sampling rate. 4'b0000 Auto detection 4'b0110 32kHz 4'b1000 44.1kHz 4'b1001 48kHz 4'b1010 88.2kHz 4'b1011 96kHz Others Reserved

7.1.6 CLOCK_DET_CTRL Register (Offset = 29h) [Reset = 00h]

CLOCK_DET_CTRL is shown in [Figure 7-6](#) and described in [Table 7-8](#).

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Clock detection control

Figure 7-6. CLOCK_DET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	DET_PLL	BCLK_RANGE	DET_FS	DET_BCLK	DET_BCLKMISS	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 7-8. CLOCK_DET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	DET_PLL	R/W	0h	Ignore PLL overrate Detection This bit controls whether to ignore the PLL overrate detection. The PLL must be slow than 150MHz or an error will be reported. When ignored, a PLL overrate error will not cause a clock error. 0: Regard PLL overrate detection 1: Ignore PLL overrate detection
5	BCLK_RANGE	R/W	0h	Ignore BCLK Range Detection This bit controls whether to ignore the BCLK range detection. The BCLK must be stable between 256kHz and 50MHz or an error will be reported. When ignored, a BCLK range error will not cause a clock error. 0: Regard BCLK Range detection 1: Ignore BCLK Range detection
4	DET_FS	R/W	0h	Ignore FS Error Detection This bit controls whether to ignore the FS Error detection. When ignored, FS error will not cause a clock error. But CLKDET_STATUS will report fs error. 0: Regard FS detection 1: Ignore FS detection
3	DET_BCLK	R/W	0h	Ignore BCLK Detection This bit controls whether to ignore the BCLK detection against LRCLK. The BCLK must be stable between 32FS and 512FS inclusive or an error will be reported. When ignored, a BCLK error will not cause a clock error. 0: Regard BCLK detection 1: Ignore BCLK detection
2	DET_BCLKMISS	R/W	0h	Ignore BCLK Missing Detection This bit controls whether to ignore the BCLK missing detection. When ignored an BCLK missing will not cause a clock error. 0: Regard BCLK missing detection 1: Ignore BCLK missing detection
1-0	RESERVED	R/W	0h	

7.1.7 SDOUT_SEL Register (Offset = 30h) [Reset = 04h]

SDOUT_SEL is shown in [Figure 7-7](#) and described in [Table 7-9](#).

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SDOUT selection

Figure 7-7. SDOUT_SEL Register

7	6	5	4	3	2	1	0
RESERVED						SDOUT_MOD	SDOUT_SEL
R/W-1h						R/W-0h	R/W-0h

Table 7-9. SDOUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	1h	
1	SDOUT_MOD	R/W	0h	Set SDOUT as open drain. This bit only applies to GPO functions with Output push-pull mode and has no effect on functions that use Open Drain mode by default 0: Output Push-pull mode 1: Open drain mode
0	SDOUT_SEL	R/W	0h	SDOUT Select This bit selects what is being output as SDOUT via GPIO pins. 0: SDOUT is the DSP output (post-processing) 1: SDOUT is the DSP input (pre-processing)

7.1.8 I2S_CTRL Register (Offset = 31h) [Reset = 00h]

I2S_CTRL is shown in [Figure 7-8](#) and described in [Table 7-10](#).

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I2S control 0

Figure 7-8. I2S_CTRL Register

7	6	5	4	3	2	1	0
RESERVED		BCLK_INV	RESERVED				
R/W-0h		R/W-0h	R/W-0h				

Table 7-10. I2S_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	BCLK_INV	R/W	0h	BCLK Polarity This bit sets the inverted BCLK mode. In inverted BCLK mode, the DAC assumes that the LRCLK and DIN edges are aligned to the rising edge of the BCLK. Normally they are assumed to be aligned to the falling edge of the BCLK. 0: Normal BCLK mode 1: Inverted BCLK mode
4-0	RESERVED	R/W	0h	

7.1.9 SAP_CTRL1 Register (Offset = 33h) [Reset = 02h]

SAP_CTRL1 is shown in [Figure 7-9](#) and described in [Table 7-11](#).

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I2S control 1

Figure 7-9. SAP_CTRL1 Register

7	6	5	4	3	2	1	0
SHIFT_MSB	RESERVED	DATA_FMT		LRCLK_PULSE		FRAME_LENGTH	
R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-2h	

Table 7-11. SAP_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SHIFT_MSB	R/W	0h	I2S Shift MSB. Combine with the 8 bits in low register 34h.
6	RESERVED	R/W	0h	
5-4	DATA_FMT	R/W	0h	I2S Data Format These bits control both input and output audio interface formats for DAC operation. 00: I2S 01: DSP/TDM 10: RTJ 11: LTJ
3-2	LRCLK_PULSE	R/W	0h	If the LRCLK pulse is shorter than 8 x BCLK, set bit 0-1 to '01' Otherwise, keep these bits as default value '00' 00: High width of LRCLK pulse is equal or greater than 8 cycles of BCLK 01: High width of LRCLK pulse is less than 8 cycles of BCLK
1-0	FRAME_LENGTH	R/W	2h	I2S Word Length These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

7.1.10 SAP_CTRL2 Register (Offset = 34h) [Reset = 00h]

SAP_CTRL2 is shown in [Figure 7-10](#) and described in [Table 7-12](#).

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I2S control 2

Figure 7-10. SAP_CTRL2 Register

7	6	5	4	3	2	1	0
SHIFT_LSB							
R/W-0h							

Table 7-12. SAP_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SHIFT_LSB	R/W	0h	I2S Shift LSB These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCLK from the starting (MSB) of audio frame to the starting of the desired audio sample. 8'b00000000: offset = 0 BCLK (no offset) 8'b00000001: offset = 1 BCLK 8'b00000010: offset = 2 BCLKs ... 8'b11111111: offset = 512 BCLKs

7.1.11 SAP_CTRL3 Register (Offset = 35h) [Reset = 11h]

SAP_CTRL3 is shown in [Figure 7-11](#) and described in [Table 7-13](#).

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I2S control 3

Figure 7-11. SAP_CTRL3 Register

7	6	5	4	3	2	1	0
RESERVED		CH1_DAC		RESERVED		CH2_DAC	
R/W-0h		R/W-1h		R/W-0h		R/W-1h	

Table 7-13. SAP_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-4	CH1_DAC	R/W	1h	Channel 1 DAC Data Path These bits control the channel 1 audio data path connection. 00: Zero data (mute) 01: Ch1 data 10: Ch2 data 11: Reserved (do not set)
3-2	RESERVED	R/W	0h	
1-0	CH2_DAC	R/W	1h	Channel 2 DAC Data Path These bits control the channel 2 audio data path connection. 00: Zero data (mute) 01: Ch2 data 10: Ch1 data 11: Reserved (do not set)

7.1.12 FS_MON Register (Offset = 37h) [Reset = 00h]

FS_MON is shown in [Figure 7-12](#) and described in [Table 7-14](#).

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FS monitor

Figure 7-12. FS_MON Register

7	6	5	4	3	2	1	0
RESERVED		BCLKRATION_MSB		FS_MON			
R-0h		R-0h		R-0h			

Table 7-14. FS_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-4	BCLKRATION_MSB	R	0h	2 MSB of detected BCLK ratio. These bits indicate the currently detected BCLK ratio, the number of BCLK clocks in one audio frame. Combine with the 8 bits in low register 38h. BCLK = 32 FS~512 FS
3-0	FS_MON	R	0h	These bits indicate the currently detected audio sampling rate. 4'b0000 FS Error 4'b0010 8kHz 4'b0100 16kHz 4'b0110 32kHz 4'b1000 Reserved 4'b1001 48kHz 4'b1011 96kHz Others Reserved

7.1.13 BCLK_MON Register (Offset = 38h) [Reset = 00h]

BCLK_MON is shown in [Figure 7-13](#) and described in [Table 7-15](#).

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Bclk monitor

Figure 7-13. BCLK_MON Register

7	6	5	4	3	2	1	0
BCLKRATIO_LSB							
R-0h							

Table 7-15. BCLK_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BCLKRATIO_LSB	R	0h	These bits indicate the currently detected BCLK ratio, the number of BCLK clocks in one audio frame. BCLK = 32 FS~512 FS

7.1.14 CLKDET_STATUS Register (Offset = 39h) [Reset = 00h]

CLKDET_STATUS is shown in [Figure 7-14](#) and described in [Table 7-16](#).

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Clock detection status

Figure 7-14. CLKDET_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		BCLK_OVERR ATE	PLL_OVERRAT E	PLL_LOCKED	BCLK_MISSIN G	BCLK_VALID	FS_VALID
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-16. CLKDET_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	BCLK_OVERRATE	R	0h	This bit indicates whether the BCLK is overrate or underrate. 0: BCLK is underrate 1: BCLK is overrate
4	PLL_OVERRATE	R	0h	This bit indicates whether the PLL is overrate or not. 0: PLL is underrate 1: PLL is overrate
3	PLL_LOCKED	R	0h	This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled. 0: PLL is locked 1: PLL is not locked
2	BCLK_MISSING	R	0h	This bit indicates whether the BCLK is missing or not. 0: BCLK is normal 1: BCLK is missing
1	BCLK_VALID	R	0h	This bit indicates whether the BCLK is valid or not. The BCLK ratio must be stable and in the range of 32-512FS to be valid. 0: BCLK is valid 1: BCLK is not valid
0	FS_VALID	R	0h	In auto detection mode(reg_fsmode=0),this bit indicated whether the audio sampling rate is valid. In non auto detection mode(reg_fsmode!=0), FS error indicates that configured sampling frequency set by LRCLK(FS) is different with detected sampling frequency. Even if FS Error Detection Ignore is set, this flag will be also asserted. 0: Sampling rate is valid 1: Not valid

7.1.15 DSP_PGM_MODE Register (Offset = 40h) [Reset = 01h]

DSP_PGM_MODE is shown in [Figure 7-15](#) and described in [Table 7-17](#).

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DSP program mode

Figure 7-15. DSP_PGM_MODE Register

7	6	5	4	3	2	1	0
RESERVED				CH1_HIZ	CH2_HIZ	RESERVED	
R/W-0h				R/W-0h	R/W-0h	R/W-1h	

Table 7-17. DSP_PGM_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	CH1_HIZ	R/W	0h	0: Normal operation 1: Force CH1 to Hi-Z mode
2	CH2_HIZ	R/W	0h	0: Normal operation 1: Force CH2 to Hi-Z mode
1-0	RESERVED	R/W	1h	

7.1.16 DSP_CTRL Register (Offset = 46h) [Reset = 01h]

DSP_CTRL is shown in [Figure 7-16](#) and described in [Table 7-18](#).

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DSP control

Figure 7-16. DSP_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			PROC_RATE	RESERVED			
R/W-0h			R/W-0h	R/W-1h			

Table 7-18. DSP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	PROC_RATE	R/W	0h	0: 96k processing flow, 2.0 processing SRC enabled 1: 48k processing flow, 2.1 processing flow enabled
3-0	RESERVED	R/W	1h	

7.1.17 DAC_GAIN_LEFT Register (Offset = 4Ch) [Reset = 30h]

DAC_GAIN_LEFT is shown in [Figure 7-17](#) and described in [Table 7-19](#).

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Left digital volume

Figure 7-17. DAC_GAIN_LEFT Register

7	6	5	4	3	2	1	0
CH1_PGA							
R/W-30h							

Table 7-19. DAC_GAIN_LEFT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_PGA	R/W	30h	Channel 1 Volume These bits control the ch1 digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 8'b00000000: +24.0 dB 8'b00000001: +23.5 dB ... 8'b00101111: +0.5 dB 8'b00110000: 0.0 dB 8'b00110001: -0.5 dB ... 8'b11111110: -103 dB 8'b11111111: Mute

7.1.18 DAC_GAIN_RIGHT Register (Offset = 4Dh) [Reset = 30h]

DAC_GAIN_RIGHT is shown in [Figure 7-18](#) and described in [Table 7-20](#).

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Right digital volume

Figure 7-18. DAC_GAIN_RIGHT Register

7	6	5	4	3	2	1	0
CH2_PGA							
R/W-30h							

Table 7-20. DAC_GAIN_RIGHT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH2_PGA	R/W	30h	Channel 2 Volume These bits control the ch2 digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 8'b00000000: +24.0 dB 8'b00000001: +23.5 dB ... 8'b00101111: +0.5 dB 8'b00110000: 0.0 dB 8'b00110001: -0.5 dB ... 8'b11111110: -103 dB 8'b11111111: Mute

7.1.19 DIG_VOL_CTRL2 Register (Offset = 4Eh) [Reset = 33h]

DIG_VOL_CTRL2 is shown in [Figure 7-19](#) and described in [Table 7-21](#).

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Digital volume control 2

Figure 7-19. DIG_VOL_CTRL2 Register

7	6	5	4	3	2	1	0
VNDF		VNDS		VNUF		VNUS	
R/W-0h		R/W-3h		R/W-0h		R/W-3h	

Table 7-21. DIG_VOL_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VNDF	R/W	0h	Digital Volume Normal Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	VNDS	R/W	3h	Digital Volume Normal Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-2	VNUF	R/W	0h	Digital Volume Normal Ramp Up Frequency These bits control the frequency of the digital volume updates when the volume is ramping up 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
1-0	VNUS	R/W	3h	Digital Volume Normal Ramp Up Step These bits control the step of the digital volume updates when the volume is ramping up 00: Increment by 4 dB for each update 01: Increment by 2 dB for each update 10: Increment by 1 dB for each update 11: Increment by 0.5 dB for each update

7.1.20 DIG_VOL_CTRL3 Register (Offset = 4Fh) [Reset = 30h]

DIG_VOL_CTRL3 is shown in [Figure 7-20](#) and described in [Table 7-22](#).

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Digital volume control 3

Figure 7-20. DIG_VOL_CTRL3 Register

7	6	5	4	3	2	1	0
VEDF		VEDS		RESERVED			
R/W-0h		R/W-3h		R/W-0h			

Table 7-22. DIG_VOL_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VEDF	R/W	0h	Digital Volume Emergency Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	VEDS	R/W	3h	Digital Volume Emergency Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-0	RESERVED	R/W	0h	

7.1.21 AUTO_MUTE_CTRL Register (Offset = 50h) [Reset = 00h]

AUTO_MUTE_CTRL is shown in [Figure 7-21](#) and described in [Table 7-23](#).

Return to the [Summary Table](#).

Auto mute control

Figure 7-21. AUTO_MUTE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED				AM_CTL	AMUTE_CH2	AMUTE_CH1	
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-23. AUTO_MUTE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	AM_CTL	R/W	0h	0: Auto mute channel 1 and channel 2 independently 1: Auto mute channel 1 and channel 2 only when both channels are about to be auto muted
1	AMUTE_CH2	R/W	0h	Auto Mute Channel 2 This bit enables or disables auto mute on Channel 2 0: Disable Channel 2 auto mute 1: Enable Channel 2 auto mute
0	AMUTE_CH1	R/W	0h	Auto Mute Channel 1 This bit enables or disables auto mute on Channel 1 0: Disable Channel 1 auto mute 1: Enable Channel 1 auto mute

7.1.22 AUTO_MUTE_TIME Register (Offset = 51h) [Reset = 55h]

AUTO_MUTE_TIME is shown in [Figure 7-22](#) and described in [Table 7-24](#).

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Auto mute time

Figure 7-22. AUTO_MUTE_TIME Register

7	6	5	4	3	2	1	0
RESERVED	CH1_AMT			RESERVED	CH2_AMT		
R/W-0h	R/W-5h			R/W-0h	R/W-5h		

Table 7-24. AUTO_MUTE_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	CH1_AMT	R/W	5h	Auto Mute Time for Channel 1 These bits specify the length of consecutive zero samples at ch1 before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec
3	RESERVED	R/W	0h	
2-0	CH2_AMT	R/W	5h	Auto Mute Time for Channel 2 These bits specify the length of consecutive zero samples at ch2 before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec

7.1.23 ANA_CTRL Register (Offset = 53h) [Reset = 00h]

ANA_CTRL is shown in [Figure 7-23](#) and described in [Table 7-25](#).

Return to the [Summary Table](#).

Analog control

Figure 7-23. ANA_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	BW_CTL	RESERVED				PHASE_CTL	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h

Table 7-25. ANA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-5	BW_CTL	R/W	0h	Class D Loop Bandwidth 00: 80kHz 01: 100kHz 10: 120kHz 11: 175kHz When Fsw=384kHz, 100kHz bandwidth is selected for high audio performance. With Fsw=768kHz, 175kHz bandwidth should be selected for high audio performance.
4-1	RESERVED	R/W	0h	
0	PHASE_CTL	R/W	0h	0: Out of phase 1: In phase

7.1.24 AGAIN Register (Offset = 54h) [Reset = 06h]

AGAIN is shown in [Figure 7-24](#) and described in [Table 7-26](#).

Return to the [Summary Table](#).

Analog gain

Figure 7-24. AGAIN Register

7	6	5	4	3	2	1	0
RESERVED				AGAIN			
R/W-0h				R/W-6h			

Table 7-26. AGAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-0	AGAIN	R/W	6h	Analog Gain Control This bit controls the analog gain b'00000: 0dB b'00001: -0.5dB b'00110: -3dB 11111: -15.5 dB

7.1.25 ADR_CTRL Register (Offset = 60h) [Reset = 00h]

ADR_CTRL is shown in [Figure 7-25](#) and described in [Table 7-27](#).

Return to the [Summary Table](#).

ADR control

Figure 7-25. ADR_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							ADR_OE
R/W-0h							R/W-0h

Table 7-27. ADR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	ADR_OE	R/W	0h	ADR Output Enable This bit sets the direction of the ADR pin 0: ADR is input 1: ADR is output

7.1.26 ADR_SEL Register (Offset = 61h) [Reset = 00h]

ADR_SEL is shown in [Figure 7-26](#) and described in [Table 7-28](#).

Return to the [Summary Table](#).

ADR output selection

Figure 7-26. ADR_SEL Register

7	6	5	4	3	2	1	0
RESERVED				ADR_SEL			
R/W-0h				R/W-0h			

Table 7-28. ADR_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-0	ADR_SEL	R/W	0h	b'00000: off (low) b'00011: Auto mute flag (asserted when both L and R channels are auto muted) b'00100: Auto mute flag for left channel b'00101: Auto mute flag for right channel b'00110: Clock invalid flag (clock error or clock missing) b'00111: PLL lock flag b'01000: Warning b'01001: Serial audio interface data output (SDOUT) b'01011: ADR as FAULTZ output Others: reserved

7.1.27 DIE_ID Register (Offset = 67h) [Reset = A8h]

DIE_ID is shown in [Figure 7-27](#) and described in [Table 7-29](#).

Return to the [Summary Table](#).

DIE ID

Figure 7-27. DIE_ID Register

7	6	5	4	3	2	1	0
DIE_ID							
R-A8h							

Table 7-29. DIE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID	R	A8h	The Die ID for TAS5802

7.1.28 POWER_STATE Register (Offset = 68h) [Reset = 00h]

POWER_STATE is shown in [Figure 7-28](#) and described in [Table 7-30](#).

Return to the [Summary Table](#).

Power State

Figure 7-28. POWER_STATE Register

7	6	5	4	3	2	1	0
RESERVED						STATE_RPT	
R-0h						R-0h	

Table 7-30. POWER_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1-0	STATE_RPT	R	0h	00: Deep sleep 01: Sleep 10: Hi-Z 11: Play

7.1.29 AUTOMUTE_STATE Register (Offset = 69h) [Reset = 00h]

AUTOMUTE_STATE is shown in [Figure 7-29](#) and described in [Table 7-31](#).

Return to the [Summary Table](#).

Auto mute state

Figure 7-29. AUTOMUTE_STATE Register

7	6	5	4	3	2	1	0
RESERVED						CH2MUTE_ST ATUS	CH1MUTE_ST ATUS
R-0h						R-0h	R-0h

Table 7-31. AUTOMUTE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	CH2MUTE_STATUS	R	0h	This bit indicates the auto mute status for Channel 2. 0: Not auto muted 1: Auto muted
0	CH1MUTE_STATUS	R	0h	This bit indicates the auto mute status for Channel 1. 0: Not auto muted 1: Auto muted

7.1.30 RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h]

RAMP_PHASE_CTRL is shown in [Figure 7-30](#) and described in [Table 7-32](#).

Return to the [Summary Table](#).

Switching clock phase control

Figure 7-30. RAMP_PHASE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED				RAMPPHASE_SEL		I2S_SYNC_EN	PHASE_SYNC_EN
R/W-0h				R/W-0h		R/W-0h	R/W-0h

Table 7-32. RAMP_PHASE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3-2	RAMPPHASE_SEL	R/W	0h	Select ramp clock phase when multi devices are integrated in one system to reduce EMI and peak supply peak current, it is recommended set all devices the same RAMP frequency and same spread spectrum. it must be set before driving device into PLAY mode if this feature is needed. 00: 0 degree 01: 45 degree 10: 90 degree 11: 135 degree all of above have a 45 degree of phase shift
1	I2S_SYNC_EN	R/W	0h	Use I2S to synchronize output PWM phase 0: Disable 1: Enable
0	PHASE_SYNC_EN	R/W	0h	0: RAMP phase sync disable 1: RAMP phase sync enable

7.1.31 RAMP_SS_CTRL0 Register (Offset = 6Bh) [Reset = 00h]

RAMP_SS_CTRL0 is shown in [Figure 7-31](#) and described in [Table 7-33](#).

Return to the [Summary Table](#).

Spread spectrum control 0

Figure 7-31. RAMP_SS_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED						RDM_EN	TRI_EN
R/W-0h						R/W-0h	R/W-0h

Table 7-33. RAMP_SS_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	RDM_EN	R/W	0h	0: Random SS disable 1: Random SS enable
0	TRI_EN	R/W	0h	0: Triangle SS disable 1: Triangle SS enable

7.1.32 RAMP_SS_CTRL1 Register (Offset = 6Ch) [Reset = 00h]

RAMP_SS_CTRL1 is shown in [Figure 7-32](#) and described in [Table 7-34](#).

Return to the [Summary Table](#).

Spread spectrum control 1

Figure 7-32. RAMP_SS_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	RDM_CTL			TRI_CTL			
R/W-0h	R/W-0h			R/W-0h			

Table 7-34. RAMP_SS_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	RDM_CTL	R/W	0h	Random SS range control For Fsw of 384kHz 3'b000: SS range +/- 0.62% 3'b010: SS range +/- 1.88% 3'b011: SS range +/- 4.38% 3'b100: SS range +/- 9.38% 3'b101: SS range +/- 19.38% Others: reserved For Fsw of 768kHz 3'b000: SS range - 1.25% 3'b001: SS range +/- 1.25% 3'b010: SS range +/- 3.75% 3'b011: SS range +/- 8.75% 3'b100: SS range +/- 18.75% 3'b101: SS range +/- 38.75% Others: reserved
3-0	TRI_CTL	R/W	0h	Triangle SS frequency and range control 4'b0000: 24kHz SS +/- 5% 4'b0001: 24kHz SS +/- 10% 4'b0010: 24kHz SS +/- 20% 4'b0011: 24kHz SS +/- 25% 4'b0100: 48kHz SS +/- 5% 4'b0101: 48kHz SS +/- 10% 4'b0110: 48kHz SS +/- 20% 4'b0111: 48kHz SS +/- 25% 4'b1000: 32kHz SS +/- 5% 4'b1001: 32kHz SS +/- 10% 4'b1010: 32kHz SS +/- 20% 4'b1011: 32kHz SS +/- 25% 4'b1100: 16kHz SS +/- 5% 4'b1101: 16kHz SS +/- 10% 4'b1110: 16kHz SS +/- 20% 4'b1111: 16kHz SS +/- 25%

7.1.33 CHAN_FAULT Register (Offset = 70h) [Reset = 00h]

CHAN_FAULT is shown in [Figure 7-33](#) and described in [Table 7-35](#).

Return to the [Summary Table](#).

Channel fault

Figure 7-33. CHAN_FAULT Register

7	6	5	4	3	2	1	0
RESERVED				CH1DC	CH2DC	CH1OC	CH2OC
R-0h				R-0h	R-0h	R-0h	R-0h

Table 7-35. CHAN_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	CH1DC	R	0h	Channel 1 DC fault. Once there is a DC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
2	CH2DC	R	0h	Channel 2 DC fault. Once there is a DC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
1	CH1OC	R	0h	Channel 1 over current fault. Once there is a OC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
0	CH2OC	R	0h	Channel 2 over current fault. Once there is a OC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.

7.1.34 GLOBAL_FAULT1 Register (Offset = 71h) [Reset = 00h]

GLOBAL_FAULT1 is shown in [Figure 7-34](#) and described in [Table 7-36](#).

Return to the [Summary Table](#).

Global fault 1

Figure 7-34. GLOBAL_FAULT1 Register

7	6	5	4	3	2	1	0
RESERVED	BQWRTFAULT_FLAG	RESERVED			CLKFAULT_FLAG	PVDDOV_FLAG	PVDDUV_FLAG
R-0h	R-0h	R-0h			R-0h	R-0h	R-0h

Table 7-36. GLOBAL_FAULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	BQWRTFAULT_FLAG	R	0h	0: The recent BQ is written successfully 1: The recent BQ is written failed
5-3	RESERVED	R	0h	
2	CLKFAULT_FLAG	R	0h	Clock fault. Once there is a Clock fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clock fault works with an auto-recovery mode, once the clock error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
1	PVDDOV_FLAG	R	0h	PVDD OV fault. Once there is a OV fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). OV fault works with an auto-recovery mode, once the OV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
0	PVDDUV_FLAG	R	0h	PVDD UV fault. Once there is a UV fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). UV fault works with an auto-recovery mode, once the UV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.

7.1.35 GLOBAL_FAULT2 Register (Offset = 72h) [Reset = 00h]

GLOBAL_FAULT2 is shown in [Figure 7-35](#) and described in [Table 7-37](#).

Return to the [Summary Table](#).

Global fault 2

Figure 7-35. GLOBAL_FAULT2 Register

7	6	5	4	3	2	1	0
RESERVED							OTSD_FLAG
R-0h							R-0h

Table 7-37. GLOBAL_FAULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	OTSD_FLAG	R	0h	Over temperature shut down fault Once there is a OT fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). OV fault works with an autorecovery mode, once the OV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.

7.1.36 OT_WARNING Register (Offset = 73h) [Reset = 00h]

OT_WARNING is shown in [Figure 7-36](#) and described in [Table 7-38](#).

Return to the [Summary Table](#).

OT Warning

Figure 7-36. OT_WARNING Register

7	6	5	4	3	2	1	0
RESERVED					OTW_FLAG	RESERVED	
R-0h					R-0h	R-0h	

Table 7-38. OT_WARNING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2	OTW_FLAG	R	0h	0: No temperature warning 1: Over temperature warning is triggered
1-0	RESERVED	R	0h	

7.1.37 PIN_CONTROL1 Register (Offset = 74h) [Reset = 00h]

PIN_CONTROL1 is shown in [Figure 7-37](#) and described in [Table 7-39](#).

Return to the [Summary Table](#).

Pin control 1

Figure 7-37. PIN_CONTROL1 Register

7	6	5	4	3	2	1	0
MASK_OTSD	MASK_DVDDU V	MASK_DVDDO V	MASK_CLKER ROR	MASK_PVDDU V	MASK_PVDDO V	MASK_DC	MASK_OC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-39. PIN_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_OTSD	R/W	0h	0: Enable OTSD fault report 1: Mask OTSD fault report
6	MASK_DVDDUV	R/W	0h	0: Enable DVDD UV fault report 1: Mask DVDD UV report
5	MASK_DVDDOV	R/W	0h	0: Enable DVDD OV fault report 1: Mask DVDD OV fault report
4	MASK_CLKERROR	R/W	0h	0: Enable CLK fault report 1: Mask CLK fault report
3	MASK_PVDDUV	R/W	0h	0: Enable UV fault report 1: Mask UV fault report
2	MASK_PVDDOV	R/W	0h	0: Enable OV fault report 1: Mask OV fault report
1	MASK_DC	R/W	0h	0: Enable DC fault report 1: Mask DC fault report
0	MASK_OC	R/W	0h	0: Enable OC fault report 1: Mask OC fault report

7.1.38 PIN_CONTROL2 Register (Offset = 75h) [Reset = F8h]

PIN_CONTROL2 is shown in [Figure 7-38](#) and described in [Table 7-40](#).

Return to the [Summary Table](#).

Pin control 2

Figure 7-38. PIN_CONTROL2 Register

7	6	5	4	3	2	1	0
RESERVED		CLKFAULTLATCH_EN	OTSDLATCH_EN	OTWLATCH_EN	MASK_OTW	RESERVED	
R/W-3h		R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	

Table 7-40. PIN_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	3h	
5	CLKFAULTLATCH_EN	R/W	1h	0: Disable CLK fault latch 1: Enable CLK fault latch
4	OTSDLATCH_EN	R/W	1h	0: Disable OTSD fault latch 1: Enable OTSD fault latch
3	OTWLATCH_EN	R/W	1h	0: Disable OTW warning latch 1: Enable OTW warning latch
2	MASK_OTW	R/W	0h	0: Enable OTW warning report 1: Mask OTW warning report
1-0	RESERVED	R/W	0h	

7.1.39 MISC_CONTROL Register (Offset = 76h) [Reset = 00h]

MISC_CONTROL is shown in [Figure 7-39](#) and described in [Table 7-41](#).

Return to the [Summary Table](#).

Miscellaneous control

Figure 7-39. MISC_CONTROL Register

7	6	5	4	3	2	1	0
CLKDET_LATCH	RESERVED		OTSD_AUTOREC	RESERVED			
R/W-0h	R/W-0h		R/W-0h	R/W-0h			

Table 7-41. MISC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLKDET_LATCH	R/W	0h	1: Latch clock detection status 0: No latch clock detection status
6-5	RESERVED	R/W	0h	
4	OTSD_AUTOREC	R/W	0h	0: Disable OTSD auto recovery 1: Enable OTSD auto recovery
3-0	RESERVED	R/W	0h	

7.1.40 FAULT_CLEAR Register (Offset = 78h) [Reset = 00h]

FAULT_CLEAR is shown in [Figure 7-40](#) and described in [Table 7-42](#).

Return to the [Summary Table](#).

Fault clear

Figure 7-40. FAULT_CLEAR Register

7	6	5	4	3	2	1	0
FAULT_CLR		RESERVED					
W-0h		W-0h					

Table 7-42. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FAULT_CLR	W	0h	WRITE CLEAR BIT 0: No fault clear 1: Clear analog fault
6-0	RESERVED	W	0h	

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This section details the information required to configure the device for several popular configurations and provides guidance on integrating the TAS5802 device into the larger system.

8.1.1 Bootstrap Capacitors

The output stage of the TAS5802 uses a high-side NMOS driver, rather than a PMOS driver. To generate the gate driver voltage for the high-side NMOS, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.22µF capacitors to connect the appropriate output pin (OUT_X) to the bootstrap pin (BST_X). For example, connect a 0.22µF capacitor between OUT_A and BST_A for bootstrapping the A channel. Similarly, connect another 0.22µF capacitor between the OUT_B and BST_B pins for the B channel inverting output.

8.1.2 Inductor Selections

It is required that the peak current is smaller than the OCP (Over current protection) value which is 5A, there are 3 cases which cause high peak current flow through inductor.

1. During power up (idle state, no audio input), the duty cycle increases from 0 to θ .

$$I_{peak_power_up} \approx PVDD \times \sqrt{C/L} \times \sin(1/\sqrt{L \times C} \times \theta / F_{sw}) \quad (1)$$

Note

$\theta=0.5$ (BD Modulation, used in [Table 8-1](#)), 0.14 (1SPW Modulation), 0.14 (Hybrid Modulation). This formula just provide a rough estimation, suggest to measure the start-up current based on your LC filter.

Table 8-1. Peak current during power up

PVDD	L (µH)	C (µF)	Fsw (kHz)	$I_{peak_power_up}$
20	4.7	0.68	384	5.06A (>5A OCP), not recommended
20	4.7	0.68	768	2.71A
20	10	0.68	384	2.5A
20	10	0.68	768	1.29A
12	4.7	0.68	384	2.77A
12	10	0.68	384	1.29A

2. During music playing, some audio burst signal (high frequency) with very hard PVDD clipping will cause PWM duty cycle increase dramatically. This is the worst case and it rarely happens.

$$I_{peak_clipping} \approx PVDD \times (1 - \theta) / (F_{sw} \times L) \quad (2)$$

3. Peak current due to Max output power. Ignore the ripple current flow through capacitor here.

$$I_{peak_output_power} \approx \sqrt{2 \times Max_Output_Power / R_{speaker_Load}} \quad (3)$$

Same PVDD and switching frequency, larger inductance means smaller idle current for lower power dissipation.

It's suggested that inductor's saturation current I_{sat} , is larger than the amplifier's peak current during power-up and play audio.

$$I_{SAT} \geq \max(I_{peak_power_up}, I_{peak_clipping}, I_{peak_output_power}) \quad (4)$$

In addition, the effective inductance at the peak current is required to be at least 80% of the inductance value in [Table 8-2](#), to meet datasheet specifications.

The minimum inductance is given in [Table 8-2](#).

Table 8-2. LC filter recommendation

Switching Frequency (kHz)	Modulation Scheme	Recommended Minimum Inductance (uH) for LC filter design
1024	1SPW	3.3 μ H (or larger) + Capacitor (0.22uF~0.68uF)
768		4.7 μ H (or larger) + Capacitor (0.22uF~0.68uF)
384 or 480		10 μ H (or larger) +Capacitor (0.22uF~0.68uF)
384~1024	BD	8.2uH (or Larger) +Capacitor (0.22uF~0.68uF)

For inductor selection refer to [LCFILTER-CALC-TOOL](#).

8.1.3 Power Supply Decoupling

To ensure high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with some good quality, low ESL, Low ESR capacitors larger than 22 μ F. These capacitors bypasses low frequency noise to the ground plane. For high frequency decoupling, place 1 μ F or 0.1 μ F capacitors as close as possible to the PVDD pins of the device.

8.1.4 Output EMI Filtering

The TAS5802 device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the L-C Filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole filter.

The L-C filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the L-C filter is determined by several system level constraints. In some low-power use cases that have no other circuits which are sensitive to EMI, a simple ferrite bead or a ferrite bead plus a capacitor can replace the tradition large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors can be used due to audio characteristics. Refer to the application report [Class-D LC Filter Design \(SLOA119\)](#) for a detailed description on the proper component selection and design of an L-C filter based upon the desired load and response.

8.2 Typical Applications

8.2.1 2.0 (Stereo BTL) System

In the 2.0 system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

Figure 8-1 and Figure 8-2 shows the 2.0 (Stereo BTL) system application with a ferrite bead filter and L-C filter, respectively.

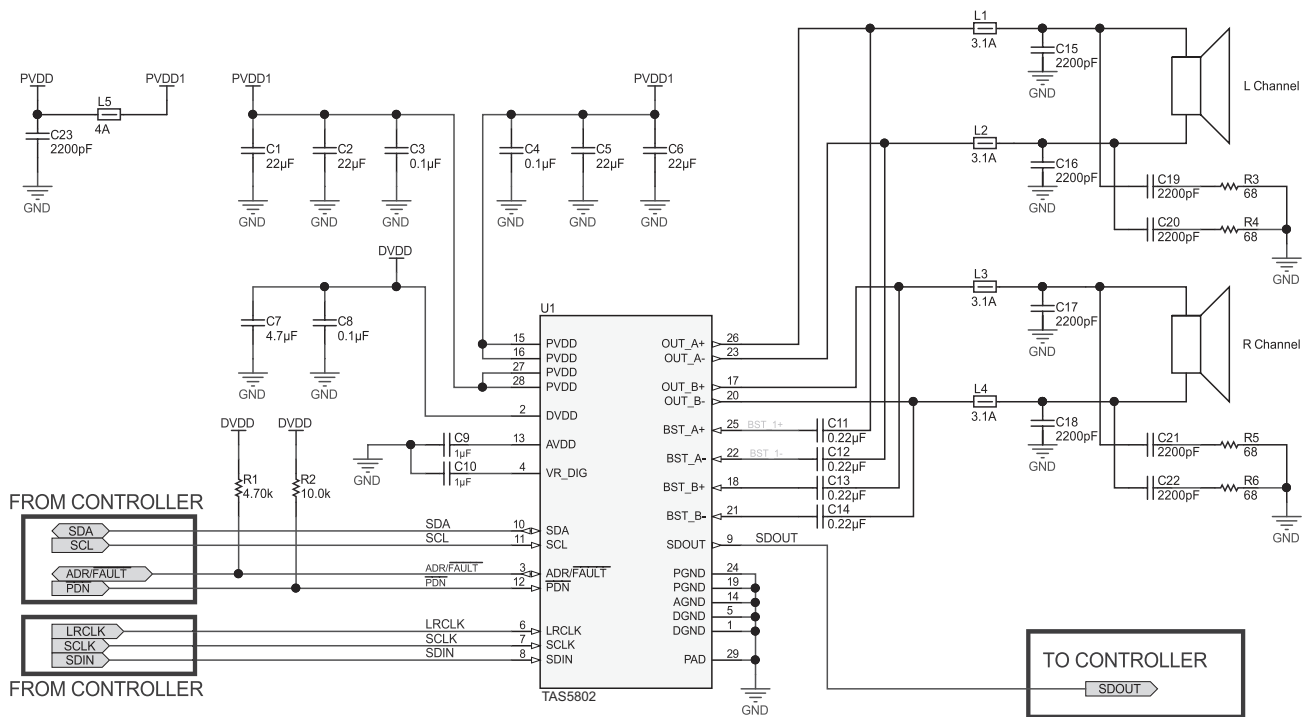


Figure 8-1. 2.0 (Stereo BTL) System Application Schematic with Ferrite Bead as the output filter

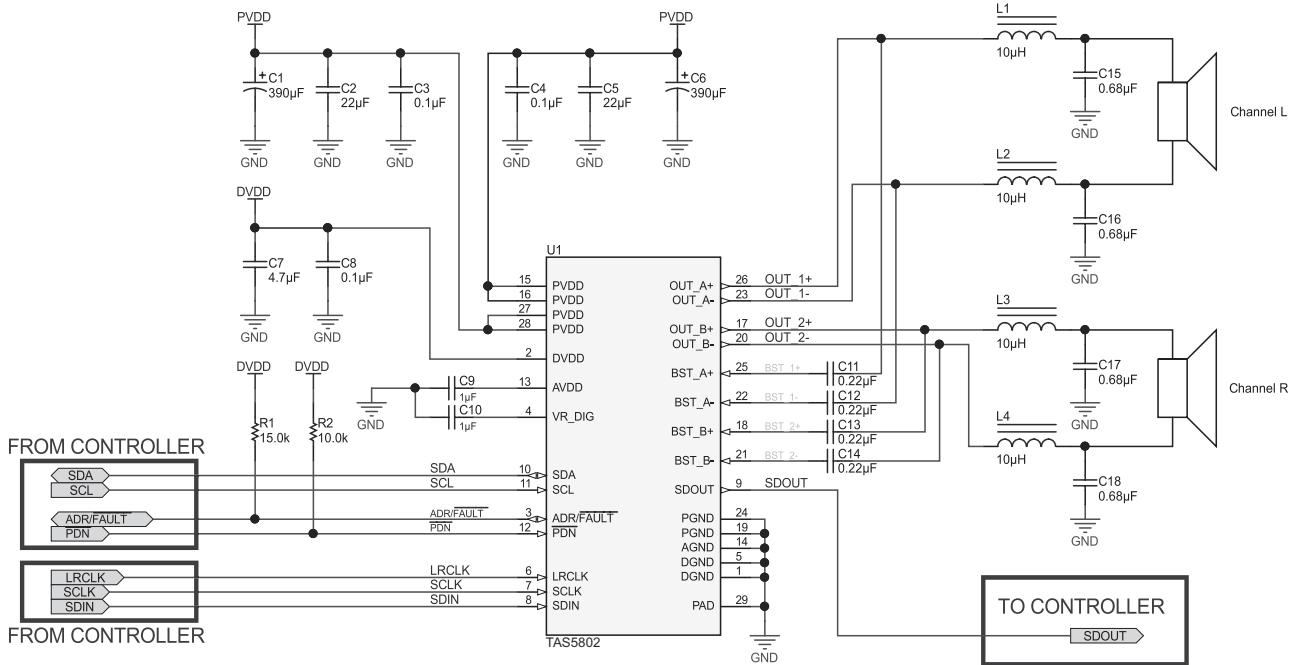


Figure 8-2. 2.0 (Stereo BTL) System Application Schematic with Inductor as the output filter

8.2.1.1 Design Requirements

- Power supplies:
 - 3.3V or 1.8V supply
 - 4.5V to 20V supply
- Communication: host processor serving as I²C compliant master
- External memory (Such as EEPROM and FLASH) used for coefficients

The requirement for the supporting components for the TAS5802 device in a Stereo 2.0 (BTL) system is provide in Table 8-3 and Table 8-4.

Table 8-3. Supporting Component Requirements for Stereo 2.0 (BTL) system (With Ferrite bead as output filter)

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C1,C2,C5,C6	22uF	0805	CAP, CERM, 22µF, 35V, +/- 20%, JB, 0805
C3,C4	0.1uF	0402	CAP, CERM, 0.1µF, 50V, +/- 10%, X7R, 0402
C7	4.7uF	0603	CAP, CERM, 4.7µF, 10V, +/- 10%, X5R, 0603
C8	0.1uF	0603	CAP, CERM, 0.1µF, 16V, +/- 10%, X7R, 0603
C9,C10	1uF	0603	CAP, CERM, 1µF, 16V, +/- 10%, X5R, 0603
R1	4.70kΩ	0402	RES, 4.70kΩ, 1%, 0.0625W, 0402
R2	10.0kΩ	0404	RES, 10.0kΩ, 1%, 0.063W, 0402
C11,C12,C13,C14	0.22uF	0603	CAP, CERM, 0.22µF, 50V, +/- 10%, X7R, 0603
C15,C16,C17,C18,C19,C20,C21,C22,C23	2200pF	0603	CAP, CERM, 2200pF, 100V,+/- 10%, X7R, 0603
R3,R4,R5,R6	68ohm	0603	ES, 68Ω, 5%, 0.1W, 0603
L1,L2,L3,L4	300ohm	0806	Ferrite Bead, 300Ω @ 100MHz, 3.1A, 0806
L5	100 ohm	0806	Ferrite Bead, 100 ohm @ 100 MHz, 4 A, 0806

With Low EMI technology, TAS5802 keeps enough EMI margin for most of application cases where PVDD < 14V with ferrite bead (Low BOM cost). With Ferrite Bead and capacitor as the output filter, [Figure 8-1](#) and [Figure 8-2](#) include a good configuration (proper value of ferrite bead, capacitor, resistor) to achieve enough EMI margin for the typical case which PVDD = 12V, Speaker Load = 8Ω/6Ω, each speaker wire with 1m length, Output Power = 1W/4W/8W for each channel.

- Select Ferrite bead (L1~L5). The trade-off is impedance and rated current. If the rated current meet the system's requirement, larger impedance means larger EMI margin for the EMI, especially for the frequency band 5 MHz~50 MHz. The typical ferrite bead recommend for TAS5802 is NFZ2MSM series (Murata) and UPZ2012E series (Sunlord). 300 ohm at 100 MHz ferrite bead is a typical value which can pass EMI for most of application cases.
- Select capacitor (C15~C23). The trade-off is capacitor value and idle current. Larger capacitor means larger idle current, increase the capacitor value from 1nF to 2.2nF makes much help for frequency band 5 MHz~100 MHz.
- Using Ferrite bead as the output filter, recommend designer to use Fsw = 384 kHz with Spread spectrum enable, BD Modulation, refer to [Section 6.4.3.1](#).
- With Ferrite bead as the output power. In order to pass EMI (AC Conducted Emission) standard, an AC to DC adapter with EMI filter in it is needed. For most of applications (TV/Voice Control Speaker/Wireless speaker/Soundbar) which need a 110V~220V power supply usually has a EMI filter in the AC to DC adapter. Some cases use DC power supply and also need to test the DC Conducted Emission , this applications (Automotive/Industry) need a simple EMI filter on PVDD for TAS5802. Refer to application note: AN-2162 Simple Success With Conducted EMI From DC to DC Converters.

Table 8-4. Supporting Component Requirements for Stereo 2.0 (BTL) system (With Inductor as output filter)

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
C1,C6	390μF	10mmx10mm	CAP, AL, 390μF, 35V, ±20%, 0.08 ohm, SMD
C2,C5	22μF	0603	CAP, CERM, 22μF, 35V, ±20%, JB, 0805
C3,C4	0.1μF	0402	CAP, CERM, 0.1μF, 50V, ±10%, X7R, 0402
C7	4.7μF	0603	CAP, CERM, 4.7μF, 10V, ±10%, X5R, 0603
C8	0.1μF	0603	CAP, CERM, 0.1μF, 16V, ±10%, X7R, 0603
C9,C10	1μF	0603	CAP, CERM, 1μF, 16V, ±10%, X5R, 0603
R1	15.0kΩ	0402	RES, 15.0kΩ, 1%, 0.0625 W, 0402
R2	10.0kΩ	0404	RES, 10.0kΩ, 1%, 0.063W, 0402
C11,C12,C13,C14	0.22μF	0603	CAP, CERM, 0.22μF, 50V, ±10%, X7R, 0603
C15,C16,C17,C18	0.68μF	0805	CAP, CERM, 0.68μF, 50V, ±10%, X7R, 0805
L1,L2,L3,L4	10μH		Inductor, Shielded, 10μH, 4.4A, 0.023Ω, SMD

With Inductor as the output filter, designers can achieve ultra low idle current (with Hybrid Modulation or 1SPW Modulation) and keep large EMI margin. As the switching frequency of TAS5802 can be adjustable from 384 kHz to 768 kHz. Higher switching frequency means smaller Inductor value needed.

- With 768kHz switching frequency. Designers can select 10uH + 0.68μF or 4.7μH +0.68μF as the output filter, this will help customer to save the Inductor size with the same rated current during the inductor selection. With 4.7uH + 0.68uF, make sure PVDD ≤ 12V to avoid the large ripple current to trigger the OC threshold (5A).
- With 384kHz switching frequency. Designers can select 22μH + 0.68μF or 15μH + 0.68μF or 10μH + 0.68μF as the output filter, this will help customer to save power dissipation for some battery power supply application. With 10μH + 0.68μF, make sure PVDD ≤ 12V to avoid the large ripple current to trigger the OC threshold (5A).

8.2.1.2 Detailed Design Procedures

The design procedure can be used for Stereo 2.0 or Mono 1.1 systems.

8.2.1.2.1 Step 1: Hardware Integration

- Use the Typical Application Schematic as a guide, integrate the hardware into the system schematic.
- Follow the recommended component placement, board layout, and routing given in the example layout above, integrate the device and its supporting components into the system PCB file.
 - The most critical sections of the circuit are the power supply inputs, the amplifier output signals, and the high-frequency signals, all of which go to the serial audio port. Constructing these signals to ensure they are given precedent as design trade-offs are made is recommended.
 - For questions and support, go to the E2E forums ([E2E.ti.com](https://e2e.ti.com)). If deviating from the recommended layout is necessary, go to the E2E forum to request a layout review.

8.2.1.2.2 Step 2: Speaker Tuning

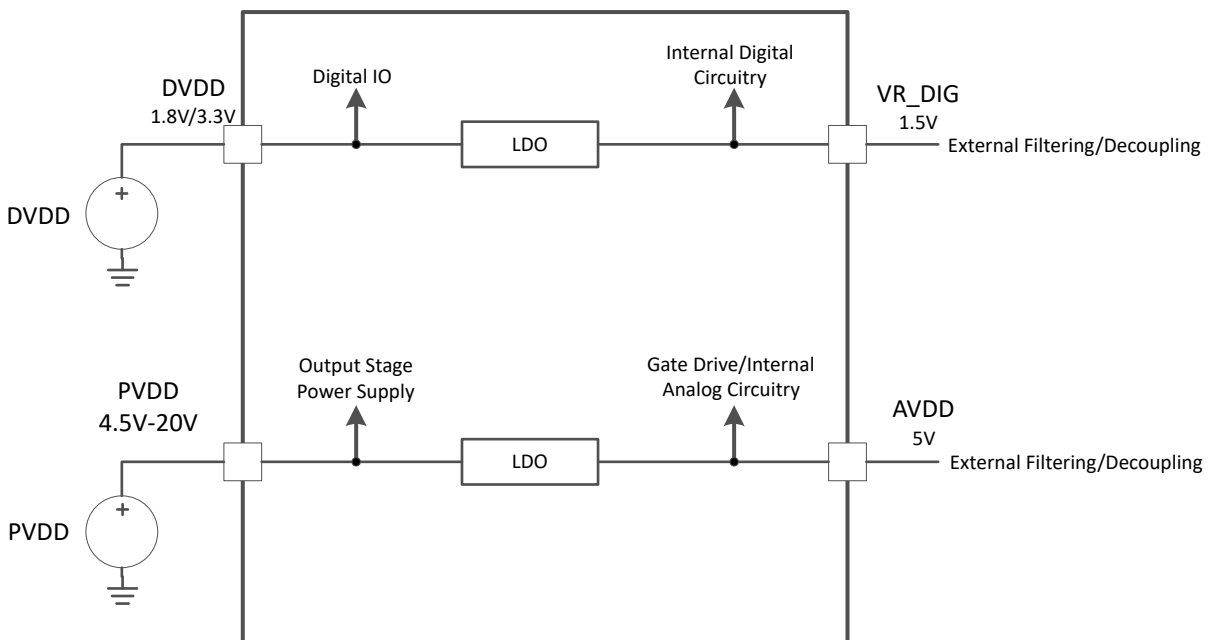
Use the [TAS5802EVM](#) evaluation module and the [PPC3](#) app to configure the desired device settings.

8.2.1.2.3 Step 3: Software Integration

- Use the End System Integration feature of the PPC3 app to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

8.3 Power Supply Recommendations

The TAS5802 device requires two power supplies for proper operation. A high-voltage supply calls PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. Additionally, one low-voltage power supply which is calls DVDD is required to power the various low-power portions of the device. The allowable voltage range for both PVDD and DVDD supply are listed in the *Recommended Operating Conditions* table. Once the device has been initialized, PVDD must keep within the normal operation voltage. Once PVDD lower than 3.5V, all registers need re-initialize again.



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Figure 8-3. Power Supply Function Block Diagram

8.3.1 DVDD Supply

The DVDD supply that is required from the system is used to power several portions of the device. As shown in [Figure 8-3](#), it provides power to the DVDD pin. Proper connection, routing and decoupling techniques are highlighted in [Section 8](#) and [Section 8.4.2](#) and must be followed as closely as possible for proper operation and performance.

Some portions of the device also require a separate power supply that is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5802 device includes an integrated low dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and its output is presented on the DVDD_REG pin, providing a connection point for an external bypass capacitor. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

8.3.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TAS5802EVM and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TAS5802 device [Section 8](#). Lack of proper decoupling, like that shown in the [Section 8](#), results in voltage spikes which can damage the device.

A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. A GVDD pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

Another separate power supply is derived from the PVDD supply via an integrated linear regulator is AVDD. AVDD pin is provided for the attachment of decoupling capacitor for the TAS5802 internal circuitry. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

8.4 Layout

8.4.1 Layout Guidelines

8.4.1.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to their layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout.

Ideally, the guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in [Section 8.4.2](#). These examples represent exemplary baseline balance of the engineering trade-offs involved with laying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, solution size can be compromised to improve thermal performance through the use of additional contiguous copper near the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, it is recommended to start from the guidance shown in [Section 8.4.2](#) and work with TI field application engineers or through the E2E community to modify it based upon the application specific goals.

8.4.1.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has long been understood in the industry. This applies to DVDD, AVDD, GVDD and PVDD. However, the capacitors on the PVDD net for the TAS5802 device deserve special attention.

The small bypass capacitors on the PVDD lines of the DUT must be placed as close to the PVDD pins as possible. Not only does placing these devices far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5802 device can cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the *Absolute Maximum Ratings* table, damaging the device. For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in [Section 8.4.2](#).

8.4.1.3 Optimizing Thermal Performance

Follow the layout example shown in [Section 8.4.2](#) to achieve the best balance of solution size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance can be required due to design constraints which cannot be avoided. In these instances, the system designer should ensure that the heat can get out of the device and into the ambient air surrounding the device. Fortunately, the heat created in the device naturally travels away from the device and into the lower temperature structures around the device.

8.4.1.3.1 Device, Copper, and Component Layout

Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips should be followed to achieve that goal:

- Avoid placing other heat producing components or structures near the amplifier (including above or below in the end equipment).
- If possible, use a higher layer count PCB to provide more heat sinking capability for the TAS5802 device and to prevent traces and copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TAS5802 device away from the edge of the PCB when possible to ensure that the heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS5802 device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.
- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient it so that the narrow end of the passive component is facing the TAS5802 device.
- Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

8.4.1.3.2 Stencil Pattern

The recommended drawings for the TAS5802 device PCB foot print and associated stencil pattern are shown at the end of this document in the package addendum. Additionally, baseline recommendations for the via arrangement under and around the device are given as a starting point for the PCB design. This guidance is provided to suit the majority of manufacturing capabilities in the industry and prioritizes manufacturability over all other performance criteria. In elevated ambient temperature or under high-power dissipation use-cases, this guidance may be too conservative and advanced PCB design techniques may be used to improve thermal performance of the system.

Note

The customer must verify that deviation from the guidance shown in the package addendum, including the deviation explained in this section, meets the customer's quality, reliability, and manufacturability goals.

8.4.1.3.2.1 PCB footprint and Via Arrangement

The PCB footprint (also known as a symbol or land pattern) communicates to the PCB fabrication vendor the shape and position of the copper patterns to which the TAS5802 device will be soldered. This footprint can be followed directly from the guidance in the package addendum at the end of this data sheet. It is important to make sure that the thermal pad, which connects electrically and thermally to the PowerPAD™ of the TAS5802 device, be made no smaller than what is specified in the package addendum. This ensures that the TAS5802 device has the largest interface possible to move heat from the device to the board.

The via pattern shown in the package addendum provides an improved interface to carry the heat from the device through to the layers of the PCB, because small diameter plated vias (with minimally-sized annular rings) present a low thermal-impedance path from the device into the PCB. Once into the PCB, the heat travels away from the device and into the surrounding structures and air. By increasing the number of vias, as shown in [Section 8.4.2](#), this interface can benefit from improved thermal performance.

Note

Vias can obstruct heat flow if they are not constructed properly.

More notes on the construction and placement of vias are as follows:

- Remove thermal reliefs on thermal vias, because they impede the flow of heat through the via.
- Vias filled with thermally conductive material are best, but a simple plated via can be used to avoid the additional cost of filled vias.
- The diameter of the drill must be 8 mm or less. Also, the distance between the via barrel and the surrounding planes should be minimized to help heat flow from the via into the surrounding copper material. In all cases, minimum spacing should be determined by the voltages present on the planes surrounding the via and minimized wherever possible.
- Vias should be arranged in columns, which extend in a line radially from the heat source to the surrounding area. This arrangement is shown in [Section 8.4.2](#).
- Ensure that vias do not cut off power current flow from the power supply through the planes on internal layers. If needed, remove some vias that are farthest from the TAS5802 device to open up the current path to and from the device.

8.4.1.3.2.2 Solder Stencil

During the PCB assembly process, a piece of metal called a stencil is placed on top of the PCB and deposits solder paste on the PCB wherever there is an opening (called an aperture) in the stencil. The stencil determines the quantity and the location of solder paste that is applied to the PCB in the electronic manufacturing process. In most cases, the aperture for each of the component pads is almost the same size as the pad itself. However, the thermal pad on the PCB is large and depositing a large, single deposition of solder paste would lead to manufacturing issues. Instead, the solder is applied to the board in multiple apertures, to allow the solder paste to outgas during the assembly process and reduce the risk of solder bridging under the device. This structure is called an aperture array, and is shown in [Section 8.4.2](#). It is important that the total area of the aperture array (the area of all of the small apertures combined) covers between 70% and 80% of the area of the thermal pad itself.

8.4.2 Layout Example

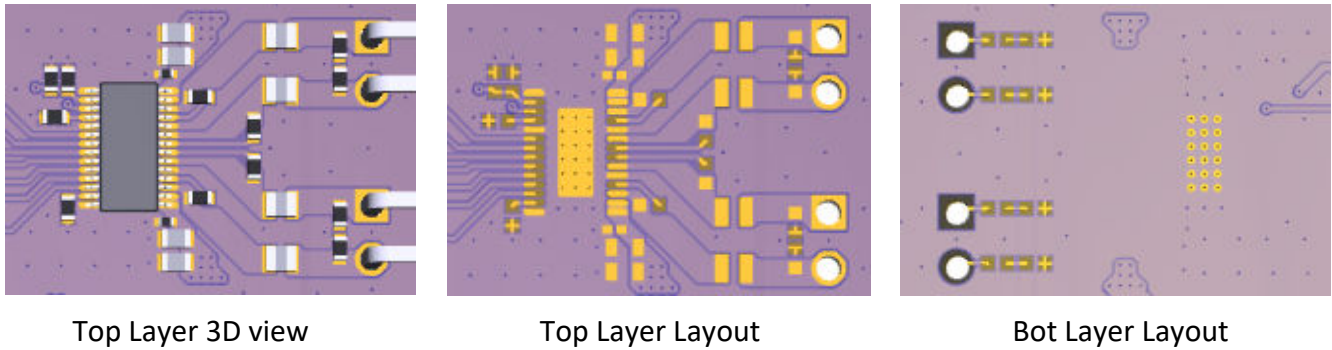


Figure 8-4. 2.0 (Stereo BTL with Ferrite Bead as Output Filter) Layout View

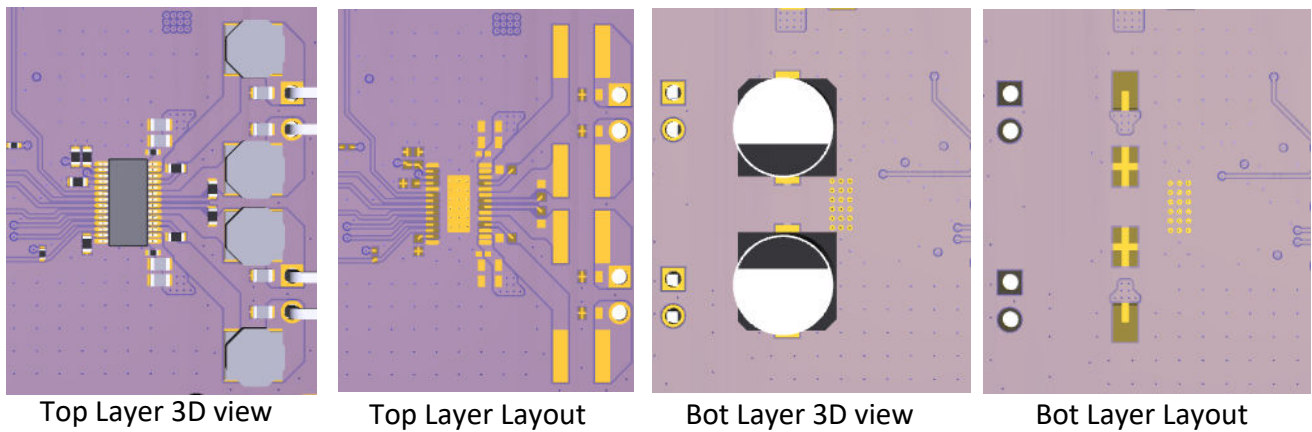


Figure 8-5. 2.0 (Stereo BTL with Inductor as Output Filter) Layout View

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

The glossary listed in the section is a general glossary with commonly used acronyms and words which are defined in accordance with a broad TI initiative to comply with industry standards such as JEDEC, IPC, IEEE, and others. The glossary provided in this section defines words, phrases, and acronyms that are unique to this product and documentation, collateral, or support tools and software used with this product. For any additional questions regarding definitions and terminology, please see the [e2e Audio Amplifier Forum](#).

Bridge tied load (BTL) is an output configuration in which one terminal of the speaker is connected to one half-bridge and the other terminal is connected to another half-bridge.

DUT refers to a *device under test* to differentiate one device from another.

Closed-loop architecture describes a topology in which the amplifier monitors the output terminals, comparing the output signal to the input signal and attempts to correct for non-linearities in the output.

Dynamic controls are those which are changed during normal use by either the system or the end-user.

GPIO is a general purpose input/output pin. It is a highly configurable, bi-directional digital pin which can perform many functions as required by the system.

Host processor (also known as System Processor, Scalar, Host, or System Controller) refers to device which serves as a central system controller, providing control information to devices connected to it as well as gathering audio source data from devices upstream from it and distributing it to other devices. This device often configures the controls of the audio processing devices (like the TAS5802) in the audio path in order to optimize the audio output of a loudspeaker based on frequency response, time alignment, target sound pressure level, safe operating area of the system, and user preference.

HybridFlow uses components which are built in RAM and components which are built in ROM to make a configurable device that is easier to use than a fully-programmable device while remaining flexible enough to be used in several applications

Maximum continuous output power refers to the maximum output power that the amplifier can continuously deliver without shutting down when operated in a 25°C ambient temperature. Testing is performed for the period of time required that their temperatures reach thermal equilibrium and are no longer increasing

$r_{DS(on)}$ is a measure of the on-resistance of the MOSFETs used in the output stage of the amplifier.

Static controls/Static configurations are controls which do not change while the system is in normal use.

Vias are copper-plated through-hole in a PCB.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2024) to Revision A (August 2025)	Page
• Updated the <i>Electrical Characteristics</i>	6
• Added the <i>PACKAGE OPTION ADDENDUM</i>	3

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

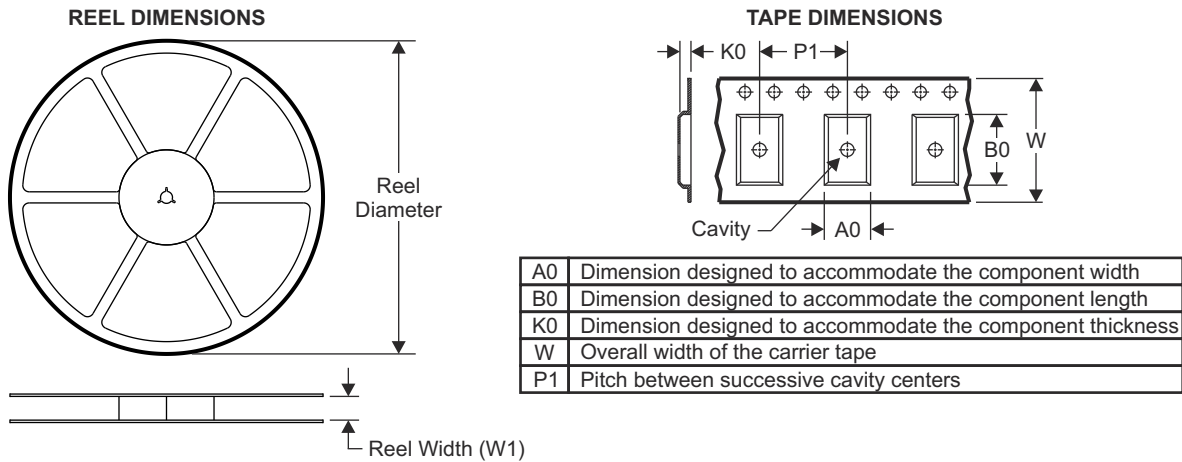
PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

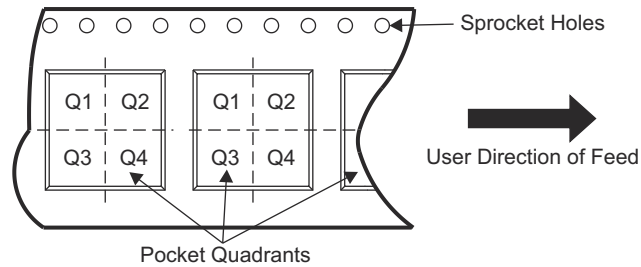
Orderable part number	Status ⁽¹⁾	Material type ⁽²⁾	Package Pins	Package qty Carrier	RoHS ⁽³⁾	Lead finish/Ball material ⁽⁴⁾	MSL rating/Peak reflow ⁽⁵⁾	Op temp (°C)	Part marking ⁽⁶⁾
TAS5802PWPR	ACTIVE	HTSSOP	PWP/28	2000/Tape&Reel	RoHS & Green	NiPdAu	Level-3-260C-168 HR	-40 to 85	5802
TAS5802PWPR.A	ACTIVE	HTSSOP	PWP/28	2000/Tape&Reel	RoHS & Green	NiPdAu	Level-3-260C-168 HR	-40 to 85	5802

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part. Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

11.1 Tape and Reel Information

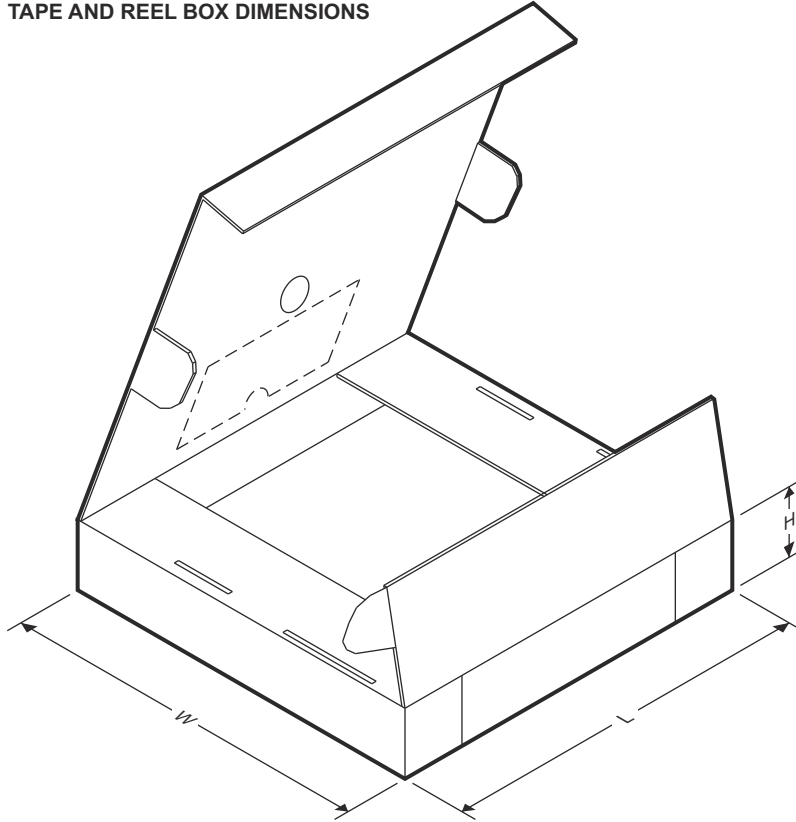


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5802PWPR	HTSSOP	PWP	28	2000	330	16.4	6.9	10.2	1.8	12	16	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5802PWPR	HTSSOP	PWP	28	2000	350	350	43

11.2 Mechanical Data

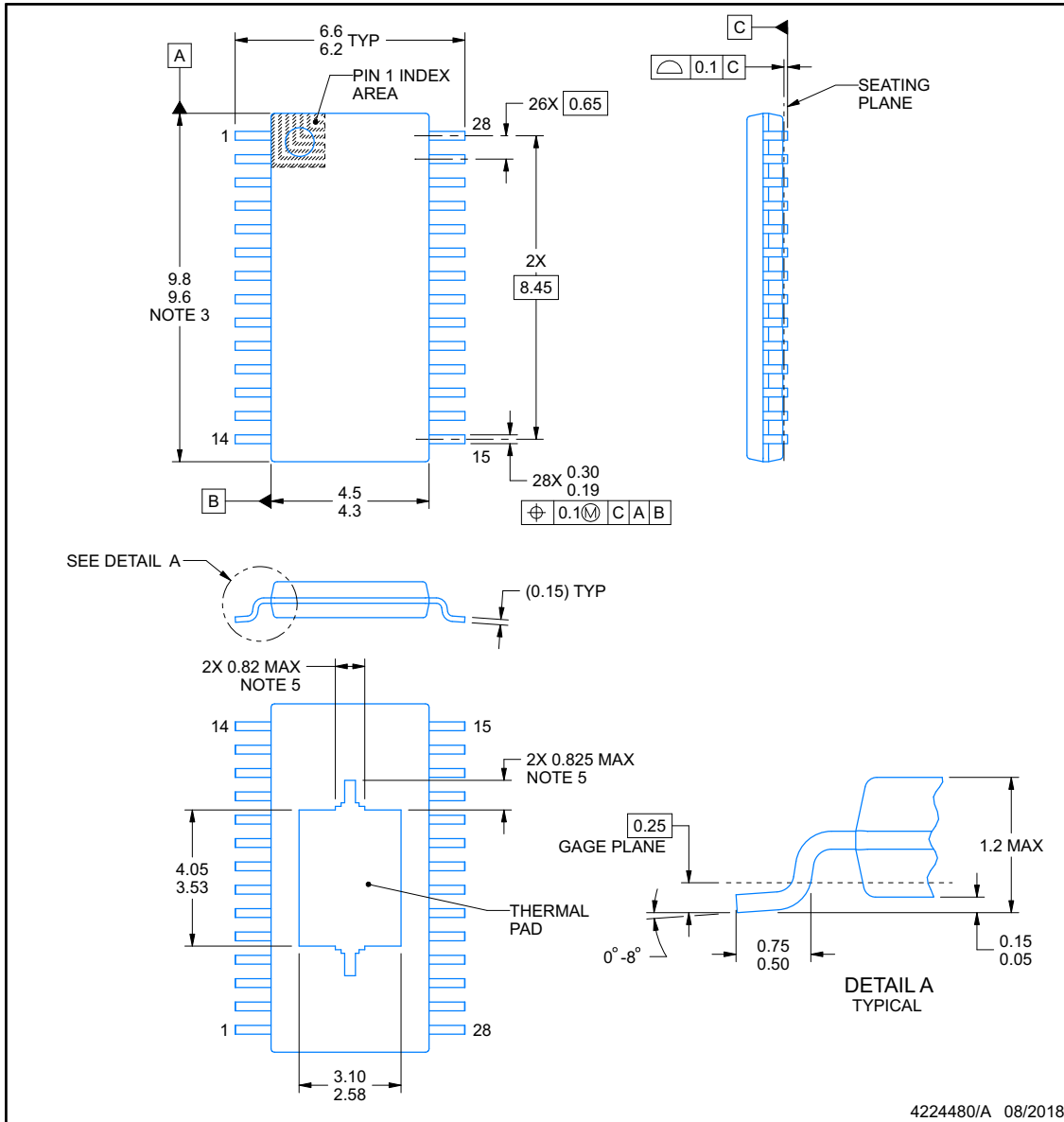


PACKAGE OUTLINE

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4224480/A 08/2018

NOTES:

PowerPAD is a trademark of Texas Instruments.

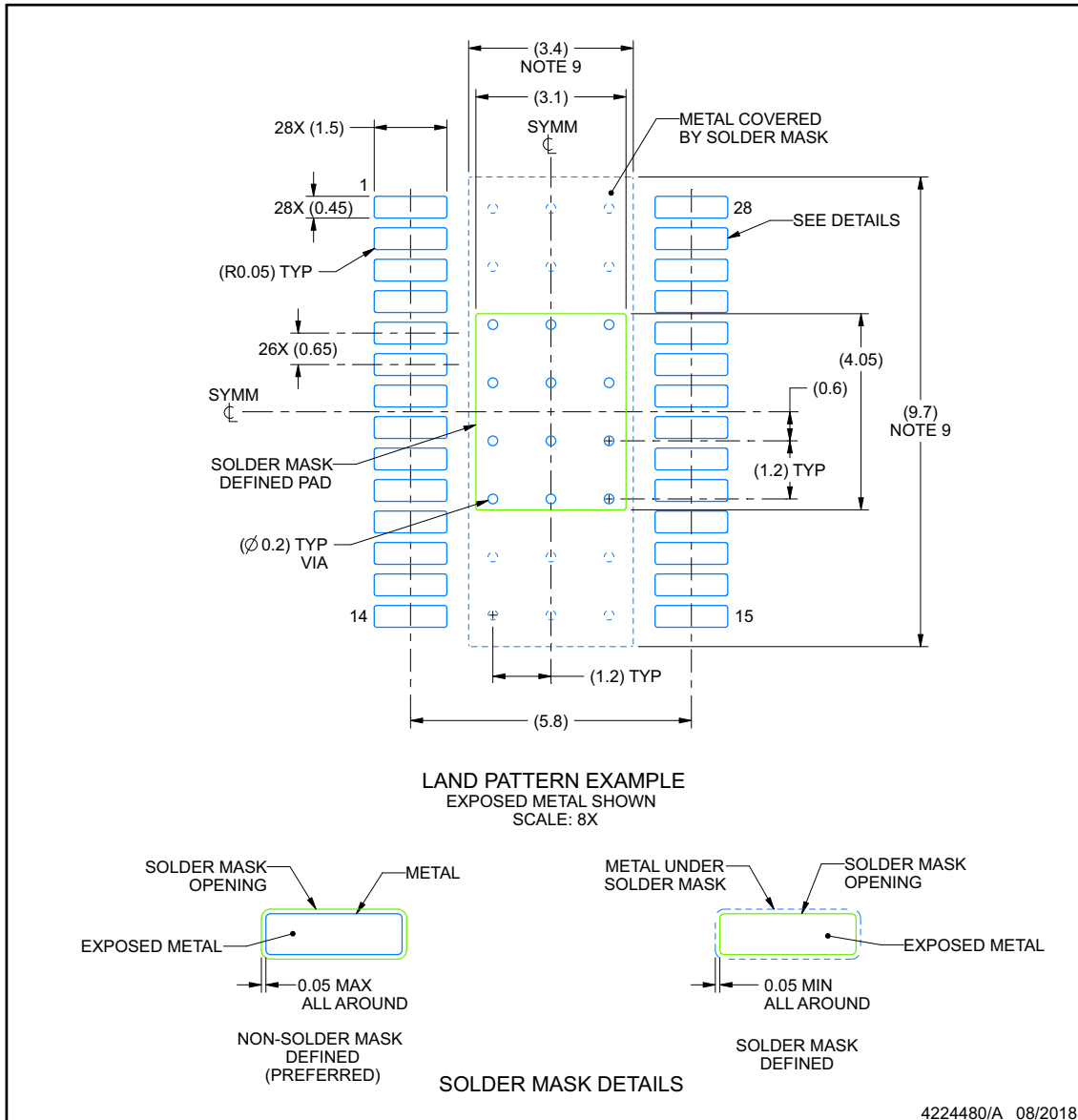
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

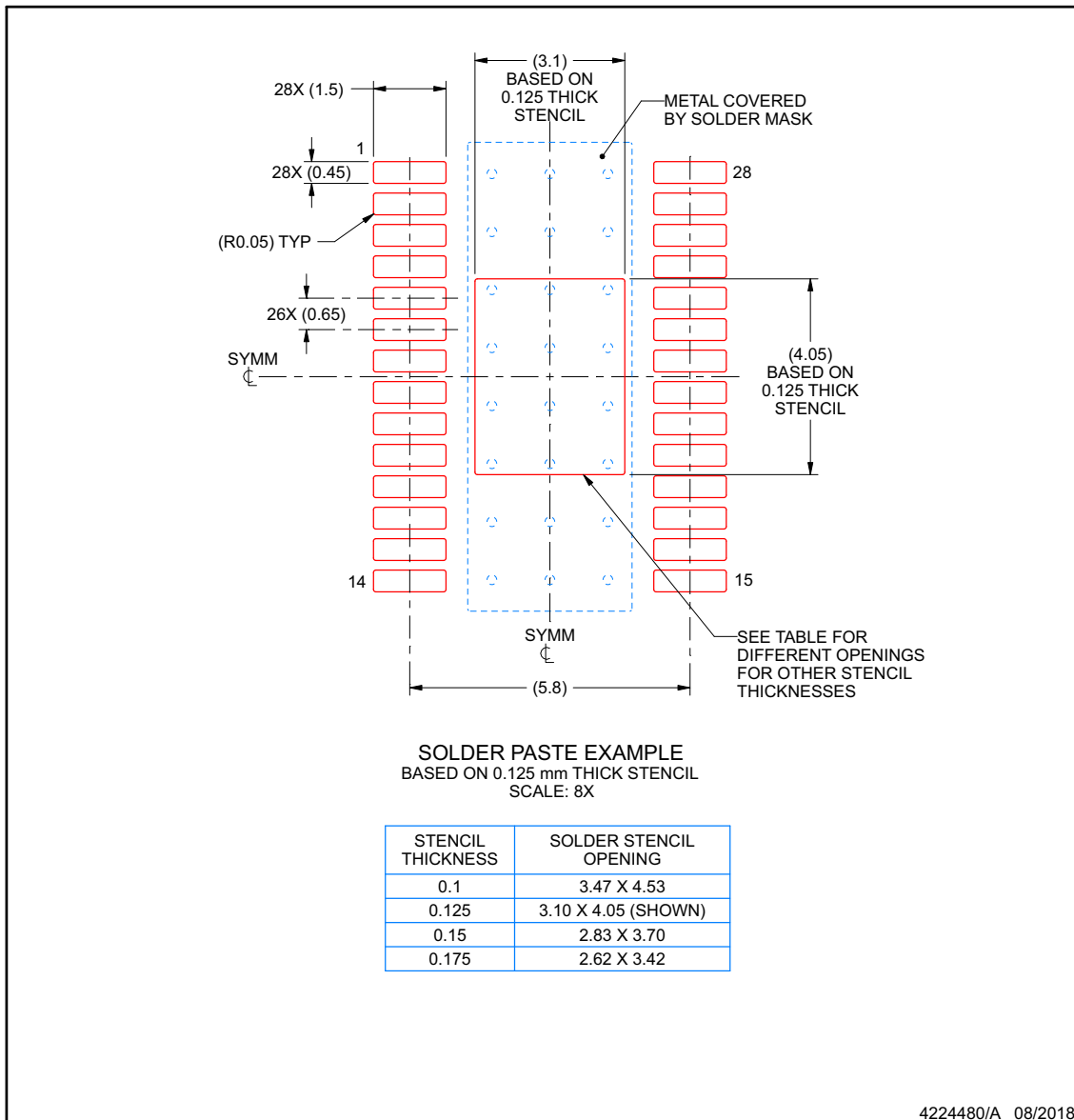
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS5802PWPR	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	5802

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

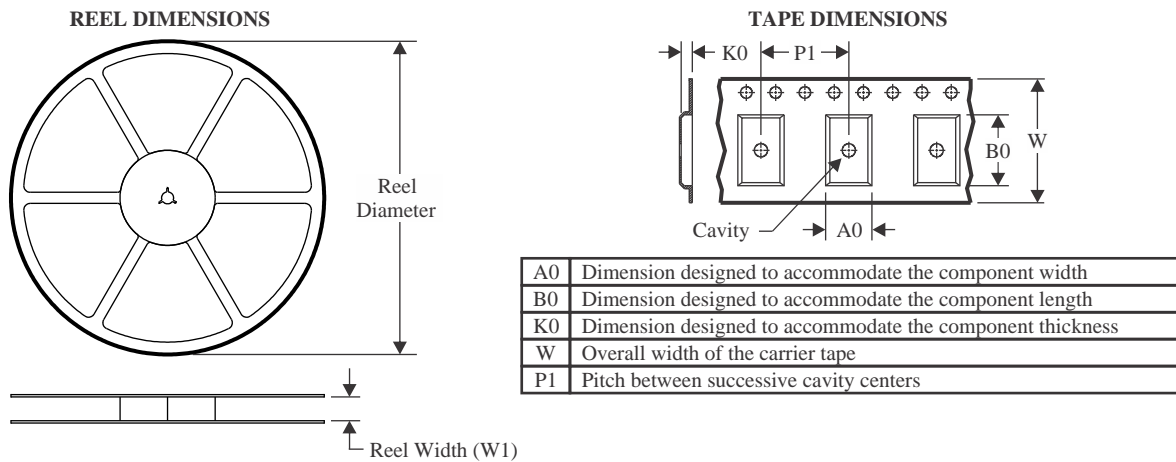
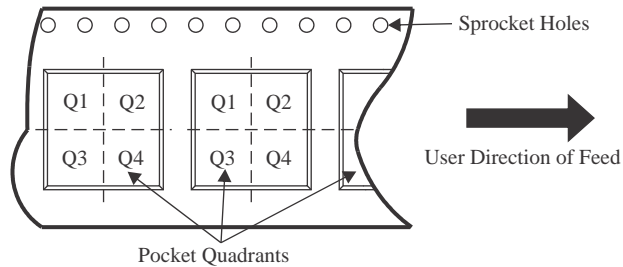
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

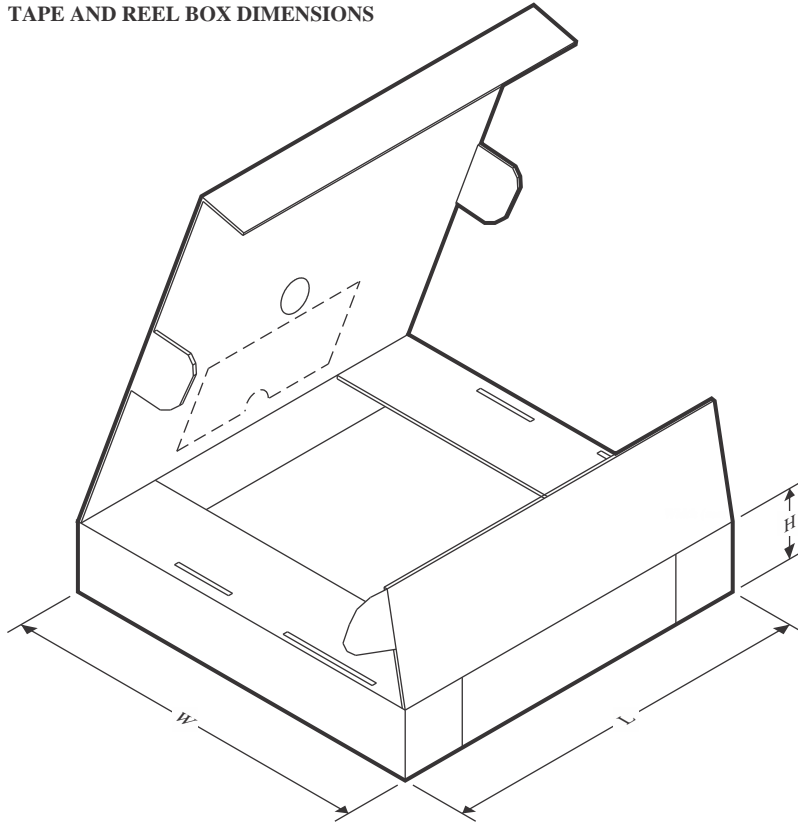
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5802PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TAS5802PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5802PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
TAS5802PWPR	HTSSOP	PWP	28	2000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

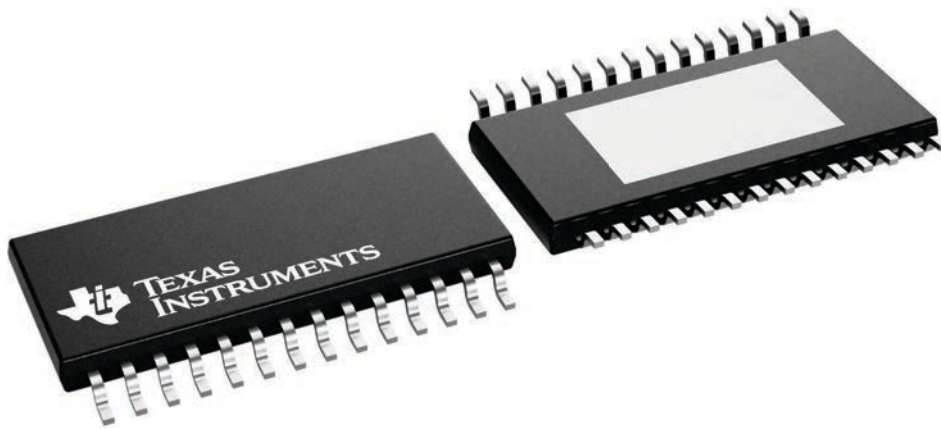
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

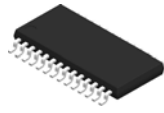
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

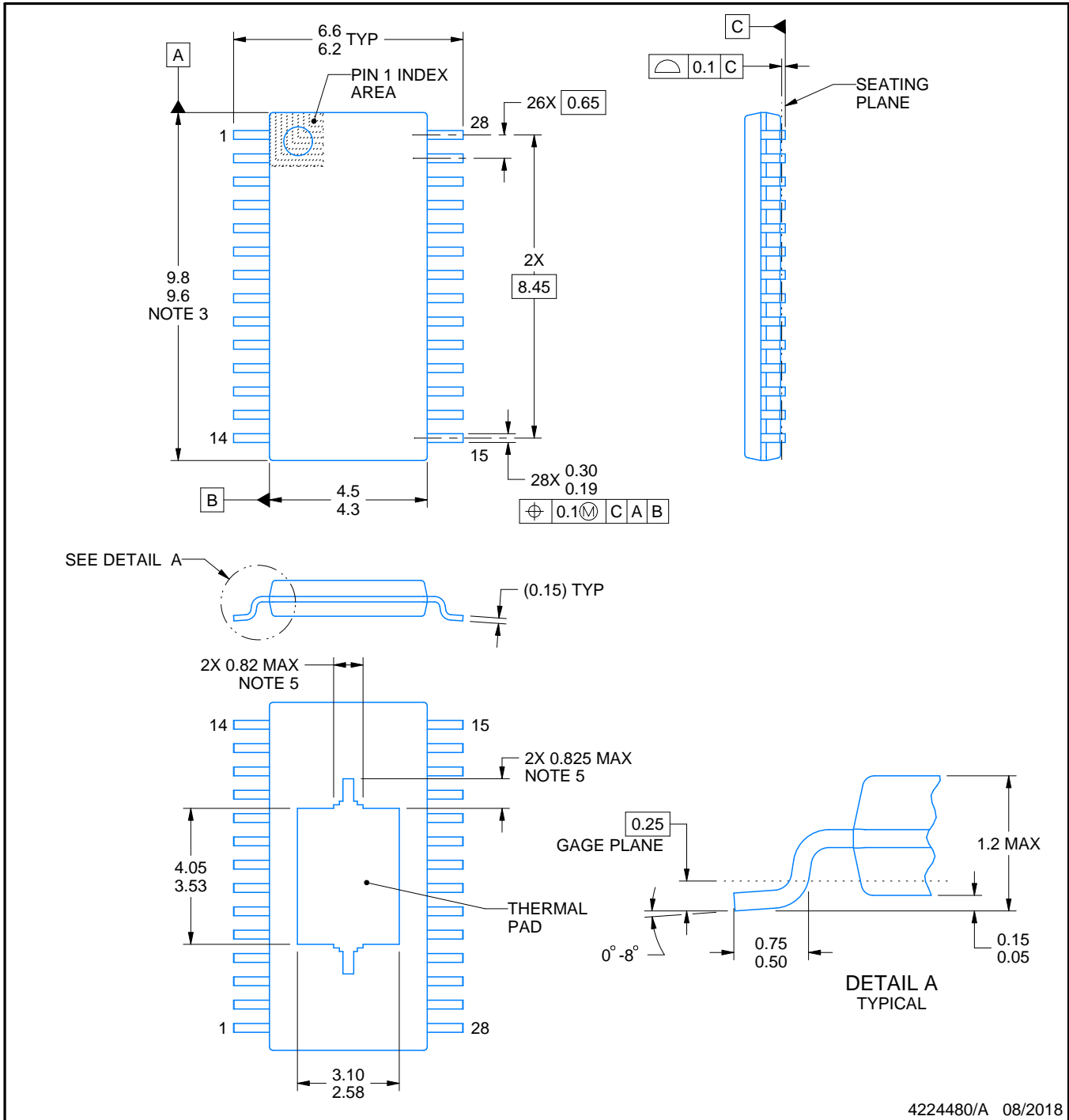
PWP0028M



PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

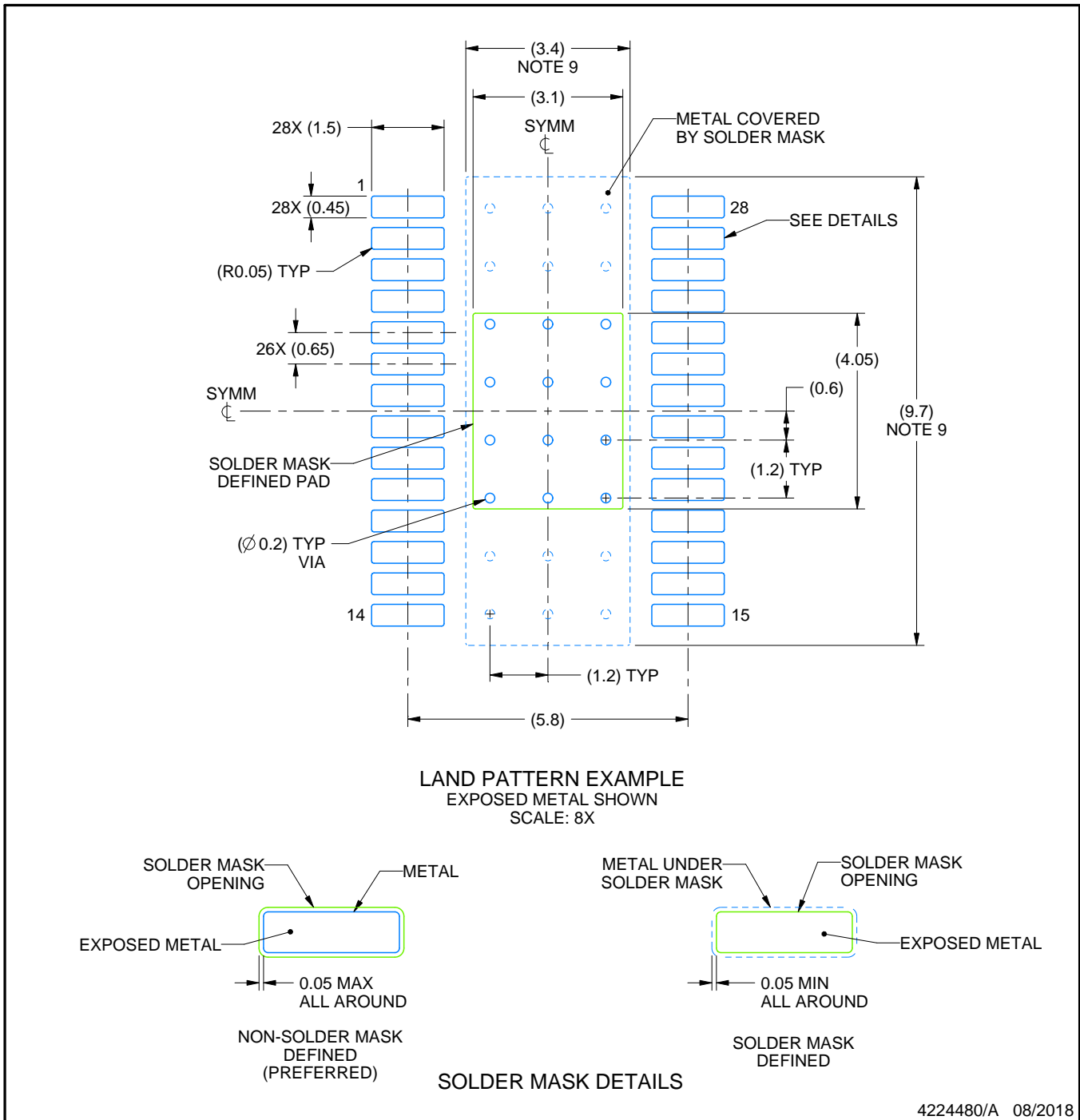
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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