

# TCA6408A Low-Voltage 8-Bit I<sup>2</sup>C and SMBus I/O Expander With Interrupt Output, Reset, and Configuration Registers

## 1 Features

- I<sup>2</sup>C to Parallel port expander
- Operating power-supply voltage range of 1.65 V to 5.5 V
- Allows bidirectional voltage-level translation and gpio expansion between 1.8-V, 2.5-V, 3.3-V, and 5-V I<sup>2</sup>C bus and P-ports
- Low standby current consumption of 1  $\mu$ A
- 5-V Tolerant I/O ports
- 400-kHz Fast I<sup>2</sup>C bus
- Hardware address pin allows two TCA6408A Devices on the same I<sup>2</sup>C/SMBus bus
- Active-low reset (  $\overline{\text{RESET}}$  ) input
- Open-drain active-low interrupt (  $\overline{\text{INT}}$  ) output
- Input and output configuration register
- Polarity inversion register
- Internal power-on reset
- Power up with all channels configured as inputs
- No glitch on power up
- Noise filter on SCL and SDA inputs
- Latched outputs with high-current drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA Per JESD 78, class II
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
- ESD Protection exceeds JESD 22
  - 2000-V Human body model (A114-A)
  - 1000-V Charged-device model (C101)

## 2 Applications

- Servers
- Routers (telecom switching equipment)
- [Personal computers](#)
- [Personal electronics](#) (gaming consoles)
- [Industrial automation](#)
- Products with GPIO-limited processors

## 3 Description

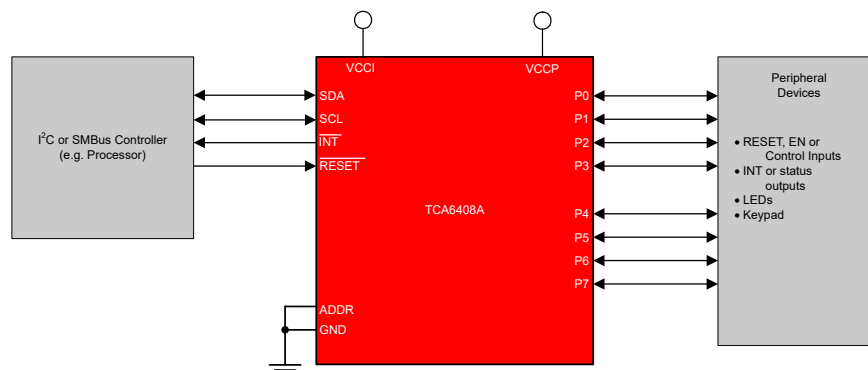
The TCA6408A is a 16-pin device that provides 8-bits of general purpose parallel input/output (I/O) expansion for the two-line bidirectional I<sup>2</sup>C bus (or SMBus) protocol. This device can operate with a power supply voltage ranging from 1.65 V to 5.5 V on both the I<sup>2</sup>C bus side ( $V_{\text{CCI}}$ ) and on the P-port side ( $V_{\text{CCP}}$ ). This allows the TCA6408A to interface with next-generation microprocessors and microcontrollers on the SDA/SCL side, where supply levels are dropping down to conserve power. In contrast to the dropping power supplies of microprocessors and microcontrollers, some PCB components such as LEDs remain at a 5-V power supply.

The device supports both 100-kHz (Standard-mode) and 400-kHz (Fast-mode) clock frequencies. I/O expanders such as the TCA6408A provide a simple solution when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, and so forth.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
TCA6408A	TSSOP (16)	5.00 mm × 4.40 mm
	VQFN (16)	3.00 mm × 3.00 mm
	UQFN (16)	2.60 mm × 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



**Simplified Schematic**



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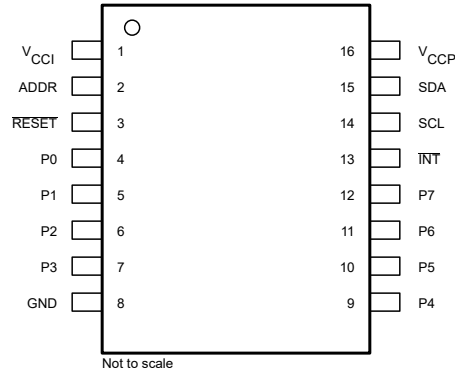
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

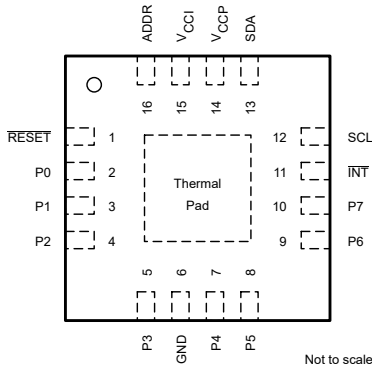
Changes from Revision D (July 2015) to Revision E (January 2023)	Page
• Changed all instances of legacy terminology to controller and target where I <sup>2</sup> C is mentioned.....	1
• Added paragraph: "Ramping up the device V <sub>CCP</sub> " to <i>Power-On Reset Requirements</i> .....	31

Changes from Revision C (July 2009) to Revision D (July 2015)	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• V <sub>IH</sub> - Split SCL, SDA and RESE $\bar{T}$ to different rows in the <i>Recommended Operating Conditions</i> table. Max value of SCL, SDA changed From: 5.5 V To: V <sub>CC1</sub> .....	5

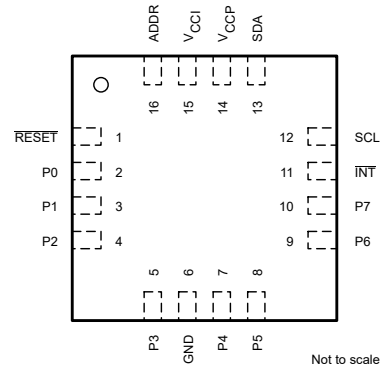
## 5 Pin Configuration and Functions



**Figure 5-1. PW Package, 16-Pin TSSOP (Top View)**



**Figure 5-2. RGT Package, 16-Pin VQFN (Top View)**



**Figure 5-3. RSV Package, 16-Pin UQFN (Top View)**

**Table 5-1. Pin Functions**

PIN			DESCRIPTION
NAME	TSSOP	UQFN, VQFN	
ADDR	2	16	Address input. Connect directly to $V_{CCP}$ or ground.
GND	8	6	Ground
$\overline{\text{INT}}$	13	11	Interrupt output. Connect to $V_{CCI}$ through a pull-up resistor.
P0	4	2	P-port input/output (push-pull design structure). At power on, P0 is configured as an input.
P1	5	3	P-port input/output (push-pull design structure). At power on, P1 is configured as an input.
P2	6	4	P-port input/output (push-pull design structure). At power on, P2 is configured as an input.
P3	7	5	P-port input/output (push-pull design structure). At power on, P3 is configured as an input.
P4	9	7	P-port input/output (push-pull design structure). At power on, P4 is configured as an input.

**Table 5-1. Pin Functions (continued)**

PIN			DESCRIPTION
NAME	TSSOP	UQFN, VQFN	
P5	10	8	P-port input/output (push-pull design structure). At power on, P5 is configured as an input.
P6	11	9	P-port input/output (push-pull design structure). At power on, P6 is configured as an input.
P7	12	10	P-port input/output (push-pull design structure). At power on, P7 is configured as an input.
$\overline{\text{RESET}}$	3	1	Active-low reset input. Connect to $V_{\text{CCI}}$ through a pull-up resistor, if no active connection is used.
SCL	14	12	Serial clock bus. Connect to $V_{\text{CCI}}$ through a pull-up resistor.
SDA	15	13	Serial data bus. Connect to $V_{\text{CCI}}$ through a pull-up resistor.
$V_{\text{CCI}}$	1	15	Supply voltage of I <sup>2</sup> C bus. Connect directly to the $V_{\text{CC}}$ of the external I <sup>2</sup> C controller. Provides voltage level translation.
$V_{\text{CCP}}$	16	14	Supply voltage of TCA6408A for P-ports

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (see <sup>(1)</sup>)

				MIN	MAX	UNIT	
V <sub>CCI</sub>	Supply voltage for I <sup>2</sup> C pins			-0.5	6.5	V	
V <sub>CCP</sub>	Supply voltage for P-ports			-0.5	6.5	V	
V <sub>I</sub>	Input voltage <sup>(2)</sup>			-0.5	6.5	V	
V <sub>O</sub>	Output voltage <sup>(2)</sup>			-0.5	6.5	V	
I <sub>IK</sub>	Input clamp current	ADDR, RESET, SCL	V <sub>I</sub> < 0		±20	mA	
I <sub>OK</sub>	Output clamp current	INT	V <sub>O</sub> < 0		±20	mA	
I <sub>IOK</sub>	Input/output clamp current	P-port	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CCP</sub>		±20	mA	
		SDA	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CCI</sub>		±20		
I <sub>OL</sub>	Continuous output low current	P-port	V <sub>O</sub> = 0 to V <sub>CCP</sub>		50	mA	
	Continuous output low current	SDA, INT	V <sub>O</sub> = 0 to V <sub>CCI</sub>		25		
I <sub>OH</sub>	Continuous output high current	P-port	V <sub>O</sub> = 0 to V <sub>CCP</sub>		50	mA	
I <sub>CC</sub>	Continuous current through GND				200	mA	
	Continuous current through V <sub>CCP</sub>				160		
	Continuous current through V <sub>CCI</sub>				10		
T <sub>stg</sub>	Storage temperature				-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Section 6.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

				MIN	MAX	UNIT	
V <sub>CCI</sub>	Supply voltage for I <sup>2</sup> C pins			1.65	5.5	V	
V <sub>CCP</sub>	Supply voltage for P-ports			1.65	5.5		
V <sub>IH</sub>	High-level input voltage	SCL, SDA	0.7 × V <sub>CCI</sub>	V <sub>CCI</sub>	V		
		RESET	0.7 × V <sub>CCI</sub>	5.5			
		ADDR, P7-P0	0.7 × V <sub>CCP</sub>	5.5			
V <sub>IL</sub>	Low-level input voltage	SCL, SDA, RESET	-0.5	0.3 × V <sub>CCI</sub>	V		
		ADDR, P7-P0	-0.5	0.3 × V <sub>CCP</sub>			
I <sub>OH</sub>	High-level output current	P7-P0			10	mA	
I <sub>OL</sub>	Low-level output current	P7-P0			25	mA	
T <sub>A</sub>	Operating free-air temperature				-40	85	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TCA6408A			UNIT
		PW (TSSOP)	RGT (VQFN)	RSV (UQFN)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122	65.5	127.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	92.1	62.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.1	40.0	48.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	10.8	6.9	2.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	66.5	21.3	48.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range,  $V_{CCI} = 1.65\text{ V to }5.5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$V_{CCP}$	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$	Input diode clamp voltage	$I_I = -18\text{ mA}$	1.65 V to 5.5 V	-1.2			V
$V_{POR}$	Power-on reset voltage <sup>(2)</sup>	$V_I = V_{CCP}$ or GND, $I_O = 0$	1.65 V to 5.5 V		1	1.4	V
$V_{OH}$	P-port high-level output voltage	$I_{OH} = -8\text{ mA}$	1.65 V	1.2			V
			2.3 V	1.8			
			3 V	2.6			
			4.5 V	4.1			
		$I_{OH} = -10\text{ mA}$	1.65 V	1.1			
			2.3 V	1.7			
			3 V	2.5			
			4.5 V	4.0			
$V_{OL}$	P-port low-level output voltage	$I_{OL} = 8\text{ mA}$	1.65 V			0.45	V
			2.3 V			0.25	
			3 V			0.25	
			4.5 V			0.2	
		$I_{OL} = 10\text{ mA}$	1.65 V			0.6	
			2.3 V			0.3	
			3 V			0.25	
			4.5 V			0.2	
$I_{OL}$	SDA	$V_{OL} = 0.4\text{ V}$	1.65 V to 5.5 V	3			mA
	$\overline{INT}$			3	15		
$I_I$	SCL, SDA, $\overline{RESET}$	$V_I = V_{CCI}$ or GND	1.65 V to 5.5 V			$\pm 0.1$	$\mu\text{A}$
	ADDR	$V_I = V_{CCP}$ or GND				$\pm 0.1$	
$I_{IH}$	P-port	$V_I = V_{CCP}$	1.65 V to 5.5 V			1	$\mu\text{A}$
$I_{IL}$	P-port	$V_I = \text{GND}$				1	$\mu\text{A}$
$I_{CC}$ ( $I_{CCI} + I_{CCP}$ )	Operating mode	SDA, P-port, ADDR, $\overline{RESET}$	$V_I$ on SDA and $\overline{RESET} = V_{CCI}$ or GND, $V_I$ on P-port and ADDR = $V_{CCP}$ or GND, $I_O = 0$ , I/O = inputs, $f_{SCL} = 400\text{ kHz}$	3.6 V to 5.5 V	10	20	$\mu\text{A}$
			2.3 V to 3.6 V	6.5	15		
			1.65 V to 2.3 V	4	9		
	Standby mode	SCL, SDA, P-port, ADDR, $\overline{RESET}$	$V_I$ on SCL, SDA and $\overline{RESET} = V_{CCI}$ or GND, $V_I$ on P-Port and ADDR = $V_{CCP}$ or GND, $I_O = 0$ , I/O = inputs, $f_{SCL} = 0$	3.6 V to 5.5 V	1.5	7	
			2.3 V to 3.6 V	1	3.2		
			1.65 V to 2.3 V	0.5	1.7		
$\Delta I_{CCI}$	Additional current in standby mode	SCL, SDA, $\overline{RESET}$	One input at $V_{CCI} - 0.6\text{ V}$ , Other inputs at $V_{CCI}$ or GND	1.65 V to 5.5 V		25	$\mu\text{A}$
$\Delta I_{CCP}$	Additional current in standby mode	P-port, ADDR	One input at $V_{CCP} - 0.6\text{ V}$ , Other inputs at $V_{CCP}$ or GND	1.65 V to 5.5 V		80	$\mu\text{A}$
$C_i$	SCL		$V_I = V_{CCI}$ or GND	1.65 V to 5.5 V	6	7	pF
$C_{io}$	SDA		$V_{IO} = V_{CCI}$ or GND	1.65 V to 5.5 V	7	8	pF
	P-port		$V_{IO} = V_{CCP}$ or GND		7.5	8.5	

- (1) All typical values are at nominal supply voltage (1.8-V, 2.5-V, 3.3-V, or 5-V  $V_{CC}$ ) and  $T_A = 25^\circ\text{C}$ .
- (2) When power (from 0 V) is applied to  $V_{CCP}$ , an internal power-on reset holds the TCA6408A in a reset condition until  $V_{CCP}$  has reached  $V_{POR}$ . At that time, the reset condition is released, and the TCA6408A registers and I<sup>2</sup>C/SMBus state machine initialize to their default states. After that,  $V_{CCP}$  must be lowered to below 0.2 V and back up to the operating voltage for a power-reset cycle.

## 6.6 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

		STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNIT
		MIN	MAX	MIN	MAX	
f <sub>scl</sub>	I <sup>2</sup> C clock frequency	0	100	0	400	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time	4		0.6		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time	4.7		1.3		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time	0	50	0	50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial data setup time	250		100		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial data hold time	0		0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time		1000	20 + 0.1C <sub>b</sub>	300	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time		300	20 + 0.1C <sub>b</sub>	300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time, 10-pF to 400-pF bus		300	20 + 0.1C <sub>b</sub>	300	μs
t <sub>buf</sub>	I <sup>2</sup> C bus free time between Stop and Start	4.7		1.3		μs
t <sub>sts</sub>	I <sup>2</sup> C Start or repeater Start condition setup time	4.7		0.6		μs
t <sub>sth</sub>	I <sup>2</sup> C Start or repeater Start condition hold time	4		0.6		μs
t <sub>sps</sub>	I <sup>2</sup> C Stop condition setup time	4		0.6		μs
t <sub>vd(data)</sub>	Valid data time, SCL low to SDA output valid		1		1	μs
t <sub>vd(ack)</sub>	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		1		1	μs

## 6.7 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-4](#))

		STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNIT
		MIN	MAX	MIN	MAX	
t <sub>w</sub>	Reset pulse duration	4		4		ns
t <sub>REC</sub>	Reset recovery time	0		0		ns
t <sub>RESET</sub>	Time to reset	600		600		ns



## 6.8 Switching Characteristics

over recommended operating free-air temperature range,  $C_L \leq 100$  pF (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNIT
			MIN	MAX	MIN	MAX	
$t_{iv}$	Interrupt valid time	P-Port		4		4	$\mu$ s
$t_{ir}$	Interrupt reset delay time	SCL		4		4	$\mu$ s
$t_{pv}$	Output data valid	SCL		400		400	ns
$t_{ps}$	Input data setup time	P-Port	0		0		ns
$t_{ph}$	Input data hold time	P-Port	300		300		ns

## 6.9 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

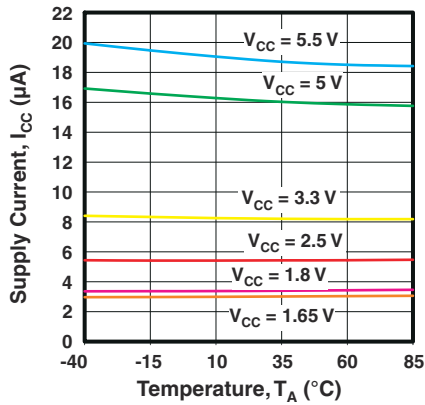


Figure 6-1. Supply Current vs Temperature

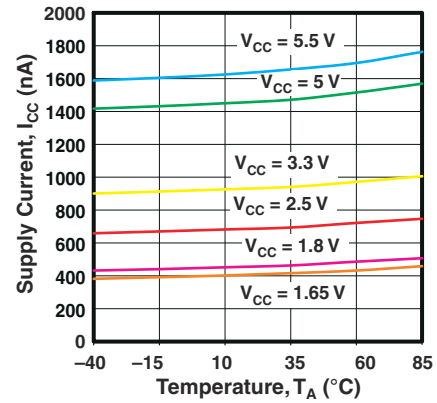


Figure 6-2. Standby Supply Current vs Temperature

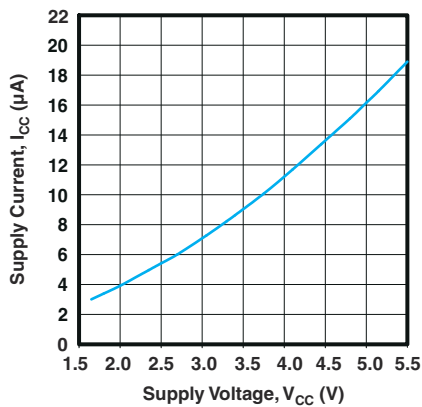


Figure 6-3. Supply Current vs Supply Voltage

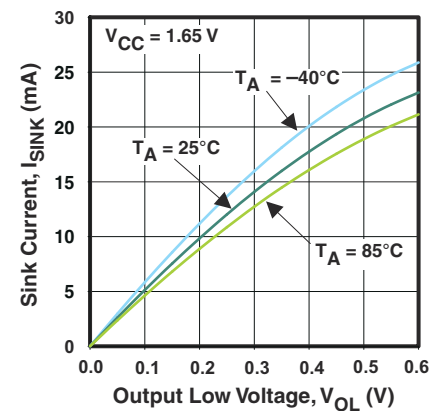


Figure 6-4. I/O Sink Current vs Output Low Voltage

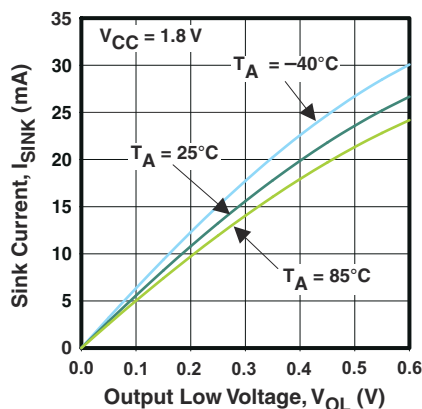


Figure 6-5. I/O Sink Current vs Output Low Voltage

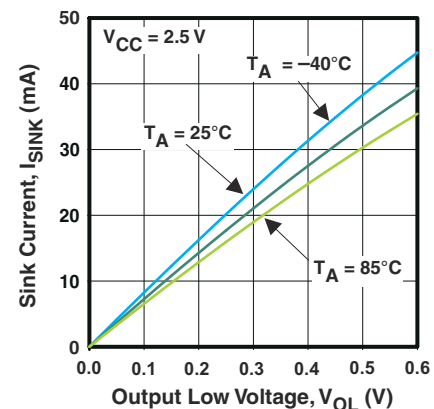


Figure 6-6. I/O Sink Current vs Output Low Voltage

## 6.9 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

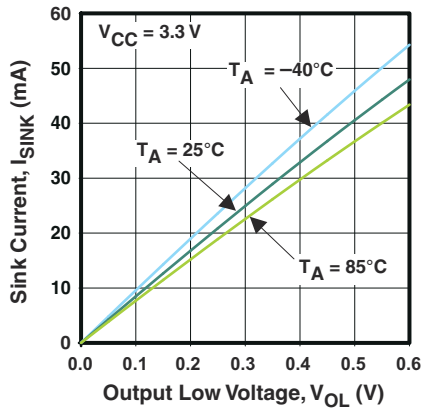


Figure 6-7. I/O Sink Current vs Output Low Voltage

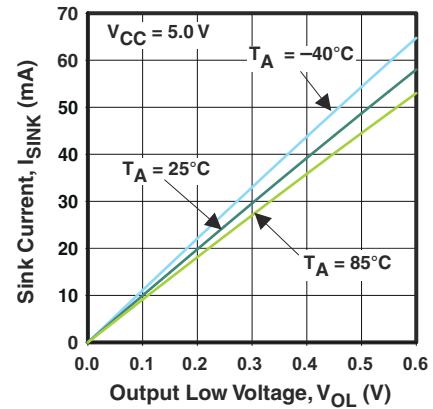


Figure 6-8. I/O Sink Current vs Output Low Voltage

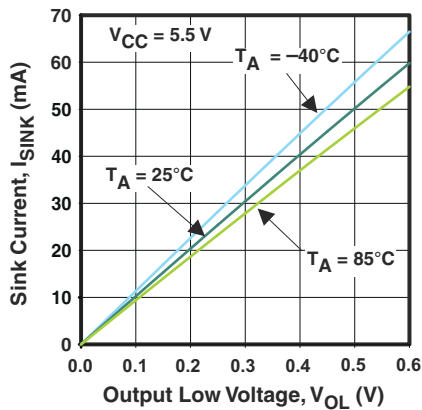


Figure 6-9. I/O Sink Current vs Output Low Voltage

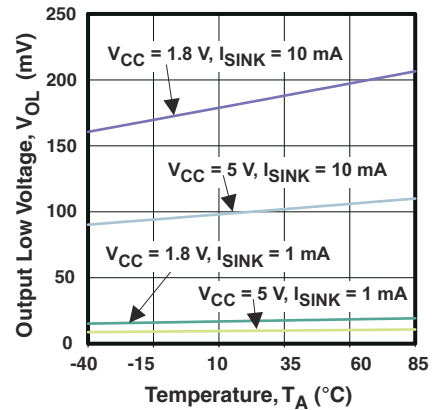


Figure 6-10. I/O Low Voltage vs Temperature

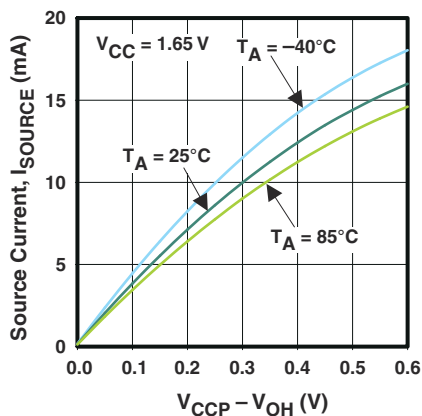


Figure 6-11. I/O Source Current vs Output High Voltage

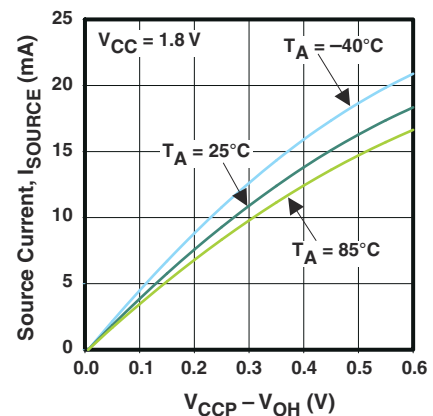


Figure 6-12. I/O Source Current vs Output High Voltage

### 6.9 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

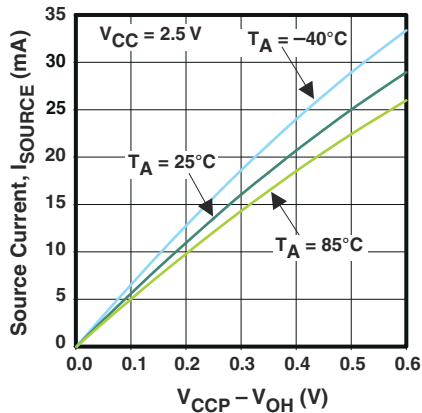


Figure 6-13. I/O Source Current vs Output High Voltage

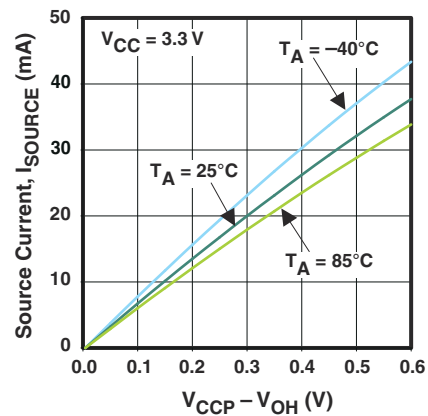


Figure 6-14. I/O Source Current vs Output High Voltage

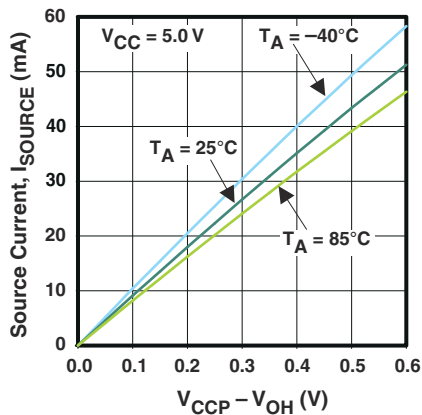


Figure 6-15. I/O Source Current vs Output High Voltage

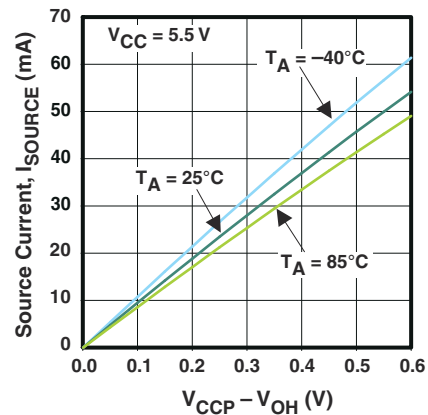


Figure 6-16. I/O Source Current vs Output High Voltage

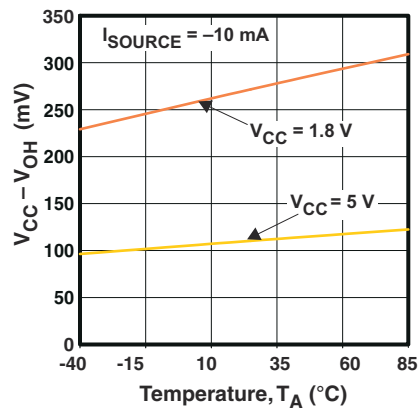
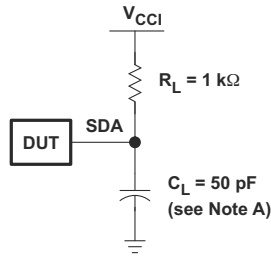
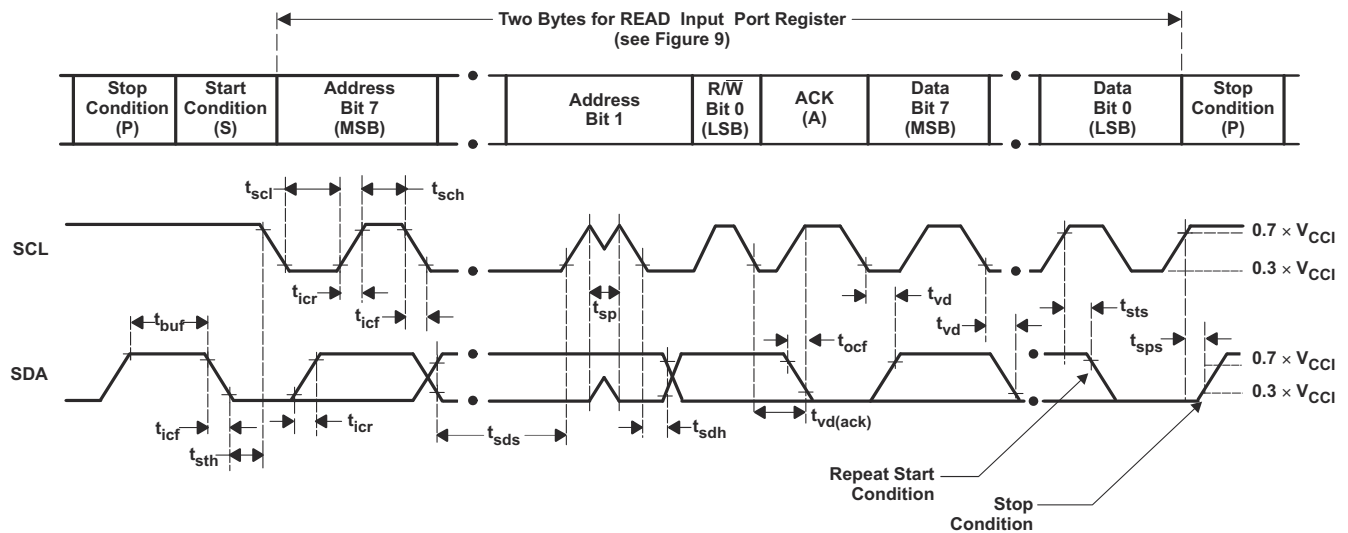


Figure 6-17. I/O High Voltage vs Temperature

## 7 Parameter Measurement Information



SDA LOAD CONFIGURATION

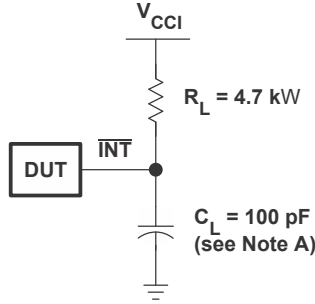


VOLTAGE WAVEFORMS

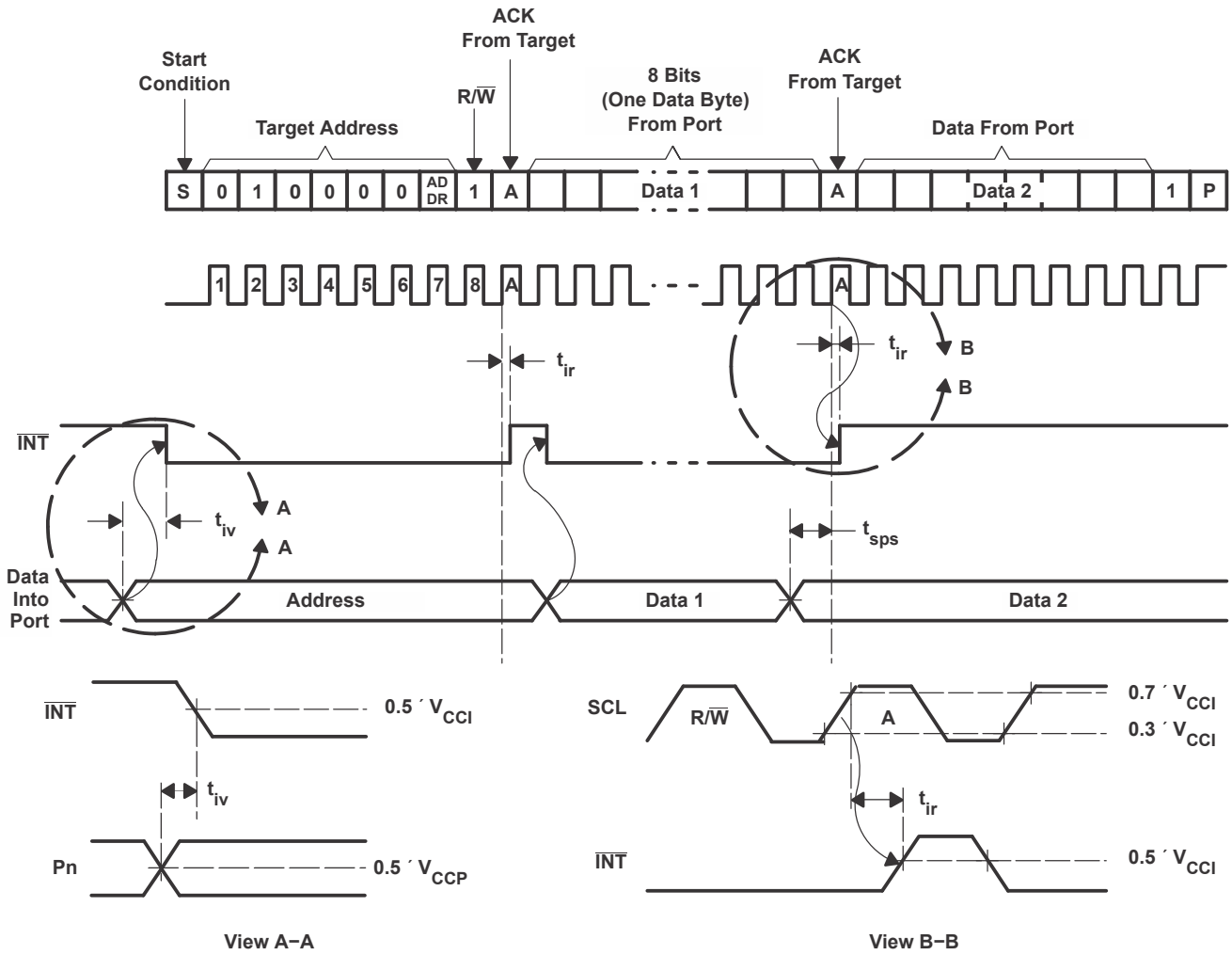
BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2	Input register port data

- A.  $C_L$  includes probe and jig capacitance.  $t_{ocf}$  is measured with  $C_L$  of 10 pF or 400 pF.
- B. All inputs are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

Figure 7-1. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms

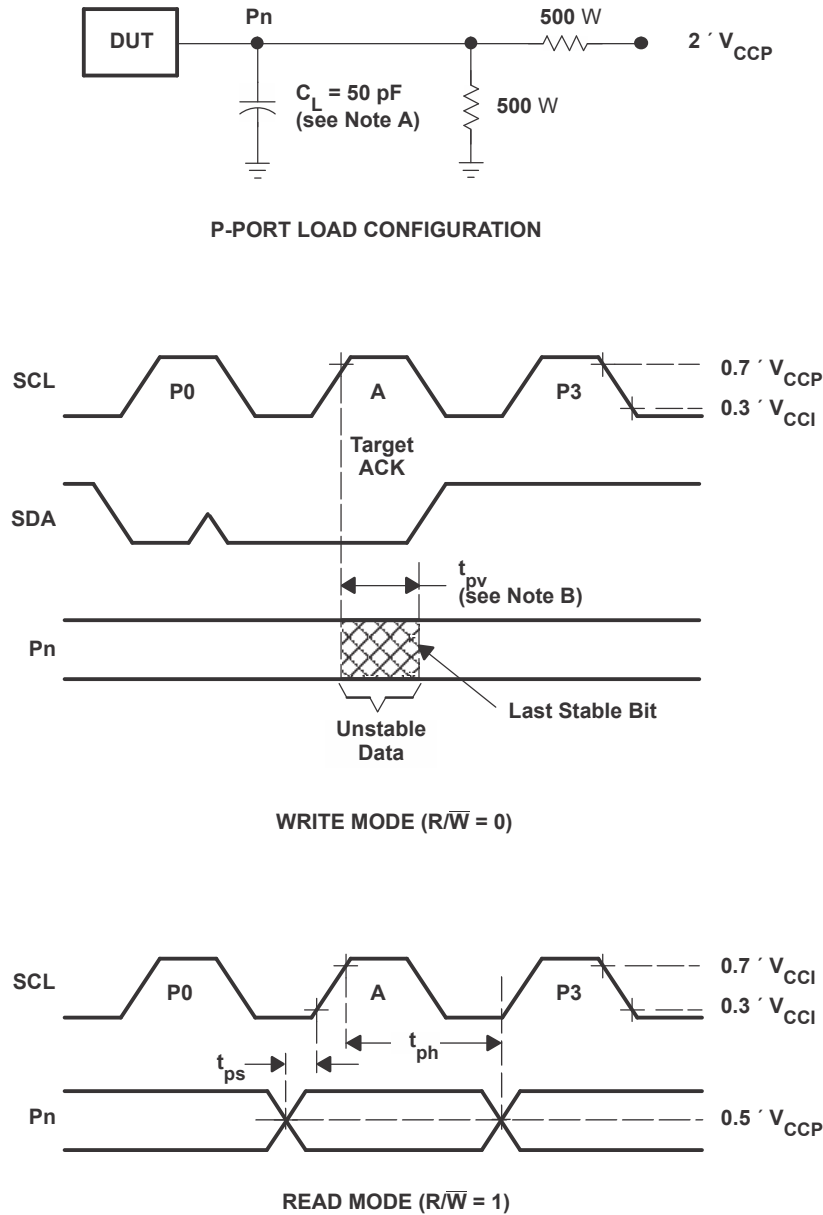


INTERRUPT LOAD CONFIGURATION



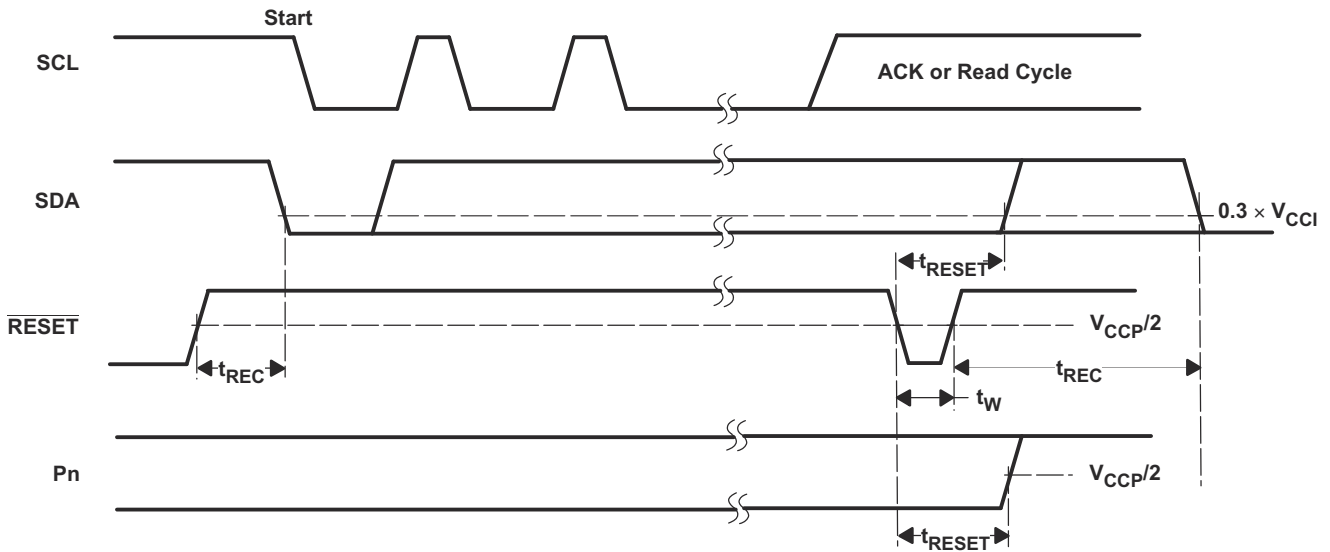
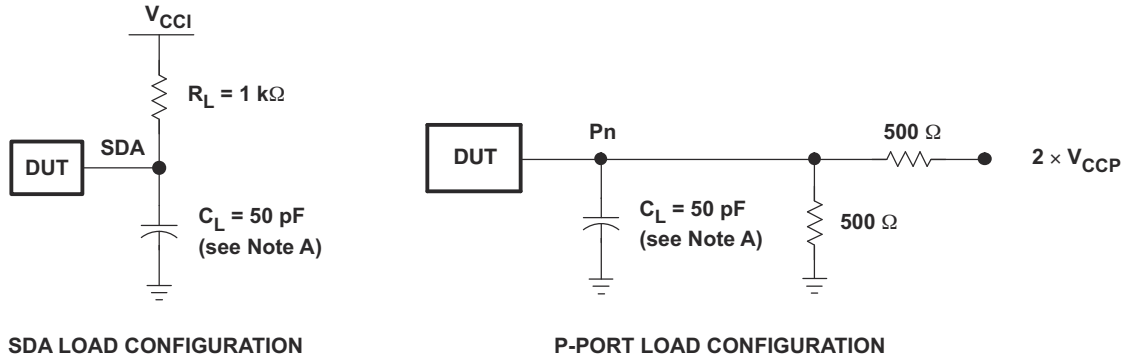
- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_0 = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

**Figure 7-2. Interrupt Load Circuit And Voltage Waveforms**



- A.  $C_L$  includes probe and jig capacitance.
- B.  $t_{pv}$  is measured from  $0.7 \times V_{CC}$  on SCL to 50% I/O ( $P_n$ ) output.
- C. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 7-3. P-Port Load Circuit And Timing Waveforms**



- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r/t_f \leq 30\text{ ns}$ .
- C. The outputs are measured one at a time, with one transition per measurement.
- D. I/Os are configured as inputs.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 7-4. Reset Load Circuits And Voltage Waveforms**



## 8 Detailed Description

### 8.1 Overview

The bidirectional voltage-level translation in the TCA6408A is provided through  $V_{CCI}$ .  $V_{CCI}$  should be connected to the  $V_{CC}$  of the external SCL/SDA lines. This indicates the  $V_{CC}$  level of the I<sup>2</sup>C bus to the TCA6408A. The voltage level on the P-port of the TCA6408A is determined by  $V_{CCP}$ .

The TCA6408A consists of one 8-bit Configuration (input or output selection), Input, Output, and Polarity Inversion (active high) Register. At power on, the I/Os are configured as inputs. However, the system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output Register. The polarity of the Input Port Register can be inverted with the Polarity Inversion Register. All registers can be read by the system controller.

The system controller can reset the TCA6408A in the event of a timeout or other improper operation by asserting a low in the  $\overline{\text{RESET}}$  input. The power-on reset puts the registers in their default state and initializes the I<sup>2</sup>C/SMBus state machine. The  $\overline{\text{RESET}}$  pin causes the same reset/initialization to occur without depowering the part.

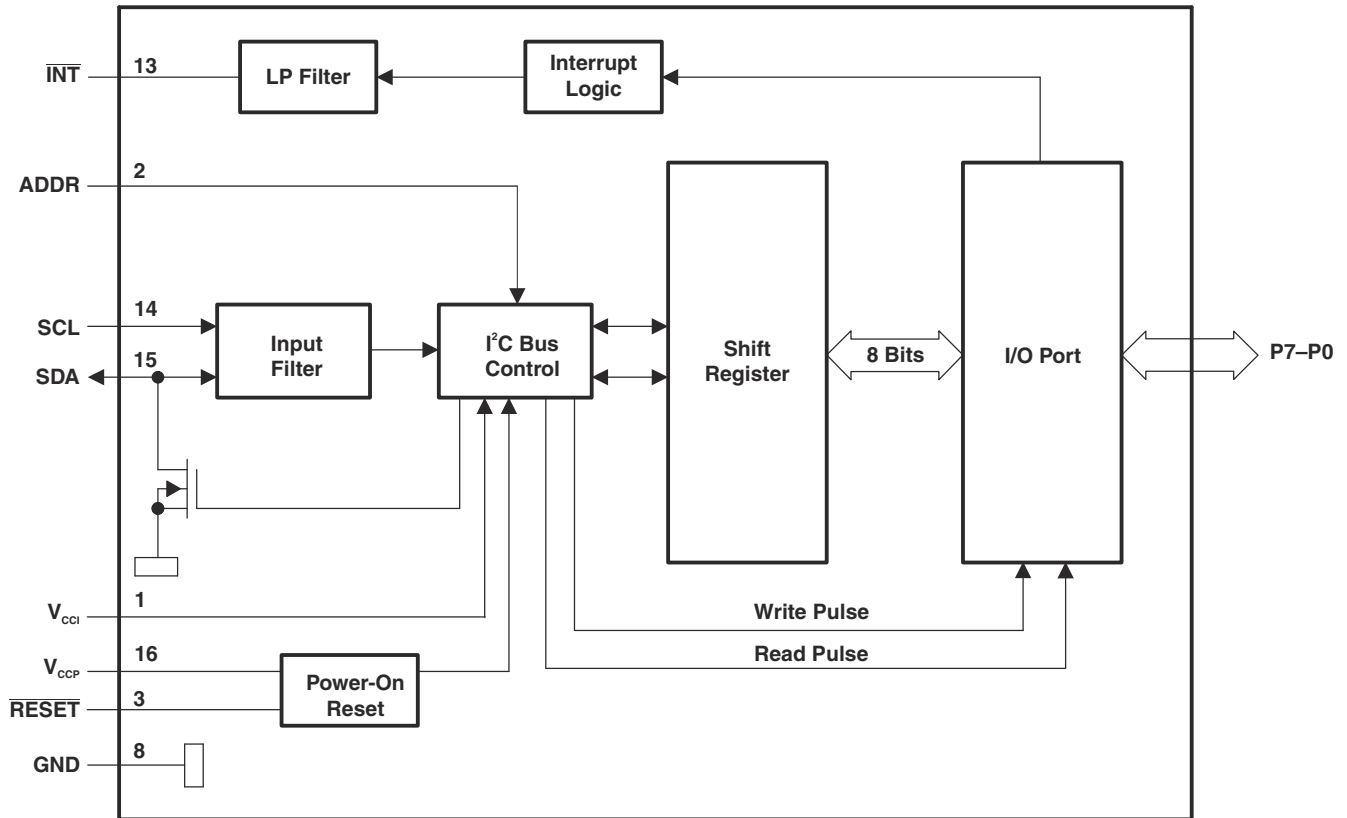
The TCA6408A open-drain interrupt ( $\overline{\text{INT}}$ ) output is activated when any input state differs from its corresponding Input Port Register state and is used to indicate to the system controller that an input state has changed.

$\overline{\text{INT}}$  can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C bus. Thus, the TCA6408A can remain a simple target device.

The device P-port outputs have high-current sink capabilities for directly driving LEDs while consuming low device current.

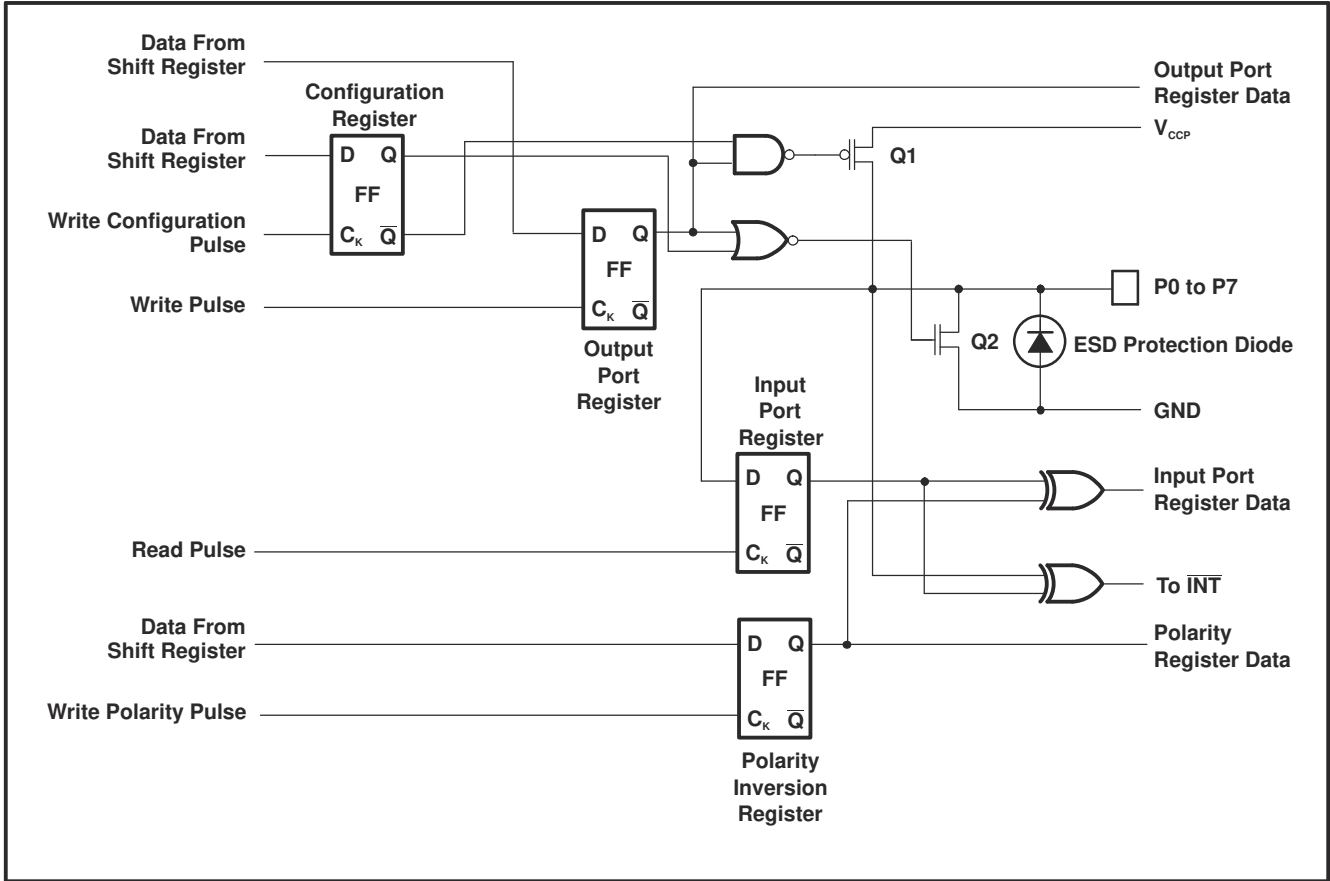
One hardware pin (ADDR) can be used to program and vary the fixed I<sup>2</sup>C address and allow up to two devices to share the same I<sup>2</sup>C bus or SMBus.

## 8.2 Functional Block Diagrams



- A. All pin numbers shown are for the PW package.
- B. All I/Os are set to inputs at reset.

**Figure 8-1. Logic Diagram (Positive Logic)**



A. On power up or reset, all registers return to default values.

**Figure 8-2. Simplified Schematic of P0 to P7**

## 8.3 Feature Description

### 8.3.1 Voltage Translation

Table 8-1 shows some common supply voltage options for voltage translation between the I<sup>2</sup>C bus and the P-ports of the TCA6408A.

**Table 8-1. Voltage Translation**

V <sub>CCI</sub> (SCL AND SDA OF I <sup>2</sup> C CONTROLLER) (V)	V <sub>CCP</sub> (P-PORT) (V)
1.8	1.8
1.8	2.5
1.8	3.3
1.8	5
2.5	1.8
2.5	2.5
2.5	3.3
2.5	5
3.3	1.8
3.3	2.5
3.3	3.3
3.3	5
5	1.8
5	2.5
5	3.3
5	5

### 8.3.2 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V<sub>CC</sub> to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V<sub>CC</sub> or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

### 8.3.3 Interrupt Output ( $\overline{\text{INT}}$ )

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time  $t_{iv}$ , the signal  $\overline{\text{INT}}$  is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or when data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as  $\overline{\text{INT}}$ .

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

The  $\overline{\text{INT}}$  output has an open-drain structure and requires pull-up resistor to V<sub>CCP</sub> or V<sub>CCI</sub>, depending on the application.  $\overline{\text{INT}}$  should be connected to the voltage source of the device that requires the interrupt information.

### 8.3.4 Reset Input ( $\overline{\text{RESET}}$ )

The  $\overline{\text{RESET}}$  input can be asserted to initialize the system while keeping the V<sub>CCP</sub> at its operating level. A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin low for a minimum of  $t_w$ . The TCA6408A registers and

I<sup>2</sup>C/SMBus state machine are changed to their default state once  $\overline{\text{RESET}}$  is low (0). When  $\overline{\text{RESET}}$  is high (1), the I/O levels at the P-port can be changed externally or through the controller. This input requires a pull-up resistor to  $V_{\text{CCI}}$ , if no active connection is used.

## 8.4 Device Functional Modes

### 8.4.1 Power-On Reset (POR)

When power (from 0 V) is applied to  $V_{\text{CCP}}$ , an internal power-on reset holds the TCA6408A in a reset condition until  $V_{\text{CCP}}$  has reached  $V_{\text{POR}}$ . At that time, the reset condition is released, and the TCA6408A registers and I<sup>2</sup>C/SMBus state machine initialize to their default states. After that,  $V_{\text{CCP}}$  must be lowered to below  $V_{\text{PORF}}$  and back up to the operating voltage for a power-reset cycle.

### 8.4.2 Powered-Up

When power has been applied to both  $V_{\text{CCP}}$  and  $V_{\text{CCI}}$  and a POR has taken place, the device is in a functioning mode. The device will always be ready to receive new requests via the I<sup>2</sup>C bus.

## 8.5 Programming

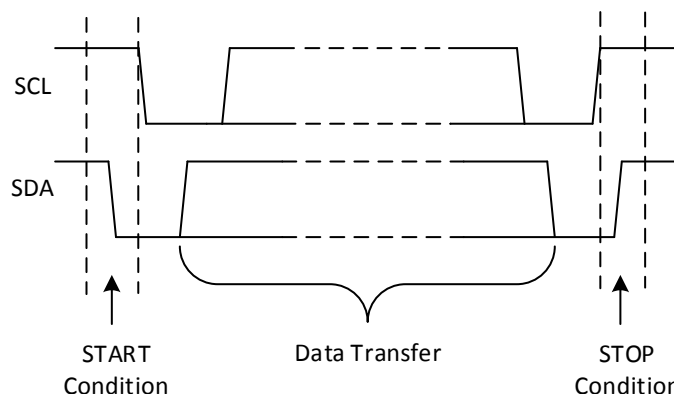
### 8.5.1 I<sup>2</sup>C Interface

The TCA6408A has a standard bidirectional I<sup>2</sup>C interface that is controlled by a controller device in order to be configured or read the status of this device. Each target on the I<sup>2</sup>C bus has a specific device address to differentiate between other target devices that are on the same I<sup>2</sup>C bus. Many target devices will require configuration upon startup to set the behavior of the device. This is typically done when the controller accesses internal register maps of the target, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read.

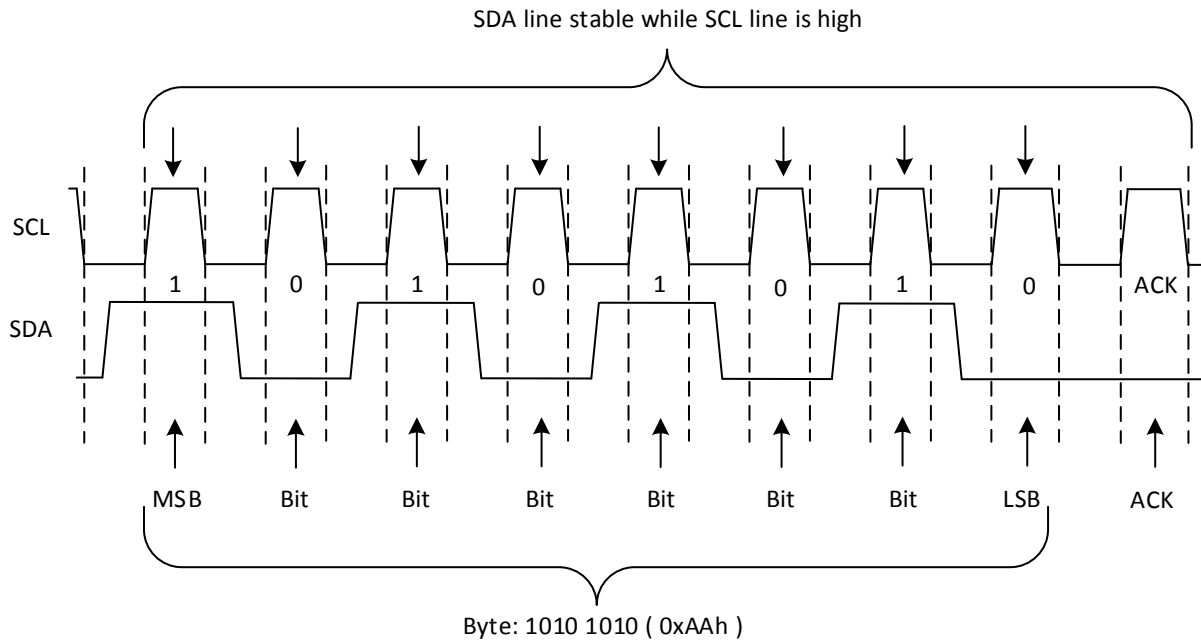
The physical I<sup>2</sup>C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to  $V_{\text{CC}}$  through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I<sup>2</sup>C lines. (For further details, refer to *I<sup>2</sup>C Pull-up Resistor Calculation (SLVA689)*.) Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition.

The following is the general procedure for a controller to access a target device:

1. If a controller wants to send data to a target:
  - Controller-transmitter sends a START condition and addresses the target-receiver.
  - Controller-transmitter sends data to target-receiver.
  - Controller-transmitter terminates the transfer with a STOP condition.
2. If a controller wants to receive or read data from a target:
  - Controller-receiver sends a START condition and addresses the target-transmitter.
  - Controller-receiver sends the requested register to read to target-transmitter.
  - Controller-receiver receives data from the target-transmitter.
  - Controller-receiver terminates the transfer with a STOP condition.



**Figure 8-3. Definition of Start and Stop Conditions**

**Figure 8-4. Bit Transfer****Table 8-2. Interface Definition**

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C target address	L	H	L	L	L	L	ADDR	R/ $\bar{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

## 8.5.2 Bus Transactions

Data must be sent to and received from the target devices, and this is accomplished by reading from or writing to registers in the target device.

Registers are locations in the memory of the target which contain information, whether it be the configuration information or some sampled data to send back to the controller. The controller must write information to these registers in order to instruct the target device to perform a task.

While it is common to have registers in I<sup>2</sup>C targets, note that not all target devices will have registers. Some devices are simple and contain only 1 register, which may be written to directly by sending the register data immediately after the target address, instead of addressing a register. An example of a single-register device would be an 8-bit I<sup>2</sup>C switch, which is controlled via I<sup>2</sup>C commands. Since it has 1 bit to enable or disable a channel, there is only 1 register needed, and the controller merely writes the register data after the target address, skipping the register number.

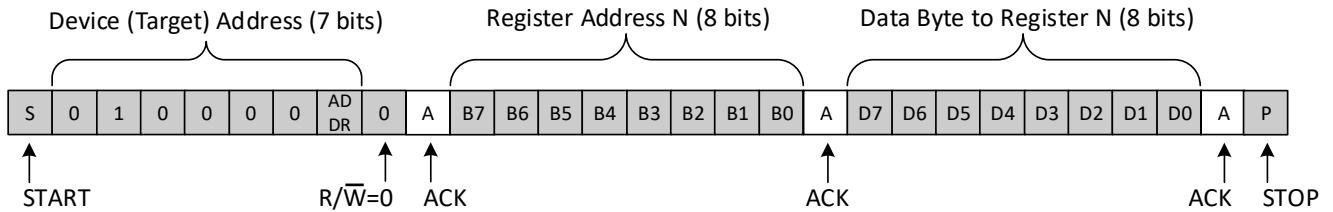
### 8.5.2.1 Writes

To write on the I<sup>2</sup>C bus, the controller will send a START condition on the bus with the address of the target, as well as the last bit (the R/  $\bar{W}$  bit) set to 0, which signifies a write. After the target sends the acknowledge bit, the controller will then send the register address of the register to which it wishes to write. The target will acknowledge again, letting the controller know it is ready. After this, the controller will start sending the register data to the target until the controller has sent all the data necessary (which is sometimes only a single byte), and the controller will terminate the transmission with a STOP condition.

Figure 8-5 shows an example of writing a single byte to a target register.

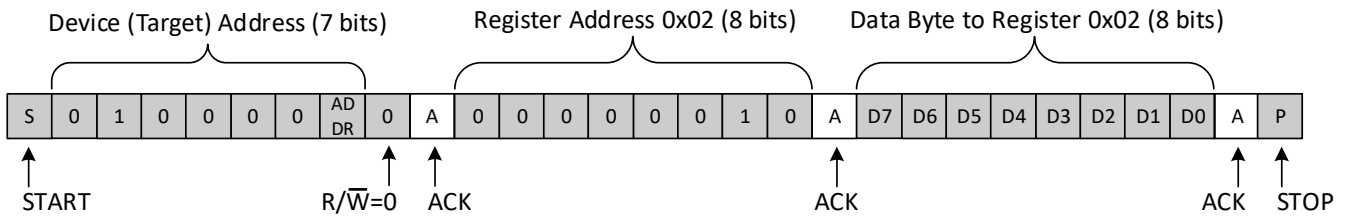
- Controller controls SDA line
- Target controls SDA line

Write to one register in a device



**Figure 8-5. Write to Register**

- Controller controls SDA line
- Target controls SDA line



**Figure 8-6. Write to the Polarity Inversion Register**

### 8.5.2.2 Reads

Reading from a target is very similar to writing, but requires some additional steps. In order to read from a target, the controller must first instruct the target which register it wishes to read from. This is done by the controller starting off the transmission in a similar fashion as the write, by sending the address with the  $R/\bar{W}$  bit equal to 0 (signifying a write), followed by the register address it wishes to read from. Once the target acknowledges this register address, the controller will send a START condition again, followed by the target address with the  $R/\bar{W}$  bit set to 1 (signifying a read). This time, the target will acknowledge the read request, and the controller will release the SDA bus but will continue supplying the clock to the target. During this part of the transaction, the controller will become the controller-receiver, and the target will become the target-transmitter.

The controller will continue to send out the clock pulses, but will release the SDA line so that the target can transmit data. At the end of every byte of data, the controller will send an ACK to the target, letting the target know that it is ready for more data. Once the controller has received the number of bytes it is expecting, it will send a NACK, signaling to the target to halt communications and release the bus. The controller will follow this up with a STOP condition.

Figure 8-7 shows an example of reading a single byte from a target register.

- Controller controls SDA line
- Target controls SDA line

#### Read from one register in a device

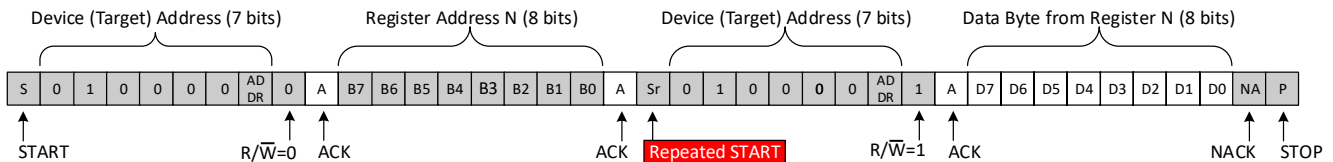
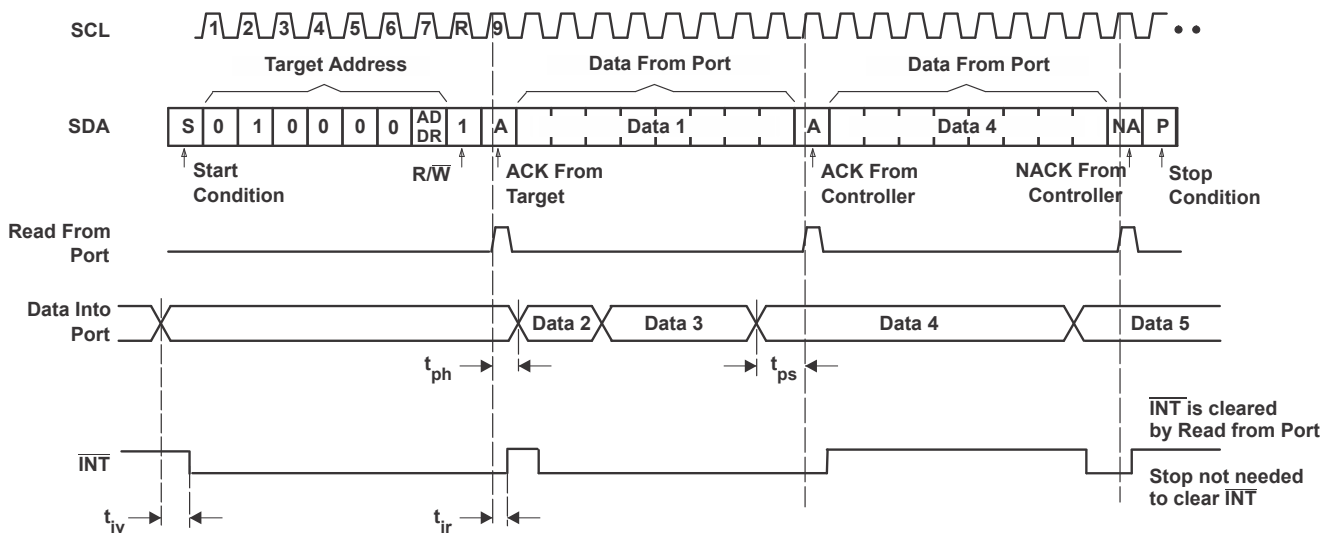


Figure 8-7. Read from Register



- A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port Register).
- B. This figure eliminates the command byte transfer, a restart, and target address call between the initial target address call and actual data transfer from P-port (see Figure 8-7).

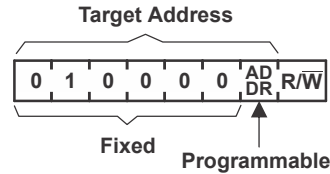
Figure 8-8. Read from Input Port Register



## 8.6 Register Map

### 8.6.1 Device Address

The address of the TCA6408A is shown in [Figure 8-9](#).



**Figure 8-9. TCA6408A Address**

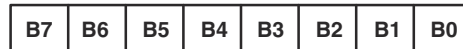
**Table 8-3. Address Reference**

ADDR	I <sup>2</sup> C BUS TARGET ADDRESS
L	32 (decimal), 20 (hexadecimal)
H	33 (decimal), 21 (hexadecimal)

The last bit of the target address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

### 8.6.2 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte, which is stored in the Control Register in the TCA6408A. Two bits of this data byte will state both the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register can be written or read through the I<sup>2</sup>C bus. The command byte is sent only during a write transmission.



**Figure 8-10. Control Register Bits**

**Table 8-4. Command Byte**

CONTROL REGISTER BITS								COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00	Input Port	Read byte	xxxx xxxx
0	0	0	0	0	0	0	1	01	Output Port	Read/write byte	1111 1111
0	0	0	0	0	0	1	0	02	Polarity Inversion	Read/write byte	0000 0000
0	0	0	0	0	0	1	1	03	Configuration	Read/write byte	1111 1111

### 8.6.3 Register Descriptions

The Input Port Register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration Register. They act only on read operation. Writes to this register have no effect. The default value (X) is determined by the externally applied logic level. Before a read operation, a write transmission is sent with the command byte to indicate to the I<sup>2</sup>C device that the Input Port Register will be accessed next.

**Table 8-5. Register 0 (Input Port Register)**

BIT	I-7	I-6	I-5	I-4	I-3	I-2	I-1	I-0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port Register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration Register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

**Table 8-6. Register 1 (Output Port Register)**

BIT	O-7	O-6	O-5	O-4	O-3	O-2	O-1	O-0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion Register (register 2) allows polarity inversion of pins defined as inputs by the Configuration Register. If a bit in this register is set (written with 1), the polarity of the corresponding port pin is inverted. If a bit in this register is cleared (written with a 0), the original polarity of the corresponding port pin is retained.

**Table 8-7. Register 2 (Polarity Inversion Register)**

BIT	N-7	N-6	N-5	N-4	N-3	N-2	N-1	N-0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration Register (register 3) configures the direction of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

**Table 8-8. Register 3 (Configuration Register)**

BIT	C-7	C-6	C-5	C-4	C-3	C-2	C-1	C-0
DEFAULT	1	1	1	1	1	1	1	1

## 9 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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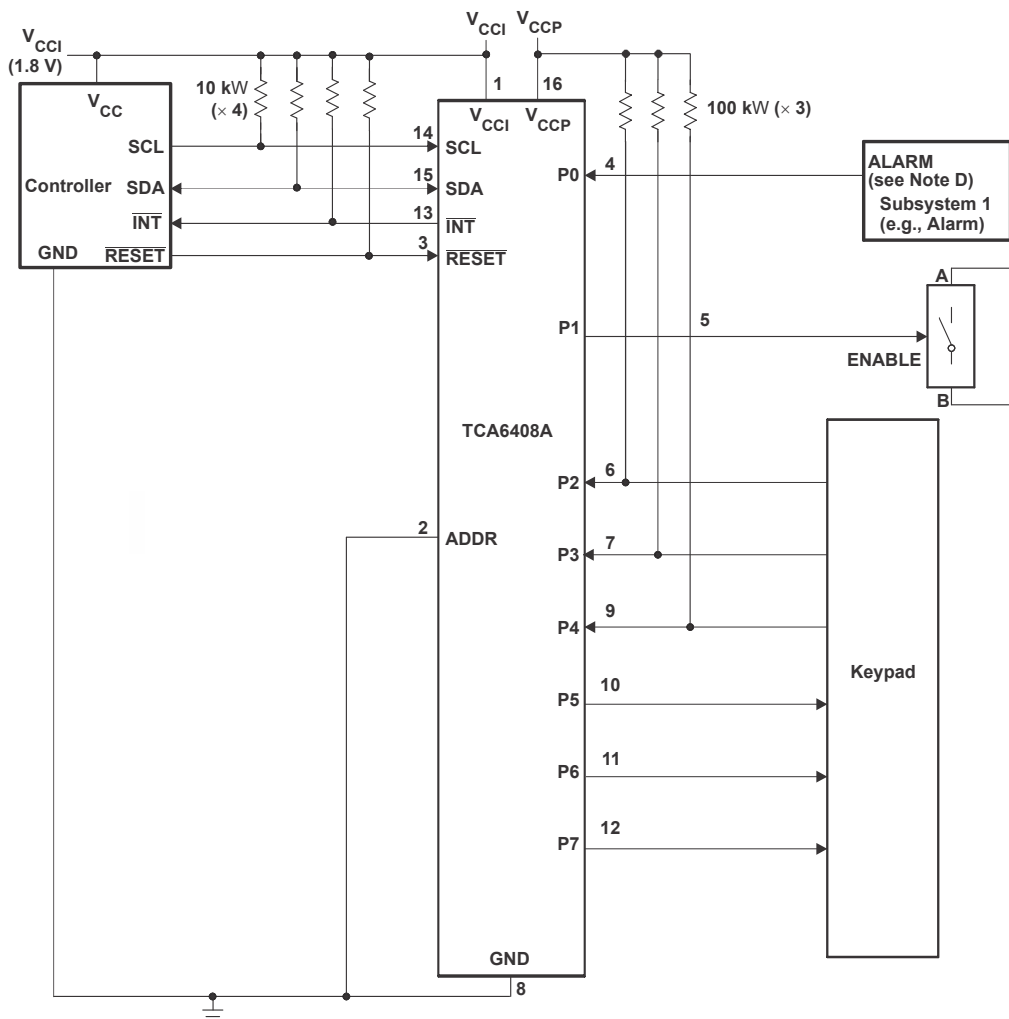
### 9.1 Application Information

Applications of the TCA6408A will have this device connected as a target to an I<sup>2</sup>C controller (processor), and the I<sup>2</sup>C bus may contain any number of other target devices. The TCA6408A will be in a remote location from the controller, placed close to the GPIOs to which the controller needs to monitor or control.

A typical application of the TCA6408A will operate with a lower voltage on the controller side ( $V_{CCI}$ ), and a higher voltage on the P-port side ( $V_{CCP}$ ). The P-ports can be configured as outputs connected to inputs of devices such as enable, reset, power select, the gate of a switch, and LEDs. The P-ports can also be configured as inputs to receive data from interrupts, alarms, status outputs, or push buttons.

## 9.2 Typical Application

Figure 9-1 shows an application in which the TCA6408A can be used.



- A. Device address configured as 0100000 for this example.
- B. P0 and P2–P4 are configured as inputs.
- C. P1 and P5–P7 are configured as outputs.
- D. Resistors are required for inputs (on P-port) that may float. If a driver to an input will never let the input float, a resistor is not needed. Outputs (in the P-port) do not need pull-up resistors.

Figure 9-1. Typical Application Schematic

### 9.2.1 Design Requirements

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
I <sup>2</sup> C input voltage (V <sub>CC1</sub> )	1.8 V
P-port input/output voltage (V <sub>CCP</sub> )	5 V
Output current rating, P-port sinking (I <sub>OL</sub> )	25 mA
Output current rating, P-port sourcing (I <sub>OH</sub> )	10 mA
I <sup>2</sup> C bus clock (SCL) speed	400 kHz

### 9.2.2 Detailed Design Procedure

The pull-up resistors,  $R_p$ , for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the I<sup>2</sup>C bus. The minimum pull-up resistance is a function of  $V_{CC}$ ,  $V_{OL(max)}$ , and  $I_{OL}$ :

$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$ :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9538,  $C_i$  for SCL or  $C_{IO}$  for SDA, the capacitance of wires, connections, and traces, and the capacitance of additional targets on the bus.

#### 9.2.2.1 Minimizing $I_{CC}$ When I/O is Used to Control LEDs

When the I/Os are used to control LEDs, normally they are connected to  $V_{CC}$  through a resistor as shown in Figure 9-1. The LED acts as a diode, so when the LED is off, the I/O  $V_{IN}$  is about 1.2 V less than  $V_{CC}$ . The  $\Delta I_{CC}$  parameter in Section 6.5 shows how  $I_{CC}$  increases as  $V_{IN}$  becomes lower than  $V_{CC}$ . Designs that must minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to  $V_{CC}$  when the LED is off.

Figure 9-2 shows a high-value resistor in parallel with the LED. Figure 9-3 shows  $V_{CC}$  less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O  $V_{IN}$  at or above  $V_{CC}$  and prevent additional supply current consumption when the LED is off.

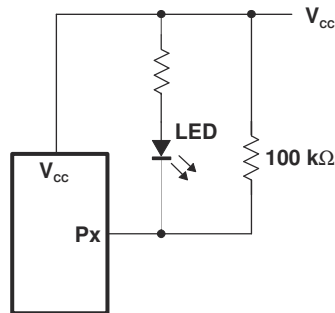


Figure 9-2. High-Value Resistor in Parallel With LED

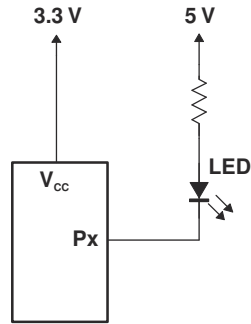
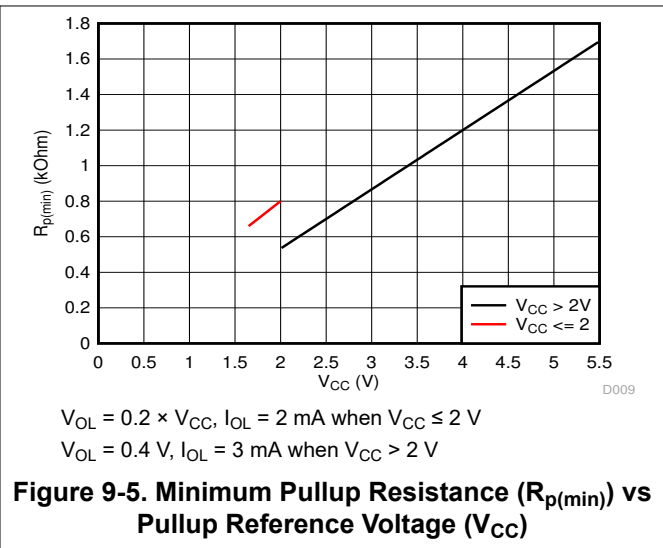
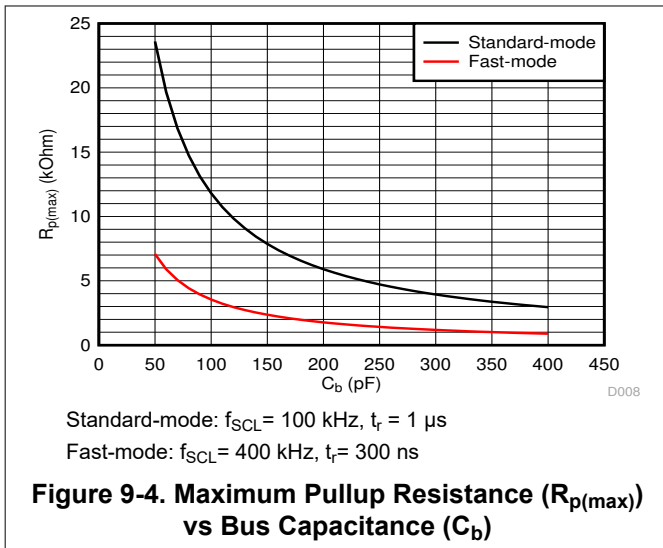


Figure 9-3. Device Supplied by a Low Voltage

9.2.3 Application Curves



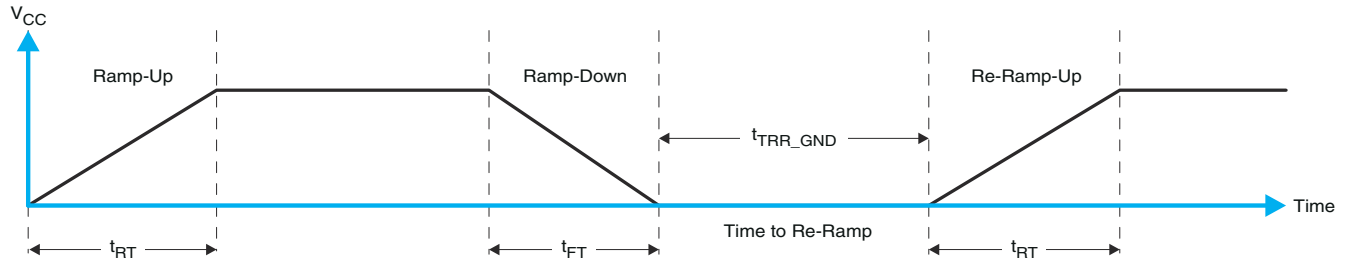
## 10 Power Supply Recommendations

### 10.1 Power-On Reset Requirements

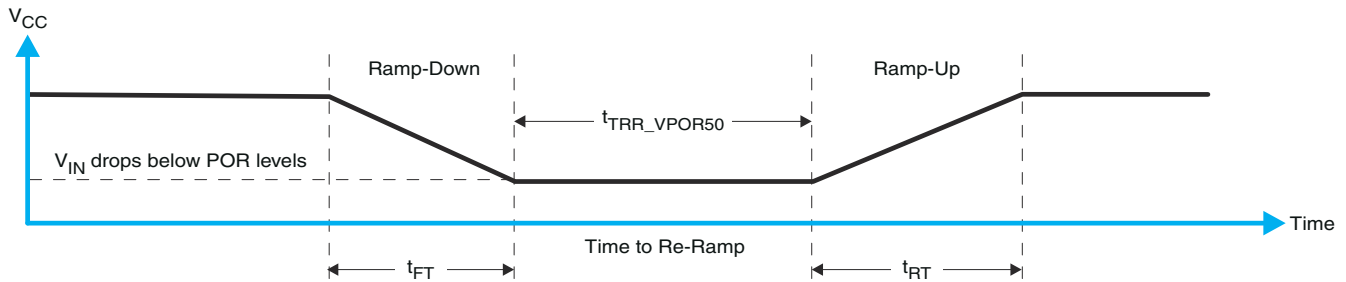
In the event of a glitch or data corruption, TCA6408A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

Ramping up the device  $V_{CCP}$  before  $V_{CCI}$  is recommended to prevent SDA from potentially being stuck LOW.

The two types of power-on reset are shown in [Figure 10-1](#) and [Figure 10-2](#).



**Figure 10-1.  $V_{CC}$  is Lowered Below 0.2 V Or 0 V and then Ramped Up to  $V_{CC}$**



**Figure 10-2.  $V_{CC}$  is Lowered Below the POR Threshold, then Ramped Back Up to  $V_{CC}$**

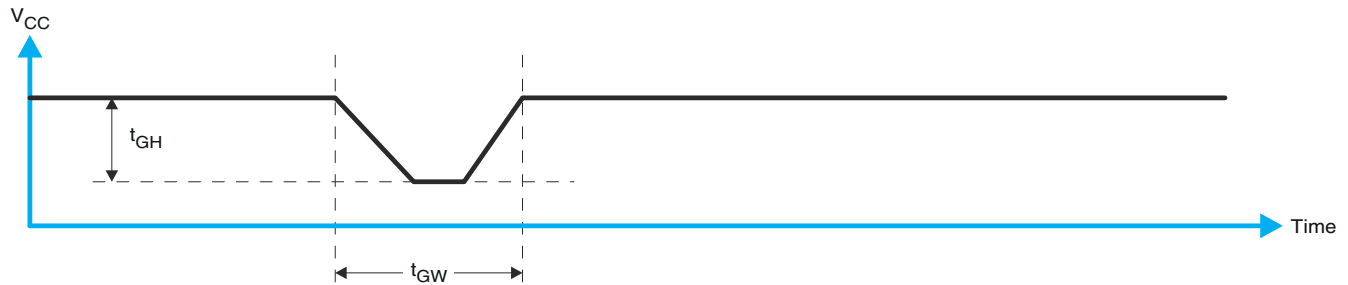
[Table 10-1](#) specifies the performance of the power-on reset feature for TCA6408A for both types of power-on reset.

**Table 10-1. Recommended Supply Sequencing and Ramp Rates at  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>**

PARAMETER			MIN	TYP	MAX	UNIT
$t_{FT}$	Fall rate	See <a href="#">Figure 10-1</a>	0.1		2000	ms
$t_{RT}$	Rise rate	See <a href="#">Figure 10-1</a>	0.1		2000	ms
$t_{RR\_GND}$	Time to re-ramp (when $V_{CC}$ drops to GND)	See <a href="#">Figure 10-1</a>	1			$\mu\text{s}$
$t_{RR\_POR50}$	Time to re-ramp (when $V_{CC}$ drops to $V_{POR\_MIN} - 50 \text{ mV}$ )	See <a href="#">Figure 10-2</a>	1			$\mu\text{s}$
$V_{CC\_GH}$	Level that $V_{CCP}$ can glitch down to, but not cause a functional disruption when $V_{CCX\_GW} = 1 \mu\text{s}$	See <a href="#">Figure 10-3</a>			1.2	V
$t_{GW}$	Glitch width that will not cause a functional disruption when $V_{CCX\_GH} = 0.5 \times V_{CCx}$	See <a href="#">Figure 10-3</a>			10	$\mu\text{s}$
$V_{PORF}$	Voltage trip point of POR on falling $V_{CC}$		0.7			V
$V_{PORR}$	Voltage trip point of POR on rising $V_{CC}$				1.4	V

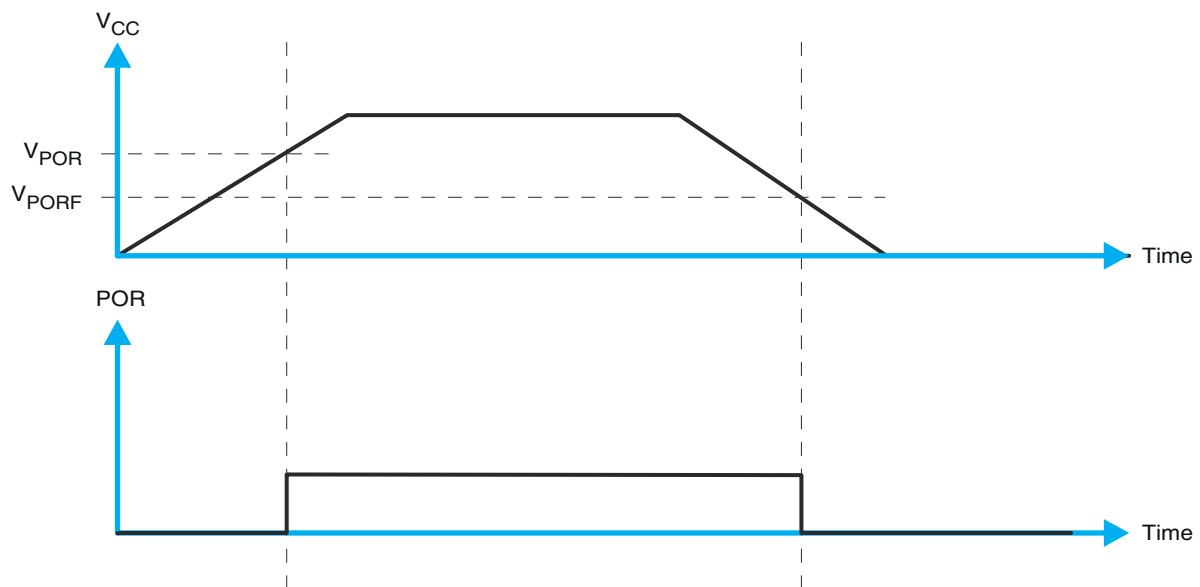
(1) Not tested. Specified by design.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $t_{GW}$ ) and height ( $t_{GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 10-3 and Table 10-1 provide more information on how to measure these specifications.



**Figure 10-3. Glitch Width And Glitch Height**

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to the default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. Figure 10-4 and Table 10-1 provide more details on this specification.



**Figure 10-4.  $V_{POR}$**



## 11 Layout

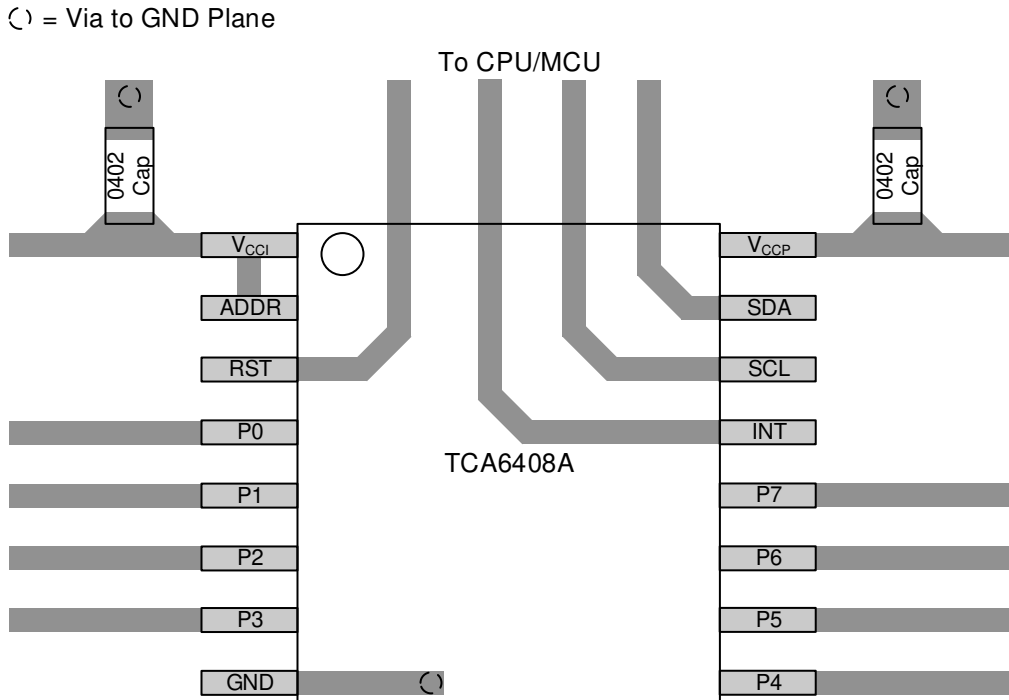
### 11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA6408A, common PCB layout practices should be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V<sub>CCP</sub> pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the TCA6408A as possible. These best practices are shown in [Section 11.2](#).

For the layout example provided in [Section 11.2](#), it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V<sub>CCI</sub> and V<sub>CCP</sub>) and ground (GND). However, a 4-layer board is preferable for boards with higher density signal routing. On a 4-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V<sub>CCI</sub>, V<sub>CCP</sub>, or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in [Section 11.2](#).

### 11.2 Layout Example



**Figure 11-1. Example Layout (PW Package)**

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.3 Trademarks

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### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

### Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA6408APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH408A	<a href="#">Samples</a>
TCA6408ARGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVU	<a href="#">Samples</a>
TCA6408ARSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZVU	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TCA6408A :**

- Automotive : [TCA6408A-Q1](#)

NOTE: Qualified Version Definitions:

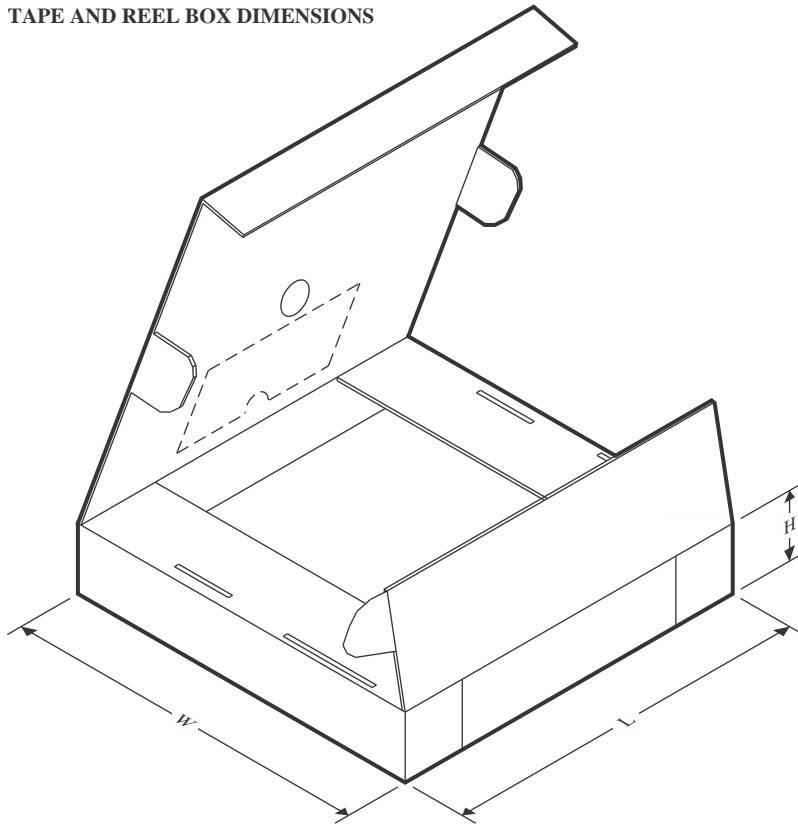
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA6408APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TCA6408ARGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TCA6408ARSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

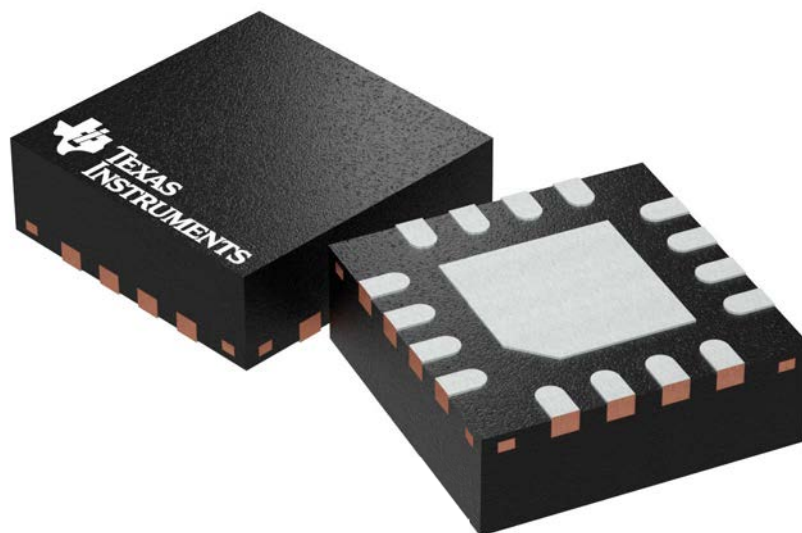
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA6408APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TCA6408ARGTR	VQFN	RGT	16	3000	356.0	356.0	35.0
TCA6408ARSVR	UQFN	RSV	16	3000	202.0	201.0	28.0

**RGT 16**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203495/1



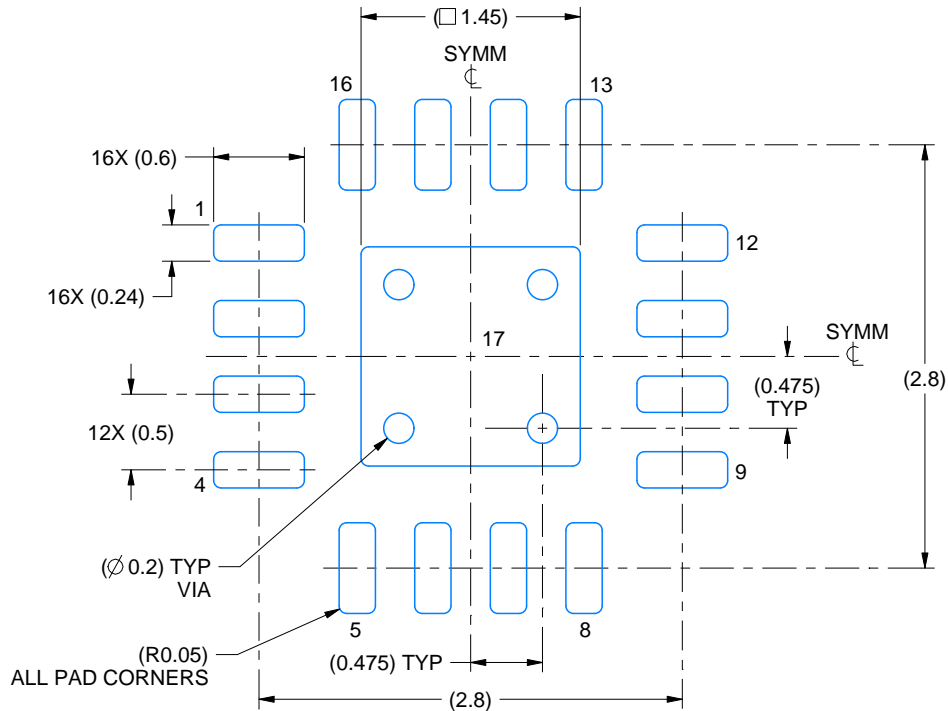


# EXAMPLE BOARD LAYOUT

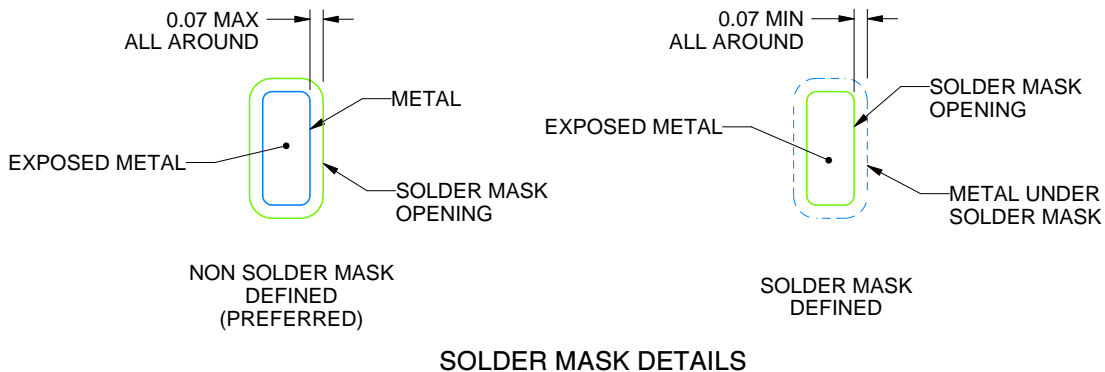
RGT0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

4219032/A 02/2017

NOTES: (continued)

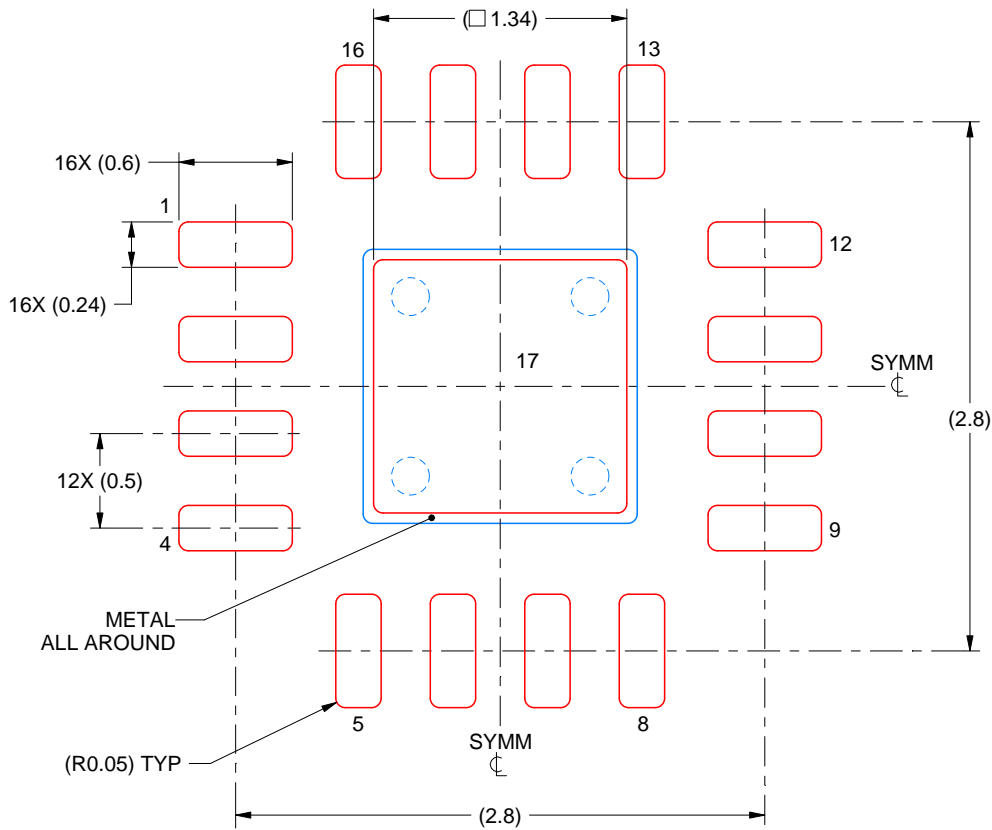
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGT0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4219032/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

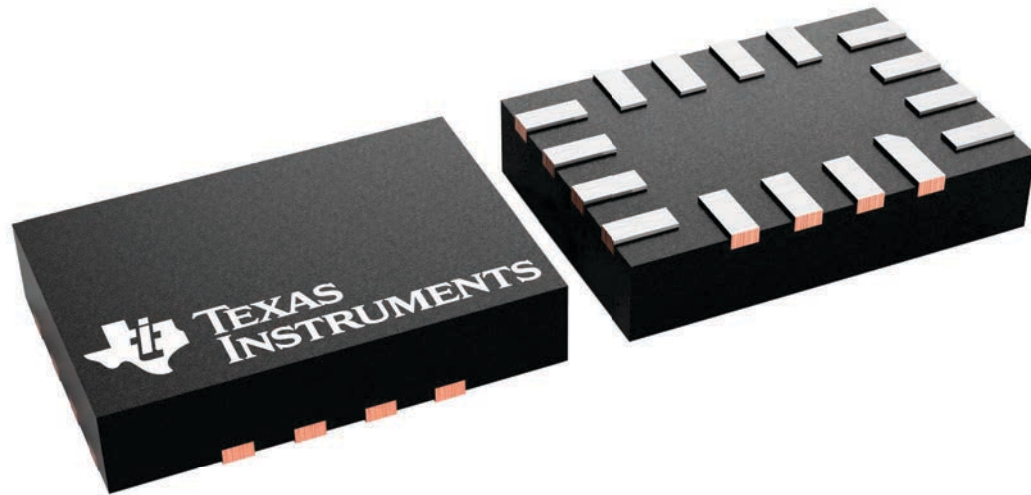
**RSV 16**

**UQFN - 0.55 mm max height**

1.8 x 2.6, 0.4 mm pitch

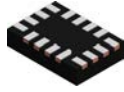
ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231225/A

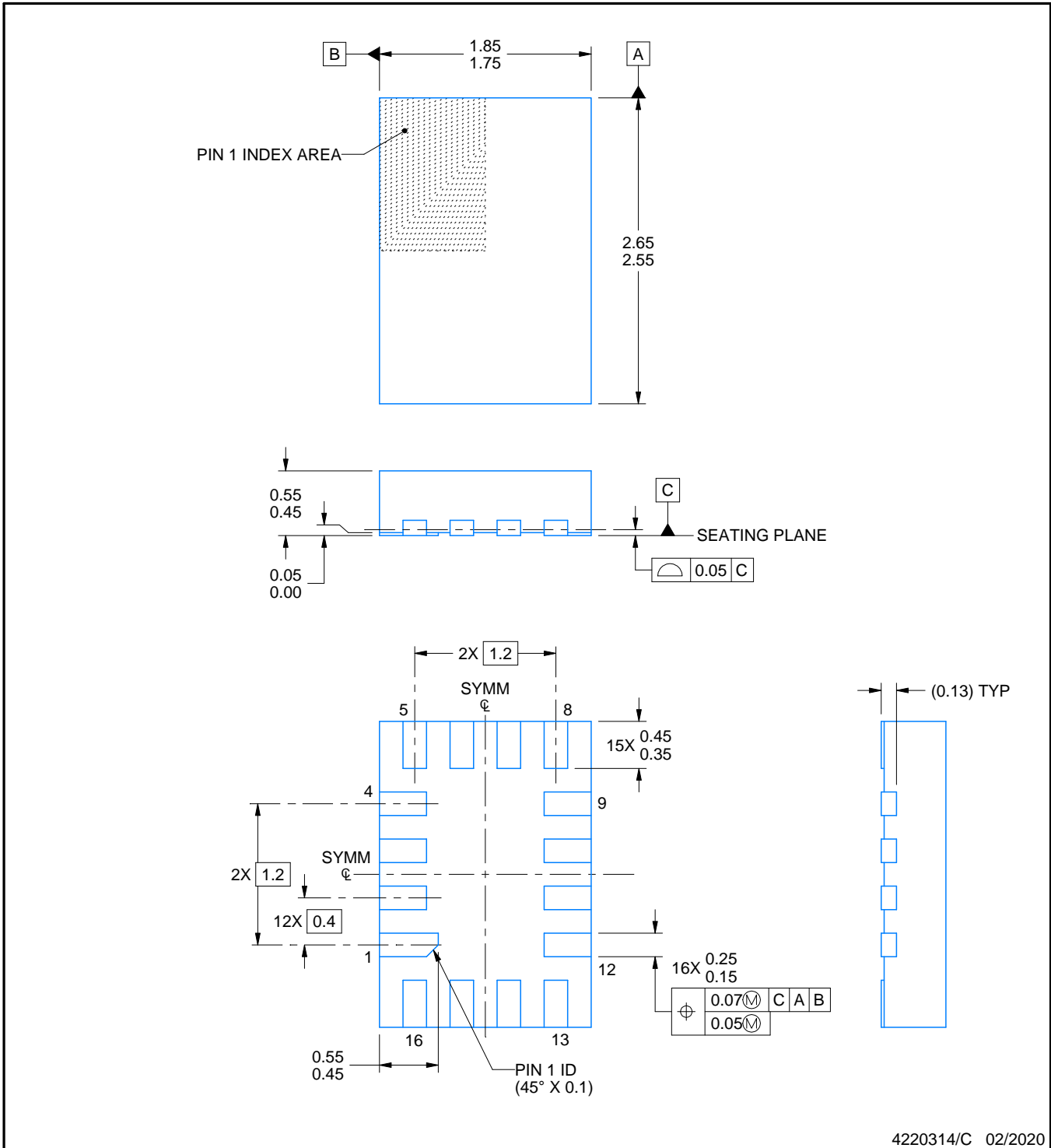
RSV0016A



# PACKAGE OUTLINE

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



NOTES:

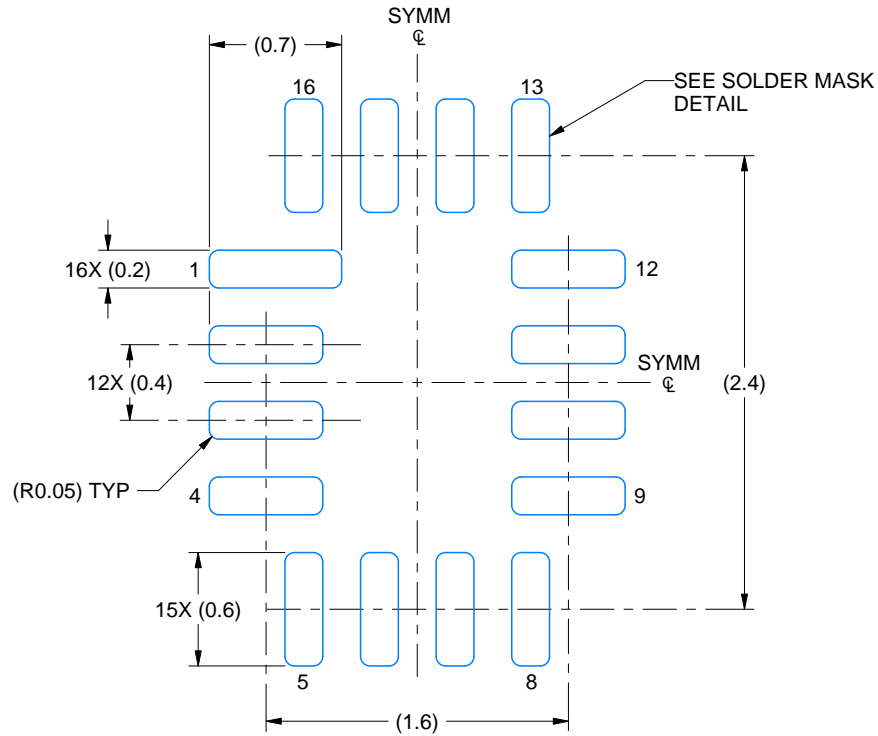
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

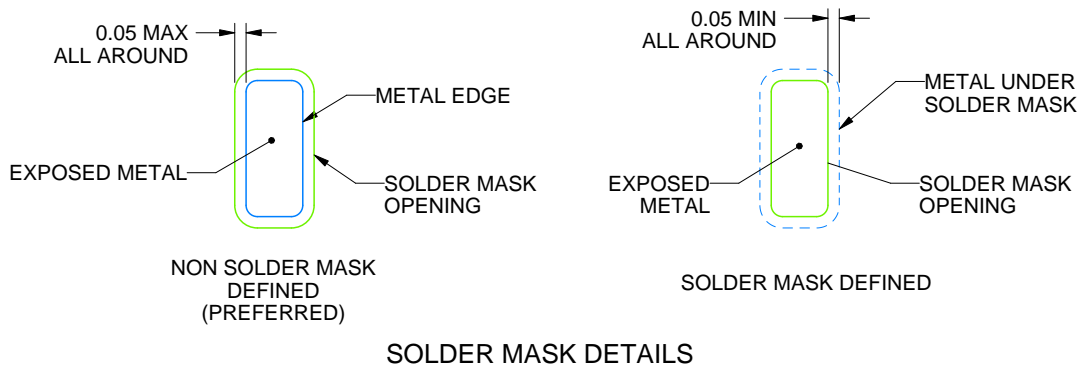
RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

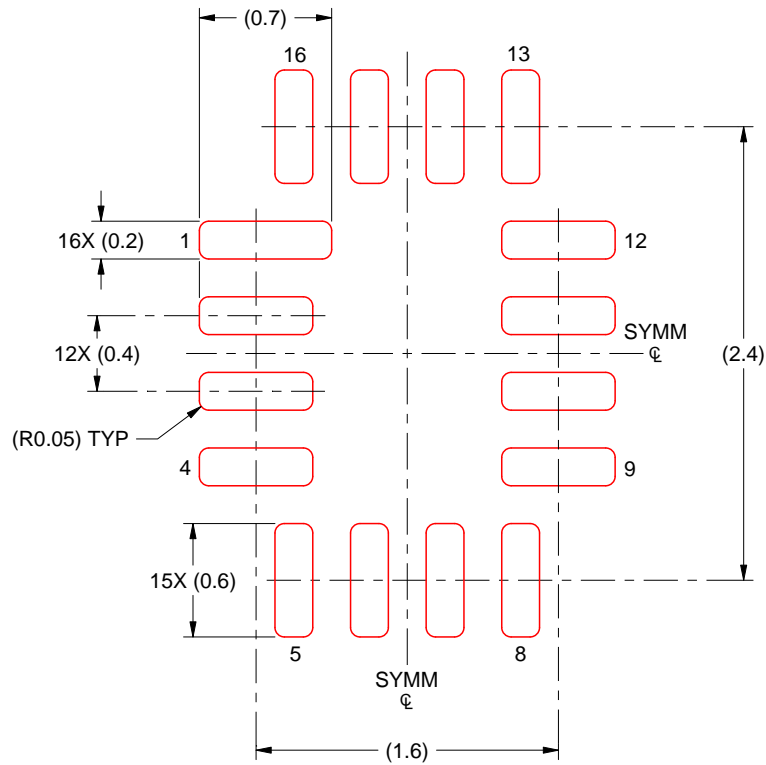


# EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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