TCAN1162-Q1 Automotive Self-Supplied CAN FD Transceiver with Sleep Mode

1 Features

- AEC Q100 (Grade 1) Qualified for automotive applications
- Meets the requirements of ISO 11898-2:2016
- Functional Safety-Capable
  - Documentation available to aid in functional safety system design
- Wide input operational voltage range
- Integrated LDO for CAN transceiver supply
- Classic CAN and CAN FD up to 8Mbps
- V_{IO} level shifting supports: 1.7V to 5.5V
- Operating modes
  - Normal mode
  - Standby mode
  - Low-power sleep mode
- High-voltage INH output for system power control
- Local wake-up support via the WAKE pin
- Defined behavior when unpowered
  - Bus and IO terminals are high impedance (no load to operating bus or application)
- Protection features:
  - ±58V CAN bus fault tolerant
  - Load dump support on V_{SUP}
  - IEC ESD protection
  - Under-voltage and over-voltage protection
  - Thermal shutdown protection
  - TXD dominant state timeout (TXD DTO)
- Extra wide junction temperature support
- Available in the leadless VSON (14) package with wettable flank for improved automated optical inspection (AOI) capability

2 Applications

- Advanced driver assistance system (ADAS)
- Body electronics and lighting
- Automotive infotainment and cluster
- Hybrid, electric and powertrain systems

3 Description

The TCAN1162-Q1 is a high-speed Controller Area Network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2016 high-speed CAN specification. The TCAN1162-Q1 supports both classical CAN and CAN FD networks up to 8 megabits per second (Mbps).

The TCAN1162-Q1 integrates a 5V LDO with a wide input operating range which provides the CAN transceiver voltage thereby eliminating the need for the 5V supply to be supplied from an external voltage source.

The TCAN1162-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a system via the INH output pin. This allows an ultra-low-current sleep state where power is gated to all system components except for the TCAN1162-Q1, while monitoring the CAN bus. When a wake-up event is detected, the TCAN1162-Q1 initiates system start-up by driving INH high.

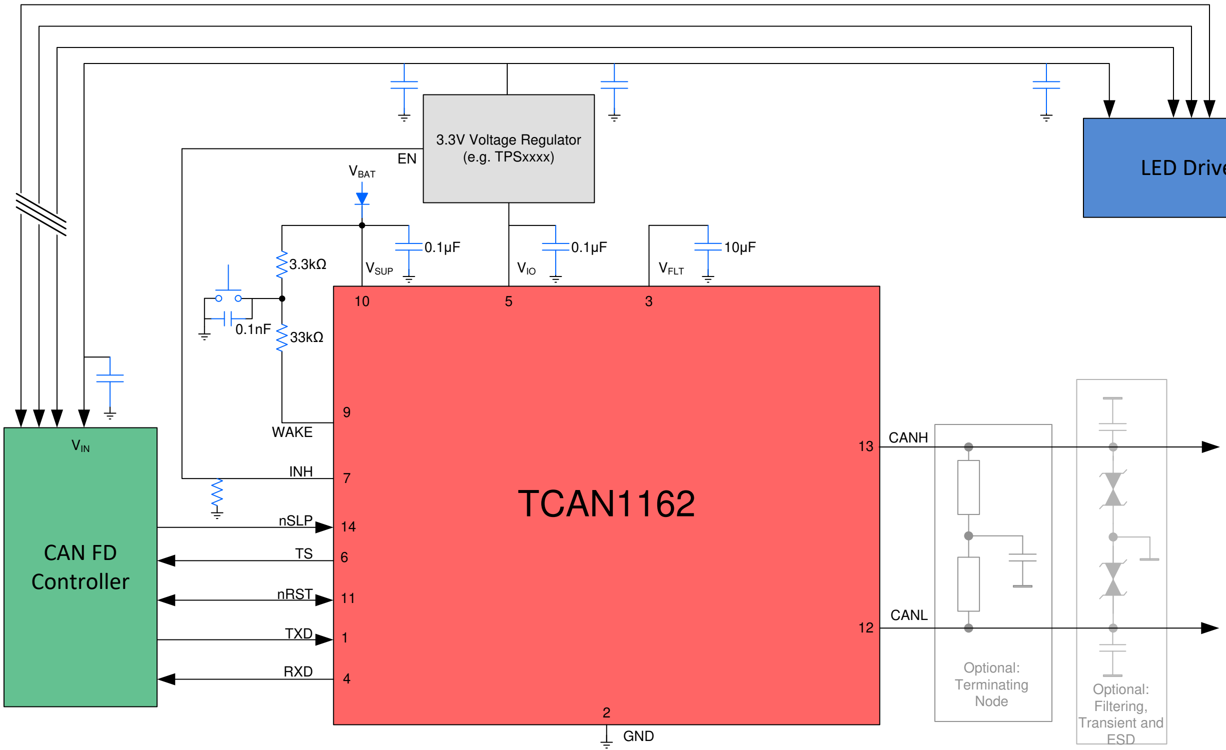
The TCAN1162-Q1 supports an ultra low-power standby mode where the high-speed transmitter and normal receiver are switched off and a low-power wake-up receiver enables remote wake-up via the ISO 11898-2:2016 defined wake-up pattern (WUP).

The TCAN1162-Q1 includes internal logic level translation via the V_{IO} terminal to allow for interfacing directly to 1.8V, 2.5V, 3.3V, or 5V controllers. The transceiver includes many protection and diagnostic features including undervoltage detection, over voltage detection, thermal shutdown (TSD), driver dominant timeout (TXD DTO), and bus fault protection up to ±58V.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TCAN1162-Q1	VSON (14)	4.5mm x 3mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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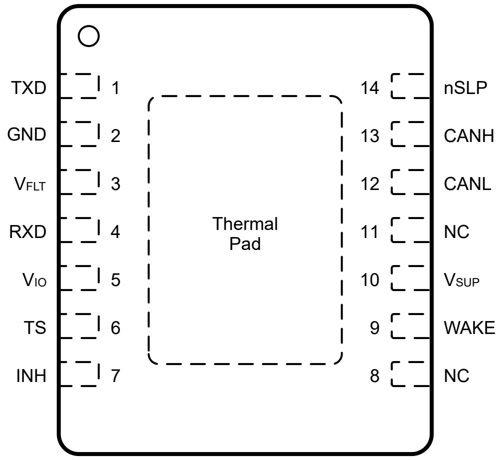
4 Pin Configurations and Functions



Not to scale

Figure 4-1. DMT Package, 14 Pin (VSON), Top View

Table 4-1. Pin Functions

PINS		TYPE	Description
Name	No.		
TXD	1	Digital	CAN transmit data input, integrated pull-up
GND	2	GND	Ground connection
V_{FLT}	3	Supply	Transceiver supply voltage
RXD	4	Digital Output	CAN receive data output, tri-state when $V_{IO} < UV_{VIO}$
V_{IO}	5	Supply	IO supply voltage
TS	6	Digital	Transceiver status
INH	7	High Voltage	Inhibit pin to control system voltage regulators and supplies, high voltage
NC	8	NC	Internally connected, leave floating or connect to GND
WAKE	9	High Voltage	Local WAKE input terminal, high voltage
V_{SUP}	10	Supply	High voltage supply from the battery
NC	11	NC	Internally connected, leave floating or connect to GND
CANL	12	Bus IO	Low level CAN bus input/output line
CANH	13	Bus IO	High level CAN bus input/output line
nSLP	14	Digital	Sleep mode control input, integrated pull-down
Thermal Pad	—		Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

5 Specifications

5.1 Absolute Maximum Ratings

over operating virtual junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage range	–0.3	42	V
V_{FLT}	Transceiver supply voltage	-0.3	6	V
V_{IO}	IO level shifting voltage range	–0.3	6	V
V_{BUS}	CAN bus IO voltage range (CANH, CANL)	–58	58	V
V_{WAKE}	WAKE input pin voltage range	–18	42 and $V_I \leq V_{SUP} + 0.3$	V
V_{INH}	INH output pin voltage range	–0.3	42 and $V_O \leq V_{SUP} + 0.3$	V
$V_{(Logic\_Input)}$	Logic input terminal voltage range	–0.3	6	V
$V_{(Logic\_Output)}$	Logic output terminal voltage range	–0.3	6	V
$I_{O(LOGIC)}$	Logic output current		8	mA
$I_{O(INH)}$	INH output current		6	mA
$I_{O(WAKE)}$	Wake current if due to ground shifts $V_{(WAKE)} \leq V_{(GND)} – 0.3$ V, thus the current into WAKE must be limited via an external serial resistor		3	mA
T_J	Operating virtual junction temperature range	–40	150	°C
T_{STG}	Storage temperature	-65	165	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	HBM classification level 3A for all pin	±4000	V
			HBM classification level 3A for V_{SUP}, WAKE, INH	±8000	
			HBM classification level 3B for global pins CANH & CANL	±10000	
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	

(1) AEC-Q100-002 indicates that HBM stresses shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings IEC Specification

				VALUE	UNIT
V_{ESD}	System level electro-static discharge (ESD)(1)	CAN bus terminals (CANH & CANL) to GND	IEC 61000-4-2 (150pF, 330Ω) unpowered contact discharge	±8000	V
		V_{SUP} and WAKE		±8000	
V_{TRAN}	ISO 7637 ISO pulse transients(2)	CAN bus terminals (CANH & CANL) to GND, V_{SUP} and WAKE	Pulse 1	–100	
			Pulse 2	75	
			Pulse 3a	–150	
			Pulse 3b	100	
	ISO 7637-3 transient(3)		DCC slow transient pulse	±30	

(1) Tested according to IEC 62228-3 CAN Transceiver, Section 6.4; DIN EN 61000-4-2
(2) Tested according to IEC 62228-3 CAN Transceiver, Section 6.3; standard pulse parameters defined in ISO 7637-2
(3) Tested according to ISO 7637-3; electrical transient transmission by capacitive and inductive coupling via lines other than supply line

5.4 Recomended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage range	5.5		28	V
V_{IO}	IO supply voltage	1.7		5.5	V
$I_{OH(DO)}$	Digital output terminal high level output current	–2			mA
$I_{OL(DO)}$	Digital output terminal low level output current			2	mA
$I_{O(INH)}$	INH output current			1	mA
C_{VSUP}	V_{SUP} pin capacitance		0.1		µF
C_{FLT}	Filter pin capacitance	10			µF
T_{SDR}	Thermal shutdown rising	175	180		°C
T_{SDF}	Thermal shutdown falling		165	170	°C
T_{HYS}	Thermal shutdown hysterisis		15		°C

5.5 Thermal Information

THERMAL METRIC(1)		DMT (VSON)	UNIT
		14 PINS	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	37.7	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	37.9	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	14.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Power Supply Characteristics

Over recomended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage and Current						
I_{SUP}	Supply current Bus biasing active: dominant	TXD = 0 V, R_L = 60 Ω, C_L = open See Figure 6-2			60	mA
		TXD = 0 V, R_L = 50 Ω, C_L = open See Figure 6-2			70	mA
	Supply current Bus biasing active: recessive	TXD = V_{IO} , R_L = 50 Ω, C_L = open See Figure 6-2			3	mA
$I_{SUP(STB)}$	Supply current Standby mode Bus bias autonomous: inactive	5.5 V < V_{SUP} ≤ 19 V See Figure 6-2			150	µA
$I_{SUP(SLP)}$	Supply current Sleep mode Bus bias autonomous: inactive	nSLP = 0 V, 5.5 V < V_{SUP} ≤ 19 V T_A > 85°C See Figure 6-2			50	µA
$I_{SUP(SLP)}$	Supply current Sleep mode Bus bias autonomous: inactive	nSLP = 0 V, 5.5 V < V_{SUP} ≤ 19 V T_A ≤ 85°C See Figure 6-2			40	µA
$I_{SUP(BIAS)}$	Supply current Bus bias autonomous: active(1)	5.5 V < V_{SUP} ≤ 28 V See Figure 6-2			60	µA
UV_{SUPR}	Under voltage V_{SUP} threshold rising	Ramp Up	4.05		4.42	V
UV_{SUPF}	Under voltage V_{SUP} threshold falling	Ramp Down	3.9		4.25	V
I_{IO}	IO Supply Current Normal mode	RXD floating, TXD = 0 V			150	µA
I_{IO}	IO Supply Current Normal, or Standby	RXD floating, TXD = V_{IO}			12	µA

5.6 Power Supply Characteristics (continued)

Over recomended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IO}	IO Supply Current Sleep mode (T_J ≤ 125℃)	nSLP = 0 V			10	μA
UV_{IOR}	Under voltage V_{IO} threshold rising	Ramp Up		1.4	1.65	V
UV_{IOF}	Under voltage V_{IO} threshold falling	Ramp Down	1	1.25		V
$V_{HYS(UVIO)}$	Hysteresis voltage on UV_{VIO}		40	80	160	mV
V_{FLT} Characteristics						
V_{FLT}	CAN regulator filter pin	V_{SUP} = 5.5 to 28 V	4.9		5.1	V
UV_{FLTR}	Under voltage V_{FLT} threshold rising	Ramp Up		4.6	4.75	V
UV_{FLTF}	Under voltage V_{FLT} threshold falling	Ramp Down	4.2	4.45		V
OV_{FLTR}	Over voltage V_{FLT} threshold rising	Ramp Up		5.7	6.15	V
OV_{FLTF}	Over voltage V_{FLT} threshold falling	Ramp Down	5.47	5.65		V

(1) After a valid wake-up the total I_{SUP} current is the sum of $I_{SUP(STB)}$ and $I_{SUP(BIAS)}$ (I_{SUP} = $I_{SUP(STB)}$ + $I_{SUP(BIAS)}$)

5.7 Electrical Characteristics

Over recommended operating conditions with T_J = –40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V and R_L = 60 Ω

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN Driver Electrical Characteristics							
$V_{O(D)}$	Dominant output voltage Bus biasing active	CANH	TXD = 0 V, 50 ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open See Figure 6-2	2.75		4.5	V
	Dominant output voltage Bus biasing active	CANL		0.5		2.25	V
$V_{O(R)}$	Recessive output voltage Bus biasing active		TXD = V_{IO} , R_L = open (no load), R_{CM} = open See Figure 6-2	2		3	V
V_{SYM}	Driver symmetry Bus biasing active ($V_{O(CANH)}$ + $V_{O(CANL)}$) / V_{FLT}		nSLP = V_{IO}, R_L = 60 Ω, C_{SPLIT} = 4.7 nF, C_L = Open, R_{CM} = Open, TXD = 250 kHz, 1 Mhz, 2.5 MHz See Figure 6-2	0.9		1.1	V/V
V_{SYM_DC}	DC Driver symmetry Bus biasing active V_{FLT} – $V_{O(CANH)}$ – $V_{O(CANL)}$		nSLP = V_{IO}, R_L = 60 Ω, C_L = open See Figure 6-2	–400		400	mV
$V_{OD(DOM)}$	Differential output voltage Bus biasing active Dominant	CANH - CANL	nSLP = V_{IO}, TXD = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open See Figure 6-2	1.5		3	V
	Differential output voltage Bus biasing active Dominant	CANH - CANL	nSLP = V_{IO}, TXD = 0 V, 45 Ω ≤ R_L ≤ 70 Ω, CL = open See Figure 6-2	1.4		3.3	V
	Differential output voltage Bus biasing active Dominant	CANH - CANL	nSLP = V_{IO}, TXD = 0 V, R_L = 2240 Ω, C_L = open See Figure 6-2	1.5		5	V
$V_{OD(REC)}$	Differential output voltage Bus biasing active Bus biasing inactive Recessive	CANH - CANL	nSLP = V_{IO}, TXD = V_{IO} , R_L = open Ω, C_L = open See Figure 6-2	–50		50	mV
$V_{O(INACT)}$	Pin output voltage Bus biasing inactive	CANH	nSLP = 0 V, TXD = V_{IO} R_L = open (no load), C_L = open See Figure 6-2	-0.1		0.1	V
		CANL	nSLP = 0 V, TXD = V_{IO} R_L = open (no load), C_L = open See Figure 6-2	-0.1		0.1	V
$V_{OD(STB)}$	Differential output voltage Bus biasing inactive	CANH - CANL	nSLP = 0 V, TXD = V_{IO} R_L = open (no load), C_L = open See Figure 6-2	-0.2		0.2	V

5.7 Electrical Characteristics (continued)

Over recommended operating conditions with T_J = –40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OS(DOM)}$	Short-circuit steady-state output current Bus biasing active Dominant	nSLP = V_{IO}, TXD = 0 V -15 V ≤ $V_{(CANH)}$ ≤ 40 V See Figure 6-2 and Figure 6-6	–75			mA
	Short-circuit steady-state output current Bus biasing active Dominant	nSLP = $V_{IO,}$ TXD = 0 V -15 V ≤ $V_{(CANL)}$ ≤ 40 V See Figure 6-2 and Figure 6-6			75	mA
$I_{OS(REC)}$	Short-circuit steady-state output current Bus biasing active Recessive	nSLP = V_{IO}, V_{BUS} = CANH = CANL -27 V ≤ V_{BUS} ≤ 42 V See Figure 6-2 and Figure 6-6	–3		3	mA
CAN Receiver Electrical Characteristics						
$V_{IT(DOM)}$	Receiver dominant state input voltage range Bus biasing active	nSLP = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V See Figure 6-3 and Table 7-4	0.9		8	V
$V_{IT(REC)}$	Receiver recessive state input voltage range Bus biasing active		-3		0.5	V
V_{HYS}	Hysteresis voltage for input threshold Bus biasing active	nSLP = V_{IO} See Figure 6-3 and Table 7-4	80	140		mV
$V_{DIFF(MAX)}$	Maximum rating of V_{DIFF}		-5		10	V
$V_{DIFF(DOM)}$	Receiver dominant state input voltage range Bus biasing inactive	nSLP = 0 V, -12 V ≤ V_{CM} ≤ 12 V See Figure 6-3 and Table 7-4	1.150		8	V
$V_{DIFF(REC)}$	Receiver recessive state input voltage range Bus biasing inactive		-3		0.4	V
V_{CM}	Common mode range	nSLP = V_{IO} See Figure 6-3 and Table 7-4	–12		12	V
$I_{OFF(LKG)}$	Power-off (unpowered) bus input leakage current	V_{SUP} = 0 V, CANH = CANL = 5 V			2.5	μA
C_I	Input capacitance to ground (CANH or CANL) (1)	TXD = V_{IO}			20	pF
C_{ID}	Differential input capacitance(1)	TXD = V_{IO}			10	pF
R_{ID}	Differential input resistance	TXD = V_{IO} , nSLP = 5 V -12 V ≤ V_{CM} ≤ 12 V	50		100	kΩ
R_{IN}	Input resistance (CANH or CANL)		25		50	kΩ
$R_{IN(M)}$	Input resistance matching: [1 – $R_{IN(CANH)}$ / $R_{IN(CANL)}$] × 100%	$V_{(CANH)}$ = $V_{(CANL)}$ = 5 V	–1		1	%
TXD Input Characteristics						
V_{IH}	High level input voltage		0.7			V_{IO}
V_{IL}	Low level input voltage				0.3	V_{IO}
I_{IH}	High level input leakage current	TXD = V_{IO} = 5.5 V	–1	0	1	μA
I_{IL}	Low level input leakage current	TXD = 0 V, V_{IO} = 5.5 V	–130		–15	μA
R_{PU}	Pull-up resistance		40	60	80	kΩ
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V, V_{SUP} = V_{IO} = 0 V	–1	0	1	μA
C_I	Input Capacitance	V_{IN} = 0.4 x sin(2 × π × 2 × 10^6 × t) + 2.5 V		5		pF
RXD Output Characteristics						
V_{OH}	High level output voltage	I_O = –2 mA.	0.8			V_{IO}
V_{OL}	Low level output voltage	I_O = 2 mA.			0.2	V_{IO}
R_{PU}	Pull-up resistance		40	60	80	kΩ
$I_{LKG(OFF)}$	Unpowered leakage curret	RXD = 5.5 V, V_{SUP} = V_{IO} = 0 V	-5		5	μA
nSLP Input Characteristics						
V_{IH}	High level input voltage		0.7			V_{IO}
V_{IL}	Low level input voltage				0.3	V_{IO}
I_{IH}	High level input leakage current	nSLP = V_{IO} = 5.5 V	50		130	μA
I_{IL}	Low level input leakage current	nSLP = 0 V, V_{IO} = 5.5 V	–1		1	μA
R_{PD}	Pull-down resistance		40	60	80	kΩ
$I_{LKG(OFF)}$	Unpowered leakage current	nSLP = 5.5 V, V_{IO} = 0 V	–1	0	1	μA

5.7 Electrical Characteristics (continued)

Over recommended operating conditions with T_J = –40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INH Output Characteristics						
ΔV_H	High level voltage drop INH with respect to V_{SUP}	I_{INH} = –6 mA		0.5	1	V
$I_{LKG(INH)}$	Sleep mode leakage current	INH = 0 V	–0.5		0.5	μA
WAKE Input Characteristics						
V_{IH}	High-level input voltage	Sleep mode	4			V
V_{IL}	Low-level input voltage				2	V
I_{IL}	Low level input leakage current	WAKE = 1 V			3	μA
V_{HYS}	Input hysteresis		800		1200	mV
I_{IH}	High level input leakage current		–1	0	1	μA
TS Output Characteristics						
V_{OH}	High-level output voltage	I_O = -2 mA	0.8			V_{IO}
V_{OL}	Low-level output voltage	I_O = 2 mA			0.2	V_{IO}
$I_{LKG(OFF)}$	Unpowered leakage current	TS = 5.5 V, V_{IO} = 0 V	–1	0	1	μA

(1) Test according to ISO 11898-2:2003

5.8 Switching Characteristics

Over recomended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Switching Characteristics						
t_{POWER_UP}	CAN supply power up time	C_{FLT} = 10 μF nSLP = 5 V See Figure 6-7		1.8	4	ms
$t_{UV(SUP)}$	V_{SUP} filter time (rising and falling)		4		25	μs
$t_{UV(FLT)}$	Undervoltage detection delay time CAN active to CAN autonomous: active or inactive		4		25	μs
t_{UVIO}	V_{IO} filter time (rising and falling)		8		12	μs
Device Switching Characteristics						
$t_{UVIO(SLP)}$	Undervoltage detection delay time standby mode to sleep mode		200		350	ms
t_{WK_FILTER}	Bus time to meet filtered bus requirments for wakeup request	See Figure 7-4	0.5		1.8	μs
$t_{WK\_TIMEOUT}$	Bus wakeup timeout value		0.8		2	ms
$t_{SILENCE}$	Time out for bus inactivity			0.9	1.2	s
$t_{INACTIVE}$	Hardware timer for failsafe and power up inactivity(1)		3	4	5	min
t_{BIAS}	Time from the start of a dominant-recessive-dominant sequence until Vsym ≥ 0.1	Each phase: 6 μs See Figure 6-9			250	μs
$t_{CAN(ACTIVE)}$	Time from swtiching to CAN active mode to TS pin transitioning high	V_{FLT} > $UV_{FLT(R)}$ V_{IO} > $UV_{IO(R)}$ nSLP = V_{IO}			25	us
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD) Recessive to dominant	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF See Figure 6-4		100	160	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD) Dominant to recessive			120	175	ns
$t_{nSLP(fltr)}$	nSLP pin filter time	Sleep pin filter time	2.5		7.5	μs
t_{SLP}	Mode change time	Low time required on nSLP to enter sleep mode	20		35	μs
$t_{mode\_slp\_stb}$	WUP or LWU event to INH asserted high, see				50	μs
Driver Switching Characteristics						

5.8 Switching Characteristics (continued)

Over recomended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, V_{IO} = 3.3 V and R_L = 60 Ω

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHR}	Propagation delay time, high TXD to driver recessive		R_L = 60 Ω, C_L = 100 pF, R_{CM} = open See Figure 6-2	20	35	70	ns
t_{pLD}	Propagation delay time, low TXD to driver dominant			15	40	70	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHR}$ - $t_{pLD}\|$)				10	20	ns
t_R	Differential output signal rise time				40		ns
t_F	Differential output signal fall time				45		ns
t_{TXD_DTO}	Dominant timeout		R_L = 60 Ω, C_L = open See Figure 6-5, TXD = 0 V	1.2		3.8	ms
Receiver Switching Characteristics							
t_{pRH}	Propagation delay time, bus recessive input to high RXD		$C_{L(RXD)}$ = 15 pF See Figure 6-3	25	80	140	ns
t_{pDL}	Propagation delay time, bus dominant input to RXD low output			20	50	110	ns
t_R	Output signal rise time (RXD)				8		ns
t_F	Output signal fall time (RXD)				5		ns
WAKE Characteristics							
t_{WAKE}	Time required for INH pin to go high after an local wake event occurs on the WAKE pin			40			µs
CAN FD Timing Characteristics							
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	V_{IO} > 1.8V	R_L = 60 Ω, C_L = 100 pF $C_{L(RXD)}$ = 15 pF Δt_{REC} = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$ See Figure 6-4	435		530	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns			155		210	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 125 ns			80		140	ns
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	V_{IO} ≤ 1.8V	R_L = 60 Ω, C_L = 100 pF $C_{L(RXD)}$ = 15 pF Δt_{REC} = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$ See Figure 6-4	435		530	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns			155		215	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 125 ns			80		140	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns		R_L = 60 Ω, C_L = 100 pF $C_{L(RXD)}$ = 15 pF Δt_{REC} = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$ See Figure 6-4	400		550	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns			120		220	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 125 ns			80		135	ns
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns		R_L = 60 Ω, C_L = 100 pF $C_{L(RXD)}$ = 15 pF Δt_{REC} = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$ See Figure 6-4	-65		40	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns			-45		15	ns
	Receiver timing symetry with $t_{BIT(TXD)}$ = 125 ns			-40		10	ns

(1) Timer is reset when the CAN bus changes states.

5.9 Typical Characteristics

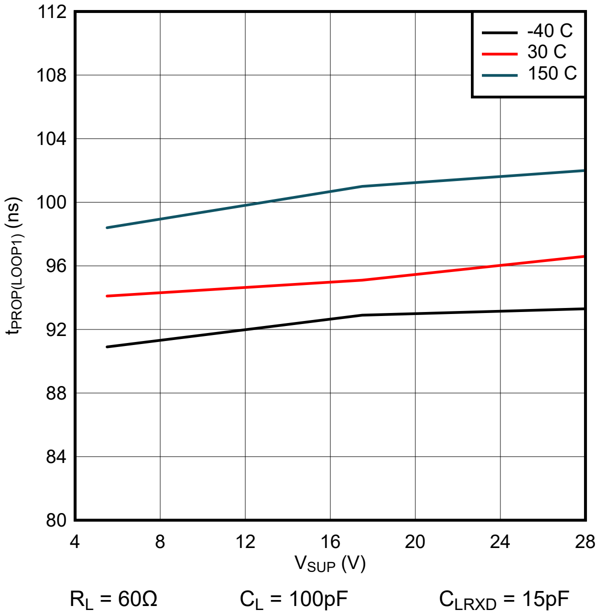


Figure 5-1. $t_{PROP(LOOP1)}$ over V_{SUP}

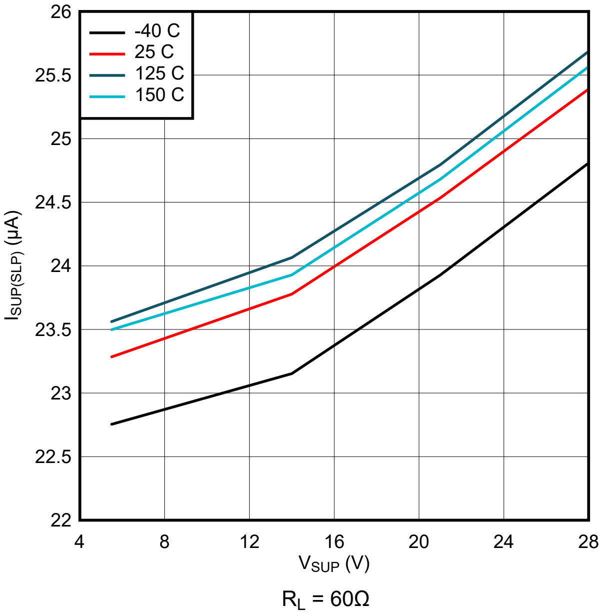


Figure 5-2. I_{SUP} over V_{SUP} Sleep Mode

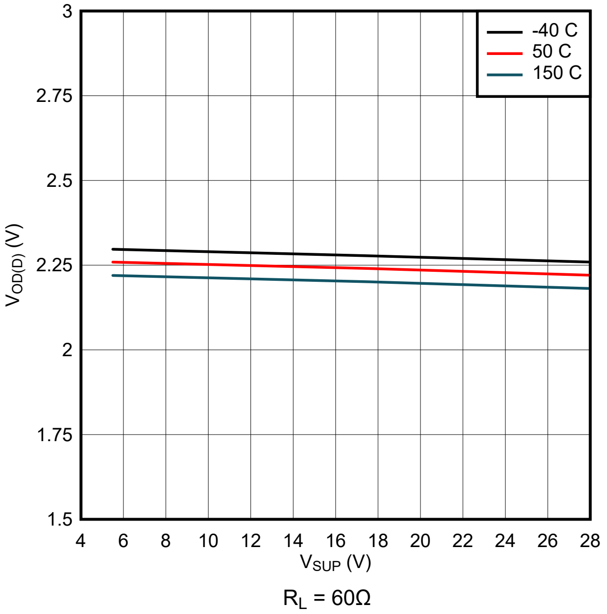


Figure 5-3. $V_{OD(DOM)}$ over V_{SUP}

6 Parameter Measurement Information

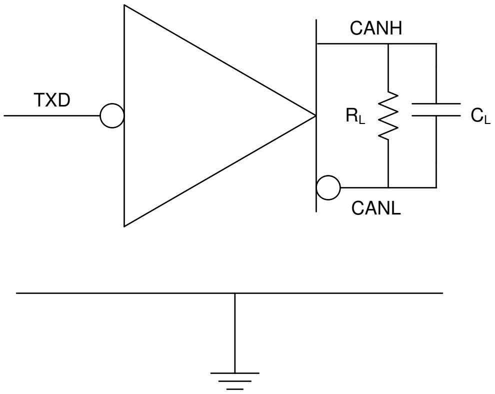


Figure 6-1. I_{SUP} Test Circuit

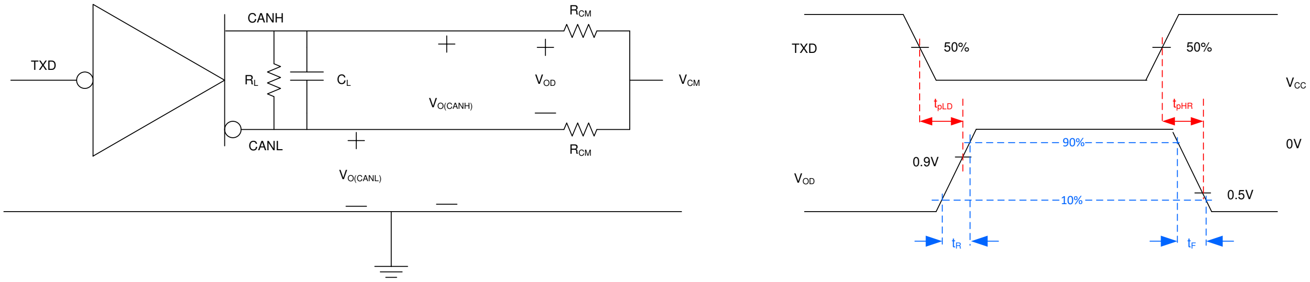


Figure 6-2. Driver Test Circuit and Measurement

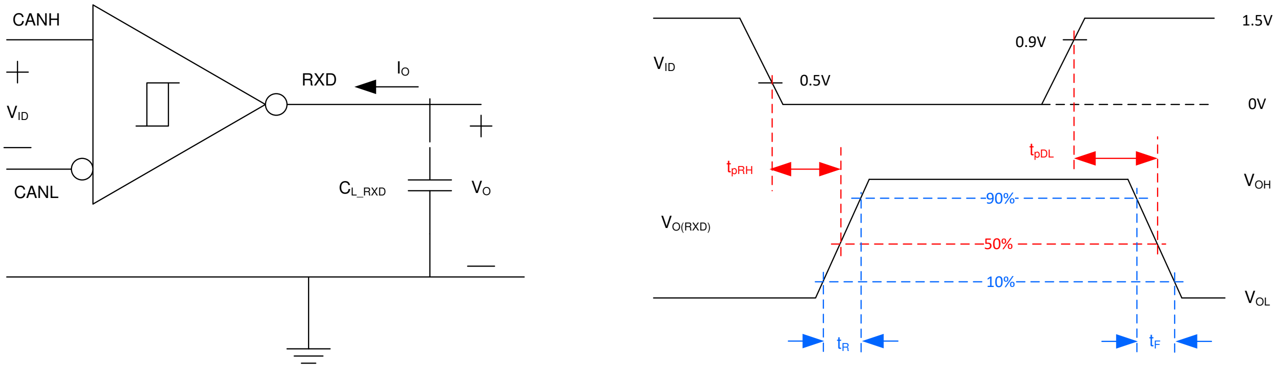


Figure 6-3. Receiver Test Circuit and Measurement

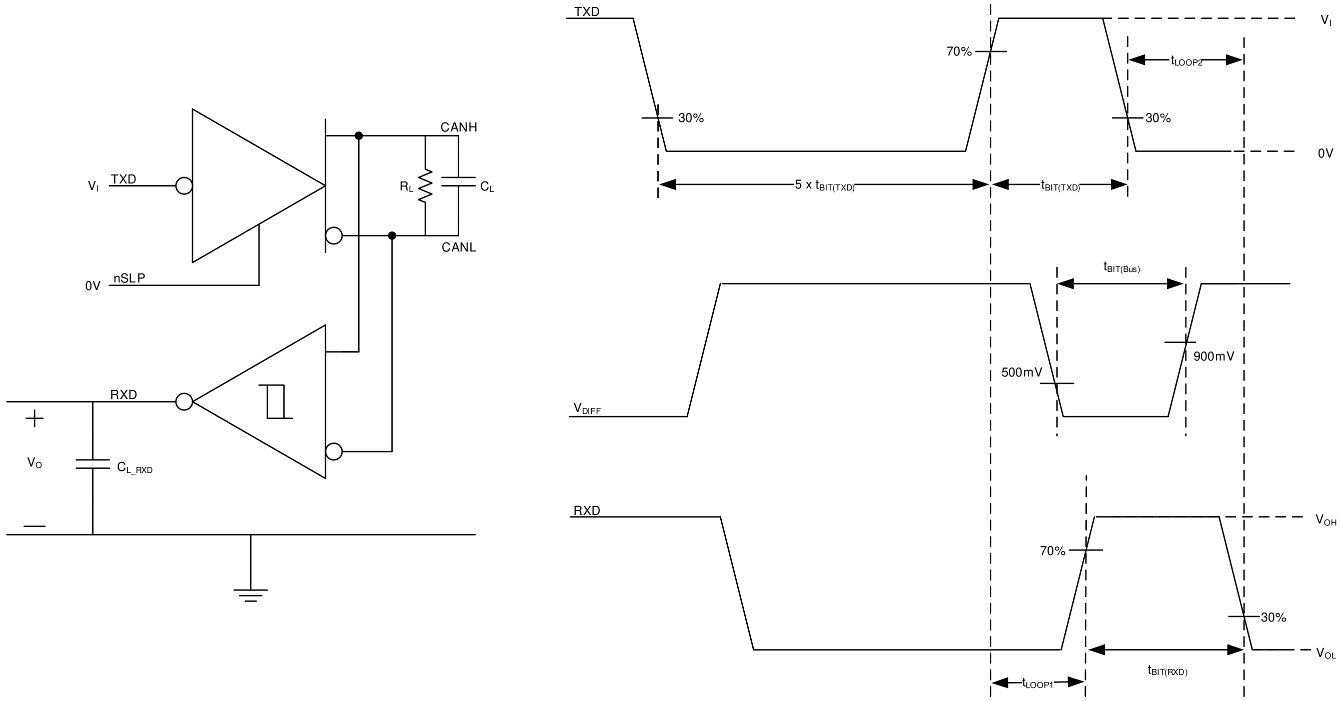


Figure 6-4. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

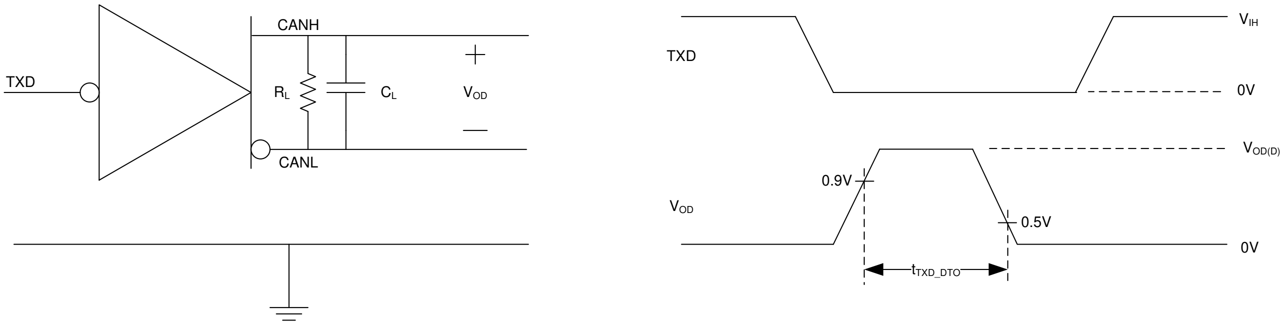


Figure 6-5. TXD Dominant Timeout Test Circuit and Measurement

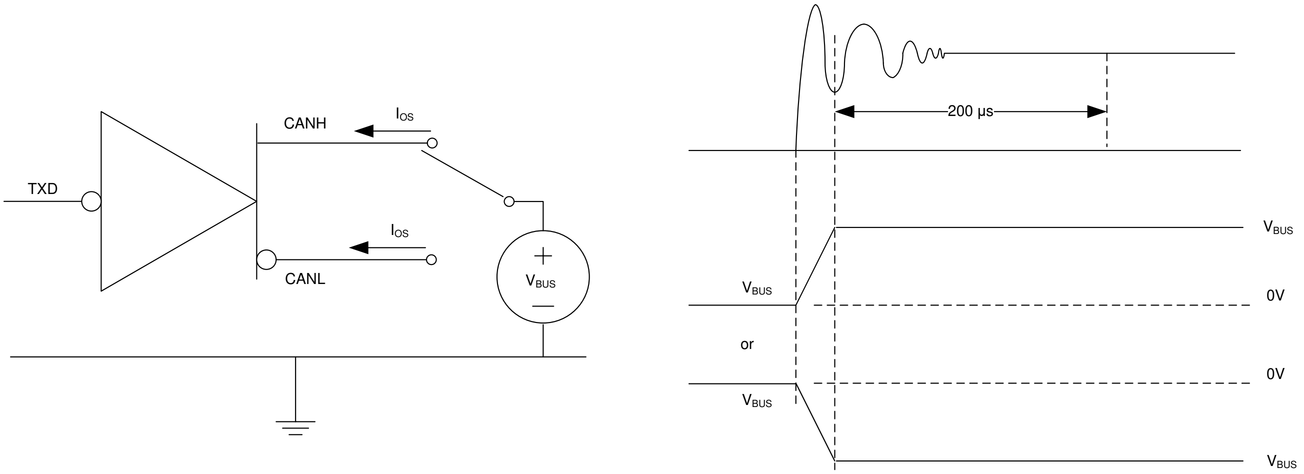


Figure 6-6. Driver Short-Circuit Current Test and Measurement

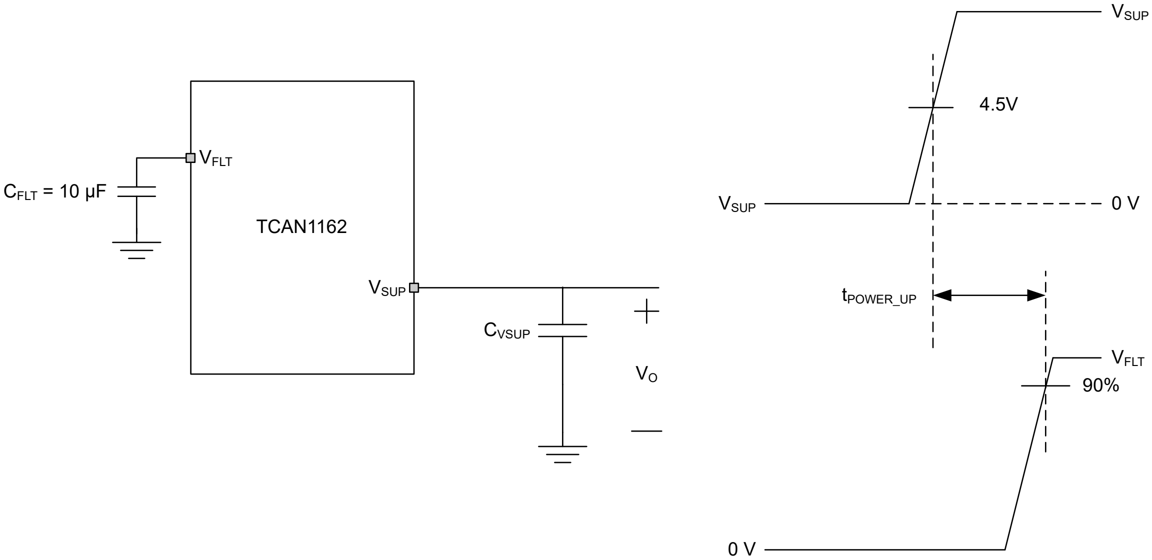


Figure 6-7. t_{POWER_UP} Timing Measurement

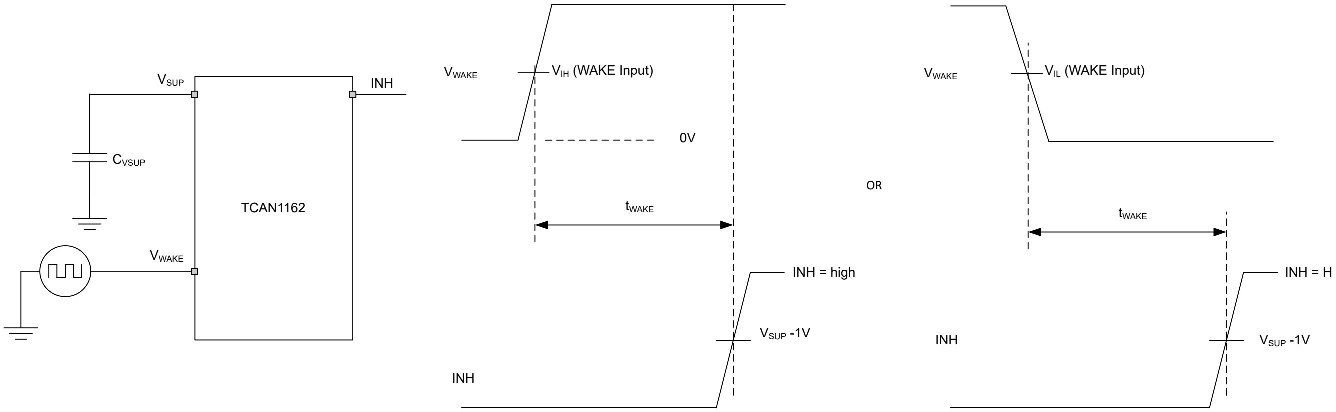


Figure 6-8. t_{WAKE} While Monitoring INH Output

Figure 6-9. Test Signal Definition for Bias Reaction Time Measurement

7 Detailed Description

7.1 Overview

The TCAN1162-Q1 is a high-speed Controller Area Network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2016 high speed CAN specification. The TCAN1162-Q1 supports both classical CAN and CAN FD networks up to 8 megabits per second (Mbps).

The TCAN1162-Q1 integrates a 5V LDO with a wide input operating range which provides the CAN transceiver voltage thereby eliminating the need for the 5V supply to be supplied from an external voltage source.

The TCAN1162-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a system via the INH output pin. This allows an ultra-low-current sleep state where power is gated to all system components except for the TCAN1162-Q1, while monitoring the CAN bus. When a wake-up event is detected, the TCAN1162-Q1 initiates system start-up by driving INH high.

7.2 Functional Block Diagram

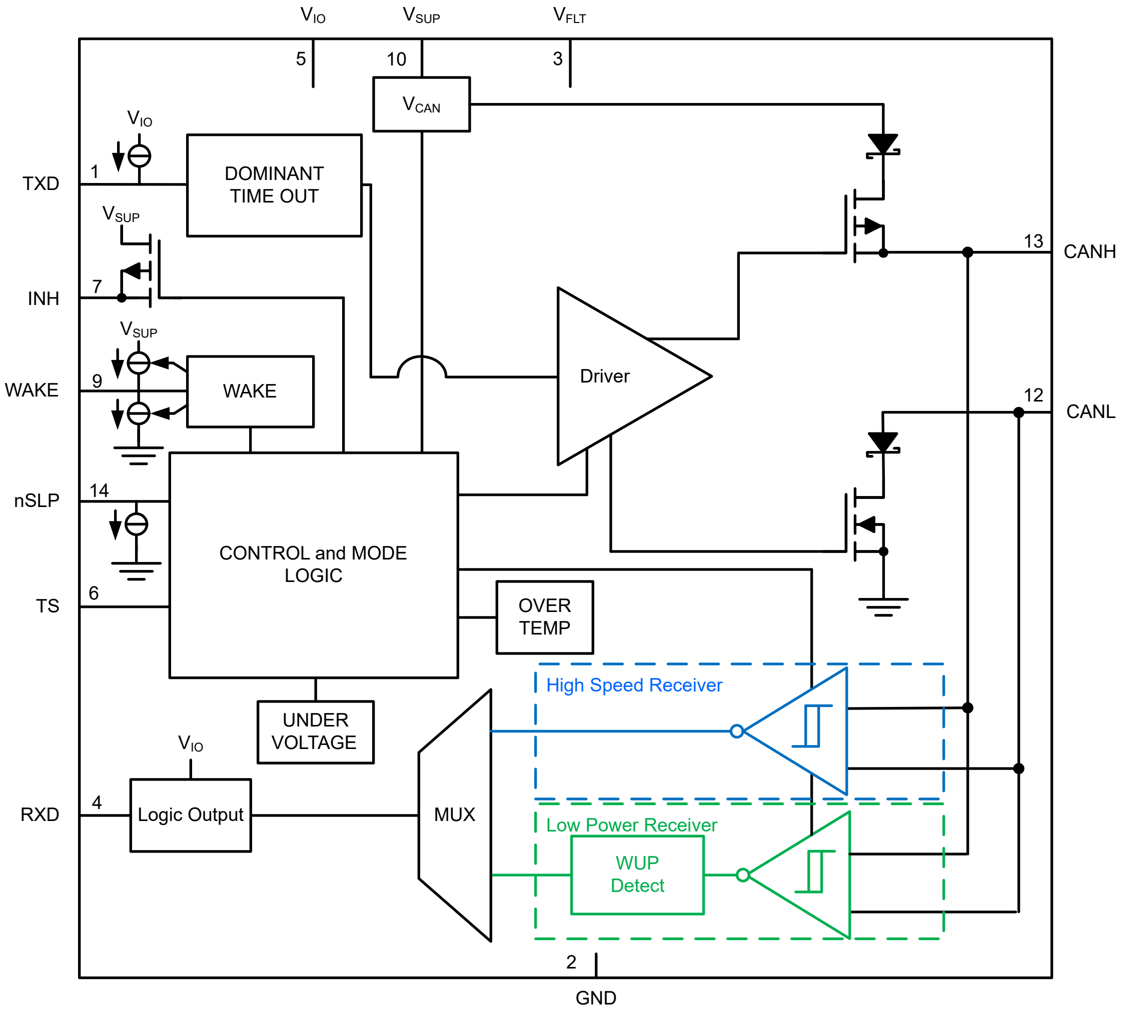


Figure 7-1. TCAN1162-Q1

7.3 Feature Description

7.3.1 V_{SUP} Pin

This pin is connected to the battery supply. It provides the supply to the internal regulators that support the digital core, the CAN transceiver, and the low power CAN receiver.

7.3.2 V_{FLT} Pin

An internal LDO provides power for the integrated CAN transceiver. While in sleep mode the LDO is disabled. Once the device leaves sleep mode and enters other active modes the LDO is enabled for normal operation. This pin requires a 10µF external capacitor as close to the pin as possible.

7.3.3 Digital Inputs and Outputs

The TCAN1162-Q1 has a V_{IO} supply that is used to set the digital input thresholds. The input thresholds are ratio metric to the V_{IO} supply using CMOS input levels, making them scalable for CAN controllers with digital IOs from 1.7V to 5.5V. The TXD input is biased to the V_{IO} level to force a recessive input in case the pin floats. The high-level output voltage for the RXD and TS output pins is driven to the V_{IO} level as logic-high outputs.

7.3.4 Digital Control and Timing

This device is a 14 pin CAN FD transceiver/SBC. Timings are all mixed signal and are covered at the device electrical specification level including the small amounts of control logic for this device. All device mode control is done via one digital input, nSTB or nSLP and through the use of timers and fault conditions internal to the device.

7.3.5 V_{IO} Pin

The V_{IO} pin provides the digital IO voltage to match the controller's IO voltage thus avoiding the requirements for an external level shifter. The integrated level shifter supports voltages from 1.7V to 5.5V providing the widest range of controller support.

7.3.6 GND

GND is the ground pin and it must be connected to the PCB ground.

7.3.7 INH Pin

The TCAN1162-Q1 inhibit (INH) output pin can be used to control the enable of system power management devices allowing for a significant reduction in battery quiescent current consumption while the application is in sleep mode. The INH pin has two states: driven high and high impedance. When the INH pin is driven high the terminal shows V_{SUP} minus a diode voltage drop. In the high impedance state, the output is left floating. The INH pin is high in the normal and standby modes and is low when in sleep mode. A 100kΩ load can be added to the INH output to make sure of a fast transition time from the driven high state to the low state, and to also force the pin low when left floating.

This terminal should be considered a high-voltage logic terminal, not a power output. Thus, should be used to drive the EN terminal of the systems power management device, and not used as a switch for the power management supply. This terminal is not reverse battery protected and thus should not be connected outside the system module.

7.3.8 WAKE Pin

The WAKE pin is a high-voltage reverse-blocked input used for the local wake-up (LWU) function. This function is explained further in Local Wake-Up (LWU) via WAKE Input Terminal section. The pin is defaulted to bi-directional edge trigger, meaning a local wake-up (LWU) is recognize on either a rising or falling edge of WAKE pin transition.

7.3.9 CAN Bus Pins

These are the CAN high and CAN low, CANH and CANL, differential bus pins. These pins are connected to the CAN transceiver and the low-voltage wake receiver.

7.3.10 Local Faults

7.3.10.1 TXD Dominant Timeout (TXD DTO)

While the CAN driver is in active mode a TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time out period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time out constant of the circuit, t_{TXD_DTO}, expires the CAN driver is disabled releasing the bus lines to the recessive level. This keeps the bus free for communication between other nodes on the network. The CAN driver is re-activated on the next dominant to recessive transition on the TXD terminal, thus clearing the dominant time out. The high-speed receiver and RXD terminal will reflect what is on the CAN bus during a TXD DTO fault. The TS terminal in driven low during a TXD DTO fault.

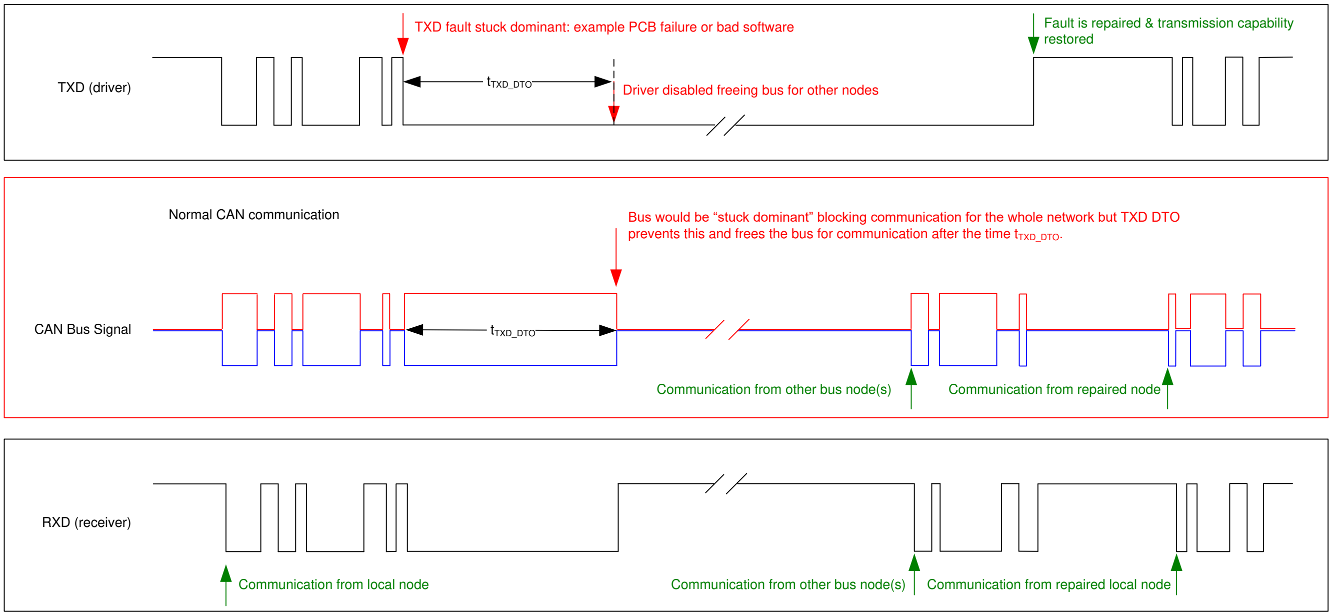


Figure 7-2. Timing Diagram for TXD DTO

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using the minimum t_{TXD_DTO} time and the maximum number of successive dominant bits (11 bits).

$$\text{Minimum Data Rate} = 11\text{ bits} / t_{TXD\_DTO} = 11\text{ bits} / 1.2\text{ ms} = 9.2\text{ kbps} \quad (1)$$

7.3.10.2 Thermal Shutdown (TSD)

If the junction temperature of the TCAN1162-Q1 exceeds the thermal shutdown threshold, $T_J > T_{SDR}$, the device transitions into fail-safe mode and disables the transceiver transmitter and receiver blocking transmission to and from the CAN bus. The TSD fault condition is cleared when the device junction temperature falls below the thermal shutdown temperature threshold, $T_J < T_{SDF}$. If the fault condition that caused the TSD fault is still present, the temperature may rise again and the device enters thermal shutdown again. Prolonged operation with a TSD fault conditions may affect device reliability.

7.3.10.3 Under/Over Voltage Lockout

The supply terminals implement undervoltage and over voltage detection circuitry. If an undervoltage is detected the TCAN1162-Q1 transitions into fail-safe mode.

If the over voltage fault is detected, the TCAN1162-Q1 transitions into fail-safe mode. These mode changes place the device in a known state which protect the system from unintended behavior.

7.3.10.4 Unpowered Devices

The device is designed to be a passive or no load to the CAN bus if the device is unpowered. The CANH and CANL pins have low leakage currents when the device is un-powered, so the pins present no load to the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation.

The logic terminals also have low leakage currents when the device is un-powered, so the terminals do not load down other circuits which may remain powered.

7.3.10.5 Floating Terminals

The TCAN1162-Q1 has internal pull-ups and pull-downs on critical pins to ensure a known operating behavior if the pins are left floating.

The TXD pin is pulled up to V_{IO} which forces a recessive level if the pin floats. This internal bias should not be relied upon by design but rather a fall-safe option. Special care needs to be taken when the device is used with a CAN controller that has open drain outputs. The device implements a weak internal pull-up resistor on the TXD pin. The CAN bit timing for CAN FD data rates will require special consideration and the pull-up strength should be considered carefully when using open drain outputs. An adequate external pull-up resistor must be used to make sure the TXD output of the CAN controller maintains adequate bit timing input to the CAN device.

The nSLP pin is weakly pulled down which forces the device into the low-power sleep mode if the terminal is left floating. See Table 7-1.

Table 7-1. Terminal Fail-Safe Biasing

TERMINAL	PULL-UP or PULL-DOWN	COMMENT
TXD	Pull-up	Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering
nSLP	Pull-down	Weakly biases the nSLP terminal towards low power sleep mode to prevent excessive system power

7.3.10.6 CAN Bus Short Circuit Current Limiting

The TCAN1162-Q1 has several protection features that limit the short circuit current during dominant and recessive when a CAN bus line is shorted. The device has TXD dominant state timeout which prevents permanently having a higher short circuit current during a dominant state fault.

During CAN communication the bus switches between the dominant and recessive states, thus the short circuit current may be viewed either as the current during each bus state or as a DC average current. The average short circuit current should be used when considering system power for the termination resistors and common mode choke. The percentage dominant is limited by the TXD dominant state timeout and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and interframe space. These ensure that there is a minimum recessive time on the bus even if the data field contains a high percentage of dominant bits.

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using Equation 2.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times I_{OS(SS)\_REC}) + (\%DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%Receive \times I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages

- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current

The short circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance and other network components.

7.3.10.7 Sleep Wake Error Timer

The sleep wake error (SWE) timer, $t_{INACTIVE}$, is a timer used to determine if specific external and internal functions are working. The SWE timer starts when the device enters standby mode and only runs in standby mode. A mode transition stops the timer. If the timer times out while the device is in standby mode the RXD pin will be pulled low to indicate an interrupt. The TCAN1162-Q1 will then transition to sleep mode.

7.4 Device Functional Modes

The TCAN1162-Q1 has five modes: normal, standby, sleep, fail-safe, and off mode. Operating mode selection is made via the nSLP input terminal in conjunction with supply conditions, temperature conditions, and wake events.

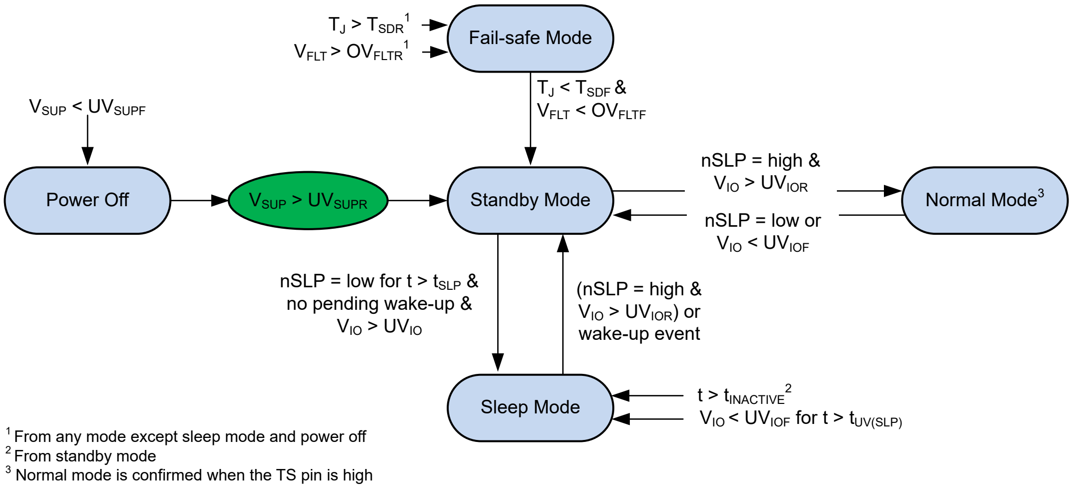


Figure 7-3. TCAN1162 State Machine

Table 7-2. Mode Overview

Block	Normal	Standby	Sleep	Fail-Safe
V_{FLT}	On	On/Off(1) (2)	Off	Off
INH	On	Active	Off	Off
Low Power CAN RX	Off	Active	Active	Active
RXD	V_{IO}	V_{IO}	High impedance(3)	V_{IO}

(1) V_{FLT} is switched on in standby mode if nSLP is pulled high enabling normal mode.
(2) V_{FLT} is switched on in standby mode if a valid WUP is detected on the CAN bus. If the nSTB pin is not pulled high within the timeout for bus inactivity window timer ($t_{(silence)}$) V_{FLT} is switched off again.
(3) V_{IO} if V_{IO} is present.

7.4.1 Operating Mode Description

7.4.1.1 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. The $t_{INACTIVE}$ timer in not active in normal mode.

7.4.1.2 Standby Mode

Standby mode is a low power mode of the TCAN1162-Q1 where the CAN transceiver is placed in the CAN autonomous inactive state by asserting the nSLP pin low. In this mode the TS pin is driven low, the CAN transmitter and receiver are switched off, the bus pins are biased to ground, and the transceiver cannot send or receive data. While in standby mode the low power receiver actively monitors the CAN bus for a valid wake-up pattern. If a valid wake-up pattern is received, the CAN bus pins transition to the CAN autonomous active state where CANH and CANL are internally biased to 2.5V from the V_{SUP} power rail. The reception of a valid wake-up pattern generates a wake-up request by the CAN transceiver by latching the RXD output pin low. The WAKE pin circuitry is active in standby mode and monitors the WAKE pin for either a high-to-low or low-to-high transition. The INH pin is active to supply an enable to the system power supply.

The RXD output pin is asserted low while in standby mode if a wake event or a fault is detected. Note that a POR counts as a wake event and will also cause RXD to latch low.

The internal CAN regulator, V_{FLT}, is switched on in standby mode if a valid CAN wake-up event is detected by the TCAN1162-Q1. If the nSLP pin does not toggle high before the $t_{SILENCE}$ timer expires, then V_{FLT} is switched off again.

In standby mode a fail-safe timer, $t_{INACTIVE}$, is enabled. The $t_{INACTIVE}$ timer adds an additional layer of protection by requiring the system controller to configure the TCAN1162-Q1 to normal mode before the timer expires. This feature forces the TCAN1162-Q1 to transition to its lowest power mode, sleep mode, if the processor does not come up properly.

Standby mode is not the lowest power mode of the device though since the INH terminal is active. This allows the rest of the system to operate normally.

7.4.1.3 Sleep Mode

Sleep mode is the lowest power mode of the TCAN1162-Q1 where the CAN transceiver is placed in the CAN autonomous inactive state by asserting the nSLP pin low for $t > t_{SLP}$. In sleep mode, the CAN transmitter and receiver are switched off, the bus pins are biased to ground after $t_{SILENCE}$ expires, and the transceiver cannot send or receive data. The INH pin is switched off in sleep mode causing any system power elements controlled by INH to be switched off thus reducing system power consumption. While in sleep mode, the low power receiver actively monitors the CAN bus for a valid wake-up pattern and the I_{SUP} current is reduced to its minimum level.

Sleep mode is entered if:

- The nSLP pin is asserted low for $t > t_{SLP}$, there are no pending wake-up events, and $V_{IO} > UV_{VIOR}$
- $V_{IO} < UV_{VIOR}$ for $t > t_{UV(SLP)}$
- SWE timer expires (see Sleep Wake Error Timer)

Sleep mode is exited if:

- $V_{IO} > UV_{VIOR}$ and nSLP = high
- If a valid wake-up pattern (WUP) is received via the CAN bus pins
- A local WAKE (LWU) event
- A reset event occurs (goes to reset mode)

7.4.1.3.1 Remote Wake Request via Wake-Up Pattern (WUP)

The TCAN1162-Q1 implements a low-power wake receiver in the standby and sleep mode that uses the multiple filtered dominant wake-up pattern (WUP) defined in the ISO11898-2:2016 standard.

The wake-up pattern (WUP) consists of a filtered dominant bus, then a filtered recessive bus time followed by a second filtered bus time. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive, other bus traffic does not reset the bus monitor. Once a filtered recessive is received, the bus monitor is now waiting on a filtered dominant. The other bus traffic does not reset the bus monitor. Immediately upon receiving of the second filtered dominant, the bus monitor recognizes the WUP and drives the RXD terminal low, if a valid V_{IO} is present signaling to the controller the wake-up request. If a valid V_{IO} is not present when the wake-up pattern is received the device drives the RXD output pin low once $V_{IO} > UV_{IOR}$.

The WUP consists of:

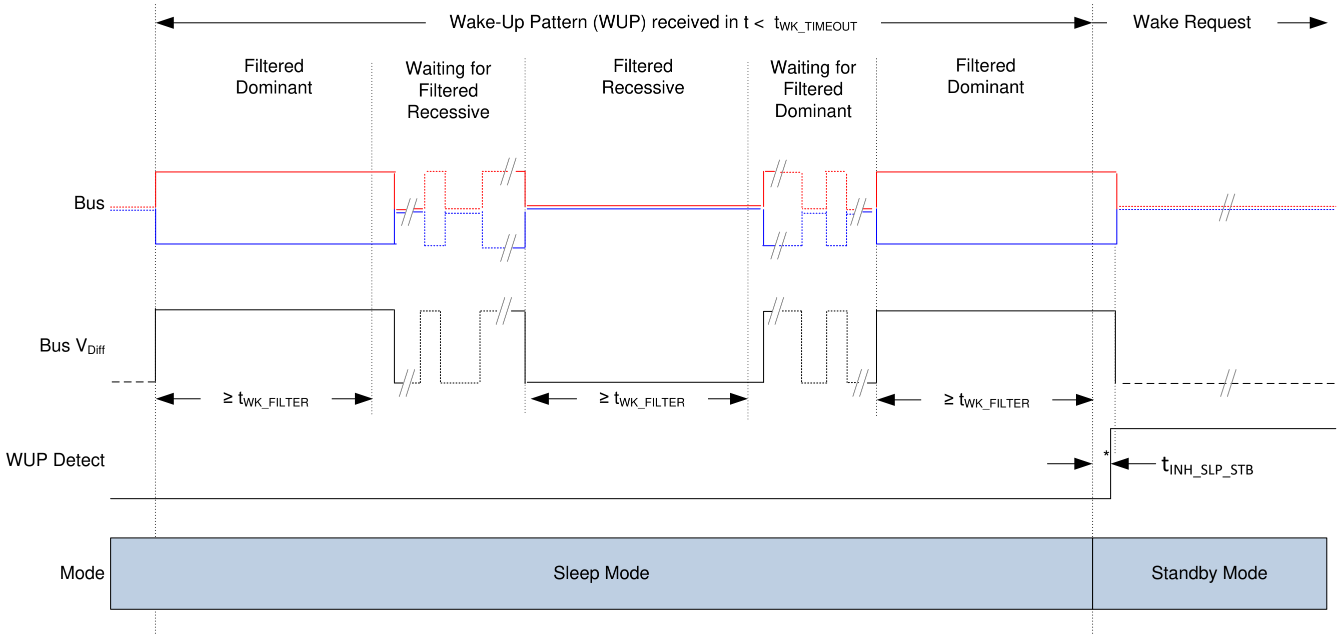
- A filtered dominant bus of at least t_{WK_FILTER} followed by
- A filtered recessive bus time of at least t_{WK_FILTER} followed by
- A second filtered dominant bus time of at least t_{WK_FILTER}

For a dominant or recessive to be considered “filtered”, the bus must be in that state for more than t_{WK_FILTER} time. Due to variability in the t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP, and thus no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP, and a wake request may be generated. Bus state times more than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP, and thus, a wake request is generated. See Figure 7-4 for the timing diagram of the WUP.

The pattern and t_{WK_FILTER} time used for the WUP and wake request prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a wake request.

ISO11898-2:2016 has two sets of times for a short and long wake-up filter times. The t_{WK_FILTER} timing for the TCAN1162-Q1 has been picked to be within the min and max values of both filter ranges. This timing has been chosen such that a single bit time at 500 kbps, or two back to back bit times at 1Mbps triggers the filter in either bus state.

For an additional layer of robustness and to prevent false wake-ups, the device implements the $t_{WK\_TIMEOUT}$ timer. For a remote wake-up event to successfully occur, the entire wake-up pattern must be received within the timeout value. If a full wake-up pattern is not received before the $t_{WK\_TIMEOUT}$ expires, then the internal logic is reset and the device remains in sleep mode without waking up. The full pattern must then be transmitted again within the $t_{WK\_TIMEOUT}$ window. See Figure 7-4.



*The RXD pin is only driven once V_{IO} is present.

Figure 7-4. Wake-Up Pattern (WUP) From Sleep Mode To Standby Mode

7.4.1.3.2 Local Wake-Up (LWU) via WAKE Input Terminal

The WAKE terminal is a bi-directional high-voltage reverse battery protected input which can be used for local wake-up (LWU) requests via a voltage transition. A LWU event is triggered on either a low-to-high or high-to-low transition since it has bi-directional input thresholds. The WAKE pin could be used with a switch to V_{SUP} or to ground. If the terminal is unused, it should be pulled to V_{SUP} or ground to avoid unwanted parasitic wake-up events.

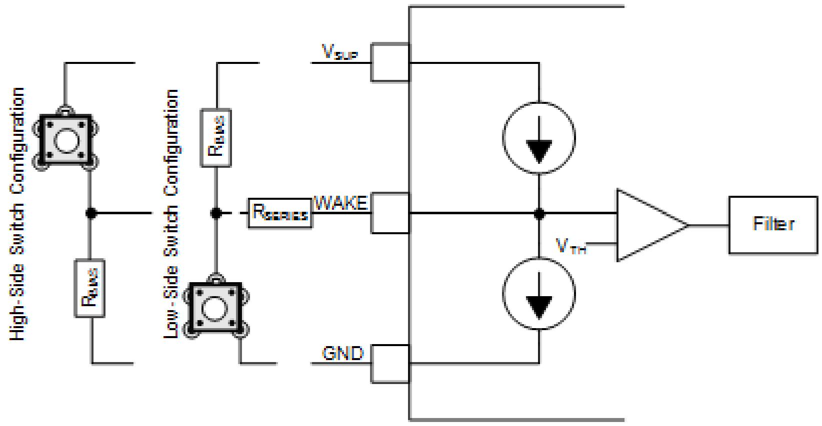


Figure 7-5. WAKE Circuit Example

Figure 7-5 shows two possible configurations for the WAKE pin, a low-side and high-side switch configuration. The objective of the series resistor, R_{SERIES}, is to protect the WAKE input of the device from over current conditions that may occur in the event of a ground shift or ground loss. The minimum value of R_{SERIES} can be calculated using the maximum supply voltage, V_{SUPMAX}, and the maximum allowable current of the WAKE pin, $I_{IO(WAKE)}$. R_{SERIES} is calculated using:

$$R_{SERIES} = V_{SUPMAX} / I_{IO(WAKE)} \tag{3}$$

If the battery voltage never exceeds 42 V_{DC}, then the R_{SERIES} value is approximately 10kΩ.

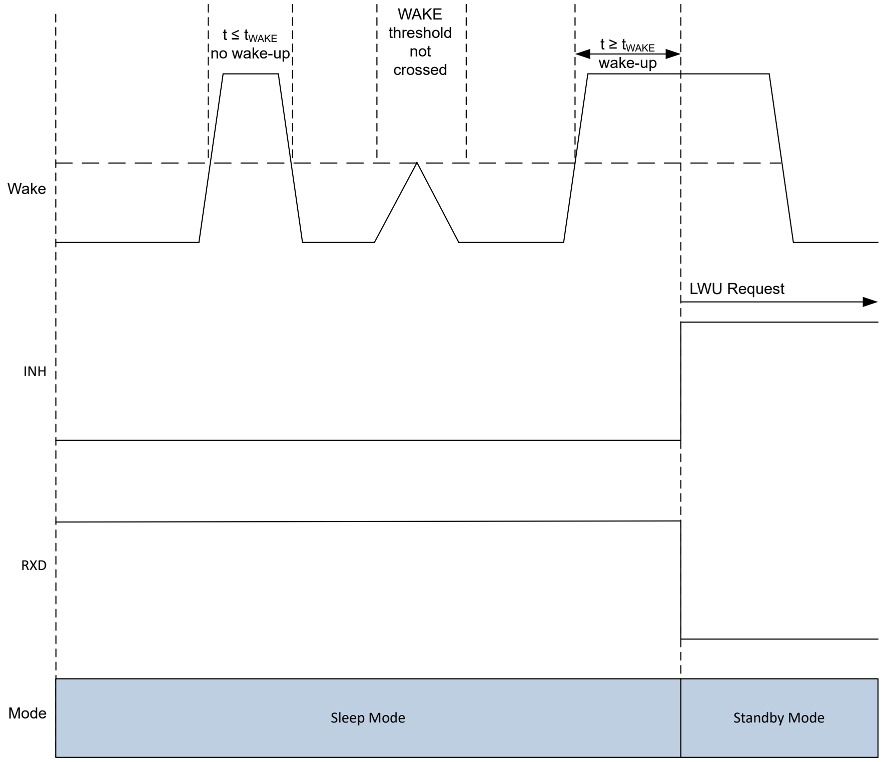
The R_{BIAS} resistor is used to set the static voltage level of the WAKE input when the switch is not in use. When the switch is in use in a high-side switch configuration, the R_{BIAS} resistor in combination with the R_{SERIES} resistor sets the WAKE pin voltage above the V_{IH} threshold. The maximum value of R_{BIAS} can be calculated using the maximum supply voltage, V_{SUPMAX}, the maximum WAKE threshold voltage V_{IH}, the maximum WAKE input current I_{IH} and the series resistor value R_{SERIES}. R_{BIAS} is calculated using:

$$R_{BIAS} < ((V_{SUPMAX} - V_{IH}) / I_{IH}) - R_{SERIES} \tag{4}$$

If the battery voltage never exceeds $42V_{DC}$, then the R_{BIAS} resistor value must be less than 650kΩ.

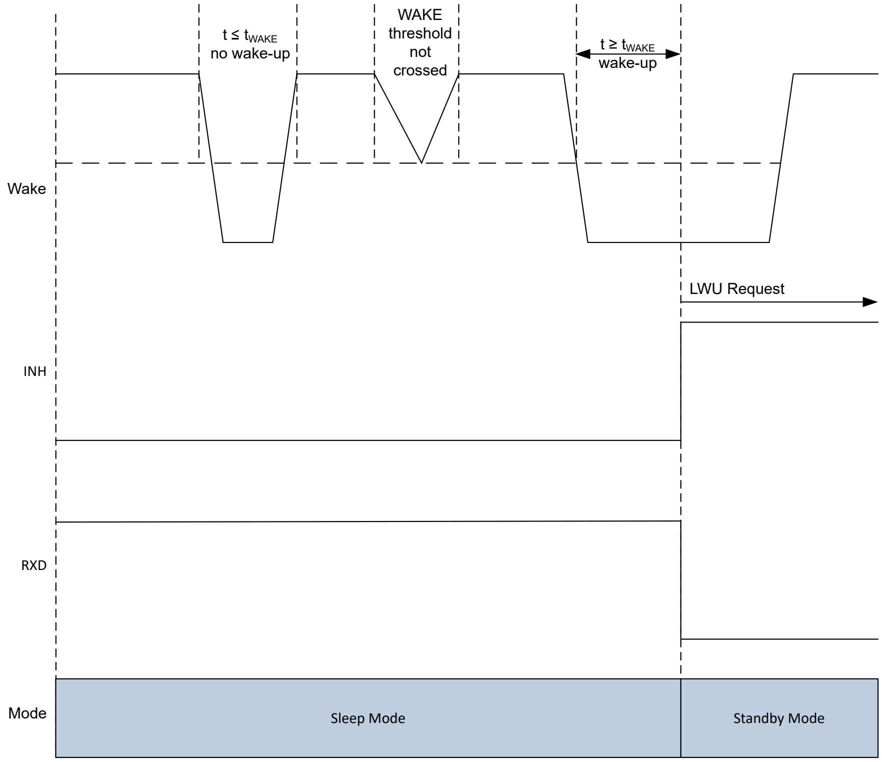
The LWU circuitry is active in sleep mode. If a valid LWU event occurs, the TCAN1162-Q1 transitions from sleep mode to standby mode.

The WAKE circuitry is switched off normal mode.



The RXD pin is only driven once V_{IO} is present.

Figure 7-6. LWU Request Rising Edge



The RXD pin is only driven once V_{IO} is present.

Figure 7-7. LWU Request Falling Edge

7.4.1.4 Fail-safe Mode

Fail-safe mode is a low power mode in which the TCAN1162-Q1 is in a protected state. While in fail-safe mode the internal regulator (V_{FLT}) is off, the INH pin is off, and the CAN transmitter and receiver are off.

Fail-safe mode is entered if:

- $T_J > T_{SDR}$
- $V_{VFLT} > OV_{FLTR}$

Fail-safe mode is exited if all of the following criteria are met:

- $T_J < T_{SDF}$
- $V_{VFLT} < OV_{FLTF}$
- A valid wake-up event exists

If the fault condition is not cleared within $t_{INACTIVE}$, then the device transitions into the lowest power mode, sleep mode.

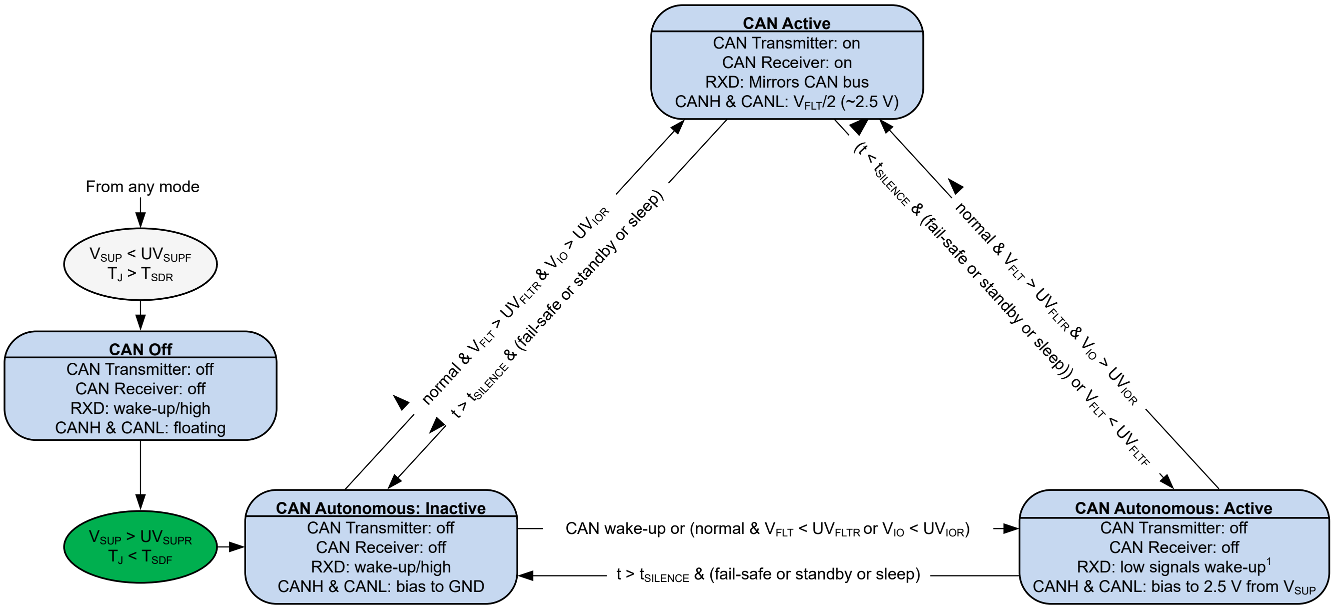
7.4.2 CAN Transceiver

7.4.2.1 CAN Transceiver Operation

The TCAN1162-Q1 CAN transverse has three modes of operation; CAN active, CAN autonomous active, and CAN autonomous inactive.

7.4.2.2 CAN Transceiver Modes

The TCAN1162-Q1 supports the ISO 11898-2:2016 CAN physical layer standard autonomous bus biasing scheme. Autonomous bus biasing enables the transceiver to switch between CAN active, CAN autonomous active, and CAN autonomous inactive which helps to reduce RF emissions.



[1] Wake-up inactive in normal mode

Figure 7-8. TCAN1162 CAN Transceiver State Machine

7.4.2.2.1 CAN Off Mode

In CAN off mode, the CAN transceiver is switched off and the CAN bus lines are truly floating. In this mode, the device presents no load to the CAN bus while preventing reverse currents from flowing into the device if the battery or ground connection is lost.

The CAN off state is entered if:

- $T_J > T_{SDR}$
- $V_{SUP} < UV_{SUPF}$

The CAN transceiver switches between the CAN off state and CAN autonomous inactive mode if:

- $V_{SUP} > UV_{SUPR}$
- $T_J < T_{SDF}$

7.4.2.2.2 CAN Autonomous: Inactive and Active

When the CAN transceiver is in standby mode or sleep mode the CAN bias circuit is switched off and the transceiver moves to the autonomous inactive state. In the autonomous inactive state the CAN pins are biased to GND. When a valid wake-up event occurs the CAN bus is biased to 2.5V. If the controller does not transition the TCAN1162-Q1 into normal mode before the $t_{SILENCE}$ timer expires, then the CAN biasing circuit is again switched off and the CAN pins are biased to ground.

The CAN transceiver switches to the CAN autonomous mode if any of the following conditions are met:

- The TCAN1162-Q1 transitions from CAN off mode to CAN autonomous inactive

- The TCAN1162-Q1 transitions from normal mode to standby mode or fail-safe mode or sleep mode and $t < t_{SILENCE}$
- $t > t_{SILENCE}$ and the TCAN1162-Q1 transitions from normal mode to standby mode or fail-safe mode or sleep mode

The CAN transceiver switches between the CAN autonomous inactive mode and CAN autonomous active mode if:

- A valid wake-up event
- The TCAN1162-Q1 transitions to normal mode and no undervoltage faults exist.

The CAN transceiver switches between the CAN autonomous active mode and CAN autonomous inactive mode if:

- $t > t_{SILENCE}$ and the TCAN1162-Q1 transitions to standby mode, sleep mode, or fail-safe mode.

7.4.2.2.3 CAN Active

When the TCAN1162-Q1 is in normal mode the CAN transceiver is in active mode. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The CAN bias voltage in CAN active mode is derived from:

- V_{FLT}

The CAN transceiver switches between the CAN autonomous inactive or active mode and CAN active mode if:

- The TCAN1162-Q1 transitions to normal mode and no undervoltage faults exist.

The CAN transceiver blocks its transmitter and receiver after entering CAN active mode if the TXD pin is asserted low before leaving standby mode. This prevents disruptions to CAN bus in the event that the TXD pin has a TXD DTO fault.

7.4.2.3 Driver and Receiver Function Tables

Table 7-3. Driver Function Table

DEVICE MODE	TXD INPUTS(1)	BUS OUTPUTS		DRIVEN BUS STATE(2)
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or Open	High impedance	High impedance	$V_{FLT}/2$
Standby	x	High impedance	High impedance	Biased to GND
Sleep	x	High impedance	High impedance	Biased to GND

(1) x = irrelevant
(2) For bus states and typical bus voltages see Figure 7-9

Table 7-4. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} – V_{CANL}$	BUS STATE	RXD TERMINAL
Normal	$V_{ID} \geq 0.9V$	Dominant	Low
	$0.5\ V < V_{ID} < 0.9V$	Indeterminate	Indeterminate
	$V_{ID} \leq 0.5V$	Recessive	High
	Open ($V_{ID} \approx 0V$)	Open	High
Standby	$V_{ID} \geq 1.15V$	Dominant	High Low if wake-up event persists
	$0.5\ V < V_{ID} < 1.15V$	Indeterminate	
	$V_{ID} \leq 0.4V$	Recessive	
	Open ($V_{ID} \approx 0V$)	Open	

Table 7-4. Receiver Function Table (continued)

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD TERMINAL
Sleep	$V_{ID} \geq 1.15V$	Dominant	High Low if wake-up event persists and V_{IO} is present. Tri-state if V_{IO} or V_{SUP} are not present
	$0.4V < V_{ID} < 1.15V$	Indeterminate	
	$V_{ID} \leq 0.4V$	Recessive	
	Open ($V_{ID} \approx 0V$)	Open	

7.4.2.4 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 7-9.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to one half of the CAN transceiver supply voltage via the high resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the CAN bus will be greater than the differential voltage of a single CAN driver. The TCAN1162-Q1 CAN transceiver implements low-power standby and sleep modes which enables a third bus state where the bus pins are biased to ground via the high resistance internal resistors of the receiver.

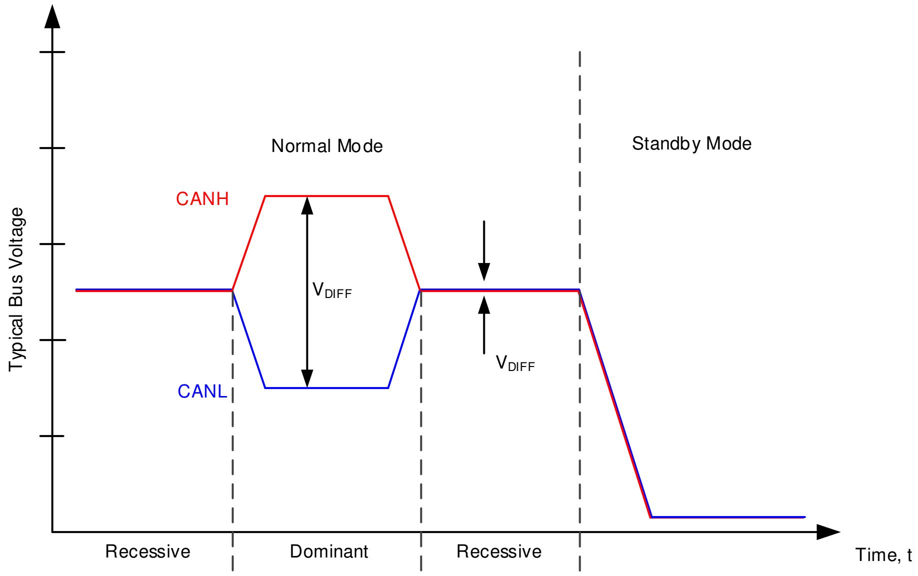


Figure 7-9. Bus States

8 Application Information

8.1 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.2 Typical Application

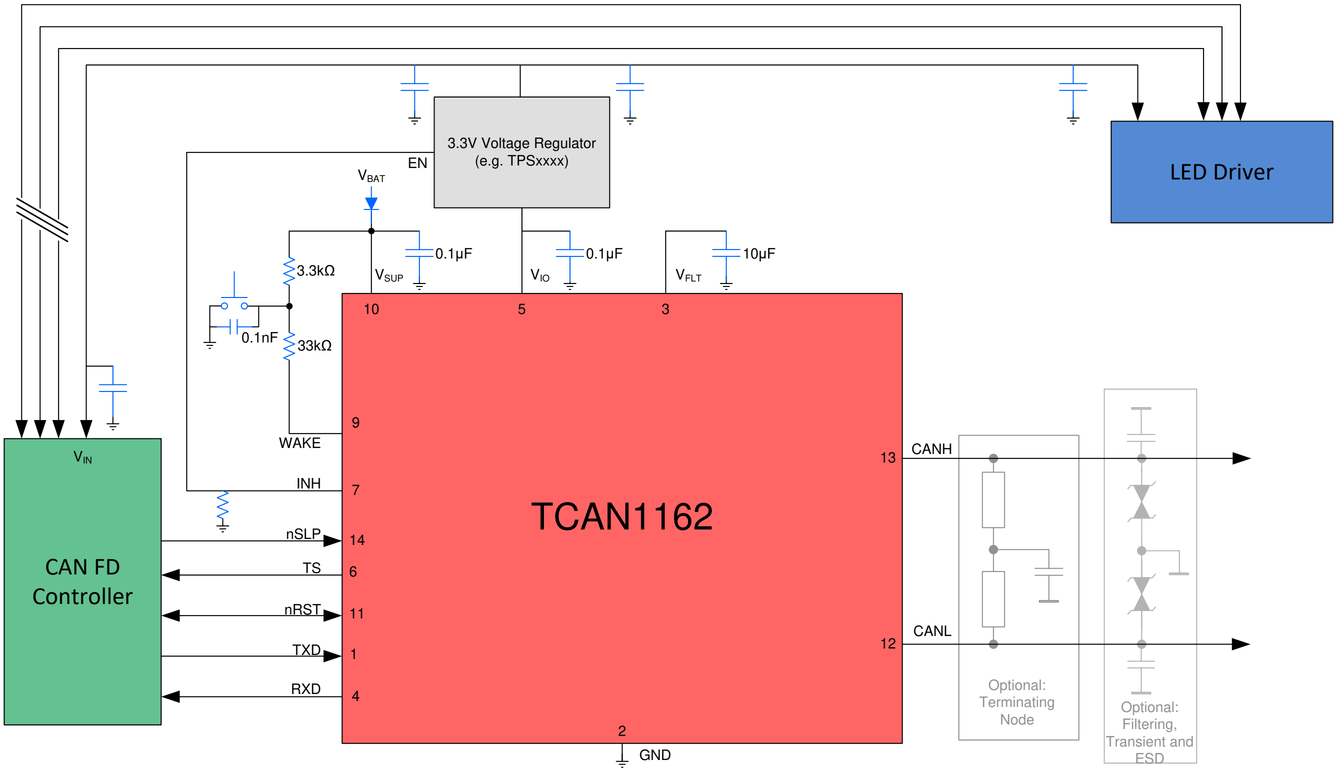


Figure 8-1. Typical Application

8.2.1 Design Requirements

8.2.1.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1162-Q1

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification, the driver differential output is specified with a bus load that can range from 50Ω to 65Ω where the differential output must be greater than 1.5V. The TCAN1162-Q1 is specified to meet the 1.5V requirement down to 50Ω and is specified to meet 1.4V differential output at 45Ω bus load. The differential input resistance of the TCAN1162-Q1 is a minimum of 4kΩ. If 100 TCAN1162-Q1 devices are in parallel on a bus, this is equivalent to a 400Ω differential load in parallel with the nominal 60Ω bus termination which gives a total bus load of approximately 52Ω. Therefore, the TCAN1162-Q1 theoretically supports over 100 devices on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

The flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using the flexibility, the CAN network system designer must take the responsibility of good network design for a robust network operation.

8.2.2 Detailed Design Procedures

8.2.2.1 CAN Termination

Termination may be a single 120Ω resistor at the end of the bus on either the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used, see Figure 8-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

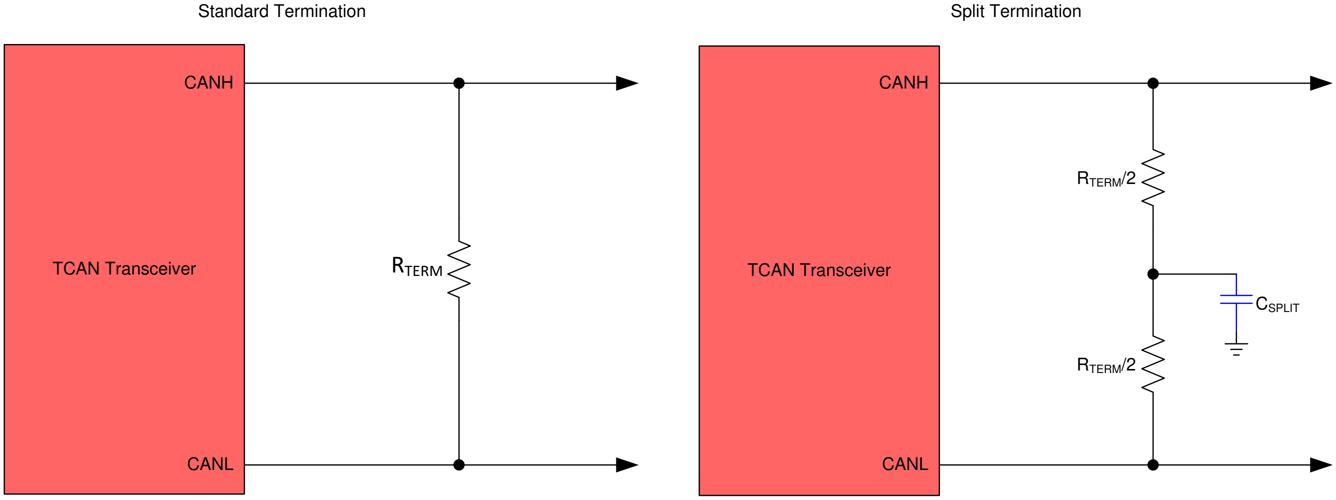


Figure 8-2. CAN Bus Termination Concepts

8.3 Application Curves

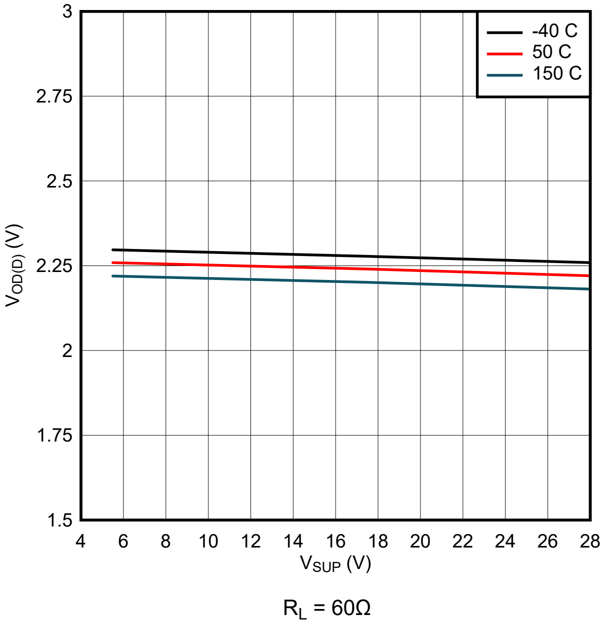


Figure 8-3. $V_{OD(D)}$ over V_{SUP}

8.4 Power Supply Requirements

The TCAN1162-Q1 is designed to operate from a V_{SUP} input supply voltage range between 5.5V and 28V. The TCAN1162-Q1 also has an output level shifting supply input, V_{IO}, designed for a range between 1.7V and 5.5V. Input supplies must be well regulated. A bypass capacitance, typically 100nF, should be placed close to the device V_{SUP} and V_{IO} supply pins. This helps to reduce supply voltage ripple present on the outputs of the switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes and traces.

8.5 Layout

8.5.1 Layout Guidelines

Place the protection and filtering circuitry as close to the bus connector to prevent transients, ESD and noise from propagating onto the board. The layout example provides information on components around the device itself. Transient voltage suppression (TVS) device can be added for extra protection. The production solution can be either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Use supply and ground planes to provide low inductance.

Note

A high-frequency current follows the path of least impedance and not the path of least resistance.

Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver.
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors with the center or split tap of the termination connected to ground via capacitor. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to make sure the terminating node is not removed from the bus, thus removing the termination.

8.5.2 Layout Example

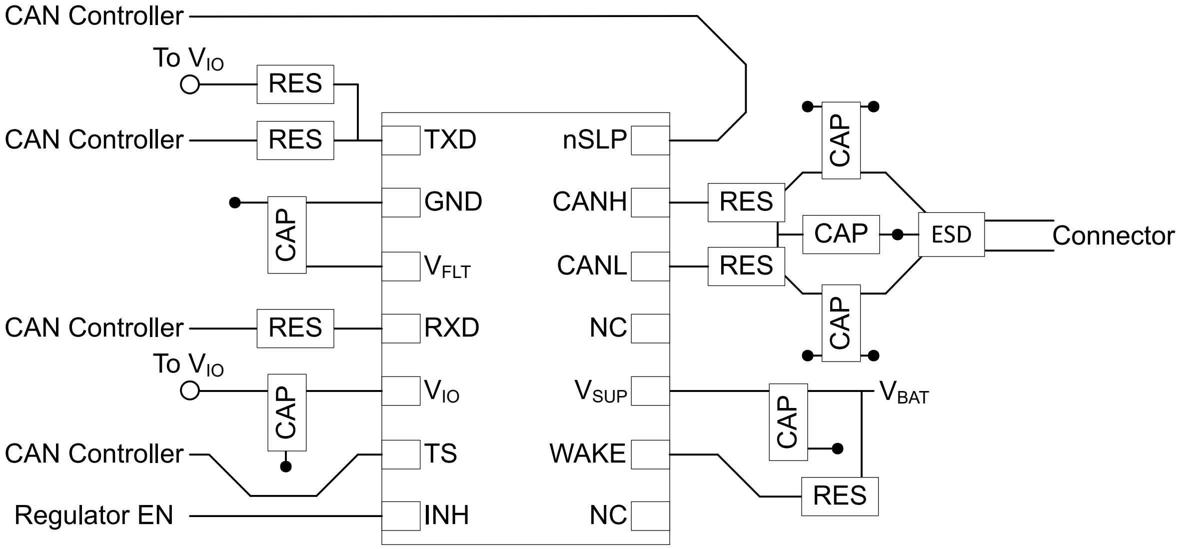


Figure 8-4. TCAN1162 Example Layout

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December2021) to Revision B (July 2025) **Page**

- Changed the Device Information table to the *Package Information* table.. 1
- Changed INH to an open drain output in Figure 7-1 15

Changes from Revision * (May 2021) to Revision A (December 2021) **Page**

- Changed the document status from *Advanced Information* to *Production* data... 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1162DMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1162
TCAN1162DMTRQ1.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1162

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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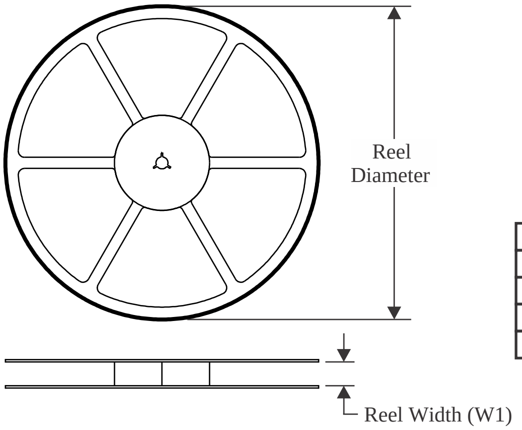
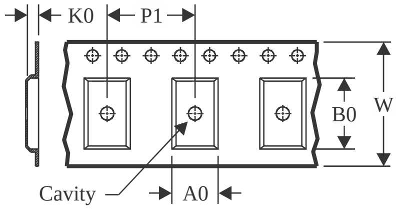
TAPE AND REEL INFORMATION

REEL DIMENSIONS

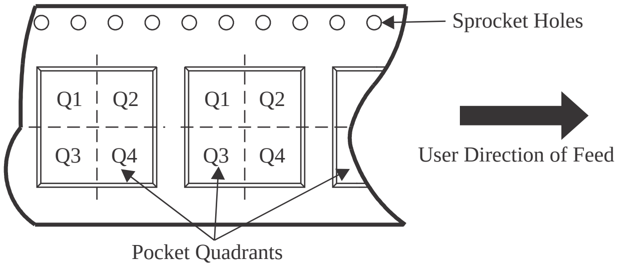


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

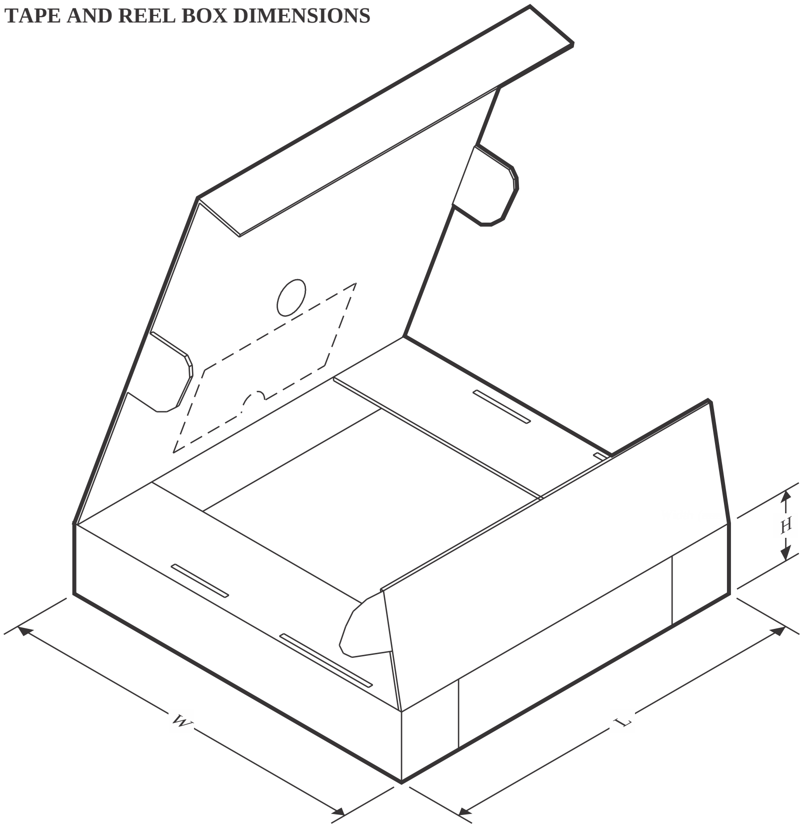
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1162DMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1162DMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

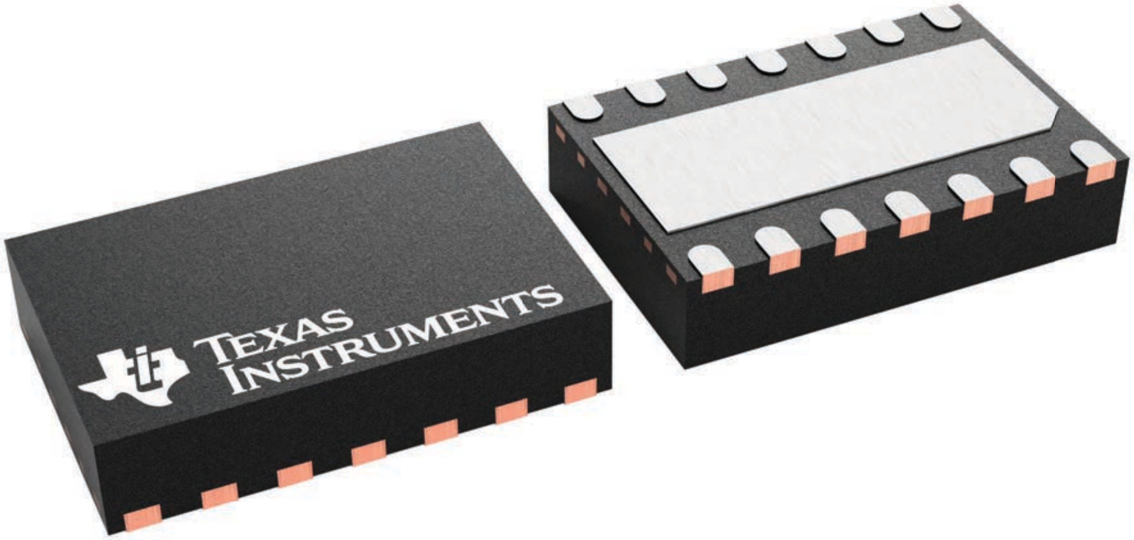
DMT 14

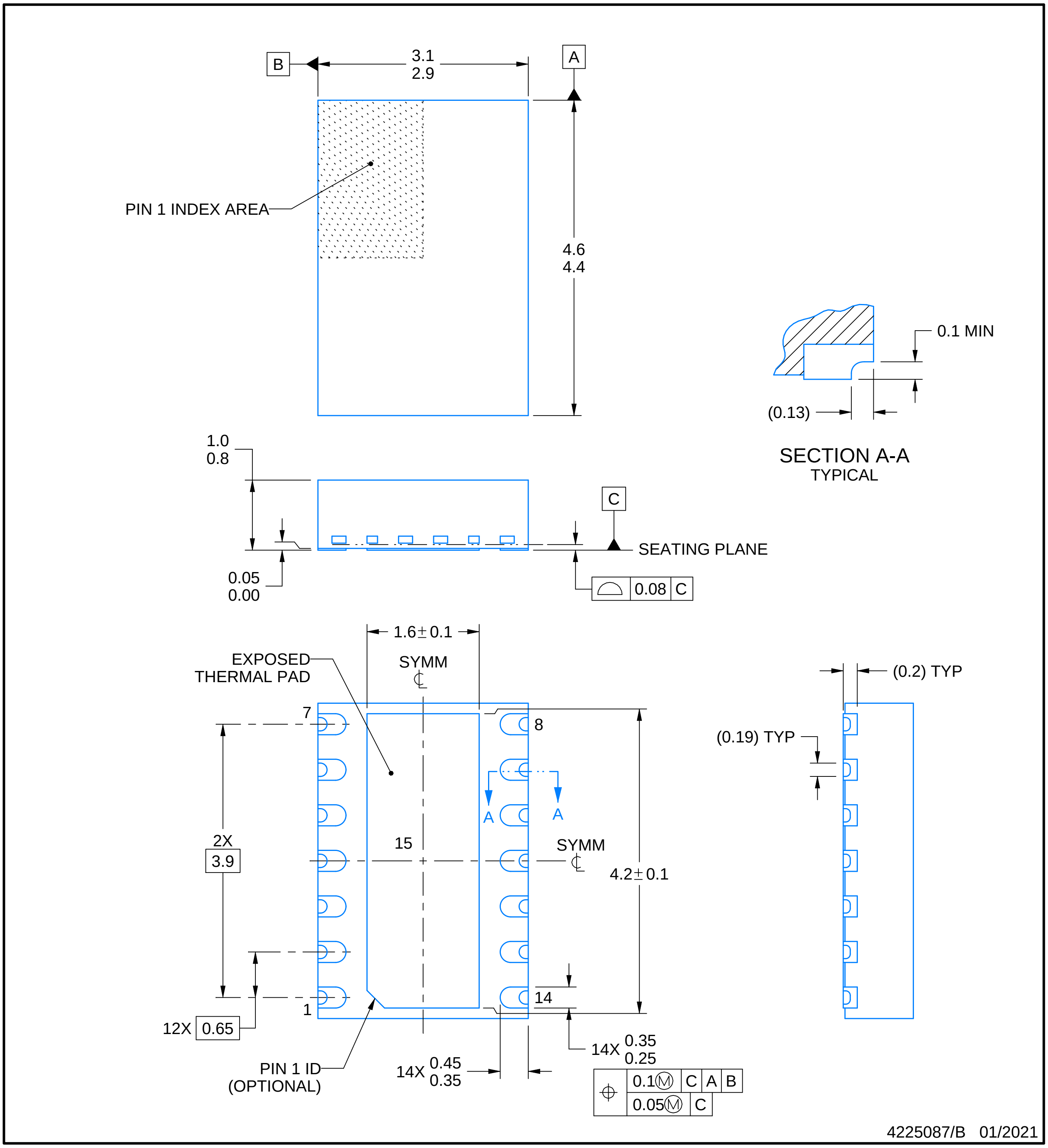
VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

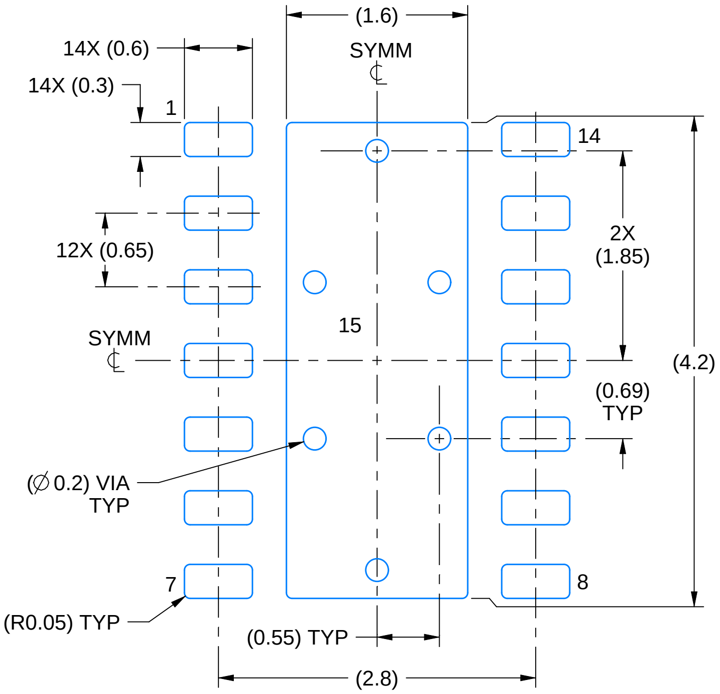




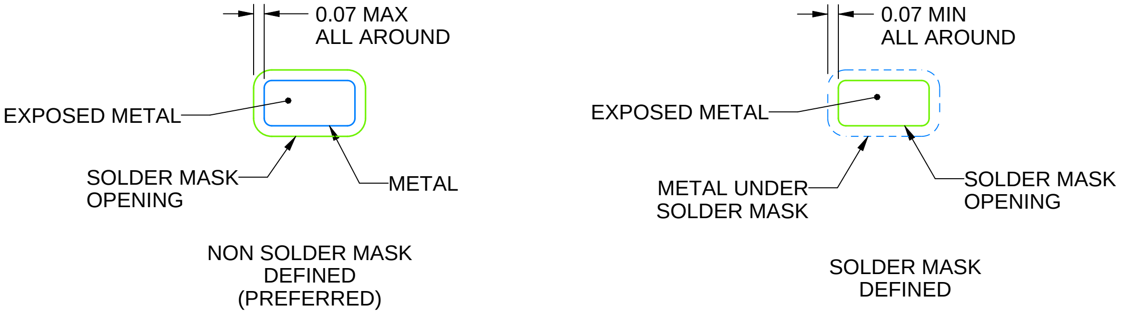
4225087/B 01/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

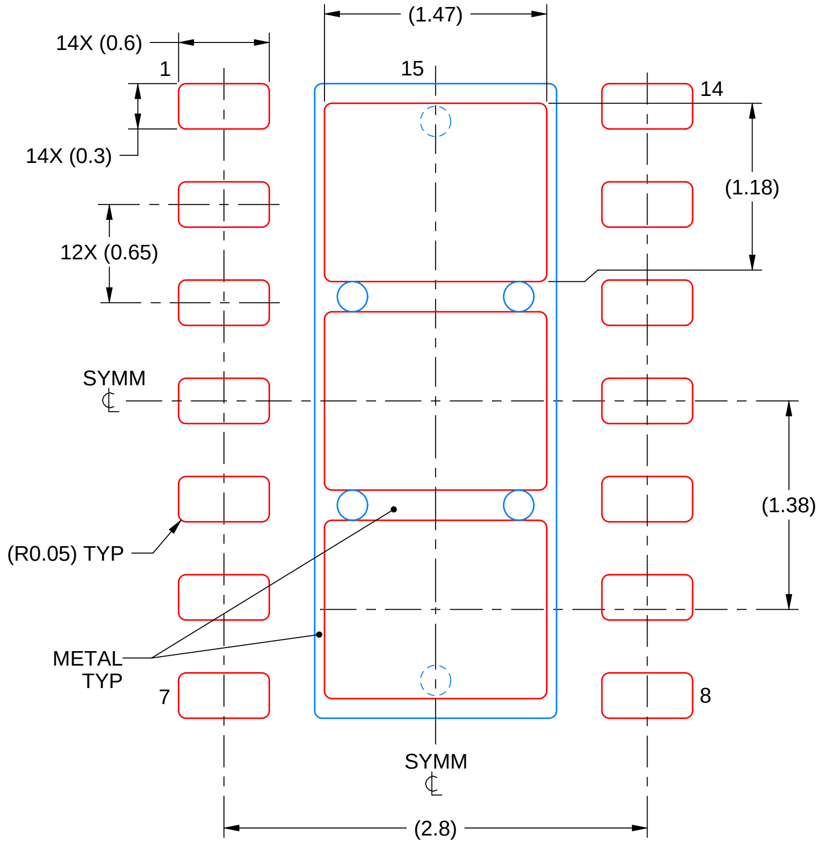


SOLDER MASK DETAILS

4225087/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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