TCAN245x-Q1 Automotive Signal Improvement Capable CAN FD System Basis Chip (SBC) with Integrated Buck Regulator and Watchdog

1 Features

- AEC-Q100 qualified for automotive applications
- Meets the requirements of ISO 11898-2:2024 for CAN-FD and CAN-FD Signal Improvement Capability (SIC)
- Functional Safety Quality-Managed
- Integrated 3.3V or 5V Buck regulator (VCC1) with 1A output capability
  - Pin-selectable output (3.3V or 5V) based on VSEL pin connection
  - Switching frequency options from 1.8MHz to 2.4MHz to enable a smaller on-board inductor
  - Integrated spread spectrum modulation to improve EMC performance
- 5V LDO regulator (VCC2) supporting up to 200mA with off-board capability and short-to-battery protection
- Multiple methods to wake-up from Sleep mode
  - CAN bus wake-up pattern (WUP)
  - Local wake up (LWU) using four WAKE pins
    - Cyclic sensing wake-up using a high-side switch (HSS4)
  - Selective wake (partial networking) capability, TCAN2451-Q1 only
  - Digital wake-up using SW pin
- WAKE pins configurable as ID pins to identify ECU location in the vehicle
- Four high-side switches to support multiple loads and allow for cyclic sensing wake
- Fail-safe output pin (LIMP):
  - Optionally used as a low-side switch
- ±58V Bus fault protection
- Advanced CAN bus fault diagnostics
- Timeout, window, and Q&A watchdog support
- Access to EEPROM to save device configuration
- Available in 32-pin leadless package with wettable flank for improved automated optical inspection (AOI) capability

2 Applications

- Body electronics and lighting
- Car access and security
- Hybrid, electric and powertrain systems
- Industrial transportation

3 Description

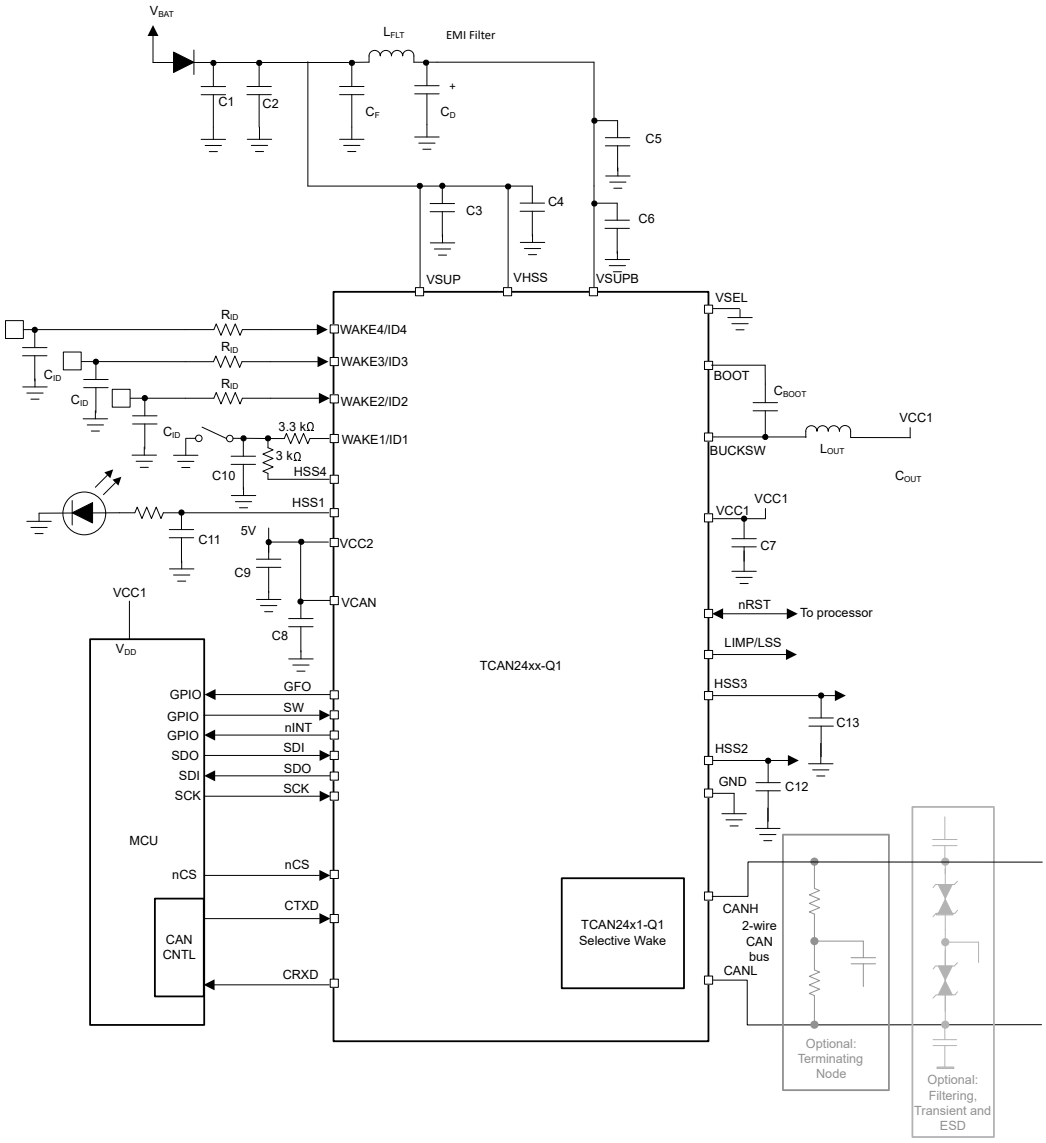
The TCAN245x-Q1 is a family of system basis chips (SBC) that provide a control area network flexible data rate capable (CAN FD) transceiver that meets the physical layer requirements of ISO-11898:2-2024 including the SIC specification. The CAN FD transceiver supports data rates up to 8Mbps. The TCAN245x-Q1 integrates a buck regulator (VCC1) that can output either 3.3V or 5V, and provide up to 1A output current. The buck regulator integrates spread spectrum modulation to improve EMC performance. VCC2 LDO provides 5V output for loads up to 200mA. TCAN2451-Q1 supports Partial Networking by recognizing a selective wakeup frame (WUF)

The TCAN245x-Q1 includes features such as LIMP, four local wake inputs and four high side switches. The high side switch can be on/off, 10-bit PWM or timer controlled. Using the GFO pin, controlling an external CAN FD, LIN transceiver, CAN SBC or LIN SBC is possible. The WAKE pins can be configured for static sensing, cyclic sensing (with HSS4 pin) and pulse based for waking up. These devices provide EEPROM to store specific device configuration information: thus, avoiding extensive reprogramming after power fluctuations.

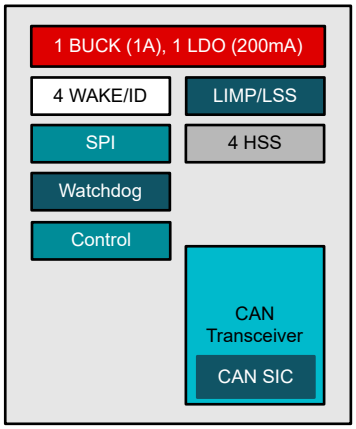
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCAN2450-Q1 TCAN2451-Q1	VQFN (32)	5mm × 5mm

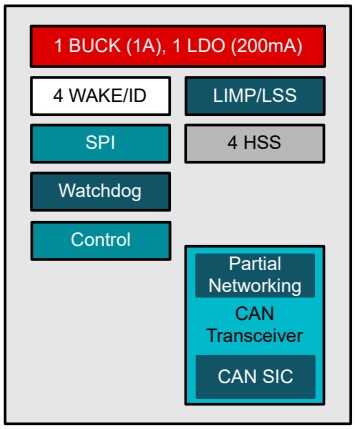
(1) For more information, see Section 13.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Diagram



TCAN2450-Q1 Diagram



TCAN2451-Q1 Diagram

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4 Device Comparison Table

Device Number	Selective Wake	Orderable Part Number	REV_ID
TCAN2450-Q1		TCAN2450RHBRQ1	20h
		TCAN2450MRHBRQ1	21h
TCAN2451-Q1	X	TCAN2451RHBRQ1	20h
		TCAN2451MRHBRQ1	21h

5 Pin Configuration and Functions

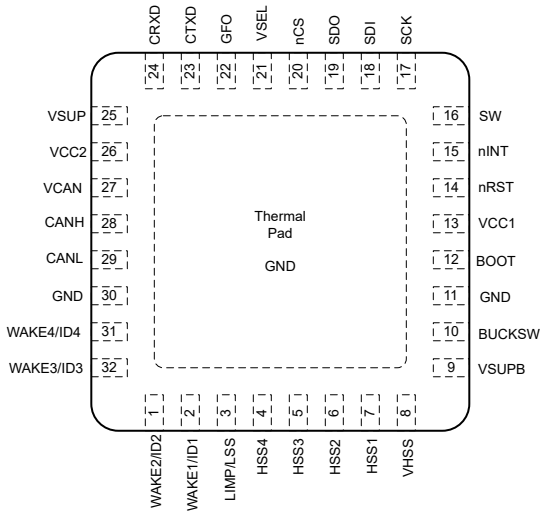


Figure 5-1. RHB Package, 32 Pin (VQFN) (Top View)

Table 5-1. Pin Functions

NAME	PIN NO.	TYPE[1]	DESCRIPTION
	RHB		
BOOT	12	P	HV. Bootstrap supply voltage for internal high-side driver. Connect a high-quality 100nF capacitor from this pin to the BUCKSW pin.
BUCKSW	10	P	HV. Buck regulator switching node. Connect to power inductor.
CANH	28	I/O	HV capable. High level CAN bus I/O line
CANL	29	I/O	HV capable. Low level CAN bus I/O line
CRXD	24	O	LV digital. CAN receive data output (low for dominant and high for recessive bus states), tri-state
CTXD	23	I	LV digital. CAN transmit data input (low for dominant and high for recessive bus states); Internal pull-up of 60kΩ.
GFO	22	O	LV digital. General function output pin (SPI configurable); Push-pull
GND	11	G	Ground
GND	30	G	Ground connection: Must be soldered to ground
GND	Thermal Pad	G	Ground connection: Must be soldered to ground
HSS1	7	O	HV. High side switch 1 output
HSS2	6	O	HV. High side switch 2 output
HSS3	5	O	HV. High side switch 3 output
HSS4	4	O	HV. High side switch 4 output
LIMP/LSS	3	O	HV capable. Limp home output (Active low; open-drain output)
NC	-	NC	Not connected internally.
nCS	20	I	LV digital. Chip select input (active low). Internal pull-up of 60kΩ
nINT	15	O	LV digital. Interrupt output (active low)
nRST	14	I/O	Low-voltage (LV) digital. VCC1 under-voltage monitor output pin (active low) and device reset input

Table 5-1. Pin Functions (continued)

NAME	PIN NO.	TYPE[1]	DESCRIPTION
	RHB		
SCK	17	I	LV digital. SPI clock input
SDI	18	I	LV digital. SPI data input. Internal pull-up of 60kΩ
SDO	19	O	LV digital. SPI data output.
SW	16	I	LV digital. Programming mode input pin (SPI configurable active high or active low). Internal pull-up (active low configuration) or pull-down (active high configuration) of 60kΩ
VCAN	27	P	5V power supply input for the CAN FD transceiver
VCC1	13	P	Buck regulator output 3.3V or 5V. Connect a high-quality capacitor to GND.
VCC2	26	P	5V LDO output. Short-to-battery protected.
VHSS	8	P	HV. Separate input supply for the high side switches. Typically connected to the battery but can also be supplied independently.
VSEL	21	I	LV digital. VCC1 output voltage selector pin. 1. Connected to GND: VCC1 = 5V 2. Floating: VCC1 = 3.3V. Internal pull-up of 30kΩ
VSUP	25	P	HV. Input supply pin, typically connected to battery.
VSUPB	9	P	HV. Input supply from the battery for the buck regulator. VSUPB and VSUP must be to the same battery supply, but separated by the EMI filter as shown in the application schematic to reduce the conducted EMI on the VSUP pin.
WAKE1/ID1	2	I	HV capable. Local wake input terminal. Configurable as an ID pin
WAKE2/ID2	1	I	High voltage (HV) capable. Local wake input terminal. Configurable as an ID pin
WAKE3/ID3	32	I	HV. Local wake input terminal. Configurable as an ID pin
WAKE4/ID4	31	I	HV capable. Local wake input terminal. Configurable as ID pin

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage (2)	–0.3	40	V
V_{SUPB}	Buck regulator input supply voltage (2)	–0.3	40	V
V_{SW}	Buck switching node voltage (2)	-1	V_{SUPB}+0.3	V
V_{BOOT_SW}	BOOT to SW voltage	-0.3	6	V
V_{HSS}	High-side switches supply voltage (2)	–0.3	40	V
V_{CC1}	Regulated 3.3V and 5V Output Supply	–0.3	6	V
V_{nRST}	Reset output voltage	-0.3	V_{CC1} + 0.3	V
V_{CAN}	CAN transceiver supply voltage	–0.3	6	V
V_{CC2}	5V CAN transceiver and external LDO (2)	–0.3	40 and $V_O \le V_{SUP}$+0.3	V
V_{BUSCAN}	CAN bus I/O voltage (CANH, CANL)	–58	58	V
$V_{WAKE/ID}$	WAKE input voltage (2)	–0.3	40 and $V_O \le V_{SUP}$+0.3	V
V_{HSSx}	High-side switch pin output voltage range (2)	–0.3	40 and $V_O \le V_{HSS}$+0.3	V
V_{LIMP}	LIMP pin output voltage range (2)	–0.3	40 and $V_O \le V_{SUP}$+0.3	V
V_{LOGIC_IN}	Logic pin input voltage range	–0.3	6	V
V_{LOGIC_OUT}	Logic pin output voltage range	–0.5	6	V
$I_{O(LOGIC)}$	Logic pin output current		8	mA
$I_{(WAKE/ID)}$	WAKE pin input current	-55	55	mA
$I_{(LIMP)}$	LIMP pin input current		40	mA
$I_{O(nRST)}$	Reset output current	–5	5	mA
T_J	Junction temperature	–55	165	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Able to support load dumps of up to 40V for 300ms

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	Between V_{SUP}, V_{SUPB}, V_{HSS}, CANL/H, WAKEx and GND	±8000	V
		Human body model (HBM), per AEC Q100-002(1)	All other pins	±4000	
		Charged device model (CDM) per AEC Q100-011		±750	
				±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 IEC ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge according to IEC 62228-3 (1)	Contact discharge, CANH, CANL, VSUP, VSUPB, VHSS, WAKE	±8000	V
$V_{(ESD)}$	SAE J2962-2 per ISO 10605 Powered Contact Discharge	Contact discharge (CANH, CANL)	±8000	V
$V_{(ESD)}$	SAE J2962-2 per ISO 10605 Powered Air Discharge	Air-gap discharge (CANH, CANL)	±15000	
ISO7637-2 and IEC 62215-3 Transients, CANH/L, VSUP, VHSS and WAKE(2)		Pulse 1	-100	V
		Pulse 2	75	
		Pulse 3a	-150	
		Pulse 3b	100	
IS07637-3 Slow Transient Pulse CAN bus terminals to GND(3)		Direct coupling capacitor "slow transient pulse" with 100nF coupling capacitor - powered	±30	V

(1) IEC 62228-3 ESD performed by IBEE Zwickau. Different system-level configurations may lead to different results. VSUP, VSUPB, VHSS are connected to the battery supply as per the recommended application diagram
(2) ISO 7637-2 according to IEC 62228-2 and IEC 62228-3 are system-level transient tests. Different system-level configurations may lead to different results.
(3) ISO 7637-3 is a system-level transient test. Different system-level configurations may lead to different results.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SUP}, V_{SUPB}	Supply voltage range	5.5		28	V
V_{SUP}, V_{SUPB}	Supply voltage range for VCC1=3.3V configuration (1)	4.5		28	V
V_{HSS}	High-side switches supply voltage	5		28	V
V_{CAN}	CAN Transceiver supply voltage	4.75	5	5.25	V
$I_{OH(DO)}$	Digital output high level current	–2			mA
$I_{OL(DO)}$	Digital output low level current			2	mA
$I_{O(LIMP)}$	LIMP/LSS pin current when configured as LIMP			6	mA
$I_{O(LSS)}$	LIMP/LSS pin current when configured as low-side switch			25	mA
$C_{(VSUP)}$, $C_{(VSUPB)}$,	V_{SUP}, V_{SUPB} supply capacitance	100			nF
$C_{(VCC2)}$	VCC2 supply effective capacitance	1			µF
ESR_{CO}	VCC2 output ESR capacitance requirements	0.001		1	Ω
TSDWR	Thermal shut down warning	140		165	°C
TSDWF	Thermal shut down warning release	130		155	°C
TSDWHYS	Thermal shut down warning hysteresis		10.0		°C
TSDR	Thermal shut down	165		200	°C
TSDF	Thermal shut down release	155		190	°C
TSDHYS	Thermal shut down hysteresis		10.0		°C
T_J	Operating junction temperature range	–40		150	°C

(1) When VCC1 is 3.3V output, VCC1 will work with a VSUP of 4.5V but other LDOs will be in pass thru mode and output voltage will not be at regulated value. For all LDOs to be in regulation VSUP needs to be at or above 5.5V.

6.5 Thermal Information

THERMAL METRIC(1)		RHB (VQFN) 32-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.6 Supply Characteristics

Over recommended operating conditions with VSUP/VSUPB/VHSS = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB/VHSS = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Battery Current Consumption (VSUP and VSUPB included)						
$ISUP_{NORMAL-150C}$	Normal mode: battery supply current	SBC in Normal mode; CAN transceiver off; VCC1= on (FPWM mode) but no load, VCC2 = off, V_{SUP} = 5.5V to 28V		8	11	mA
$ISUP_{STDBY-85C}$	Standby mode: Battery supply current up to 85℃	VCC1 = on but no load; Spread spectrum modulation disabled; VCC2 = off; All HSS= off; VCC1 sink disabled; CAN transceiver off; Wake pins are off; Selective wake = off; cyclic sensing = off, cyclic wake = off; WD=off, Long Window has expired VSUP,VSUPB = 6.5V to 12V; T_J : - 40℃ to 85℃		60	70	µA
$ISUP_{SLP-85C}$	Sleep mode: Battery supply current up to 85℃	Sleep mode; selective wake off; VCC1 and VCC2 = off; 6.5V ≤ VSUP ≤ 12V; transceiver is off; all HSS are off; 1 WAKE pin active; cyclic sensing/wake off, VCC1 and VCC2 are off; T_J <= 85℃		18	31	µA
$ISUP_{SLP-150C}$	Sleep mode: Battery supply current up to 150℃	Sleep mode; VCC1 and VCC2 = off; 1 wake pin active; CAN transceiver = off; cyclic sensing wake = off; cyclic wake = off VSUP, VSUPB = 6.5V to 28V ; T_J : - 40℃ to 150℃;		18	50	µA
Feature Incremental Current Consumption (VSUP and VSUPB Included)						
$ISUP_{STDBY-CS-WK-85C}$	Additional current when cyclic sensing wake is enabled in Standby or Sleep mode for WAKE1 or WAKE2, WAKE3 pins (1)	Cyclic sensing wake enabled, VSUP=14V, T_J ≤ 85℃, TIMERx with ON width = 1ms, period = 100ms		2.5	8	µA
$ISUP_{STDBY-CS-WK4-85C}$	Additional current when cyclic sensing wake is enabled in Standby or Sleep mode for WAKE4 pin (1)	Cyclic sensing wake enabled, VSUP=14V, T_J ≤ 85℃, TIMERx with ON width = 1ms, period = 100ms		45	50	µA
$ISUP_{STDBY-HSS-NOLOAD}$	Standby mode: Additional supply current draw when each HSS is enabled	For each HSS set to ON but no load VSUP = 6.5V to 12V; T_J : - 40℃ to 85℃		35	60	µA

6.6 Supply Characteristics (continued)

Over recommended operating conditions with VSUP/VSUPB/VHSS = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB/VHSS = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ISUP_{SLP-VCC2-85C}$	Sleep mode: Additional supply current when VCC2 is enabled	Sleep mode; additional current when VCC2 is enabled and no load. VSUP = 6.5V to 12V; T_J : - 40℃ to 85℃		25	35	µA
$ISUP_{SLP-VCC1-85C}$	Sleep mode: Additional supply current when VCC1 buck regulator is enabled	VCC1= on but no load; VCC1 sink = off; Spread Spectrum Modulation = off; VSUP = 6.5V to 12V; T_J : - 40℃ to 85℃		30	39	µA
$ISUP_{SLP-swk}$	Additional current when selective wake is on and WUP has taken place on CAN bus - bus active	Additional sleep current draw when selective wake is enabled and bus active; VCC1 and VCC2 = off		480	550	µA
$ISUP_{SLP-CANWK-85C}$	Sleep mode: Additional supply current when CAN transceiver is wake capable	Sleep mode: Additional supply current when CAN transceiver is wake capable; VSUP = 6.5V to 12V; T_J : - 40℃ to 85℃		7	10	µA
$ISUP_{SLP-wake-85C}$	Sleep mode: Additional supply current draw from WAKE pin	Sleep mode: Additional current from each WAKE pin when wake capable; WAKE pin floating or grounded.		0.5	1	µA
$ISUP_{WD-TO-85C}$	Standby or Sleep mode: Additional supply current when WD type is set to Timeout	Standby or Sleep mode: Additional supply current when WD type is set to Timeout. VSUP = 6.5V to 12V; T_J : - 40℃ to 85℃		2	2.5	µA
$ISUP_{WD-85C}$	Standby mode: Additional supply current when WD is set to Window or Q/A type	Standby mode: Additional supply current when WD is set to Window or Q/A. VSUP = 6.5V to 12V; T_J : - 40℃ to 85℃		40	50	µA
VSUP Supply Monitoring						
$VSUP_{(PU)R}$	Supply on detection	VSUP rising; see Figure 10-6 and Figure 10-4	3.1	3.4	3.7	V
$VSUP_{(PU)F}$	Supply off detection	VSUP falling; see Figure 10-6 and Figure 10-4	2.7	3	3.3	V
$VSUP_{(PU)HYS}$	Supply off detection hysteresis		50	150	550	mV
$UVSUP_{5R}$	Supply undervoltage recovery	VSUP rising; see Figure 10-3 and Figure 10-4	4.9		5.5	V
$UVSUP_{5F}$	Supply undervoltage detection	VSUP falling; see Figure 10-3 and Figure 10-4	4.5		5.1	V
$UVSUP_{5HYS}$	Supply undervoltage detection hysteresis			400		mV
$UVSUP_{33R}$	Supply undervoltage recovery	VSUP rising; see Figure 10-5 and Figure 10-6	3.7		4.4	V
$UVSUP_{33F}$	Supply undervoltage detection	VSUP falling; see Figure 10-5 and Figure 10-6	3.55		4.25	V
$UVSUP_{33HYS}$	Supply undervoltage detection hysteresis			150		mV
$VSUP_{UVLOVCC1(F)}$	Under-voltage lockout falling VSUP threshold value where VCC1 regulator is turned-off	Falling VSUP, VSUP_UVLO_SEL = 0b	3.1		3.3	V
$VSUP_{UVLOVCC1(R)}$	Under-voltage lockout release value	Rising VSUP, VSUP_UVLO_SEL = 0b	3.3		3.5	V
$VSUP_{UVLOVCC1(F)}$	Under-voltage lockout release value	Falling VSUP, VSUP_UVLO_SEL = 1b	4.9		5.1	V

6.6 Supply Characteristics (continued)

Over recommended operating conditions with VSUP/VSUPB/VHSS = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB/VHSS = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VSUP_{UVLOVCC1(R)}$	Under-voltage lockout falling VSUP threshold value where VCC1 regulator is turned-off	Rising VSUP, VSUP_UVLO_SEL = 1b	5.1		5.3	V
VSUPB - Buck regulator input supply						
$ISUPB_{VCC1-OFF-85c}$	VSUPB supply current when buck is disabled	Sleep mode; VCC1 disabled; VSUPB= 12V; T_J <= 85℃		1	3	µA
$ISUPB_{VCC1-ON-85c}$	VSUPB supply current when buck is enabled but no load current; VCC1 = 5V	VCC1 enabled and no load, VCC1 sink disabled; Buck in Auto mode; VSUPB=12V; T_J <= 85℃		3	8	µA
$ISUPB_{VCC1-ON-85c}$	VSUPB supply current when buck is enabled but no load current; VCC1 = 3.3V	VCC1 enabled and no load, VCC1 sink disabled; Buck in Auto mode; VSUPB=12V; T_J <= 85℃		2.5	5	µA
VHSS - High Side Switch Supply Input						
$IVHSS_{SLP}$	High-side switch supply (VHSS) current consumption in Sleep mode	Sleep Mode; cyclic sensing wake = off; -40℃ ≤ T_J ≤ 85℃		1	2	µA
$IHSS_{NOLOAD}$	Additional current draw for each HSS turned ON	For each HSS turned ON, No load on HSS output		100	140	µA
$UVHSS_R$	High-side switches supply undervoltage recovery	VHSS rising	4.6		4.9	V
$UVHSS_F$	High-side switches supply undervoltage detection	VHSS falling	4.4		4.7	V
$UVHSS_{HYS}$	High-side switches supply undervoltage detection hysteresis		100			mV
$OVHSS_F$	VHSS over-voltage falling threshold; VHSS must be below this threshold to enable the high-side switches again	VHSS falling	18.8		21.2	V
$OVHSS_R$	VHSS over-voltage rising threshold; high-side switches turn-off if HSS_OV_DIS = 0b	VHSS rising	20		22	V
$OVHSS_{HYS}$	VHSS over-voltage threshold hysteresis		800		1200	mV
VCC1 - Buck Regulator Output						
$VCC1_5$	Regulated output range, 5V version	VSUPB = 6V to 28 V, ICC1 = 0 to 1A, PWM Mode	4.9	5	5.1	V
$VCC1_5$	Regulated output range, 5V version	VSUPB = 6V to 28 V, ICC1 = 0 to 1A, PFM Mode	4.85	5	5.15	V
$VCC1_{33}$	Regulated output range, 3.3V version	VSUPB = 4.5V to 28 V, ICC1 = 0 to 1A, PWM Mode	3.23	3.3	3.37	V
$VCC1_{33}$	Regulated output range, 3.3V version	VSUPB = 4.5V to 28 V, ICC1 = 0 to 1A, PFM Mode	3.20	3.3	3.40	V
$VCC1_{EFF}$	Buck converter efficiency	ICC1 = 500mA; VCC1 current sink disabled. VCC1= 3.3V, VSUPB = 12V; PWM Mode		0.85		

6.6 Supply Characteristics (continued)

Over recommended operating conditions with VSUP/VSUPB/VHSS = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB/VHSS = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VCC1_{EFF}$	Buck converter efficiency	ICC1 = 100mA; VCC1 current sink disabled. VCC1= 3.3V, VSUPB = 12V; PFM Mode		0.80		
		ICC1 = 10mA; VCC1 current sink disabled. VCC1= 3.3V, VSUPB = 12V; PFM Mode		0.8		
		ICC1 = 1mA; VCC1 current sink disabled. VCC1= 3.3V, VSUPB = 12V; PFM Mode		0.7		
		ICC1 = 0.1mA; VCC1 current sink disabled. VCC1= 3.3V, VSUPB = 12V; PFM Mode		0.4		
$R_{DS-ON-LS}$	Low-side MOSFET on-resistance	ICC1= 0.3A, VSUPB = 12V		0.24		Ω
$R_{DS-ON-HS}$	High-side MOSFET on-resistance	ICC1= 0.3A, VSUPB = 12V		0.45		Ω
ICC1	VCC1 output current	VCC1 in regulation; VSUPB= 12V	0		1	A
$ICC1_{SINK}$	VCC1 current sink capability (if enabled), when VCC1 is ON	VSUPB = 12V and register 8'h0C[4] = 0b and 8'h0D[3] = 0b		–10		µA
		VSUPB = 12V and register 8'h0C[4] = 0b and 8'h0D[3] = 1b		–1000		µA
$R_{QOD-VCC1}$	Output discharge resistor on VCC1 when VCC1 is disabled	VCC1 is disabled and VCC1=100mV externally (for 3.3V VCC1 option)		0.9		kΩ
$R_{QOD-VCC1}$	Output discharge resistor on VCC1 when VCC1 is disabled	VCC1 is disabled and VCC1=100mV externally (for 5V VCC1 option)		0.9		kΩ
$ICC1_{SC}$	Buck high-side current limit	Register 8'h65[0]=0	1.2	1.6	1.95	A
$ICC1_{SC}$	Buck high-side current limit	Register 8'h65[0]=1	0.6	0.8	1	A
$ICC1_{LS}$	Buck low-side current limit	Register 8'h65[0]=0	0.9	1.1	1.3	A
$ICC1_{LS}$	Buck low-side current limit	Register 8'h65[0]=1	0.45	0.55	0.65	A
$UVCC1_{5FPR}$	VCC1 undervoltage recovery threshold pre-warning	VCC1 rising	4.65	4.78	4.9	V
	VCC1 undervoltage detection threshold pre-warning	VCC1 falling	4.55	4.67	4.80	V
$UVCC1_{5R1}$	VCC1 undervoltage recovery threshold 1	VCC1 rising, Register 8'h0E[4:3] = 00b	4.60	4.72	4.85	V
$UVCC1_{5F1}$	VCC1 undervoltage detection threshold 1	VCC1 falling, Register 8'h0E[4:3] = 00b	4.50	4.62	4.75	V
$UVCC1_{5R2}$	VCC1 undervoltage recovery threshold 2	VCC1 rising, Register 8'h0E[4:3] = 01b	3.85	4.00	4.15	V
$UVCC1_{5F2}$	VCC1 undervoltage detection threshold 2	VCC1 falling, Register 8'h0E[4:3] = 01b	3.75	3.90	4.05	V
$UVCC1_{5R3}$	VCC1 undervoltage recovery threshold 3	VCC1 rising, Register 8'h0E[4:3] = 10b	3.25	3.40	3.55	V
$UVCC1_{5F3}$	VCC1 undervoltage detection threshold 3	VCC1 falling, Register 8'h0E[4:3] = 10b	3.15	3.30	3.45	V
$UVCC1_{5R4}$	VCC1 undervoltage recovery threshold 4	VCC1 rising, Register 8'h0E[4:3] = 11b	4.60	4.72	4.85	V
$UVCC1_{5F4}$	VCC1 undervoltage detection threshold 4	VCC1 falling, Register 8'h0E[4:3] = 11b	3.45	3.6	3.75	V
$UVCC1_{5HYS}$	Undervoltage detection 5V hysteresis, VCC1 set to 5V	Register 8'h0E[4:3] = 00b, 01b or 10b	50.00		150.00	mV
$UVCC1_{5HYS4}$	Undervoltage detection 5V hysteresis, VCC1 set to 5V	Register 8'h0E[4:3] = 11b		1200		mV

6.6 Supply Characteristics (continued)

Over recommended operating conditions with VSUP/VSUPB/VHSS = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB/VHSS = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$UVCC1_{33RPR}$	VCC1 undervoltage recovery threshold pre-warning	VCC1 rising	3.1	3.2	3.28	V
$UVCC1_{33FPR}$	VCC1 undervoltage detection threshold pre-warning	VCC1 falling	3	3.1	3.2	V
$UVCC1_{33R1}$	VCC1 undervoltage recovery threshold 1	VCC1 rising, Register 8'h0E[4:3] = 00b	3	3.1	3.2	V
$UVCC1_{33F1}$	VCC1 undervoltage detection threshold 1	VCC1 falling, Register 8'h0E[4:3] = 00b	2.95	3.05	3.15	V
$UVCC1_{33R2}$	VCC1 undervoltage recovery threshold 2	VCC1 rising, Register 8'h0E[4:3] = 01b	2.55	2.65	2.75	V
$UVCC1_{33F2}$	VCC1 undervoltage detection threshold 2	VCC1 falling, Register 8'h0E[4:3] = 01b	2.5	2.6	2.7	V
$UVCC1_{33R3}$	VCC1 undervoltage recovery threshold 3	VCC1 rising, Register 8'h0E[4:3] = 10b	2.25	2.35	2.45	V
$UVCC1_{33F3}$	VCC1 undervoltage detection threshold 3	VCC1 falling, Register 8'h0E[4:3] = 10b	2.2	2.3	2.4	V
$UVCC1_{33R4}$	VCC1 undervoltage recovery threshold 4	VCC1 rising, Register 8'h0E[4:3] = 11b	3	3.1	3.2	V
$UVCC1_{33F4}$	VCC1 undervoltage detection threshold 4	VCC1 falling, Register 8'h0E[4:3] = 11b	2.2	2.3	2.4	V
$UVCC1_{33HYS}$	Undervoltage detection hysteresis, VCC1 set to 3.3V	Register 8'h0E[4:3] = 00b, 01b or 10b	30		140	mV
$UVCC1_{33HYS4}$	Undervoltage detection hysteresis, VCC1 set to 3.3V	Register 8'h0E[4:3] = 11b		800		mV
VDROP-OUT-33	Drop-out voltage. VCC1 set to 3.3V	VSUPB = 3.5V, ICC1 = 0.5A, F_{SW}= 2.2MHz, $L_{OUT-ESR}$ = 50mΩ		0.35		V
VDROP-OUT-33	Drop-out voltage. VCC1 set to 3.3V	VSUPB = 3.5V, ICC1 = 1A, F_{SW}= 2.2MHz, $L_{OUT-ESR}$ = 50mΩ		0.7		V
VDROP-OUT-5	Drop-out voltage. VCC1 set to 5V	VSUPB = 5V, ICC1 = 0.5A, F_{SW}= 2.2MHz, $L_{OUT-ESR}$ = 50mΩ		0.35		V
VDROP-OUT-5	Drop-out voltage. VCC1 set to 5V	VSUPB = 5V, ICC1 = 1A, F_{SW}= 2.2MHz, $L_{OUT-ESR}$ = 50mΩ		0.7		V
$OVCC1_{5R1}$	Over voltage 5V VCC1 threshold to enter sleep mode or fail-safe mode	Ramp up, Register 8'h0C[7] = 0b	5.3	5.45	5.6	V
$OVCC1_{5F1}$	Over voltage 5V VCC1 threshold	Ramp down, Register 8'h0C[7] = 0b	5.2	5.35	5.5	V
$OVCC1_{5R2}$	Over voltage 5V VCC1 threshold to enter sleep mode or fail-safe mode	Ramp up, Register 8'h0C[7] = 1b	5.47	5.6	5.73	V
$OVCC1_{5F2}$	Over voltage 5V VCC1 threshold	Ramp down, Register 8'h0C[7] = 1b	5.37	5.5	5.63	V
$OVCC1_{5HYS}$	Over voltage 5V VCC1 threshold hysteresis			100		mV
$OVCC1_{33R1}$	Over voltage 3.3V VCC threshold to enter sleep mode or fail-safe mode	Ramp Up, Register 8'h0C[7] = 0b	3.5	3.6	3.7	V
$OVCC1_{33F1}$	Over voltage 3.3V VCC threshold	Ramp Down, Register 8'h0C[7] = 0b	3.4	3.5	3.6	V
$OVCC1_{33R2}$	Over voltage 3.3V VCC threshold to enter sleep mode or fail-safe mode	Ramp Up, Register 8'h0C[7] = 1b	3.6	3.7	3.8	V
$OVCC1_{33F2}$	Over voltage 3.3V VCC threshold	Ramp Down, Register 8'h0C[7] = 1b	3.55	3.65	3.75	V
$OVCC1_{33HYS1}$	Over voltage 3.3V VCC threshold hysteresis	Register 8'h0C[7] = 0b		100		mV
$OVCC1_{33HYS2}$	Over voltage 3.3V VCC threshold hysteresis	Register 8'h0C[7] = 1b		50		mV

6.6 Supply Characteristics (continued)

Over recommended operating conditions with VSUP/VSUPB/VHSS = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB/VHSS = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VCC1_{5SC}$	VCC1 short circuit threshold to enter sleep mode or fail-safe mode for 5V version		1.7	2	2.3	V
$VCC1_{33SC}$	VCC1 short circuit threshold to enter sleep mode or fail-safe mode for 3.3V version		1.12	1.22	1.26	V
VCC2 - LDO Regulator Output						
VCC2nom	Regulated output voltage including load regulation	VSUP = 14V, ICC2 = 5 to 200mA	4.9	5	5.1	V
VCC2reg	Regulated output voltage including load and line regulation	VSUP = 8V to 18V, ICC2 = 10µA to 200mA	4.85	5	5.15	V
VCC2red	Regulated output voltage for reduced load range	VSUP = 8V - 18V; ICC2 = 10µA - 5mA; T_J= -40°C - 125°C	4.95	5	5.05	V
$ICC2_{LIM}$	VCC2 output current limit	VCC2 = 2.5V	250		650	mA
$UVCC2_R$	Undervoltage recovery VCC2	VCC2 rising	4.6		4.9	V
$UVCC2_F$	Undervoltage detection VCC2	VCC2 falling	4.5		4.75	V
$UVCC2_{HYS}$	Undervoltage detection VCC2 hysteresis		70	125	175	mV
$OVCC2_R$	Over voltage CAN LDO threshold	Ramp Up	5.37	5.5	5.63	V
$OVCC2_F$	Over voltage CAN LDO threshold	Ramp Down	5.25	5.38	5.5	V
$OVCC2_{HYS}$	Over voltage CAN LDO threshold hysteresis			125		mV
$VCC2_{SC}$	VCC2 LDO short circuit threshold	VSUP ≥ UVSUP	1.7		2.3	V
V_{5DROP2}	Dropout voltage (5V LDO output VCC2)	VSUP = 5V, ICC2 = 100mA			750	mV
VCAN - CAN Supply Input						
$I_{CAN-NORMAL-REC}$	Normal mode: CAN FD bus recessive	Normal mode: Recessive, V_{TXD} = VCC1 , VCC1 and VCC2 = no load		3	5	mA
$I_{CAN-NORMAL-DOM}$	Normal mode: CAN FD bus dominant	Normal mode: Dominant, V_{TXD} = 0V, R_L = 60Ω and C_L = open, typical bus load, VCC1 and VCC2 = no load			60	mA
		Normal mode: Dominant, V_{TXD} = 0V, R_L = 50Ω and C_L = open, high bus load, VCC1 and VCC2 = no load			65	mA
		Normal mode: Dominant with bus fault, V_{TXD} = 0V, CANH = - 25V, R_L and C_L = open, VCC1 and VCC2 = no load			100	mA
$UVCAN_R$	Supply undervoltage recovery	VCAN rising	4.6		4.85	V
$UVCAN_F$	Supply undervoltage detection	VCAN falling	4.5		4.75	V
$UVCAN_{HYS}$	VCAN Supply undervoltage detections hysteresis			100		mV

(1) Cyclic sensing for WAKE1, WAKE2 and WAKE3 pin uses a low power 10kHz internal clock to reduce the current consumption. Cyclic sensing for WAKE4 pin uses the 1MHz internal clock that consumes more current than the 10kHz clock. It is recommended to use WAKE1-3 pins for cyclic sensing for lower current consumption.

6.7 Electrical Characteristics

Over recommended operating conditions with VSUP/VSUPB/VHSS = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB/VHSS = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN Driver					

6.7 Electrical Characteristics (continued)

Over recommended operating conditions with VSUP/VSUPB/VHSS = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB/VHSS = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CANH(D)}$	Bus output voltage (dominant) CANH	See Figure 7-4, V_{CTXD} = 0V, R_L =45Ω to 65Ω, C_L = open, R_{CM} = open	3		4.26	V
$V_{CANL(D)}$	Bus output voltage (dominant) CANL		0.75		2.01	V
$V_{CANH(R)}$ $V_{CANL(R)}$	Bus output voltage (recessive)	See Figure 7-1 and Figure 7-4 V_{CTXD} = VCC1, R_L = open (no load), R_{CM} = open	2	2.5	3	V
$V_{(DIFF)}$	Maximum differential voltage rating		–42		42	V
$V_{DIFF(D)}$	Differential output voltage(dominant)	See Figure 7-1 and Figure 7-4 , V_{CTXD} = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open	1.5		3	V
		See Figure 7-1 and Figure 7-4 V_{CTXD} = 0V, 45Ω ≤ R_L ≤ 70Ω, C_L = open, R_{CM} = open	1.5		3.3	V
		See Figure 7-1 and Figure 7-4 V_{CTXD} = 0V, R_L = 2.24kΩ, C_L = open, R_{CM} = open	1.5		5	V
$V_{DIFF(R)}$	Differential output voltage(recessive)	See Figure 7-1 and Figure 7-4 , V_{CTXD} = VCC1, R_L = 60Ω, C_L = open, R_{CM} = open	–120		12	mV
		See Figure 7-1 and Figure 7-4 V_{CTXD} = VCC1, R_L = open (no load), C_L = open, R_{CM} = open	–50		50	mV
$V_{CANH(INACT)}$	Bus output voltage on CANH with bus biasing inactive (STBY)	See Figure 7-1 and Figure 7-4 , V_{CTXD} = VCC1, R_L = open, C_L = open, R_{CM} = open	–0.1		0.1	V
$V_{CANL(INACT)}$	Bus output voltage on CANL with bus biasing inactive (STBY)		–0.1		0.1	V
$V_{DIFF(INACT)}$	Bus output voltage on CANH - CANL (recessive) with bus biasing inactive (STBY)		–0.2		0.2	V
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{REC} where V_{REC} = $V_{CANH(R)}$ + $V_{CANL(R)}$	See Figure 7-1 and Figure 7-4 , 45Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open, C_1 = 4.7nF, CTXD = 250kHz, 1MHz, 2.5MHz	0.95		1.05	V/V
V_{SYM_DC}	DC Output symmetry (V_{CAN} – $V_{O(CANH)}$ – $V_{O(CANL)}$)	See Figure 7-1 and Figure 7-4 , 45Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open, C_1 = 4.7nF	–300		300	mV
$I_{CANH(OS)}$	Short-circuit steady-state output current, dominant See Figure 7-1 and Figure 7-8	–3.0V ≤ V_{CANH} ≤ +18.0V, CANL = open, V_{CTXD} = 0V	–100			mA
$I_{CANL(OS)}$		–3.0V ≤ V_{CANL} ≤ +18.0V, CANH = open, V_{CTXD} = 0V			100	mA
I_{OS_REC}	Short-circuit steady-state output current, recessive See Figure 7-1 and Figure 7-8	–42V ≤ V_{BUS} ≤ +42V, V_{BUS} = CANH = CANL	–5		5	mA
CAN Receiver						
$V_{DIFF\_RX(D)}$	Receiver dominant state differential input voltage range, bus biasing active	–12.0V ≤ V_{CANL} ≤ +12.0V –12.0V ≤ V_{CANH} ≤ +12.0V See Figure 7-5 and Table 8-3	0.9		8	V
$V_{DIFF\_RX(R)}$	Receiver recessive state differential input voltage range, bus biasing active		–3		0.5	V
V_{HYS}	Hysteresis voltage for input-threshold, normal and selective wake modes			135		mV

6.7 Electrical Characteristics (continued)

Over recommended operating conditions with VSUP/VSUPB/VHSS = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB/VHSS = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DIFF\_RX(D\_INACT)}$	Receiver dominant state differential input voltage range, bus biasing inactive	–12.0V ≤ V_{CANL} ≤ +12.0V –12.0V ≤ V_{CANH} ≤ +12.0V See Figure 7-5 and Table 8-3	1.15		8	V
$V_{DIFF\_RX(R\_INACT)}$	Receiver recessive state differential input voltage range, bus biasing inactive		–3		0.4	V
V_{CM_NORM}	Common mode range: normal		–12		12	V
V_{CM_STBY}	Common mode range: standby mode		–12		12	V
$I_{LKG(OFF)}$	Power-off (unpowered) bus input leakage current	CANH = CANL = 5V, VCAN = VSUP = 0			5	µA
C_I	Input capacitance to ground (CANH or CANL)				30	pF
C_{ID}	Differential input capacitance				15	pF
$R_{SE\_CANH/L}$	Single ended Input resistance (CANH or CANL)	–2.0V ≤ V_{CANH} ≤ +7.0V –2.0V ≤ V_{CANL} ≤ +7.0V	6		50	kΩ
$R_{DIFF\_PAS\_REC}$	Differential input resistance during passive recessive phase	V_{TXD} = V_{IO}, normal mode: –2.0V ≤ V_{CANH} ≤ +7.0V; –2.0V ≤ V_{CANL} ≤ +7.0V	12		100	kΩ
$R_{IN(M)}$	Input resistance matching: [2x ($R_{IN(CANH}$ - RI_{NCANL})/(R_{CANH}+R_{INCANL})] x100 (%)	V_{CANH} = V_{CANL} = 5.0V	–1		1	%
CAN Signal Improvement Function						
$R_{SE\_ACT\_REC}$	Single ended SIC impedance (CANH to common mode bias and CANL to common mode bias) during active recessive drive phase	2V ≤ $V_{CANH, CANL}$ ≤ V_{CAN} - 2V Duration from the TXD low-to-high edge to the elapse of the active recessive phase (t_{SIC_END}). See Figure 7-17	37.5		66.5	Ω
$R_{DIFF\_ACT\_REC}$	Differential input resistance in active recessive drive phase (CANH to CANL)	2V ≤ $V_{CANH, CANL}$ ≤ V_{CAN} - 2V Duration from the TXD low-to-high edge to the elapse of the active recessive phase (t_{SIC_END}). See Figure 7-17	75		133	Ω
LIMP Output (Open-drain)						
V_{OL}	Open-drain output voltage (active low)	4.5V < V < 28V, I_{LIMP} = – 6mA		0.5	1	V
$I_{LKG(LIMP)}$	Output current (inactive)	V_{LIMP} = 0V to 28V	–2		2	µA
$V_{OL-LSS1}$	Low-side output voltage (If configured as low-side switch)	5V < VSUP < 28V, I_{LSS} = -20mA;			1	V
$V_{OL-LSS2}$	Low-side output voltage (If configured as low-side switch)	5V < VSUP < 28V, I_{LSS} = -100µA			5	mV
I_{LSS}	Low-side switch current limit	5V < VSUP < 28V	22	30	38	mA
HSS1, HSS2, HSS3, HSS4 (High voltage output)						
R_{dson}	HSS output drain-to-source on resistance	I_O = – 60mA		7	16	Ω
$I_{OC(HSS)}$	HSS overcurrent detection limit	VHSS = 14V	150		300	mA
$I_{OL(HSS)}$	HSS open load detection current threshold, falling	VHSS = 14V	0.4		3.0	mA
$I_{OLHYS(HSS)}$	HSS open load detection current hysteresis	VHSS = 14V	0.05	0.45	1	mA
I_{lkg}	Leakage current	HSSx = 0V, Sleep Mode	–1		1	µA
$SR_{R/F}$	Output rising and falling slew rates (HSS1-4)	5V ≤ VHSS ≤ 18V, R_L = 220Ω, $V_{O(HSSx)}$ 20% to 80% (for t_R) and 80% to 20% (for t_F)	0.45		2.5	V/µs

6.7 Electrical Characteristics (continued)

Over recommended operating conditions with VSUP/VSUPB/VHSS = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB/VHSS = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{HSS_on}	Switching on delay of HSSx from nCS=HIGH to 80% of VHSS	VHSS = 14V, R_L = 220Ω, V_{OUT} = 80% of VHSS	30		90	µs
t_{HSS_off}	Switching off delay of HSSx from nCS=HIGH to 20% of VHSS	VHSS = 14V, R_L = 220Ω, V_{OUT} = 20% of VHSS	30		90	µs
t_{OCFLTR}	HSS overcurrent filter time to set the overcurrent interrupt fault	VHSS = 14V		16		µs
t_{OLFLTR}	HSS open load filter time	VHSS = 14V		64		µs
t_{OCOFF}	HSS overcurrent shut off time. HSS is turned off if the overcurrent condition exists for this duration	$I_{O(HSS)} > I_{OC(HSS)}$	200		350	µs
WAKE1/ID1, WAKE2/ID2, WAKE3/ID3, WAKE4/ID4 Input Terminal (High voltage input)						
V_{IH}	High-level input voltage: WAKE pin enabled and in Sleep, selective wake-up or standby mode or when ID function enabled (1)	Register setting 00b VCC1 based	0.7*V_{CC1}			V
		Register setting 01b	2.7	2.8	2.9	V
		Register setting 10b	4.0	4.1	4.2	V
		Register setting 10b (TCAN245x**M**RHBRQ1 variants only)	3.9	4.1	4.3	V
		Register setting 11b	6.4	6.6	6.8	V
V_{IL}	Low-level input voltage: WAKE pin enabled in Sleep, selective wake-up or standby mode or when ID function enabled(1)	Register setting 00b VCC1 based			0.3*V_{CC1}	V
		Register setting 01b	2.1	2.2	2.4	V
		Register setting 10b	3.2	3.35	3.5	V
		Register setting 11b	5.3	5.45	5.6	V
		Register setting 11b (TCAN245x**M**RHBRQ1 Variants Only)	5.2	5.45	5.6	V
I_{IH}	High-level input current, WAKE pin enabled	WAKE = 12V		10	15	µA
I_{IL}	Low-level input current, WAKE pin enabled	WAKE = 1V		1	2	µA
t_{WAKE}	Wake up hold time from a wake edge (rising or falling) on WAKE in standby or sleep mode for static sensing.	See Figure 8-18 and Figure 8-19	140			µs
$t_{WAKE\_INVALID}$	WAKE pin pulses shorter than this will be filtered out in standby or sleep mode for static sensing.	See Figure 8-18 and Figure 8-19			10	µs
ID_{Pu}	Pull-up current	IDx pin enabled (register bit IDx_EN = 1b), VSUP = 5.5V to 18V, WAKE_ID_PU_PD = 10b	-2		-1	mA
ID_{Pd}	Pull-down current (TCAN245xMRHBRQ1 variants)	IDx pin enabled (register bit IDx_EN = 1b), VSUP = 5.5V to 18V, WAKE_IDx_PU_PD = 01b, IDx_PD_VALUE=0b	3		5	mA
ID_{Pd}	Pull-down current	IDx pin enabled (register bit IDx_EN = 1b), VSUP = 5.5V to 18V, WAKE_IDx_PU_PD = 01b, IDx_PD_VALUE=0b	3		5.5	mA
ID_{Pd}	Pull-down current	IDx pin enabled (register bit IDx_EN = 1b), VSUP = 5.5V to 18V, WAKE_IDx_PU_PD = 01b, IDx_PD_VALUE=1b	9		18	mA

6.7 Electrical Characteristics (continued)

Over recommended operating conditions with VSUP/VSUPB/VHSS = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB/VHSS = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d_IDSTAT}	Delay between command via SPI and updated status of ID pin in IDx_STAT register	IDx pin enabled (register bit IDx_EN = 1b with automatic detection) OR WAKE_IDx_PU_PD bit value changed from 00b/01b/10b to 11b	20		30	ms
t_{dCS}	Delay between command via SPI and activation of current source	IDx pin enabled (register bit IDx_EN = 1b). WAKE_IDx_PU_PD bit value changed from 00b to 10b or 01b	0.5		50	µs
SW Input Terminal						
V_{IL}	Low-level input voltage: SW (When VCC1 is present)				0.3	VCC1
V_{IH}	High-level input voltage: SW (When VCC1 is present)		0.7			VCC1
$V_{IHSWINT}$	SW pin high-level input voltage when VCC1 is missing for sleep or fail-safe mode	Register 8'h0E[1] = 1 and/or 8'h0E[2] = 1 and VCC1 missing in sleep or fail-safe mode	1.2			V
$V_{ILSWINT}$	SW low-level input voltage when VCC1 is missing for sleep or fail-safe mode	Register 8'h0E[1] = 1 and/or 8'h0E[2] = 1 and VCC1 missing in sleep or fail-safe mode			0.4	V
$I_{IHSWINT-PD}$	High-level input leakage current for SW pin (active-high) when VCC1 is off	VCC1 off, internal pull-down enabled, (SW_POL_SEL=1b), V_{SW} = 5V	–2.5		125	µA
$I_{ILSWINT-PD}$	Low-level input leakage current for SW pin (active-high) when VCC1 is off	VCC1 off, internal pull-down enabled, (SW_POL_SEL=1b), V_{SW} = 0V	–1		1	µA
$I_{IHSWINT-PU}$	High-level input leakage current for SW pin (active-low) when VCC1 is off	VCC1 off, internal pull-up enabled (SW_POL_SEL= 0b), V_{SW} = 5V	–1		1	µA
$I_{ILSWINT-PU}$	Low-level input leakage current for SW pin (active-low) when VCC1 is off	VCC1 off, internal pull-up enabled (SW_POL_SEL=0b), V_{SW} = 0V	–125		–2	µA
I_{IHSW}	High-level input leakage current for SW pin when VCC1 is on	VCC1 on, internal pull-down enabled, V_{SW}=VCC1	–2		125	µA
I_{ILSW}	Low-level input leakage current for SW pin when VCC1 is on	VCC1 on, internal pull-up enabled, V_{SW}=0V	–125		–2	µA
Rpd	SW pin pull-down resistor		40	60	80	kΩ
Rpu	SW pin Pull-up resistor		40	60	80	kΩ
$I_{LKG(OFF)}$	Unpowered leakage current	Inputs = 5.5V, VCC1 = VSUP = 0V, T_J = -40 to 85°C	–1	0	1	µA
C_{IN}	Input Capacitance				10	pF
VSEL Input Terminal						
$R_{VSEL-SHORT}$	Maximum external resistance between VSEL pin and GND that is detected as short (VCC1 set to 5V)				10	kΩ
$R_{VSEL-OPEN}$	Minimum external resistance between VSEL pin and GND that is detected as open(VCC1 set to 3.3V)		35			kΩ
CTXD, SDI, CLK and nCS Input Terminals						
$I_{LKG(OFF)}$	Unpowered leakage current	Inputs = 5.5V, VCC1 = VSUP = 0V, T_J = -40 to 85°C	–1	0	1	µA
C_{IN}	Input Capacitance			2	10	pF
I_{IH}	High-level input leakage current	VCC1 ± 2%	–1		1	µA
I_{IL}	Low-level input leakage current	Inputs = 0V, VCC1 ± 2%	–125		–2	µA
V_{IH}	High-level input voltage		0.7			VCC1
V_{IL}	Low-level input voltage				0.3	VCC1

6.7 Electrical Characteristics (continued)

Over recommended operating conditions with VSUP/VSUPB/VHSS = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB/VHSS = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{pd}	Internal pull-down resistor at SDI if SDI_POL=0b and SCK if SPI is configured for Mode 0 or Mode1		40	60	80	kΩ
R_{pu}	Internal pull-up resistor at CTXD, nCS, SDI if configured for pull-up (SDI_POL=1b) and SCK if SPI is configured for Mode 2 or Mode 3		40	60	80	kΩ
CRXD, SDO, GFO, nINT Output Terminals						
V_{OH}	HIGH level output voltage	I_{OH} = -2mA	0.8			VCC1
V_{OL}	LOW level output voltage	I_{OL} = 2mA			0.2	VCC1
$I_{LKG(OFF)}$	Unpowered leakage current	VSUP = 0V; VCC1 = 0V; V_O = 0V to 5V	–5		5	µA
nRST Terminal (input/output)						
V_{IH}	High level input switching threshold voltage	Based off of internal voltage	2.1			V
V_{IL}	Low level input switching threshold voltage	Based off of internal voltage			0.8	V
V_{OL}	Low-level output voltage	I_{OL}=1.5mA			0.4	V
I_{OL}	Low-level output current, open drain	nRST = 0.4V	1.5			mA
I_{LKG}	Leakage current, high-level	nRST = VCC1	–5		5	µA
R_{PU}	Pull-up resistance (Output pulled up to VCC1)		10	30	50	kΩ

(1) Selected using Register 8'h12[1:0] default value 10b for WAKE1; Register 8'h2B[5:4] default value 10b for WAKE2; Register 8'h2B[1:0] default value 10b for WAKE3

6.8 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Supply						
t_{PWRUP}	Time after VSUP exceeds UVSUP3R and VCC1> UVCC1. (4)				5	ms
t_{UVFLTR}	Under-voltage detection delay time for VCC1 and VCC2 (4)		25		50	µs
$t_{UVCC1PR}$	Under-voltage filter time for VCC1 pre-warning (4)		2		14	µs
$t_{UVCANFLTR}$	Under-voltage filter time for VCAN (4)		4	10	15	µs
$t_{OVFLTR-VCC1}$	Over-voltage detect filter time on VCC1 (4)		50	60	75	µs
$t_{OVFLTR-VCC2}$	Over-voltage detect filter time on VCC2 (4)		20		40	µs
$t_{OVFLTRVHSS}$	Over-voltage detect filter time on VHSS (4)		4		35	µs
$t_{VSC-VCC1}$	Short to ground on VCC1 detection delay time (4)		75	100	125	µs
$t_{VSC-VCC2}$	Short to ground on VCC2 detection delay time (4)		75	100	125	µs
$t_{ss-VCC2}$	VCC2 soft-start time (4)	V_{CC2} from 0V to 4.5V		0.75	1.25	ms

6.8 Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{REGON}	The short circuit filter time for VCC1 at its startup; VCC1 should clear short-circuit threshold before this timer expires. (4)	See Figure 7-14	3	3.4	3.8	ms
t_{VCC2ON}	The short circuit filter time for VCC2 at its startup; VCC2 should clear short-circuit threshold before this timer expires. (4)	See Figure 7-14	3	3.4	3.8	ms
t_{REGOFF}	Time VCC1 is off in fail-safe mode before accepting wake events and checking for fault conditions (4)	Time VCC1 is off in fail-safe mode before accepting wake events and checking for fault conditions	250	300	350	ms
Buck Regulator						
t_{ON-MIN}	Minimum switch on-time (4)	I_{CC1} = 1A		70		ns
$t_{OFF-MIN}$	Minimum switch off-time (4)	I_{CC1} = 1A		125		ns
t_{ON-max}	Maximum switch on-time (4)			7.5		µs
D_{MAX}	Maximum switch duty cycle (4)			98		%
$t_{ss-VCC1}$	VCC1 soft-start time	V_{CC1} from 0V to 90% of V_{CC1}		1.8	2.1	ms
f_{SW}	Switching Frequency, register setting 1 (4)	BUCK_FSW Register field 65h[5:4] = 00b	1.62	1.8	2.1	MHz
f_{SW}	Switching Frequency, register setting 2 (4)	BUCK_FSW Register field 65h[5:4] = 01b	1.8	2.0	2.3	MHz
f_{SW}	Switching Frequency, register setting 3, default setting (4)	BUCK_FSW Register field 65h[5:4] = 10b	1.98	2.2	2.42	MHz
f_{SW}	Switching Frequency, register setting 4 (4)	BUCK_FSW Register field 65h[5:4] = 11b	2.1	2.4	2.7	MHz
f_{SS-MOD}	Spread Spectrum Modulation Frequency, Setting 1 (4)	SS_MOD_FREQ Register field 65h[7:6]=00b		0		%
f_{SS-MOD}	Spread Spectrum Modulation Frequency, Setting 2 (4)	SS_MOD_FREQ Register field 65h[7:6]=01b (6)		4		%
f_{SS-MOD}	Spread Spectrum Modulation Frequency, Setting 3 (4)	SS_MOD_FREQ Register field 65h[7:6]=10b (6)		8		%
Mode Change						
$t_{MODE\_STBY\_NOM\_CTRX}$	CAN transceiver state change time based upon SPI write from off or wake capable to on or listen state where CRXD mirror CAN bus (4)	CAN transceiver state change time based upon SPI write from off or wake capable to on or listen state where CRXD mirrors CAN bus			20	µs
$t_{MODE\_NOM\_SLP}$	Time from SPI sleep command where CAN transceiver is off and CRXD doesn't reflect the bus (4)	See Figure 7-15			5	µs
$t_{MODE\_NOM\_STBY}$	SPI write to go to standby from normal mode (4)	See Figure 7-16			5	µs
Device Timing						
t_{RSTN_act}	Time required for VCC1 ≥ UVCC1 to leave Restart mode (4)	reg 29h[5] = 0b (default); See Figure 7-13, Figure 7-14, Figure 8-16 and Figure 10-3 as examples	1.5	2	2.5	ms
t_{RSTN_act}	Time required for VCC1 ≥ UVCC1 to leave Restart mode (4)	reg 29h[5] = 1b; See Figure 7-13, Figure 7-14, Figure 8-16 and Figure 10-3 as examples	10	15	20	ms

6.8 Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{NRSTIN}	Input pulse required on the nRST pin to recognize a device reset (4)	See Figure 8-59.	75	100	125	µs
t_{RSTTO}	Restart timer timeout. Time required after UVCC1 event before the device enters fail-safe mode (if enabled) or Sleep mode (if fail-safe mode disabled) (4)		120	150	180	ms
t_{NRST_TOG}	nRST output pulse width (4)	reg 29h[5] = 0, see Figure 8-59	1.5	2	2.5	ms
		reg 29h[5] = 1, see Figure 8-59	10	15	20	ms
$t_{WK\_TIMEOUT}$	Bus wake-up timeout value(4)	See Figure 8-16	0.8		2	ms
t_{WK_FILTER}	Bus time to meet filtered bus requirements for wake up request	See Figure 8-16	0.5		0.95	µs
$t_{WK\_WIDTH\_MIN}$ (2) (3) (5)	Minimum WAKE Pin pulse width (4)	WAKE_WIDTH_INVALID = 00b; See Figure 8-20 and Figure 8-21	10			ms
		Minimum WAKE Pin pulse width WAKE_WIDTH_INVALID = 01b; See Figure 8-20 and Figure 8-21	20			ms
		Minimum WAKE Pin pulse width WAKE_WIDTH_INVALID = 10b; See Figure 8-20 and Figure 8-21	40			ms
		Minimum WAKE Pin pulse width WAKE_WIDTH_INVALID = 11b; See Figure 8-20 and Figure 8-21	80			ms
$t_{WK\_WIDTH\_INVALID}$ (2) (3) (5)	Maximum WAKE Pin pulse width that is considered invalid (4)	WAKE_WIDTH_INVALID = 00b; See Figure 8-20 and Figure 8-21			5	ms
		Maximum WAKE Pin pulse width that is considered invalid WAKE_WIDTH_INVALID = 01b; See Figure 8-20 and Figure 8-21			10	ms
		Maximum WAKE Pin pulse width that is considered invalid WAKE_WIDTH_INVALID = 10b; See Figure 8-20 and Figure 8-21			20	ms
		Maximum WAKE Pin pulse width that is considered invalid WAKE_WIDTH_INVALID = 11b; See Figure 8-20 and Figure 8-21			40	ms
$t_{WK\_WIDTH\_MAX}$ (2)	Maximum WAKE Pin pulse window (4)	WAKE_WIDTH_MAX = 00b; See Figure 8-20	750		950	ms
		Maximum WAKE Pin pulse window WAKE_WIDTH_MAX = 01b; See Figure 8-20	1000		1250	ms
		Maximum WAKE Pin pulse window WAKE_WIDTH_MAX = 10b; See Figure 8-20	1500		1875	ms
		Maximum WAKE Pin pulse window WAKE_WIDTH_MAX = 11b; See Figure 8-20	2000		2500	ms

6.8 Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{WK_CYC}	t_{WK_CYC} (4)	Sampling window for cyclic sensing; Standby or Sleep mode, Register 8'h12[5] = 0b; see Figure 8-23	10	25	35	µs
		Sampling window for cyclic sensing; Standby or Sleep mode, Register 8'h12[5] = 1b; see Figure 8-23	55	70	85	µs
$t_{SILENCE\_CAN}$	$t_{SILENCE\_CAN}$ (4)	Timeout for bus inactivity Timer is reset and restarted, when bus changes from dominant to recessive or vice versa.	0.6		1.2	s
$t_{INACTIVE}$	$t_{INACTIVE}$ (4)	SWE timer used for fails-safe and mode inactivity. Can be programmed to different values using register 8'h1C[6:3]	4	5	6	min
t_{Bias}	t_{Bias} (4)	Time from the start of a dominant-recessive-dominant sequence. Each phase 6µs until Vsym ≥ 0.1. See Figure 7-10			250	µs
t_{SW}	SW pin filter time for a state change to be recognized (4)	SW pin filter time for a state change to be recognized	130			µs
t_{INITWD}	Initial long window for watchdog (4)	Initial long window for watchdog, see Figure 8-43	127	150	173	ms
		WD_CONFIG_1 register 8'h13[1:0] = 01b; see Figure 8-42	255	300	345	ms
		WD_CONFIG_1 register 8'h13[1:0] = 10b (default); see Figure 8-42	510	600	690	ms
		WD_CONFIG_1 register 8'h13[1:0] = 11b; see Figure 8-42	850	1000	1150	ms
t_{CTXD_DTO}	t_{CTXD_DTO} (4)	Dominant time out (1) See , R_L = 60Ω, C_L = open; See Figure 7-7	1		5	ms
t_{TOGGLE}	t_{TOGGLE} (4)	CRXD pin toggle timing when programmed after a WUP; See Figure 8-16	5	10	15	µs
$t_{WD\text{-}ACC}$	Timeout watchdog timing accuracy(4)	Timeout watchdog enabled. Typical values for watchdog timer selected per Table 8-16	–15	tWD	15	%
$f_{PWM\text{-}ACC}$	HSS1-4 PWM Frequency accuracy (4)	HSS set to PWM and PWM frequency set to 200Hz or 400Hz per PWMx_FREQ bit	–10		10	%
$t_{WD\text{-}ACC}$	Window and Q&A watchdog timing accuracy (4)	Window watchdog or Q&A watchdog enabled. Typical values for watchdog timer selected per Table 8-16	–10	tWD	10	%
t_{TMRACC}	Timer1, Timer2 period/on-time accuracy OR SWE timer accuracy(4)	Typical value of Timer1 or Timer2 configured per register 8'h25 (TIMER1_CONFIG) or 8'h26 (TIMER2_CONFIG); Typical value of SWE timer configured per 8'h25 (SWE_TIMER_SET)	–15		15	%
$F_{OSC\text{-}16M}$	16MHz clock frequency		15.36	16	16.64	MHz
$F_{OSC\text{-}1M}$	1MHz clock frequency		0.94	1.04	1.14	MHz
$F_{OSC\text{-}10k}$	10kHz clock frequency		8.8	10.4	12	kHz

(1) The CTXD dominant time out (t_{CTXD_DTO}) disables the driver of the transceiver once the CTXD has been dominant longer than t_{CTXD_DTO}, which releases the CAN bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after CTXD has been returned HIGH (recessive). While this protects the CAN bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on CTXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This,

along with the t_{CTXD_DTO} minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11÷ t_{CTXD_DTO} = 11 bits ÷ 1.2ms = 9.2kbps.

(2) This parameter is valid only when register 11h[7:6] = 11b

(3) This is the minimum pulse width for a WAKE pin input that device detects as a good pulse. Values between the minimum $t_{WK_WIDTH_MIN}$and maximum $t_{WK\_WIDTH\_INVALID}$ is indeterminate and is or is not considered as valid.

(4) Specified by design

(5) This parameter is set based upon the programmed value for $t_{WK\_WIDTH\_INVALID}$ register 11h[3:2]

(6) Not applicable for devices with REV_ID=20h

6.9 Switching Characteristics

Over recommended operating conditions with VSUP/VSUPB = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmitter and Receiver Characteristics						
$t_{prop(TxD-busrec)}$	Propagation delay time, low-to-high CTXD edge to driver recessive (dominant to recessive)	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open; See Figure 7-4		50	80	ns
$t_{prop(TxD-busdom)}$	Propagation delay time, high-to-low CTXD edge to driver dominant (recessive to dominant)			50	80	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{prop(TxD-busrec)} - t_{prop(TxD-busdom)} \rvert$)			10	25	ns
t_R	Differential output signal rise time:			30	50	ns
t_F	Differential output signal fall time:			35	55	ns
$t_{prop(busrec-RXD)}$	Propagation delay time, bus recessive input to CRXD high output (dominant to recessive)	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open, C_{RXD} = 15pF see Figure 7-5		75	110	ns
$t_{prop(busdom-RXD)}$	Propagation delay time, bus dominant input to CRXD low output (recessive to dominant)			75	110	ns
t_{LOOP}	Loop Delay(1)	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, C_{RXD} = 15pF, VCC1 ± 2%, see Section 7			170	ns
CAN FD timing characteristics according to ISO 11898-2:2024 including Signal Improvement Characteristics (SIC); $t_{bit(TXD)}$ ≥ 125ns. Typical conditions: R_L = 45Ω to 65Ω, C_L = 100pF, C_{CRXD} = 15pF; See Section 7						
$t_{\Delta Bit(Bus)}$	Transmitted bit width variation	Bus recessive bit length variation relative to TXD bit length, $\Delta t_{Bit(Bus)}$ = $t_{Bit(Bus)}$ - $t_{Bit(TXD)}$	–10		10	ns
$t_{\Delta Bit(RXD)}$	Received bit width variation	RXD recessive bit length variation relative to TXD bit length, $\Delta t_{Bit(RXD)}$ = $t_{Bit(RXD)}$ - $t_{Bit(TXD)}$	–30		20	ns
$t_{\Delta REC}$	Receiver timing symmetry	RXD recessive bit length variation relative to bus bit length, Δt_{REC} = $t_{Bit(RXD)}$ - $t_{Bit(Bus)}$	–20		15	ns
t_{REC_START}	Delay time from TXD rising edge to the start of passive recessive phase	See Figure 7-17			530	ns
t_{SIC_START}	Delay time from TXD rising edge to the start of active recessive phase				120	ns
t_{SIC_END}	Delay time from TXD rising edge to the end of active recessive phase		355			ns
SPI Switching Characteristics						
f_{SCK}	SPI clock frequency (2)	Normal and standby modes, Sleep mode - if VCC1 is present, if register BYTE_CNT, 09h[3]=0b (single byte mode)			4	MHz
f_{SCK}	SPI clock frequency (2)	Normal and standby modes, Sleep mode - if VCC1 is present, if register BYTE_CNT, 09h[3]=1b (two-byte mode)			2	MHz
t_{SCK}	SPI clock period (2)	Normal and standby modes and Sleep mode - if VCC1 is present; if register BYTE_CNT, 09h[3]=0b (single byte mode) See Figure 7-12	250			ns
t_{SCK}	SPI clock period (2)	Normal and standby modes and Sleep mode - if VCC1 is present; if register BYTE_CNT, 09h[3]=1b (two-byte mode) See Figure 7-12	500			ns

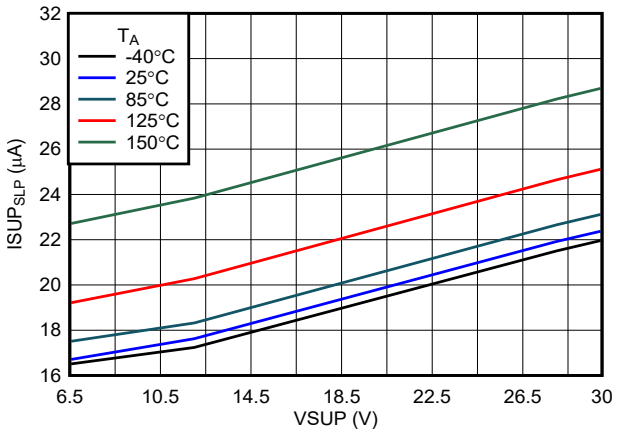
6.9 Switching Characteristics (continued)

Over recommended operating conditions with VSUP/VSUPB = 5.5V to 28V unless otherwise noted. All typical values are specified at T_J = 25°C, VSUP/VSUPB = 12V, VCAN = 5V and R_L = 60Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SCKR}	SPI clock rise time (2)	Normal and standby modes and Sleep mode - if VCC1 is present; See Figure 7-11			40	ns
t_{SCKF}	SPI clock fall time (2)	Normal and standby modes and Sleep mode - if VCC1 is present; See Figure 7-12			40	ns
t_{SCKH}	SPI clock high (2)	Normal and standby modes and Sleep mode - if VCC1 is present; if register BYTE_CNT, 09h[3]=0b (single byte mode) See Figure 7-12	125			ns
t_{SCKH}	SPI clock high (2)	Normal and standby modes and Sleep mode - if VCC1 is present; if register BYTE_CNT, 09h[3]=1b (two-byte mode) See Figure 7-12	250			ns
t_{SCKL}	SPI clock low (2)	Normal and standby modes and Sleep mode - if VCC1 is present; if register BYTE_CNT, 09h[3]=0b (single byte mode) See Figure 7-12	125			ns
t_{SCKL}	SPI clock low (2)	Normal and standby modes and Sleep mode - if VCC1 is present; if register BYTE_CNT, 09h[3]=1b (two-byte mode) See Figure 7-12	250			ns
t_{nCSS}	nCS chip select setup time (2)	Normal and standby modes and Sleep mode - if VCC1 is present; See Figure 7-12	100			ns
t_{nCSH}	nCS chip select hold time (2)	Normal and standby modes and Sleep mode - if VCC1 is present; See Figure 7-12	100			ns
t_{nCSD}	nCS chip select disable time (2)	Normal and standby modes and Sleep mode - if VCC1 is present; See Figure 7-11	50			ns
t_{SISU}	Data in setup time (2)	Normal and standby modes and Sleep mode - if VCC1 is present; See Figure 7-11	50			ns
t_{SIH}	Data in hold time (2)	Normal and standby modes and Sleep mode - if VCC1 is present; See Figure 7-11	50			ns
t_{SOV}	Data out valid (2)	Normal and standby modes and Sleep mode - if VCC1 is present; See Figure 7-12			80	ns
t_{RSO}	SDO rise time (2), C_{LOAD} <= 20pF	Normal and standby modes and Sleep mode - if VCC1 is present; See Figure 7-12			40	ns
t_{FSO}	SDO fall time (2),C_{LOAD} <= 20pF	Normal and standby modes and Sleep mode - if VCC1 is present; See Figure 7-12			40	ns

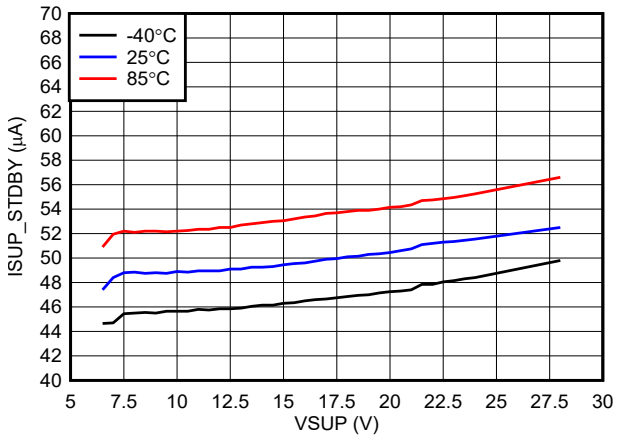
(1) Time span from signal edge on TXD input to next signal edge with same polarity on RXD output, the maximum of delay of both signal edges is to be considered.
(2) Specified by design

6.10 Typical Characteristics



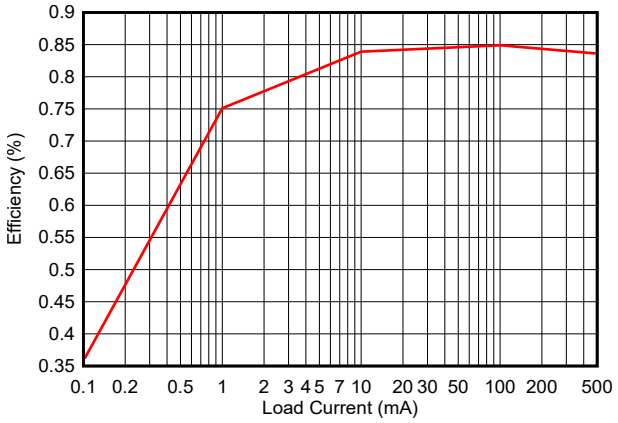
WAKE pin active, floating | CAN = off | Cyclic sensing = off
Cyclic wake = off | VCC1 = off | Selective wake = off

Figure 6-1. Sleep Mode Battery Current Consumption vs. VSUP and Temperature



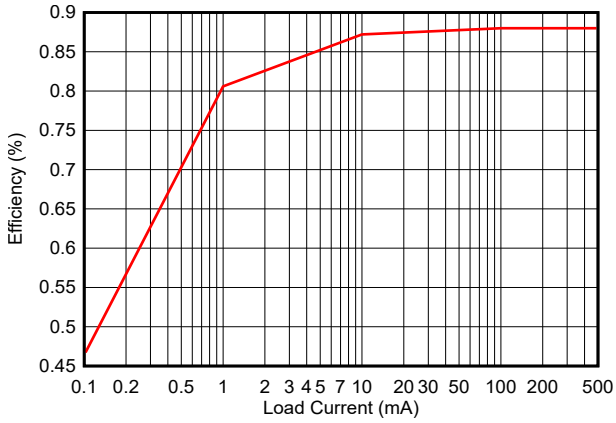
Wake pins disabled | CAN = off | Cyclic sensing = off
Cyclic wake = off | WD = off | Selective wake = off

Figure 6-2. Standby Mode Battery Current Consumption vs. VSUP and Temperature



T_A = 25°C

Figure 6-3. VCC1 Buck Converter Efficiency (VCC1 = 3.3V) in Auto Mode



T_A = 25°C

Figure 6-4. VCC1 Buck Converter Efficiency (VCC1 = 5V) in Auto Mode

7 Parameter Measurement Information

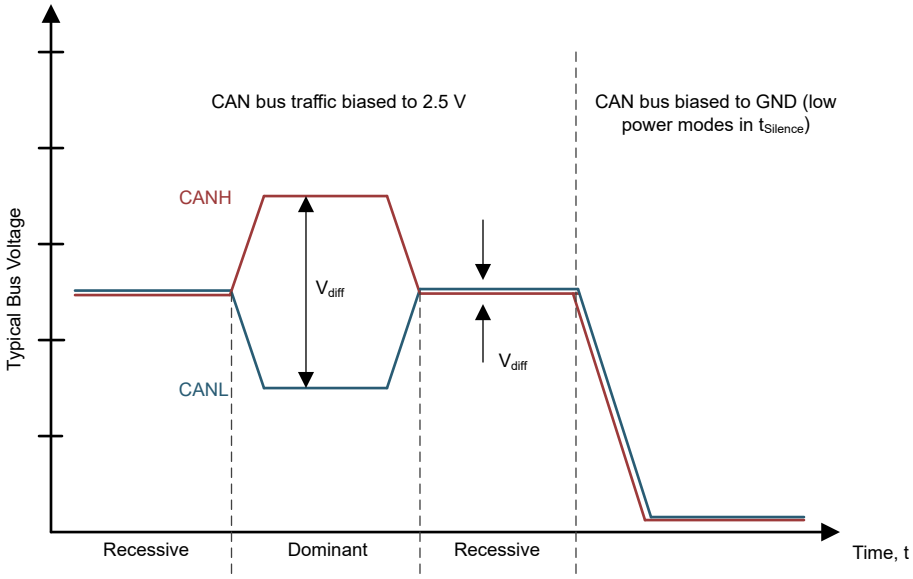
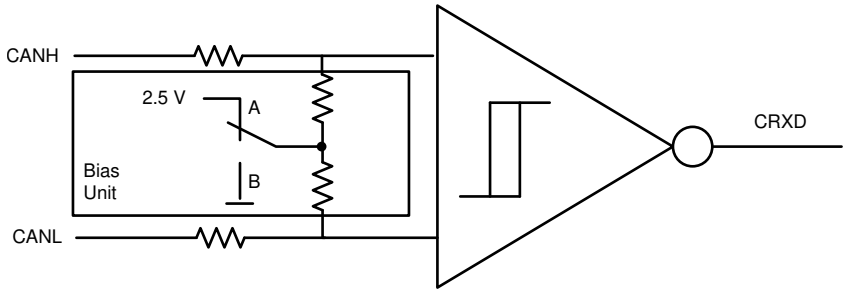


Figure 7-1. Bus States (Physical Bit Representation)



A. Normal, Listen Modes
B. Standby and Sleep Modes (Low Power)

Figure 7-2. Simplified Recessive Common Mode Bias Unit and Receiver

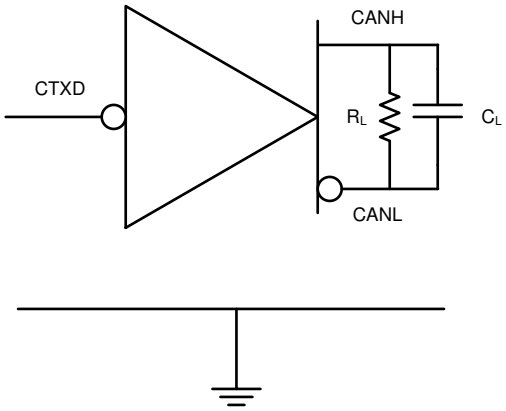


Figure 7-3. Supply Test Circuit

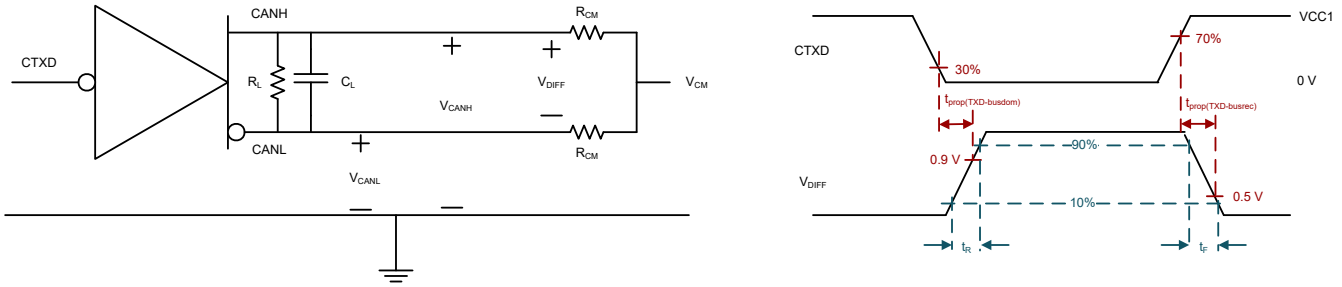


Figure 7-4. Driver Test Circuit and Measurement

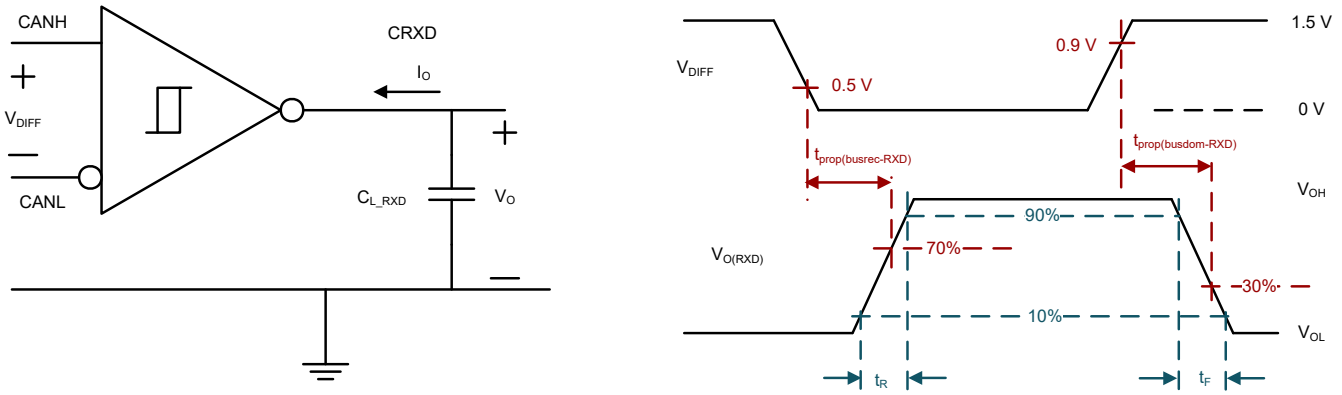


Figure 7-5. Receiver Test Circuit and Measurement

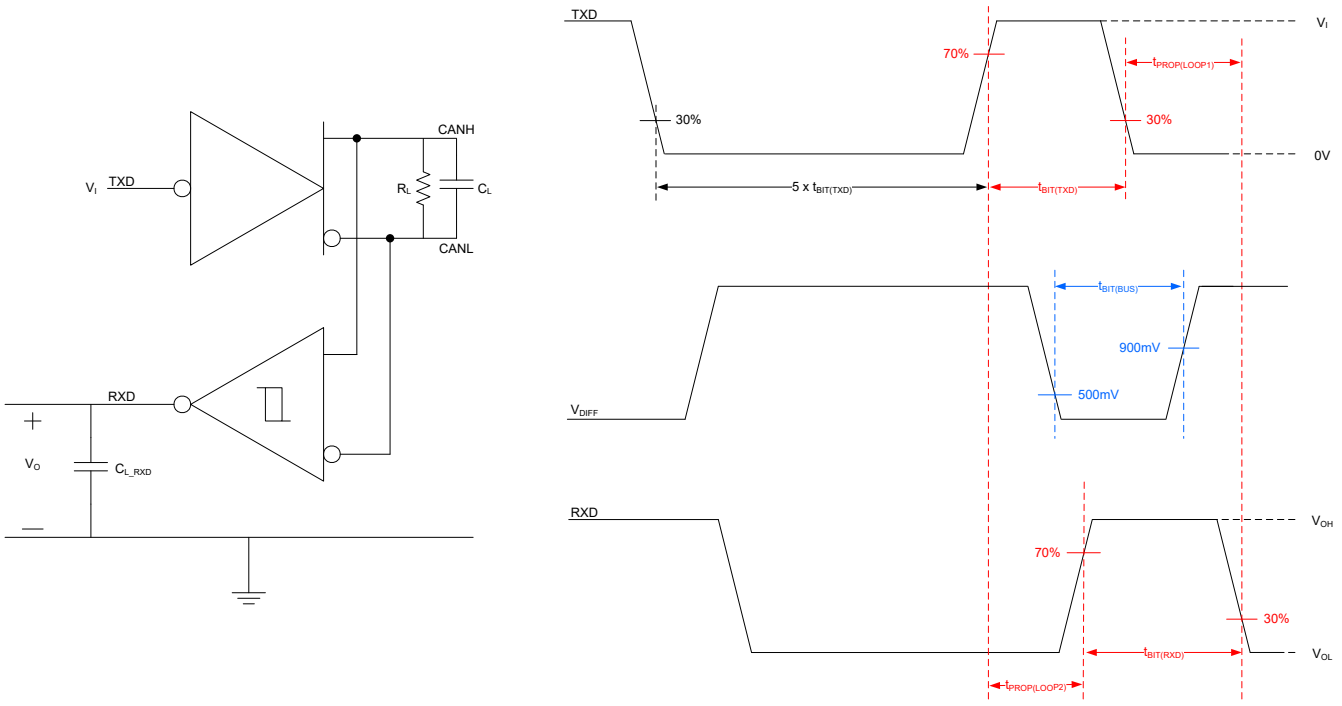


Figure 7-6. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

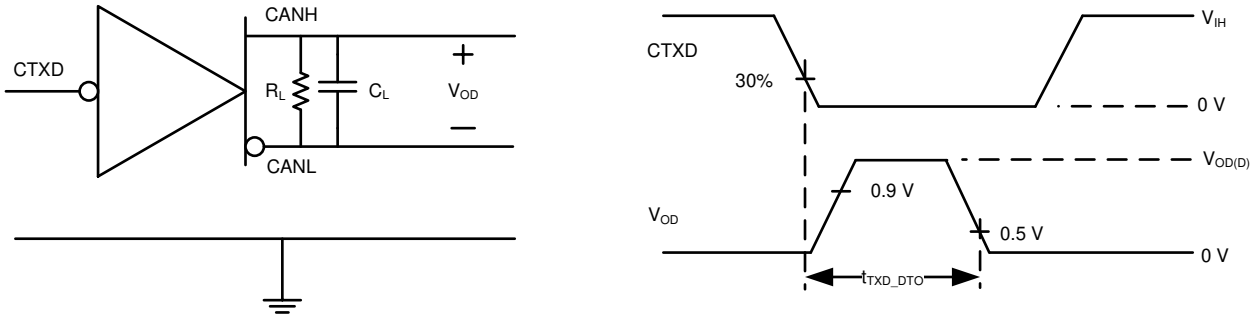


Figure 7-7. TXD Dominant Time Out Test Circuit and Measurement

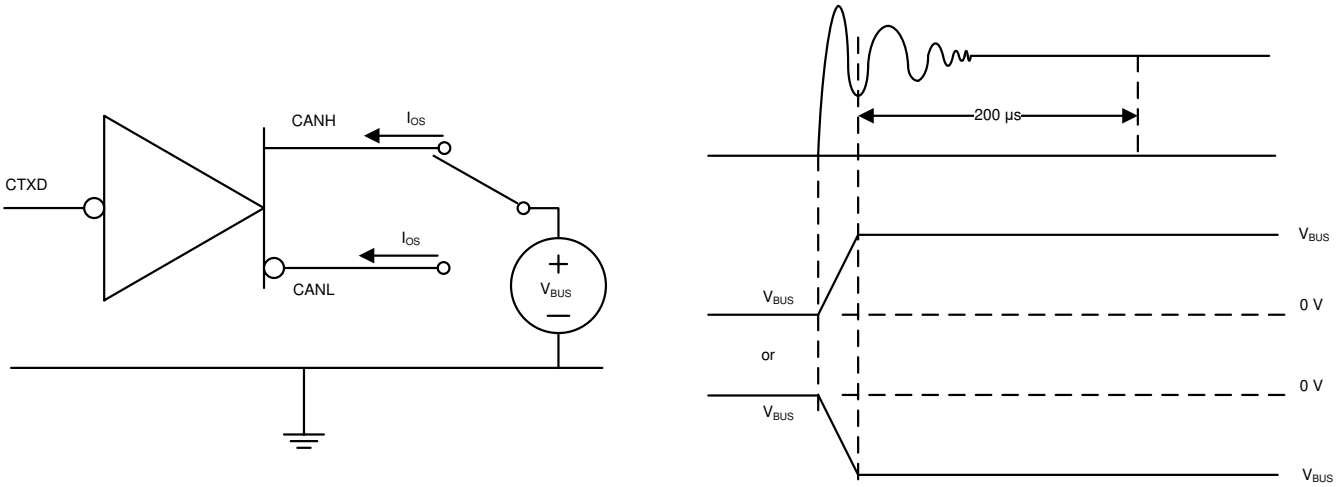


Figure 7-8. Driver Short-Circuit Current Test and Measurement

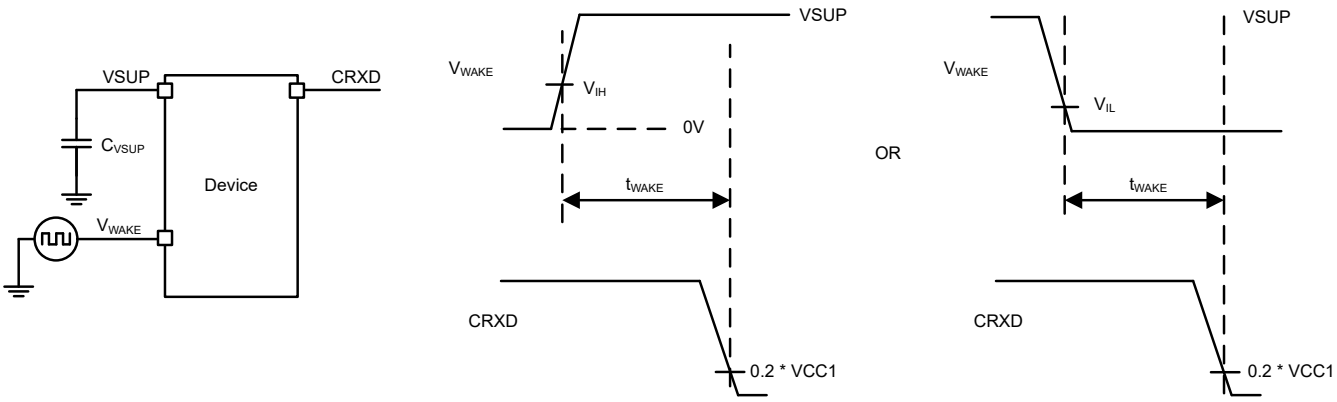


Figure 7-9. t_{WAKE} While Monitoring RXD Output

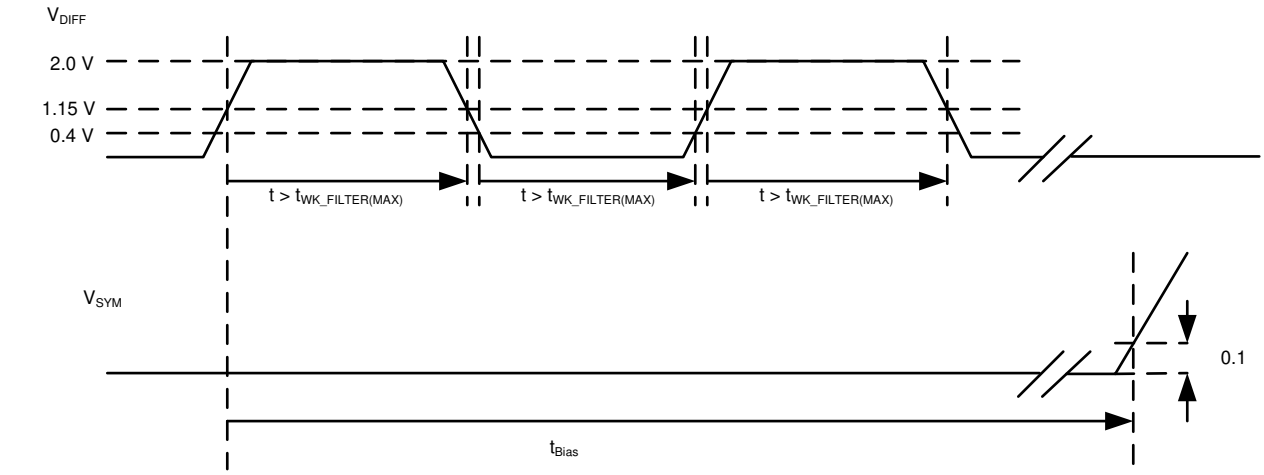


Figure 7-10. Test Signal Definition for Bias Reaction Time Measurement

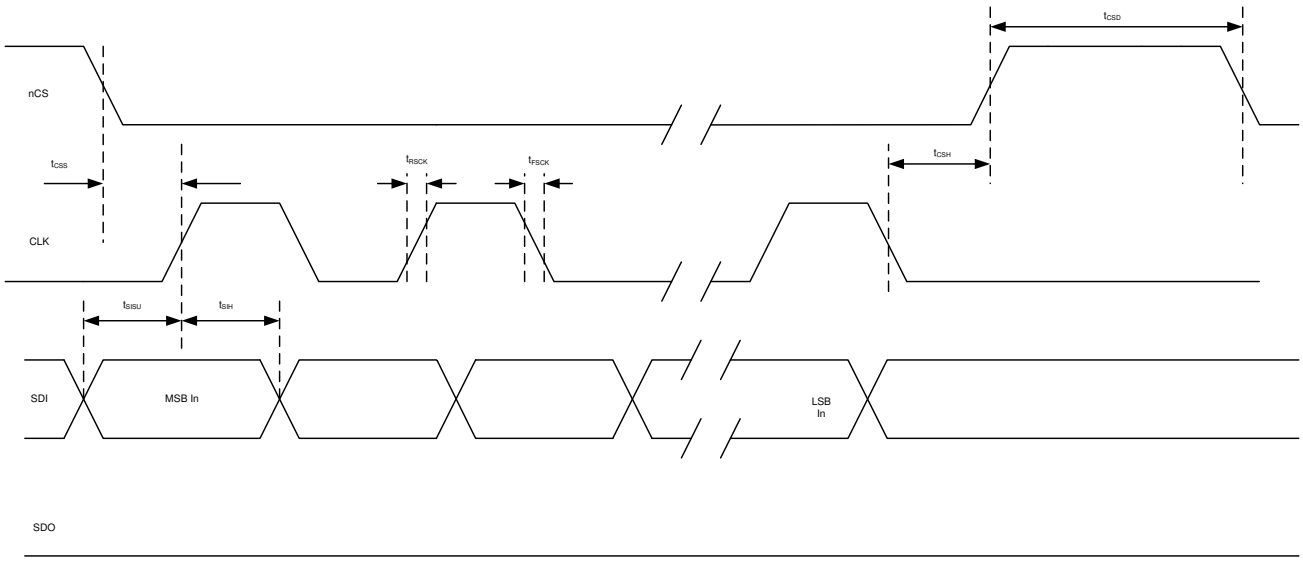


Figure 7-11. SPI AC Characteristic Write

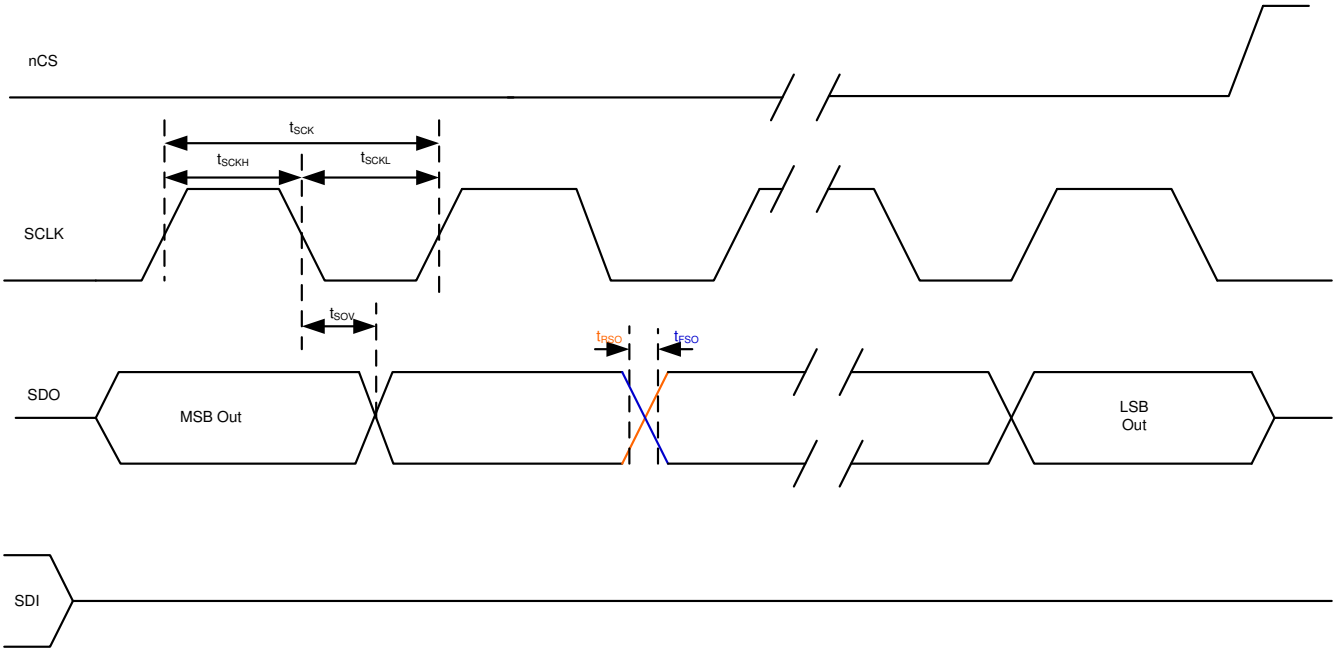


Figure 7-12. SPI AC Characteristic Read

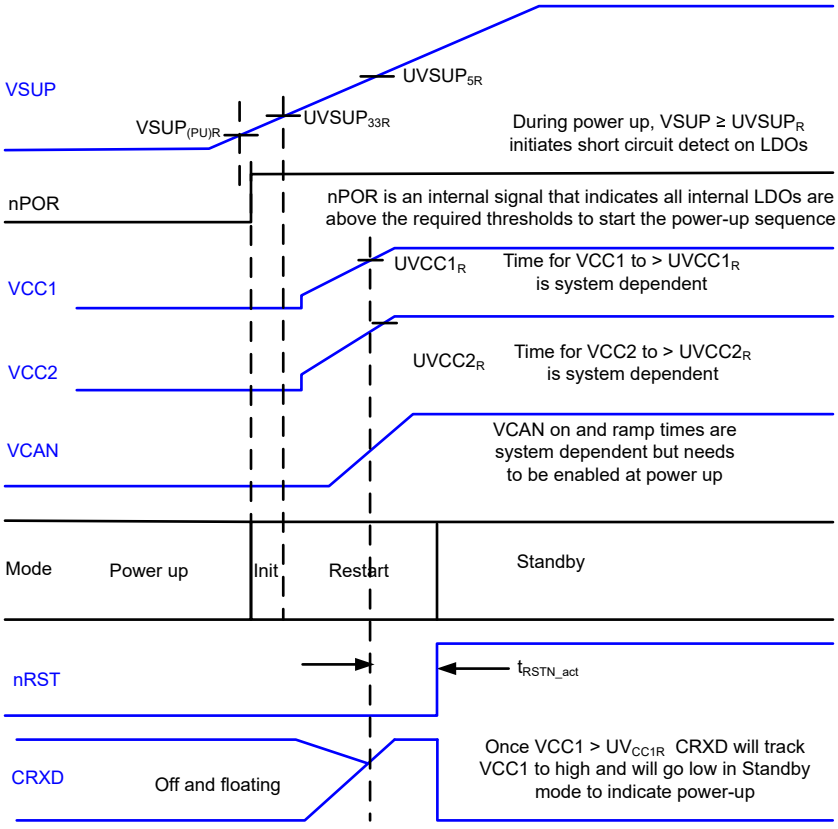


Figure 7-13. Power Up Timing

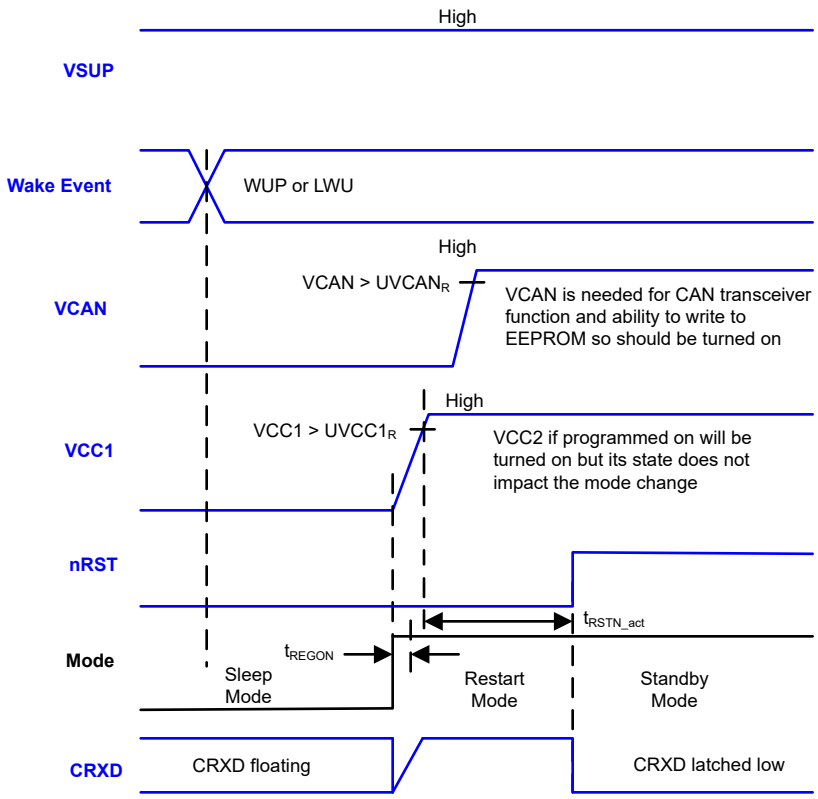


Figure 7-14. Sleep to Restart Timing

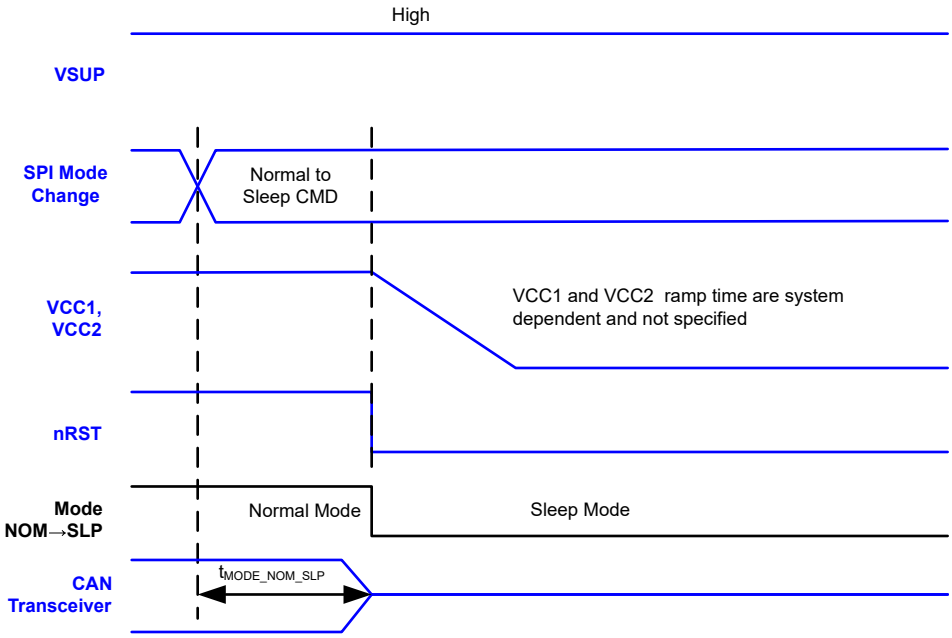


Figure 7-15. Normal to Sleep Timing

A. VCC1 and VCC2 turn-off in Sleep mode if configured to be device-mode dependent (off in Sleep mode). Please note VCC1 and VCC2 can be configured to stay on in Sleep mode.
B. The blue signals are input or output of the TCAN245x-Q1 and the black signals are internal to the TCAN245x-Q1. This is for the timing diagrams Figure 7-13 , Figure 7-14, Figure 7-15, Figure 7-16.

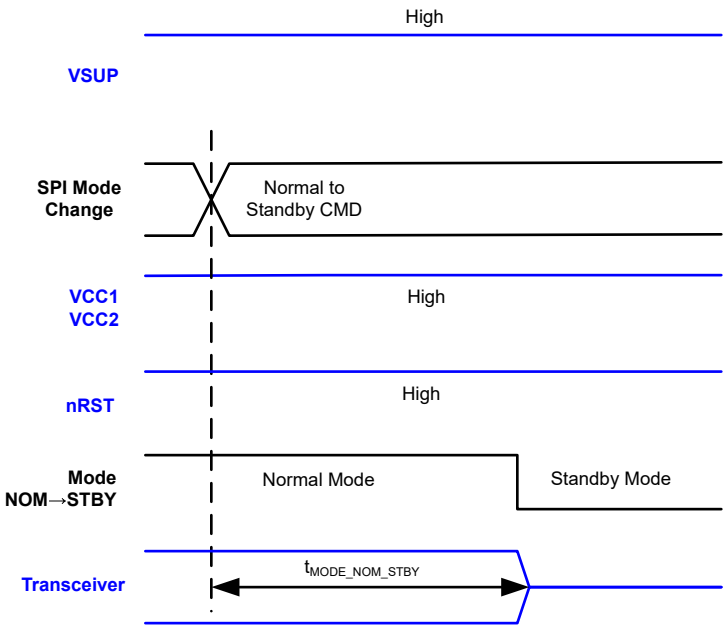


Figure 7-16. Normal to Standby Timing

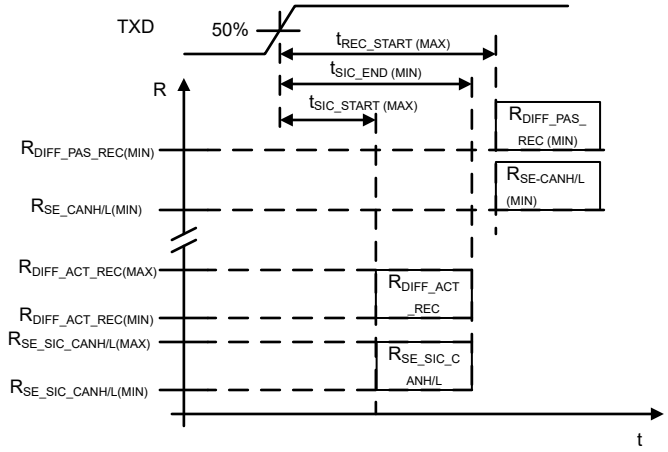


Figure 7-17. Resistance Value During Active Recessive Phase for Signal Improvement Capability

8 Detailed Description

8.1 Overview

The TCAN245x-Q1 family of system basis chips (SBC) integrates the CAN FD transceiver. The CAN FD transceiver supports data rates up to 5Mbps while meeting the high-speed CAN physical layer standards: ISO 11898-2:2024. TCAN2451-Q1 supports selective wake-up on dedicated CAN-frames. The device can wake up with remote wake up using CAN bus implementing the ISO 11898-2:2024 Wake Up Pattern (WUP). The device has a serial peripheral interface (SPI) that connects to a local microprocessor for configuration. The SPI supports clock rates up to 4MHz. The device provide a software development pin to help implementer with development. In this mode, the watchdog is still active but only sets a flag.

The devices provides a V_{CC1} of either 3.3V or 5V output depending upon the VSEL pin connection and supports loads up to 1A. The devices have a separate 5V LDO, V_{CC2}, that provides up to 200mA externally and is short to battery protected. Use a 5V input supply, VCAN, for the CAN FD transceiver.

8.2 Functional Block Diagram

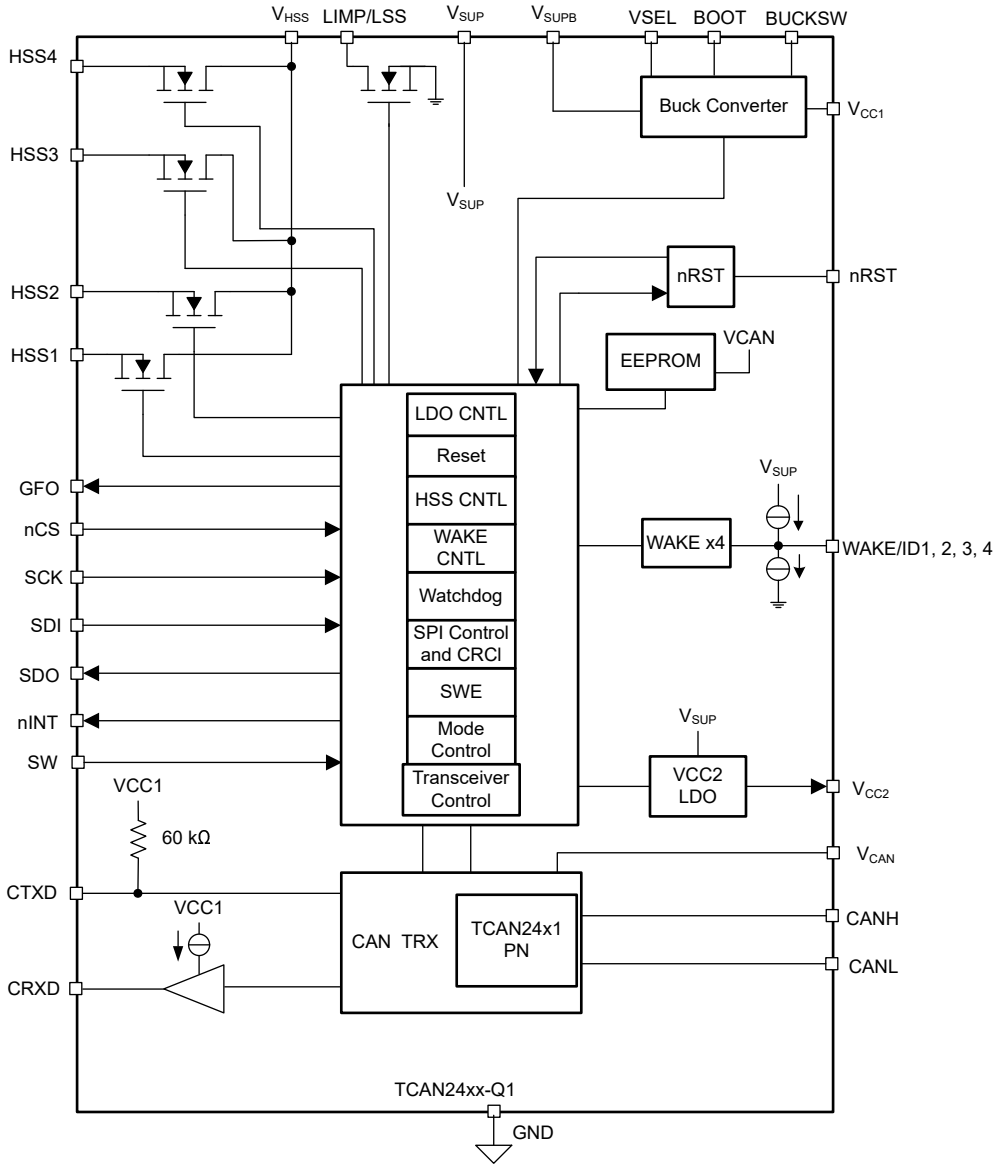


Figure 8-1. TCAN245x-Q1 Functional Block Diagram

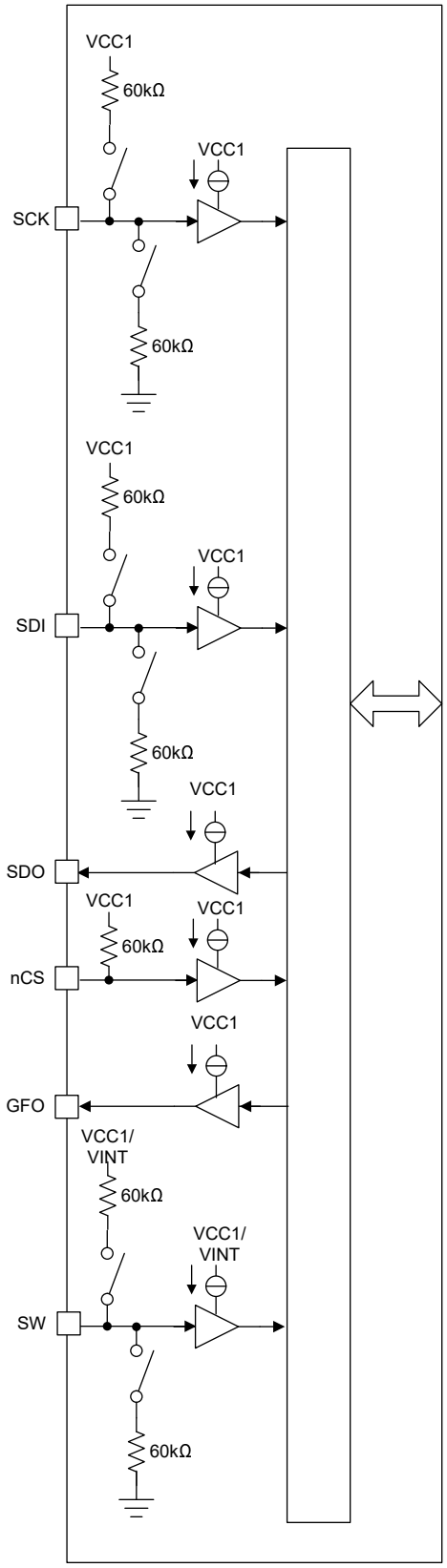


Figure 8-2. Digital Input/output Block Diagram

8.3 Feature Description

8.3.1 CAN FD Transceiver

Figure 8-3 shows the block diagram for the CAN FD Transceiver.

The CTXD is the input to the CAN FD transmitter from the processor that controls the state of the CAN FD bus. When CTXD is low, the bus output is dominant. When CTXD is high, the bus output is recessive, which is a logic 0. The CTXD input structure is compatible with processors with 3.3V to 5V V_O. CTXD has an internal pull-up resistor to VCC1. The bus is protected from being stuck dominant through a system failure driving CTXD low through the dominant state time-out timer.

CRXD is the output of the CAN FD receiver. When a CAN wake event takes place the CRXD pin is latched low. CRXD also indicates the local wake up (LWU) from the high voltage WAKE pins. The CRXD is a push-pull output buffer and, as such, an external pull-up is not needed. In restart mode, the RXD pins drive high. When VCC1 is > UVCC1 for t_{RSTN_act}, the device automatically transition to standby mode. The CRXD pin pulls low to indicate a wake up request. Program the CRXD pin to toggle low or high with a pulse width of t_{TOGGLE}, see Figure 8-16 as an example of this feature.

The VCAN pin is the 5V supply input for the CAN FD transceiver. VCAN is monitored for under-voltage events, UVCAN. When VCAN is present and not in a fault state, register 8'h4F[1], VCAN_STATUS, is set to 1b. For the CAN FD transceiver to be available, VCAN must be present. This pin is also used for EEPROM writing so must be on for this function to happen.

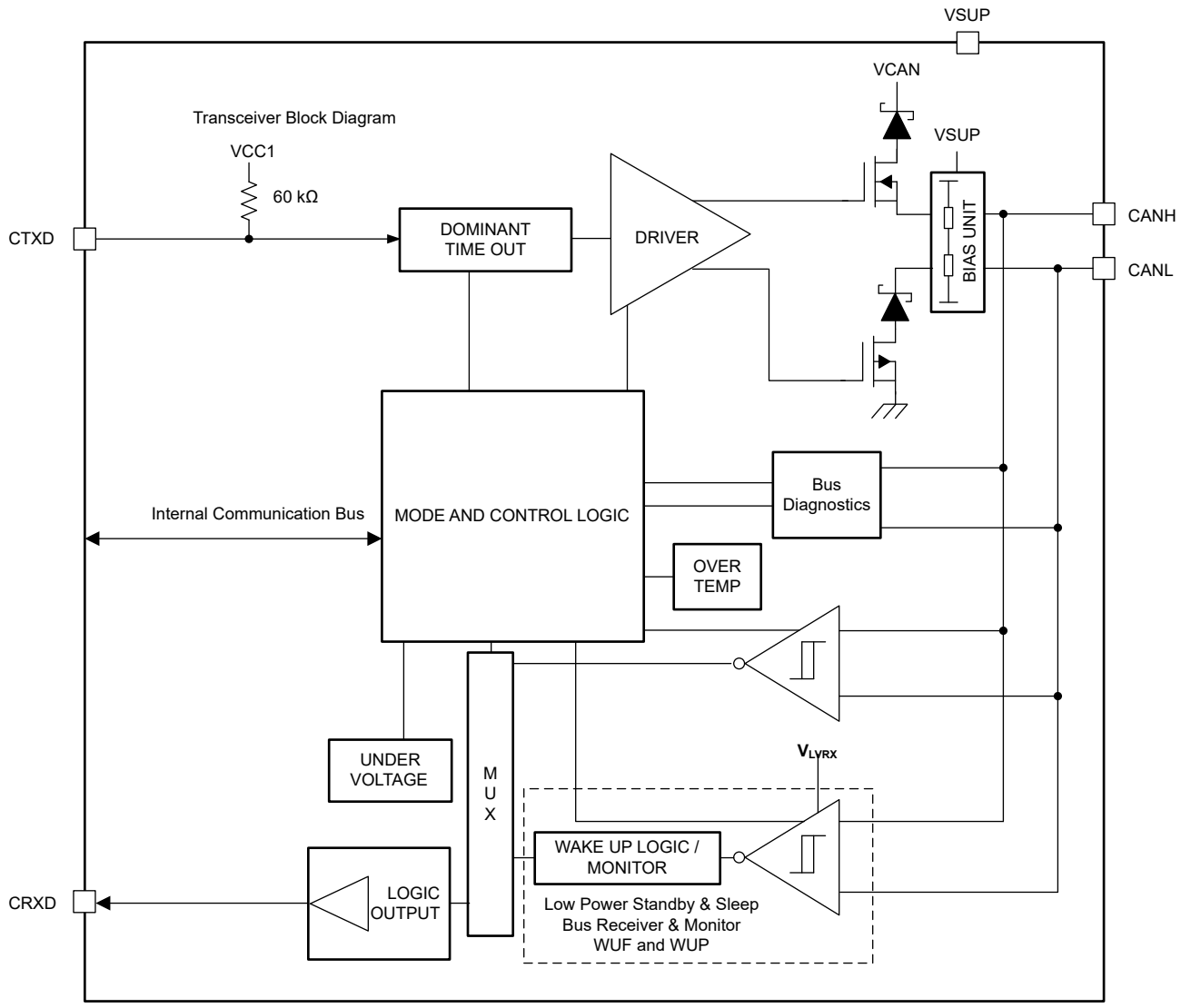


Figure 8-3. CAN Transceiver Block Diagram

Separately program the CAN FD outside of the SBC mode control or tied to the SBC mode control. When tied to the SBC mode control, changing the SBC mode to normal mode automatically changes the transceivers to ON state. All other states are wake capable. When programmed separately than the SBC modes, there are certain states that the transceivers cannot be in for the mode. If a mode change initiates and the transceiver is not in an allowed state, the mode change does not take place, and the MODE_ERR interrupt at 8'h5A[3] is set to 1b. Similarly, if the transceiver state changes to a state not allowed in an SBC mode, the state change does not happen and the MODE_ERR interrupt at 8'h5A[3] is set to 1b. Here are a few specific cases for consideration.

- A transceiver in Normal mode configured for listen, wake capable and off can transition to standby mode, and the state is the same.
- Transitioning to restart mode is wake capable unless the transceiver is programmed off.
- Transitioning from restart mode to standby mode is wake capable unless the transceiver is programmed off.
- When using the SWE timer and the timer times out, the transceivers automatically become wake capable when entering sleep mode or fail-safe mode.

Note

If the device is in SBC normal mode and the transceivers are programmed on, the CTXD pin is checked. If the CTXD pin is dominant, the transceiver does not turn on the transmitter until the CTXD pin has transitioned to recessive.

The CAN FD transceiver supports off, on, listen, and wake capable. The state of the transceiver is programmed using register 8'h10[2:0]. On represents normal mode for a stand-alone transceiver. The CAN transceiver defaults to wake capable when entering fail-safe mode, but can be disabled for this mode by using CAN1_FSM_DIS at register 8'h10[3] = 1b.

The V_{CAN} pin is the 5V supply input for the CAN FD transmitter. V_{CAN} is monitored for under-voltage events, UVCAN. When V_{CAN} is present and not in a fault state, register 8'h4F[1], VCAN_STATUS, is set to 1b. For the CAN FD transmitter to be available, VCAN must be present. This pin is also used for EEPROM writing, and VCAN must be present for this function.

When a CAN wake event takes place the CRXD pin is latched low. CRXD also indicates wake up due to WAKEx pins. CRXD pin is a push-pull output and as such an external pull-up is not needed. In restart mode, the CRXD pin is driven high. When VCC1 is > UVCC1 for t_{RSTN_act}, the device automatically transition to standby mode. The CRXD pin is then pulled low to indicate a wake up request. Program the CRXD pin to toggle low or high with a pulse width of t_{TOGGLE}, see Static Wake as an example of this feature.

Table 8-1. CAN FD Transceiver Programmable State by SBC Mode

SBC Mode	On	Listen	Wake Capable	Off	SBC Mode Control
Normal	✓	✓	✓	✓	On
Standby		✓	✓	✓	Wake Capable
Sleep			✓ default	✓	Wake Capable
Restart			✓ default	✓	Wake Capable
Fail-safe			✓ default	✓	Wake Capable

Note

- When entering SBC restart mode, the transceiver changes to wake capable
- When entering SBC fail-safe mode, the transceiver defaults to wake capable.

8.3.1.1 Driver and Receiver Function

The CTXD and CRXD pins are input and output between the processor and the CAN FD physical layer transceiver. The digital logic input and output levels for these devices are TTL levels with respect to VCC1 for compatibility with protocol controllers having 3.3V or 5V logic. Table 8-2 and Table 8-3 provides the states of the CAN driver and CAN receiver in each mode.

Table 8-2. Driver Function Table

Transceiver State	TXD Input	Bus Outputs		Driven Bus State
		CANH	CANL	
CAN On	L	H	L	Dominant
	H or Open	Z	Z	Biased Recessive
Wake capable (CAN)	X	Z	Z	Weak Pull to GND
Off	X	Z	Z	

Table 8-3. CAN Receiver Function Table

Transceiver State	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus States	RXD Terminal
On/Listen	$V_{ID} \geq 0.9V$	Dominant	L
	$0.5V < V_{ID} < 0.9V$	Undefined	Undefined
	$V_{ID} \leq 0.5V$	Recessive	H

Table 8-3. CAN Receiver Function Table (continued)

Transceiver State	CAN Differential Inputs $V_{ID} = V_{CANH} – V_{CANL}$	Bus States	RXD Terminal
Wake capable	$V_{ID} \geq 1.15V$	Dominant	See Figure 8-16
	$0.4V < V_{ID} < 1.15V$	Undefined	
	$V_{ID} \leq 0.4V$	Recessive	
Off	Open ($V_{ID} \cong 0V$)	Open	H

8.3.2 VCC1 Regulator

TCAN245x-Q1 includes a fully integrated synchronous buck (step-down) regulator on VCC1. VCC1 is the main supply for the low-voltage digital I/O pins and is the intended supply for the microcontroller. Figure 8-4 shows the simplified block diagram.

VSUPB is the input supply pin to the buck regulator. However, verify that VSUP and VSUPB connect on the board together for the buck regulator to turn ON and function properly. Verify that VSUP/VSUPB connect to the battery through an external reverse battery-blocking diode and EMI filtering network. The V_{SUPB} pin is a high-voltage-tolerant pin. Decoupling capacitor with a value of 100nF is recommended to connect close to this pin to improve the transient performance.

The VCC1 output pin sources either 3.3V or 5V to external circuits with up to 1A of current. If VSEL pin connects to GND, the VCC1 output is set to 5V. If VSEL pin is left floating, the VCC1 output is set to 3.3V. The state of the VSEL pin is detected at power-up and VCC1 output level is configured accordingly. After the power-up sequence completes, the state of the VSEL pin does not affect the VCC1 output configuration. The internal pull-up disables after the power-up sequence to avoid current draw from VSEL pin.

The VCC1 pin is capable of sinking either 10µA or 1000µA of current depending upon the register setting VCC1_SINK and is active by default. Disable the current sink by setting the register bit VCC1_SNK_DIS.

Connect an inductor L_{OUT} of suitable value between BUCKSW and VCC1 pins. A output capacitor C_{OUT} is required between VCC1 and GND. The application section explains selection criteria for the correct values for L_{OUT} and C_{OUT}. Connect a boot capacitor C_{BOOT} of 100nF between BUCKSW and BOOT pins. The C_{BOOT} capacitor is required for the proper operation of high-side switch.

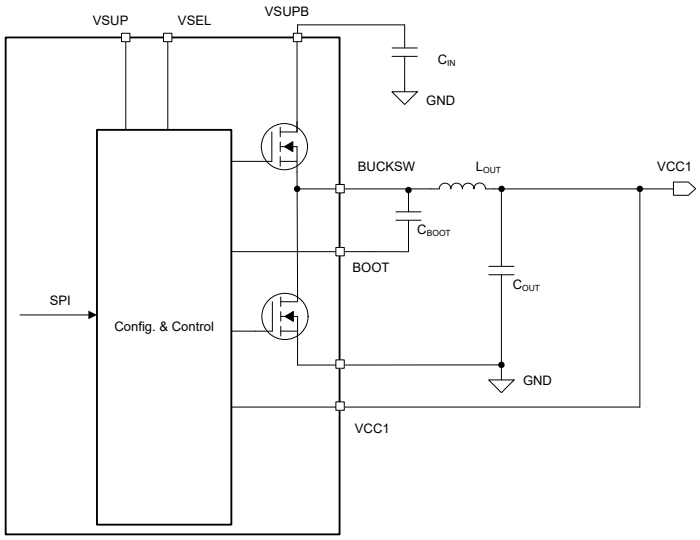


Figure 8-4. VCC1 Buck Regulator Block Diagram

The TCAN245x-Q1 allows configuration of buck regulator via SPI registers. The register VCC1_CFG determines whether the buck regulator is always ON, or whether the status is controlled by the device mode (default), as described in Table 8-27.

The register BUCK_CONFIG1 allows user to set the spread spectrum modulation options SS_MOD_FREQ, regular switching frequency, the configuration of PWM and Auto modes in low-power modes, and current limiting settings. The buck regulator employs dual random spread spectrum (DSRSS) method

There are three monitors on V_{CC1}: under-voltage (UVCC1), over-voltage (OVCC1) and short to ground ($VCC1_{SC}$). V_{CC1} is the main regulator output and sets the digital IO voltage levels. Any fault on V_{CC1} causes a device state change as described in Figure 8-53.

8.3.2.1 Functional Description of Buck Regulator

8.3.2.1.1 Fixed Frequency Peak Current Mode Control

The buck regulator integrated in TCAN245x-Q1 is a step-down synchronous buck converter with integrated high-side (HS) and low-side (LS) switches. The regulator supplies a regulated output voltage by turning on the high-side and low-side NMOS switches with controlled duty cycle. Refer to Figure 8-5. During high-side switch ON time, the BUCKSW pin voltage swings up to approximately VSUPB, and the inductor current, i_L, increases with linear slope (VSUPB – VCC1) / L. When the high-side switch is turned off by the control logic, the low-side switch is turned on after an anti-shoot-through dead time (t_D). Inductor current discharges through the low-side switch with a slope of –VCC1/L. The control parameter of a buck converter is defined as Duty Cycle D = t_{ON} / T_{SW}, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The converter control loop maintains a constant output voltage by adjusting the duty cycle D. In a buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = VCC1/VSUPB.

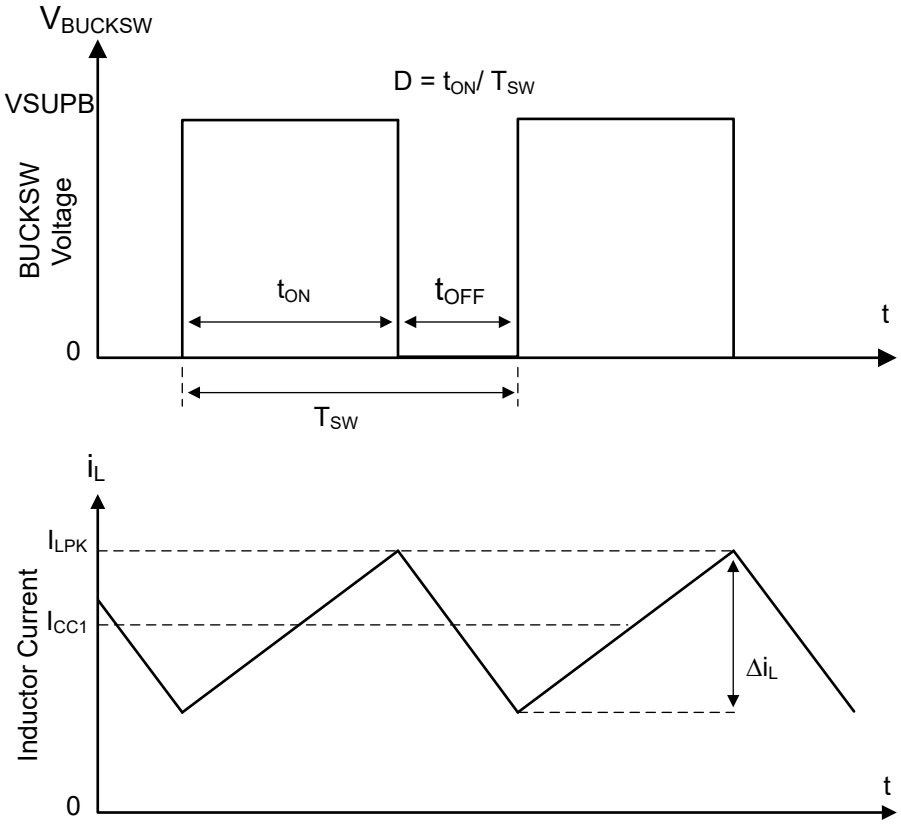


Figure 8-5. Switching node waveform in the Continuous Current Mode (CCM)

The buck regulator employs fixed-frequency peak-current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak-current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON time of the high-side switch. The voltage feedback loop is internally-compensated, which allows for fewer external components, making designing easy, and providing stable operation when using a variety of output capacitors. The converter operates with fixed switching frequency at normal load conditions. When set to Auto

mode (Automatic transition from PWM to PFM mode), during light-load conditions, the buck regulator operates in PFM mode to maintain high efficiency. When set to Forced PWM (FPWM) mode, the regulator operates in PWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency.

8.3.2.1.2 Minimum ON-Time, Minimum OFF-Time, and Frequency Foldback

Minimum ON-time (T_{ON_MIN}) is the shortest duration of time that the high-side switch can be turned on. T_{ON_MIN} is typically 60ns. Minimum OFF-time (T_{OFF_MIN}) is the shortest duration of time that the high-side switch can be off. T_{OFF_MIN} is typically 110ns. In CCM operation, T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion range without switching frequency foldback. The minimum duty cycle without frequency foldback allowed is:

$$D_{MIN} = T_{ON\_MIN} \times f_{SW} \quad (1)$$

The maximum duty cycle without frequency foldback allowed is:

$$D_{MAX} = 1 - T_{OFF\_MIN} \times f_{SW} \quad (2)$$

Given a required output voltage, the maximum VSUPB without frequency foldback can be found by:

$$VSUPB\_MAX = VCC1 \div \left[f_{SW\ ON\_} \times TMIN\right] \quad (3)$$

The minimum VSUPB without frequency foldback can be calculated by:

$$VSUPB\_MIN = VCC1 \div \left[1 - f_{SW} \times T_{OFF\_MIN}\right] \quad (4)$$

The frequency foldback scheme is employed once the T_{ON_MIN} or T_{OFF_MIN} is triggered, which can extend the maximum duty cycle or lower the minimum duty cycle. The on-time decreases while VSUPB voltage increases. Once the on-time decreases to T_{ON_MIN}, the switching frequency starts to decrease while VSUPB continues to go up, which lowers the duty cycle further to keep VCC1 in regulation.

The frequency foldback scheme also works when a larger duty cycle is needed under low VSUPB condition. The frequency decreases once the device hits the T_{OFF_MIN}, which extends the maximum duty cycle. In such condition, the frequency can be as low as approximately 133kHz. Wide range of frequency foldback allows for VCC1 to stay in regulation with a much lower supply voltage VSUPB, which leads to a lower effective dropout. With frequency foldback while maintaining a regulated output voltage, VSUPB_MAX is raised, and VSUPB_MIN is lowered by decreased f_{SW}.

8.3.2.1.3 Overcurrent and Short Circuit Protection

The buck regulator incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for sustained short circuits. High-side MOSFET overcurrent protection is implemented by the nature of the Peak Current Mode control. The high-side switch current is sensed when the high-side is turned on after a set blanking time. The high-side switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. The peak current of high-side switch is limited by a clamped maximum peak current threshold Isc, which is constant. The current going through low-side MOSFET is also sensed and monitored. When the low-side switch turns on, the inductor current begins to ramp down. The low-side switch is not turned OFF at the end of a switching cycle if its current is above the low-side current limit I_{LS_LIMIT} . The low-side switch is kept ON so that inductor current keeps ramping down, until the inductor current ramps below the I_{LS_LIMIT}. Then the low-side switch is turned OFF and the high-side switch is turned on after a dead time. After I_{LS_LIMIT} is achieved, peak and valley current limit controls the max current delivered to the load and it can be calculated as:

$$I_{CC1-max} = \left[I_{LS\_LIMIT} + I_{SC}\right] \div 2 \quad (5)$$

If the internal feedback voltage is lower than $VCC1_{33SC}$ threshold ($VCC1_{33SC}$ for 3.3V VCC1 and $VCC1_{5SC}$ for 5V VCC1), short-circuit protection mode is activated and the TCAN245x-Q1enters fail-safe mode. In fail-safe mode, the buck regulator shuts down. Figure 8-36 describes how the TCAN245x-Q1 exits fail-safe mode after a short-circuit fault on VCC1.

8.3.2.1.4 Soft Start

The integrated soft-start circuit prevents input inrush current impacting the regulator and the input power supply. Soft start is achieved by slowly ramping up the internal reference voltage when the device is first enabled or powered up. The typical soft-start time is 1.8ms. Without this feature, in applications with a large amount of output capacitors and high VOUT, the inrush current is large enough to trigger the current-limit protection, which can cause a false start as the device entering into Fail-safe mode. The device also blocks short-circuit detection for t_{REGON} after the regulator is turned on to prevent the false start.

8.3.2.2 Buck Regulator Functional Modes

8.3.2.2.1 Buck Shutdown Mode

The buck regulator is in Shutdown mode when:

- The TCAN245x-Q1 is in Off or Fail-safe mode
- The TCAN245x-Q1 is in Sleep mode, unless programmed as On

8.3.2.2.2 Buck Active Modes

When the buck regulator is active, the operating mode depends on the SBC mode and the settings in the BUCK_CONFIG1 register. If the TCAN245x-Q1 is in SBC Normal mode, the buck regulator is in forced PWM mode by default. If the TCAN245x-Q1 is in SBC Standby or SBC Sleep mode, the buck regulator is in Auto mode by default. However, the regulator can be forced to be in PWM (FPWM) mode in SBC Standby or SBC Sleep mode by using BUCK_CONFIG1 register 8'h65[2]=1b. Similarly, the regulator can be forced to be Auto mode in the SBC Normal mode by using BUCK_CONFIG1 register 8'h65[3]=0b. In the SBC Restart mode, the buck regulator is in Auto mode.

In Auto mode, the regulator automatically switches from PWM to PFM mode depending upon the load current. If the peak current through the high-side switch is less than 300mA (typical), the regulator transitions to PFM mode.

Table 8-4. Buck Regulator Modes versus SBC modes

PWM_PFM_CNTL Setting (8'h65[3:2])	Normal	Standby	Sleep	Fail-safe	Restart
00b	Auto	Auto	Auto	Off	Auto
01b	Auto	FPWM	FPWM	Off	Auto
10b (default)	**FPWM**	**Auto**	**Auto**	**Off**	**Auto**
11b	FPWM	FPWM	FPWM	Off	Auto

8.3.3 V_{CC2} Regulator

The V_{CC2} pin provides 5V with up to 200mA to external circuitry and requires an external capacitor to ground. The V_{CC2} pin is short to battery protected and if connected to VCAN or an external CAN transceiver, do not take the VCC2 off board where a short to battery can take place. There are three monitors on V_{CC2}, under-voltage (UVCC2), over-voltage (OVCC2) and short to ground ($VCC2_{SC}$). When these faults are detected an interrupt is provided and the LDO may or may not be turned off. No mode change take place. When VCC2 is on and not in a fault state, register 8'h4F[2], VCC2_STATUS, indicates this by being set to 1b.

8.3.3.1 V_{CC2} Short to Battery Protection

The output stage of V_{CC2} is short to battery protected. No inverse current flow if external voltage is at or above OVCC2. This protection is for up to the rated Absolute Maximum Rating for this pin. If the device powers up with a short to battery that is above the rated voltage, the device can be damaged or reliability issues can occur.

8.3.4 Reset Function (nRST Pin)

The nRST pin is a bi-directional open-drain low side driver that serves several functions, an VCC1 monitor output for under-voltage events, an indicator to the processor that restart has been entered and a device input reset.

The nRST is connected to V_{CC1} through a 30kΩ resistor, see Figure 8-6. When a V_{CC1} under-voltage (UVCC1) event takes place, the device transitions to restart mode, and nRST pin is latched low. nRST pin behavior is shown in Figure 8-7 based upon the SBC mode of operation and how entering the mode occurred.

When the device enters restart mode, this pins behavior depends upon the method of entry. If entering restart mode turns on the VCC1 regulator, the nRST is latched low until the device enters standby mode. This is t_{RSTN_act} after the LDOs exceed the LDO rising under-voltage level. If the VCC1 regulator is already on when entering restart mode, the pin is pulled low for t_{NRST_TOG}. After this time, the device transitions to standby mode and nRST returns to high.

The pin can determine when an input pulse of t_{NRSTIN} is applied causing the device to reload EEPROM, set other registers to factory default and enters restart mode.

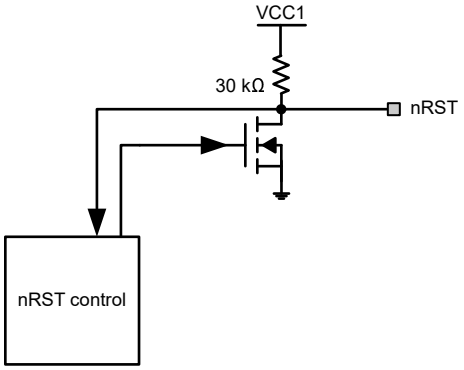


Figure 8-6. nRST Block Diagram

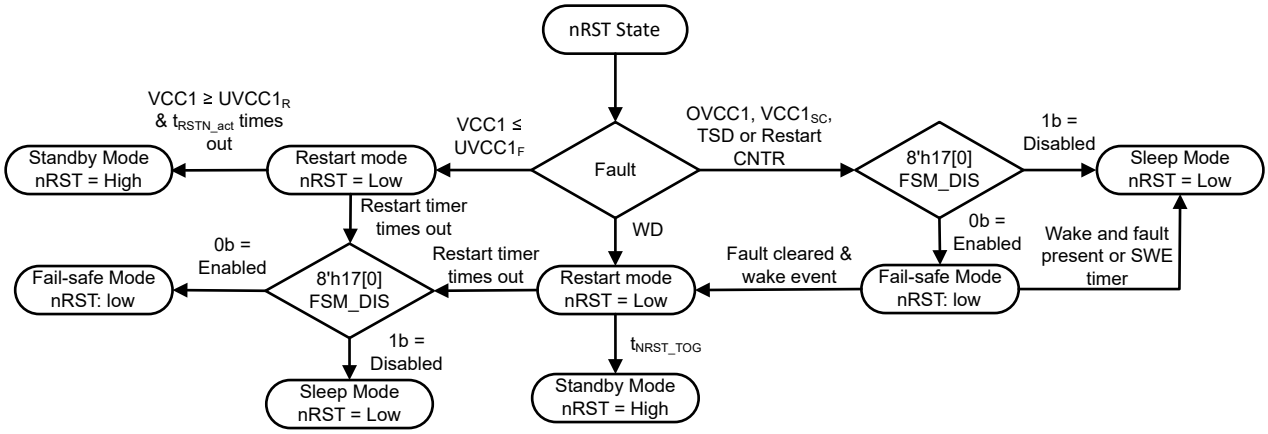


Figure 8-7. nRST State Diagram

8.3.5 LIMP Function

The LIMP pin is for the limp home function and is an open-drain, active low, output. The pin is used for a limp home mode if the watchdog has timed out causing a reset. Pull up the pin with an external resistor connected to a supply, typically, the battery supply, V_{SUP}. For the LIMP pin to be turned off, verify that the watchdog error counter reaches zero from correct input triggers or SPI write of 1b into LIMP_RESET bit (8'h1A[1]). If programmed, any event that triggers the fail-safe mode also turns on the LIMP pin. Configure the LIMP pin as active in Sleep mode in case of VCC1SC, OVCC1, Watchdog error or thermal shutdown faults using the register

bit LIMP_SLP_FLT_EN (8'h1A[7]). This feature enables LIMP to be activated on entering Sleep mode due to any faults in case fail-safe mode is disabled.

Program the LIMP pin for use as a low-side switch. Configure the low-side switch using the register bit LIMP_LSS_SEL. To use the pin as low-side switch, disable the LIMP functionality using the register bit LIMP_DIS. Otherwise, the device ignores the low-side switch setting. Use the low-side switch as either always On or always Off or configure to use PWM1, PWM2, Timer1, or Timer2 using the register bit LIMP_LSS_CNTL.

8.3.6 High Side Switches

HSS1-4 pins are outputs of the high-side switches. The V_{HSS} pin is a dedicated supply pin for the high-side switches outputs. Program the pins to support a 200Hz or 400Hz 10-bit PWM. PWM1, PWM2, PWM3 or PWM4 can be assigned to the HSSx. Configure HSS4 to use one of two timers that allows HSS4 to work with WAKEx/IDx pins supporting cyclic sensing. Cyclic sensing is used for sleep mode; thus, reducing sleep mode current.

To configure HSS3 and HSS4, use register 8'h4D[7:0]. To configure PWM3 and PWM4 SBC_CONFIG0 register 8'h0C[5:4] = 01b, use the PWM1 and PWM2 configuration registers to program them. This changes the PWM1 control registers to PWM3 and the PWM2 control registers to PWM4. After configuring the registers, the best practice is to change 8'h0C[5:4] = 00b. Thus, converting the PWM registers back to PWM1 and PWM2.

Any HSS connects to any other HSS and is synchronized by assigning the HSS the same control mechanism. This allows the use of higher current loads. Assigning the same PWM to multiple HSS synchronizes the selected HSS'es. Use Timer1 and Timer2 in the same way. When synchronizing the high-side switches, use the following procedure.

To synchronize using the same timer:

- Make sure the selected timer is off to begin with
- Program the selected high-side switches to the same control timer
- Program the timer period and on-time
- High-side switches start as soon as the on-time is programmed and the selected HSSx synchronizes

To synchronize multiple HSSx with the same PWM, follow these steps in the order described:

- Program the PWMx_FREQ
- Program the PWMx_DC_MSB
- Program the PWMx_DC (LSB bits), after this step, the PWM is programmed and HSSx turn on with the selected PWM frequency and duty cycle
- Verify that any changes to the PWMx_FREQ or PWMx_DC_MSB include programming the PWMx_DC (LSB bits) as the last step for the updates to implement

The high side switches are monitored for open load and overcurrent faults. When an overcurrent is detected through an HSS, there is a filter time, t_{OCFLTR}, to determine if overcurrent is valid. If valid, a corresponding HSSx overcurrent interrupt flag is set in the INT_7 register (8'h55). If the overcurrent condition persists for t_{OCOFF}, the HSS is turned off and HSSx_CNTL register is reset to 000b. HSS is not turned back ON automatically. HSS can be turned ON again after another t_{OCOFF} period by writing into the corresponding HSSx_CNTL register. If the overcurrent fault is cleared, HSS stays ON. If the overcurrent fault exists, HSS is shutoff after t_{OCOFF}. When an open load fault is detected at an HSS, an interrupt flag is set in the INT_7 register (8'h55). HSS is not turned off due to open load fault. Please note that HSSx overcurrent or open load fault interrupt flags are not automatically cleared after the fault is cleared.

The VHSS pin is also monitored for a high-side switch over-voltage condition based upon OVHSS thresholds. If VHSS exceeds this threshold, an interrupt flag is set in the INT_4 register (8'h5A[2]) and all four high-side switches are turned off and HSSx_CNTL register bits are reset to 000b. Similarly, when VHSS drops below UVHSS threshold, an interrupt flag is set in the INT_4 register (8'h5A[2]) and all four high-side switches are turned off and HSSx_CNTL register bits are reset to 000b. After VHSS returns to normal level, the high-side switches are automatically enabled to the previous state if HSS_OV_UV_REC register (8'h4F[5]) is set to 1b. If HSS_OV_UV_REC = 0b, the high-side switches stay off due to an over-voltage or under-voltage event on VHSS. OVHSS and UVHSS faults can also be disabled via HSS_OV_DIS and HSS_UV_DIS register bits

(8'h4F[7] and 8'h4F[6]) respectively. Please note that OVHSS/UVHSS interrupt flags are not automatically cleared after the faults are cleared.

Note

- For resistive loads an external capacitor to ground in not required.
- For inductive loads an external 100nF capacitor to ground is needed.
- When using the 10-bit PWM with the HSS, selecting values that are unrealizable due to the on and off times of the switch is possible. An example of this is 00 0000 0001b

8.3.7 WAKE and ID Inputs

WAKE1/ID1, WAKE2/ID2, WAKE3/ID3 and WAKE4/ID4 are pins are ground biased local wake up (LWU) input pins that are high voltage tolerant. These pins can also be configured as ID pins to help identify location of the ECU in the vehicle. Please see ID Functionality

Pins can be configured individually for wake functionality by setting register bits [7:4] in WAKE_PIN_CONFIG3 Register (Address = 2Ah) [Reset = F0h]. The wake function is explained further in Local Wake Up (LWU) via WAKE Input Terminal. The pins can be both rising and falling edge trigger, meaning it recognizes a LWU on either edge of WAKE pin transition. The pin can be configured to accept a pulse, see Figure 8-20 for timing diagram of this behavior. The WAKE pins are default enabled but can be disabled by using register 8'h2A[7:5], WAKE_PIN_SET, to turn off individual ones. Register 8'h11[7:6] sets the method the pins are used to register a wake event. These pins can be configured for cyclic sensing wake, see Cyclic Sensing Wake, or static wake.

The WAKE pins have four individual thresholds that can be set for a state change.

- Register 8'h12[1:0], WAKE1_LEVEL
- Register 8'h2B[5:4], WAKE2_LEVEL
- Register 8'h2B[1:0], WAKE3_LEVEL
- Register 8'h7B[5:4], WAKE4_LEVEL

Note

If WAKEx_LEVEL = 10b or 11b is selected and uses static wake, the system designer must make sure that VSUP does not cross the wake pin threshold; otherwise, a false wake up can take place. Normal undervoltage events on VSUP does not cause this to take place.

If WAKEx_LEVEL = 00b and the device enters Fail-safe mode or Sleep mode where VCC1 is off, the WAKEx pin becomes disabled and CAN and LIN are set wake-capable.

Register 8'h2A[4:0], MULTI_WAKE_STAT, provides which WAKE pin or combination of WAKE pins caused the LWU event. The individual status of the pins, low or high, can be read via SPI in any mode that SPI is available.

- Register 8'h11[5], WAKE1_STAT
- Register 8'h2B[6], WAKE2_STAT
- Register 8'h2B[2], WAKE3_STAT
- Register 8'h7B[6], WAKE4_STAT

8.3.7.1 ID Functionality

To configure WAKE1/ID1, WAKE2/ID2, WAKE3/ID3,WAKE4/ID4 pins for ID functionality, use the IDx_EN field in the registers WAKE_ID_CONFIG1 Register (Address = 79h) [Reset = 66h] and WAKE_ID_CONFIG2 Register (Address = 7Ah) [Reset = 66h] :

- Register 8'h79[3] = 1b to set WAKE1/ID1 as ID1 pin
- Register 8'h79[7] = 1b to set WAKE2/ID2 as ID2 pin
- Register 8'h7A[3] = 1b to set WAKE3/ID3 as ID3 pin
- Register 8'h7A[7] = 1b to set WAKE4/ID4 as ID4 pin

When IDx_EN field is set to 1b, the device automatically switches on internal pull-up and pull-down currents (if PU_PD_CONFIG register is set to 'Automatic') to detect the status of the ID pin connection. The device

determines if the ID pin is connected to VSUP, GND or floating. If the pin is connected to GND, the device internally activates the pull-down to reduce the current consumption. If the pin is connected to VSUP, the device internally activates the pull-up to reduce the current consumption. If the pin is floating, the device deactivates both the pull-up and pull-down at the pin.

User can force the pin to either activate the pull-down or a pull-up at the pin by setting the WAKE_ID_PU_PD field in the registers WAKE_ID_CONFIG1 Register (Address = 79h) [Reset = 66h] and WAKE_ID_CONFIG2 Register (Address = 7Ah) [Reset = 66h] . The recommendation is to do this only for brief period of time to keep the current consumption low. If pull-up or pull-down are forcefully activated, IDx_STAT registers do not reflect the status of the pin connection and instead the status is set to 'Unknown'. WAKEx_STAT registers can be used to read the logic at the pin and the ID pin connection can be derived manually.

The status of the IDx pin connections are stored in the ID_PIN_STATUS Register (Address = 78h) [Reset = 00h]:

- Register fields 8'h78[7-6] store the connection status of ID1 pin
- Register fields 8'h78[5-4] store the connection status of ID2 pin
- Register fields 8'h78[3-2] store the connection status of ID3 pin
- Register fields 8'h78[1-0] store the connection status of ID4 pin

8.3.8 Interrupt Function (nINT Pin)

This pin is the interrupt output pin to the processor. When the TCAN245x-Q1 requires the attention of the processor, this pin is pulled low. After the interrupt is cleared and the nINT pin is released back to high, a 1ms delay takes place before another interrupt can take place and latch the nINT pin low again.

The interrupt block is designed as a push-pull output stage referenced to VCC1 supply. When the TCAN245x-Q1 requires the attention of the processor due to any interrupt-generating event (any unmasked interrupt set in the interrupt registers), this pin is pulled low. After the interrupt is cleared the nINT pin is released back to high. A 1ms delay take places before another interrupt can take place and latch the nINT pin low again.

By default, nINT pin is a global interrupt indicator and is activated for any unmasked interrupt in the interrupt registers 8'h51-8'h55, 8'h5A and 8'h5C. If desired, specific interrupts can be masked such that those interrupts do not activate the nINT pin. The interrupts can be masked using the interrupt enable bits in the registers 8'h51-8'h55, 8'h5D and 8'h60.

All interrupts are stored in the respective interrupt registers until cleared by writing 1b (W1C) via SPI.

8.3.9 SPI Communication

The SPI communication uses a standard SPI interface. Physically the digital interface pins are nCS (Chip Select Not), SDI (SPI Data In), SDO (SPI Data Out) and SCK (SPI Clock). Each SPI transaction is initiated by a seven bit address with a R/W bit. The TCAN245x-Q1 can be configured for one data byte or two date bytes per transaction depending upon the value of the BYTE_CNT bit at SPI_CONFIG register 8'h09[3]. The default is one byte. When two byte is selected, the second data byte is for address + 1.

The data shifted out on the SDO pin for the transaction always starts with the register 8'h50[7:0] which is the global interrupt register. This register provides the high-level interrupt status information about the device. The data byte which are the ‘response’ to the address and R/W byte are shifted out next. See Figure 8-8 and Figure 8-9 for read and write method when cyclic redundancy is disabled.

For two byte read, see Figure 8-10. When a two byte SPI write takes place, the current information in the address and address + 1 is fed back out on the SDO pin. See Figure 8-11 for the SPI write in two-byte mode. Two-byte mode does not support CRC.

The device defaults to mode 0 where SPI data input data on SDI is sampled on the low to high edge of SCK. The SPI output data on SDO is changed on the high to low edge of SCK. The device can be configured to support Mode 1 - 3 by using SPI_MODE bits in SPI_CONFIG. SPI communication diagrams are based upon Mode 0.

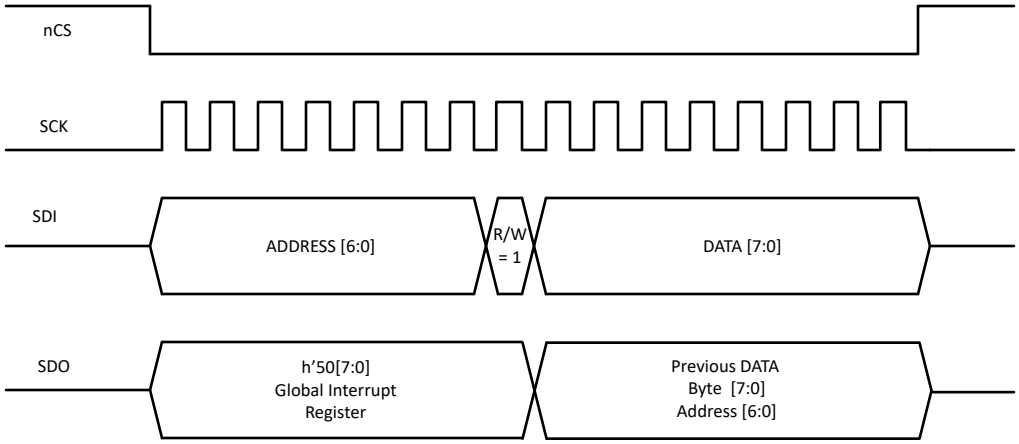


Figure 8-8. SPI Write

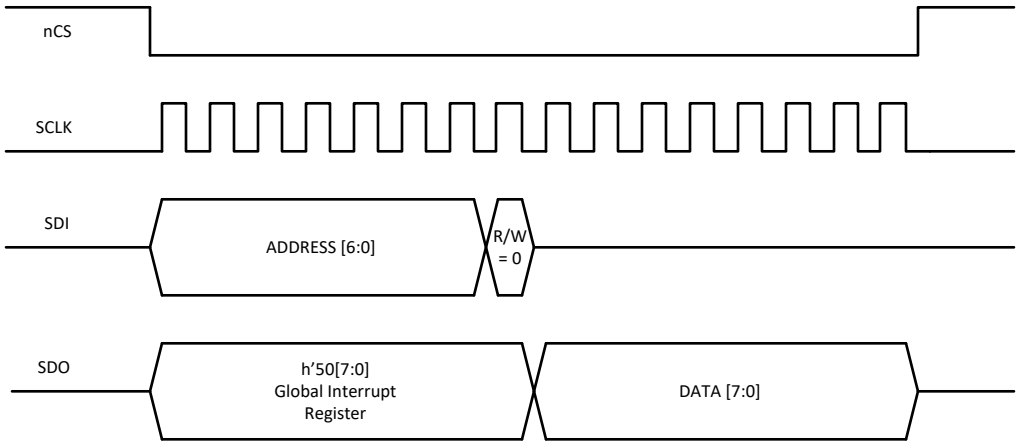


Figure 8-9. SPI Read

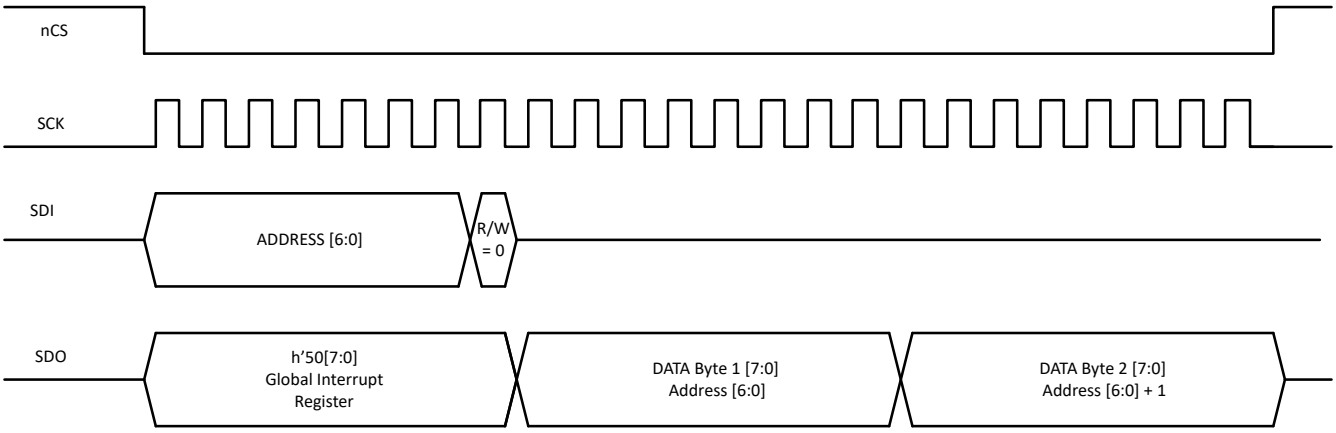


Figure 8-10. SPI Read (Two-byte mode)

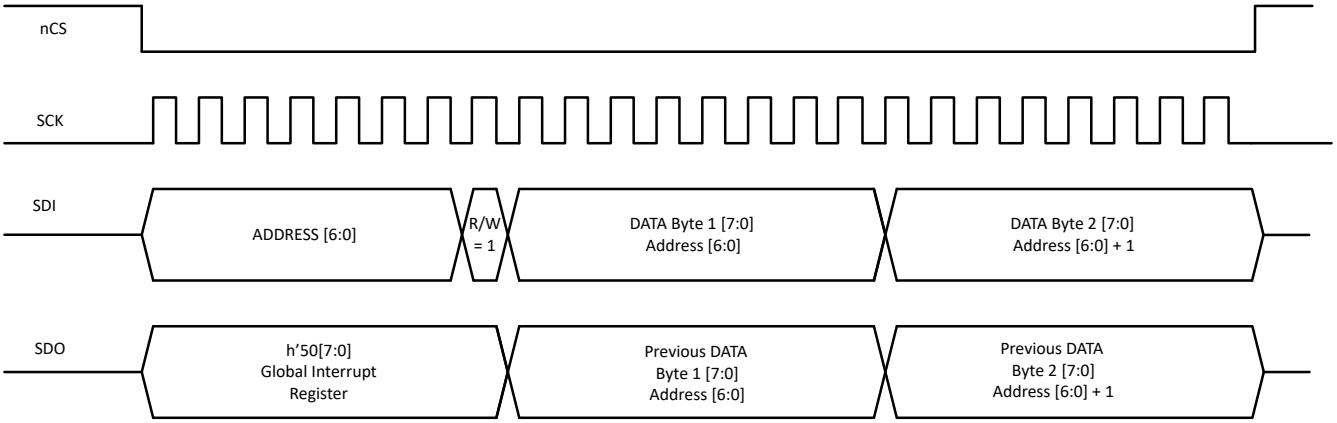


Figure 8-11. SPI Write (Two-byte mode)

8.3.9.1 Cyclic Redundancy Check

The TCAN245x-Q1 family cyclic redundancy check (CRC) for SPI transactions, default disabled. Register 'h0A[0] can be used to enable this feature. The default polynomial supports AutoSAR CRC8H2F, $X^8 + X^5 + X^3 + X^2 + X + 1$, see Table 8-5. CRC8 according to SAE J1850 is also supported and can be selected at register 8'h0B[0]. When CRC is enabled, a filler byte of 00h is used to calculate the CRC value during a read/write operation, see Figure 8-12 and Figure 8-13.

Note

CRC is not implemented when two byte data is configured. Enabling CRC in two-byte mode prevents SPI communication and requires device reset to recover from the SPI communication loss.

Table 8-5. CRC8H27

SPI Transactions	
CRC result width	8 bits
Polynomial	2Fh
Initial value	FFh
Input data reflected	No
Result data reflected	No
XOR value	FFh
Check	DFh
Magic Check	42h

Table 8-6. CRC8 SAE J1850

SPI Transactions	
CRC result width	8 bits
Polynomial	1Dh
Initial value	FFh
Input data reflected	No
Result data reflected	No
XOR value	FFh
Check	4Bh
Magic Check	C4h

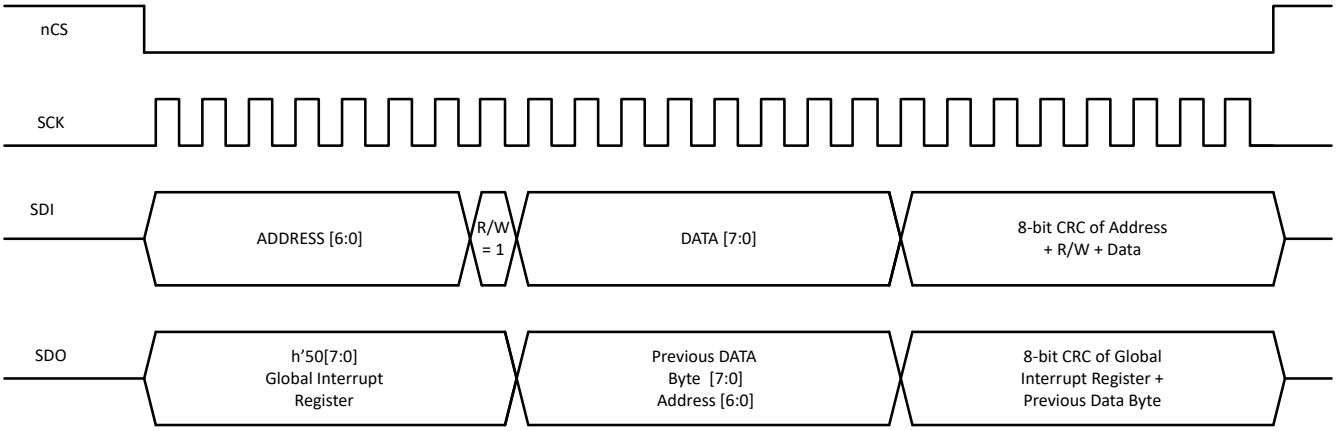


Figure 8-12. CRC SPI Write

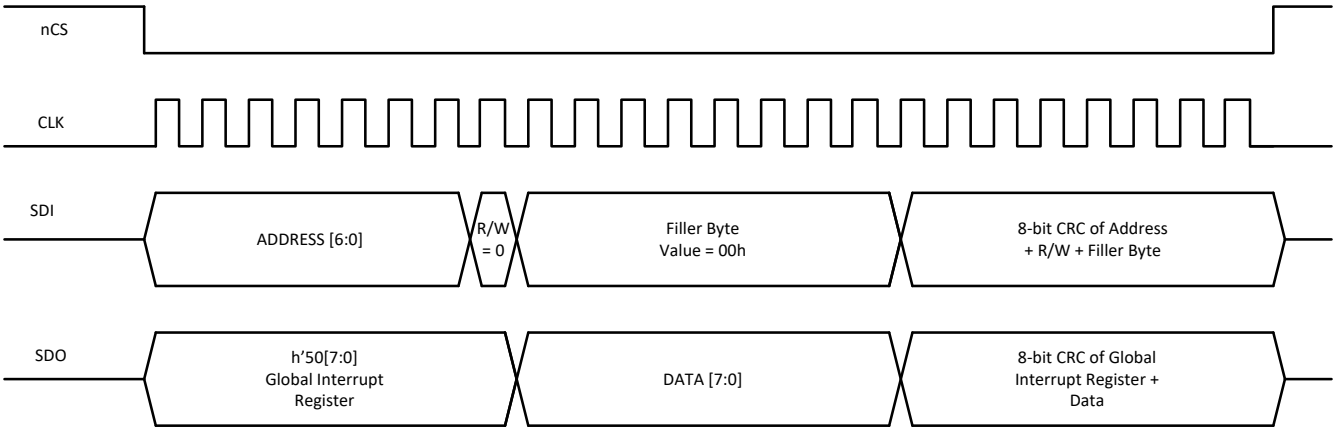


Figure 8-13. CRC SPI Read

8.3.9.2 Chip Select Not (nCS):

This input pin is used to select the device for a SPI transaction. The pin is active low, so while nCS is high the SPI Data Output (SDO) pin of the device is high impedance allowing an SPI bus to be designed. When nCS is low the SDO driver is activated and communication may be started. The nCS pin is held low for a SPI transaction. A special feature on this device allows the SDO pin to immediately show the Global Fault Flag on a falling edge of nCS.

8.3.9.3 SPI Clock Input (SCK):

This input pin is used to input the clock for the SPI to synchronize the input and output serial data bit streams. The default SPI mode 0 is where data input is sampled on the rising edge of SCK and the SPI data output is changed on the falling edge of the SCK. See Figure 8-14. Figure shown provides the timing based upon Mode 0 which is the default. Table 8-7 provides the configurable modes with the clock phase.

Table 8-7. SPI Modes

Mode	CPOL	CPHA	Clock Phase
0	0	0	Data sampled on rising edge and shifted on falling edge
1	0	1	Data sampled on falling edge and shifted on rising edge
2	1	0	Data sampled on falling edge and shifted on rising edge
3	1	1	Data sampled on rising edge and shifted on falling edge

Note

- CPOL is the clock polarity where 0 = logic low and 1 = logic high
- CPHA is the clock phase

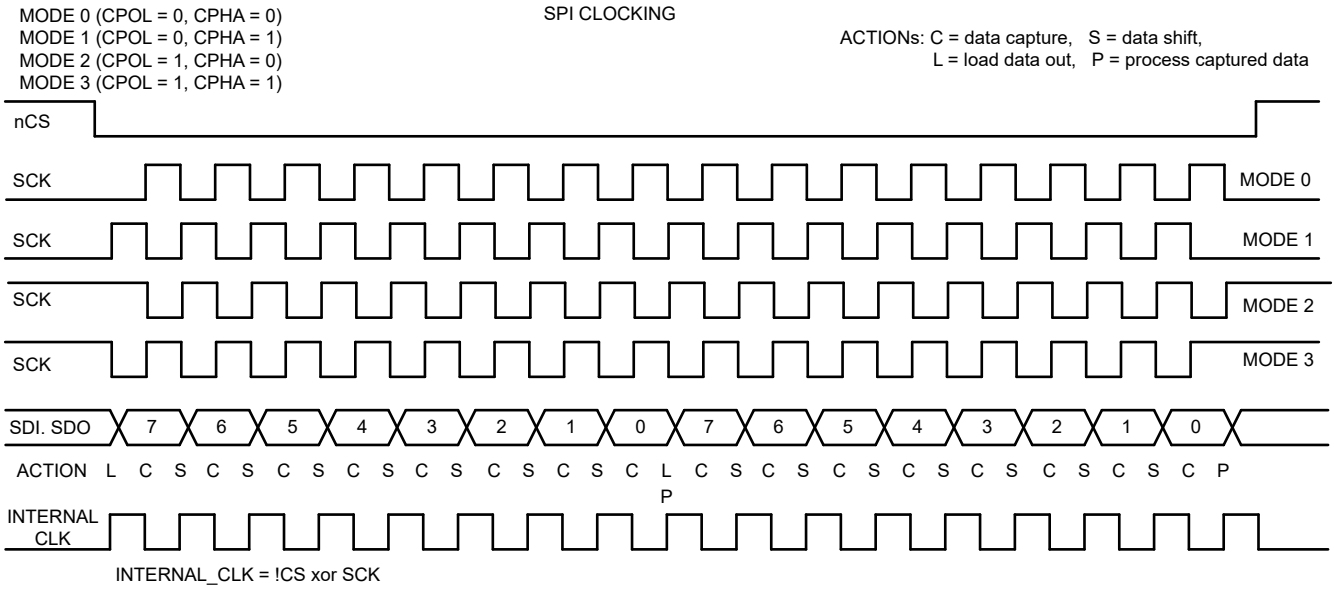


Figure 8-14. SPI Clocking

8.3.9.4 SPI Data Input (SDI):

This input pin is used to shift data into the device. Once the SPI is enabled by a low on nCS, the SDI samples the input shifted data on each rising edge of the SPI clock (SCK). The data is shifted into an 8-bit shift register. After eight (8) clock cycles and shifts, the addressed register is read giving the data to be shifted out on SDO. After eight clock cycles, the shift register is full and the SPI transaction is complete. If the command code is a write, the new data is written into the addressed register only after exactly 8 bits have been shifted in by SCK and the nCS has a rising edge to deselect the device. If there are not exactly 8 bits shifted in to the device during one SPI transaction (nCS low), the SPI command is ignored, the SPIERR flag is set and the data is not written into the device preventing any false actions by the device.

8.3.9.5 SPI Data Output (SDO):

This pin is high impedance until the SPI output is enabled via nCS. Once the SPI is enabled by a low on nCS, the SDO is immediately driven high or low showing the Global Fault Flag status which is also the first bit (bit 7) to be shifted out if the SPI is clocked. On the first falling edge of SCK, the shifting out of the data continues with each falling edge on SCK until all 8 bits have been shifted out the shift register.

8.3.10 SW Pin

During debug or development this pin can be used to disable the watchdog actions. When the pin is active, the device expects normal WD triggers, but ignores any mode changes or actions outside of setting the watchdog failure interrupt flag and incrementing and decrementing the watchdog counter. When the pin is released, the flags self-clears and the watchdog counter either goes back to default or programmed value. The pin is default active high but can be configured active low by using register 8'h0E[0] = 0b.

When the device is in sleep or fail-safe mode, this pin can be used as a digital wake up pin by enabling this feature using register 8'h0E[1] = 1b and 8'h0E[2] = 1b. If VCC1 is present in sleep mode, the thresholds is based on VCC1 levels. If V_{CC1} is not present, the levels is based off an internal voltage rail, $V_{IHSWINT}$ and $V_{ILSWINT}$. This pin can then be used to wake up when an external CAN FD or LIN transceiver is wake capable or MCU to wake up the TCAN245x-Q1. This can be accomplished in several ways. If the external transceiver has an inhibit pin,

external circuitry can be used to provide a wake input to this pin. The processor can connect directly to this pin and initiate the wake up without using a SPI command.

Figure 8-15 provides a state diagram on how the SW pin behaves.

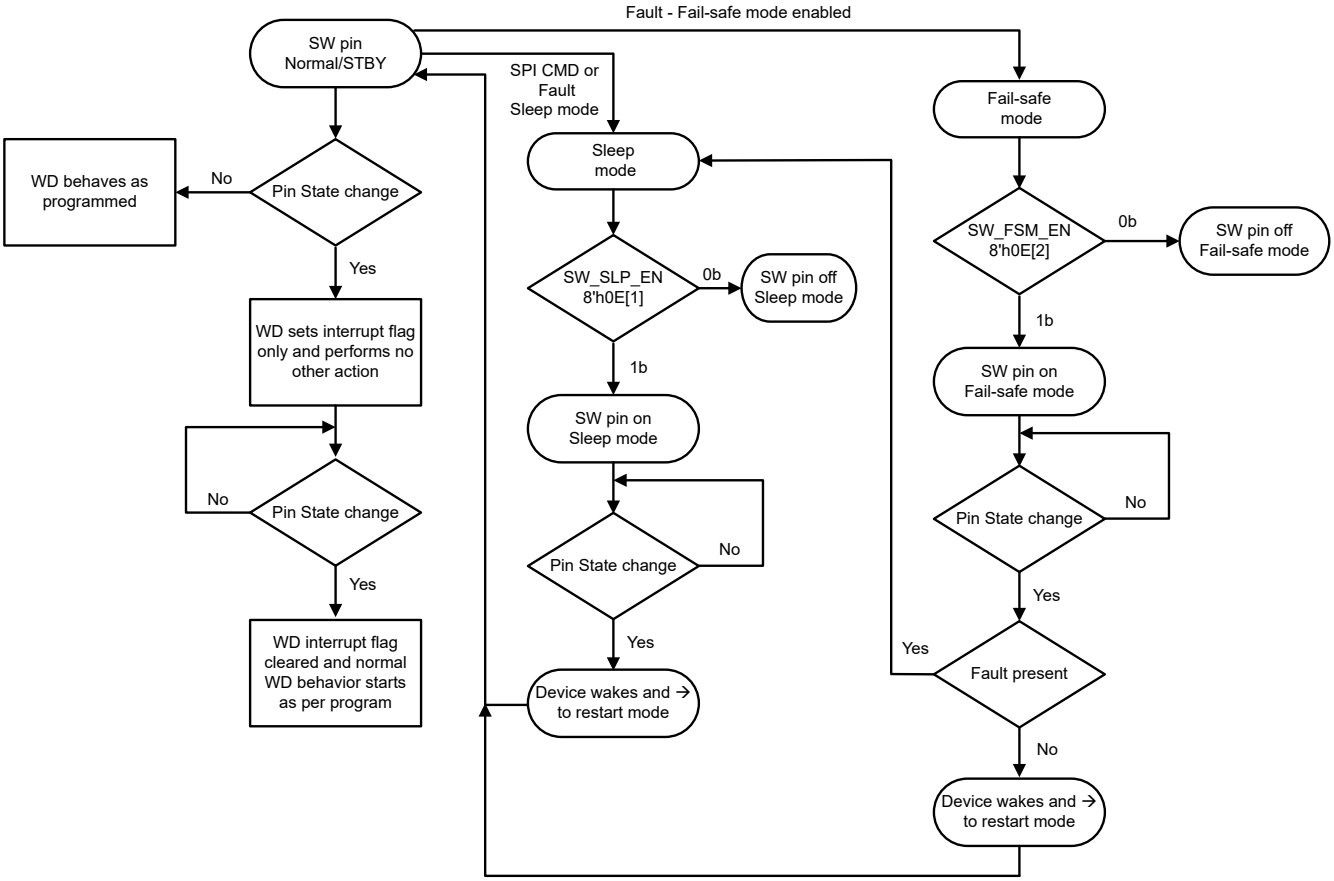


Figure 8-15. SW Pin State Diagram

Note

- The SW pin has a filter timer that the state change has to be at least t_{SW} = 140µs
- The pull-up and pull-down resistor is self-configured based upon register 8'h0E[0] setting. Active high means pull-down active, active low means pull-up active.
- If the device is powered up with the SW pin connected high, the device treats this as no watchdog actions to take place.

8.3.11 GFO Pin

This pin is can be programmed using nRST_GFO_CNTL Register (Address = 29h) [Reset = 0Ch] to provide certain information back to the processor. These can be considered interrupts such as a UVCC1 or watchdog failures. The pin can be configured to state which wake event has taken place, bus or local via WAKE pin. Configurable to indicate device has entered fail-safe mode.

Pin can also be configured to act as an enable pin to control an external LIN or CAN transceiver. This is accomplished by configuring the pin to support the correct polarity and then programming the external device mode.

8.3.12 Wake Functions

There are multiple ways to wake up from sleep mode.

- CAN bus wake using BWRR
- CAN bus wake using selective wake (TCAN2451-Q1)
- Local wake up through the WAKEx pins
- SW pin if programmed as a digital wake input

8.3.12.1 CAN Bus Wake Using RXD Request (BWRR) in Sleep Mode

The TCAN245x-Q1 supports low power sleep and standby modes, and uses a wake up from the CAN bus mechanism called bus wake through the RXD Request (BWRR). Once this pattern is received, the device automatically switches to standby mode from sleep mode, and insert an interrupt onto the nINT pin, if enabled, to indicate to a host microprocessor that the bus is active. If successful, the processor wakes up and services the device. The low power receiver and bus monitor are enabled in sleep mode to allow for RXD Wake Requests via the CAN bus. A wake-up request is output to the RXD (driven low) as shown in Figure 8-16. The external CAN FD controller monitors RXD for transitions (high to low) and reactivate the device to normal mode based on the RXD Wake Request. The CAN bus terminals are weakly pulled to GND during this mode, see Figure 7-2.

The device uses the wake-up pattern (WUP) from ISO 11898-2: 2016 to qualify bus traffic into a request to wake the host microprocessor. The bus wake request is signaled to the integrated CAN FD controller by a falling edge and low corresponding to a “filtered” bus dominant on the RXD terminal (BWRR).

The wake-up pattern (WUP) consists of:

- A filtered dominant bus of at least t_{WK_FILTER} followed by
- A filtered recessive bus time of at least t_{WK_FILTER} followed by
- A second filtered dominant bus time of at least t_{WK_FILTER}

Once the WUP is detected, the device starts issuing wake up requests (BWRR) on the RXD pin. The behavior of this pin is determined by register 8'h12[2]. If 8'h12[2] = 0b the RXD pin is pulled low once the WUP pattern has been received that meets the dominant, recessive, dominant filtered times. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive, other bus traffic does not reset the bus monitor. Once a filtered recessive is received, the bus monitor is now waiting on a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon receiving of the second filtered dominant the bus monitor recognizes the WUP and transition to BWRR output. Immediately upon verification receiving a WUP the device transitions the bus monitor into BWRR mode, and indicates all filtered dominant bus times on the RXD internal signal by driving it low for the dominant bus time that is in excess of t_{WK_FILTER}, thus the RXD output during BWRR matches the classical 8 pin CAN devices that used the single filtered dominant on the bus as the wake-up request mechanism from ISO 11898-2: 2016.

For a dominant or recessive to be considered “filtered”, the bus must be in that state for more than t_{WK_FILTER} time. Due to variability in the t_{WK_FILTER} the following scenarios are applicable.

- Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP, and thus no BWRR generates.
- Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ can be detected as part of a WUP and a BWRR can generate.
- Bus state times more than $t_{WK\_FILTER(MAX)}$ is always detected as part of a WUP; thus, a BWRR always generates.

See Figure 8-16 for the timing diagram of the WUP.

The pattern and t_{WK_FILTER} time used for the WUP and BWRR prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a BWRR. If the device is switched to normal mode or an under-voltage event occurs on V_{CC} the BWRR is lost. The WUP pattern must take place within the $t_{WK\_TIMEOUT}$ time; otherwise, the device is in a state waiting for the next recessive and then a valid WUP pattern.

If 8'h12[2] = 1 the RXD pin toggles low too high too low for t_{TOGGLE} = 10µS until the device is put into normal mode or listen mode. BWRR is active in standby mode upon power up and once coming out of sleep mode or certain failsafe mode conditions. If a SPI write puts the device into standby mode, the RXD pin is high until a wake event takes place. The RXD pin then behaves similar to the device coming out of sleep mode due to a wake event.

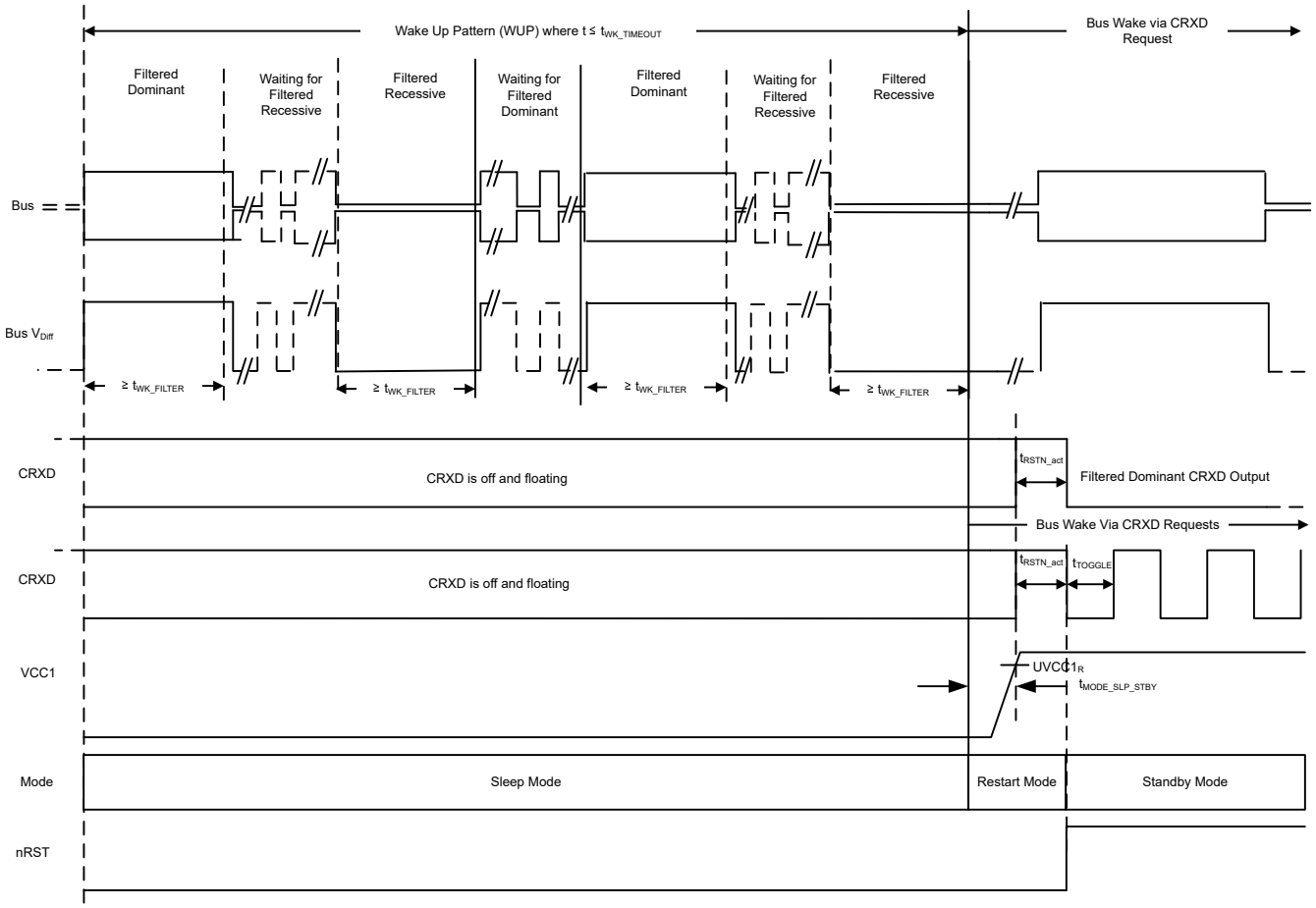


Figure 8-16. Wake Up Pattern (WUP) and Bus Wake Through RXD Request (BWRR)

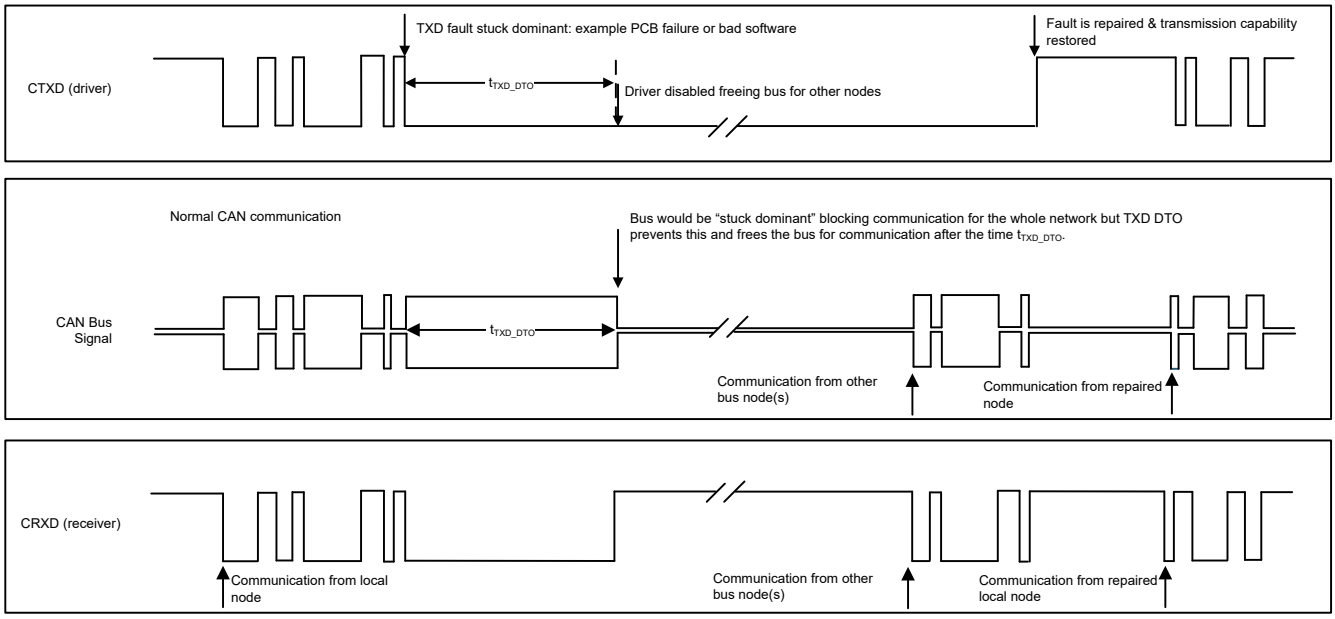


Figure 8-17. Example Timing Diagram With TXD DTO

8.3.12.2 Local Wake Up (LWU) via WAKEx Input Terminal

The WAKEx terminals are a highly configurable ground based, high voltage capable inputs which can be used for local wake up (LWU) request via a voltage transition. There are two methods for this wake event. A static wake based on a level changed on the pin or a timing based, cyclic sensing where the WAKEx pin is periodically turned on and a change during this on time is the trigger event is checked.

The device provides a WAKE pin status change update using reg 2Ah[4:0] showing which WAKE pin has changed states.

There are two methods of using the WAKE pins, determined by the WAKEx_SENSE register bit setting:

- Static wake
- Cyclic sensing wake

The WAKE pins have a global control for which method a wake takes place, rising edge, falling edge, bi-directional, pulse or filtered pulse. The WAKE pins have programmable thresholds.

8.3.12.2.1 Static Wake

The WAKEx pins default to static sensing wake (default values of WAKEx_SENSE register bits in WAKE_CONFIG2, WAKE_CONFIG4 and WAKE_CONFIG5 registers). The WAKEx pins default to bi-directional input but can be configured for rising edge and falling edge transitions, see Figure 8-18 and Figure 8-19, by using WAKE_CONFIG register 8'h11[7:6]. WAKE pins are ground based wake inputs and can be used with a switch to ground or V_{SUP}. The WAKEx pins input thresholds can be based on VCC1 levels which allows a direct connection to the processor or a switch to the VCC1 rail. If the terminal is not used, connect it to ground to avoid unwanted parasitic wake up. Once the device enters sleep mode the WAKEx terminals voltage level need to be at either a low state or high state for t_{WAKE} before a state transition for a WAKE input can be determined. A pulse width less than $t_{WAKE\_INVALID}$ is filtered out.

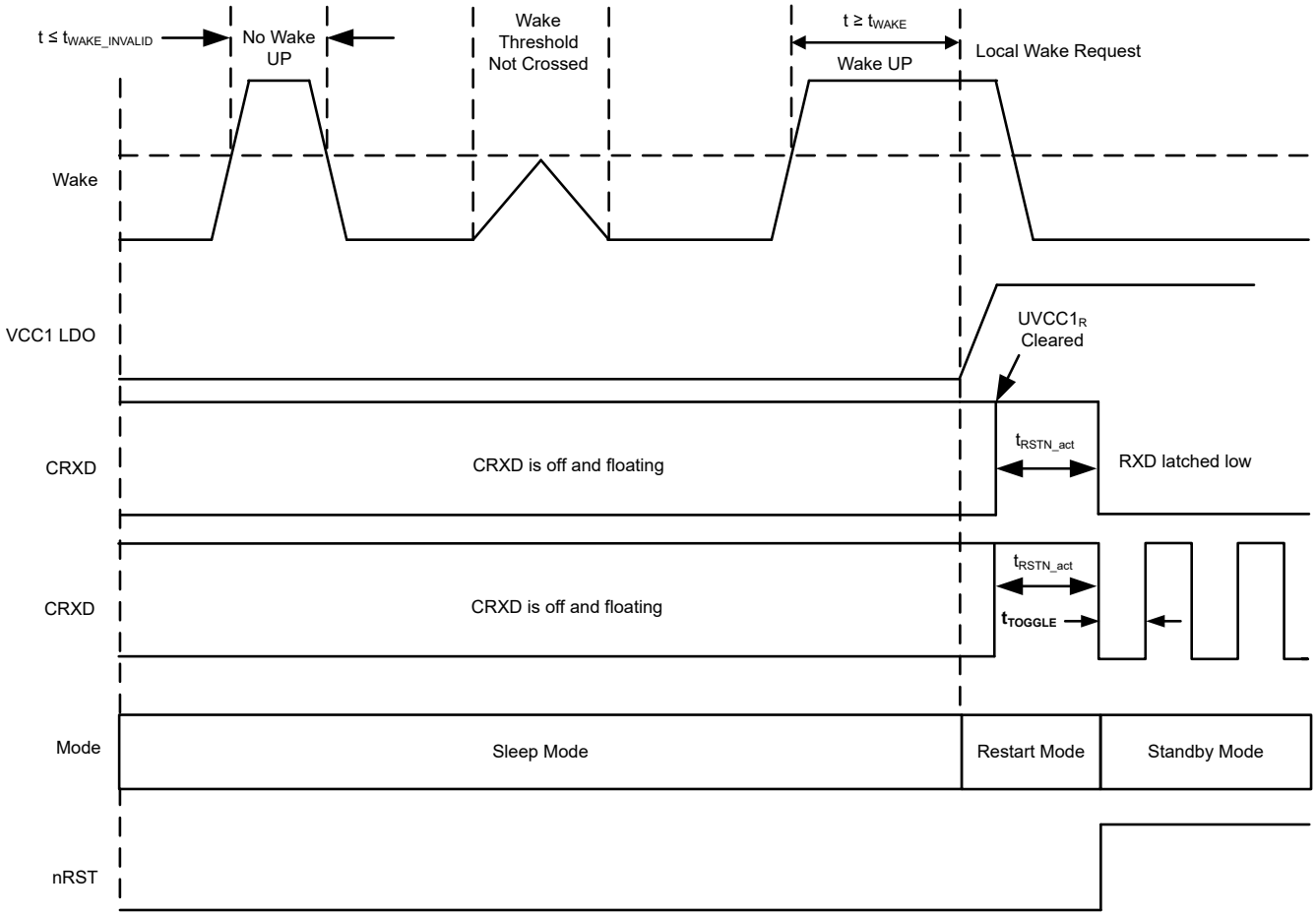


Figure 8-18. Local Wake Up – Rising Edge

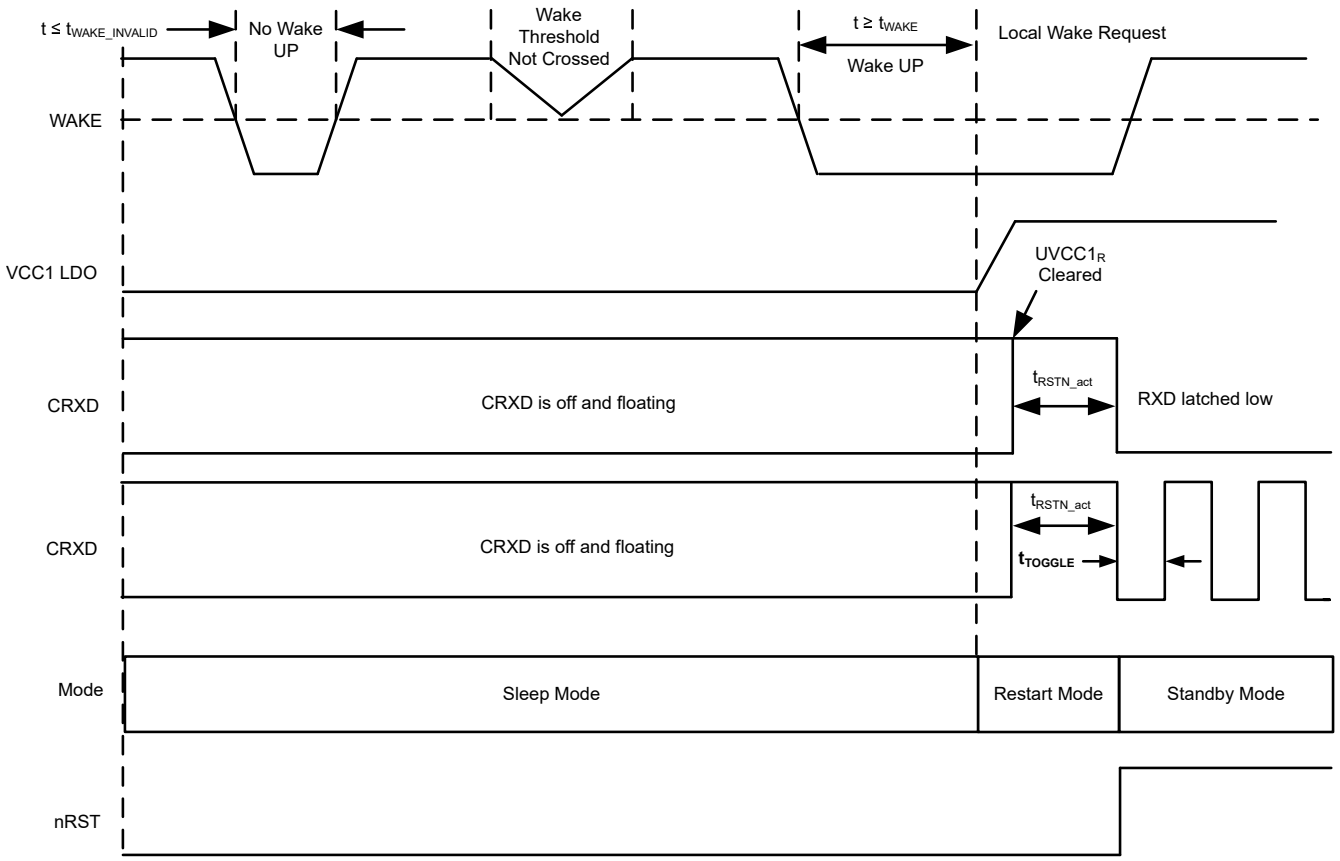


Figure 8-19. Local Wake Up – Falling Edge

Note

When WAKE pins are configured for static sensing and WAKE_CONFIG is set to bi-directional, rising or falling edge, the WAKE pin must be stable for at least a t_{WAKE} period of time after the pin crosses the selected wake threshold for a valid wake event to be recognized.

- If a rising edge is selected and the device goes to sleep with WAKE high, a low of at least t_{WAKE} must be present prior to the rising edge wake event
- If a falling edge is selected and the device goes to sleep with WAKE low, a high of at least t_{WAKE} must be present prior to the falling edge wake event
- In case of bi-directional edge configuration, the device determines the change in the wake level based on the threshold crossing and applies the t_{WAKE} filter accordingly.
- Figure 8-18 and Figure 8-19 provide examples of a rising or falling edge WAKE input. RXD is pulled low once VCC1 > UVCC1, and standby mode is entered.

The WAKE terminal can be configured for a pulse, see Figure 8-20, by using WAKE_CONFIG register 8'h11[7:6]. The terminal can be configured to work off a pulse only. The pulse must be between $t_{WK\_WIDTH\_MIN}$ and $t_{WK\_WIDTH\_MAX}$. This figure provides three examples of pulses and whether the device wakes or not wakes. $t_{WK\_WIDTH\_MIN}$ is determined by the value for $t_{WK\_WIDTH\_INVALID}$ is set to in register 8'h11[3:2]. There are two regions where a pulse may or may not be detected. By using register 8'h1B[1], WAKE_WIDTH_MAX_DIS, the pulse mode can be configured as a filtered wake input. Writing a 1 to this bit disables $t_{WK\_WIDTH\_MAX}$ and the WAKE input is based upon the configuration of register 8'h11[3:2] which selects a $t_{WK\_WIDTH\_INVALID}$ and $t_{WK\_WIDTH\_MIN}$ value. A WAKE input of less than $t_{WK\_WIDTH\_INVALID}$ is filtered out. If longer than $t_{WK\_WIDTH\_MIN}$, the device enters restart mode, and turn on the LDOs. The region between the two may or may not be counted, see Figure 8-21. Register 8'h12[7] determines the direction of the pulse or filter edge that is recognized. The default pulse detection is positive (low-high-low) but register 8'h12[7], WAKE_PULSE_CONFIG, can be set to '1b' to

detect a negative pulse (high-low-high) as well. The status of the WAKE pin can be determined from register 8'h11[5:4]. When a WAKE pin change takes place, the device registers this as a rising edge or falling edge. This is latched until a 00 is written to the bits.

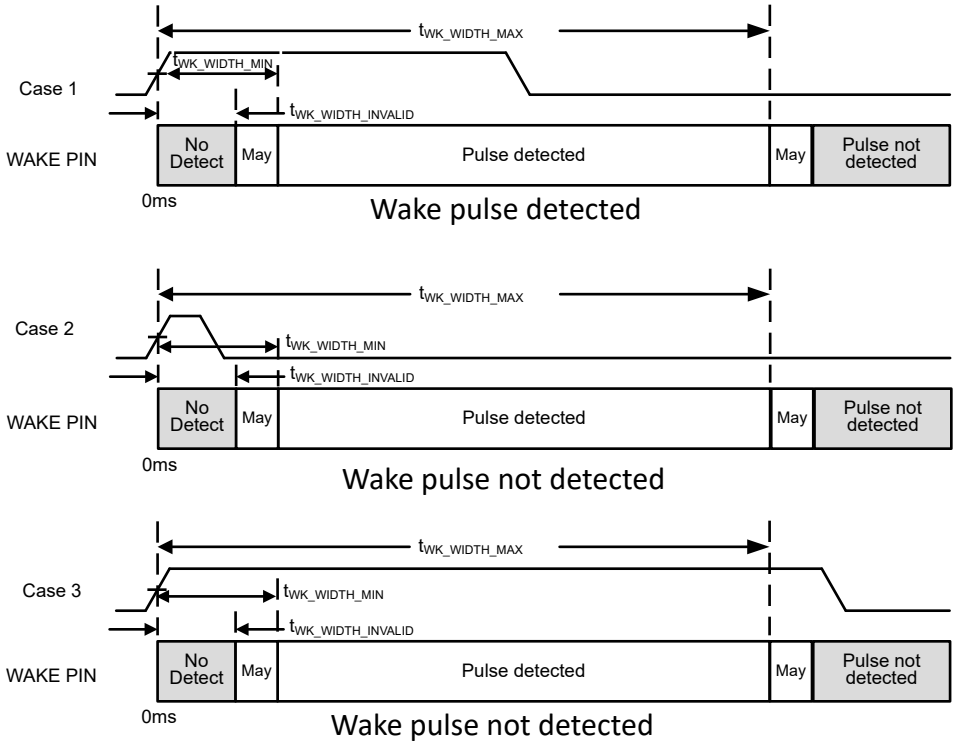


Figure 8-20. WAKE Pin Pulse Behavior (Positive pulse Example)

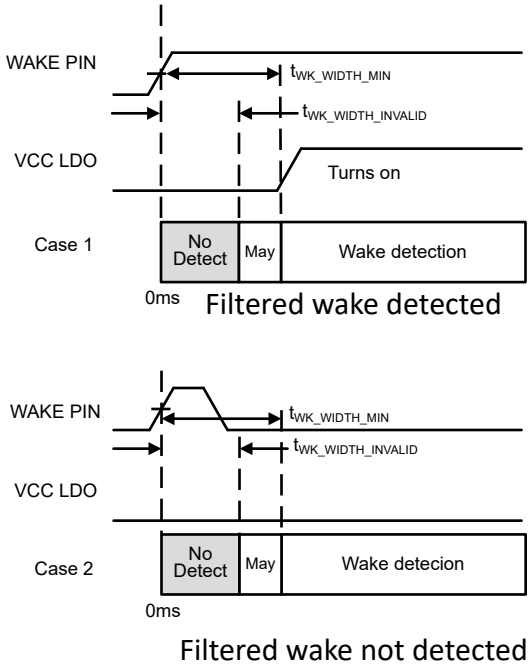


Figure 8-21. WAKE Pin Filtered Pulse Behavior

8.3.12.2.2 Cyclic Sensing Wake

Cyclic sense WAKE can be used to reduce the quiescent current of the device in sleep mode. When cyclic sensing WAKE is enabled, the quiescent current of the device is reduced because the WAKE circuitry is only active during the on time of HSS4.

Cyclic sensing wake is also supported in Standby mode. In Standby mode, the device only sets the corresponding wake pin interrupt. Cyclic sensing wake is not supported in Normal mode. TI recommends setting the WAKEx_SENSE bit to 0b before entering Normal mode to operate HSS4 in the SBC Normal mode.

To enable cyclic sensing wake:

- Connect the desired WAKE pins to HSS4 as shown in Figure 8-22
- Set the desired WAKEx pin to cyclic sensing mode
  - WAKE1: h’12[6] WAKE1_SENSE=1b
  - WAKE2: h’2B[7] WAKE2_SENSE=1b
  - WAKE3: h’2B[3] WAKE3_SENSE=1b
  - WAKE4: h’7B[7] WAKE4_SENSE=1b
- Set HSS4 to the desired timer using HSS4_CNTL bits
  - h'4D[2:0] = Timer1 or Time2
- Set the selected timer configuration with the desired on-time and period (Note: do not set the cyclic wake bit in the timer configuration unless cyclic wake needs to be configured in addition to cyclic sensing wake)
  - Set h'25 for Timer1 period and on-time
  - Set h'26 for Timer2 period and on-time

Verify that the configuration is complete before entering the Sleep mode. HSS4 turns on as soon as on-time is configured. HSS4 pin turns on per the selected period and on-time, applying VSUP to the external local wake circuitry. Each time this is done WAKEx sets a bit stating the pin is high or low and compares the bit to the previous state. If there has been a change, then the device wakes up: otherwise, it remains in sleep mode. See Figure 8-23 for a timing diagram. A filter time of t_{WK_CYC} is implemented as shown in Figure 8-23, determined by register 8'h12[5]. The filter time is applied at the end of the on-time and the wake input level should not cross the wake threshold during the filter time (wake input should be stable). This is implemented to ignore the transients and avoid false wake-ups.

Note

- REV_ID = 20h: Cyclic sensing wake does not function when CAN transceiver mode is programmed as off (CAN1_TRX_SEL = 000b). If CAN transceiver needs to be off in Sleep mode and cyclic sensing function is needed, program CAN1_TRX_SEL = 010b (SBC Mode Control WUP disabled)
- If HSS4 overcurrent or OVHSS faults occur during cyclic sensing wake, cyclic sensing wake may not function as expected

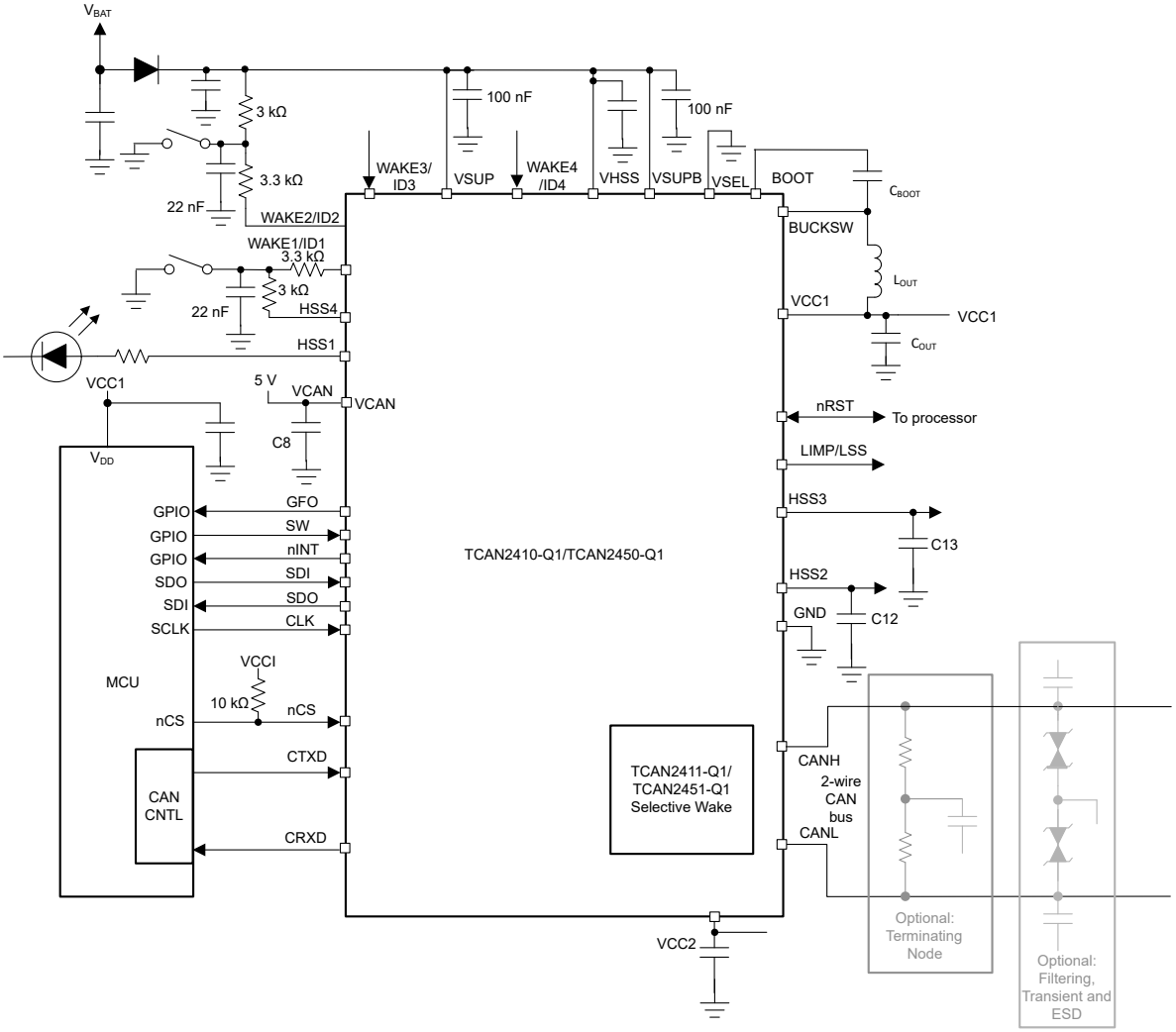


Figure 8-22. Application Drawing With Cyclic Sensing Configuration

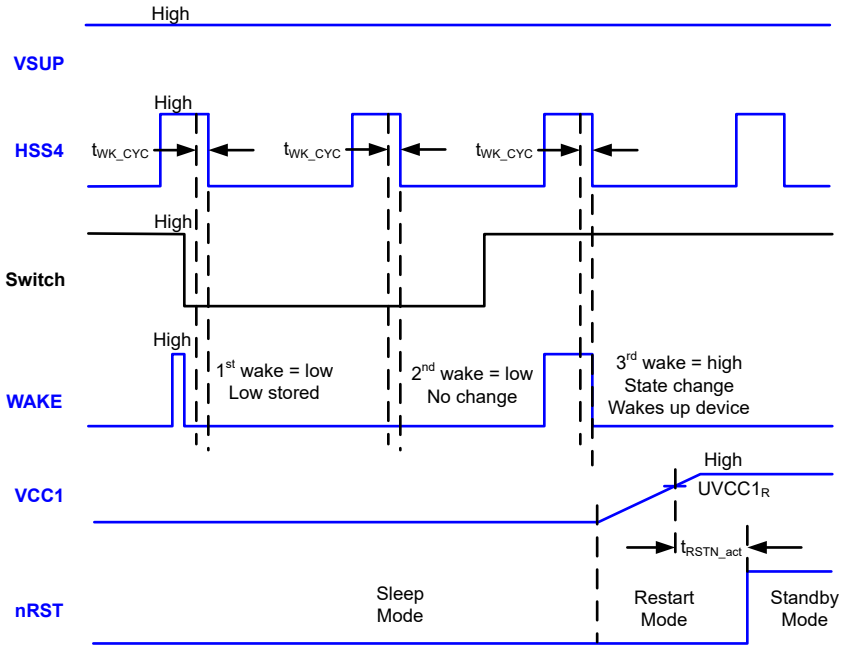


Figure 8-23. Cyclic Sensing Timing Diagram

8.3.12.3 Cyclic Wake

Cyclic Wake can be used to self-wake the device using timer1 or timer2 period without a need for an external wake event. This feature behaves in a specific manner depending upon the SBC mode the device is in and if enabled. This function is available in normal, standby, fail-safe and sleep modes. In normal and standby, at the start of the programmed on time, the device pulls nINT low for programmed-on time and release. The first on time pulse is ignored but each afterward causes the interrupt. Cyclic wake is enabled by using register 8'h25[3] for timer1 or 8'h26[3] for timer2.

This can be enabled in fail-safe mode by using register 8'h0E[6]=1b. As VCC1 is off in fail-safe mode, nINT pin is not used. When enabled, the period selected for the timer needs to be 500ms, 1s or 2s. When the on time takes place, the device determines if a fault is still present. If fault has not cleared, the device stays in fail-safe mode and repeats the process until the SWE timer times out at which time the device transitions to sleep mode. If fault has cleared, this is treated as a wake event and the device transitions to restart mode.

This feature can be enabled in sleep mode by setting register 8'h4F[4]=1b. In sleep mode, the device wakes up and transition to restart mode where the regulators are turned on. Once the device enters standby mode, the programmed long window starts and is expecting a WD trigger from the processor within this window. If this does not take place, the device transitions back to sleep mode. During this process, if a fault is detected the device transitions back to sleep mode.

8.3.12.4 Selective Wake-up

The TCAN245x-Q1 performs CAN communication according to ISO 11898-1 and Bosch CAN protocol specification 3.2.1.1.

8.3.12.4.1 Selective Wake Mode (TCAN2451-Q1)

This is the medium level of power saving mode of the device. The WUF receiver is turned on and connected internally to the frame detection logic is looking for a Wake-Up Frame (WUF) as outlined in the Frame Detection section of the data sheet. The CAN bus data is not put on the RXD pin in this state. The device is supplied via the VSUP supply coming from the system battery.

The valid wakes up sources in selective wake mode are:

- Wake-Up Frame (WUF)

- WAKE pin local wake up (LWU). Event on WAKE pin must match the programmed requirements for WAKE pin in register 8'h11[7:6]
- Frame Overflow (FRAME_OVF)
- SPI command to another state

If a WUF and/or LWU event occurs, the corresponding wake event flag (WUF and/or LWU) flag is set. At this point, an interrupt is provided to the MCU using the nINT pin if enabled or by pulling down the RXD pin.

To enter selective wake mode, the following conditions must be met:

- Selective Wake Configured, SWCFG, flag is set
  - Write all Selective Wake registers as followed by a read to make sure the programming is correct for the proper frame detection and selective wake configuration. Once configured, the SWCFG bit is set to 1b.
- Selective Wake Error, SWERR, flag is cleared
- Set Selective Wake Enable (SW_EN) = 1b, register 8'h10[7] = 1b

If a frame is incoming during the transition, the frame can be lost and frame detection can possibly not sync to the frames for an additional four incoming CAN frames.

Note

If a fault condition or FRAME_OVF forces the device into sleep mode, fail-safe mode disabled, or into fail-safe mode; SW_EN is disabled turning off selective wake function.

8.3.12.4.2 Frame Detection

The frame detection logic is what enables processing of serial data, or CAN frames, from the CAN bus. The device has Selective Wake Control Registers to set up the device to look for a programmed match using either the CAN ID (11 bit or 29 bit), or the CAN ID plus the data frame including data masking. If the detected CAN frame received from the bus matches the configured requirements in the frame detection logic, the condition is called a Wake-Up Frame (WUF).

Before Frame Detection may be enabled or used the data needed for validation, or match, of the WUF needs to be correctly configured in the device registers. Once the device has been correctly configured to allow frame detection, or selective wake function the SWCFG (Selective Wake Configuration) must be set to load the parameters for WUF for the device. If a valid WUF is detected, the WUF is shown via the CANINT flag, including selective wake up.

When Frame Detection is enabled, several other actions can take place as the logic is decoding the CAN frames the device receives on the bus. These include error detection and counting and the indication of reception of a CAN frame via the CAN_SYNC and CAN_SYNC_FD flags.

If a Frame Overflow (FRAME_OVF) occurs while in Frame Detection mode, the condition is disabled, clearing the SW_EN bit.

When Frame Detection is enabled transitioning from a mode where the receiver bias is not on up to four CAN frames for 500kbps and slower data rates and up to eight CAN frames for greater than 500kbps may be ignored by the device until the Frame Detection is stabilized.

The procedure to correctly configure the device to use frame detection and selective wake up is:

- Write all control registers for frame detection (selective wake), Selective Wake Config 1-4 (Registers 8'h44 through 8'h47), and ID and ID mask (Registers 8'h30 and 8'h40)
- Recommend reading all Selective Wake registers, allowing the software to confirm the device is properly written and configured
- Set Selective Wake Configured (SWCFG) bit to 1b, register 8'h47[7] = 1b
- Set Selective Wake Enable = 1b, register 8'h10[7] = 1b
- Set device into standby mode by SPI write to 8'h10[2:0] =100b. Step must be done even if already in standby mode.

If a SWERR interrupt occurs from the Frame Overflow flag, the Frame Overflow interrupt needs to be cleared, and then the SWCFG bit must be set again to 1b.

8.3.12.4.3 Wake-Up Frame (WUF) Validation

When the following conditions are all met the received frame are valid as a Wake-Up Frame (WUF):

- The received frame is a Classical CAN data frame when DLC (Data Length Code) matching is not disabled. The frame can also be a remote frame when DLC matching is disabled.
- The ID (as defined in ISO 11898-1:2015, 8.4.2.2) of the received Classical CAN frame is exactly matching a configured ID in the relevant bit positions. The relevant bit positions are given by an ID-mask illustrated in WUF DLC Validation
- The DLC (as defined in ISO 11898-1:2015, 8.4.2.4) of the received Classical CAN data frame is exactly matching a configured DLC. See the mechanism illustrated in WUF Data Validation. Optionally, this DLC matching condition can be disabled by configuration in the implementation.
- When the DLC is greater than 0 and DLC matching is enabled, the data field (as defined in ISO 11898-1:2015, 8.4.2.5) of the received frame has at least one bit set in a bit position which corresponds to a set bit in the configured data mask. See the mechanism illustrated in WUF DLC Validation.
- A correct cyclic redundancy check (CRC) has been received, including a recessive CRC delimiter, and no error (according to ISO 11898-1:2015, 10.11) is detected prior to the acknowledgment (ACK) Slot.

8.3.12.4.4 WUF ID Validation

The ID of the received frame matches the configured ID in all required bit positions. The relevant bit positions are determined by the configured ID in 8'h30 through 8'h33 and the programmed ID mask in 8'h34 and 8'h38. Classic Base Frame Format (CBFF) 11-bit Base ID and Classic Extended Frame Format (CEFF) 29-bit Extended ID and ID masks are supported. All masked ID bits except "do not care" must match exactly the configured ID bits for a WUF validation. If the masked ID bits are configured as "do not care" then both "1" and "0" are accepted in the ID. In the ID mask register a 1 represents “do not care”.

Figure 8-24 shows an example for valid WUF ID and corresponding ID Mask register

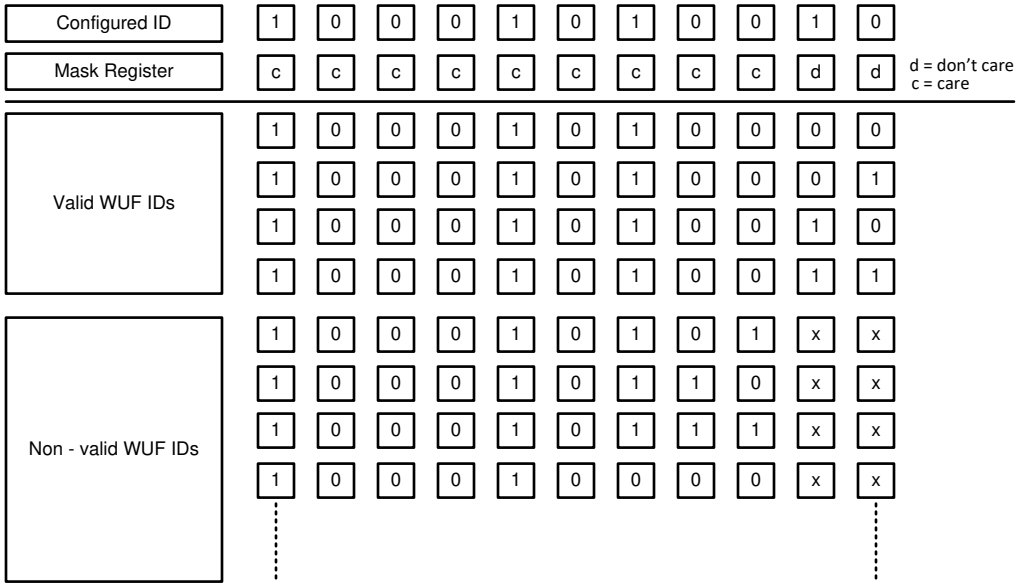


Figure 8-24. ID and ID Mask Example for WUF

8.3.12.4.5 WUF DLC Validation

The DLC (Data Length Code) of the received frame must match exactly the configured DLC if the data mask bit is set. The DLC is configured in 8'h38[4:1]. The data mask bit is set in 8'h38[0].

Table 8-8. DLC

Frames	Data Length Code				Number of Data Bytes
	DLC3	DLC2	DLC1	DLC0	
Classical Frames & FD Frames	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
Classical Frames	1	0 or 1	0 or 1	0 or 1	8

8.3.12.4.6 WUF Data Validation

When the Data mask is enabled via the data mask bit, the data of the received frame must match the configured Data where at least one logic high (1) bit within the data field of the received frame matches a logic high (1) of the data field within the configured data. The relevant bit positions are determined by the configured Data in 8'h39 through 8'h40 and enabled by Data mask enable in 8'h38[0]. An example of a matching and non-matching Data is shown in Figure 8-25

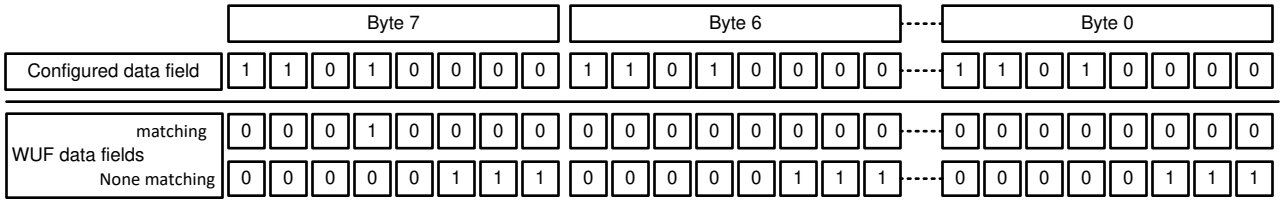


Figure 8-25. Data Field Validation for WUF Example

The selective wake data validation makes sure the last byte sent on the bus is interpreted as data mask byte 0. This means for 8 bytes of data, the first byte sent is interpreted as data mask byte 7. For a DLC of 3, the last byte sent on the bus is interpreted as data mask byte 0 and the first byte sent is interpreted as data mask byte 2. Figure 8-26 provides a few examples of which bytes are used for various bytes sent and received.

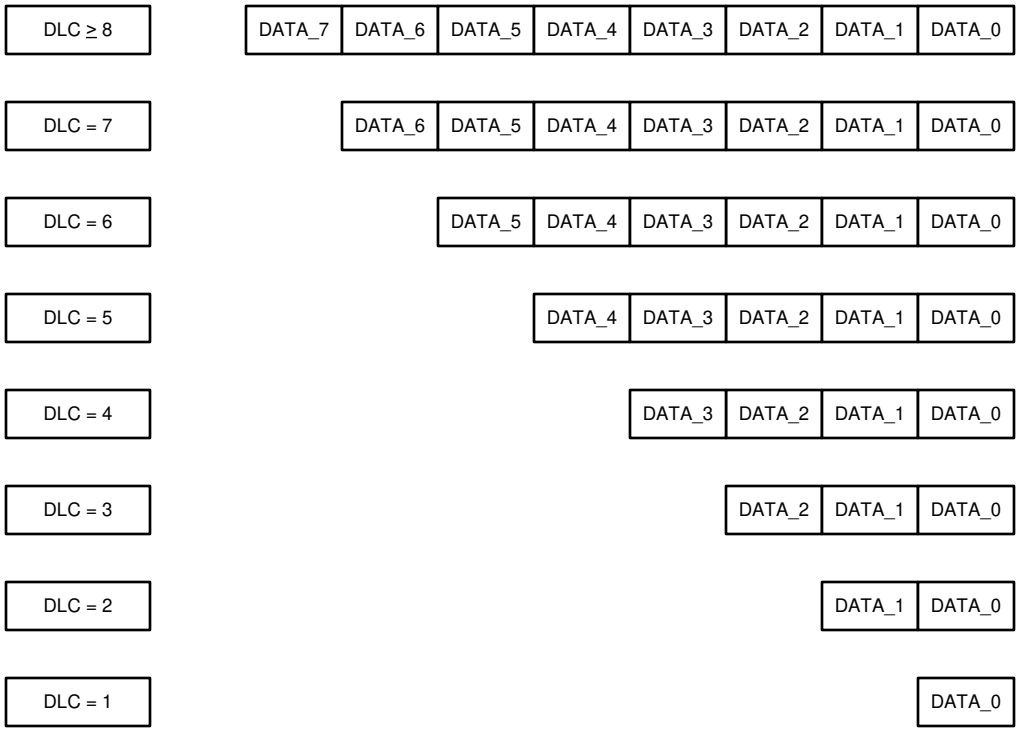


Figure 8-26. Data register mask values for different DLC values

8.3.12.4.7 Frame Error Counter

Upon activation of the selective wake up function and upon the expiration of $t_{SILENCE}$ the CAN frame error counter is set to zero. This error counter determines the CAN frame errors detected by the device. The error is in 8'h45, and the error counter is called FRAME_CNTx.

The initial counter value is zero and is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. If the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame has no impact on the frame error counter (no increment or decrement). If a valid Classical CAN frame has been received, and the counter is not zero, the counter shall be decremented by one. Dominant bits between the CRC delimiter and the end of the intermission field does not increase the frame error counter.

On each increment or decrement of the error counter, the decoder unit waits for nBits_idle recessive bits before considering a dominant bit as a start of frame (SOF). See Figure 8-27 for the position of the mandatory start of frame detection when classic CAN frame is received and in case of error scenario.

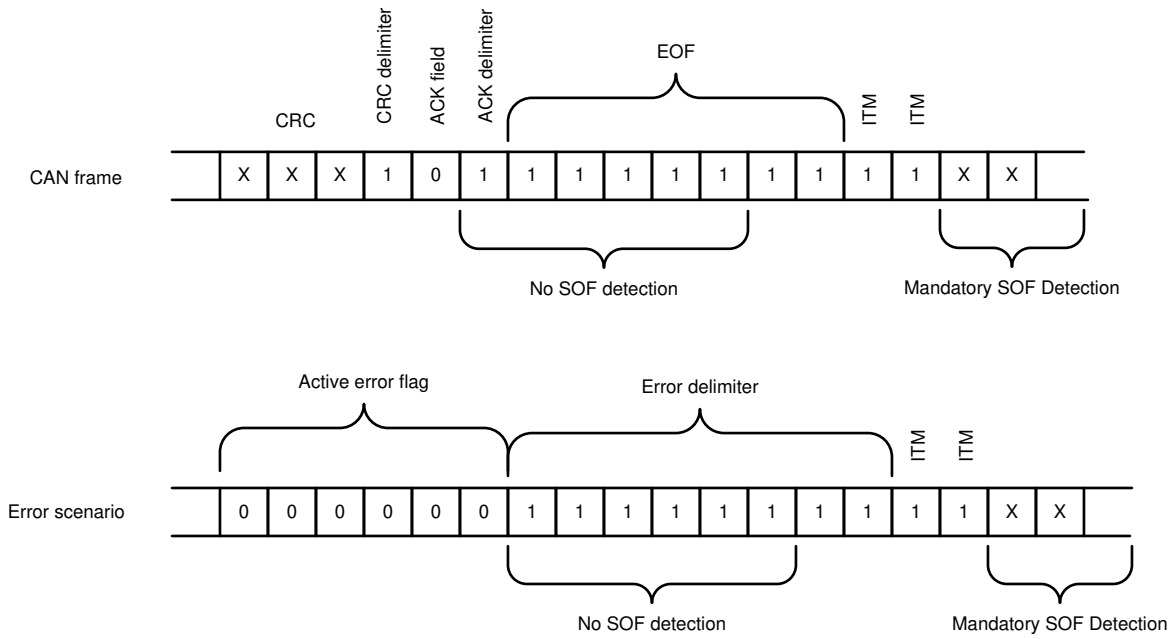


Figure 8-27. Mandatory SOF Detection After Classic CAN Frames and Error Scenarios

The default value for the frame error counter threshold is 31, so that on the 32nd error, the frame overflow flag (FRAME_OVF) is set.

Up to four (or eight when bit rate > 500kbps) consecutive Classic CAN data and remote frames that start after the bias reaction time, t_{Bias}, has elapsed can be either ignored, no error counter increase of failure, or judged as erroneous (error counter increases even in case of no error).

Received a frame in CEFF with non-nominal reserved bits (SRR, r0) are not led to an increase of the error counter.

The frame error counter compares to the frame error counter threshold, FRAME_CNT_THRESHOLD in 8'h46. If the counter overflows the threshold the frame error overflow flag, FRAME_OVF, is set. The default value for the frame error counter threshold is 31 so that on the 32nd error the overflow flag is set. However, if the application requires a different frame, program the required value for the error count overflow threshold into the FRAME_CNT_THRESHOLD register.

The counter is reset by the following: disabling the frame detection, CANSLNT flag set, and setting register 8'h51[2] = 1b.

The description for the errors detected:

- **Stuff bit error:** A stuff bit error is detected when the 6th consecutive bit of the same state (level) is received. CAN message coding has had a stuff bit at this bit position in the data stream.
- **CRC error:** The CRC sequence consists of the result of the CRC calculation by the transmitting node. This device calculates the CRC with the same polynomial as the transmitting node. A CRC error is detected if the calculated result is not the same as the result received in the CRC sequence.
- **CRC delimiter error:** The CRC delimiter error is detected when a bit of the wrong state (logic low or dominant) is received in the CRC delimiter bit position which is defined as logic high (recessive).

8.3.12.4.8 CAN FD Frame Tolerance

After receiving a FD Format indicator (FDF) followed by a dominant res bit, the decoder unit waits for n_{Bits_idle} recessive bits before considering a further dominant bit as a SOF as per Figure 8-27. Table 8-9 defines n_{Bits_idle}.

Table 8-9. Number of Recessive Bits Prior to Next SOF

Parameter	Notation	Value	
		Min	Max
Number of recessive bits before a new SOF is accepted	n_{Bits_idle}	6	10

There are two bitfilter options available to support different combinations of arbitration and data phase bit rates. Register 8'h47[4] is where the $p_{Bitfilter}$ option is selected.

- Bitfilter 1: A data phase bit rate ≤ four times the arbitration rate or 2Mbps whichever is lower shall be supported
- Bitfilter 2: A data phase bit rate ≤ ten times the arbitration rate or 5Mbps whichever is lower shall be supported

Dominant signals ≤ the minimum pBitfilter, see Table 8-10, of the arbitration bit time in duration is not considered valid and does not restart the recessive bit counter. Dominant signals ≥ the maximum of pBitfilter of the arbitration bit time duration restart the recessive bit counter.

Table 8-10. Number of Recessive Bits Prior to Next SOF

Parameter	Notation	Value	
		Min	Max
CAN FD data phase bitfilter 1	pBitfilter1	5.00%	17.50%
CAN FD data phase bitfilter 2	pBitfilter2	2.50%	8.75%

8.3.12.4.9 8Mbps Filtering

- Bitfilter 3: A data phase bit rate ≤ 16 times the arbitration rate or 8Mbps whichever is lower shall be supported
- pBitffilter 3 Min 1.25% to Max 4.375%

8.3.13 Protection Features

The TCAN245x-Q1 has several protections features that are described as follows.

8.3.13.1 Fail-safe Features

The TCAN245x-Q1has a fail-safe mode that can be used to reduce node power consumption for a node system issue. This can be separated into two operation modes, sleep and failsafe modes.

8.3.13.1.1 Sleep Mode Through Sleep Wake Error

The sleep wake error (SWE) timer is a timer used to determine if specific functions are working or if the communication between the device and the processor is present. SWE timer is disabled by default. The SWE timer can be enabled by setting SWE_EN, 8'h1C[7]=1b, if needed. See Figure 8-28 for information on which modes the SWE timer start in and when.

The device wakes up if the CAN bus provides a WUP or a local wake event takes place, thus entering standby mode. Once in standby mode, SWE timer starts. Any SPI command resets the SWE timer. If SWE timer expires after $t_{INACTIVE}$, the device re-enter sleep mode.

When in standby or normal mode, if the CANSLNT flag gets set due to inactivity on the CAN bus for $t_{SILENCE}$, the SWE timer starts. If CANSLNT_SWE_DIS=0, the CANSLNT flag must be cleared to reset the SWE timer. If CANSLNT_SWE_DIS=1, any activity on the CAN bus automatically resets the SWE timer.

Note

- When VCC1 is enabled on for sleep mode, a SWE timer time-out causes the device to transition to restart mode instead of sleep mode. This causes the nRST pin to be pulled low to reset the processor and set the WKERR and SMS interrupt flags.
- A SWE timer time-out does not impact VCC2 if enabled on for sleep mode.

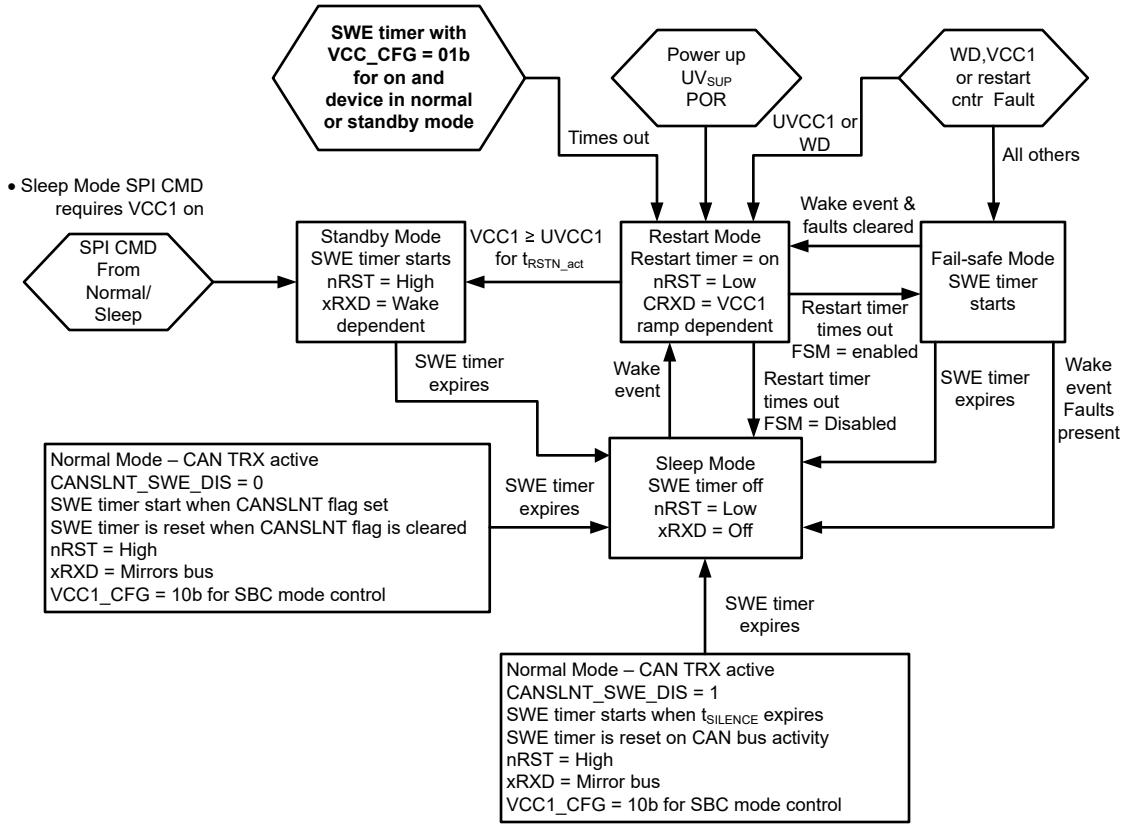
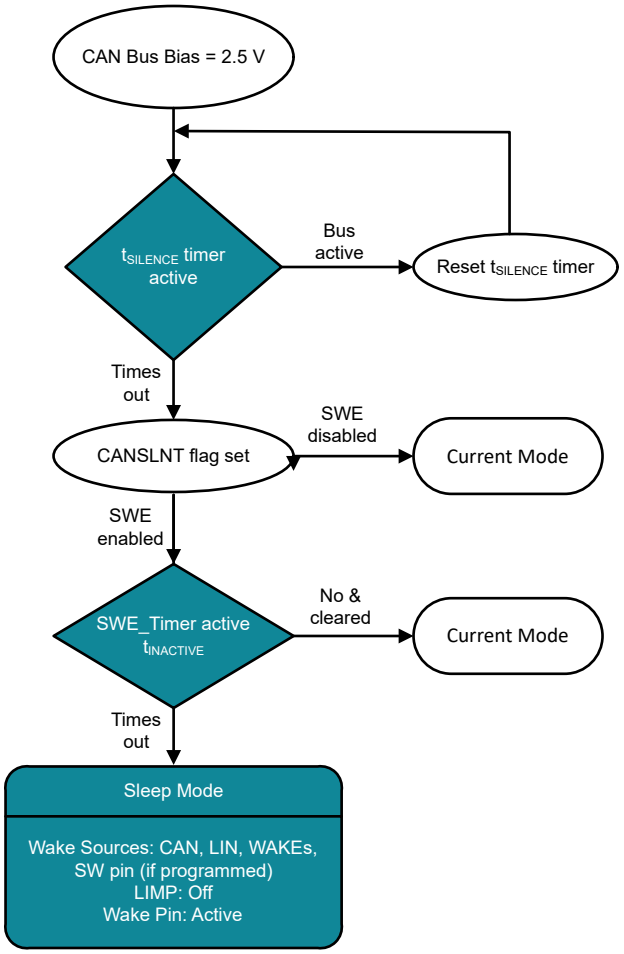


Figure 8-28. SWE Timer by Mode



Note

This figure is based upon the CAN FD transceiver being on or in listen only states.

Figure 8-29. Normal and Standby to Sleep Mode

8.3.13.2 Device Reset

The TCAN245x-Q1 family has three methods to reset the device. Two are accomplished with SPI commands and are a soft reset and hard reset. Soft reset and hard reset are accomplished by writing a 1b to DEVICE_RST register 8'h19[1] for soft reset or to 8'h19[0] for hard reset.

Hard reset can also be performed by pulling nRST low for t_{NRSTIN}, see Figure 8-30.

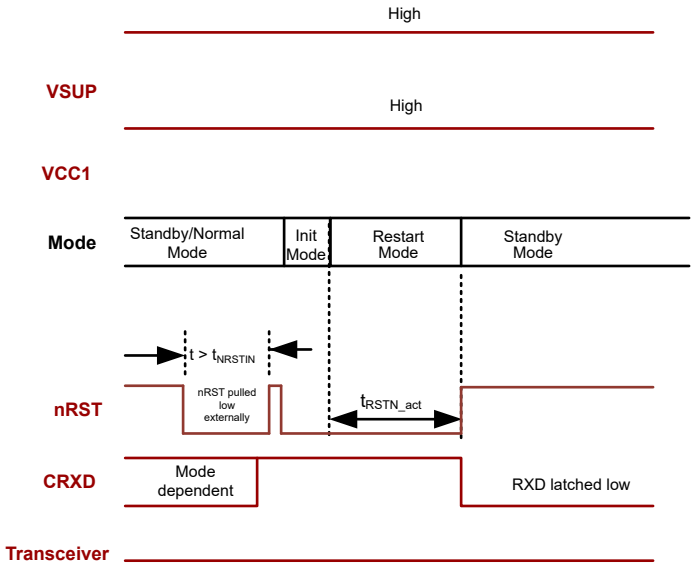


Figure 8-30. Performing Hard Reset with the nRST Pin

When performing a soft reset, the following takes place:

- Saved EEPROM registers are reloaded
- All other registers are reset to default values
- VCC1 and VCC2 do not change state
- Device transitions to standby mode

When performing a hard reset, the following takes place:

- Device transitions to Init mode
- Saved EEPROM registers are reloaded
- All other registers are reset to default values
- Most of the internal device logic is reset to default
- VCC1 and VCC2 do not change state
- Device then transitions to restart mode and finally to standby mode where the device can be reprogrammed

When pulling nRST pin low and releasing, the following takes place:

- Device transitions to Init mode
- Saved EEPROM registers are reloaded
- All other registers are reset to default values
- Most of the internal logic is reset to default
- VCC1 and VCC2 do not change state
- Device then transitions to restart mode and finally to standby mode where the device can be reprogrammed

Note

The recommended is for any changes to registers that are stored into EEPROM be saved to EEPROM. A reset causes these registers to be loaded from EEPROM. This overwrites unsaved changes with the last-saved register values from EEPROM.

8.3.13.3 Floating Terminals

There are internal pull ups and pull downs on critical terminals to place the device into known states if the terminal floats. See Table 8-11 for details on terminal bias conditions.

Table 8-11. Terminal Bias

TERMINAL	PULL-UP or PULL-DOWN	COMMENT
SW	60kΩ Pull-down or Pull-up	When SW pin is active high pin weakly biases input to GND When SW pin is active low pin weakly biases input to either VCC1 or internal voltage rail

Table 8-11. Terminal Bias (continued)

TERMINAL	PULL-UP or PULL-DOWN	COMMENT
SCK	60kΩ Pull-up Or Pull-down	Automatically configures to pull-up or pull-down based upon the SPI mode selected which weakly biases input • Mode 0 or 1 configures for pull-down • Mode 2 or 3 configures for pull-up
SDI	60kΩ Pull-up or Pull-down	Configured as either a pull-up or pull-down based upon SDI_POL configuration in SPI_CONFIG register 8'h09[2] which weakly biases input
nCS	60kΩ Pull-up	Weakly biases input so the device is not selected
nRST	30kΩ Pull-up	Pulled-up to VCC1
CTXD	60kΩ Pull-up	Weakly biases input

Note

Do not rely on the internal bias as the only termination, especially in noisy environments. Consider the internal bias as a fail-safe protection. Take special care when the device is used with MCUs with open drain outputs.

8.3.13.4 TXD Dominant Time Out (DTO)

The TCAN245x-Q1 supports dominant state time out on CAN bus. This is an internal function based upon the TXD path. The TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant (LOW) longer than the time out period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time out constant of the circuit, t_{TXD_DTO}, the bus driver is disabled. This frees the bus for communication between other nodes on the network. The driver is re-activated when a recessive signal (HIGH) is seen on TXD terminal; thus, clearing the dominant time out. The receiver remains active and the RXD terminal reflects the activity on the CAN bus terminal is biased to recessive level during a TXD DTO fault. This feature can be disabled by using register 8'h10[6] TXD_DTO_DIS for CAN.

Note

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame.

8.3.13.5 CAN Bus Short Circuit Current Limiting

These devices have several protections features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting (dominant and recessive). The device has TXD dominant time out which prevents permanently having the higher short circuit current of dominant state for a system fault. During CAN communication the bus switches between dominant and recessive states; thus, the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings, use the average short circuit current. The percentage dominant is limited by the TXD dominant time out and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and inter frame space. This makes sure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

Note

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. Calculate the average short circuit current using Equation 6.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times IOS(SS)\_REC) + (\%DOM\_Bits \times IOS(SS)\_DOM)] + [\%Recieve \times IOS(SS)\_REC] \quad (6)$$

Where

- $I_{OS(AVG)}$ is the average short circuit current.
- %Transmit is the percentage the node is transmitting CAN messages.
- %Receive is the percentage the node is receiving CAN messages.
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages.
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages.
- IOS(SS)_REC is the recessive steady state short circuit current and IOS(SS)_DOM is the dominant steady state short circuit current.

Note

Take into consideration the short circuit current and possible fault cases of the network when sizing the power ratings of the termination resistance, other network components, and the power supply used to generate VSUP.

8.3.13.6 Thermal Shutdown

The TCAN245x-Q1 has two thermal sensors in the device to monitor the junction temperature of the die.

1. TSD_SBC: Covers VCC1 buck regulator and high-side switches
2. TSD_CAN: Covers VCC2 LDO and CAN transceiver

There is a thermal shutdown pre-warning provided (TSDW interrupt) that is set when the junction temperature of the TSD_SBC thermal sensor hits the warning temperature level. There are two other interrupts for when the junction temperature of one of the sensors reaches the thermal shutdown temperature. The behavior of the device depends upon which sensor hits the TSD event. This is a device preservation feature.

- INT_6 register 8'h5C[7] is TSDW interrupt
- INT_2 register 8'h52[0] is TSD_SBC interrupt which covers the VCC1 buck regulator
- INT_3 register 8'h53[1] is TSD_CAN interrupt which includes VCC2 LDO

Exceeding the maximum junction temperature for > t_{TSD} causes interrupt flags to be set and is indicated by pulling nINT low. If TSD_SBC causes the TSD event (due to VCC1 or high-side switches); the device turns off the VCC1 regulator and enter either fail-safe mode (if enabled) or sleep mode. A thermal shut down interrupt flag (TSD_SBC) is set but not indicated on nINT pin as VCC1 is off. The nRST pin is pulled to ground during this TSD event. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the TSDF temperature for 1s, the device transitions from fail-safe mode to restart mode and turn on VCC1 (if enabled).

TSD_SBC fault also causes the high-side switches to be turned off by resetting the HSS1-4_CNTL registers. After the junction temperature has dropped below TSDF for 1s the high-side switches can be re-enabled.

If TSD is detected by the second sensor which covers the CAN transceiver and VCC2, CAN transmitter is disabled placing the transceiver into listen mode. VCC2 LDO is disabled and the interrupt flag is set. This does not cause an SBC state change. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the TSDF temperature, the CAN transmitter is re-enabled. After 1s of further wait time, VCC2 LDO is turned on. Note that UVCC2 is not set here because the LDO is disabled. Read VCC2_STATUS at register 8'h4F[2] to determine when VCC2 has been re-enabled. If VCC2 is used in the system as the supply source for VCAN, then the VCC2 off condition creates a UVCAN condition. The CAN transceiver changes to wake capable, and cannot be re-enabled until VCC2 is fully powered again. VCC2_STATUS is also indicating the status of VCAN. When VCC2_STATUS=1b, the CAN transceiver is re-enabled and UVCAN interrupt flag can be cleared.

8.3.13.7 Under and Over Voltage Lockout and Unpowered Device

The TCAN245x-Q1 monitors both input (VSUP, VHSS and VCAN) and output (VCC1 and VCC2). For the input supply rails, VSUP and VHSS are monitored for under-voltage and VHSS can be monitored for over-voltage. For the output supply rails, all are monitored for under-voltage, over-voltage and short circuit failures. Each of these fault events have a corresponding interrupt with VSUP and VCC1 faults causing device SBC mode changes. See Table 8-12 for the relationship between the device mode and the VSUP, VCC1 and VCC2 faults.

Table 8-12. Impact of VSUP, VCC1 and VCC2 Faults on Device Mode

VSUP	VCC1	VCC2	DEVICE MODE
> UVSUP	> UVCC1	> UVCC2	Normal or Standby
> UVSUP	< $UVCC1_{PR}$	> UVCC2	Previous
> UVSUP	< UVCC1	N/A	Restart
> UVSUP	N/A	< UVCC2	Previous
< UVSUP	N/A	N/A	UVSUP
> UVSUP	> OVCC1	N/A	Fail-safe or Sleep
> UVSUP	N/A	> OVCC2	Previous
> UVSUP	< VCC1SC	N/A	Fail-safe or Sleep
> UVSUP	> UVCC1	< VCC2SC	Previous

Note

OVHSS is not shown in the table as it only impacts the high-side switches.

- If a permanent fault on VCC1 takes place and fail-safe mode is disabled, getting into a loop between restart and sleep mode due to wake events and VCC1 SBC fault is possible.
  - The recommendation is to either enable fail-safe mode when VCC1 is programmed to be on for sleep mode or configure LIMP to be turned on in Sleep mode due to VCC1 faults.
  - To avoid the loop situation for a permanent fault with fail-safe mode enabled, the recommendation is to use FSM_CONFIG register 8'h17[7:4] = 0100b which is FSM_CNTR_ACT, and places the device into sleep mode with regulators turned off until a power cycle reset takes place.

The TCAN245x-Q1 monitors VCC1 and VCC2 for over-voltage condition. Over-voltage is represented by OVCC1 and OVCC2. The TCAN245x-Q1 monitors VCC1 and VCC2 for short to ground conditions. Short to ground is represented by $VCC1_{33SC}$, $VCC1_{5SC}$ and $VCC2_{SC}$.

The TCAN245x-Q1 monitors the high-side switches supply voltage, V_{HSS}, for over-voltage events. This can be disabled by writing 1b to 8'h4F[7], HSS_OV_DIS. Under-voltage is monitored on the HVSS supply, UVHSS. This can be disabled by writing 1b to 8'h4F[6], HSS_UV_DIS. The HSS switches automatically recovers from an OVHSS or UVHSS unless disabled by writing 1b to 8'h4F[5], HSS_OV_UV_REC.

8.3.13.7.1 Under-Voltage

The device monitors VSUP, VHSS, VCAN, VCC1 and VCC2 for under-voltage events. Under-voltage events are represented by $UVSUP_x$, UVHSS, UVCAN and UVCC2. VCC1 has a pre-warning, $UVCC1_{xPR}$, and a failure, $UVCC1_x$. The x is 33 (for 3.3V VCC1) or 5 (for 5V VCC1). As VCC1 is either 3.3V or 5V, there are different thresholds for each. As VCC1 is 3.3V or 5V, UVSUP has different thresholds for each one, $UVSUP_{33R/F}$ and $UVSUP_{5R/F}$. VSUPB supply is not monitored explicitly as VSUP and VSUPB must be connected on the board. In the case when VSUPB gets disconnected from VSUP, VCC1 experiences undervoltage event and the device eventually enters Fail-safe (if enabled) or Sleep mode (if Fail-safe mode is disabled).

The device also provides over voltage and short circuit (short to GND) protection on the VCC1 and VCC2. Once OVCC1 or $VCC1_{33/5SC}$ are detected, the device enters Fail-safe or Sleep mode depending upon device set up. As the transceivers are programmed independently from the device modes, the behavior of the transceivers is not covered here. Table 8-13 provides the device mode based upon VCC1 and VCC2 under fault conditions.

Table 8-13. VSUP, VCC1 and VCC2 Faults

VSUP	VCC1	VCC2	DEVICE MODE
> UVSUP	> UVCC1	> UVCC2	Normal or Standby
> UVSUP	< $UVCC1_{PR}$	> UVCC2	Previous
> UVSUP	< UVCC1	N/A	Restart
> UVSUP	N/A	< UVCC2	Previous
> UVSUP	N/A	N/A	Previous
< UVSUP	N/A	N/A	UVSUP
> UVSUP	> OVCC1	N/A	Fail-safe or Sleep (OVCC1_ACTION=0b) Previous (OVCC1_ACTION=1b)
> UVSUP	N/A	> OVCC2	Previous
> UVSUP	< VCC1SC	N/A	Fail-safe or Sleep
> UVSUP	N/A	< VCC2SC	Previous

Note

VSUP, VCC1 and VCC2 Faults does not show OVHSS because OVHSS only impacts the high-side switches.

8.3.13.7.1.1 VSUP and VHSS Under-voltage

VSUP is the primary input supply rail required for the device to function properly. There are three voltage levels monitored by the device-power on reset and two under-voltage levels. For all functions and output voltage rails to be in regulation, the VSUP rail must exceed $UVSUP_{5R}$. If VSUP is in under-voltage, the device loses the supply source needed to keep the internal regulators in regulation. If VSUP keeps ramping down and drops below $VSUP_{(PU)F}$, the device enters powered off state. When VSUP returns, the device comes up as if the initial power is on. All registers are cleared and the device has to be reconfigured from the stored EEPROM values that were retained. Please see the power brown-out diagrams Figure 10-3, Figure 10-4, Figure 10-6, and Figure 10-6 for further information.

When VCC1 is configured for 5V output, $UVSUP_{5R/F}$ is the only VSUP under-voltage rail monitored. When VSUP drops below $UVSUP_{5F}$, The CAN transceiver is turned off and the device enters a protected UVSUP state. VCC2 LDO is in pass thru mode and can trigger UVCC2 event. The VCC1 regulator is in a maximum duty cycle switching mode and can trigger a UVCC1 event depending upon the chosen UVCC1 threshold. See Table 8-14 for relationship between VSUP, $VCC1_5$, VCAN, device mode and the CAN transceiver.

When VCC1 is configured for 3.3V output, both $UVSUP_{33R/F}$ and $UVSUP_{5R/F}$ are monitored. When powering up, VSUP has to exceed $UVSUP_{33R}$ for VCC1 to be in regulation and above $UVSUP_{5R}$ for VCC2 and other functions of the device to work properly. When VSUP is ramping down, $UVSUP_{5F}$ is the first UVSUP level that sets an UVSUP5 interrupt flag, register 8'h52[4], and turns off the CAN transceiver. If VSUP keeps dropping, the next level is $UVSUP_{33F}$. When this is reached, the $UVSUP_{33}$ interrupt flag is set, register 8'h52[3] and the device enters UVSUP mode. See Table 8-15 for relationship between VSUP, $VCC1_{33}$, VCAN, device mode and the CAN transceiver.

Under-voltage on the high-side switches power, VHSS, is indicated by interrupt INT_4 register 8'5A[0] UVHSS. The behavior of high-side switches due to an UVHSS event is determined by HSS_CNTL3 register 8'h4F[6:5].

Table 8-14. Under-voltage Events for $VCC1_5$, Device State and Transceiver State

VSUP	VCC1	VCAN	DEVICE STATE	CAN TRANSCEIVER
> $UVSUP_5$	> $UVCC1_5$	> UVCAN	Normal or Standby	As Programmed
> $UVSUP_5$	< $UVCC1_5$	N/A	Restart	Wake capable or off
> $UVSUP_5$	> $UVCC1_5$	> UVCAN	Previous State	As Programmed
< $UVSUP_5$	> N/A	N/A	UVSUP	Off

Table 8-14. Under-voltage Events for $VCC1_5$, Device State and Transceiver State (continued)

VSUP	VCC1	VCAN	DEVICE STATE	CAN TRANSCEIVER
> $UVSUP_5$	< $UVCC1_5$	< UVCAN	Restart	Listen Mode

Table 8-15. Under-voltage Events for $VCC1_{33}$, Device State and Transceiver State

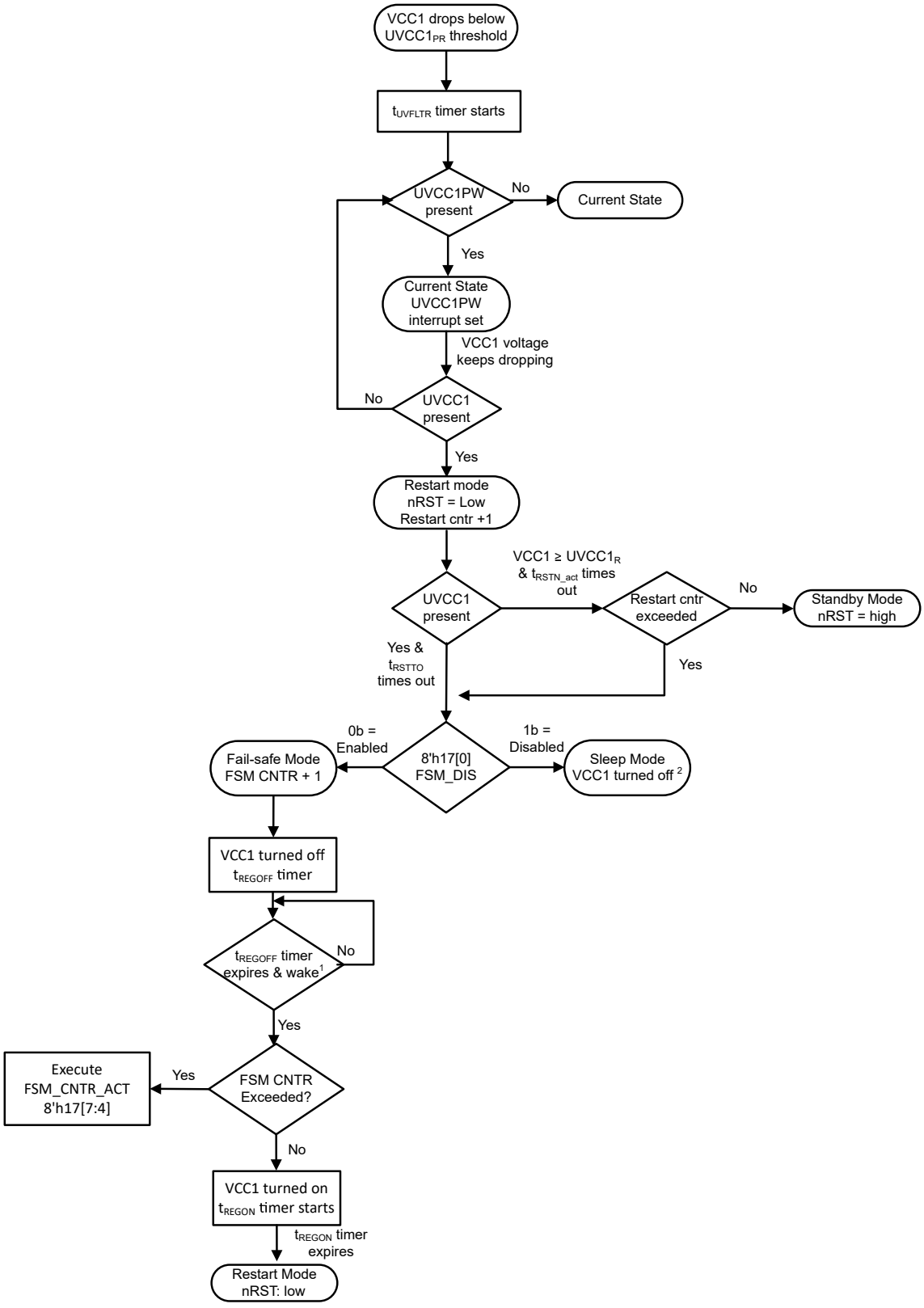
VSUP	VCC1	VCAN	DEVICE STATE	CAN TRANSCEIVER
> $UVSUP_5$	> $UVCC1_{33}$	> UVCAN	Normal or Standby	As Programmed
> $UVSUP_5$	< $UVCC1_{33}$	N/A	Restart	Wake capable or off
> $UVSUP_5$	> $UVCC1_{33}$	> UVCAN	Previous State	As Programmed
< $UVSUP_5$ > $UVSUP_{33}$	> $UVCC1_{33}$	N/A	Normal or Standby	Off
< $UVSUP_5$ > $UVSUP_{33}$	< $UVCC1_{33}$	N/A	Restart	Off
< $UVSUP_{33}$	N/A	N/A	UVSUP	Off
> $UVSUP_5$	> $UVCC1_{33}$	< UVCAN	Normal or Standby	Wake capable or off

Note

- If a thermal shut down or short circuit event takes place while the regulator is in UV, the device transitions to sleep mode (fail-safe mode disabled) or fail-safe mode if enabled.
- When UVCC1 does not clear within restart timer, the device enters fail-safe mode, if enabled. If fail-safe mode is disabled, the device transitions to sleep mode and turn off VCC1. When VCC1 is enabled on for sleep mode, an UVCC1 event proceeds in the same manner.
- OV/UVHSS is not shown in the table as only impacts the high-side switches.

8.3.13.7.1.2 VCC1 Under-Voltage

VCC1 power rail provides power for the digital input or output pins and is expected to be connected to the node processor. VCC1 is monitored for under-voltage and has two levels that are monitored, pre-warning ($UVCC1_{xPR}$) and under-voltage ($UVCC1_{XXR/FX}$). The under-voltage has one of four levels that can be programmed using register 8'h0E[4:3], UVCC1_SEL. Of the supply rails providing external power, VCC1 is the only one considered an SBC fault which causes a state change. When the under-voltage pre-warning event takes place an interrupt is set, INT_6 register 8'h5C[6] and the nINT pin is pulled low. Once VCC1 reaches one of the programmed thresholds, SBC_CONFIG1 register 8'h0E[4:3], the device transitions to restart mode and latch nRST low until VCC1 exceeds the under-voltage rising threshold. nRST remains latched low, and the device stays in restart mode for t_{RSTN_act} after clearing the UV threshold. For UVCC1, there is a filter time, $t_{UVFLTR,}$ that the under-voltage event must last longer than for the device to enter restart mode, See Figure 8-31 for UVCC1 behavior.



If the exit events do not take place before the SWE timer timeouts the device will enter sleep mode

Note

1. When VCC1_CFG = 01b for VCC1 always on, a wake event is not needed to exit the fail-safe mode. The device exits the fail-safe mode after t_{REGOFF} timer expires.
2. If Sleep mode is entered when Restart counter is exceeded (due to FSM_DIS=1b), VCC1 stays ON if VCC1-CFG=01b

Figure 8-31. UVCC1 State Diagram

8.3.13.7.1.3 VCC2 Under-voltage

A UVCC2 sets the interrupt flag (Register INT_6; 8'h5C[2]), but does not cause a mode change. See Figure 8-32 for under-voltage behavior.

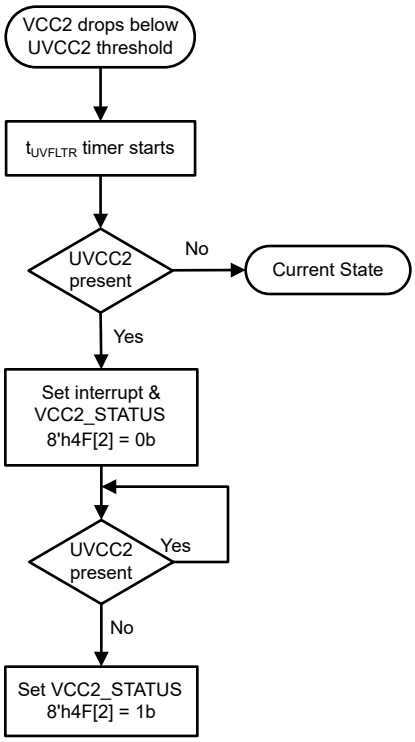


Figure 8-32. UVCC2 State Diagram

8.3.13.7.1.4 VCAN Under-voltage

If VCAN drops below UVCAN under-voltage detection, the CAN driver switches off and disengages from the bus until VCAN has recovered. See Figure 8-33 on how the device behaves. The device is designed to be an "passive" or “no load” to the CAN bus if the device is unpowered. The bus terminals (CANH, CANL) have low leakage currents when the device is unpowered, so the terminals do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational. Logic terminals also have extremely low leakage currents when the device is unpowered, so the terminals do not load other circuits which may remain powered.

The UVLO circuit monitors both rising and falling edge of a power rail when ramping and declining.

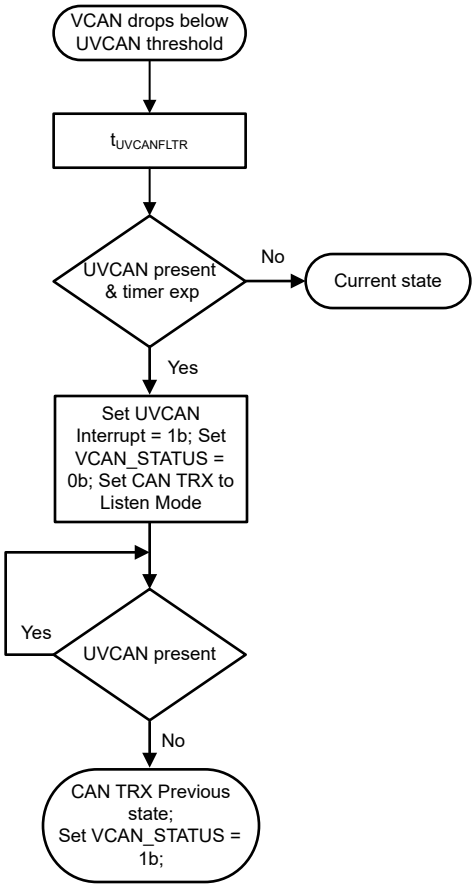


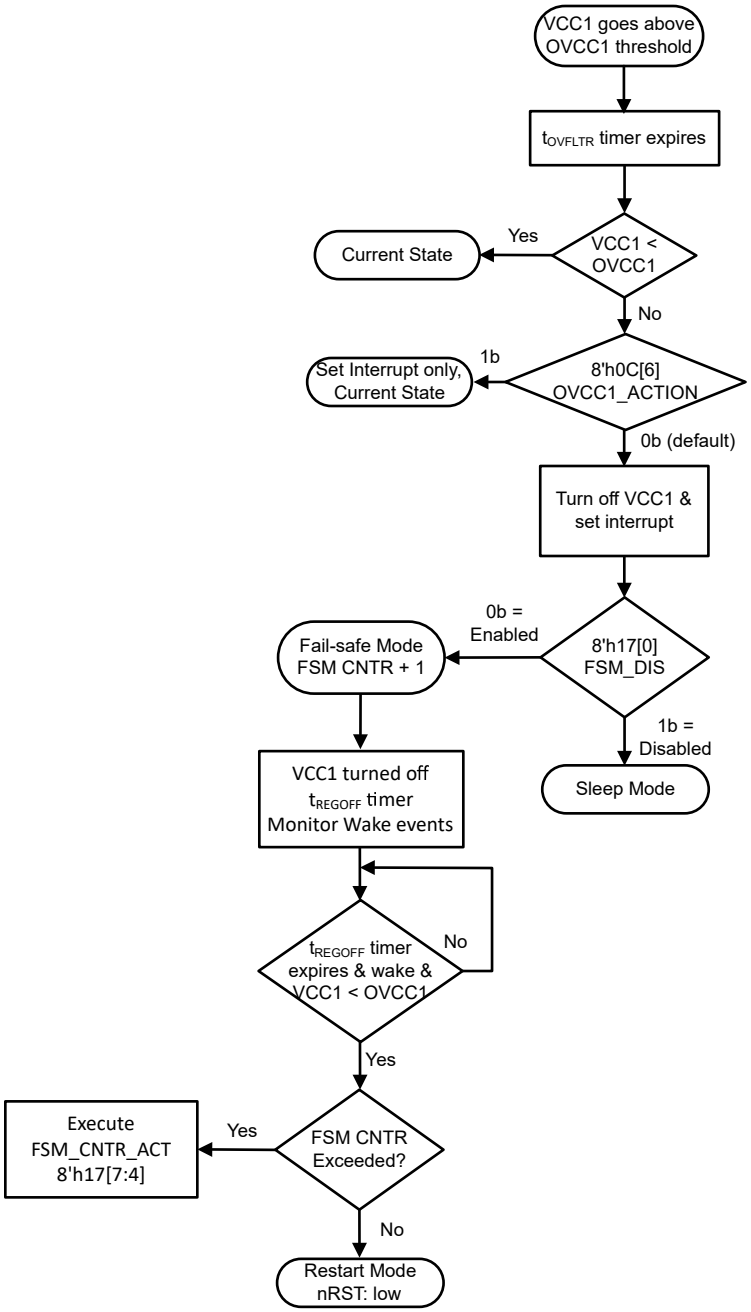
Figure 8-33. UVCAN State Diagram

Note

- UVCAN comparator is only enabled in the SBC Normal and Standby modes.
- VCAN is required for EEPROM writes, so VCAN_STATUS = 1b at register 8'h4F[1] needs to be checked before writing to the EEPROM.

8.3.13.7.2 VCC1 and VCC2 Over-voltage

TCAN245x-Q1monitors VCC1 and VCC2 for over-voltage condition. Over-voltage is represented by OVCC1 and OVCC2. If OVCC1_ACTION (8'h0C[6]) is 0b (default) and OVCC1 occurs, VCC1 is turned-off and the device enters either fail-safe mode, if enabled, or sleep mode. The device can be configured to only set an OVCC1 interrupt and not enter fail-safe or sleep mode by setting OVCC1_ACTION to 1b. When OVCC2 takes place, the LDO is turned off and an interrupt flag is set but no mode change takes place. When entering fail-safe mode, the device turns off all the regulators and starts the t_{REGOFF} timer. After this timer times out, OVCC1 is checked for over-voltage. If the OV event has cleared, and a wake event has taken place, the device enters restart mode. If OVCC1 is still present, the device remains in fail-safe mode. Wake events are monitored but not acted upon until t_{REGOFF} time out. If no wake event has taken place and the OV event has cleared, the device is still in fail-safe mode until the SWE timer times out or a wake event takes place. See Figure 8-34 and Figure 8-35 for device behavior during an over-voltage event.



If the exit events do not take place before the SWE timer timeouts the device will enter sleep mode

Note

When VCC1_CFG = 01b for VCC1 always on, a wake event is not needed to exit the fail-safe mode. The device exits the fail-safe mode after t_{REGOFF} timer expires.

Figure 8-34. OVCC1 State Diagram

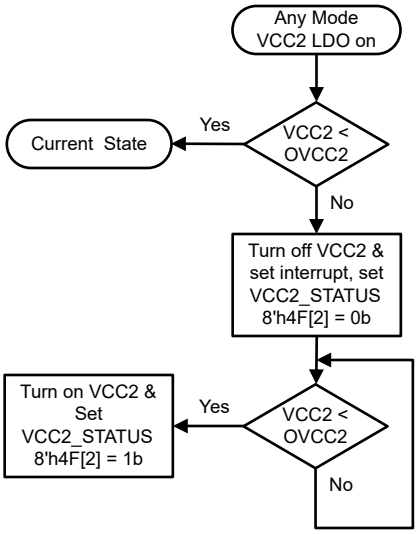


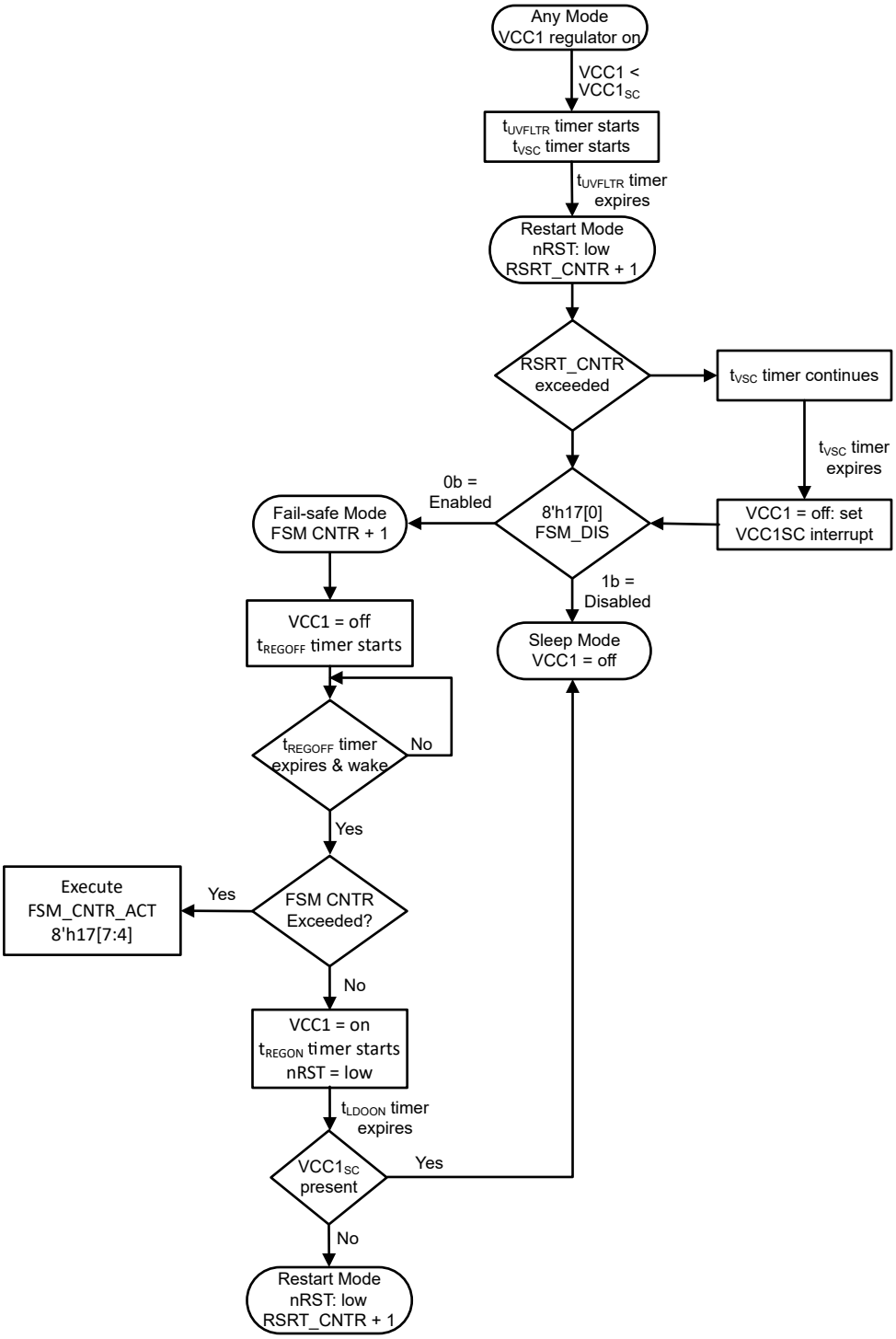
Figure 8-35. OVCC2 State Diagram

8.3.13.7.3 VCC1 and VCC2 Short Circuit

The TCAN245x-Q1monitors VCC1 and VCC2 (CAN LDO) for short to ground conditions. Short to ground is represented by $VCC1_{33SC}$, $VCC1_{5SC}$ and $VCC2_{SC}$. A short to ground turns off the integrated regulators. On VCC1 supply, a short is detected when the VCC1 voltage is below the set UVCC1 threshold for a period longer than $t_{VSC-VCC1}$. On VCC2 supply, a short is detected when the VCC2 voltage is below the set UVCC2 threshold for a period longer than $t_{VSC-VCC2}$

.

When a $VCC1_{SC}$ occurs, VCC1 is turned off for a minimum of t_{REGOFF}, and the device enters fail-safe mode (if enabled) or sleep mode. During this time, wake events are monitored and preserved. A short circuit event cannot be monitored while the LDO is off. A wake event causes VCC1 to be turned on for t_{REGON} to see if the SC event is still present. If still present, the device transitions to sleep mode. If not present, the device transitioned to restart mode. While in fail-safe mode, the SWE timer starts and if the fault is not cleared and a wake event has not taken place before the timer times out the device transitions to sleep mode. If fail-safe mode is disabled, the device transitions to sleep mode. See Figure 8-36 and Figure 8-37 for device behavior during a short to ground event.



Note

When VCC1_CFG = 01b for VCC1 always on, a wake event is not needed to exit the fail-safe mode. The device exits the fail-safe mode after t_{REGOFF} timer expires.

Figure 8-36. $VCC1_{SC}$ State Diagram

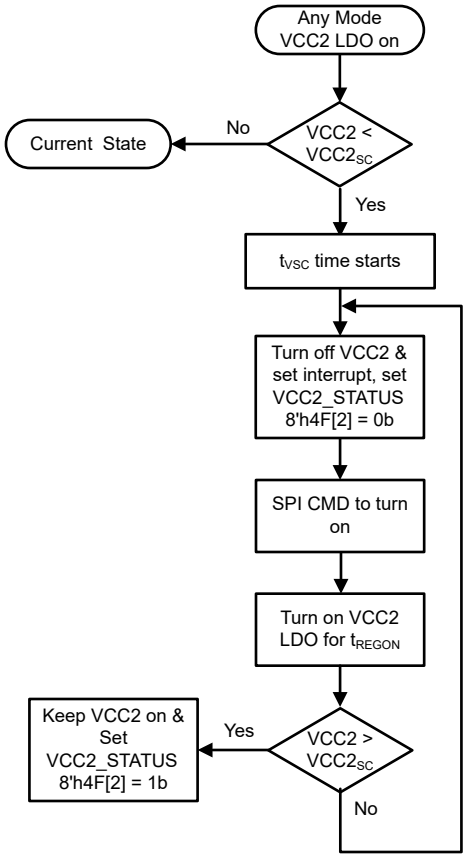


Figure 8-37. $VCC2_{SC}$ State Diagram

8.3.13.8 Watchdog

The TCAN245x-Q1 has an integrated watchdog function. The device provides a default window based, time-out and question and answer (Q&A) watchdog using SPI programming at WD_CONFIG_1 register 8'h13[7:6], WD_CONFIG. The watchdog configuration and type can only be programmed when the device is in standby mode. Normal mode supports all three watchdog configurations while standby mode defaults to timeout. When the device enters standby mode, the watchdog configuration automatically changes to a timeout watchdog. The standby mode watchdog can be configured to the same type as normal mode by programming register 8'h13[2] = 1b. The watchdog is default off in sleep mode but can be configured to be active as a timeout watchdog by programming WD_SLP_EN at register 8'h13[3] = 1b. Figure 8-40 provides flow chart for the behavior of the device when the watchdog is enabled or disabled in Sleep mode.

When entering standby mode from restart mode, there is a nRST transition from low to high. This transition starts the t_{INITWD} timer, and includes the t_{RSTN_act} timer in restart mode. A WD trigger input must take place prior to this initial long window times out. See The initial long window defaults to 600ms, but can be programmed to other values, WD_LW_SEL at register 8'h13[1:0]. See Figure 8-38 for the timing diagram. Once the long window watchdog is served, the watchdog configured in the Standby mode starts immediately.

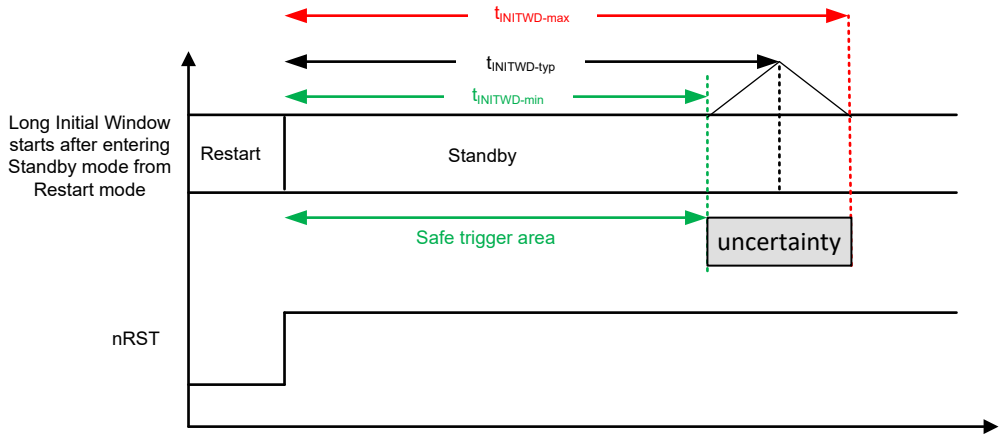


Figure 8-38. Long Window Watchdog Timing Diagram

When entering normal mode, the programmed watchdog timer starts based upon the programmed configuration. The watchdog timer is off in sleep, restart and fail-safe modes. The LIMP pin provides a limp home capability. When in sleep mode, the LIMP pin is off. When the error counter exceeds the watchdog trigger event level, the LIMP pin turns pulling the LIMP pin to ground as described in the LIMP pin section. The watchdog has extensive configurability including the ability to select the time-out or Q&A watchdog. Watchdog is default enabled for standby mode, but can be disabled by setting register 8'h14[0] = 1b. Register 8'h13[7:6] can be set to 00b to disable the WD. There is a WD error counter available, see Section 8.3.13.8.1 for description of this counter.

Figure 8-39 provides a flow chart on the watchdog in Standby mode.

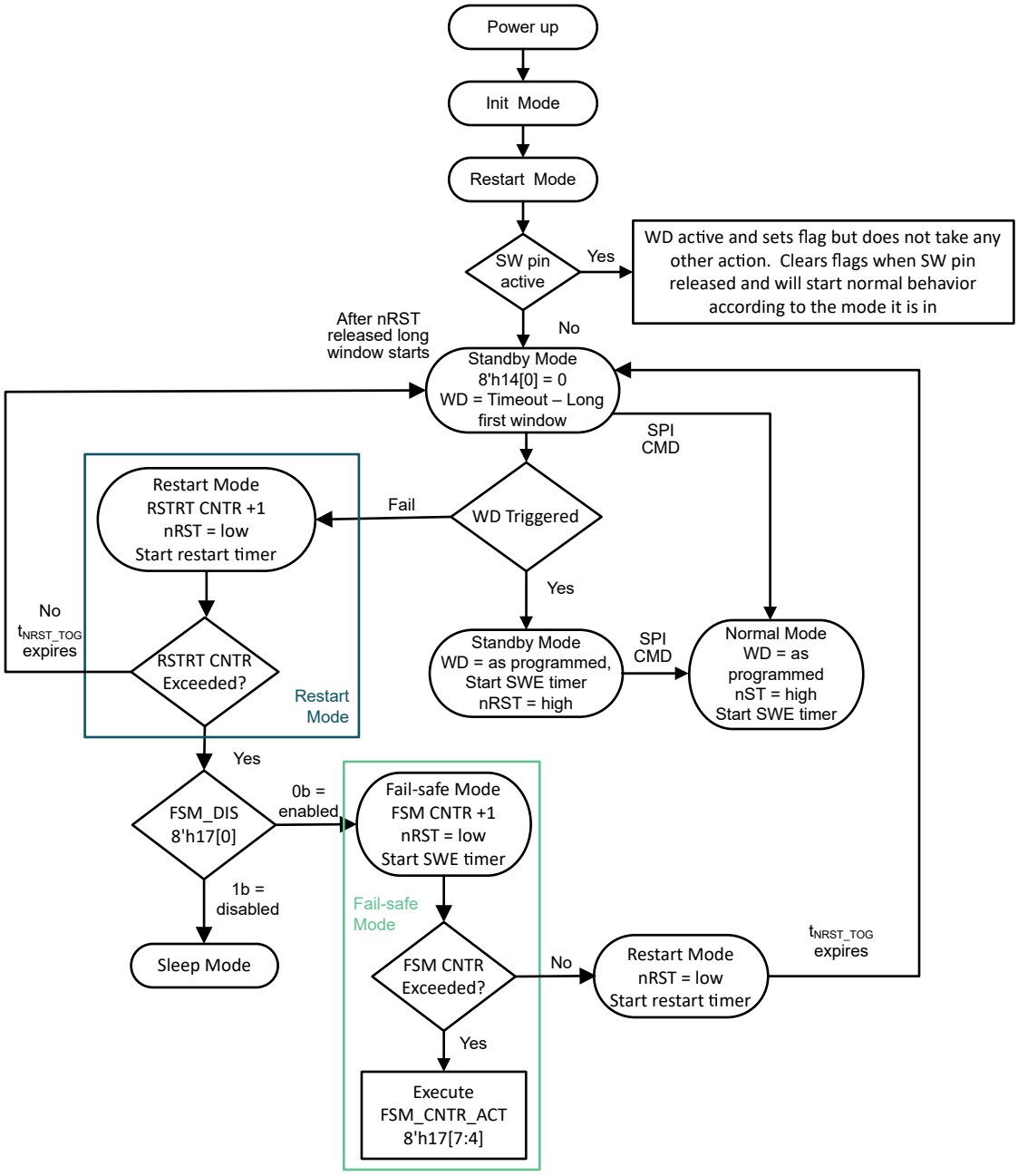


Figure 8-39. Watchdog in Standby Mode

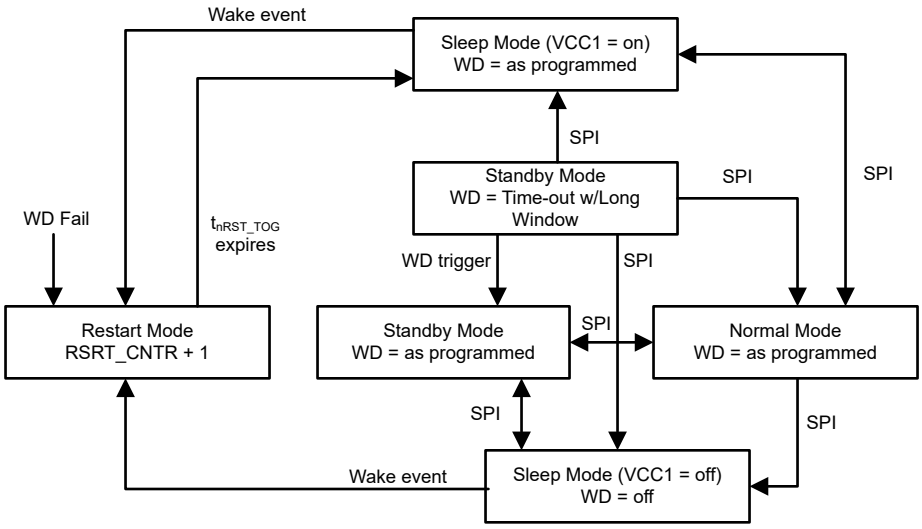


Figure 8-40. Watchdog in Sleep Mode

Note

- When the SBC mode is changed, the watchdog timer does not restart as long as the watchdog type is the same between the SBC modes. If the watchdog type is configured to be different between SBC modes, the watchdog timer restarts on SBC mode change. In such cases, the recommendation is to trigger the watchdog in the current SBC mode just before changing to Normal mode to avoid a watchdog error by missing the safe trigger window.
- When changing the WD timer value from a longer value to a shorter value, it is recommended to provide a WD trigger before programing the shorter value to avoid a WD error.

8.3.13.8.1 Watchdog Error Counter and Action

The TCAN245x-Q1 has a watchdog error counter. This counter is an up down counter that increments for every missed window or incorrect input watchdog trigger event. For every correct input trigger, the counter decrements but does not drop below zero. The default trigger for this counter is to trigger a watchdog event is for every event. This counter can be configured at register 8'h16[7:4] which sets the limit for incorrect input triggers up to 15. The error counter can be read at register 8'14[4:1].

Once the programmed WD error counter limit has been exceeded, the device transitions to restart mode which pulls nRST low for t_{NRST_TOG}. The error counter resets back to 0 at this point. Once t_{NRST_TOG} times out, the device transitions back to standby mode releasing nRST high. If the WD failure causes the restart counter to exceed its programmed limit, the device transitions to either fail-safe mode if enabled or to sleep mode.

8.3.13.8.2 Watchdog SPI Programming

Registers 8’h13 through 8’h15 control the watchdog function. The watchdog can be set as a time-out watchdog or window watchdog by setting 8’h13[6] to the method of choice. The timer is based upon registers 8’h13[5:4] WD prescalar and 8’h14[7:5] WD timer and is in ms. See Table 8-16 for the achievable times. If using smaller time windows, the suggestion is to use the Time-out version of the watchdog. This is for times between 4ms and 64ms.

Table 8-16. Watchdog Window and Time-out Timer Configuration (ms)

WD_TIMER (ms)	8'h13[5:4] WD_PRE			
8'h14[7:5]	00	01	10	11
000	4	8	12	16
001	32	64	96	128
010	128	256	384	512

Table 8-16. Watchdog Window and Time-out Timer Configuration (ms) (continued)

WD_TIMER (ms)	8'h13[5:4] WD_PRE			
011	256	384	512	768
100	512	1024	1536	2048
101	2048	4096	6144	8192
110	10240	20240	RSVD	RSVD
1111	RSVD	RSVD	RSVD	RSVD

Note

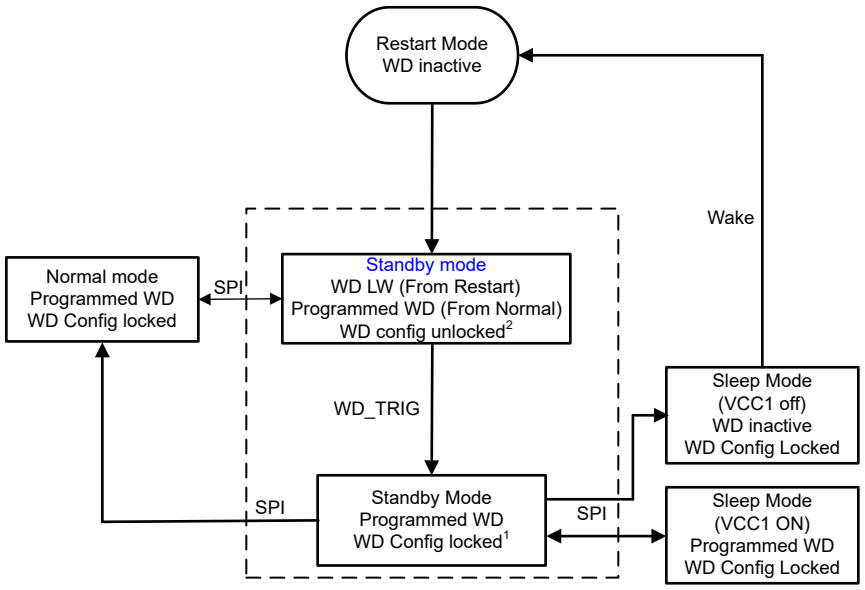
If timing parameters are changed while the watchdog is running, the WD timer restarts to the new window automatically.

8.3.13.8.2.1 Watchdog Configuration Lock Mechanism

To avoid inadvertent watchdog configuration changes, the TCAN245x-Q1 family implements a watchdog configuration register locking and unlocking mechanism. Registers 8'h13, 8'h14, 8'16 and 8'h2D are only programmable in standby mode and are the registers that become locked. These registers automatically lock with the first WD input trigger event or when transitioning to normal mode via SPI command. The watchdog can be unlocked for programming again by transitioning to standby mode; which allows one write to each of the four registers. If the registers are locked while in standby mode, there are two ways to unlock the configuration registers:

- SW pin activation: The watchdog registers remain unlocked as long as the SW pin is active in Standby mode
- By transitioning the device to any other mode and back to Standby mode.

The WD can be enabled in sleep mode and is only capable of timeout and the configuration registers are locked. See Figure 8-41 which shows the described behavior.



1 As long as SW pin is active in Standby mode, WD is unlocked for programming in Standby mode
2 Allows one write to registers 8'h13, 8'h14, 8'h16 and 8'h2D before WD trigger.

Figure 8-41. Watchdog Configuration Registers Locking and Unlocking Flow Chart

8.3.13.8.2.1.1 Watchdog Configuration in SPI Two-byte Mode

In device versions with REV_ID = 20h, the device inadvertently locks the configuration registers after the first SPI write into registers 13h and 14h when in SPI two-byte mode (BYTE_CNT=1b). Therefore, the device enters Restart mode and sets the LIMP pin active if WD_ERR_CNT_SET=0.

If WD_ERR_CNT_SET=0 and the device is in two-byte mode, the following steps need to be performed in order to avoid entering the Restart mode and setting LIMP pin active:

- Change WD_ERR_CNT_SET at 0x16h to a non-zero value.
  - This creates a lock at 16h
- Modify 13/14h as per the desired configuration needed.
  - These are now locked. Watchdog error interrupt sets.
  - Clear the interrupt. The device does not enter Restart mode because error counter threshold is not reached
- Only if WD_ERR_CNT_SET needs to be set to 0 again:
  - Change mode to Normal and back to Standby mode to unlock the WD configuration lock
  - Write to 16h to set the WD_ERR_CNT_SET to 0

8.3.13.8.3 Watchdog Timing

The TCAN245x-Q1 provides three methods for setting up the watchdog, window, time-out and question and answer. Question and Answer watch dog is covered in Section 8.3.13.8.4. If more frequent, < 64ms, input trigger events are desired, the suggestion is to use the time-out timer as this is an event within the time event and not specific to an open window. Refer to Figure 8-42 for the Timeout watchdog timing diagram. Timeout watchdog has an internal accuracy of ± 15%.

When using the window watchdog, understanding the closed and open window aspects is important. The TCAN245x-Q1 is set up with a 50%/50% open and closed window and is based on an internal oscillator with a ± 10% accuracy range. To determine when to provide the input trigger, this variance needs to be considered. Using the 64ms nominal total window, t_{WINDOW}, provides a closed and open window that are each 32ms. Taking the ±10% internal oscillator into account means t_{WINDOW} can be from 57.6ms to 70.4ms. The closed, t_{CLOSED}, and open window, t_{OPEN}, are from 28.8ms to 35.2ms. Using t_{WINDOW} of 57.6ms and t_{CLOSED} of 35.2ms, the total t_{OPEN} is 22.4ms. The safe trigger area needs to happen at the 46.4ms ± 11.2ms which is half the t_{OPEN} min + t_{CLOSED} max. The same method is used for the other window values. Figure 8-43 provides the above information graphically.

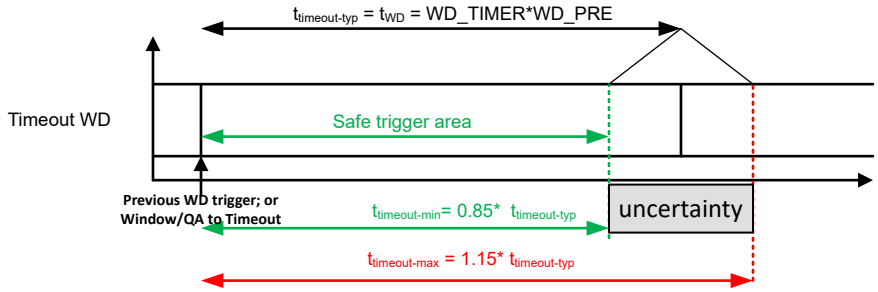


Figure 8-42. Timeout Watchdog Timing Diagram

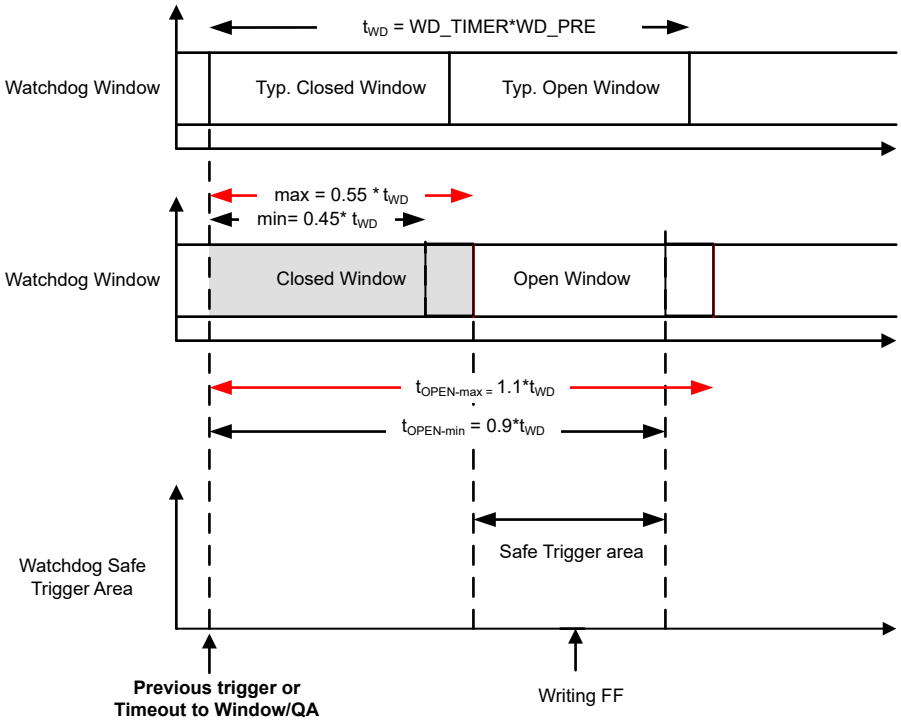


Figure 8-43. Watchdog Timing Diagram

8.3.13.8.4 Question and Answer Watchdog

The TCAN245x-Q1 devices include a question and answer watchdog selectable from SPI. Device defaults to window watchdog.

Question and Answer WD Example explains the WD initialization events.

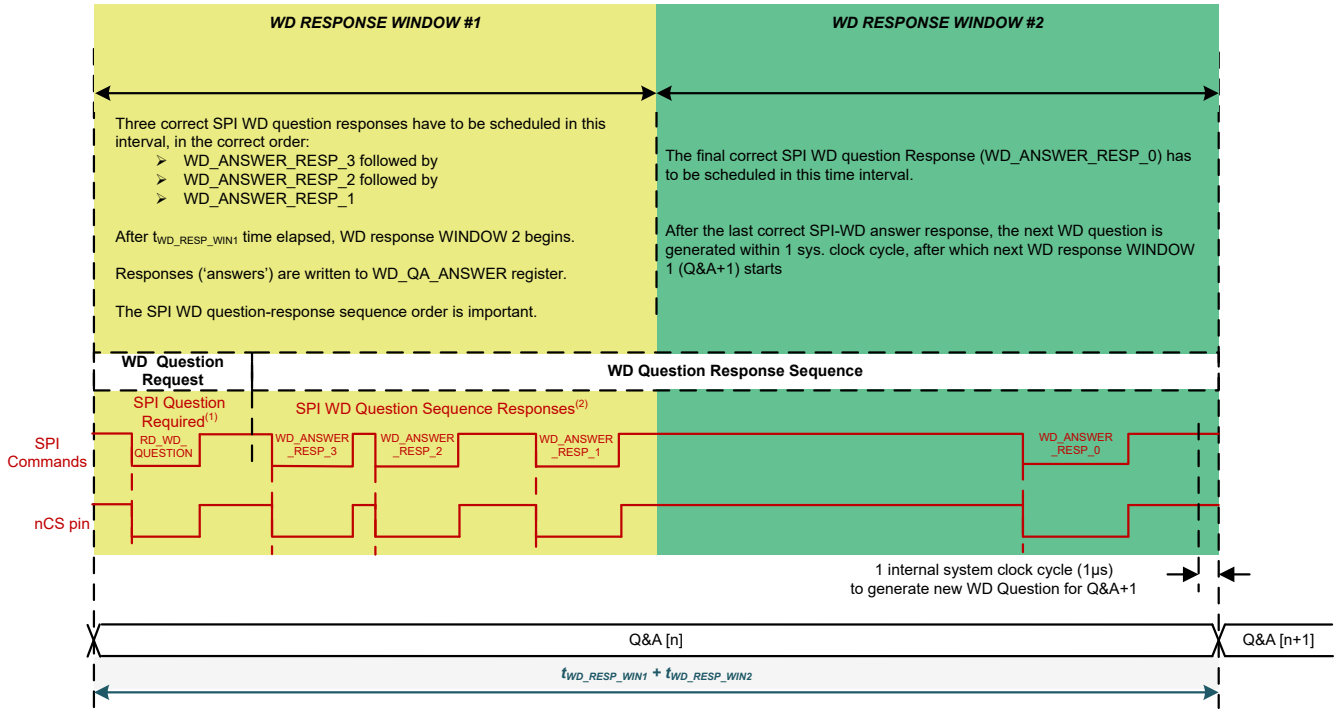
8.3.13.8.4.1 WD Question and Answer Basic Information

A Question and Answer (Q&A) watchdog is a type of watchdog where instead of simply resetting the watchdog via a SPI write, the MCU must read a 'question' from the TCAN245x-Q1, do math based on the question and then write the computed answers back to the TCAN245x-Q1. The correct answer is a 4-byte response. Each byte must be written in order, and with the correct timing to have a correct answer.

There are 2 watchdog windows, referred to as WD Response window #1 and WD Response window #2 (Figure 8-44 WD QA Windows as example). The size of each window is 50% of the total watchdog window time, $t_{WD\_RESP\_WIN1}$ + $t_{WD\_RESP\_WIN2}$, which is selected from the WD_TIMER and WD_PRE register bits.

Each watchdog question and answer is a full watchdog cycle. The general process is that the MCU reads the question during WD Response Window #1. The CPU must perform a mathematical function on the question, resulting in 4 bytes of answers. 3 of the 4 answer bytes must be written to the answer register within the WD Response Window #1, in correct order. The last answer must be written to the answer register after the first response window, inside of WD Response Window #2. If all 4 answer bytes were correct and in the correct order, then the response is considered good, the error counter is decremented and a new question is generated, starting the cycle over again.

If anything is incorrect or missed, the response is considered bad and the watchdog question does NOT change. In addition, an error counter is incremented. Once this error counter exceeds the threshold (defined in the WD_ERR_CNT_SET register field), the watchdog failure action is performed. Examples of actions are an interrupt, or reset toggle, and so on.



A. The MCU is not required to request the WD question. The MCU can start with correct answers, WD_ANSWER_RESP_x bytes anywhere within RESPONSE WINDOW 1. The new WD question is always generated within one system clock cycle after the final WD_ANSWER_RESP_0 answer during the previous WD Q&A sequence run.

B. The MCU can schedule other SPI commands between the WD_ANSWER_RESPx responses (even a command requesting the WD question) without any impact to the WD function as long as the WD_ANSWER_RESP_[3:1] bytes are provided within the RESPONSE WINDOW 1 and WD_ANSWER_RESP_0 is provided within the RESPONSE WINDOW 2.

Figure 8-44. WD Q&A Sequence Run for WD Q&A Multi-Answer Mode

8.3.13.8.4.2 Question and Answer Register and Settings

There are several registers used to configure the watchdog registers, see Table 8-17.

Table 8-17. List of Watchdog Related Registers

Register Address	Register Name	Description
0x16	WD_RST_PULSE	Sets error counter threshold
0x2D	WD_QA_CONFIG	Configuration related to the QA configuration
0x2E	WD_QA_ANSWER	Register for writing the calculated answers
0x2F	WD_QA_QUESTION	Reading the current QA question

The WD_CONFIG_1 and WD_CONFIG_2 registers mainly deal with setting up the watchdog window time length. Refer to Table 8-16 to see the options for window sizes, and the required values for the WD_TIMER values and WD_PRE values. Take note that each of the 2 response windows are half of the selected value. Due to the need for several bytes of SPI to be used for each watchdog QA event, the recommendation is the windows greater than 64ms be used when using the QA watchdog functionality.

There are also different actions that can be performed when the watchdog error counter exceeds the error counter threshold.

8.3.13.8.4.3 WD Question and Answer Value Generation

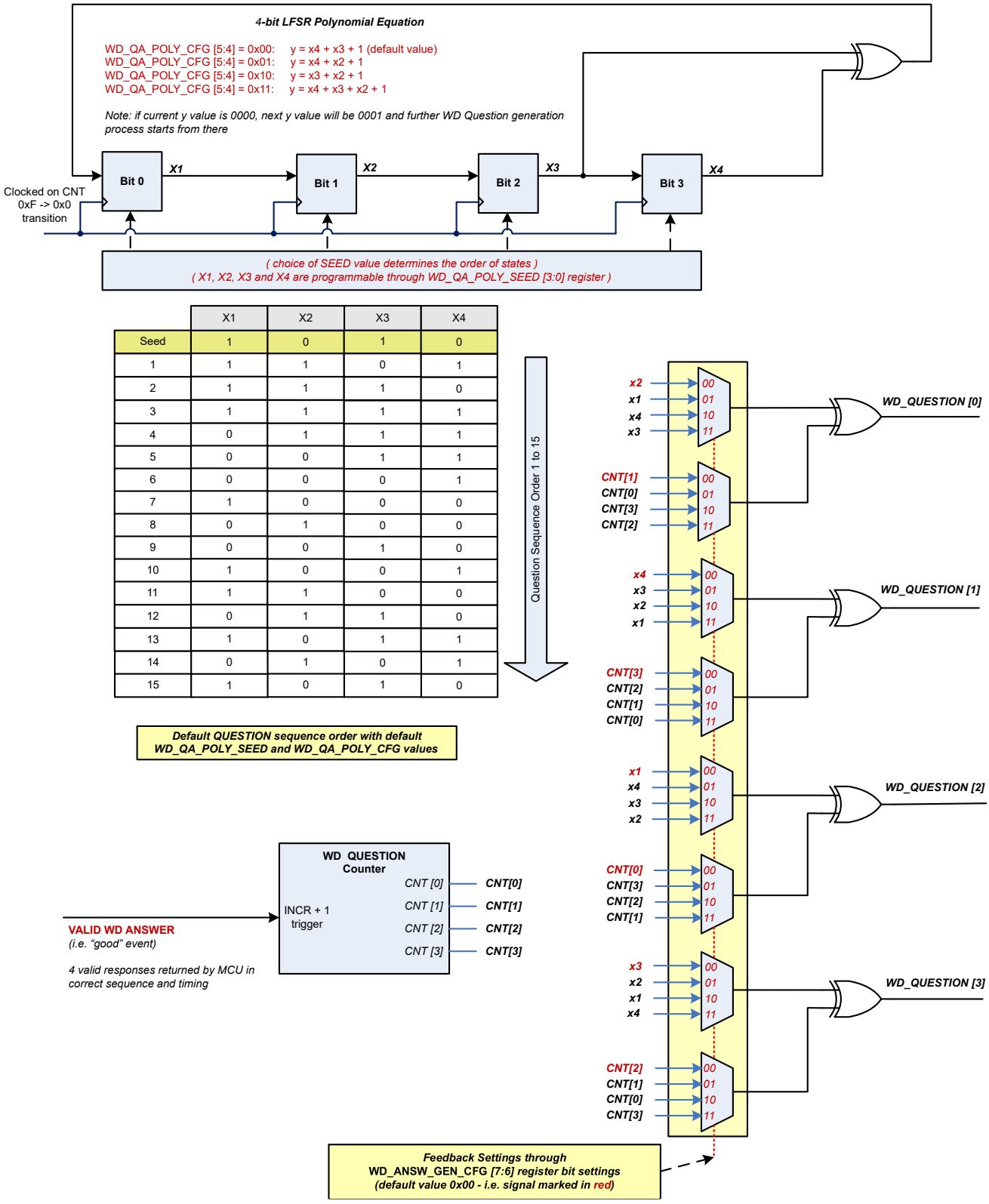
The 4-bit WD question, WD_QA_QUESTION[3:0], is generated by 4-bit Markov chain process. A Markov chain is a stochastic process with Markov property, which means that state changes are probabilistic, and the future

state depends only on the current state. The valid and complete WD answer sequence for each WD Q&A mode is as follows:

- In WD Q&A multi-answer mode:
  1. Three correct SPI WD answers are received during RESPONSE WINDOW 1.
  2. One correct SPI WD answer is received during RESPONSE WINDOW 2.
  3. In addition to the previously listed timing, the sequence of four responses shall be correct.

The WD question value is latched in the WD_QUESTION bits of the WD_QA_QUESTION register and can be read out at any time.

The Markov chain process is clocked by the 4-bit Question counter at the transition from 1111b to 0000b. This includes the condition of a correct answer (correct answer value and correct timing response). The logic combination of the 4-bit questions WD_QA_QUESTION [3:0] generation is given in Figure 8-45. The question counter is reset to default value of 0000b and the Markov chain is re-initialized to programmed register value when a watchdog fail puts the device in restart mode.



	X1	X2	X3	X4
Seed	1	0	1	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1
6	0	0	0	1
7	1	0	0	0
8	0	1	0	0
9	0	0	1	0
10	1	0	0	1
11	1	1	0	0
12	0	1	1	0
13	1	0	1	1
14	0	1	0	1
15	1	0	1	0

A. If the current *y* value is 0000, the next *y* value is 0001. The next watchdog question generation process starts from that value. Any changes to WD_QA_CONFIG register in Standby mode re-initializes the Markov chain to the current register value. The question counter is not affected.

Figure 8-45. Watchdog Question Generation

8.3.13.8.4.3.1 Answer Comparison

The 2-bit, watchdog-answer counter, WD_ANSW_CNT[1:0], counts the number of received answer-bytes and controls the generation of the reference answer-byte as shown in Figure 8-46. At the start of each watchdog sequence, the default value of the WD_ANSW_CNT[1:0] counter is 11b to indicate that the watchdog expects the MCU to write the correct Answer-3 in WD_QA_ANSWER[7:0].

The device sets the WD_QA_ERR status bit as soon as one answer byte is not correct. The device clears this status bit only if the MCU writes a '1' to this bit.

8.3.13.8.4.3.2 Sequence of the 2-bit Watchdog Answer Counter

The sequence of the 2-bit, watchdog answer-counter is as follows for each counter value:

- WD_ANSW_CNT[1:0] = 11b:
  1. The watchdog calculates the reference Answer-3.
  2. A write access occurs. The MCU writes the Answer-3 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-3 with the Answer-3 byte in WD_QA_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 10b and sets the WD_QA_ERR status bit to 1 if the Answer-3 byte is incorrect.
- WD_ANSW_CNT[1:0] = 10b:
  1. The watchdog calculates the reference Answer-2.
  2. A write access occurs. The MCU writes the Answer-2 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-2 with the Answer-2 byte in WD_QA_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 01b and sets the WD_QA_ERR status bit to 1 if the Answer-2 byte is incorrect.
- WD_ANSW_CNT[1:0] = 01b:
  1. The watchdog calculates the reference Answer-1.
  2. A write access occurs. The MCU writes the Answer-1 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-1 with the Answer-1 byte in WD_QA_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 00b and sets the WD_QA_ERR status bit to 1 if the Answer-1 byte is incorrect.
- WD_ANSW_CNT[1:0] = 00b:
  1. The watchdog calculates the reference Answer-0.
  2. A write access occurs. The MCU writes the Answer-0 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-0 with the Answer-0 byte in WD_QA_ANSWER[7:0].
  4. The watchdog sets the WD_QA_ERR status bit to 1 if the Answer-0 byte is incorrect.
  5. The watchdog starts a new watchdog sequence and sets the WD_ANSW_CNT[1:0] to 11b.

The MCU needs to clear the bit by writing a '1' to the WD_QA_ERR bit

Table 8-18. Set of WD Questions and Corresponding WD Answers Using Default Setting

QUESTION IN WD_QA_QUESTION REGISTER	WD ANSWER BYTES (EACH BYTE TO BE WRITTEN INTO WD_QA_ANSWER REGISTER)			
	WD_ANSWER_RESP_3	WD_ANSWER_RESP_2	WD_ANSWER_RESP_1	WD_ANSWER_RESP_0
WD_QUESTION	WD_ANSW_CNT[1:0] 11b	WD_ANSW_CNT[1:0] 10b	WD_ANSW_CNT[1:0] 01b	WD_ANSW_CNT[1:0] 00b
0x0	FF	0F	F0	00
0x1	B0	40	BF	4F
0x2	E9	19	E6	16
0x3	A6	56	A9	59
0x4	75	85	7A	8A
0x5	3A	CA	35	C5
0x6	63	93	6C	9C
0x7	2C	DC	23	D3

Table 8-18. Set of WD Questions and Corresponding WD Answers Using Default Setting (continued)

QUESTION IN WD_QA_QUESTION REGISTER	WD ANSWER BYTES (EACH BYTE TO BE WRITTEN INTO WD_QA_ANSWER REGISTER)			
	WD_ANSWER_RESP_3	WD_ANSWER_RESP_2	WD_ANSWER_RESP_1	WD_ANSWER_RESP_0
WD_QUESTION	WD_ANSW_CNT[1:0] 11b	WD_ANSW_CNT[1:0] 10b	WD_ANSW_CNT[1:0] 01b	WD_ANSW_CNT[1:0] 00b
0x8	D2	22	DD	2D
0x9	9D	6D	92	62
0xA	C4	34	CB	3B
0xB	8B	7B	84	74
0xC	58	A8	57	A7
0xD	17	E7	18	E8
0xE	4E	BE	41	B1
0xF	01	F1	0E	FE

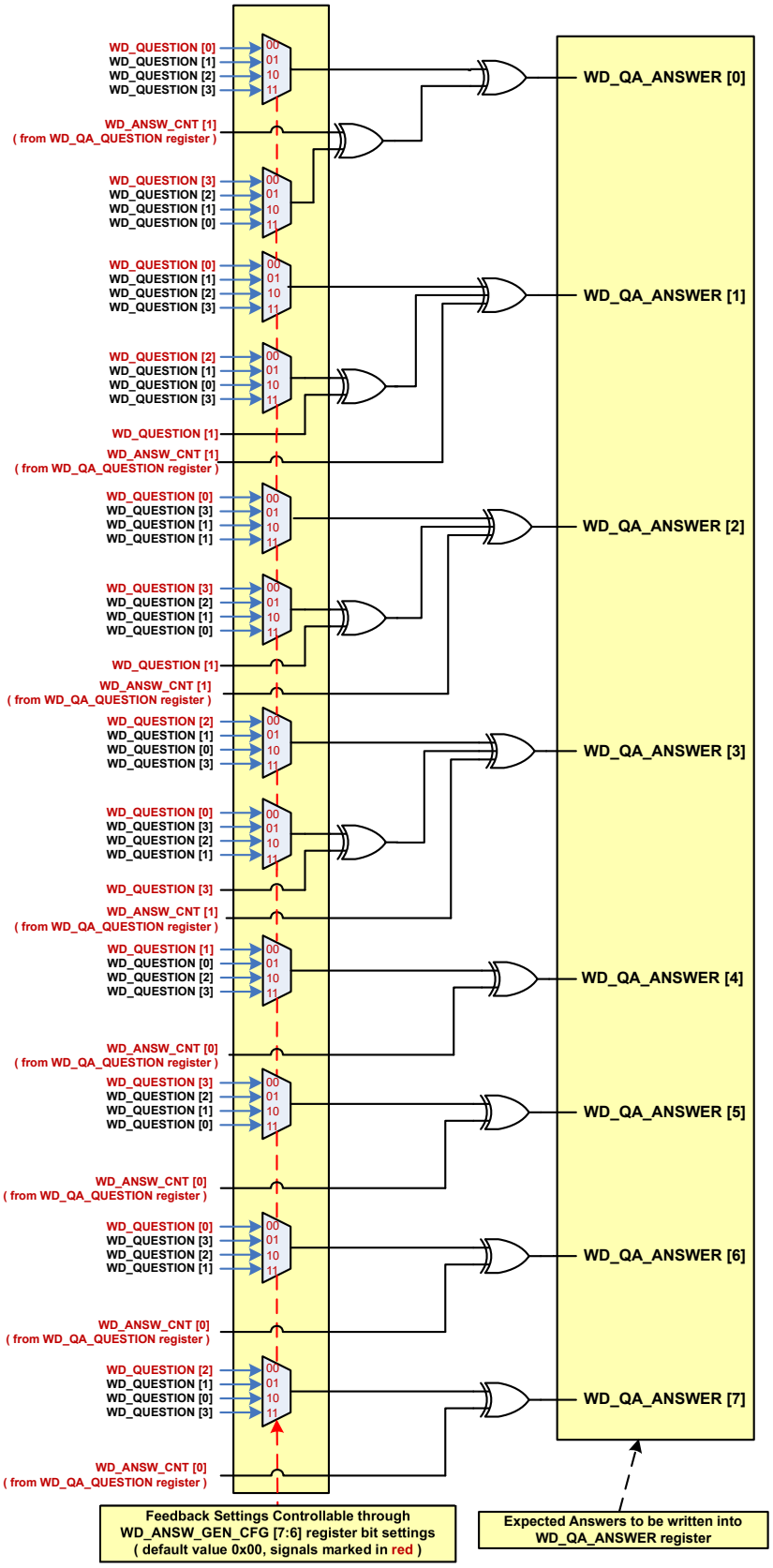


Figure 8-46. WD Expected Answer Generation

Table 8-19. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A Multi-Answer Mode

NUMBER OF WD ANSWERS		ACTION	WD_QA_ERR (in WD_QA_QUESTION Register) (1)	COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2			
0 answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	No answers
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
0 answer	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 CORRECT answer			
2 CORRECT answer	1 CORRECT answer			
0 answer	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 INCORRECT answer			
2 CORRECT answer	1 INCORRECT answer			
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWER in WIN1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 CORRECT answer			
2 CORRECT answer	2 CORRECT answer			
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 INCORRECT answer			
2 CORRECT answer	2 INCORRECT answer			
0 answer	3 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	
2 INCORRECT answer	1 CORRECT answer			
0 answer	3 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 INCORRECT answer			
2 INCORRECT answer	1 INCORRECT answer			

Table 8-19. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A Multi-Answer Mode (continued)

NUMBER OF WD ANSWERS		ACTION	WD_QA_ERR (in WD_QA_QUESTION Register) (1)	COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2			
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 CORRECT answer			
2 INCORRECT answer	2 CORRECT answer		1b	
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 INCORRECT answer			
2 INCORRECT answer	2 INCORRECT answer			
3 CORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD Question	1b	Less than 4 CORRECT ANSW in RESPONSE WINDOW 1 and more than 0 ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
2 CORRECT answer	0 answer			
1 CORRECT answer	0 answer		1b	
3 CORRECT answer	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Decrement WD failure counter -New WD cycle starts with a new WD question	0b	CORRECT SEQUENCE
3 CORRECT answer	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
3 INCORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received < 4
3 INCORRECT answer	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
3 INCORRECT answer	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
4 CORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	
3 CORRECT answer + 1 INCORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	4 CORRECT or INCORRECT ANSWER in RESPONSE WINDOW 1
2 CORRECT answer + 2 INCORRECT answer	Not applicable			
1 CORRECT answer + 3 INCORRECT answer	Not applicable			

(1) WD_QA_ERR is the logical OR of all QA watchdog errors

8.3.13.8.4.3.3 Question and Answer WD Example

For this example, we'll walk through a single sequence with the following configuration settings, Table 8-20.

Table 8-20. WD Function Initialization

Item	Value	Description
Watchdog window size	1024ms	Window size of 1024ms
Answer Generation Option	0 (default)	Answer generation configuration
Question Polynomial	0 (default)	Polynomial used to generate the question
Question polynomial seed	A (default)	Polynomial seed used to generate questions
WD Error Counter Limit	15	On the 15th fail event, do the watchdog action

8.3.13.8.4.3.3.1 Example Configuration for Desired Behavior

Table 8-21 register writes configures the part for the example behavior specified above. Most of the settings are power on defaults.

Table 8-21. Example Register Configuration Writes

Step	Register	Data
1	WD_CONFIG_1 (0x13)	[W] 0b11010000 / 0xD0
2	WD_CONFIG_2 (0x14)	[W] 0b10000000 / 0x80
3	WD_RST_PULSE (0x16)	[W] 0b11110000 / 0xF0
4	WDT_QA_CONFIG (0x2D)	[W] 0b00001010 / 0x0A

8.3.13.8.4.3.3.2 Example of performing a question and answer sequence

The normal sequence summary is as follows:

1. Read the question
2. Calculate the 4 answer bytes
3. Send 3 of them within the first response window
4. Wait and send the last byte in the second response window

See Table 8-22 for an example of the first loop sequence.

Table 8-22. Example First Loop

Step	Register	Data	Description
1	WD_QA_QUESTION (0x2F)	[R] 0x0C	Read the question. Question is 0x0C
2	WD_QA_ANSWER (0x2E)	[W] 0x58	Write answer 3 (See Table 8-18 Example answers to questions with default settings to see answers)
3	WD_QA_ANSWER (0x2E)	[W] 0xA8	Write answer 2
4	WD_QA_ANSWER (0x2E)	[W] 0x57	Write answer 1
5	WD_QA_ANSWER (0x2E)	[W] 0xA7	Write answer 0 once window 2 has started

At this point, the user can read the WD_QA_QUESTION[6] (0x2F) register to determine if WD_QA_ERR is set.

8.3.13.9 Bus Fault Detection and Communication

The TCAN245x-Q1 provides advanced bus fault detection. The device can determine certain fault conditions and set a status/interrupt flag so that the MCU can understand what the fault is. As with any bus architecture where termination resistors are at each end not every fault can be specified to the lowest level, meaning exact location.

The fault detection circuitry is monitoring the CANH and CANL pins (currents) to determine if there is a short to battery, short to ground, short to each other or opens. From a system perspective, the location of the device also determines what can be detected. See Figure 8-47 as an example of node locations and how the ability to determine the actual fault location is impacted. Figure 8-48 through Figure 8-52 show the various bus faults based upon the three-node configuration. Table 8-23 shows what can be detected and by which device. Fault 2 is detected as no termination.

Bus fault detection is a system level situation. If the fault is occurring at the ECU, then the general communication of the bus is compromised. For complete coverage of a node, a system level diagnostic step is needed for each node and the ability to communicate this back to a central point.

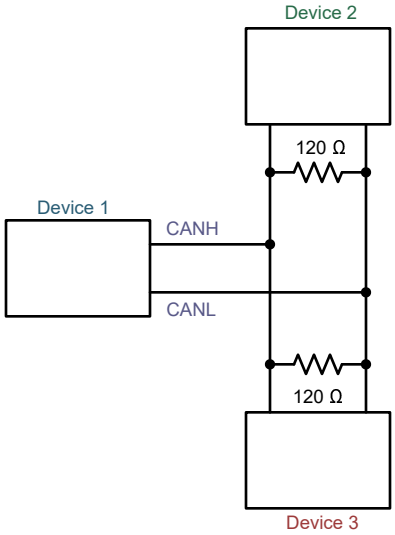


Figure 8-47. Three Node Example

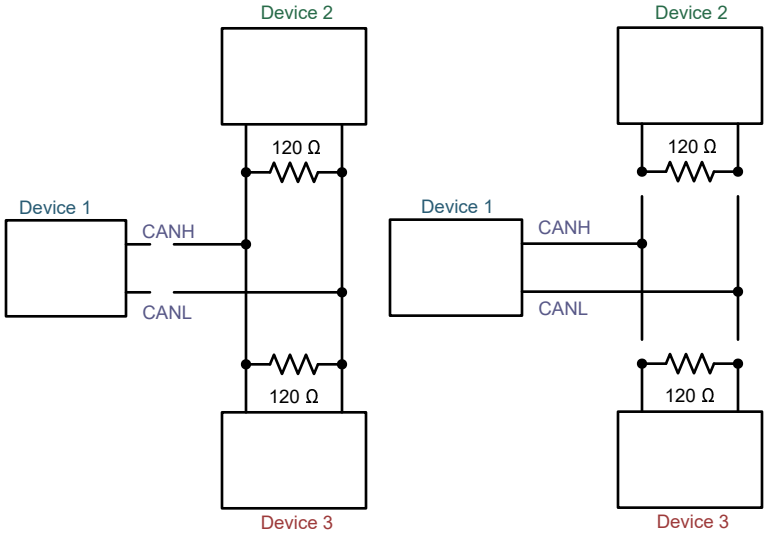


Figure 8-48. Open Fault 2 Examples

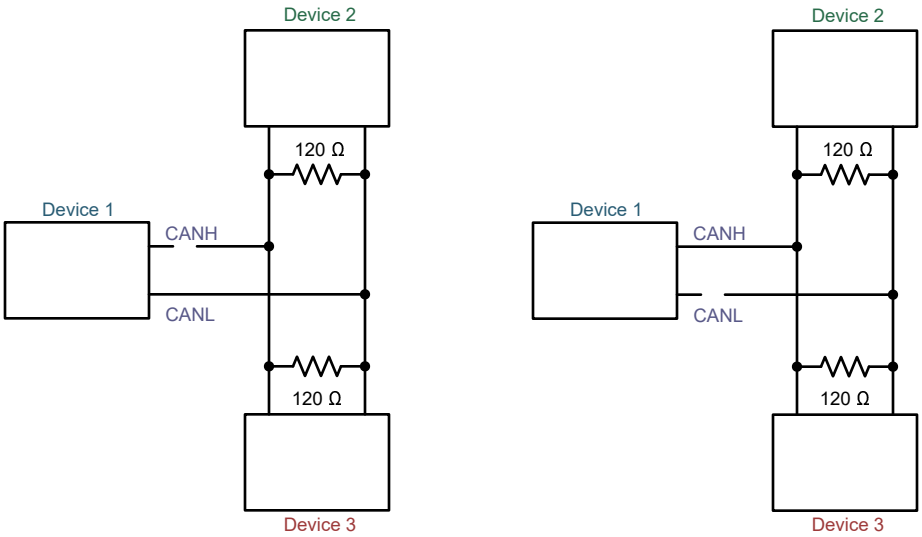


Figure 8-49. Open Faults 3 and 4 Examples

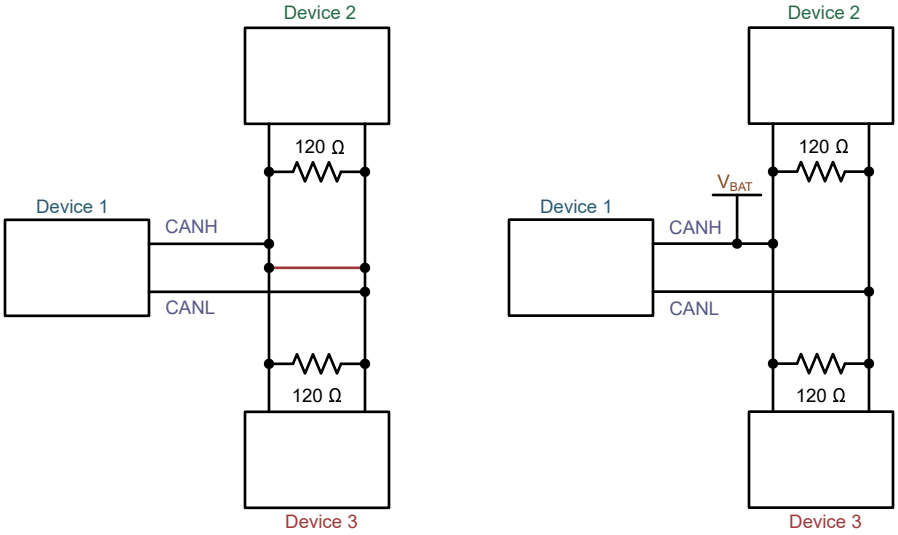


Figure 8-50. Short Faults 5 and 6 Examples

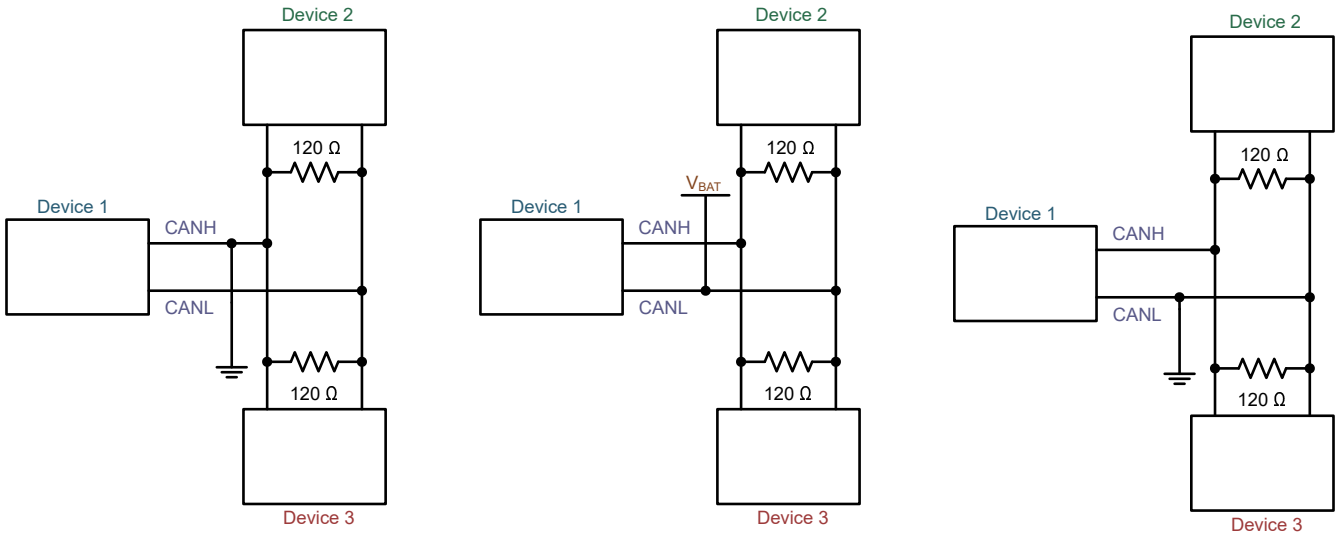


Figure 8-51. Short Faults 7, 8 and 9 Examples

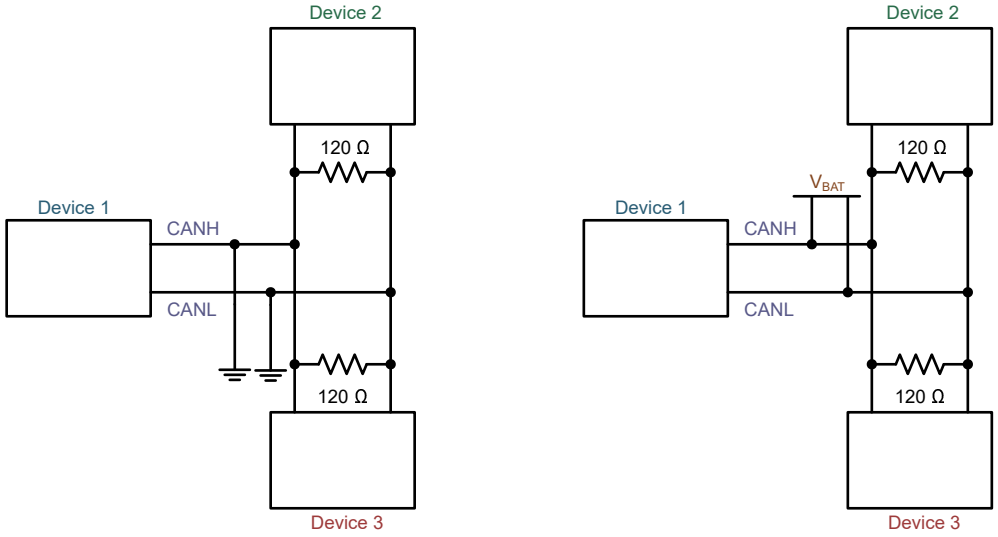


Figure 8-52. Short Faults 10 and 11 Examples

Table 8-23. Bus Fault Pin State and Detection Table

Fault #	CANH	CANL	Fault Detected
2	Open	Open	Depending upon open location the device detects this as no termination.
3	Open	Normal	Device 1 detects this fault, but cannot tell the difference between it and Fault 2 and 4; Device 2 and Device 3 do not see this fault
4	Normal	Open	Device 1 detects this fault but cannot tell the difference between it and Fault 2 and 3; Device 2 and Device 3 do not see this fault
5	Shorted to CANL	Shorted to CANH	Yes, but not location
6	Shorted to V_{bat}	Normal	Yes, but not location
7	Shorted to GND	Normal	Yes, but cannot tell the difference between this and Fault 10
8	Normal	Shorted to V_{bat}	Yes, but cannot tell the difference between this and Fault 11
9	Normal	Shorted to GND	Yes, but not location
10	Shorted to GND	Shorted to GND	Yes, but cannot tell the difference between this and Fault 7
11	Shorted to V_{bat}	Shorted to V_{bat}	Yes, but cannot tell the difference between this and Fault 8

Table 8-24. Bus Fault Interrupt Flags Mapping to Fault Detection Number

Address	BIT(S)	DEFAULT	FLAG	DESCRIPTION	FAULT DETECTED	ACCESS
8'h54	7	1'b0	UVCAN	VCAN undervoltage interrupt	VCAN undervoltage	R/W1C
	6	1'b0	RSVD	Reserved	N/A	R
	5	1'b0	CANHCANL	CANH and CANL Shorted Together	Fault 3	R/W1C
	4	1'b0	CANHBAT	CANH Shorted to V_{bat}	Fault 6	R/W1C
	3	1'b0	CANLGND	CANL Shorted to GND	Fault 9	R/W1C
	2	1'b0	CANBUSOPEN	CAN Bus Open (One of three possible places)	Faults 2, 4 and 5	R/W1C
	1	1'b0	CANBUSGND	CANH Shorted to GND or Both CANH & CANL Shorted to GND	Faults 7 and 10	R/W1C
	0	1'b0	CANBUSBAT	CANL Shorted to Vbat or Both CANH & CANL Shorted to Vbat	Faults 8 and 11	R/W1C

8.3.14 Customer EEPROM Programming

The TCAN245x-Q1 family uses EEPROM for two purposes. The first is for device trimming and is not accessible. This portion of EEPROM is monitored and loaded upon power and when exiting sleep mode, checking for a valid CRC. If the CRC is not valid, this process is performed a total of eight time. If still not valid, the INT_3 register 8'h53[0] is set to 1b. Meaning the device has an issue that may impact performance and functionality.

The second use of the EEPROM is to allow the user to store the device configuration. The configuration bits saved are provided in each register. To save the configuration to EEPROM, CRC must be enabled for the save function at a minimum. Saving the configuration to EEPROM is accomplished by writing a 1b to register 8'h4E[7], and default code Ah to 8'h4E[3:0] followed by the CRC byte. See Table 8-25 for procedure if the processor does not support CRC. Register 8'h4E[3:0] reads back 0h. Once the configuration bits have been stored to EEPROM, a 0b is read back from 8'h4E[7]. If a power on reset takes place, the configuration of the device is reloaded from EEPROM. Table 8-26 provides the list of registers and the bits saved to EEPROM if used.

Note

- The EEPROM is reprogrammable a maximum of 500 times.
- REV_ID = 20h: Customer EEPROM Programing is not available in SPI two-byte mode. Contact factory for programing two-byte mode as the default option.

Table 8-25. Process for Non-CRC-Capable Processors

Step	Description	Register	Data	Second Data Byte (CRC POLY_8_SET = 0b)	Second Data Byte (CRC POLY_8_SET = 1b)
1	Configure device	See Table 8-26	N/A	N/A	N/A
2	Set CRC Polynomial • 0x2F AutoSar • 0X1D SAE J11850	8'h0B[0]	• 00h • 01h	• Selected • N/A	• N/A • Selected
3	Enable SPI CRC if not enable	8'h0A[0]	01h	N/A	N/A
4	Save to EERPOM	8'h4E[7:0]	8Ah	36h	0Ch
5	Disable SPI CRC if not supported	8'h0A[0]	00h	5Eh	6Bh

The saved configuration can be forced to check if the saved configuration CRC is valid but using register 8'h4E[6], EEPROM_CRC_CHK, = 1b. This takes approximately 200 µs to complete. If CRC is valid, then no action is taken, If CRC is not valid, the device attempts this action eight times. If still not valid, the device sets an interrupt indicating there is an issue are INT_4 register 8'h5A[1], EEPROM_CRC_INT.

The following are power and reset scenarios and how the EEPROM is used.

- UVSUP event; no action as registers are not lost
- Power on reset event; EEPROM is read and registers restored in Init mode
- Soft reset; EEPROM is read and registers restored and device transitions to standby mode
- Hard reset; EERPOM is read and registers restored and device transitions to Init mode
- nRST input; EEPROM is read and register restored and device transitions to restart mode

Table 8-26. EEPROM Saved Registers and Bits

Register	Bits Saved
SPI_CONFIG (Address = 09h)	0-3
SBC_CONFIG (Address = Ch)	0-1, 4, 7
VREG_CONFIG1 (Address = Dh)	3, 5, 6-7
SBC_CONFIG1 Register (Address = Eh)	0, 3-5,
WAKE_PIN_CONFIG1 Register (Address = 11h)	0-3
WAKE_PIN_CONFIG2 Register (Address = 12h	0-1, 5-7
WD_CONFIG_1 Register (Address = 13h)	0-7
WD_CONFIG_2 Register (Address = 14h)	0, 5-7
WD_RST_PULSE Register (Address = 16h)	4-7
DEVICE_CONFIG2 (Address = 1Bh)	2
SWE_TIMER (Address = 1Ch)	3-6, 7
nRST_CNTL (Address = 29h)	4, 5
WAKE_PIN_CONFIG3 Register (Address = 2Ah)	4-7
WAKE_PIN_CONFIG4 Register (Address = 2Bh)	0-1, 3-5, 7
HSS_CNTL3 Register (Address = 4Fh)	0
BUCK_CONFIG1 Register (Address = 65h)	0-7
WAKE_ID_PIN_CONFIG1 Register (Address = 79h)	1-3, 5-7
WAKE_ID_PIN_CONFIG2 Register (Address = 7Ah)	1-3, 5-7
WAKE_PIN_CONFIG5 Register (Address = 7Bh)	4-5, 7

8.4 Device Functional Modes

The TCAN245x-Q1has several SBC operating modes: normal, standby, sleep, restart and fail-safe. The first three mode selections are made by the SPI register, 8'h10[2:0]. Fail-safe mode if enabled is entered due to various fault conditions. TheTCAN245x-Q1 automatically goes from sleep to restart and then to standby mode when receiving a WUP or LUP event. When selective wake is enabled, the device looks for a WUF and if not received the TCAN2451-Q1remains in sleep mode. See Table 8-27 for the various modes and what parts of the device are active during each mode.

Table 8-27. Mode Overview

Block	Restart	Sleep	Standby	Normal	Fail-safe
nINT	High (VCC1 present) off others	High (VCC1 present) High-Z others	Active	Active	High-Z
GFO	High (VCC1 present) off others	High-Z	Active	Active	High-Z
SW	Off	Wake capable/Off	Active	Active	Wake capable/Off
HSSx	Off	Off - HSS4 can be on if WAKE pins setup for cyclic sensing	As Programmed	As Programmed	Off - HSS4 can be on if WAKE pins setup for cyclic sensing
LIMP (Open-drain active low)	Same as previous state unless from fail-safe mode. Off (high from external pull-up) from fail-safe mode unless WD error and then Low	High (LIMP_SLP_FLT_EN =0b);Enabled (LIMP_SLP_FLT_EN =1b)	Previous state prior to entering STBY	Previous state prior to entering normal mode	Low

Table 8-27. Mode Overview (continued)

Block	Restart	Sleep	Standby	Normal	Fail-safe
WAKEx	Off	On (default); programmable off	On (default); programmable off	On (default); programmable off	On (default); programmable off
CRXD	High (VCC1 present)	High (VCC1 present) High-Z others	Transceiver configuration dependent	Transceiver configuration dependent	High-Z
nRST	Low	Low unless VCC1 programmed to be on in sleep mode, then high.	High	High	Off
SPI	Off	Active if VCC1 present	Active	Active	Off
Watchdog	Off	Off (default); programmable on when VCC1 is on	Default on with long first pulse but programmable off - Timeout only	Active	Off
Low Power CAN RX	Default on for Wake capable	Default on for Wake capable	On if Wake capable	On if Wake capable	Default on for Wake capable
CAN Transceiver	Off	Off	Programmable - Receiver only	Programmable	Off
VCC1	Ramping	Off (default); programmable on	On (default); programmable off	On	Off
VCC2	Ramping	Off (default); programmable on	On (default); programmable off	On (default); programmable off	Off

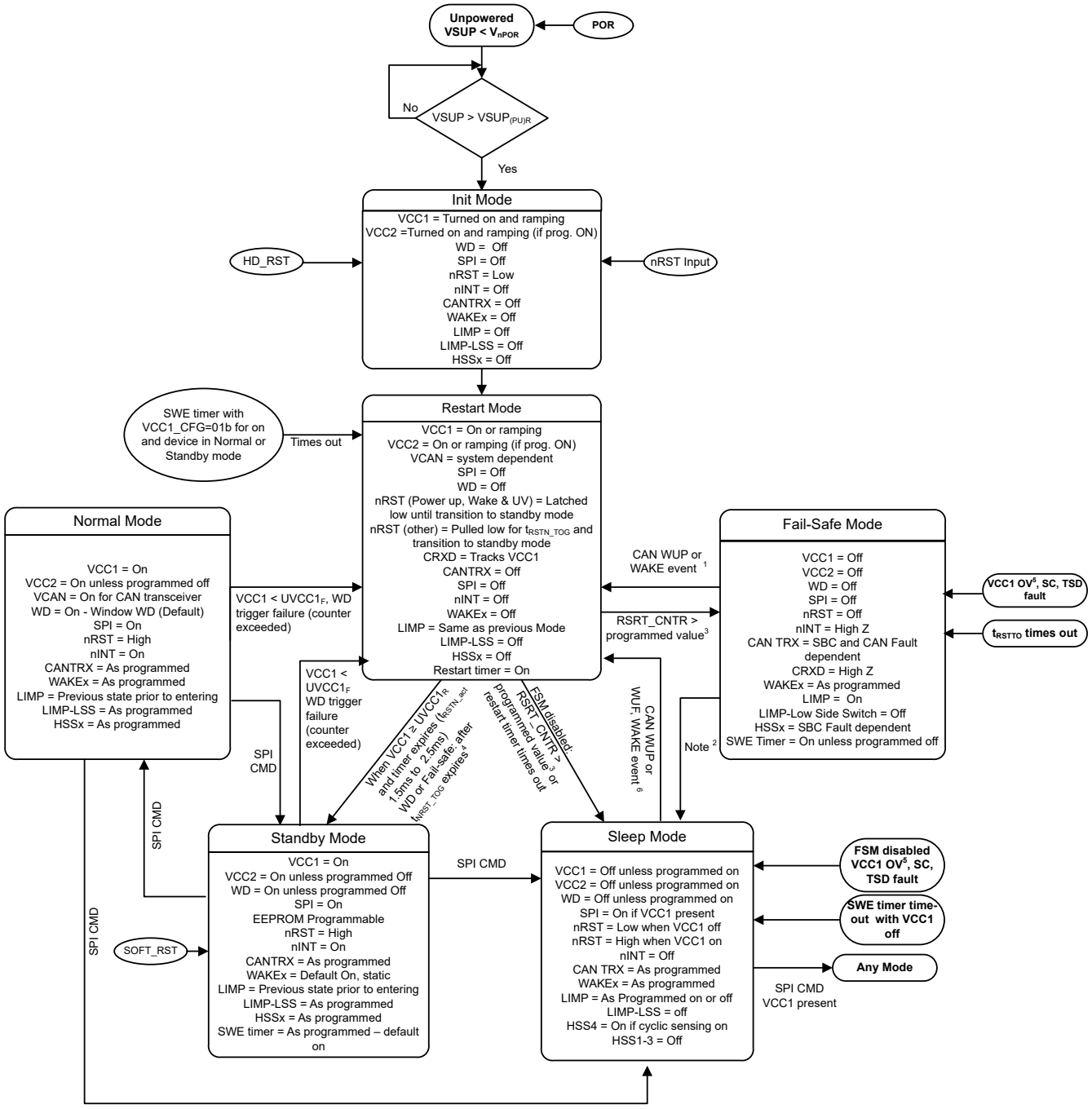


Figure 8-53. Device State Diagram

Note

1. Fail-safe mode is exited after t_{REGOFF} expires and a wake event has taken place if the fault has cleared. Wake event is not needed to exit fail-safe mode if VCC1_CFG = 01b (VCC1 is always ON). If the fail-safe mode is entered due to a TSD event, the device exits the fail-safe mode 1s after temperature falls below TSDF threshold without needing a wake event. If cyclic wake is turned ON in fail-safe mode, device automatically wakes up according to the selected timer intervals to check if the fault is cleared.
2. SWE timer starts upon entering fail-safe mode and if timer times out the device transitions to sleep mode regardless of VCC1 configuration.
3. Restart counter increments when entered from Normal or Standby modes
4. Transition from Restart mode to Standby mode can take place if:
   - VCC1 > $UVCC1_R$ and
   - t_{NRST_TOG} expires (in case of WD failure or entering from fail-safe mode) OR t_{RSTN_act} expires (entering from sleep mode or power-up)
5. If OVCC1_ACTION (8'h0C[6]) is set to 1b and there is an OVCC1 event, the device only sets the OVCC1 interrupt and stays in the current SBC mode.
6. If VCC1 is ON in Sleep mode, the transition from Sleep mode to Restart mode due to wake event is enabled only when VCC1_SLP_ACT =1b. If instead VCC1_SLP_ACT = 0b (default), the device only sets a wake interrupt and indicates the wake-up via CRXD pin.

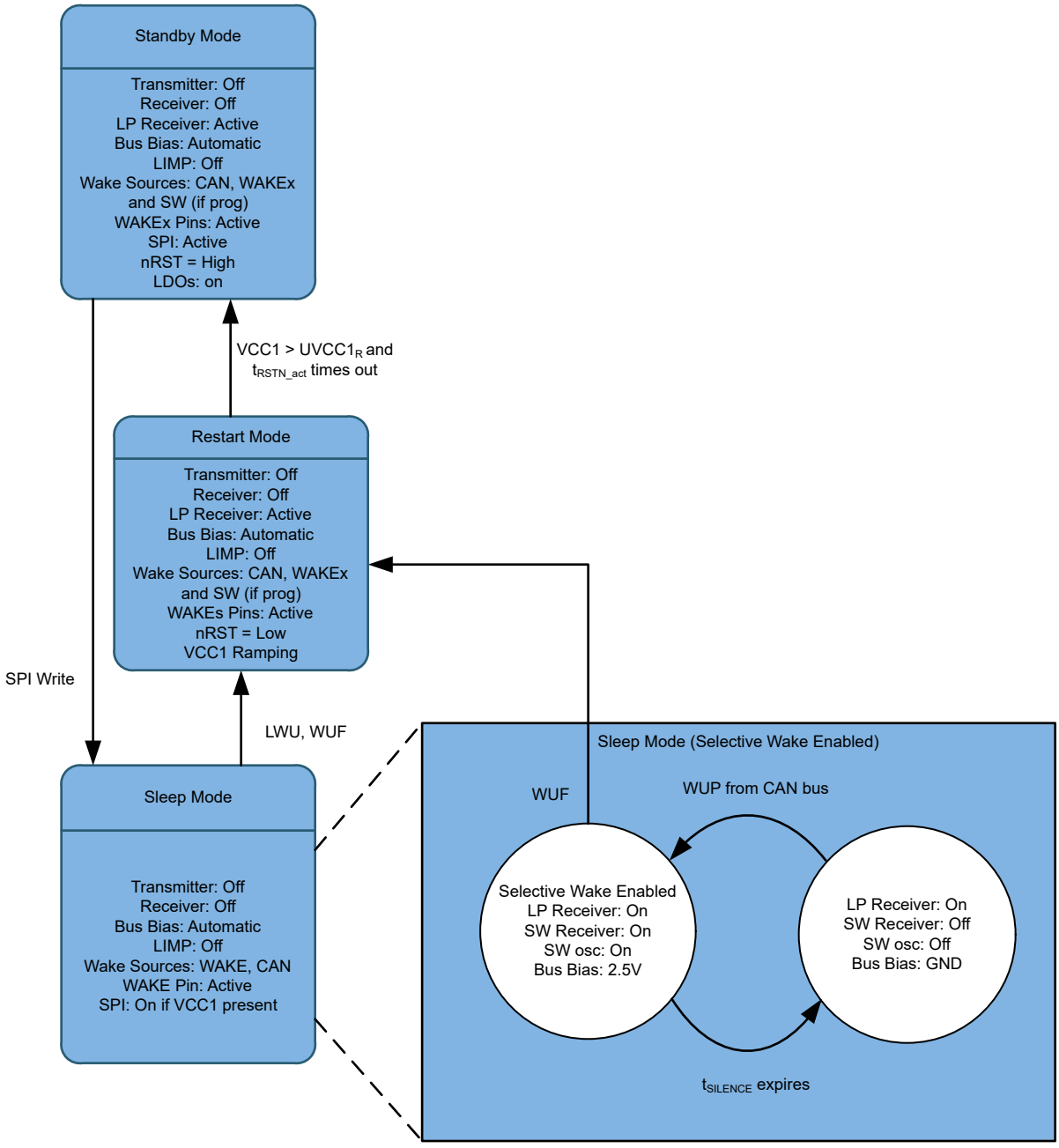


Figure 8-54. Selective Wake Enabled Sleep Mode

Note

For the state diagrams, by default SPI is off in sleep mode. SPI can be configured to work in sleep mode which includes selective wake sub state as shown in Figure 8-54.

8.4.1 Init Mode

This is the initial mode of operation upon powering up. This is a transitional mode that is entered once VSUP is above $VSUP_{(PU)R}$ threshold. The device transitions to restart mode once the device defaults are set.

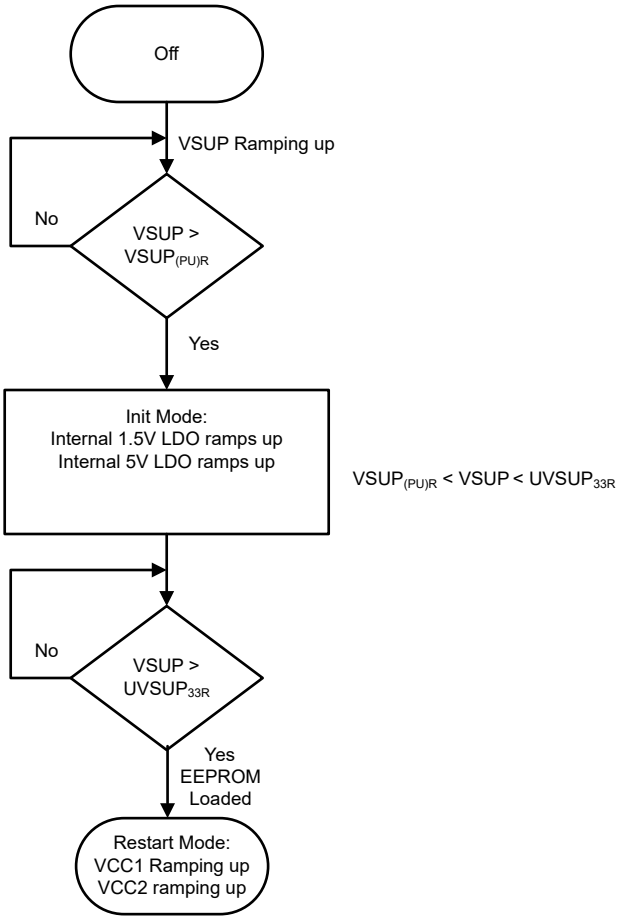


Figure 8-55. Init Mode

8.4.2 Normal Mode

In normal mode, the CAN FD transceiver can be configured as on, listen, wake capable or off. The transmitter translates the digital inputs from the CAN controller connected to the CTXD pin to the CAN signals on CAN bus (CANH and CANL pins). The receiver translates the signals from the CAN bus to a digital output on the CRXD pin connected to the CAN controller. Normal mode is entered by a SPI command and does not change the programmed configuration of the CAN transceiver.

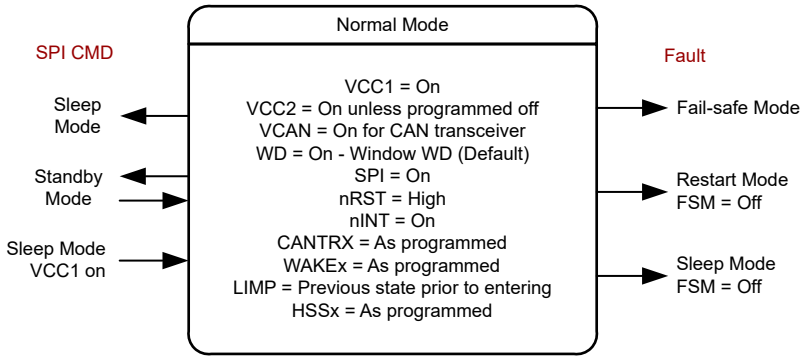


Figure 8-56. Normal Mode

8.4.3 Standby Mode

The device automatically enters standby mode from restart mode. Upon initial power up, this transition happens when VCC1 > UVCC1 and t_{RSTN_act} time has expired. VCC2 is turned on at power up but is not required to

by greater than UVCC2 to transition to standby mode. The TCAN245x-Q1 can enter standby mode by writing a 00b to register 8'h0B[7:6] from normal mode. The watchdog function is default on in standby mode. Standby mode only supports timeout watchdog and automatically changes to this when entered. When WD_STBY_DIS, register 8'h14[0] = 0b (default value) entrance to standby mode has a long timeout window, t_{INITWD}, that a WD trigger event must take place when entered from restart mode. The watchdog can be disabled for standby mode by setting 8'h14[0] = 1b. In this mode, the transceiver can be programmed to meet the applications requirements. There are several blocks that are active in this mode. In standby mode, the CAN FD transceiver can be configured as listen, wake capable or off. If programmed as wake capable, the low power CAN receiver is actively monitoring the bus for the wake up pattern (WUP). The WAKEx pins monitor is active. The SPI interface is active so that the microprocessor can read and write registers in the memory for status and configuration. The device goes from sleep mode to restart mode to standby mode automatically upon a bus WUP event, WUF (TCAN2451-Q1) or a local wake up from the WAKEx pins and when VCC1 > $UVCC1_R$. If VCC1 is disabled, the device enters standby mode after t_{RSTN_act} timer times out.

Upon entering standby mode, the SWE timer, $t_{INACTIVE}$, starts and any SPI commend from the processor clears the SWE timer. This feature makes sure the node is in the lowest power mode if the processor does not come up properly. This automatic mode change also takes place when the device has been put into sleep mode and receives a wake event, WUP, WUF or LWU. To disable this feature for sleep events, register 8'h10[3] (SWE_DIS) must be set to one. This does not disable the feature when powering up or when a power on reset takes place.

The following provides the description on how selective wake interacts between sleep and standby modes for the TCAN2451-Q1.

- At power up, the device is in standby. Clear all Wake flags (PWRON, WUP/LWU), configured the Selective Wake registers, and then set selective wake config (SWCFG = 1) and selective wake enable (SW_EN = 1).
- When SWCFG = 1 and the device is placed into sleep mode the low power WUP receiver is active and waiting for a WUP.
- Once a WUP is received the WUF receiver is active.
- The device receives the wake-up frame and determine if the node requested to wake up.
  - If the WUF address is correct, the device wakes up the node entering standby mode.
  - If the WUF is not address is incorrect, the device stays in sleep mode.
- A wake interrupt occurs from any type, WUF (CANINT), FRAME_OVF or LWU (if enabled), the device enters standby mode.

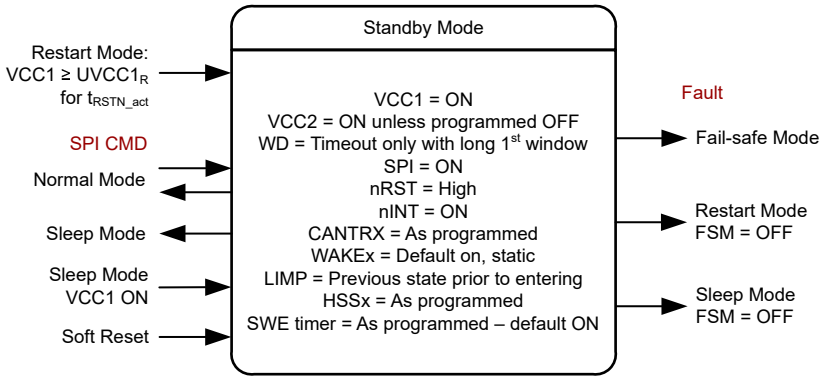


Figure 8-57. Standby Mode

8.4.4 Restart Mode

Restart mode is a transitional mode. Enter this mode from any of the other modes depending upon whether fail-safe mode is disabled. In this mode the enabled LDOs are ramping or are on. At initial power up, once VCC1 ≥ $UVCC1_R$ for t_{RSTN_act} (approximately 2ms) the device transitions to standby mode. While in restart mode, nRST is latched low. When restart mode is entered, at restart timer is started. Select this timer between t_{RSTTO} and $t_{INACTIVE}$ (SWE) timer by programming register 8'h4F[0], RSTRT_TMR_SEL. The default is t_{RSTTO}. If the device has not exited restart mode prior to the timer timing out, the device transitions to fail-safe mode

if enabled or sleep mode if fail-safe mode is disabled. Each time restart mode is entered from normal or standby modes, the restart mode counter, RSRT_CNTR, is incremented. The exception to this is if exceeding the restart counter caused the device to enter fail-safe or sleep mode. When re-entering restart mode due to this event, the counter is ignored and device enters standby mode. Once in standby mode, the counter clears. This counter is programmable from register 8'h28[7:4], which sets the number of times restart can be entered before transitioning to sleep or fail-safe mode, up to 15 times. The default value is 4. Register 8'h28[3:0] is RSRT_CNTR. The counter can be disabled by programming the counter to 0000b. To prevent the transition to sleep or fail-safe mode, the counter periodically clears.

The nRST output pin behavior depends upon the reason the device entered restart mode. When entered due a watchdog failure, from fail-safe mode or an external nRST toggle, the nRST pin is pulled low for t_{NRST_TOG} which defaults to 20ms. This pulse width can be configured to 2ms by changing register 8'h29[5] = 0. After this time the device transitions to standby mode and release nRST pin to high. See Figure 8-59.

When restart mode is entered from sleep mode or due to an under-voltage event, the device latches nRST low until VCC1 > $UVCC1_R$ for t_{RSTN_act}, and then transitions to standby mode and release nRST high. When entering restart mode, the t_{RSTTO} timer starts and if times out transitions the device to sleep mode. See Figure 8-58 on how restart mode is entered and exited.

The nRST pin is the TCAN245x-Q1 reset input which transitions the device into restart mode when the pin is pulled low for t_{nRSTIN}, see Figure 8-59

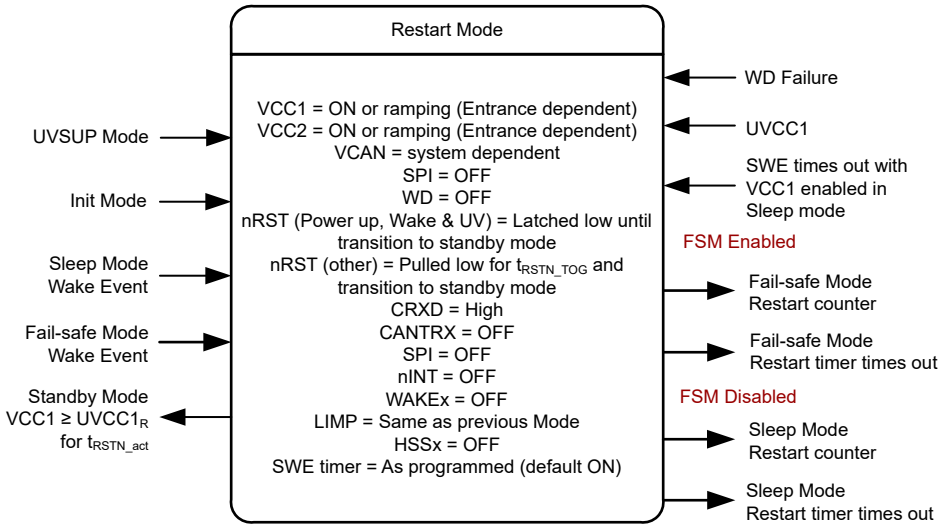


Figure 8-58. Restart Mode

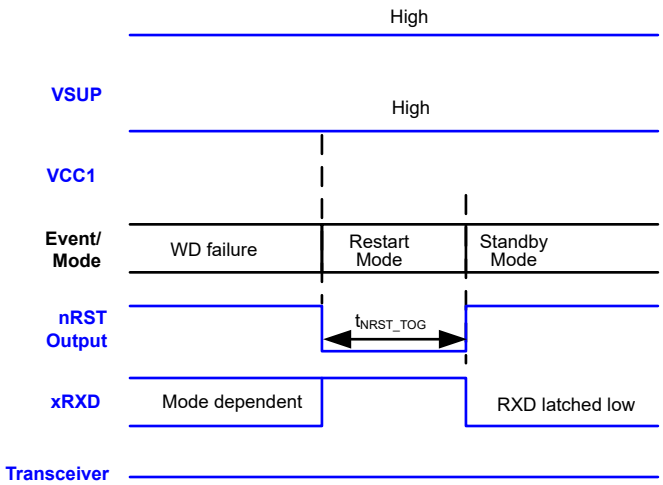


Figure 8-59. Event to Restart Timing Diagram

8.4.5 Fail-safe Mode

The TCAN245x-Q1 has a fail-safe mode, default on, which is entered when certain fault events take place. When fail-safe mode is entered, LIMP is turned ON (if enabled), a global interrupt is issued and the sleep wake error (SWE) timer, $t_{INACTIVE}$, if enabled starts and VCC1 and VCC2 are turned off. The reason for entering fail-safe mode is provided by register 8'h17[3:1], and expanded further with other interrupt flags. This mode can be disabled by using register 8'h17[0], but the recommendation is to keep enabled as fault monitoring is active in fail-safe mode and not sleep mode. This mode brings other functions into lower power mode states. When entering fail-safe mode, the regulators are kept off for at least t_{REGOFF}, approximately 300ms. During this time wake events are monitored and preserved. After t_{REGOFF} times out wake events causes the device to transition to restart mode. If the SWE timer times out prior to faults being cleared and a wake event taking place, the device transitions to sleep mode. Figure 8-60 shows the various fault conditions that causes the device to enter fail-safe mode. If the fault conditions are cleared and a wake event takes place, the device transitions to restart mode. Figure 8-61 provides a high level flow chart for fail-safe mode.

A fail-safe mode counter is available allowing a set number of fail-safe events in a row which then causes the device to perform the programmed action which can include going to sleep where a WUP, WUF or LWU event does not wake the device. A power on reset is required. The counter is default disabled and can be enabled at 8'h17[7:4] ≠ 0000b. The counter expiration action is at 8'h17[7:4]. The number of events before action is programmed is set at 8'h18[7:4] with a value up to 16 events. 8'h18[3:0] is the running up/down fail-safe event counter that can be read and cleared.

There are multiple ways to exit fail-safe mode depending upon the fault and programmed configuration.

- A wake event and cleared fault sends the device into restart mode.
- SWE timer, if enabled, causes the device to transition to sleep mode after the timer expires
- If FSM_CYC_WK_EN, 8'h0E[6] = 1b, the device wakes up during the on time of the selected timer and check to see if the fault has cleared. If so, it transitions to restart mode.

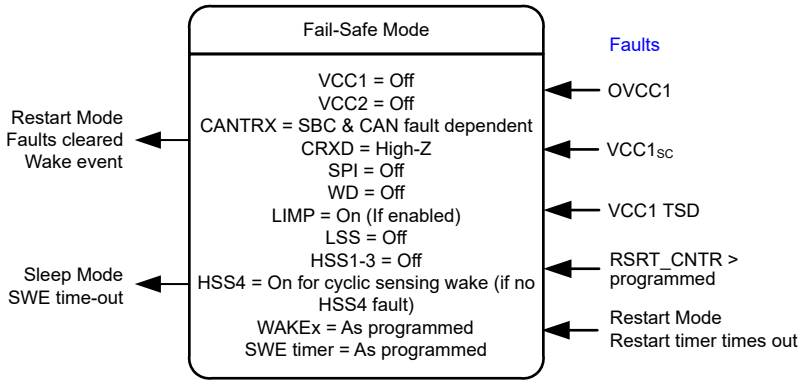


Figure 8-60. Fail-safe Mode

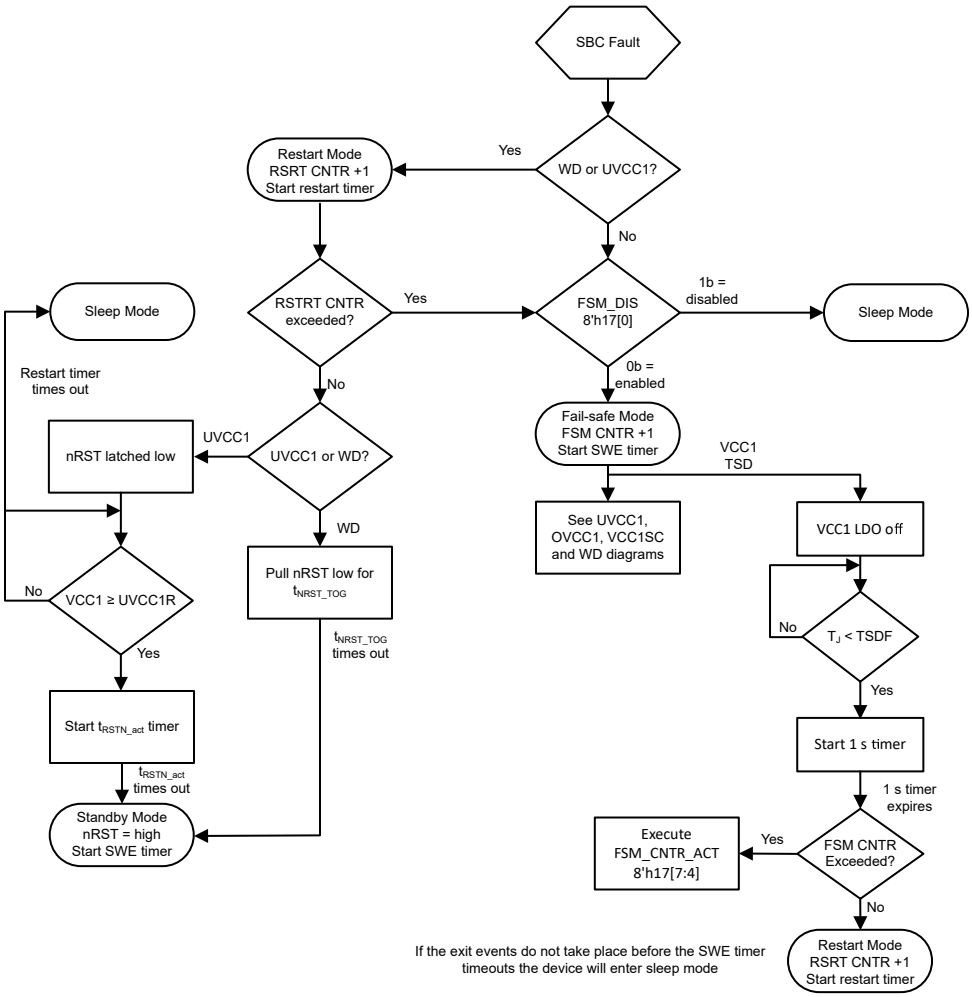


Figure 8-61. Fail-safe mode flow chart

Note

For the device to enter fail-safe mode there has to be a method for the device to wake up. This can be by the communication bus or a WAKE pin. If these are all disabled for fail-safe mode, the device automatically makes the CAN FD transceiver wake capable.

When the device enters fail-safe mode the SWE timer automatically starts.

- If SWE timer times out, the device enters sleep mode
- If a wake event takes place prior to the SWE timer timing out, the device determines if fault is still present.
  - If fault is present the device stays in fail-safe mode monitoring the fault.
  - If fault has cleared the device enters restart mode.

When the device enters fail-safe mode due to any condition other than TSD, the following takes place.

- The VCC1 regulator is turned off.
- If the device receives a wake event, the regulator is turned on for t_{REGON} to determine if the short-circuit event is present.
  - At the end of t_{REGON}, if a short circuit is detected, the device turns off the regulator and wait for next wake event.
- Over-voltage is continuously monitored immediately enters sleep mode.
- If fault is cleared, the device enters restart mode.

8.4.5.1 SBC Faults

SBC faults are faults that cause the device to change the mode of the device. If fail-safe mode is enabled, these faults cause the device to enter either restart or fail-safe mode. If fail-safe mode is disabled, the faults cause the device to enter either restart or sleep mode. SBC Faults are:

- Over-voltage for VCC1
- Under-voltage for VCC1
- Short circuit on VCC1
- Thermal Shutdown due to TSD_SBC
- Watchdog failure
- Restart counter exceeds programmed value
- SWE timer expires
- Under-voltage on VSUP is an SBC fault, but does not cause the device to enter fail-safe mode

8.4.5.2 CAN Transceiver Faults

CAN transceiver faults impact the transceiver, but and does not cause the device to enter fail-safe mode. It does turn off the CAN transmitter. The CAN transceiver faults are:

- VCC2 thermal shutdown
- CAN transceiver thermal shutdown
- CTXD pin stuck dominant - CTXD dominant timeout
- UVCAN

Note

If VCC2 is connected to VCAN, faults on VCC2 may cause a CAN fault.

8.4.6 Sleep Mode

Sleep mode is the power saving mode for the TCAN245x-Q1. In this mode, the device can wake up from the CAN bus, WAKEx pins or SW pin (if programmed). If V_{CC1} is present, SPI is available to change modes and nRST is high. If sleep mode is entered due to a fault condition, INT_2 register 8'h52[7] (SMS) is set to 1. Figure 8-62 shows the various ways that sleep mode is entered and exited.

While the device is in sleep mode, the following conditions exist:

- The CAN bus driver is disabled and the internal CAN bus termination is switched to a weak ground.
- The CAN transceiver receiver is disabled.
- The CAN low power wake up receivers are as programmed.
- WAKE pin is active.
- If cyclic sensing is enabled the selected high side switch periodically turns on.
- SW pin if programmed as a digital wake input is on.

Note

To enter sleep mode via SPI command, all wake interrupts must be cleared before issuing the SPI command for transition to Sleep mode. Additionally, at least one method to wake up must be available. If all have been disabled, the device does not enter sleep mode, and sets an interrupt, 8'h5A[3].

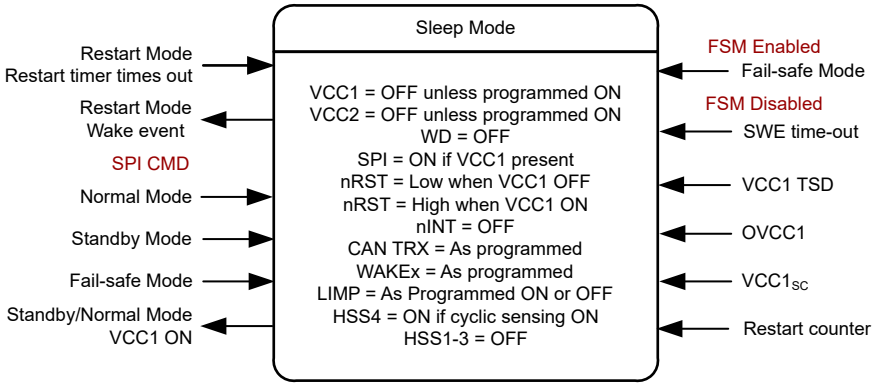


Figure 8-62. Sleep Mode

9 Device Register Tables

9.1 Device Registers

Table 9-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 9-1 should be considered as reserved locations and the register contents should not be modified.

Table 9-1. DEVICE Registers

Address	Acronym	Register Name	Section
0h	DEVICE_ID_245x	Device Part Number	Section 9.1.1
8h	REV_ID	Major and Minor Revision	Section 9.1.2
9h	SPI_CONFIG	SPI mode configuration	Section 9.1.3
Ah	CRC_CNTL	SPI CRC control	Section 9.1.4
Bh	CRC_POLY_SET	Sets SPI CRC polynomial	Section 9.1.5
Ch	SBC_CONFIG	SBC, HSS and VCC2 select	Section 9.1.6
Dh	VREG_CONFIG1	Configures VCC1 regulator	Section 9.1.7
Eh	SBC_CONFIG1	SBC Configuration	Section 9.1.8
Fh	Scratch_Pad_SPI	Read and Write Test Register SPI	Section 9.1.9
10h	CAN_CNTRL_1	CAN transceiver 1 control	Section 9.1.10
11h	WAKE_PIN_CONFIG1	WAKE pin configuration 1	Section 9.1.11
12h	WAKE_PIN_CONFIG2	WAKE pin configuration 2	Section 9.1.12
13h	WD_CONFIG_1	Watchdog configuration 1	Section 9.1.13
14h	WD_CONFIG_2	Watchdog configuration 2	Section 9.1.14
15h	WD_INPUT_TRIG	Watchdog input trigger	Section 9.1.15
16h	WD_RST_PULSE	Watchdog output pulse width	Section 9.1.16
17h	FSM_CONFIG	Fail safe mode configuration	Section 9.1.17
18h	FSM_CNTR	Fail safe mode counter	Section 9.1.18
19h	DEVICE_CONFIG0	Device reset configuration	Section 9.1.19
1Ah	DEVICE_CONFIG1	Device configuration 1	Section 9.1.20
1Bh	DEVICE_CONFIG2	Device configuration 2	Section 9.1.21
1Ch	SWE_TIMER	Sleep wake error timer configuration	Section 9.1.22
1Eh	HSS_CNTL	High side switch 1 and 2 control	Section 9.1.23
1Fh	PWM1_CNTL1	Pulse width modulation frequency configuration	Section 9.1.24
20h	PWM1_CNTL2	Pulse width modulation duty cycle two MSB select	Section 9.1.25
21h	PWM1_CNTL3	Pulse width modulation duty cycle eight LSB select	Section 9.1.26
22h	PWM2_CNTL1	Pulse width modulation 2 frequency selection	Section 9.1.27
23h	PWM2_CNTL2	Pulse width modulation duty cycle two MSB select	Section 9.1.28
24h	PWM2_CNTL3	Pulse width modulation duty cycle eight LSB select	Section 9.1.29
25h	TIMER1_CONFIG	High side switch timer 1 configuration	Section 9.1.30
26h	TIMER2_CONFIG	High side switch timer 2 configuration	Section 9.1.31
28h	RSRT_CNTR	Restart counter configuration	Section 9.1.32
29h	nRST_GFO_CNTL	nRST and GFO pin control	Section 9.1.33
2Ah	WAKE_PIN_CONFIG3	Multiple wake input configuration and reporting for WAKE pin	Section 9.1.34
2Bh	WAKE_PIN_CONFIG4		Section 9.1.35
2Dh	WD_QA_CONFIG	Question and Answer Watchdog Configuration	Section 9.1.36
2Eh	WD_QA_ANSWR	Register for writing answer to the QA watchdog	Section 9.1.37
2Fh	WD_QA_QUESTION	QA watchdog question value and error count setting	Section 9.1.38
30h	SW_ID1	Selective wake ID1 register	Section 9.1.39

Table 9-1. DEVICE Registers (continued)

Address	Acronym	Register Name	Section
31h	SW_ID2	Selective wake ID2 register	Section 9.1.40
32h	SW_ID3	Selective wake ID3 register	Section 9.1.41
33h	SW_ID4	Selective wake ID4 register	Section 9.1.42
34h	SW_ID_MASK1	Selective wake ID MASK1 register	Section 9.1.43
35h	SW_ID_MASK2	Selective wake ID MASK2 register	Section 9.1.44
36h	SW_ID_MASK3	Selective wake ID MASK3 register	Section 9.1.45
37h	SW_ID_MASK4	Selective wake ID MASK4 register	Section 9.1.46
38h	SW_ID_MASK_DLC	Selective wake ID MASK DLC register	Section 9.1.47
39h	DATA0	Selective wake DATA0	Section 9.1.48
3Ah	DATA1	Selective wake DATA1	Section 9.1.49
3Bh	DATA2	Selective wake DATA2	Section 9.1.50
3Ch	DATA3	Selective wake DATA3	Section 9.1.51
3Dh	DATA4	Selective wake DATA4	Section 9.1.52
3Eh	DATA5	Selective wake DATA5	Section 9.1.53
3Fh	DATA6	Selective wake DATA6	Section 9.1.54
40h	DATA7	Selective wake DATA7	Section 9.1.55
44h	SW_CONFIG_1	Selective wake config register1	Section 9.1.56
45h	SW_CONFIG_2	Selective wake config register2	Section 9.1.57
46h	SW_CONFIG_3	Selective wake config register3	Section 9.1.58
47h	SW_CONFIG_4	Selective wake config register4	Section 9.1.59
4Dh	HSS_CNTL2	HSS3 and 4 Control register	Section 9.1.60
4Eh	EEPROM	Customer EEPROM programming register	Section 9.1.61
4Fh	HSS_CNTL3	VHSS OV/UV, Control for Cyclic wake in Sleep mode	Section 9.1.62
50h	INT_GLOBAL	Global interrupt register	Section 9.1.63
51h	INT_1	Includes CAN, LWU, SW pin wake interrupts	Section 9.1.64
52h	INT_2	Includes UVCC1, OVCC1, UVSUP interrupts	Section 9.1.65
53h	INT_3	INT3 register	Section 9.1.66
54h	INT_CANBUS_1	CAN BUS fault interrupts	Section 9.1.67
55h	INT_7	HSS OC and OL interrupts	Section 9.1.68
56h	INT_EN_1	Enable for INT1	Section 9.1.69
57h	INT_EN_2	Enable for INT2	Section 9.1.70
58h	INT_EN_3	Enable for INT3	Section 9.1.71
59h	INT_EN_CANBUS_1	Enable for INT_CANBUS	Section 9.1.72
5Ah	INT_4	INT4 register	Section 9.1.73
5Ch	INT_6	INT6 register	Section 9.1.74
5Eh	INT_EN_4	Enable for INT4	Section 9.1.75
60h	INT_EN_6	Enable for INT6	Section 9.1.76
62h	INT_EN_7	Enable for INT7	Section 9.1.77
65h	BUCK_CONFIG1	BUCK regulator configuration register	Section 9.1.78
78h	ID_PIN_STATUS	ID Pin Status register	Section 9.1.79
79h	WAKE_ID_CONFIG1	ID1 and ID2 configuration	Section 9.1.80
7Ah	WAKE_ID_CONFIG2	ID3 and ID4 configuration	Section 9.1.81
7Bh	WAKE_PIN_CONFIG5	WKAE4 pin configuration	Section 9.1.82

Complex bit access types are encoded to fit into small table cells. Table 9-2 shows the codes that are used for access types in this section.

Table 9-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W0C	W 0C	Write 0 to clear
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

9.1.1 DEVICE_ID_245x Register (Address = 0h) [Reset = 00h]

DEVICE_ID_245x is shown in Table 9-3.

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Device part number. Offset = 0h + y; where y = 0h to 7h

Table 9-3. DEVICE_ID_245x Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEVICE_ID	R	00000000b	The DEVICE_ID[1:8] registers determine the part number of the device. The reset values and value of each DEVICE_ID register are listed for the corresponding register address Address 00h = 43h = C Address 01h = 32h = 2 Address 02h = 34h = 4 Address 03h = 35h = 5 Address 04h = 30h = 0 for TCAN2450-Q1 Address 04h = 31h = 1 for TCAN2451-Q1 Address 05h - 07h = RSVD

9.1.2 REV_ID Register (Address = 8h) [Reset = 2Xh]

REV_ID is shown in Table 9-4.

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Table 9-4. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Major_Revision	RH	0010b	Major die revision. Reset value indicate the major die revision (full layer revisions) 0001b = 1 0010b = 2
3-0	Minor_Revision	RH	xxxxb	Minor die revision. Reset value indicate the minor die revision (metal layer revisions) 0000b = 0 0001b = 1

9.1.3 SPI_CONFIG Register (Address = 9h) [Reset = 00h]

SPI_CONFIG is shown in Table 9-5.

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Table 9-5. SPI_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	Reserved
3	BYTE_CNT	R/W	0b	Selects the data byte count for a read or write operation. Note that for two byte configuration, SPI CRC is not available 0b = One byte 1b = Two byte
2	SDI_POL	R/W	0b	Selects the idle polarity of the SDI input pin by configuring the internal pull-up or pull-down resistor configuration 0b = Pull-down 1b = Pull-up
1-0	SPI_MODE	R/W	00b	Configures the SPI mode 00b = Mode 0 (CPOL is 0, CPHA is 0) 01b = Mode 1 (CPOL is 0, CPHA is 1) 10b = Mode 2 (CPOL is 1, CPHA is 0) 11b = Mode 3 (CPOL is 1, CPHA is 1)

9.1.4 CRC_CNTL Register (Address = Ah) [Reset = 00h]

CRC_CNTL is shown in Table 9-6.

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Table 9-6. CRC_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0b	Reserved
0	CRC_EN	R/W	0b	Enables SPI CRC 0b = Disable 1b = Enable

9.1.5 CRC_POLY_SET Register (Address = Bh) [Reset = 00h]

CRC_POLY_SET is shown in Table 9-7.

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Table 9-7. CRC_POLY_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0b	Reserved
0	POLY_8_SET	R/W	0b	Sets the 8-bit polynomial for CRC. 0b = X^8 + X^5 + X^3 + X^2 + X + 1 (0x2F) 1b = X^8 + X^4 + X^3 + X^2 + 1 (0x1D SAE J1850)

9.1.6 SBC_CONFIG Register (Address = Ch) [Reset = 86h]

SBC_CONFIG is shown in Table 9-8.

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Table 9-8. SBC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VCC1_OV_SEL	R/W	1b	OVCC1 threshold selection bit 0b = Lower threshold 1b = Higher threshold
6	OVCC1_ACTION	R/W	0b	Configuring the SBC action due to OVCC1 0b = Enter fail-safe mode 1b = Only set OVCC1 interrupt and do not enter fail-safe mode
5	PWM_SEL	R/W	0b	Determines which PWM is selected for programming 0b = PWM1 and PWM2 1b = PWM3 and PWM4
4	VCC1_SNK_DIS	R/W	0b	Enables/Disables VCC1 sink current 0b = VCC1 sink enabled (default) 1b = VCC1 sink disabled
3-2	SBC_MODE_SEL	RH/W	01b	Determines the mode that the SBC is in. Can be set by the controller. These bits also updated by hardware e.g. when waking up from Sleep to Standby mode or fail-safe to Standby mode 00b = Sleep 01b = Standby 10b = Normal 11b = Reserved
1-0	VCC2_CFG	R/W	10b	VCC2 voltage regulator configuration 00b = VCC2 off in all SBC modes 01b = VCC2 on in all SBC modes except Failsafe 10b = VCC2 on in all SBC modes except Sleep and Failsafe 11b = Reserved

9.1.7 VREG_CONFIG1 Register (Address = Dh) [Reset = A0h]

VREG_CONFIG1 is shown in Table 9-9.

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Table 9-9. VREG_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VCC1_CFG	R/W	10b	VCC1 voltage regulator configuration 00b = Reserved 01b = On in all SBC modes except Fail-safe mode 10b = On in all SBC modes except Sleep and Fail-safe modes 11b = Reserved
5	FPWM_OVSUP_DIS	R/W	1b	Disable FPWM on OVSUP to reduce ringing on VCC1 output at High VSUP values. If selected, the buck regulator automatically switches to PFM mode 0b = Do not disable FPWM on OVSUP 1b = Disable FPWM on OVSUP
4	RESERVED	R	0b	Reserved
3	VCC1_SINK	R/W	0b	VCC1 current sink strength selection 0b = 10µA 1b = 1000µA
2-0	RESERVED	R	0b	Reserved

9.1.8 SBC_CONFIG1 Register (Address = Eh) [Reset = 01h]

SBC_CONFIG1 is shown in Table 9-10.

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Table 9-10. SBC_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	FSM_CYC_WK_EN	R/W	0b	Enables cyclic wake in fail-safe mode 0b = Disabled 1b = Enabled
5	VCC1_SLP_ACT	R/W	0b	Action to take when VCC1 is enabled on in sleep mode due to a wake event 0b = Indicate wake event with nINT/RXD pins only, device remains in Sleep mode 1b = Transition to Standby mode via Restart mode
4-3	UVCC1_SEL	R/W	00b	VCC1 under-voltage threshold selection 00b = Threshold 1 01b = Threshold 2 10b = Threshold 3 11b = Threshold 4
2	SW_FSM_EN	R/W	0b	Enables the SW pin to become a digital wake up pin when in Fail-safe mode 0b = Disabled 1b = Enabled
1	SW_SLP_EN	R/W	0b	Enables the SW pin to become a digital wake up pin when in Sleep mode 0b = Disabled 1b = Enabled
0	SW_POL_SEL	R/W	1b	SW pin polarity select 0b = Active low 1b = Active high

9.1.9 Scratch_Pad_SPI Register (Address = Fh) [Reset = 00h]

Scratch_Pad_SPI is shown in Table 9-11.

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Table 9-11. Scratch_Pad_SPI Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Scratch_Pad	R/W	00000000b	Read and Write Test Pad for SPI

9.1.10 CAN_CNTRL_1 Register (Address = 10h) [Reset = 04h]

CAN_CNTRL_1 is shown in Table 9-12.

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Table 9-12. CAN_CNTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_EN	R/W	0b	Selective wake enable 0b = Disabled 1b = Enabled
6	TXD_DTO_DIS	R/W	0b	CAN TXD Dominant time out disable control 0b = Enabled 1b = Disabled
5	FD_EN	R/W	0b	Bus fault diagnostic enable 0b = Disabled 1b = Enabled
4	RESERVED	R	0b	Reserved
3	CAN1_FSM_DIS	R/W	0b	Sets the CAN transceiver operating state when device enters FSM 0b = Wake capable 1b = Off
2-0	CAN1_TRX_SEL	R/W	100b	CAN transceiver control 000b = Off 001b = Reserved 010b = SBC Mode Control WUP disabled 011b = Reserved 100b = Wake capable 101b = Listen 110b = SBC Mode Control 111b = On

9.1.11 WAKE_PIN_CONFIG1 Register (Address = 11h) [Reset = 00h]

WAKE_PIN_CONFIG1 is shown in Table 9-13.

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Table 9-13. WAKE_PIN_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WAKE_CONFIG	R/W	00b	Wake pin configuration: Note: Pulse requires more programming 00b = Bi-directional - either edge 01b = Rising edge 10b = Falling edge 11b = Pulse
5	WAKE1_STAT	RH	0b	Provides status of WAKE1 pin. 0b = Low 1b = High
4	RESERVED	R	0b	Reserved
3-2	WAKE_PULSE_INVALID	R/W	00b	Pulses less than or equal to these pulses are considered invalid 00b = 5ms and sets tWAKE_WIDTH_MIN to 10ms 01b = 10ms and sets tWAKE_WIDTH_MIN to 20ms 10b = 20ms and sets tWAKE_WIDTH_MIN to 40ms 11b = 40ms and sets tWAKE_WIDTH_MIN to 80ms
1-0	WAKE_PULSE_MAX	R/W	00b	Maximum WAKE pin input pulse width to be considered valid. 00b = 750ms 01b = 1000ms 10b = 1500ms 11b = 2000ms

9.1.12 WAKE_PIN_CONFIG2 Register (Address = 12h) [Reset = 02h]

WAKE_PIN_CONFIG2 is shown in Table 9-14.

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Table 9-14. WAKE_PIN_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE_PULSE_CONFIG	R/W	0b	Sets the expected pulse direction for all wake pins 0b = Low->High->Low 1b = High->Low->High
6	WAKE1_SENSE	R/W	0b	WAKE1 pin configured for static or cyclic sensing wake 0b = Static Sensing 1b = Cyclic Sensing
5	TWK_CYC_SET	R/W	0b	Sets the tWK_CYC time (µs) for determining WAKE pin status for cyclic sensing for all WAKE pins 0b = 35 us 1b = 100 us
4-3	nINT_SEL	R/W	00b	nINT configuration selection 00b = Global interrupt 01b = Watchdog failure output 10b = Bus fault interrupt 11b = Wake request
2	RXD_WK_CONFIG	R/W	0b	Configures RXD pin behavior from a wake event 0b = Pulled low 1b = Toggle
1-0	WAKE1_LEVEL	R/W	10b	Sets the WAKE1 pin input thresholds 00b = VCC1 01b = 2.5V 10b = 4V 11b = 6V

9.1.13 WD_CONFIG_1 Register (Address = 13h) [Reset = 82h]

WD_CONFIG_1 is shown in Table 9-15.

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Table 9-15. WD_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_CONFIG	R/W	10b	Watchdog configuration 00b = Disabled 01b = Timeout 10b = Window 11b = Q&A
5-4	WD_PRE	R/W	00b	Watchdog pre-scalar 00b = Factor 1 01b = Factor 2 10b = Factor 3 11b = Factor 4
3	WD_SLP_EN	R/W	0b	Enables watchdog in Sleep mode 0b = watchdog disabled in Sleep mode 1b = watchdog enabled in Sleep mode
2	WD_STBY_TYPE	R/W	0b	Selects the watchdog type in Standby mode if enabled 0b = Timeout 1b = Matches the watchdog type in Normal mode
1-0	WD_LW_SEL	R/W	10b	Selects the long window duration in Standby mode. 00b = 150ms 01b = 300ms 10b = 600ms (default) 11b = 1000ms

9.1.14 WD_CONFIG_2 Register (Address = 14h) [Reset = 60h]

WD_CONFIG_2 is shown in Table 9-16.

Return to the Summary Table.

Table 9-16. WD_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	WD_TIMER	R/W	011b	Sets window or timeout times based upon the WD_PRE setting, See WD_TIMER table
4-1	WD_ERR_CNT	RH	0000b	Watchdog error counter Running count of errors up to 15 errors
0	WD_STBY_DIS	R/W	0b	Disables the watchdog in standby mode. 0b = Enabled 1b = Disabled

9.1.15 WD_INPUT_TRIG Register (Address = 15h) [Reset = 00h]

WD_INPUT_TRIG is shown in Table 9-17.

Return to the Summary Table.

Table 9-17. WD_INPUT_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_INPUT	R/W1C	00000000b	Write FFh to trigger WD at appropriate time

9.1.16 WD_RST_PULSE Register (Address = 16h) [Reset = 00h]

WD_RST_PULSE is shown in Table 9-18.

Return to the Summary Table.

Table 9-18. WD_RST_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	WD_ERR_CNT_SET	R/W	0000b	Sets the watchdog event error counter that upon overflow the watchdog output and action triggers
3-0	RSRT_CNTR	R/W1C	0000b	Provides the number of times the device has entered restart mode and should be cleared prior to reaching the RSRT_CNTR_SEL value

9.1.17 FSM_CONFIG Register (Address = 17h) [Reset = 00h]

FSM_CONFIG is shown in Table 9-19.

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Table 9-19. FSM_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FSM_CNTR_ACT	R/W	0000b	Action if fail safe counter exceeds programmed value 0000b = Disabled 0001b = Reserved 0010b = Reserved 0011b = Perform hard reset - POR 0100b = Stop responding to wake events and go to sleep until power cycle reset
3-1	FSM_SLP_STAT	RH	000b	Reason for entering fail-safe or sleep mode 000b = Status Clear 001b = Thermal shut down event 010b = Reserved 011b = VCC1 fault 100b = Reserved 101b = SWE Timer (Sleep Mode) 110b = Reserved 111b = Restart counter exceeded These values are held until cleared by writing oh to FSM_CNTR_STAT
0	FSM_DIS	R/W	0b	Fail safe mode disable 0b = Enabled 1b = Disabled

9.1.18 FSM_CNTR Register (Address = 18h) [Reset = 00h]

FSM_CNTR is shown in Table 9-20.

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Table 9-20. FSM_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FSM_CNTR_SET	R/W	0000b	Sets the number of times FS mode enters before action taken per FSM_CNTR_ACT. 0000b = 1 0001b = 1 0010b = 2 0011b = 3 0100b = 4 0101b = 5 0110b = 6 0111b = 7 1000b = 8 1001b = 9 1010b = 10 1011b = 11 1100b = 12 1101b = 13 1110b = 14 1111b = 15
3-0	FSM_CNTR_STAT	RH/W0C	0000b	Reads back the number of time FSM has been entered in a row up to 15. Can be cleared by writing 0h.

9.1.19 DEVICE_CONFIG0 Register (Address = 19h) [Reset = 20h]

DEVICE_CONFIG0 is shown in Table 9-21.

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Table 9-21. DEVICE_CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	NVM_REV	R	0010b	Internal NVM revision
3-2	RESERVED	R	0b	Reserved
1	SF_RST	R/W1C	0b	Soft Reset: Writing a 1 causes a soft reset. Device registers return to default values while keeping the regulators on.
0	HD_RST	R/W1C	0b	Hard Reset: Forces a power on reset on writing a 1. This sets the PWRON interrupt flag

9.1.20 DEVICE_CONFIG1 Register (Address = 1Ah) [Reset = 00h]

DEVICE_CONFIG1 is shown in Table 9-22.

Return to the Summary Table.

Table 9-22. DEVICE_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LIMP_SLP_FLT_EN	R/W	0b	Turn on LIMP in Sleep mode for TSD and VCC1 faults (in addition to watchdog fault) 0b = Disabled 1b = Enabled
6-5	RESERVED	R	0b	Reserved
4	LIMP_DIS	R/W	0b	Configures the LIMP function 0b = Enabled 1b = Disabled
3-2	LIMP_SEL_RESET	R/W	00b	Selects the method to reset/turn off LIMP 00b = On third successful input trigger the error counter receives 01b = First correct input trigger 10b = Reserved 11b = Reserved
1	LIMP_RESET	R/W1C	0b	LIMP reset. Writing 1b to this bit resets the LIMP pin and bit is cleared automatically. Note: If the fault causing the LIMP pin to go active is not cleared, the LIMP pin is set to active again.
0	FSM_CYC_SEN_EN	R/W	0b	Enables cyclic sensing wake up for fail-safe mode 0b = Disabled 1b = Enabled

9.1.21 DEVICE_CONFIG2 Register (Address = 1Bh) [Reset = 00h]

DEVICE_CONFIG2 is shown in Table 9-23.

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Table 9-23. DEVICE_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LIMP_LSS_SEL	R/W	00b	Selects LIMP pin function. Note: This register field readsback 00b if 8'h1A[4]=0b (LIMP functionality is enabled) 00b = LIMP 01b = Low side switch 10b = Reserved 11b = Reserved
5-3	LIMP_LSS_CNTL	R/W	000b	Selects the output of LSS at the LIMP pin 000b = Off 001b = PWM1 010b = PWM2 011b = Timer1 100b = Timer2 101b = On 110b = PWM3 111b = PWM4
2	VSUP_UVLO_SEL	R/W	0b	Selects the UVLO level on VSUP at which the buck regulator is turned off 0b = Lower UVLO Level (Typ 3.2V) 1b = Higher UVLO Level (Typ 5V)
1	WAKE_WIDTH_MAX_DIS	R/W	0b	Disables the Max limit, tWK_PULSE_WIDTH_MAX detection when pulse is selected for WAKE pin configuration. 0b = Enabled 1b = Disabled
0	RESERVED	R	0b	Reserved

9.1.22 SWE_TIMER Register (Address = 1Ch) [Reset = 28h]

SWE_TIMER is shown in Table 9-24.

Return to the Summary Table.

Table 9-24. SWE_TIMER Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SWE_EN	R/W	0b	Sleep wake error enable: NOTE: This enables the SWE timer when coming out of sleep mode on a wake event. If this is enabled a SPI read or write must take place within this four minute window or the device goes back to sleep. This does not disable the function for initial power on or in case of a power on reset. 0b = Disabled 1b = Enabled
6-3	SWE_TIMER_SET	R/W	0101b	Sets the timer used for tINACTIVE in minutes 0000b = 2 0001b = 2.5 0010b = 3 0011b = 3.5 0100b = 4 0101b = 4.5 0110b = 5 0111b = 5.5 1000b = 6 1001b = 6.5 1010b = 8 1011b = 8.5 1100b = 10
2	CANSLNT_SWE_DIS	R/W	0b	Disables the SWE timer connection with the CANSLNT flag. 0b = Enabled 1b = Disabled
1-0	RESERVED	R	0b	Reserved

9.1.23 HSS_CNTL Register (Address = 1Eh) [Reset = 00h]

HSS_CNTL is shown in Table 9-25.

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Table 9-25. HSS_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6-4	HSS1_CNTL	R/W	000b	Control for high side switch 1 000b = Off 001b = PWM1 010b = PWM2 011b = Timer1 100b = Timer2 101b = On 110b = PWM3 111b = PWM4
3	RESERVED	R	0b	Reserved
2-0	HSS2_CNTL	R/W	000b	Control for high side switch 2 000b = Off 001b = PWM1 010b = PWM2 011b = Timer1 100b = Timer2 101b = On 110b = PWM3 111b = PWM4

9.1.24 PWM1_CNTL1 Register (Address = 1Fh) [Reset = 00h]

PWM1_CNTL1 is shown in Table 9-26.

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Table 9-26. PWM1_CNTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM1_FREQ	R/W	0b	Selects PWM1 frequency (Hz) 0b = 200 1b = 400
6-0	RESERVED	R	0b	Reserved

9.1.25 PWM1_CNTL2 Register (Address = 20h) [Reset = 00h]

PWM1_CNTL2 is shown in Table 9-27.

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Table 9-27. PWM1_CNTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0b	Reserved
1-0	PWM1_DC_MSB	R/W	00b	Most significant two bits for 10-bit PWM1 duty cycle select. Works with 'h21[7:0] Note: When configuring HSS3 it is best to align PWM3 if PWM is to be used. PWM1 control changes to PWM3 when register 8'hC[5] = 0b. 00b = 100% off when used with 'h21[7:0] 11b = 100% on when used with h21[7:0]

9.1.26 PWM1_CNTL3 Register (Address = 21h) [Reset = 00h]

PWM1_CNTL3 is shown in Table 9-28.

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Table 9-28. PWM1_CNTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWM1_DC	R/W	00000000b	Bits 7-0 for 10-bit PWM1 duty cycle select. Works with 'h20[1:0] Note: When configuring HSS3 it is best to align PWM3 if PWM is to be used. PWM1 control changes to PWM3 when register 8'hC[5] = 0b.

9.1.27 PWM2_CNTL1 Register (Address = 22h) [Reset = 00h]

PWM2_CNTL1 is shown in Table 9-29.

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Table 9-29. PWM2_CNTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM2_FREQ	R/W	0b	Selects PWM2 frequency (Hz) 0b = 200 1b = 400
6-0	RESERVED	R	0b	Reserved

9.1.28 PWM2_CNTL2 Register (Address = 23h) [Reset = 00h]

PWM2_CNTL2 is shown in Table 9-30.

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Table 9-30. PWM2_CNTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0b	Reserved
1-0	PWM2_DC_MSB	R/W	00b	Most significant two bits for 10-bit PWM2 duty cycle select. Works with 'h24[7:0] Note: When configuring HSS4 it is best to align PWM4 if PWM is to be used. PWM2 control changes to PWM4 when register 8'hC[5] = 0b. 00b = 100% off when used with 'h24[7:0] 11b = 100% on when used with 'h24[7:0]

9.1.29 PWM2_CNTL3 Register (Address = 24h) [Reset = 00h]

PWM2_CNTL3 is shown in Table 9-31.

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Table 9-31. PWM2_CNTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWM2_DC	R/W	00000000b	Bits 7-0 for 10-bit PWM2 duty cycle select. Works with 'h23[1:0] Note: When configuring HSS4 it is best to align PWM4 if PWM is to be used. PWM2 control changes to PWM4 when register 8'hC[5] = 0b.

9.1.30 TIMER1_CONFIG Register (Address = 25h) [Reset = 00h]

TIMER1_CONFIG is shown in Table 9-32.

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Table 9-32. TIMER1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TIMER1_ON_WIDTH	R/W	0000b	Sets the high side switch on time (ms) for timer 1 0000b = Off (HSS is high impedance) 0001b = 0.1 0010b = 0.3 0011b = 0.5 0100b = 1 0101b = 10 0110b = 20 0111b = 30 1000b = 40 1001b = 50 1010b = 60 1011b = 80 1100b = 100 1101b = 150 1110b = 200 1111b = On (HSS is on 100%)
3	TIMER1_CYC_WK_EN	R/W	0b	Enables Cyclic Wake using Timer 1 0b = Disabled 1b = Enabled
2-0	TIMER1_PERIOD	R/W	000b	Sets the timer period (ms) for timer 1 000b = 10 001b = 20 010b = 50 011b = 100 100b = 200 101b = 500 110b = 1000 111b = 2000

9.1.31 TIMER2_CONFIG Register (Address = 26h) [Reset = 00h]

TIMER2_CONFIG is shown in Table 9-33.

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Table 9-33. TIMER2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TIMER2_ON_WIDTH	R/W	0000b	Sets the high side switch on time (ms) for timer 2 0000b = Off (HSS is high impedance) 0001b = 0.1 0010b = 0.3 0011b = 0.5 0100b = 1 0101b = 10 0110b = 20 0111b = 30 1000b = 40 1001b = 50 1010b = 60 1011b = 80 1100b = 100 1101b = 150 1110b = 200 1111b = On (HSS is on 100%)
3	TIMER2_CYC_WK_EN	R/W	0b	Enables Cyclic Wake using Timer 2 0b = Disabled 1b = Enabled
2-0	TIMER2_PERIOD	R/W	000b	Sets the timer period (ms) for timer 2 000b = 10 001b = 20 010b = 50 011b = 100 100b = 200 101b = 500 110b = 1000 111b = 2000

9.1.32 RSRT_CNTR Register (Address = 28h) [Reset = 40h]

RSRT_CNTR is shown in Table 9-34.

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Table 9-34. RSRT_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RSRT_CNTR_SEL	R/W	0100b	Selects the number of times the device can enter restart mode prior to device entering sleep mode, 0 to 15 times. Note: Writing 0h here disables the restart counter.
3-0	RESERVED	R	0b	Reserved

9.1.33 nRST_GFO_CNTL Register (Address = 29h) [Reset = 0Ch]

nRST_GFO_CNTL is shown in Table 9-35.

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Table 9-35. nRST_GFO_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0b	Reserved
5	nRST_PULSE_WIDTH	R/W	0b	Sets the pulse width for nRST when the device enters restart mode due to WD failure or nRST release delay after VCC1 clears UVCC1 threshold 0b = 2ms 1b = 15ms
4	GFO_POL_SEL	R/W	0b	Selects the polarity for the GFO pin Note: When 8'h29[3:1] = 110b, this bit determines the state of the GFO output 0b = Active low 1b = Active high
3-1	GFO_SEL	R/W	110b	Selects the information that causes this pin to be pulled to the state selected by 'h29[4] for tNRST_TOG except for when general purpose output is selected 000b = VCC1/2 interrupt (overvoltage, undervoltage or short) 001b = WD interrupt event (each one) 010b = Reserved 011b = Local wake request (LWU) 100b = Bus wake request (WUP) 101b = Restart counter exceeded (indicated in standby mode) 110b = General purpose output 111b = CAN Bus fault
0	RESERVED	R	0b	Reserved

9.1.34 WAKE_PIN_CONFIG3 Register (Address = 2Ah) [Reset = F0h]

WAKE_PIN_CONFIG3 is shown in Table 9-36.

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Table 9-36. WAKE_PIN_CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE4_PIN_SET	R/W	1b	Configures whether WAKE4 is active or inactive 0b = WAKE4 inactive 1b = WAKE4 active
6	WAKE3_PIN_SET	R/W	1b	Configures whether WAKE3 is active or inactive 0b = WAKE3 inactive 1b = WAKE3 active
5	WAKE2_PIN_SET	R/W	1b	Configures whether WAKE2 is active or inactive 0b = WAKE2 inactive 1b = WAKE2 active
4	WAKE1_PIN_SET	R/W	1b	Configures whether WAKE1 is active or inactive 0b = WAKE1 inactive 1b = WAKE1 active
3-0	MULTI_WAKE_STAT	R/W0C	0000b	Provides which WAKE input state has changed based upon specific bits. Bits represent WAKE input so if multiple WAKE input bits are set indicates that those specific WAKE inputs cause the WAKE event. 0001b = Wake 1 0010b = Wake 2 0100b = Wake 3 1000b = Wake 4

9.1.35 WAKE_PIN_CONFIG4 Register (Address = 2Bh) [Reset = 22h]

WAKE_PIN_CONFIG4 is shown in Table 9-37.

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Table 9-37. WAKE_PIN_CONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE2_SENSE	R/W	0b	WAKE2 pin configured for static or cyclic sensing wake 0b = Static sensing 1b = Cyclic sensing
6	WAKE2_STAT	RH	0b	Provides status of WAKE2 pin. 0b = Low 1b = High
5-4	WAKE2_LEVEL	R/W	10b	Sets the WAKE2 pin input thresholds 00b = VCC1 01b = 2.5V 10b = 4V 11b = 6V
3	WAKE3_SENSE	R/W	0b	WAKE3 pin configured for static or cyclic sensing wake 0b = Static sensing 1b = Cyclic sensing
2	WAKE3_STAT	RH	0b	Provides status of WAKE3 pin. 0b = Low 1b = High
1-0	WAKE3_LEVEL	R/W	10b	Sets the WAKE3 pin input thresholds 00b = VCC1 01b = 2.5V 10b = 4V 11b = 6V

9.1.36 WD_QA_CONFIG Register (Address = 2Dh) [Reset = 0Ah]

WD_QA_CONFIG is shown in Table 9-38.

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Table 9-38. WD_QA_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_ANSW_GEN_CFG	R/W	00b	WD answer generation configuration
5-4	WD_QA_POLY_CFG	R/W	00b	WD Q&A polynomial configuration
3-0	WD_QA_POLY_SEED	R/W	1010b	WD Q&A polynomial seed value loaded when device is in the RESET state

9.1.37 WD_QA_ANSWR Register (Address = 2Eh) [Reset = 00h]

WD_QA_ANSWR is shown in Table 9-39.

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Table 9-39. WD_QA_ANSWR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_QA_ANSWER	R/W1C	00000000b	MCU Q&A Watchdog answer

9.1.38 WD_QA_QUESTION Register (Address = 2Fh) [Reset = 3Ch]

WD_QA_QUESTION is shown in Table 9-40.

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Table 9-40. WD_QA_QUESTION Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	QA_ERROR	R/W1C	0b	Watchdog Q&A answer error flag
5-4	WD_ANSW_CNT	RH	11b	Current state of received watchdog Q&A error counter
3-0	WD_QUESTION	RH	1100b	Current watchdog question value

9.1.39 SW_ID1 Register (Address = 30h) [Reset = 00h]

SW_ID1 is shown in Table 9-41.

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Table 9-41. SW_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_17:10	R/W	00000000b	Extended ID bits 17:10

9.1.40 SW_ID2 Register (Address = 31h) [Reset = 00h]

SW_ID2 is shown in Table 9-42.

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Table 9-42. SW_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_9:2	R/W	00000000b	Extended ID bits 9:2

9.1.41 SW_ID3 Register (Address = 32h) [Reset = 00h]

SW_ID3 is shown in Table 9-43.

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Table 9-43. SW_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	EXT_ID_1:0	R/W	00b	Extended ID bits 1:0
5	IDE	R/W	0b	Extended ID field 0b = Standard ID (11-bits) 1b = Extended ID (29-bits)
4-0	ID_10:6__EXT_ID_28:24	R/W	00000b	ID[10:6] and Extended ID[28:24]

9.1.42 SW_ID4 Register (Address = 33h) [Reset = 00h]

SW_ID4 is shown in Table 9-44.

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Table 9-44. SW_ID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	ID_5:0__EXT_ID_23:18	R/W	000000b	ID[5:0] and Extended ID[23:18]
1-0	RESERVED	R	0b	Reserved

9.1.43 SW_ID_MASK1 Register (Address = 34h) [Reset = 00h]

SW_ID_MASK1 is shown in Table 9-45.

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Table 9-45. SW_ID_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0b	Reserved
1-0	EXT_ID_MASK_17:16	R/W	00b	Extended ID Mask 17:16

9.1.44 SW_ID_MASK2 Register (Address = 35h) [Reset = 00h]

SW_ID_MASK2 is shown in Table 9-46.

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Table 9-46. SW_ID_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_MASK_15:8	R/W	00000000b	Extended ID Mask 15:8

9.1.45 SW_ID_MASK3 Register (Address = 36h) [Reset = 00h]

SW_ID_MASK3 is shown in Table 9-47.

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Table 9-47. SW_ID_MASK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_MASK_7:0	R/W	00000000b	Extended ID Mask 7:0

9.1.46 SW_ID_MASK4 Register (Address = 37h) [Reset = 00h]

SW_ID_MASK4 is shown in Table 9-48.

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Table 9-48. SW_ID_MASK4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ID_MASK_10:3__EXT_ID_MASK_28:21	R/W	00000000b	ID Mask 10:3 and Extended ID Mask 28:21 (Base ID)

9.1.47 SW_ID_MASK_DLC Register (Address = 38h) [Reset = 00h]

SW_ID_MASK_DLC is shown in Table 9-49.

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Table 9-49. SW_ID_MASK_DLC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	ID_MASK_2:0__EXT_ID_MASK_20:18	R/W	000b	ID Mask 2:0 and Extended ID Mask 20:18 (Base ID)
4-1	DLC	R/W	0000b	DLC[3:0]
0	DATA_MASK_EN	R/W	0b	Data mask enable 0b = DLC field and Data field are not compared and assumed valid. Remote frames are allowed. 1b = DLC field must match DLC[3:0] register and data field bytes are compared with DATAx registers for a matching 1. Remote frames are ignored

9.1.48 DATA0 Register (Address = 39h) [Reset = 00h]

DATA0 is shown in Table 9-50.

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Table 9-50. DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA0	R/W	00000000b	CAN data byte 0

9.1.49 DATA1 Register (Address = 3Ah) [Reset = 00h]

DATA1 is shown in Table 9-51.

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Table 9-51. DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA1	R/W	00000000b	CAN data byte 1

9.1.50 DATA2 Register (Address = 3Bh) [Reset = 00h]

DATA2 is shown in Table 9-52.

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Table 9-52. DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA2	R/W	00000000b	CAN data byte 2

9.1.51 DATA3 Register (Address = 3Ch) [Reset = 00h]

DATA3 is shown in Table 9-53.

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Table 9-53. DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA3	R/W	00000000b	CAN data byte 3

9.1.52 DATA4 Register (Address = 3Dh) [Reset = 00h]

DATA4 is shown in Table 9-54.

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Table 9-54. DATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA4	R/W	00000000b	CAN data byte 4

9.1.53 DATA5 Register (Address = 3Eh) [Reset = 00h]

DATA5 is shown in Table 9-55.

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Table 9-55. DATA5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA5	R/W	00000000b	CAN data byte 5

9.1.54 DATA6 Register (Address = 3Fh) [Reset = 00h]

DATA6 is shown in Table 9-56.

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Table 9-56. DATA6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA6	R/W	00000000b	CAN data byte 6

9.1.55 DATA7 Register (Address = 40h) [Reset = 00h]

DATA7 is shown in Table 9-57.

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Table 9-57. DATA7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA7	R/W	00000000b	CAN data byte 7

9.1.56 SW_CONFIG_1 Register (Address = 44h) [Reset = 50h]

SW_CONFIG_1 is shown in Table 9-58.

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Table 9-58. SW_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_FD_PASSIVE	R/W	0b	Selective Wake FD Passive: this bit modifies the behavior of the error counter when CAN with flexible data rate frames are seen. 0b = CAN with flexible data rate frame counts as an error frame 1b = CAN with flexible data rate frame are ignored (passive)
6-4	CAN_DR	R/W	101b	CAN bus data rate 000b = 50Kbps 001b = 100Kbps 010b = 125Kbps 011b = 250Kbps 100b = Reserved 101b = 500Kbps 110b = Reserved 111b = 1Mbps
3-2	FD_DR	R/W	00b	CAN bus FD data rate 10b = CAN FD 8Mbps versus 500k CAN data rate 11b = Reserved
1-0	RESERVED	R	0b	Reserved

9.1.57 SW_CONFIG_2 Register (Address = 45h) [Reset = 00h]

SW_CONFIG_2 is shown in Table 9-59.

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Table 9-59. SW_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FRAME_CNTx	RH	00000000b	Frame Error Counter: this error counter is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. In case the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame does not impact the frame error counter (no increment or decrement). If the frame counter reaches FRAME_CNT_THRESHOLD[7:0] value the next increment overflows the counter, set FRAME_OVF flag. The counter is reset by the following: enabling the frame detection or tSILENCE detection.

9.1.58 SW_CONFIG_3 Register (Address = 46h) [Reset = 1Fh]

SW_CONFIG_3 is shown in Table 9-60.

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Table 9-60. SW_CONFIG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FRAME_CNT_THRESHOLD	R/W	00011111b	Frame Error Counter Threshold: these bits set the point at which the error counter reaches its maximum and on the next error frame overflows and sets the FRAME_OVF flag. Default is 31 so the 32nd error sets the overflow flag.

9.1.59 SW_CONFIG_4 Register (Address = 47h) [Reset = 00h]

SW_CONFIG_4 is shown in Table 9-61.

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Table 9-61. SW_CONFIG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SWCFG	R/W	0b	Selective wake configuration complete. Note: Writing to any of these wake configuration registers (8'h30-8'h44, 8'h46) clears the SWCFG bit. 0b = SW registers not configured or received a FRAME_OVF fault. 1b = SW registers configured Note: Make this the last step in configuring and turning on selective wake.
6	CAN_SYNC_FD	RH	0b	device is properly decoding CAN FD frames if frame detection is enabled. This flag, is updated after every received frame. By polling this flag the system may determine if the device is properly decoding CAN FD frames, up to but not including the Data Field. This flag is self-clearing.
5	CAN_SYNC	RH	0b	Synchronized to CAN data: this flag indicates the device is properly decoding CAN frames if frame detection is enabled. This flag is updated after every received frame. By polling this flag, the system may determine if the device is properly decoding CAN frames. This flag is self-clearing.
4-0	RESERVED	R	0b	Reserved

9.1.60 HSS_CNTL2 Register (Address = 4Dh) [Reset = 00h]

HSS_CNTL2 is shown in Table 9-62.

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Table 9-62. HSS_CNTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6-4	HSS3_CNTL	R/W	000b	Control for high side switch 3 000b = Off 001b = PWM1 010b = PWM2 011b = Timer1 100b = Timer2 101b = On 110b = PWM3 111b = PWM4
3	RESERVED	R	0b	Reserved
2-0	HSS4_CNTL	R/W	000b	Control for high side switch 4 000b = Off 001b = PWM1 010b = PWM2 011b = Timer1 100b = Timer2 101b = On 110b = PWM3 111b = PWM4

9.1.61 EEPROM Register (Address = 4Eh) [Reset = 00h]

EEPROM is shown in Table 9-63.

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Table 9-63. EEPROM Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EEPROM_SAVE	R/W	0b	Saves configuration bits to EEPROM. Write a 1b and correct code to register 8'h4E[3:0] to save configuration bits to EEPROM. Self clears after EEPROM is written to.
6	EEPROM_CRC_CHK	R/W	0b	Force EEPROM CRC check 0b = Do not read or check CRC 1b = Force read and CRC check
5	EEPROM_RELOAD	R/W	0b	Forces memory to be reloaded from EEPROM 0b = Don not reload 1b = Reload EEPROM
4	RESERVED	R	0b	Reserved
3-0	EEPROM_CODE	R/W	0000b	Code to access EERPOM

9.1.62 HSS_CNTL3 Register (Address = 4Fh) [Reset = 00h]

HSS_CNTL3 is shown in Table 9-64.

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Table 9-64. HSS_CNTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSS_OV_SD_DIS	R/W	0b	Configures HSS shut-down due to OVHSS 0b = HSS are shut-off due to OVHSS 1b = HSS remain ON even during OVHSS
6	HSS_UV_SD_DIS	R/W	0b	Configures HSS shut-down due to UVHSS 0b = HSS are shut-off due to UVHSS 1b = HSS remain ON even during UVHSS
5	HSS_OV_UV_REC	R/W	0b	Configures the auto-recovery of the high-side switches when turned off due to an OVHSS or UVHSS event 0b = Enabled (auto-recovers HSS outputs when OV/UVHSS event is cleared) 1b = Disabled (auto-recovery disabled. Controller has to manually turn the HSS back on after the OV/UVHSS event is cleared)
4	SLP_CYC_WK_EN	R/W	0b	Enables cyclic wake when in sleep mode based upon timer1 or timer2 0b = Disabled 1b = Enabled
3	RESERVED	R	0b	Reserved
2	VCC2_STATUS	RH	0b	VCC2 LDO status 0b = UVCC2 or off 1b = In regulation
1	VCAN_STATUS	RH	0b	VCAN LDO status 0b = UVCAN or off 1b = In regulation
0	RSTRT_TIMER_SEL	R/W	0b	Selects the restart timer used to exit restart mode if VCC1 does not exceed UVCC1R 0b = tRSTTO 1b = tINACTIVE

9.1.63 INT_GLOBAL Register (Address = 50h) [Reset = 00h]

INT_GLOBAL is shown in Table 9-65.

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Table 9-65. INT_GLOBAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_7	RH	0b	Logical OR of INT_7
6	INT_1	RH	0b	Logical OR of INT_1
5	INT_2	RH	0b	Logical OR of INT_2
4	INT_3	RH	0b	Logical OR of INT_3
3	INT_CANBUS	RH	0b	Logical OR of INT_CANBUS register
2	INT_4	RH	0b	Logical OR of INT_4
1	RESERVED	R	0b	Reserved
0	INT_6	RH	0b	Logical OR of INT_6

9.1.64 INT_1 Register (Address = 51h) [Reset = 00h]

INT_1 is shown in Table 9-66.

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Table 9-66. INT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD	R/W1C	0b	Watchdog event interrupt. NOTE: This interrupt bit is set for every watchdog error event and does not rely upon the Watchdog error counter
6	CANINT_1	R/W1C	0b	CAN bus wake up interrupt
5	LWU	R/W1C	0b	Local wake up
4	WKERR	R/W1C	0b	Wake error bit is set when the SWE timer has expired and the state machine has returned to Sleep mode
3	FRAME_OVF_1	R/W1C	0b	Frame error counter overflow
2	CANSLNT_1	R/W1C	0b	CAN bus inactive for tSILENCE
1	SWPIN_WU	R/W1C	0b	SW pin wake up interrupt
0	CANDOM_1	R/W1C	0b	CAN bus stuck dominant

9.1.65 INT_2 Register (Address = 52h) [Reset = 40h]

INT_2 is shown in Table 9-67.

Return to the Summary Table.

Table 9-67. INT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SMS	R/W1C	0b	Sleep mode status flag. Only sets when sleep mode is entered by a WKERR, UVIO timeout or UVIO + TSD fault
6	PWRON	R/W1C	1b	Power on
5	OVCC1	R/W1C	0b	VCC1 overvoltage
4	UVSUP5	R/W1C	0b	UVSUP5 undervoltage
3	UVSUP3	R/W1C	0b	UVSUP3 undervoltage
2	UVCC1	R/W1C	0b	VCC1 undervoltage
1	TSD_SBC	R/W1C	0b	SBC Thermal Shutdown due to VCC1 Or HSS (interrupt indicated after recovering from fail-safe mode)
0	SME	R/W1C	0b	Sleep Mode Exit interrupt when device is in sleep mode, VCC1 is on and exited to restart or fail-safe mode due to a VCC1 fault or watchdog fault if enabled

9.1.66 INT_3 Register (Address = 53h) [Reset = 00h]

INT_3 is shown in Table 9-68.

Return to the Summary Table.

Table 9-68. INT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR	R/W1C	0b	Sets when SPI status bit sets
6	SWERR	RH	0b	Logic OR of (SWE_EN and NOT (SWCFG)) and FRAME_OVF Selective wake may not be enabled while SWERR is set
5	FSM	R/W1C	0b	Entered fail-safe mode. Can be cleared while in FSM
4	CRCERR	R/W1C	0b	SPI transaction CRC error detected
3	VCC1SC	R/W1C	0b	VCC1 short detected
2	RSRT_CNT	R/W1C	0b	Restart counter exceeded programmed count
1	TSD_CAN	R/W1C	0b	Thermal Shutdown due to VCC2 or CAN
0	CRC_EEPROM	R/W1C	0b	EEPROM CRC error

9.1.67 INT_CANBUS_1 Register (Address = 54h) [Reset = 00h]

INT_CANBUS_1 is shown in Table 9-69.

Return to the Summary Table.

Table 9-69. INT_CANBUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UVCAN	R/W1C	0b	UVCAN interrupt
6	RESERVED	R	0b	Reserved
5	CANHCANL	R/W1C	0b	CANH and CANL shorted together
4	CANHBAT	R/W1C	0b	CANH shorted to Vbat
3	CANLGND	R/W1C	0b	CANL shorted to GND
2	CANBUSOPEN	R/W1C	0b	CAN bus open
1	CANBUSGND	R/W1C	0b	CAN bus shorted to GND or CANH shorted to GND
0	CANBUSBAT	R/W1C	0b	CAN bus shorted to Vbat or CANL shorted to Vbat

9.1.68 INT_7 Register (Address = 55h) [Reset = 00h]

INT_7 is shown in Table 9-70.

Return to the Summary Table.

Table 9-70. INT_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSSOC1	R/W1C	0b	High side switch 1 over current
6	HSSOL1	R/W1C	0b	High side switch 1 open load
5	HSSOC2	R/W1C	0b	High side switch 2 over current
4	HSSOL2	R/W1C	0b	High side switch 2 open load
3	HSSOC3	R/W1C	0b	High side switch 3 over current
2	HSSOL3	R/W1C	0b	High side switch 3 open load
1	HSSOC4	R/W1C	0b	High side switch 4 over current
0	HSSOL4	R/W1C	0b	High side switch 4 open load

9.1.69 INT_EN_1 Register (Address = 56h) [Reset = FFh]

INT_EN_1 is shown in Table 9-71.

Return to the Summary Table.

Table 9-71. INT_EN_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_EN	R/W	1b	Watchdog event detected mask
6	CANINT_EN	R/W	1b	CAN bus wake up interrupt mask
5	LWU_EN	R/W	1b	Local wake up mask
4	WKERR_EN	R/W	1b	Wake error mask
3	FRAME_OVF_EN	R/W	1b	Frame error counter overflow mask
2	CANSLNT_EN	R/W	1b	CAN silent mask
1	SWPIN_WU_EN	R/W	1b	SW pin wake up interrupt mask
0	CANDOM_EN	R/W	1b	CAN bus stuck dominant mask

9.1.70 INT_EN_2 Register (Address = 57h) [Reset = 7Fh]

INT_EN_2 is shown in Table 9-72.

Return to the Summary Table.

Table 9-72. INT_EN_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SMS_EN	R	0b	SMS flag enable (read-only)
6	PWRON_EN	R	1b	Power on flag enable (not changeable)
5	OVCC1_EN	R/W	1b	VCC1 overvoltage mask
4	UVSUP5_EN	R/W	1b	VSUP5 undervoltage mask
3	UVSUP3_EN	R/W	1b	UVSUP3 undervoltage mask
2	UVCC1_EN	R/W	1b	VCC1 undervoltage mask
1	TSD_SBC_EN	R/W	1b	Masking bit for interrupt due to SBC Thermal Shutdown
0	SME_EN	R	1b	SME interrupt enable (always enabled)

9.1.71 INT_EN_3 Register (Address = 58h) [Reset = FEh]

INT_EN_3 is shown in Table 9-73.

Return to the Summary Table.

Table 9-73. INT_EN_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR_EN	R/W	1b	SPI error interrupt mask
6	SWERR_EN	R/W	1b	Selective wake error mask
5	FSM_EN	R/W	1b	Fail-safe status flag mask
4	CRCERR_EN	R/W	1b	SPI CRC error interrupt mask
3	VCC1SC_EN	R/W	1b	VCC1 short circuit interrupt mask
2	RSRT_CNT_EN	R/W	1b	Restart counter exceeded programmed count mask
1	TSD_CAN_EN	R	1b	Masking bit for CAN/VCC2 thermal shutdown
0	RESERVED	R	0b	Reserved

9.1.72 INT_EN_CANBUS_1 Register (Address = 59h) [Reset = BFh]

INT_EN_CANBUS_1 is shown in Table 9-74.

Return to the Summary Table.

Table 9-74. INT_EN_CANBUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UVCAN_EN	R/W	1b	UVCAN interrupt mask
6	RESERVED	R	0b	Reserved
5	CANHCANL_EN	R/W	1b	Masking bit for CANH and CANL shorted together fault interrupt
4	CANHBAT_EN	R/W	1b	Masking bit for CANH shorted to Vbat fault interrupt
3	CANLGND_EN	R/W	1b	CANL shorted to GND enable
2	CANBUSOPEN_EN	R/W	1b	CAN bus open enable
1	CANBUSGND_EN	R/W	1b	CAN bus shorted to GND enable
0	CANBUSBAT_EN	R/W	1b	CAN bus shorted to Vbat enable

9.1.73 INT_4 Register (Address = 5Ah) [Reset = 00h]

INT_4 is shown in Table 9-75.

Return to the Summary Table.

Table 9-75. INT_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	RESERVED	R	0b	Reserved
5	RESERVED	R	0b	Reserved
4	CYC_WUP	R/W1C	0b	Cyclic wake interrupt via internal timer
3	MODE_ERR	R/W1C	0b	Illegal transceiver state for mode change request
2	OVHSS	R/W1C	0b	VHSS over-voltage for high-side switches
1	EEPROM_CRC_INT	R/W1C	0b	EEPROM CRC check fail
0	UVHSS	R/W1C	0b	VHSS under-voltage for high-side switches

9.1.74 INT_6 Register (Address = 5Ch) [Reset = 00h]

INT_6 is shown in Table 9-76.

Return to the Summary Table.

Table 9-76. INT_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TSDW	R/W1C	0b	Thermal shutdown warning
6	UVCC1PW	R/W1C	0b	VCC1 undervoltage pre-warning
5	RESERVED	R	0b	Reserved
4	RESERVED	R	0b	Reserved
3	RESERVED	R	0b	Reserved
2	UVCC2	R/W1C	0b	VCC2 pin undervoltage
1	OVCC2	R/W1C	0b	VCC2 pin overvoltage
0	VCC2SC	R/W1C	0b	VCC2 pin short circuit

9.1.75 INT_EN_4 Register (Address = 5Eh) [Reset = 1Fh]

INT_EN_4 is shown in Table 9-77.

Return to the Summary Table.

Table 9-77. INT_EN_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	RESERVED	R	0b	Reserved
5	RESERVED	R	0b	Reserved
4	CYC_WUP_EN	R/W	1b	Masking bit for cyclic wake interrupt
3	MODE_ERR_EN	R/W	1b	Illegal transceiver state for mode change request mask
2	OVHSS_EN	R/W	1b	VHSS over-voltage for high-side switches mask
1	EEPROM_CRC_INT_EN	R/W	1b	EEPROM CRC check fail mask
0	UVHSS_EN	R/W	1b	VHSS under-voltage for high-side switches mask

9.1.76 INT_EN_6 Register (Address = 60h) [Reset = C7h]

INT_EN_6 is shown in Table 9-78.

Return to the Summary Table.

Table 9-78. INT_EN_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TSDW_EN	R/W1C	1b	Thermal shutdown warning mask
6	UVCC1PW_EN	R/W1C	1b	VCC1 undervoltage pre-warning mask
5	RESERVED	R	0b	Reserved
4	RESERVED	R	0b	Reserved
3	RESERVED	R	0b	Reserved
2	UVCC2_EN	R/W	1b	VCC2 pin undervoltage mask
1	OVCC2_EN	R/W	1b	VCC2 pin overvoltage mask
0	VCC2SC_EN	R/W	1b	VCC2 pin short circuit mask

9.1.77 INT_EN_7 Register (Address = 62h) [Reset = FFh]

INT_EN_7 is shown in Table 9-79.

Return to the Summary Table.

Table 9-79. INT_EN_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSSOC1_EN	R/W	1b	High side switch 1 over current interrupt mask
6	HSSOL1_EN	R/W	1b	High side switch 1 open load interrupt mask
5	HSSOC2_EN	R/W	1b	High side switch 2 over current interrupt mask
4	HSSOL2_EN	R/W	1b	High side switch 2 open load interrupt mask
3	HSSOC3_EN	R/W	1b	High side switch 3 over current interrupt mask
2	HSSOL3_EN	R/W	1b	High side switch 3 open load interrupt mask
1	HSSOC4_EN	R/W	1b	High side switch 4 over current interrupt mask
0	HSSOL4_EN	R/W	1b	High side switch 4 open load interrupt mask

9.1.78 BUCK_CONFIG1 Register (Address = 65h) [Reset = 28h]

BUCK_CONFIG1 is shown in Table 9-80.

Return to the Summary Table.

Table 9-80. BUCK_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SS_MOD_FREQ (REV_ID = 21h)	R/W	00b	REV_ID: 21h Spread Spectrum Modulation frequency spread options. NOTE: These bits are available only with REV_ID = 21h (silicon revision 2.1). NOTE: Switching frequency of 1.8MHz with Spread Spectrum enabled can create emissions in the AM band. Recommended to use 4% delta fc modulation option to minimize interference in the AM band 00b = Off 01b = 4% delta fc 10b = 8% delta fc 11b = Reserved
7-6	RSVD (REV_ID = 20h)	R/W	00b	REV_ID: 20h RESERVED
5-4	BUCK_FSW	R/W	10b	Buck regulator switching frequency setting 00b = 1.8MHz 01b = 2.0MHz 10b = 2.2MHz 11b = 2.4MHz
3	PWM_PFM_CNTL_NORMAL	R/W	1b	PFM and PWM Mode Configuration in Normal mode 0b = Auto (Automatic transition between PFM and PWM mode) 1b = PWM
2	PWM_PFM_CNTL_STDBY_SLP	R/W	0b	PFM and PWM Mode Configuration in Standby/Sleep mode 0b = Auto (Automatic transition between PFM and PWM mode) 1b = PWM
1	RSVD (REV_ID = 20h)	R/W	0b	REV_ID: 20h Reserved bit when REV_ID is 20h (Silicon revision 2.0). Note: Do not set this bit in ES_2.0
1	PRSS_EN (REV_ID = 21h)	R/W	0b	REV_ID: 21h Enables the Pseudo Random Spread Spectrum (PRSS) NOTE: This bit is available only with REV_ID = 21h (Silicon rev 2.1) 0b = Linear Spread Spectrum 1b = Pseudo Random Spread Spectrum
0	ICC1_CUR_LIMIT	R/W	0b	Current limit threshold for the buck regulator 0b = High threshold (1A load) 1b = Low threshold (500mA load)

9.1.79 ID_PIN_STATUS Register (Address = 78h) [Reset = 00h]

ID_PIN_STATUS is shown in Table 9-81.

Return to the Summary Table.

Table 9-81. ID_PIN_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ID4_STAT	R/W0C	00b	Status of the ID4 pin connection Note: If WAKE_ID4_PU_PD register bit is set to 01b (pulldown) or 10b (pull-up), the status bits resets to 00b. WAKE4_STAT bit reflects the real time pin logic of ID4 pin in such a case. 00b = Unknown 01b = Connected to GND 10b = Connected to VSUP 11b = Floating
5-4	ID3_STAT	R/W0C	00b	Status of the ID3 pin connection Note: If WAKE_ID3_PU_PD register bit is set to 01b (pulldown) or 10b (pull-up), the status bits resets to 00b. WAKE3_STAT bit reflects the real time pin logic of ID3 pin in such a case. 00b = Unknown 01b = Connected to GND 10b = Connected to VSUP 11b = Floating
3-2	ID2_STAT	R/W0C	00b	Status of the ID2 pin connection Note: If WAKE_ID2_PU_PD register bit is set to 01b (pulldown) or 10b (pull-up), the status bits resets to 00b. WAKE2_STAT bit reflects the real time pin logic of ID2 pin in such a case. 00b = Unknown 01b = Connected to GND 10b = Connected to VSUP 11b = Floating
1-0	ID1_STAT	R/W0C	00b	Status of the ID1 pin connection Note: If WAKE_ID1_PU_PD register bit is set to 01b (pulldown) or 10b (pull-up), the status bits resets to 00b. WAKE1_STAT bit reflects the real time pin logic of ID1 pin in such a case. 00b = Unknown 01b = Connected to GND 10b = Connected to VSUP 11b = Floating

9.1.80 WAKE_ID_CONFIG1 Register (Address = 79h) [Reset = 66h]

WAKE_ID_CONFIG1 is shown in Table 9-82.

Return to the Summary Table.

Table 9-82. WAKE_ID_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ID2_EN	R/W	0b	Enables/disables ID2 functionality Note: If both ID2_EN and WAKE2_PIN_SET are set to 1b, the device ignores WAKE2_PIN_SET setting and the ID function enables at the WAKE2/ID2 pin 0b = ID2 pin disabled 1b = ID2 pin enabled
6-5	WAKE_ID2_PU_PD	R/W	11b	ID2 configuration for pull-up, pull-down, automatic or disabled Note: Only the Automatic selection (11b) updates the ID2_STAT register bit 00b = Neither pull-up nor pull-down activated 01b = Pull-down activated 10b = Pull-up activated 11b = Automatic selection of pull-up/pull-down
4	ID2_PD_VALUE	R	0b	ID2 pin pull-down current strength setting 0b = 3mA 1b = 10mA
3	ID1_EN	R/W	0b	Enables/disables ID1 functionality Note: If both ID1_EN and WAKE1_PIN_SET are set to 1b, the device ignores WAKE1_PIN_SET setting and the ID function enables at the WAKE1/ID1 pin 0b = ID1 pin disabled 1b = ID1 pin enabled
2-1	WAKE_ID1_PU_PD	R/W	11b	ID1 configuration for pull-up, pull-down, automatic or disabled Note: Only the Automatic selection (11b) updates the ID1_STAT register bit 00b = Neither pull-up nor pull-down activated 01b = Pull-down activated 10b = Pull-up activated 11b = Automatic selection of pull-up/pull-down
0	ID1_PD_VALUE	R	0b	ID1 pin pull-down current strength setting 0b = 3mA 1b = 10mA

9.1.81 WAKE_ID_CONFIG2 Register (Address = 7Ah) [Reset = 66h]

WAKE_ID_CONFIG2 is shown in Table 9-83.

Return to the Summary Table.

Table 9-83. WAKE_ID_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ID4_EN	R/W	0b	Enables/disables ID4 functionality Note: If both ID4_EN and WAKE4_PIN_SET are set to 1b, the device ignores WAKE4_PIN_SET setting and the ID function enables at the WAKE4/ID4 pin 0b = ID4 pin disabled 1b = ID4 pin enabled
6-5	WAKE_ID4_PU_PD	R/W	11b	ID4 configuration for pull-up, pull-down, automatic or disabled Note: Only the Automatic selection (11b) updates the ID4_STAT register bit 00b = Neither pull-up nor pull-down activated 01b = Pull-down activated 10b = Pull-up activated 11b = Automatic selection of pull-up/pull-down
4	ID4_PD_VALUE	R	0b	ID4 pin pull-down current strength setting 0b = 3mA 1b = 10mA
3	ID3_EN	R/W	0b	Enables/disables ID3 functionality Note: If both ID3_EN and WAKE3_PIN_SET are set to 1b, the device ignores WAKE3_PIN_SET setting and the ID function enables at the WAKE3/ID3 pin 0b = ID3 pin disabled 1b = ID3 pin enabled
2-1	WAKE_ID3_PU_PD	R/W	11b	ID3 configuration for pull-up, pull-down, automatic or disabled Note: Only the Automatic selection (11b) updates the ID3_STAT register bit 00b = Neither pull-up nor pull-down activated 01b = Pull-down activated 10b = Pull-up activated 11b = Automatic selection of pull-up/pull-down
0	ID3_PD_VALUE	R	0b	ID3 pin pull-down current strength setting 0b = 3mA 1b = 10mA

9.1.82 WAKE_PIN_CONFIG5 Register (Address = 7Bh) [Reset = 20h]

WAKE_PIN_CONFIG5 is shown in Table 9-84.

Return to the Summary Table.

Table 9-84. WAKE_PIN_CONFIG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE4_SENSE	R/W	0b	WAKE4 pin configured for static or cyclic sensing wake 0b = Static sensing 1b = Cyclic sensing
6	WAKE4_STAT	RH	0b	Provides status of WAKE4 pin. 0b = Low 1b = High
5-4	WAKE4_LEVEL	R/W	10b	Sets the WAKE4 pin input thresholds 00b = VCC1 based 01b = 2.5V 10b = 4V 11b = 6V
3-0	RESERVED	R	0b	Reserved

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TCAN245x-Q1 family supports CAN FD communication.

10.1.1 CAN BUS Loading, Length and Number of Nodes

The ISO11898-2:2024 standard specifies a maximum bus length of 40m and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes require a transceiver with high input impedance such as this transceiver family.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898-2:2024 standard. The CAN organizers made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC825, CANopen, DeviceNet, SAEJ2284, SAEJ1939, and NMEA200.

A CAN network system design is a series of tradeoffs. In ISO11898-2 the driver differential output is specified with a 60Ω bus load (the two termination resistors in parallel) where the differential output must be greater than 1. V. The TCAN245x-Q1 is specified to meet the 1.5V requirement with a across this load range and is specified to meet 1.4V differential output at 45Ω bus load. The differential input resistance of this family of transceiver is a minimum of 30kΩ. If 167 of these transceivers are in parallel on a bus, this is equivalent to an 180Ω differential load in parallel with the 60Ω from termination gives a total bus load of 45Ω. Therefore, this family theoretically supports over 167 transceivers on a single bus segment with margin to the 1.2V minimum differential input voltage requirement at each receiving node. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is much lower. Bus length may also be extended beyond the original ISO11898-2:2024 standard of 40m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of its key strengths allowing for these system level network extensions and additional standards to build on the original ISO11898-2 CAN standard. However, when using this flexibility, the CAN network system designer must take the responsibility of good network design to make sure robust network operation.

10.1.2 CAN Termination

The ISO11898-2:2024 standard specifies the interconnection to be a single twisted pair cable (shielded or unshielded) with 120Ω characteristic impedance (Z_O).

10.1.2.1 CAN Bus Biasing

Bus biasing can be normal biasing, active in normal mode and inactive in low-power mode. Automatic voltage biasing is where the bus is active in normal mode but is controlled by the voltage between CANH and CANL in lower power modes. See Figure 10-1 for the state diagram on how the TCAN245x-Q1 performs automatic biasing.

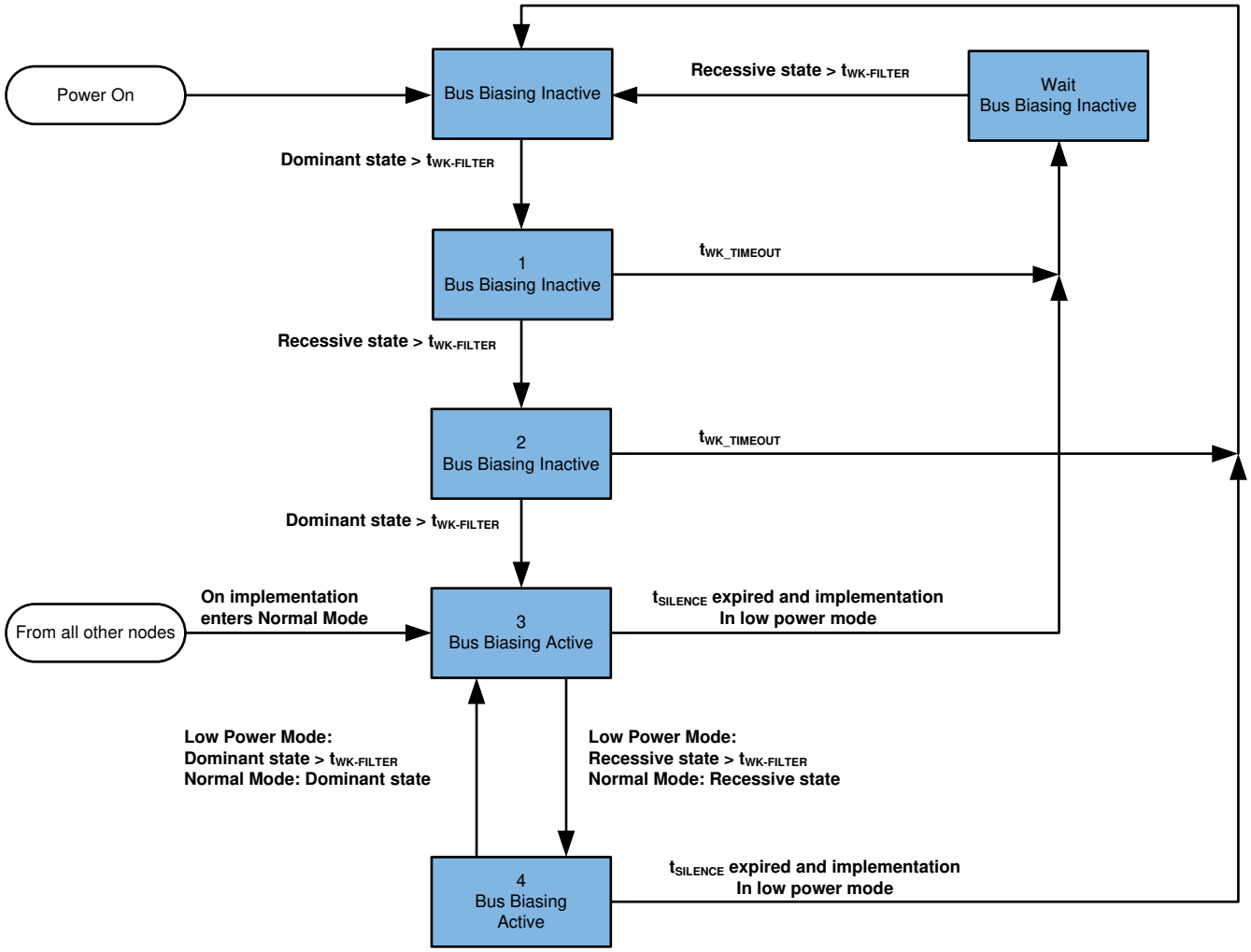
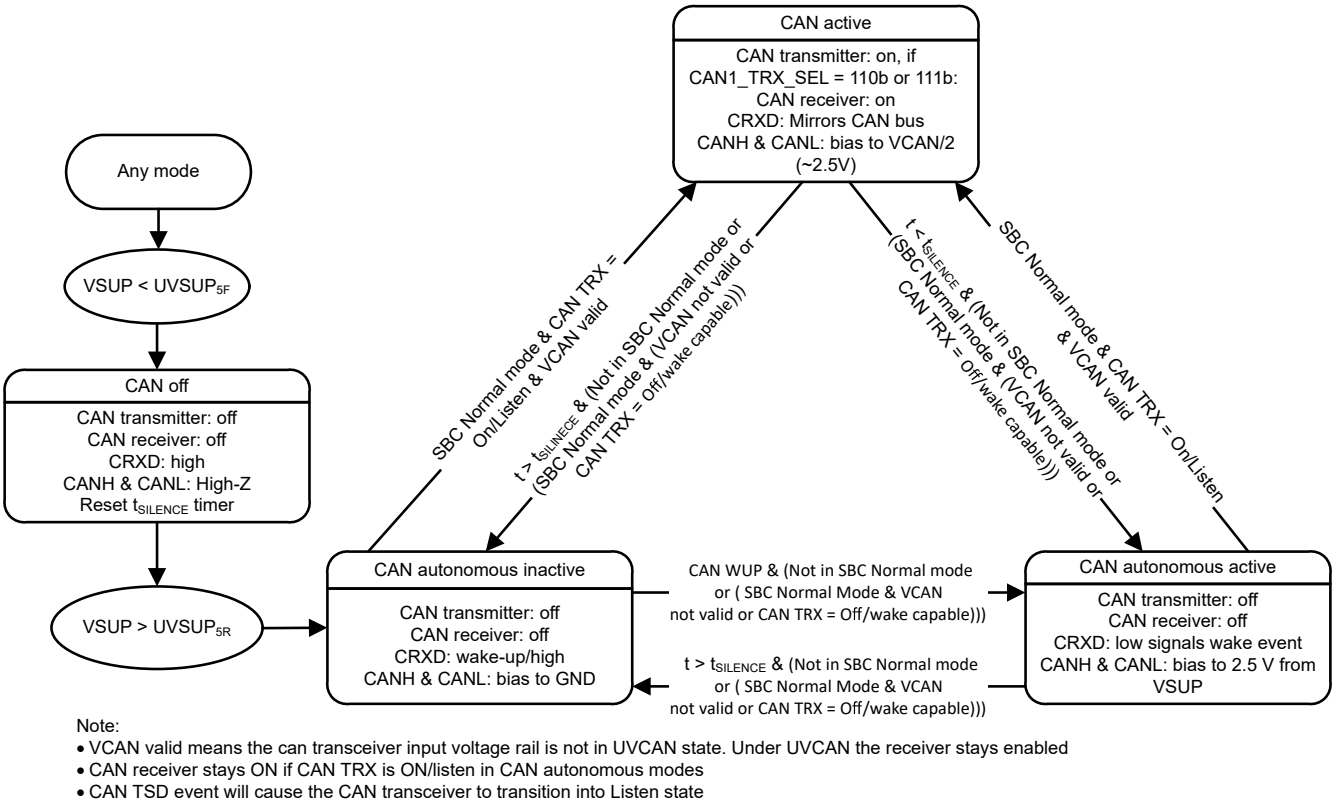


Figure 10-1. Automatic bus biasing state diagram



Note:
- VCAN valid means the can transceiver input voltage rail is not in UVCAN state. Under UVCAN the receiver stays enabled
- CAN receiver stays ON if CAN TRX is ON/listen in CAN autonomous modes
- CAN TSD event will cause the CAN transceiver to transition into Listen state

Figure 10-2. Bus biasing

10.1.3 Device Brownout Information

The brownout behavior of the TCAN245x-Q1 depends upon the VCC1 setting, and whether or not VSUP drops below $VSUP_{(PU)F}$. When VCC1 = 5V, the device behaves as per Figure 10-3. When VSUP continues to fall below $VSUP_{(PU)F}$, the devices enters power on reset as shown in Figure 10-4.

When VCC1 = 3.3V, the device behaves as per Figure 10-5 when VSUP falls below $UVSUP_{33F}$, but stays above $VSUP_{(PU)F}$. When VSUP continues to fall below $VSUP_{(PU)F}$, the devices enters power on reset as shown in Figure 10-6.

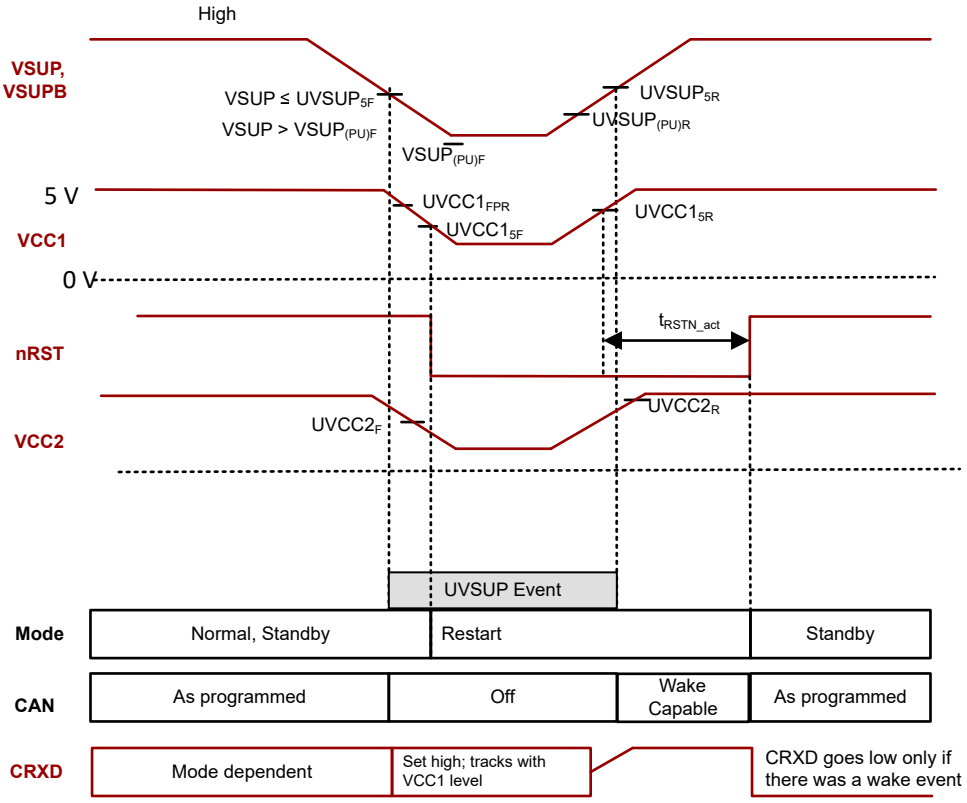


Figure 10-3. Brownout Above $VSUP_{(PU)F}$ for VCC1 = 5V

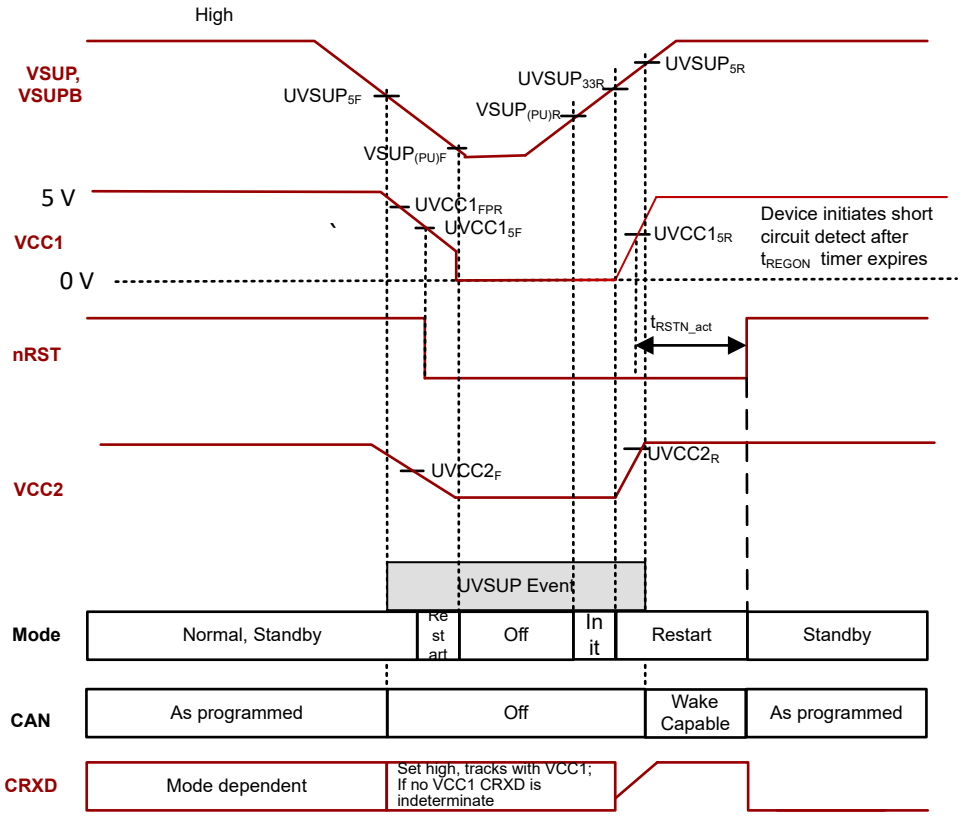


Figure 10-4. Brownout Below $VSUP_{(PU)F}$

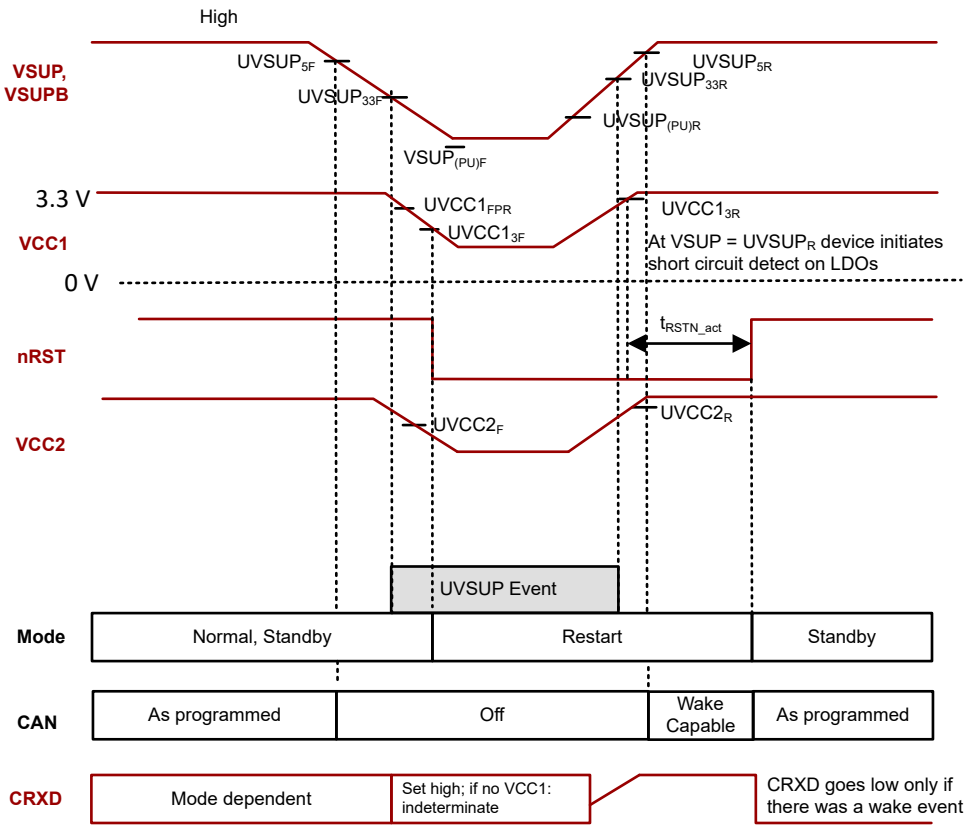


Figure 10-5. Brownout Above $VSUP_{(PU)F}$ for VCC1= 3.3V

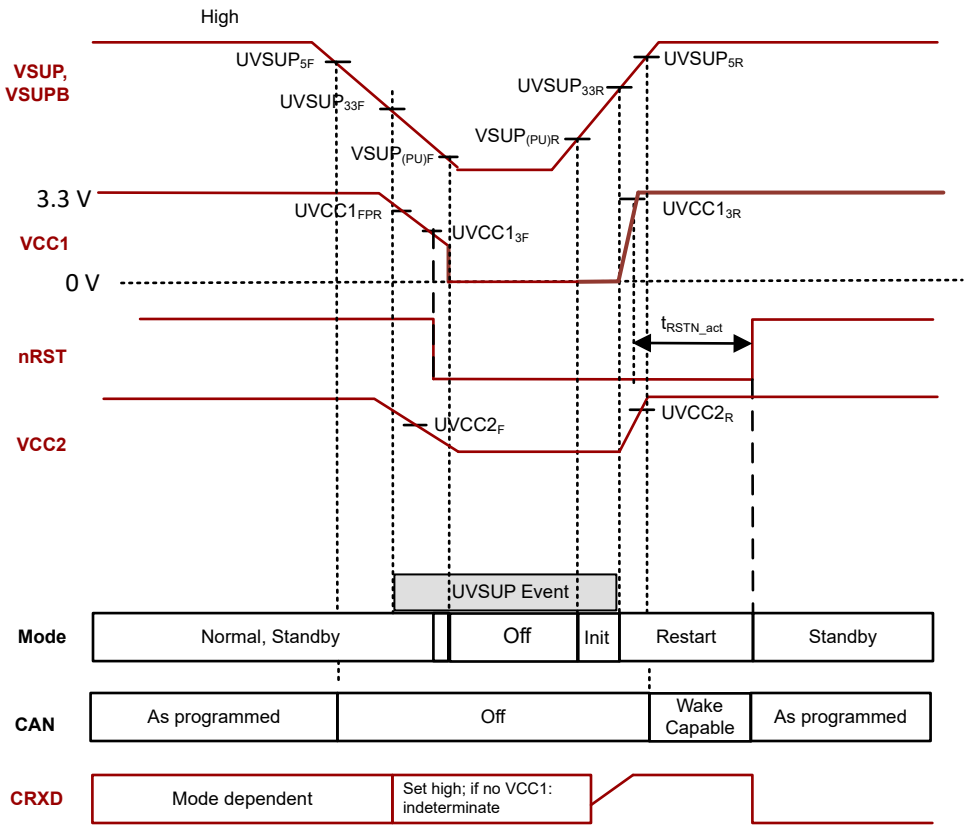


Figure 10-6. Brownout Below $VSUP_{(PU)F}$ for VCC1 = 3.3V

10.2 Typical Application

The TCAN245x-Q1 SBC family is typically used in applications with a host microprocessor or FPGA that requires CAN FD support while using many of the device features like the watchdog, advanced bus fault diagnostics for CAN FD bus and high side switches. The following typical application configuration is for 3.3V microprocessor applications. These devices work with 3.3V and 5V microprocessors depending upon the value of VCC1. The bus termination is shown for illustrative purposes.

Figure 10-7 shows the TCAN245x-Q1 configured to support Cyclic sensing on WAKE pin and the high side switch controlling the LED. The buck regulator supports applications that need currents up to 1A.

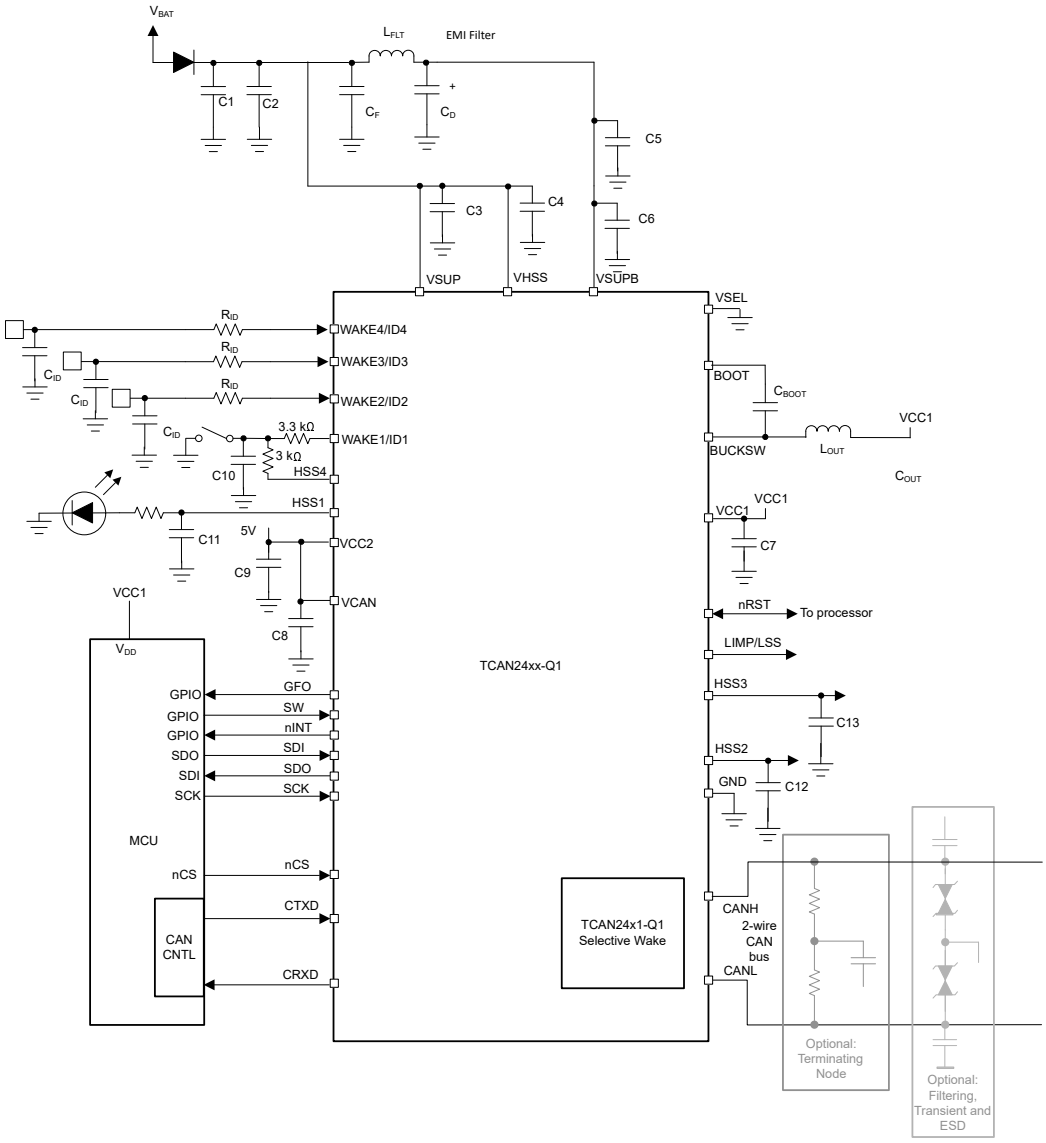


Figure 10-7. Typical CAN Application for TCAN245x-Q1

Table 10-1. Recommended External Component Values

Component	Value	Comments
C1	100nF	High frequency spike filtering capacitance. Needed for EMC robustness.
C2	22 µF	Decoupling capacitance to cut-off battery spike, protect from ISO pulses. May need higher capacitance per application requirements.
C3	100nF	High frequency spike filtering capacitance. Needed for EMC robustness. Place close to the pin of the device.
C4	100nF	High frequency spike filtering capacitance. Needed for EMC robustness. Place close to the pin of the device.
L_{FLT}	1.5µH	Filter inductance for the pi-filter
C_F	2.2µF	EMI pi-filter capacitance
C_D	47µF	Needs to be at least 4 times C5 (buck supply input capacitance). Damping capacitor for the pi-filter. Bulk capacitor recommended due to the need for the damping resistance.
C5	10µF	Low ESR input capacitance for the buck supply input. Adjust as needed for the application. Note: This is the capacitance value used for EMC certification with 0.8A load on VCC1.
C6	100nF	Low ESR, high frequency spike filtering capacitance. Needed for EMC robustness. Place close to the pin of the device.
L_{OUT}	3.3µH for VCC1 = 3.3V	Typical recommended value for the buck output filter inductor.
	4.7µH for VCC1 = 5V	
C_{OUT}	Min. 10µF	10V rated. Buck output filter inductor. Higher capacitor value can be chosen to account for lifetime/temp derating, and to handle load transient.
C_{BOOT}	100nF	10V rated. Boot capacitor
C8	100nF	High frequency spike filtering capacitance. Needed for EMC robustness. Place close to the pin of the device.
C9	4.7µF	VCC2 LDO output capacitor. EMC certification tests done with X7R/50V capacitor of this value.
C10	22nF	Low ESR capacitor needed for EMC robustness.
C11, C12, C13	100nF	Needed only if the HSS is driving external loads, for EMC robustness.
C_{ID}	22nF	Low ESR capacitor needed for EMC robustness.
R_{ID}	510Ω	Needed for ID pin protection from ground shift/ground loss and EMC robustness.

10.2.1 Design Requirements

The ISO 11898-2_2024 Standard specifies a maximum bus length of 40m and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the TCAN245x-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2_2024. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. The device is specified to meet the 1.5V requirement with a 50Ω load, incorporating the worst case including parallel transceivers.

The differential input resistance of the device is a minimum of 30kΩ. If 100 of the devices are in parallel on a bus, this is equivalent to a 300Ω differential load worst case. That transceiver load of 300Ω in parallel with the 60Ω gives an equivalent loading of 50Ω. Therefore, the device theoretically supports up to 100 transceivers on a single bus segment.

However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity. Thus, a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO 11898-2_2024 standard of 40m by careful system design and data rate tradeoffs.

For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate. This flexibility in CAN

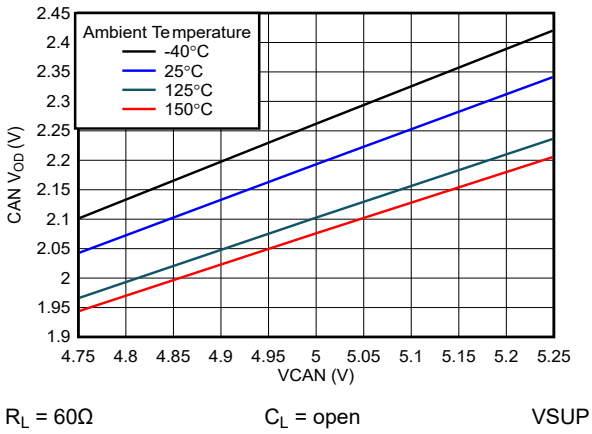
network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2_2024 CAN standard. Using this flexibility comes with the responsibility of a good network design, and balancing these tradeoffs.

10.2.2 Detailed Design Procedures

10.2.2.1 CAN Detailed Design Procedure

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120Ω characteristic impedance (Z_O). Use resistors equal to the characteristic impedance of the line to terminate both ends of the cable to prevent signal reflections. Keep unterminated drop lines (stubs) connecting nodes to the bus as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but nodes may be removed from the bus, the termination must be carefully placed so that two terminations always exist on the network. Termination may be a single 120Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

10.2.3 Application Curves



R_L = 60Ω C_L = open VSUP = 14V

Figure 10-8. CAN Driver Differential Output ($V_{DIFF(D)}$) in Dominant Mode

10.3 Power Supply Recommendations

The TCAN245x-Q1 is designed to operate off of the battery (to supply to VSUP, VSUPB and VHSS) and VCAN. To support a wide range of microprocessors the logic I/O and SPI are powered off of VCC1 which supports levels 3.3V and 5V. The CAN FD transceiver 5V supply is powered from VCAN input. As VCAN is used for the CAN transceiver and needed for EEPROM writes, do not use VCC2 to supply VCAN if VCC2 is providing power off the board. Please refer to the typical application diagram for the recommended values of external components needed for the supply input and output terminals.

10.4 Layout

Robust and reliable CAN node design can require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, apply high-frequency layout techniques during PCB design.

10.4.1 Layout Guidelines

Place the protection and filtering circuitry as close to the bus connector, to prevent transients, ESD and noise from propagating onto the board. The layout example provides information on components around the device. Add a transient voltage suppression (TVS) device for extra protection. A series common mode choke (CMC) is placed on the CANH and CANL lines between and connector.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Use supply and ground planes to provide low inductance.

Note

High-frequency currents follows the path of least impedance and not the path of least resistance.

- Verify that high-frequency filtering capacitors, typically 100nF, are placed as close as possible to the supply terminals of the device. Establish that this capacitor is low ESR.
- Input and output supply capacitors, C_{IN} and $C_{VCC2,}$ can be low ESR, and must be close to the supply terminal pins.
- VSUPB is the supply input to the switching FETs of the buck regulator; and therefore, are separated from VSUP and VHSS by a pi-filter as shown.
- The routing resistance must be minimized from the VCC1 output capacitor to the VCC1 pin of the TCAN245x-Q1. The internal circuits of the digital pins of the TCAN245x-Q1 are powered by the VCC1 pin; therefore, any excessive resistance in this path can cause problems with VCC1 regulation.
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R_{TERM}, with the center or split tap of the termination connected to ground via capacitor C_{SPLIT}. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to make sure the terminating node is not removed from the bus; thus, removing the termination.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

10.4.2 Layout Example

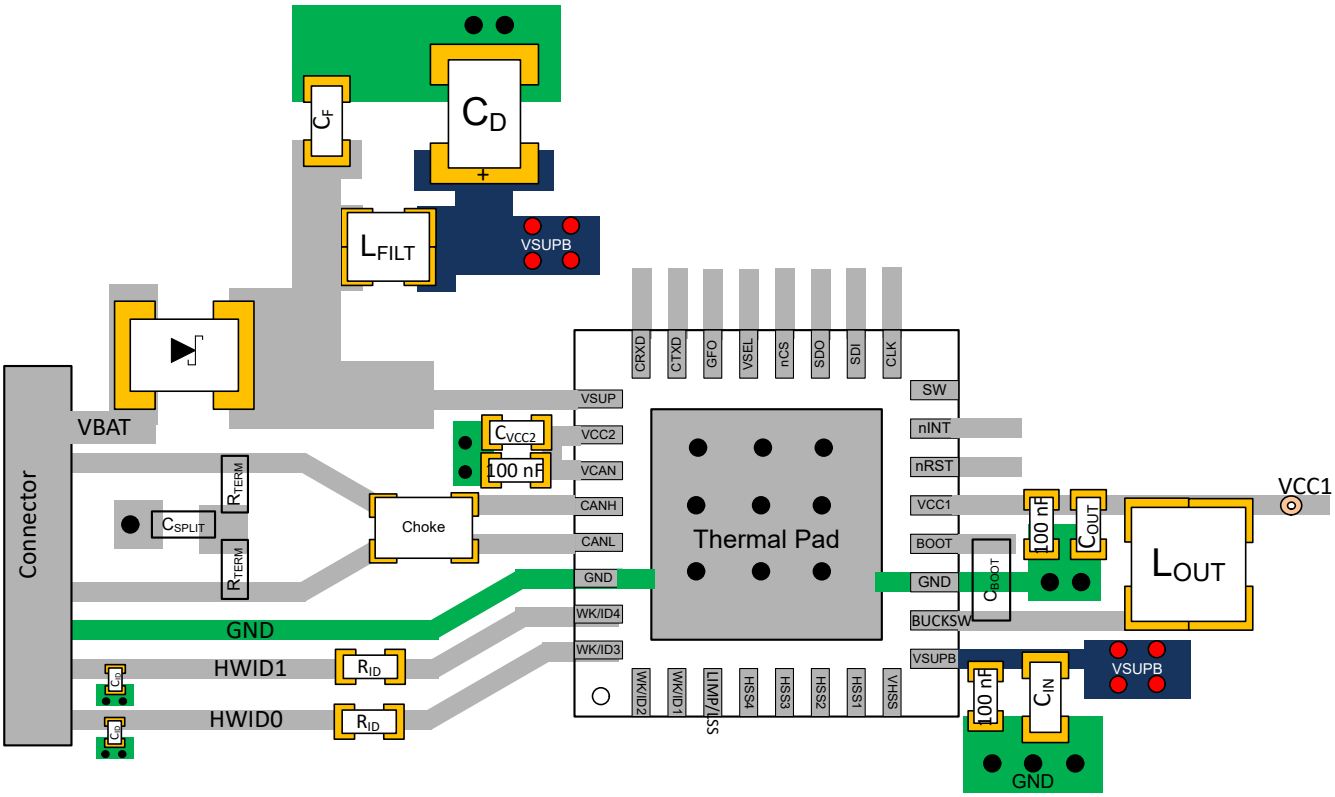


Figure 10-9. Example Layout

11 Device and Documentation Support

This device conforms to the following CAN standards. The core of what is needed is covered within this system spec, however reference should be made to these standards and any discrepancies pointed out and discussed. This document should provide all the basics of what is needed. However, for a full understanding of CAN including the protocol these additional sources is very helpful as the scope of CAN protocol in detail is outside the scope of this physical layer (transceiver) specification.

11.1 Documentation Support

11.1.1 CAN Transceiver Physical Layer Standards:

- ISO 11898-2:2024: High speed medium access unit with low power mode (super sets -2 standard electrically in several specs and adds the original wake up capability via the bus in low power mode)
- ISO 8802-3: CSMA/CD – referenced for collision detection from ISO11898-2
- SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250kbps
- SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500kbps

11.1.2 EMC Requirements:

- CISPR25
- HW Requirements for CAN, LIN, FR V1.3: German OEM requirements for CAN and LIN
- IEC 61000-4-2
- IEC 61967-4
- IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150kHz to 1GHz - Part 4: Direct RF power injection method
- ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
- ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
- ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
- ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
- SAEJ2962-2: US3 requirements for CAN Transceivers (-2, -5, GM proposes updates to address -6 + FD, but this is the best place for a working start)

11.1.3 Conformance Test Requirements:

- HS_TRX_Test_Spec_V_1_0: GIFT / ICT CAN test requirements for High Speed Physical Layer
- ISO/DIS 17987-7.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
- SAEJ2602-2: LIN Network for Vehicle Applications Conformance Test

11.1.4 Related Documentation

- Wilfried Voss, Copperhill Technologies, *A Comprehensible Guide to Controller Area Network* book
- Dr. Wolfhard Lawrenz, Springer, *CAN System Engineering: From Theory to Practical Applications*, book, 2nd edition, 2013

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2025) to Revision C (October 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• First public release of the device	1
• Added Functional Safety Quality-Managed rating	1
• Added the TCAN2450-Q1 and TCAN2451-Q1 Diagrams	1
• Removed the DCP package from the Thermal Information Table	9
• Updated and clarified the test condition for VSYM and added a note that VSYM is specified by design and characterization	14
• Relaxed the VIH minimum and maximum specification (setting 10b) for TCAN245xMRHBRQ1	14
• Relaxed the VIL minimum specification (setting 11b) for TCAN245xMRHBRQ1	14
• Tightened the ID_{PD} maximum specification from 5.5mA to 5mA for TCAN245xMRHBRQ1 variants	14
• Updated formatting in Driver Function Table	38
• Updated the reset values of registers 8h (REV_ID) to 2Xh to indicate that both 20h or 21h are valid reset values depending upon the silicon revision	113

Changes from Revision A (April 2024) to Revision B (June 2025)	Page
• Changed the document status from *Advanced Information* to *Production* data	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN2450MRHBRQ1	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TCAN 2450M
TCAN2450RHBRQ1	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TCAN 2450
TCAN2450RHBRQ1.A	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TCAN 2450
TCAN2451MRHBRQ1	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TCAN 2451M
TCAN2451RHBRQ1	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TCAN 2451

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

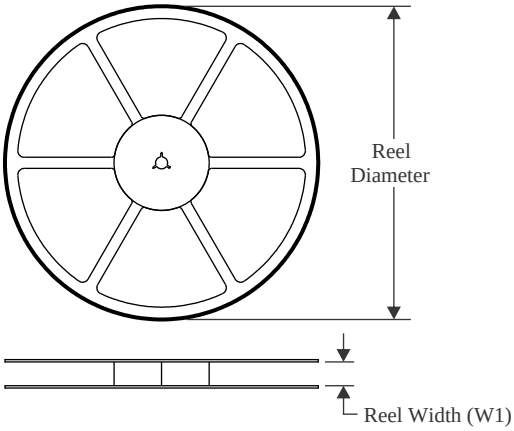
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

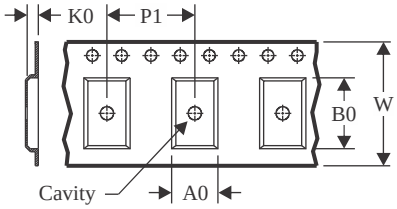
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

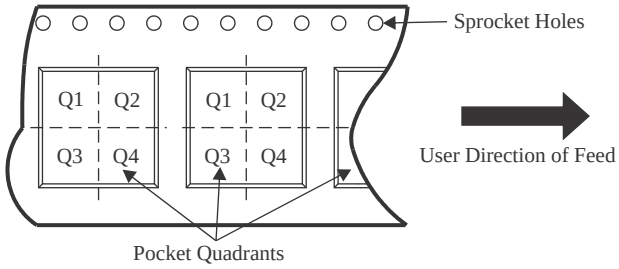


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

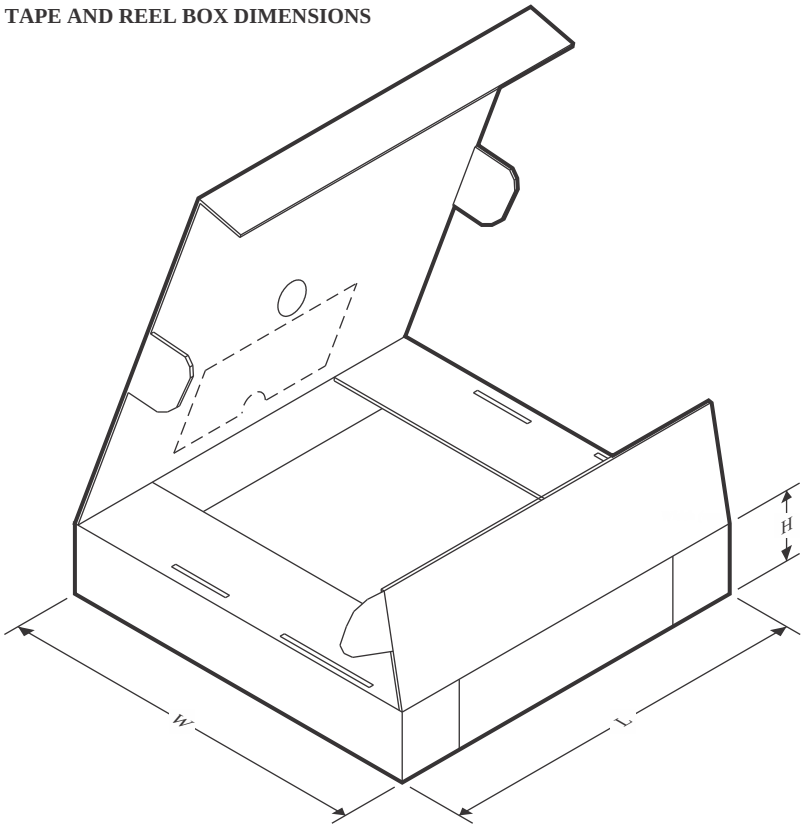
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN2450MRHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TCAN2450MRHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TCAN2450RHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TCAN2451MRHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TCAN2451MRHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TCAN2451RHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN2450MRHBRQ1	VQFN	RHB	32	5000	346.0	346.0	33.0
TCAN2450MRHBRQ1	VQFN	RHB	32	5000	360.0	360.0	36.0
TCAN2450RHBRQ1	VQFN	RHB	32	5000	367.0	367.0	35.0
TCAN2451MRHBRQ1	VQFN	RHB	32	5000	360.0	360.0	36.0
TCAN2451MRHBRQ1	VQFN	RHB	32	5000	346.0	346.0	33.0
TCAN2451RHBRQ1	VQFN	RHB	32	5000	367.0	367.0	35.0

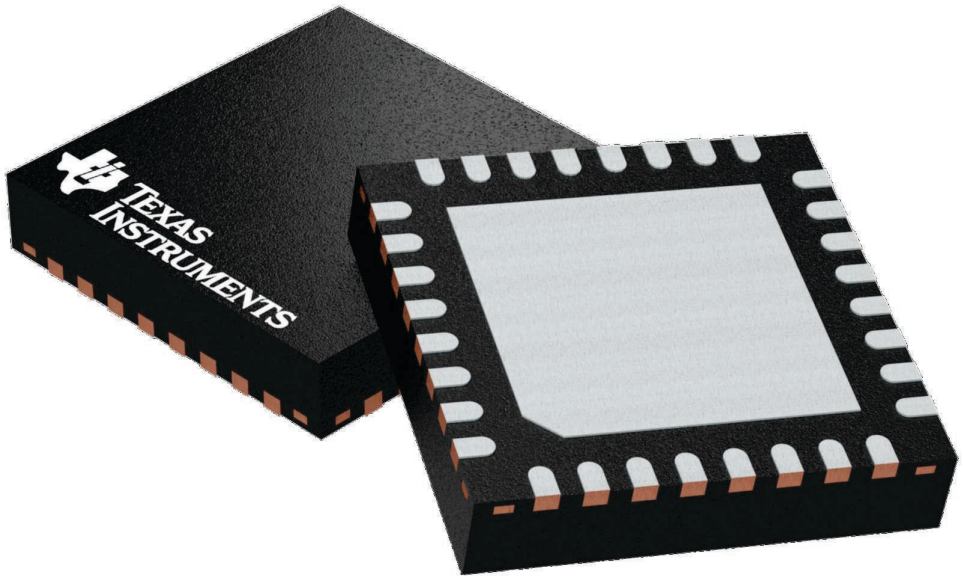
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

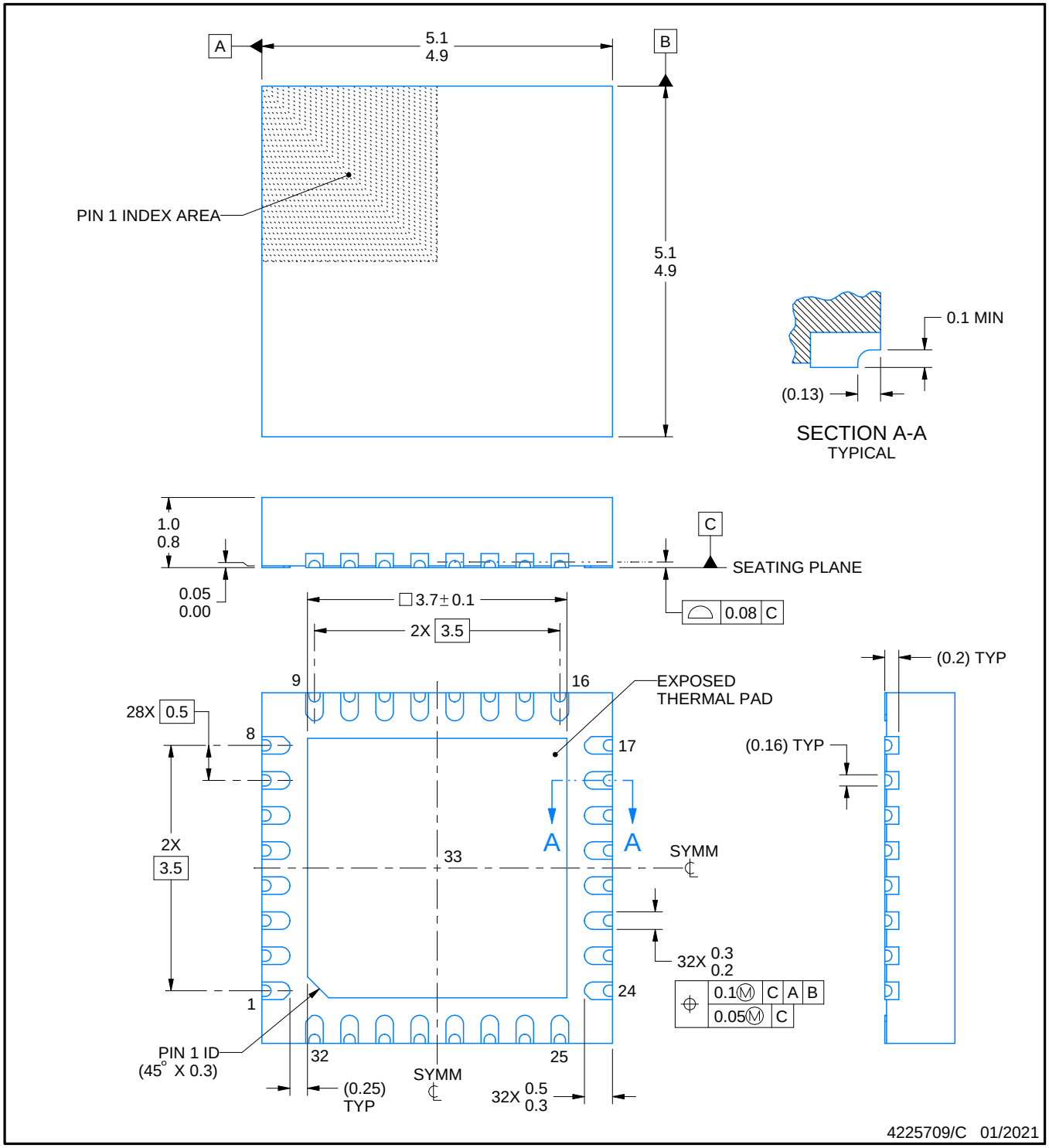
4224745/A

RHB0032U

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

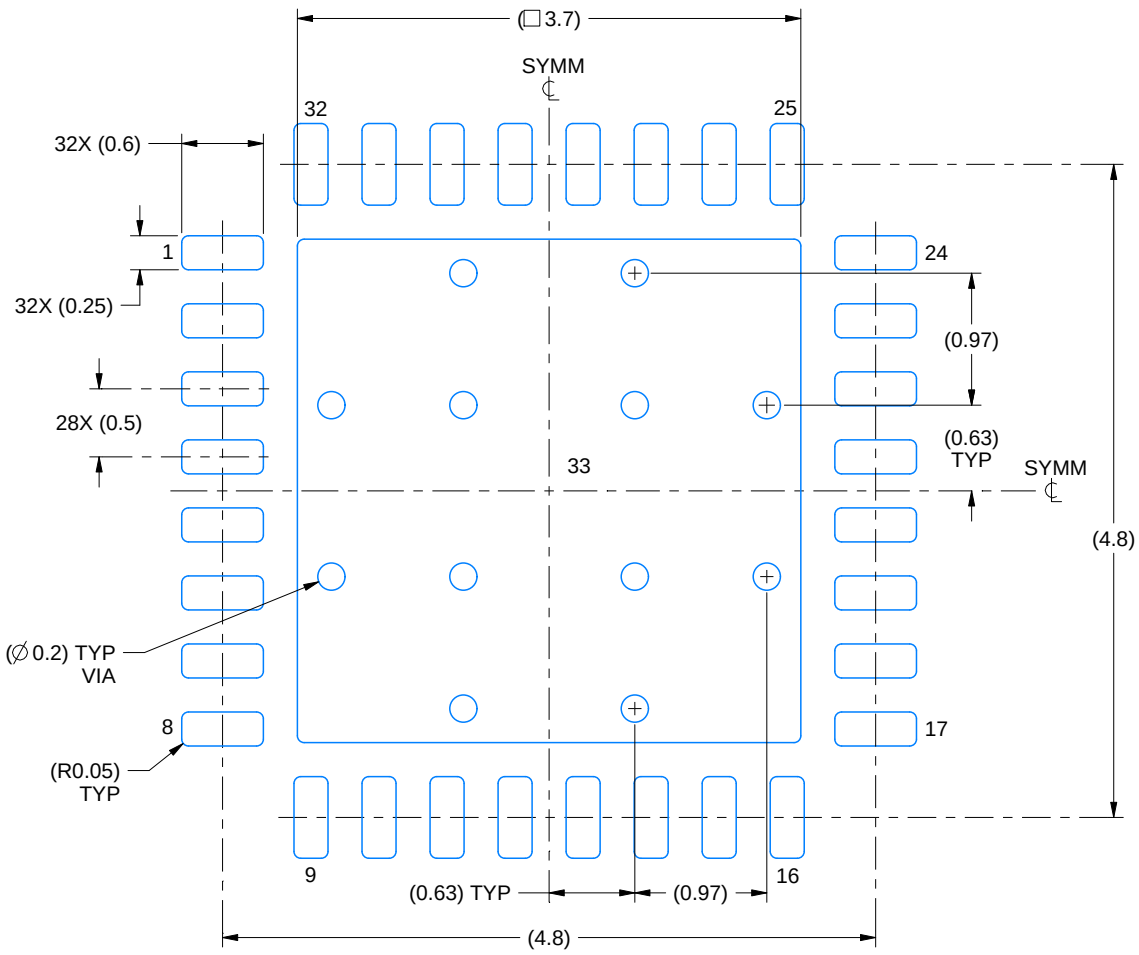
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

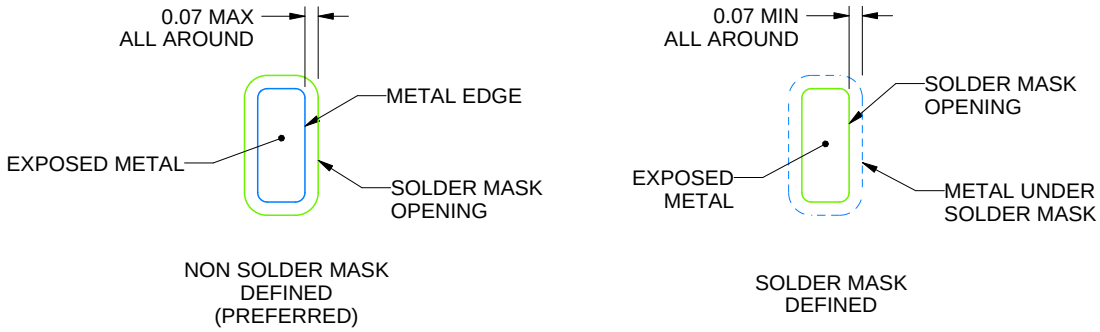
RHB0032U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

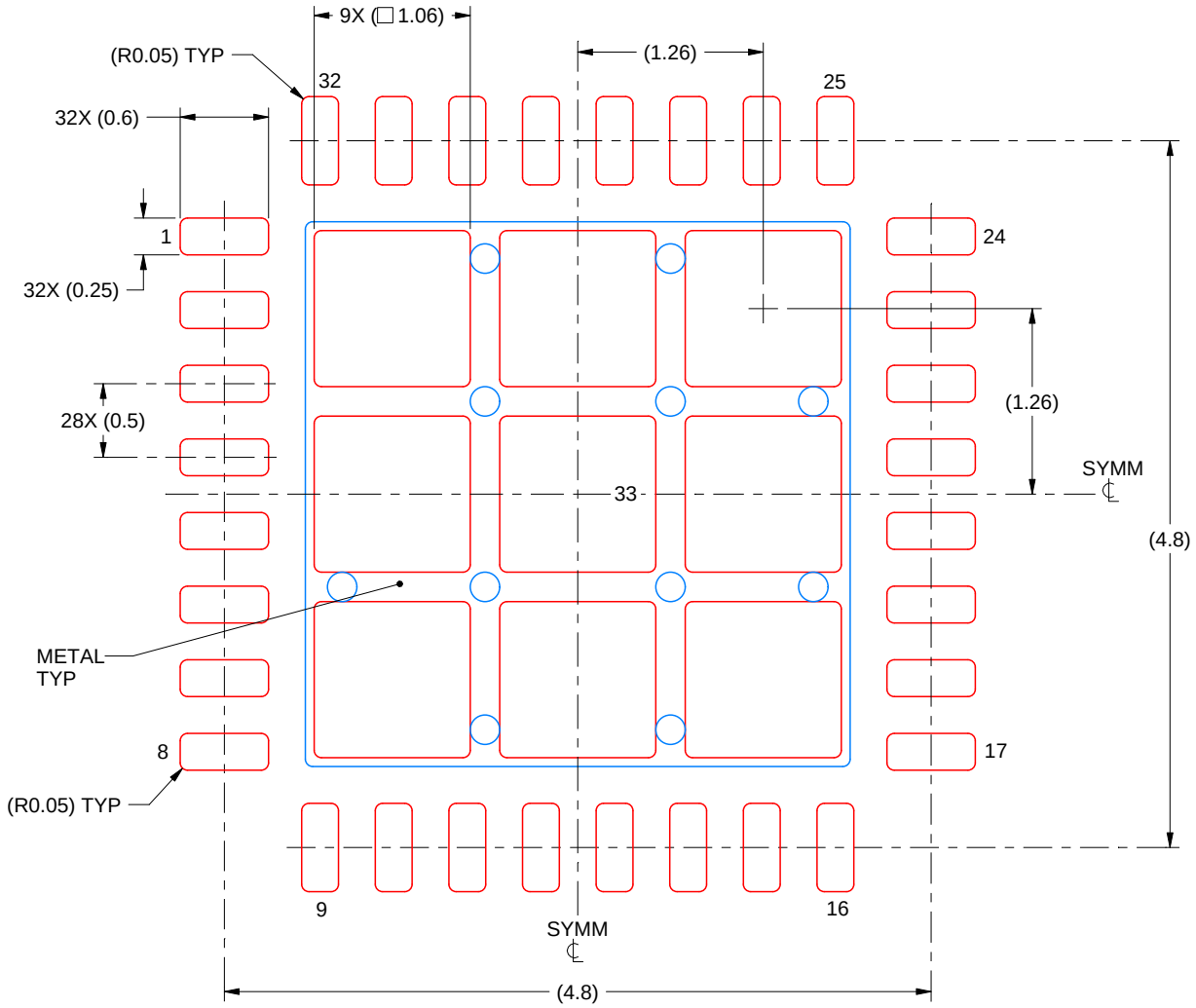


SOLDER MASK DETAILS

4225709/C 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225709/C 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025