TCAN942H-Q1 Automotive CAN FD Transceiver With Standby Mode and Enhanced Fault Protection

1 Features

- AEC-Q100 (Grade 1) Qualified for automotive applications
- Meets the requirements of ISO 11898-2:2024 and SAE J2284/5 physical layer standards for CAN FD
- Functional Safety-Capable
  - Documentation will be available upon device release to aid in functional safety system design
- Supports CAN and CAN FD communication up to 8Mbps
- Increased robustness for 48V battery architectures and other higher-voltage applications
  - High system-level short-to-battery and loss-of-ground resiliency
- V_{IO} level shifting supports 2.9V to 5.5V
- Wide ±30V receiver input common-mode range
- Protection features:
  - IEC ESD protection on bus pins
  - Absolute maximum rating of ±72 on CAN pins
  - Rated for system-level CAN bus faults of 58V or higher
  - Undervoltage and loss-of-GND protection
  - TXD dominant time-out (DTO)
  - Thermal shutdown protection (TSD)
- Operating modes:
  - Normal mode
  - Low-power standby mode supporting remote wake-up requests
- Ultra-passive behavior when unpowered
  - CAN pins become high-impedance when the device is unpowered
  - Hot plug capable: glitch-free operation on RXD during power-up and power-down
  - Defined device behavior during undervoltage conditions and when logic pins are floating
- Available in SOIC (8) and leadless 3mm × 3mm VSON (8) package with wettable flanks for automated optical inspection (AOI) capability

2 Applications

- 48V in automotive
- Advanced driver assistance system (ADAS)
- Body electronics and lighting
- Hybrid, electric & powertrain systems
- Automotive infotainment & cluster
- Robotics

3 Description

The TCAN942H-Q1 is a Controller Area Network (CAN) transceiver that meets the physical layer requirements of ISO 11898-2:2026 for CAN FD applications up to 8Mbps along with SAE J2284-1 through SAE J2284-5.

This family of transceivers has enhanced protection capability for system-level CAN short-to-battery and ECU loss-of-GND scenarios in 48V battery automotive settings, including for implementations using common-mode chokes. Additionally, these transceivers have certified electromagnetic compatibility (EMC) operation, making it an excellent choice for CAN CC and CAN FD networks in EMC-sensitive settings across all operation speeds. It is pin-compatible with 8-pin CAN FD and CAN SIC transceivers such as TCAN1044A(V)-Q1 and/or TCAN1472(V)-Q1.

The TCAN942HV-Q1 variant includes internal logic voltage translation using the V_{IO} pin, allowing the transceiver to work with either 3.3V or 5V controller logic levels. These devices also support low-power standby mode with remote wake-up via the CAN bus, compliant with the wake-up pattern (WUP) defined in ISO 11898-2:2024. The device family also includes many protection features such as undervoltage detection, thermal shutdown (TSD), driver dominant timeout (TXD DTO), and transient overvoltage protection on the CAN pins.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCAN942H-Q1	VSON (DRB)	3mm × 3mm
	SOIC (D)	4.9mm × 6mm

(1) For all available packages, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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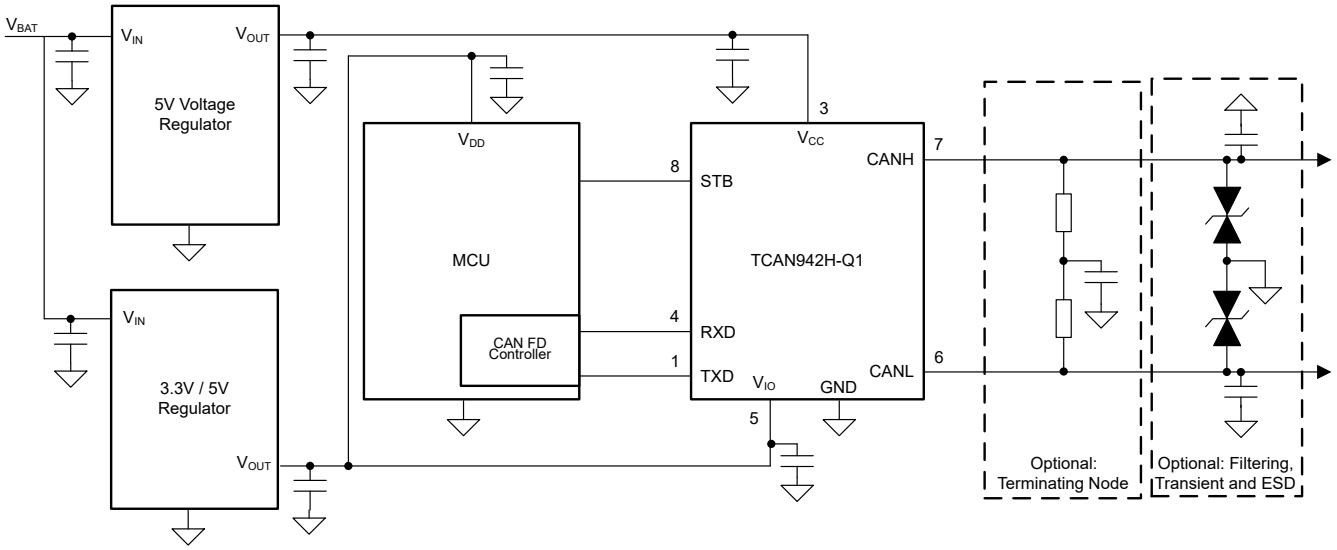

Simplified Block Diagram

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4 Device Comparison

Table 4-1. Device Comparison

DEVICE NAME	V_{IO} logic level translation support on pin 5
TCAN942H-Q1	No
TCAN942HV-Q1	Yes

5 Pin Configuration and Functions

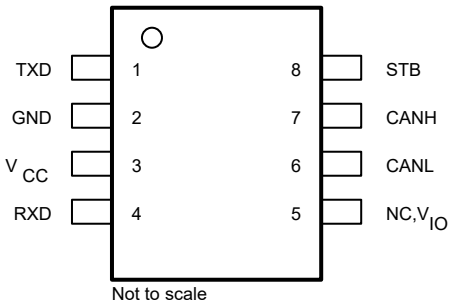

Figure 5-1. SOIC (D) Package, 8 Pin (Top View)

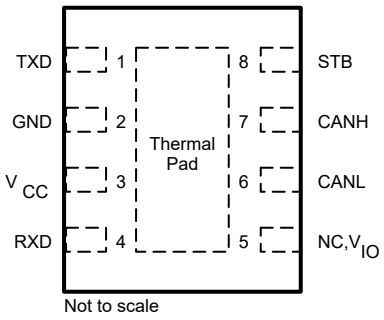

Figure 5-2. VSON (DRB) Package, 8 Pin (Top View)

Table 5-1. Pin Functions

PINS		TYPE	DESCRITION
NAME	NO.		
TXD	1	Digital Input	CAN transmit data input
GND	2	GND	Ground connection
V_{CC}	3	Supply	5V supply voltage
RXD	4	Digital Output	CAN receive data output, tristate when powered off
NC	5	—	Not internally connected (TCAN942H-Q1)
V_{IO}		Supply	Logic supply voltage (TCAN942HV-Q1)
CANL	6	Bus IO	Low-level CAN bus input/output line
CANH	7	Bus IO	High-level CAN bus input/output line
STB	8	Digital Input	Standby mode control input; integrated pull-up
Thermal Pad (VSON only)	—		Electrically connected to GND. Connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief.

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6 Specifications

6.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN Bus I/O voltage	–70	70	V
V_{DIFF}	Max differential voltage between CANH and CANL	–70	70	V
V_{Logic_Input}	Logic input terminal voltage	–0.3	6	V
V_{RXD}	RXD output terminal voltage range	–0.3	6	V
$I_{O(RXD)}$	RXD output current	–8	8	mA
T_J	Junction temperature	–40	150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	HBM classification level 3A for all pins	±4000	V
			HBM classification level 3B for global pins CANH and CANL with respect to GND	±8000	V
		Charged-device model (CDM), per AEC Q100-011		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 System-Level Transient and ESD Ratings

				VALUE	UNIT
V_{ESD}	System-level Electrostatic discharge	CAN bus terminals to GND	Unpowered contact discharge per ISO 10605(1)	±8000	V
			SAE J2962-2 per ISO 10605 Powered Contact Discharge(2)	±8000	V
			SAE J2962-2 per ISO 10605 Powered Air Discharge(2)	±15000	V
V_{Tran}	Transient voltage per ISO 7637-2(3)		Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	Transient voltage per ISO 7637-3(4)		DCC slow transient pulse	±30	V
V_{STB}	System-level CAN short-to-battery rating	Short-circuit rating for CAN lines using TCAN942H-Q1 with a 100µH common-mode choke	Standby mode or Normal mode (recessive)	70	V
			Normal mode, transmitter active and driving dominant and recessive bits onto the bus	58	V

(1) Tested according to IEC 62228-3:2019 CAN Transceivers.
(2) Results given here are specific to the SAE J2962-2 Communication Transceivers Qualification Requirements - CAN. Testing performed by OEM approved independent third party, EMC report available upon request.
(3) Tested according to IEC 62228-3:2019 CAN Transceivers.
(4) Tested according to SAE J2962-2.

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IO}	Supply voltage for I/O level shifter	2.9		5.5	V
$I_{OH(RXD)}$	RXD terminal high-level output current	–2			mA
$I_{OL(RXD)}$	RXD terminal low-level output current			2	mA
T_J	Operating junction temperature	-40		150	℃

6.5 Thermal Characteristics

THERMAL METRIC(1)		TCAN942H-Q1		UNIT
		D (SOIC)	DRB (VSON)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	℃/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	℃/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	TBD	℃/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.6 Supply Characteristics

Over recommended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current Normal mode	Dominant	STB = 0V, TXD = 0V R_L = 60Ω, C_L = open		45	70	mA
			STB = 0V, TXD = 0V R_L = 50Ω, C_L = open		49	80	mA
		Dominant with bus fault	STB = 0V, TXD = 0V CANH = CANL = ±25V R_L = open, C_L = open			130	mA
		Recessive	STB = 0V, TXD = V_{CC} or V_{IO} R_L = 50Ω, C_L = open		4.5	8	mA
I_{CC}	Supply current Standby mode Devices with V_{IO}		STB = TXD = V_{IO} R_L = 50Ω, C_L = open			5	µA
I_{CC}	Supply current Standby mode Devices without V_{IO}		STB = TXD = V_{CC} R_L = 50Ω, C_L = open			35	µA
I_{IO}	I/O supply current Normal mode	Dominant	STB = 0V, TXD = 0V RXD floating		125	410	µA
	I/O supply current Normal mode	Recessive	STB = 0V, TXD = V_{IO} RXD floating		25	60	µA
	I/O supply current Standby mode		STB = V_{IO}, TXD = V_{IO} RXD floating			30	µA
UV_{CC}	Rising undervoltage detection on V_{CC} for protected mode				4.2	4.4	V
	Falling undervoltage detection on V_{CC} for protected mode			3.5	4	4.25	V
$V_{HYS(UVCC)}$	Hysteresis voltage on UV_{CC}				200		mV
UV_{VIO}	Rising undervoltage detection on V_{IO} (Devices with V_{IO})				2.5	2.9	V
	Falling undervoltage detection on V_{IO} (Devices with V_{IO})			2.1	2.4		V
$V_{HYS(UVIO)}$	Hysteresis voltage on UV_{IO}				100		mV

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6.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation Normal mode	V_{CC} = 5V, V_{IO} = 3.3V, T_J = 27°C, R_L = 60Ω, C_{L_RXD} = 15pF TXD input = 250kHz 50% duty cycle square wave		TBD		mW
		V_{CC} = 5V, V_{IO} = 5V, T_J = 27°C, R_L = 60Ω, C_{L_RXD} = 15pF TXD input = 250kHz 50% duty cycle square wave		TBD		mW
		V_{CC} = 5.5V, V_{IO} = 3.3V, T_J = 150°C, R_L = 60Ω, C_{L_RXD} = 15pF TXD input = 2.5MHz 50% duty cycle square wave		TBD		mW
		V_{CC} = 5.5V, V_{IO} = 5V, T_J = 150°C, R_L = 60Ω, C_{L_RXD} = 15pF TXD input = 2.5MHz 50% duty cycle square wave		TBD		mW
T_{TSD}	Thermal shutdown temperature		165	180	195	°C
$T_{TSD(HYS)}$	Thermal shutdown hysteresis			10		°C

6.8 Electrical Characteristics

Over recommended operating conditions with T_J = -40°C to 150°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{O(DOM)}$	Dominant output voltage Normal mode	CANH	STB = 0V, TXD = 0V 50Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(REC)}$	Recessive output voltage Normal mode	CANH and CANL	STB = 0V, TXD = V_{IO} R_L = open (no load), R_{CM} = open	2	0.5V_{CC}	3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}		STB = 0V, TXD = 250kHz, 1MHz, 2.5MHz R_L = 60Ω, C_{SPLIT} = 4.7nF, C_L = open, R_{CM} = open	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry (V_{CC} - $V_{O(CANH)}$ - $V_{O(CANL)}$)		STB = 0V R_L = 60Ω, C_L = open	–400		400	mV
$V_{OD(DOM)}$	Differential output voltage Normal mode Dominant	CANH - CANL	STB = 0V, TXD = 0V 50Ω ≤ R_L ≤ 65Ω, C_L = open	1.5		3	V
			STB = 0V, TXD = 0V 45Ω ≤ R_L ≤ 70Ω, C_L = open	1.4		3.3	V
			STB = 0V, TXD = 0V R_L = 2240Ω, C_L = open	1.5		5	V
$V_{OD(REC)}$	Differential output voltage Normal mode Recessive	CANH - CANL	STB = 0V, TXD = V_{IO} R_L = 60Ω, C_L = open	–120		12	mV
			STB = 0V, TXD = V_{IO} R_L = open, C_L = open	–50		50	mV
$V_{O(STB)}$	Bus output voltage Standby mode	CANH	STB = V_{IO} R_L = open	-0.1		0.1	V
		CANL		-0.1		0.1	V
		CANH - CANL		-0.2		0.2	V
$I_{OS(SS\_DOM)}$	Short-circuit steady-state output current, dominant Normal mode		STB = 0V, TXD = 0V $V_{(CANH)}$ = -70V to 70V, CANL = open	–115			mA
			STB = 0V, TXD = 0V $V_{(CAN\_L)}$ = -70V to 70V, CANH = open			115	mA
$I_{OS(SS\_REC)}$	Short-circuit steady-state output current, recessive Normal mode		STB = 0V, TXD = V_{IO} –70V ≤ V_{BUS} ≤ 70V, where V_{BUS} = CANH = CANL	–5		5	mA
Receiver Electrical Characteristics							
V_{IT}	Input threshold voltage Normal mode - with OOB disabled		STB = 0V -30V ≤ V_{CM} ≤ 30V	500		900	mV
V_{HYS}	Hysteresis voltage for input threshold Normal mode - with OOB disabled		STB = 0V -30V ≤ V_{CM} ≤ 30V		115		mV

Over recommended operating conditions with T_J = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(STB)}$	Input threshold Standby mode	STB = V_{IO} -30V ≤ V_{CM} ≤ 30V	400		1150	mV
V_{DOM}	Dominant state differential input voltage range Normal mode	STB = 0V -30V ≤ V_{CM} ≤ 30V	0.9		9	V
V_{REC}	Recessive state differential input voltage range Normal mode	STB = 0V -30V ≤ V_{CM} ≤ 30V	-8		0.5	V
$V_{DOM(STB)}$	Dominant state differential input voltage range Standby mode	STB = V_{IO} -30V ≤ V_{CM} ≤ 30V	1.15		9	V
$V_{REC(STB)}$	Recessive state differential input voltage range Standby mode	STB = V_{IO} -30V ≤ V_{CM} ≤ 30V	-8		0.4	V
V_{CM}	Common-mode range Normal and standby modes		–30		30	V
$I_{LKG(IOFF)}$	Unpowered bus input leakage current	CANH = CANL = 5V, V_{CC} = V_{IO} = GND CANH = CANL = 5V, V_{CC} = V_{IO} = floating, GND = 0V			5	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{IO} (1)			20	pF
C_{ID}	Differential input capacitance				10	pF
R_{ID}	Differential input resistance	STB = 0V, TXD = V_{IO} (1) -30V ≤ V_{CM} ≤ 30V	40		90	kΩ
R_{IN}	Single-ended input resistance (CANH or CANL)		20		45	kΩ
$R_{IN(M)}$	Input resistance matching [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	$V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5V	–1		1	%
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7V_{CC}			V
		Devices with V_{IO}	0.7V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3V_{CC}	V
		Devices with V_{IO}			0.3V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5V	–2.5	0	1	µA
I_{IL}	Low-level input leakage current	TXD = 0V V_{CC} = V_{IO} = 5.5V	–200	-100	–20	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5V V_{CC} = V_{IO} = 0V	–1	0	1	µA
C_I	Input capacitance	V_{IN} = 0.4×sin(2×π×2×10^6×t) + 2.5V		2		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level output voltage	I_O = –2mA Devices without V_{IO}	0.8V_{CC}			V
		I_O = –1.5mA Devices with V_{IO}	0.8V_{IO}			V
V_{OL}	Low-level output voltage	I_O = 2mA Devices without V_{IO}			0.2V_{CC}	V
		I_O = 1.5mA Devices with V_{IO}			0.2V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5V V_{CC} = V_{IO} = 0V	–1	0	1	µA
STB Terminal (Standby Mode Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7V_{CC}			V
		Devices with V_{IO}	0.7V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3V_{CC}	V
		Devices with V_{IO}			0.3V_{IO}	V
I_{IH}	High-level input leakage current	V_{CC} = V_{IO} = STB = 5.5V	–2		2	µA
I_{IL}	Low-level input leakage current	STB = 0V V_{CC} = V_{IO} = 5.5V	–20		–2	µA
$I_{LKG(OFF)}$	Unpowered leakage current	STB = 5.5V V_{CC} = V_{IO} = 0V	–1	0	1	µA

(1) V_{IO} = V_{CC} in non-V variants of device

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6.9 Switching Characteristics

Over recommended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay Driver input (TXD) to receiver output (RXD), recessive to dominant	STB = 0V, V_{IO} = 2.9V to 5.5V R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF		125	210	ns
$t_{PROP(LOOP2)}$	Total loop delay Driver input (TXD) to receiver output (RXD), dominant to recessive	STB = 0V, V_{IO} = 2.9V to 5.5V R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF		150	210	ns
t_{MODE}	Mode change time, from normal to standby or from standby to normal				45	µs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout		0.8		6	ms
t_{WK_FILTER}	Filter time for a valid wake-up pattern		0.5		1.8	µs
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	STB = 0V R_L = 60Ω, C_L = 100pF		80		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			70		ns
$t_{sk(p)}$	Pulse skew (|tpHR - tpLD|)			14		ns
t_R	Differential output signal rise time			28		ns
t_F	Differential output signal fall time			50		ns
t_{TXD_DTO}	Dominant timeout		0.8		6.5	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high output (dominant to recessive)	STB = 0V $C_{L(RXD)}$ = 15pF		81		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (recessive to dominant)			66		ns
t_R	RXD output signal rise time			10		ns
t_F	RXD output signal fall time			10		ns
FD Timing Characteristics						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 500ns	STB = 0V R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF	455		510	ns
	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 200ns	STB = 0V R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF	155		210	ns
	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 125ns	STB = 0V R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF	85		130	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins $t_{BIT(TXD)}$ = 500ns	STB = 0V R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF	420		520	ns
	Bit time on RXD output pins $t_{BIT(TXD)}$ = 200ns	STB = 0V R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF	120		220	ns
	Bit time on RXD output pins $t_{BIT(TXD)}$ = 125ns	STB = 0V R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF	75		135	ns
Δt_{REC}	Receiver timing symmetry $t_{BIT(TXD)}$ = 500ns	STB = 0V R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	-45		15	ns
	Receiver timing symmetry $t_{BIT(TXD)}$ = 200ns	STB = 0V R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	-45		15	ns
	Receiver timing symmetry $t_{BIT(TXD)}$ = 125ns	STB = 0V R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	-40		10	ns

7 Detailed Description

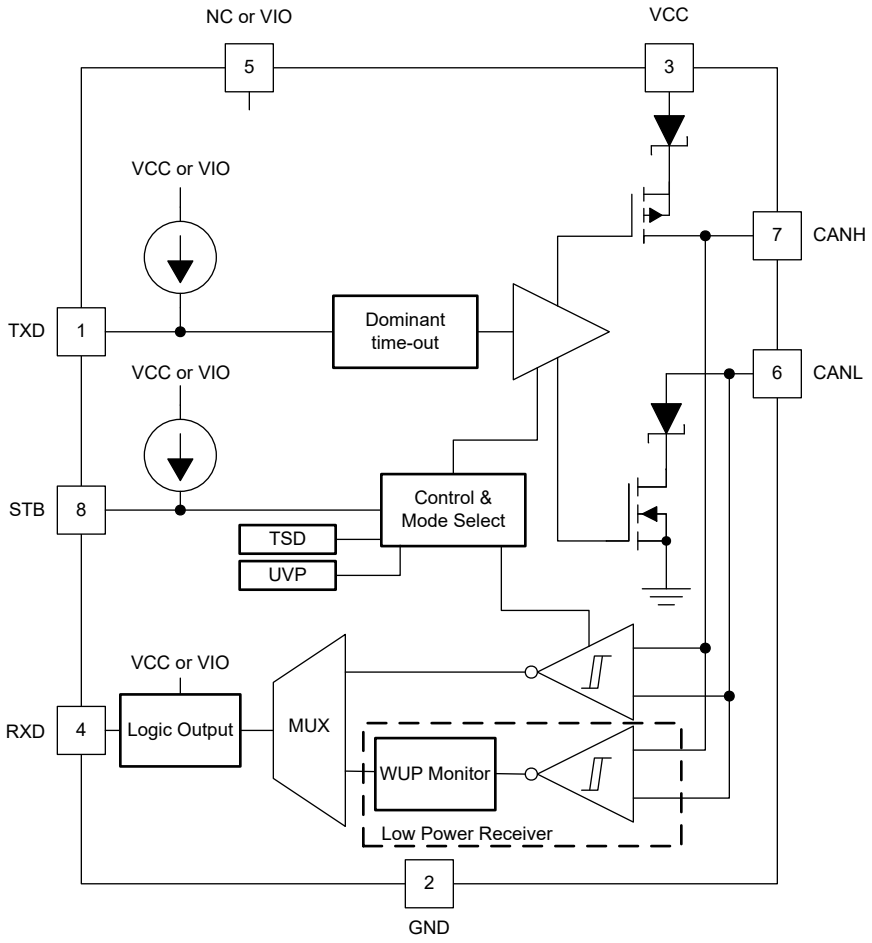
7.1 Overview

The TCAN942H-Q1 devices meet or exceed the specifications of the ISO 11898-2 Controller Area Network (CAN) physical layer standard. The devices support both CAN and CAN FD at data rates up to 8Mbps, allowing for high-performance multipoint communication across various network topologies. This generation of transceivers is designed with enhanced functionality to provide system-level robustness against short-circuit and ground-loss faults in higher-voltage environments, such as battery electric vehicles or automobiles with 48V battery supplies.

In CAN networks, common mode chokes (CMCs) can cause high voltage transients due to inductive flyback in system-level short-circuit conditions which may greatly exceed the maximum ratings of the transceiver. The TCAN942H-Q1 is designed to handle these fault events without destroying the device. ECUs using TCAN942H-Q1 can be designed to meet stringent system-level requirements, such as those outlined in ISO 16750, ISO 21780, and ISO/WD 25769.

The TCAN942HV-Q1 has two separate supply input rails: V_{CC} for the 5V CAN bus supply and V_{IO} logic supply for logic-level translation, allowing for connection directly to 3.3V or 5V controllers.

7.2 Functional Block Diagram



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7.3 Detailed Pin Description

7.3.1 TXD

The TXD input is a logic-level signal from a CAN controller to the transceiver. This input is referenced to V_{IO} (or V_{CC} for devices without V_{IO}).

7.3.2 GND

GND is the ground pin of the transceiver. It must be connected to the PCB ground.

7.3.3 V_{CC}

V_{CC} provides the 5V power supply to the CAN transceiver.

7.3.4 RXD

The RXD output is a logic-level signal from the CAN transceiver to the CAN controller. RXD is referenced to V_{CC} for TCAN942H-Q1 or to V_{IO} for TCAN942HV-Q1. For TCAN942HV-Q1, RXD is only driven once V_{IO} is present.

When a wake event takes place, RXD is driven low.

7.3.5 V_{IO} (only for TCAN942HV-Q1)

The V_{IO} pin is an input supply pin to the transceiver which provides the digital I/O voltage reference for the logic pins. This allows the digital I/O voltage to match the CAN controller voltage, thereby avoiding the requirement of a level shifter. The pin supports voltages from 2.9V to 5.5V.

7.3.6 CANH and CANL

These are the CAN high (CANH) and CAN low (CANL) differential bus pins. These pins are connected to the CAN transceiver and the low-voltage WUP CAN receiver.

The CANH and CANL pins are designed to withstand transient voltage spikes resulting from system-level short-circuit and loss-of-GND events, including in implementations with common-mode chokes (CMCs).

7.3.7 STB (Standby)

The STB pin is an input pin used for mode control of the transceiver. The STB input can be provided by either the system processor or by a static system voltage source or rail. If normal mode is the only intended mode of operation, the STB pin can be tied directly to GND.

7.4 Feature Description

7.4.1 CAN Bus States

The CAN bus has two logical states during operation: *recessive* and *dominant* (see Figure 7-1). A dominant bus state occurs when the bus is driven differentially with $V_{DIFF} \geq +1.5V$ and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins. A dominant state overwrites the recessive state during arbitration or error conditions. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCAN942H-Q1 family implements a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high-resistance internal resistors of the receiver (see Figure 7-1 and Figure 7-2).

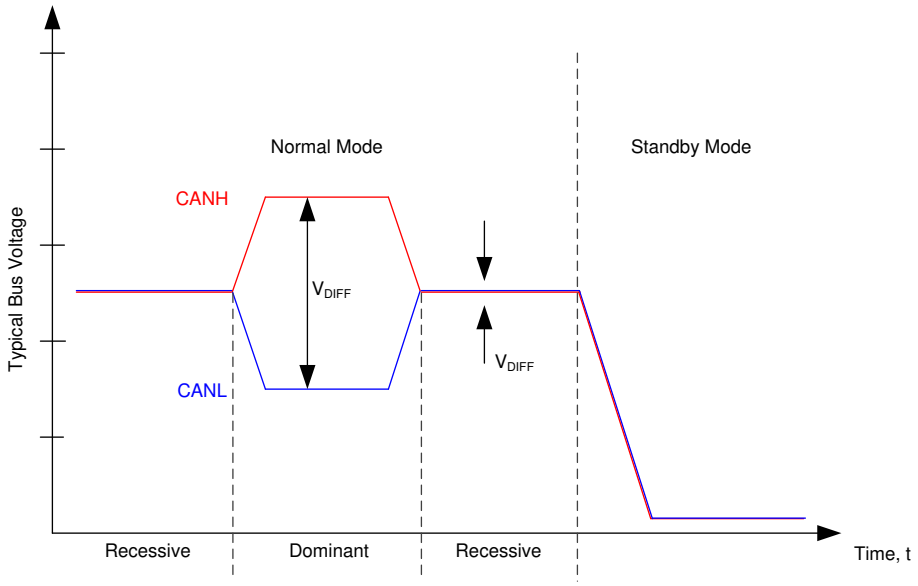
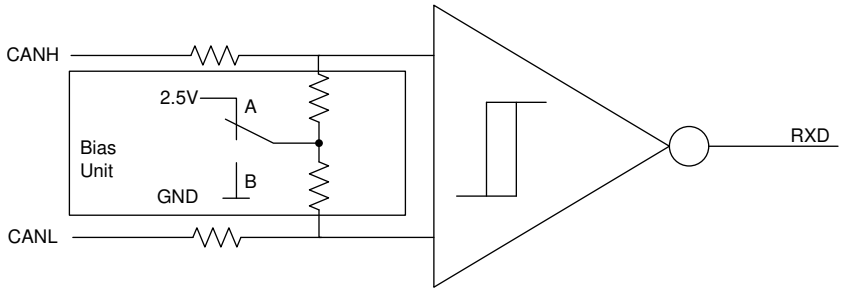


Figure 7-1. Bus States



A - Normal Mode B - Standby Mode

Figure 7-2. Simplified Recessive Common Mode Bias Unit and Receiver

7.4.2 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin; thus, clearing the dominant time out. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate can be calculated using Equation 1.

$$\text{Minimum Data Rate} = \frac{11 \text{ bits}}{t_{TXD\_DTO}} = \frac{11\ bits}{0.8ms} = 13.8\text{kbps} \quad (1)$$

ADVANCE INFORMATION

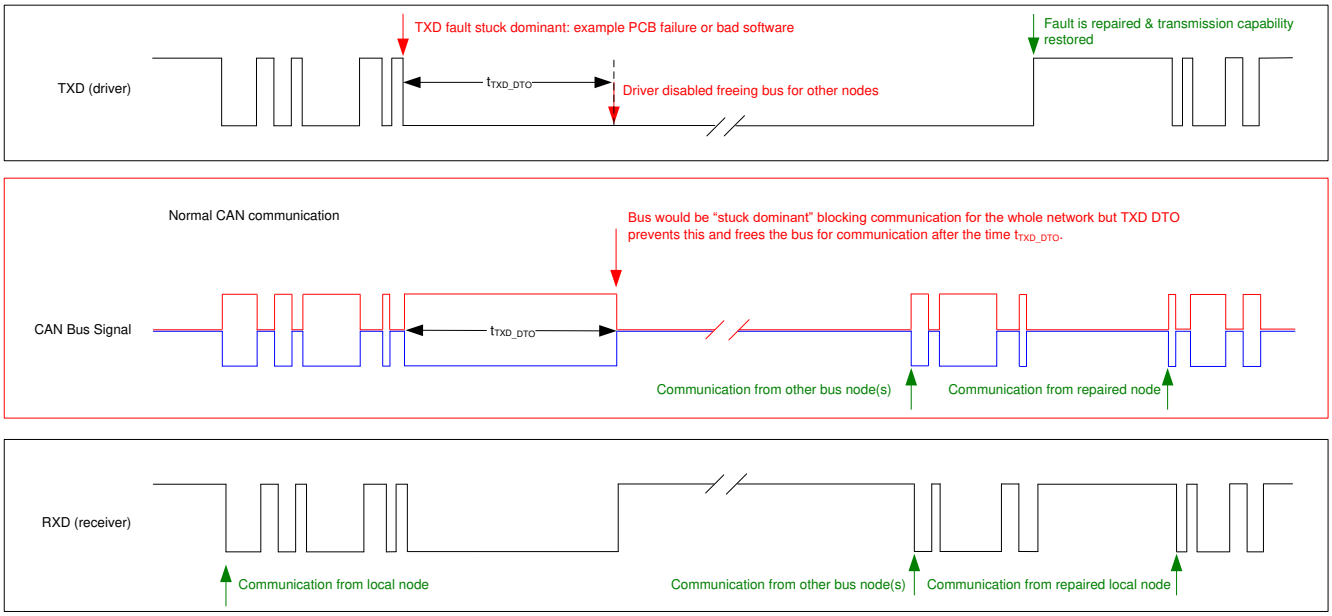


Figure 7-3. Example Timing Diagram for TXD Dominant Timeout

7.4.3 CAN Bus Short-Circuit Tolerance

The TCAN942H-Q1 has several features that protect the device during both device-level and system-level short-circuits on the CAN bus. Features include TXD dominant timeout, CAN driver current limiting in both the dominant and recessive states, and resiliency transient stresses on CANH and CANL caused by CMC flyback during short-to-battery fault conditions. Short-circuit current limiting on CANH and CANL keeps current flow and power dissipation within a regulated range during fault conditions. TXD dominant timeout prevents scenarios where the full short-circuit current flows permanently into or out of the CAN pins due to a prolonged low-level input to TXD in these faults. Additionally, the TCAN942H-Q1 family is designed to handle transient stresses on the CANH and CANL pins that can be generated by CAN networks that utilize common-mode chokes.

These protection features allow for device survival during system-level short-circuit events, both with and without continued activity from the transmitter.

7.4.4 Thermal Shutdown (TSD)

If the junction temperature of the TCAN942H-Q1 exceeds the thermal shutdown threshold (T_{TSD}), the device turns off the CAN driver circuitry and blocks the TXD-to-bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver-to-RXD path remains operational. The TCAN942H-Q1 TSD circuit includes hysteresis, which prevents the CAN driver output from oscillating during a TSD fault.

7.4.5 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

Table 7-1. Undervoltage Lockout - TCAN942H-Q1

V_{CC}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	Protected	High impedance	High impedance

Table 7-2. Undervoltage Lockout - TCAN942HV-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus

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Table 7-2. Undervoltage Lockout - TCAN942HV-Q1 (continued)

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
< UV_{VCC}	> UV_{VIO}	STB = V_{IO}: standby mode	High impedance	V_{IO}: Remote wake request(1)
		STB = GND: Protected		Recessive
> UV_{VCC}	< UV_{VIO}	Protected		High impedance
< UV_{VCC}	< UV_{VIO}	Protected		High impedance

(1) See Section 7.5.3.1

Once the undervoltage condition is cleared and t_{MODE} has expired, the TCAN942H-Q1 transitions to normal mode and the host controller can send and receive CAN traffic again.

7.4.6 Unpowered Device

The TCAN942H-Q1 is designed to be passive to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so the pins do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the network remains operational.

The logic pins also have low leakage currents when the device is unpowered so that the pins do not load other powered circuits.

7.4.7 Floating Pins

The TCAN942H-Q1 has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias is intended as a failsafe feature rather than a default design consideration, especially in noisy environments.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This ensures that the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See Table 7-3 for details on pin bias conditions.

Table 7-3. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD towards recessive to prevent bus blockage or TXD DTO triggering
STB	Pull-up	Weakly biases STB towards low-power standby mode to prevent excessive system power

7.5 Device Functional Modes

7.5.1 Operating Modes

The TCAN942H-Q1 has two main operating modes: normal mode and standby mode. The operating mode selection is made by applying a high or low level to the STB pin.

Table 7-4. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Standby Mode	Disabled	Low-power receiver and bus monitor enabled	High (recessive) until valid WUP is received(1)
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

(1) See Section 7.5.3.1

7.5.2 Normal Mode

This is the normal operating mode of the TCAN942H-Q1. In this mode, CAN communication is bidirectional. The driver is translating a signal on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD pin.

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7.5.3 Standby Mode

This is the low-power mode of the device. The CAN driver and main receiver are switched off and bidirectional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD as shown in Figure 7-4. The local CAN protocol controller should monitor RXD for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB pin low. The CAN bus pins are weakly pulled to GND in this mode (see Figure 7-1 and Figure 7-2).

In standby mode, only the V_{IO} supply is required; therefore, the V_{CC} may be switched off for additional system level current savings.

7.5.3.1 Remote Wake Request Using Wake-Up Pattern (WUP) in Standby Mode

The TCAN942H-Q1 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node needs to return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2024 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the TCAN942H-Q1.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP; thus, no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ can be detected as part of a WUP and a wake-up request can be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is always generated. See Figure 7-4 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2024 standard has defined times for a short and long wake-up filter time. The t_{WK_FILTER} timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500kbps, or two back-to-back bit times at 1Mbps triggers the filter in either bus state. Any CAN frame at 500kbps or less contains a valid WUP.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \leq t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in the current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See Figure 7-4 for the timing diagram of the wake-up pattern with wake timeout feature.

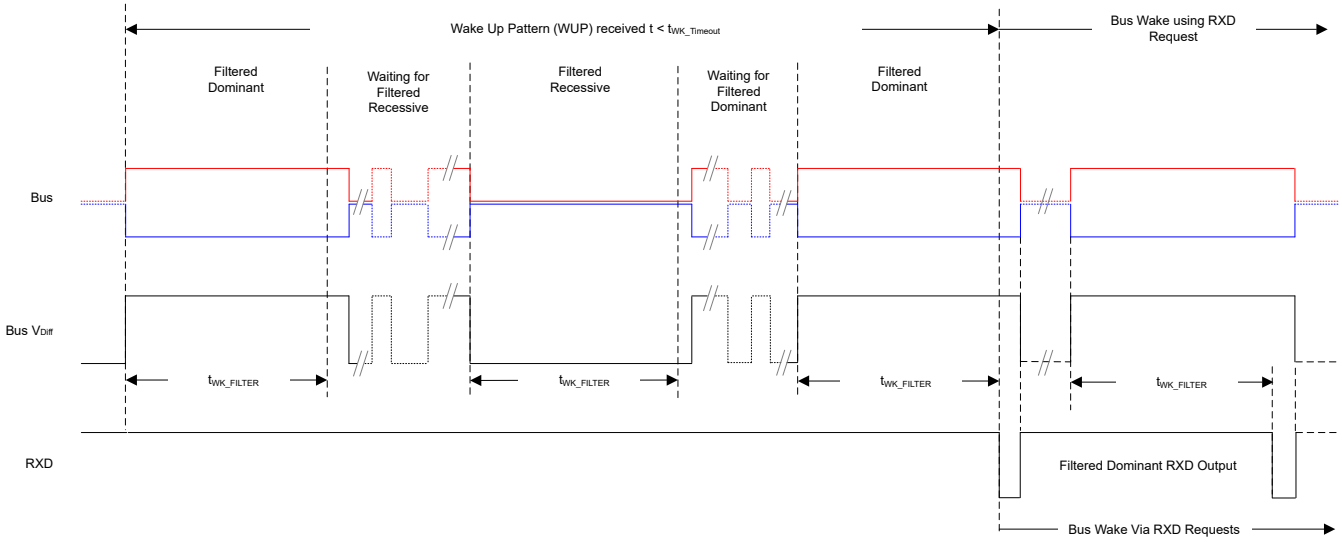

Figure 7-4. Wake-Up Pattern (WUP) With $t_{WK\_TIMEOUT}$

7.5.4 Driver and Receiver Function

The TCAN942H-Q1 logic I/Os support CMOS levels with respect to either V_{CC} for 5V systems (TCAN942H-Q1) or V_{IO} for compatibility with MCUs that support 3.3V or 5V systems (TCAN942HV-Q1).

Table 7-5. Driver Function Table

Device Mode	TXD Input(1)	Bus Outputs		Driven Bus State(2)
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Standby	X	High impedance	High impedance	Biased to ground

(1) X = irrelevant
(2) For bus state and bias see Figure 7-1 and Figure 7-2

Table 7-6. Receiver Function Table Normal and Standby Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal	$V_{ID} \geq 0.9V$	Dominant	Low
	$0.5V < V_{ID} < 0.9V$	Undefined	Undefined
	$V_{ID} \leq 0.5V$	Recessive	High
Standby	$V_{ID} \geq 1.15V$	Dominant	High Low if a remote wake event occurred (See Figure 7-4)
	$0.4V < V_{ID} < 1.15V$	Undefined	
	$V_{ID} \leq 0.4V$	Recessive	
Any	Open ($V_{ID} \approx 0V$)	Open	High

ADVANCE INFORMATION

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTCAN942HDRQ1	Active	Preproduction	SOIC (D) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	
PTCAN942HVDRQ1	Active	Preproduction	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

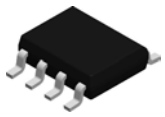
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

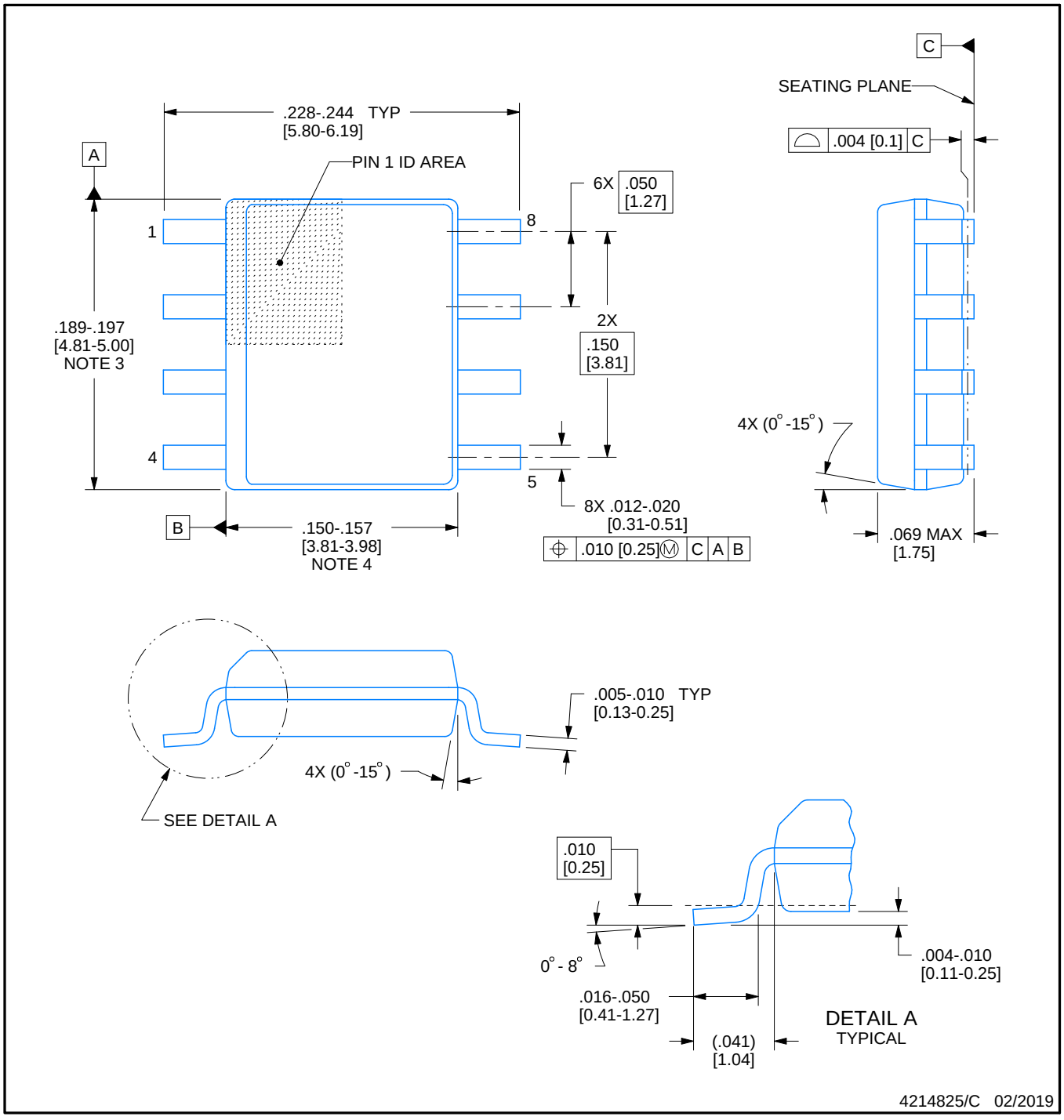


PACKAGE OUTLINE

D0008A

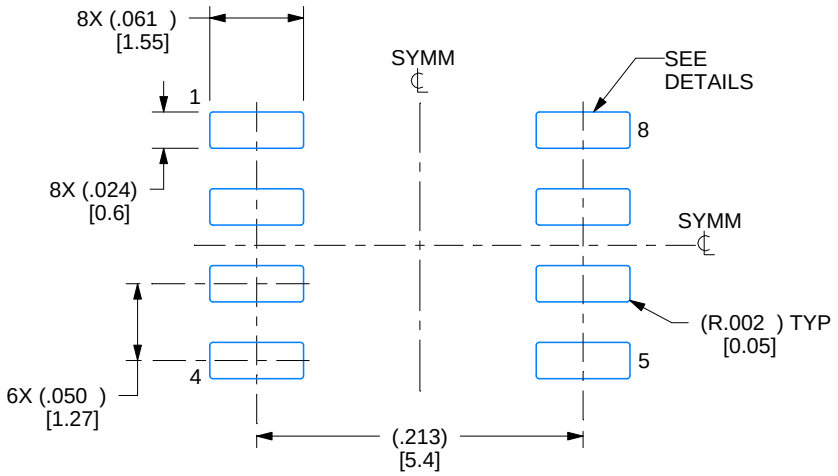
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

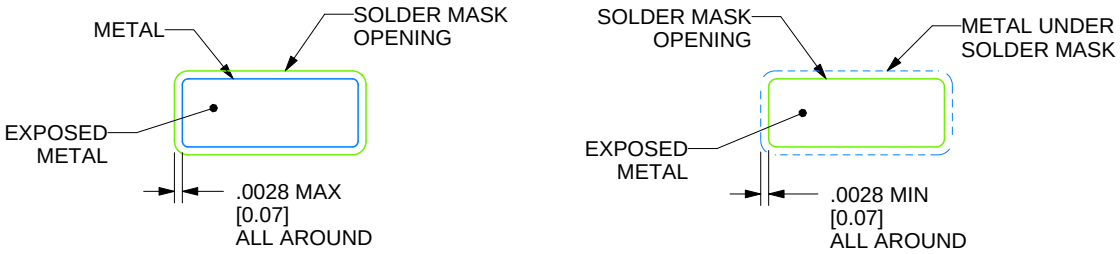


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

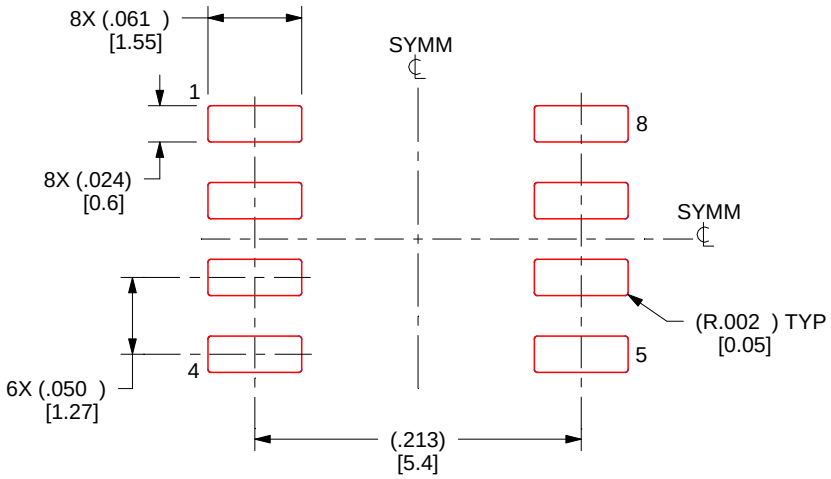
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025