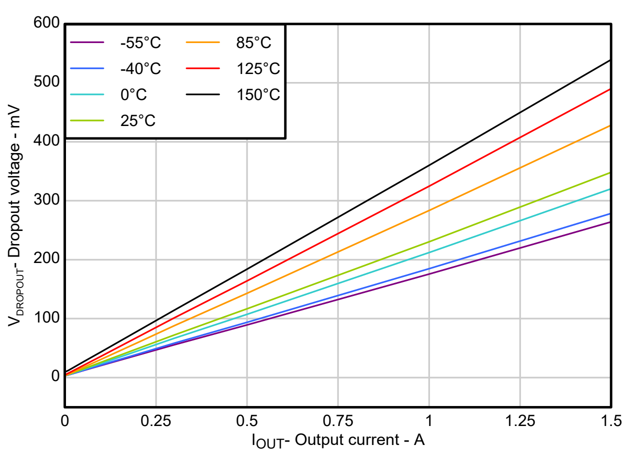
TL1963A 1.5A Low-Noise Fast-Transient-Response Low-Dropout Regulator

1 Features

- Input voltage range: 2.4V to 20V
- Output voltage range (adjustable): 1.21V to 20V
- Output voltage range (fixed):
  - Legacy chip: 1.5V, 1.8V, 2.5V and 3.3V
  - New chip: 1.8V, 3.3V
- Output accuracy (over line, load and temperature):
  - Legacy chip: ±3% (all packages)
  - New chip:
    - +3%/-2% (DCY only)
    - ±1.5% (DCQ and KTT only)
- Maximum output current (I_{OUT}): Up to 1.5A
- Dropout voltage: 340mV (typical) for I_{OUT} = 1.5A
- Output capacitor for stable operation: ≥ 10µF with ESR ≤ 3Ω
- Low noise: 23µV_{RMS} (10Hz to 100kHz) for V_{OUT} = 1.21V
- Integrated fault protection:
  - Reverse-current, thermal shutdown and overcurrent protection (both legacy and new chip)
  - Reverse-battery protection (legacy chip only)
- Package:
  - 4-pin SOT-223 (DCY)
  - 6-pin SOT-223 (DCQ)
  - 5-pin DDPAK/TO-263 (KTT)

2 Applications

- EV charging infrastructure
- Energy storage systems
- Medical Imaging
- Semiconductor test and ATE



Dropout Voltage versus Output Current (New Chip)

3 Description

The TL1963A-xx regulators are low-dropout (LDO) regulators provides a robust, easy-to-use power management design for wide variety of applications. The device can supply 1.5A of output current with a dropout voltage of 340mV (typical) and supports wide output range (from 1.21V to 20V) in adjustable configuration. In addition, TL1963A-xx also supports tighter output accuracy ±1.5% across line, load and temperature (for DCQ, KTT package of new chip), fast transient response, and low output noise (23µV_{RMS} in unity-gain adjustable configuration), making it an excellent choice for sensitive RF supply applications.

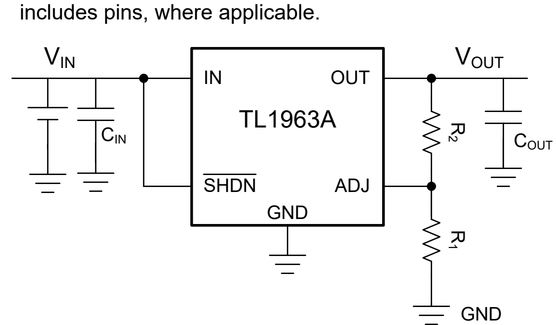
The TL1963A-xx regulators are stable with output capacitor as low as 10µF and supports ESR range up-to 3Ω. The TL1963A-xx (both legacy chip and new chip) has built-in protection mechanism for over-current, over-temperature (thermal shutdown) and reverse-current protection for reliable operation of the LDO and the legacy chip of TL1963A-xx also includes reverse-battery protection.

The TL1963A-xx is available in a 6.50mm × 7.0mm, 4-pin SOT-223 (DCY) [only fixed], 6.50mm × 7.06mm, 6-pin SOT-223 (DCQ) and 10.16mm × 15.24mm, 5-pin DDPAK/TO-263 (KTT) package for fixed and adjustable outputs.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TL1963A-xx	DCY (SOT-223, 4)	6.50mm × 7.00mm
	DCQ (SOT-223, 6)	6.50mm × 7.06mm
	KTT (DDPAK/ TO-263, 5)	10.16mm × 15.24mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

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4 Pin Configuration and Functions

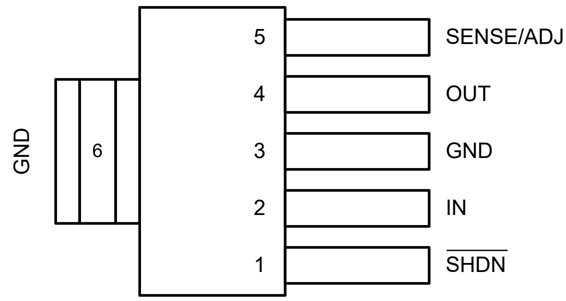


Figure 4-1. DCQ (SOT-223-6) Pin Configuration (Top View)

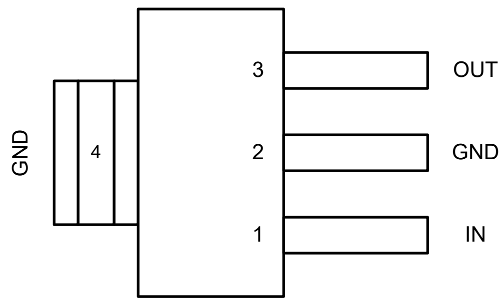


Figure 4-2. DCY (SOT-223-4) Pin Configuration (Top View)

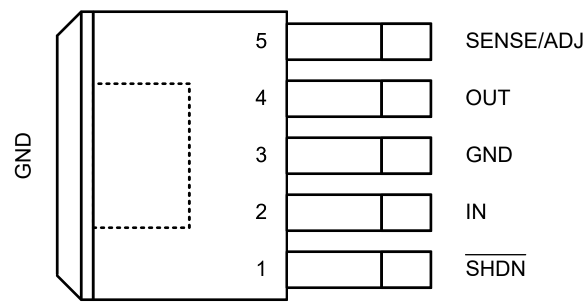


Figure 4-3. KTT (DDPAK/TO-263-5) Pin Configuration (Top View)

Table 4-1. Pin Functions

PIN				TYPE[(1)]	DESCRIPTION
NAME	DCQ	DCY	KTT		
ADJ	5	—	5	I	For TL1963A adjustable configuration, this pin sets the output voltage with the help of a feedback divider. This pin must be connected to output either directly or through a resistor divider for the device to function. Current flowing in ADJ pin can impact output accuracy and is captured as I_{ADJ} in Electrical Characteristics: TL1963A (for DCQ, KTT package).
GND	3, 6	2, 4	3	—	Ground
IN	2	1	2	I	Input supply pin. See the Recommended Operating Conditions table and the *Input/Output Capacitance and Transient Response* for more information. The TL1963A-xx regulators (legacy chip only) are designed with reverse-polarity protection and both new and legacy chip versions are designed with reverse-current protection.
OUT	4	3	4	O	Output of the regulator. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; See the Recommended Operating Conditions table and the *Input/Output Capacitance and Transient Response* section. Place the output capacitor as close to output of the device as possible.

Table 4-1. Pin Functions (continued)

PIN				TYPE[(1)]	DESCRIPTION
NAME	DCQ	DCY	KTT		
SENSE	5	—	5	I	For fixed voltage versions of the TL1963A-xx, the SENSE pin is the input to the error amplifier. The SENSE pin bias current is captured as I_{SENSE} in Electrical Characteristics: TL1963A (for DCQ, KTT package). For legacy chip, the SENSE pin can be pulled below ground (as in a dual supply system in which the regulator load is returned to a negative supply) and still allow the device to start and operate. See the Kelvin Sense Connection with SENSE pin for further details.
$\overline{SHDN}$	1	—	1	I	Driving the $\overline{SHDN}$ pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the Electrical Characteristics: TL1963A (for DCQ, KTT package) table. If unused, the $\overline{SHDN}$ pin must be connected to V_{IN}. For legacy chip, the device is in the low-power shutdown state if the $\overline{SHDN}$ pin is not connected.
Thermal Pad	—	—	—	—	For the KTT, DCY and DCQ package, the exposed thermal pad is connected to ground and must be soldered to the PCB for rated thermal performance.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Voltage	Input Voltage (for legacy chip)	–20	20	V
	Input Voltage (for new chip)	–0.3	20.2	V
	Output Voltage (for legacy chip)	–20	20	V
	Output Voltage (for new chip, DCY)	–0.3	7	V
	Output Voltage (for new chip, DCQ & KTT)	–0.3	20	V
	Input-to-Output Differential (for legacy chip)	–20	20	V
	Input-to-Output Differential (for new chip)	–7.0	20	V
	Sense Voltage (for legacy chip)	–20	20	V
	Sense Voltage (for new chip)	–0.3	7	V
	ADJ Voltage (for legacy chip)	–7	7	V
	ADJ Voltage (for new chip)	–0.3	7	V
	$\overline{SHDN}$ Voltage (for legacy chip)	–20	20	V
	$\overline{SHDN}$ Voltage (for new chip)	–0.3	20	V
Output short-circuit duration, t_{SHORT}			Indefinite	°C
Maximum lead temperature (10s soldering time), T_{LEAD}			300	°C
Maximum junction temperature, T_{JMAX} (for legacy chip)			125	°C
Operating junction temperature, T_J (for new chip)		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE (Legacy chip)	VALUE (New chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000		V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±1000		

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage	Legacy Chip	V_{OUT} + V_{DO}		20	V
		New chip	2.4		20	
V_{IH}	$\overline{SHDN}$ High Level Input Voltage		2		20	V
V_{IL}	$\overline{SHDN}$ Low Level Input Voltage				0.25	V
I_{OUT}	Output current		0		1.5	A
T_J	Operating junction temperature		–40		125	°C

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	TYP	MAX	UNIT
C_{IN}	Input capacitor	New chip		1		µF
C_{OUT}	Output capacitor		10			µF
$C_{OUT\ ESR}$	Output capacitor ESR (New Chip)		10m		3	Ω

(1) TL1963A may require a higher minimum input voltage under some output voltage/load conditions as indicated under Electrical Characteristics.

5.4 Thermal Information

THERMAL METRIC[(1)]		TL1963A-xx				UNIT
		KTT 5 PINS	DCQ 6 PINS	DCY 4 PINS		
				Legacy chip	New chip	
$R_{\theta JA}$	Junction-to-ambient thermal resistance, Legacy Device	32.9	50.5	57.9	73.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance, Legacy Device	37.6	31.1	38.6	44.01	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance, Legacy Device	18.9	5.1	7.1	12.67	°C/W
Ψ_{JT}	Junction-to-top characterization parameter, Legacy Device	5.7	1.0	1.7	3.56	°C/W
Ψ_{JB}	Junction-to-board characterization parameter, Legacy Device	17.3	5.0	7.0	12.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance, Legacy Device	1.0	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics: TL1963A (for DCQ, KTT package)

Specified at $V_{IN} = V_{OUT} + 1V$, $V_{EN} = 5V$, $I_{OUT} = 1mA$, $C_{OUT} = 10µF$, $C_{IN} = 1µF$ and $T_J = -40°C$ to $125°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
V_{IN} Minimum Input Voltage, Legacy Device	$I_{LOAD} = 0.5A$		$T_J = 25°C$		1.9		V
	$I_{LOAD} = 1.5A$		$T_J = –40°C$ to 125°C		2.1	2.5	V
V_{IN} Minimum Input Voltage, New Chip	$I_{LOAD} = 0.5A$		$T_J = 25°C$			2.4	V
	$I_{LOAD} = 1.5A$		$T_J = –40°C$ to 125°C			2.4	V
$V_{UVLO\ (RISING)}$, New Chip	V_{IN} rising, $I_{OUT} = 10mA$		$T_J = –40°C$ to 125°C	2.0	2.2	2.3	V
$V_{UVLO\ (FALLING)}$, New Chip	V_{IN} falling, $I_{OUT} = 10mA$		$T_J = –40°C$ to 125°C	1.9	2.05	2.15	V
$V_{UVLO\ (HYST)}$, New Chip			$T_J = –40°C$ to 125°C		150		mV
V_{OUT} Regulated output voltage, Legacy Device	TL1963A-18	$V_{IN} = 2.3V$, $I_{LOAD} = 1mA$	$T_J = 25°C$	1.773	1.8	1.827	V
		$V_{IN} = 2.8V$ to 20V, $I_{LOAD} = 1mA$ to 1.5A	$T_J = –40°C$ to 125°C	1.737	1.8	1.854	V
	TL1963A-33	$V_{IN} = 3.8V$, $I_{LOAD} = 1mA$	$T_J = 25°C$	3.25	3.3	3.35	V
		$V_{IN} = 4.3V$ to 20V, $I_{LOAD} = 1mA$ to 1.5A	$T_J = –40°C$ to 125°C	3.2	3.3	3.4	V

5.5 Electrical Characteristics: TL1963A (for DCQ, KTT package) (continued)

Specified at V_{IN} = V_{OUT} + 1V, V_{EN} = 5V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{IN} = 1µF and T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
V_{ADJ} ADJ pin voltage, Legacy Device	TL1963A	V_{IN} = 2.21V, I_{LOAD} = 1mA	T_J = 25°C	1.192	1.21	1.228	V
		V_{IN} = 2.5V to 20V, I_{LOAD} = 1mA to 1.5A	T_J = –40°C to 125°C	1.174	1.21	1.246	V
V_{OUT} Regulated output voltage, New Chip	TL1963A-18	V_{IN} = 2.4V, I_{LOAD} = 1mA	T_J = 25°C	1.782	1.8	1.818	V
		V_{IN} = 2.8V to 20V, I_{LOAD} = 1mA to 1.5A	T_J = –40°C to 125°C	1.773	1.8	1.827	V
	TL1963A-33	V_{IN} = 3.8V, I_{LOAD} = 1mA	T_J = 25°C	3.284	3.3	3.316	V
		V_{IN} = 4.3V to 20V, I_{LOAD} = 1mA to 1.5A	T_J = –40°C to 125°C	3.25	3.3	3.35	V
V_{ADJ} ADJ pin voltage, New Chip	TL1963A	V_{IN} = 2.4V, I_{LOAD} = 1mA	T_J = 25°C	1.204	1.21	1.216	V
		V_{IN} = 2.4V to 20V, I_{LOAD} = 1mA to 1.5A	T_J = –40°C to 125°C	1.192	1.21	1.228	V
Line Regulation, Legacy Device	TL1963A-18	ΔV_{IN} = 2.3V to 20V, I_{LOAD} = 1mA	T_J = –40°C to 125°C		2.5	7	mV
	TL1963A-33	ΔV_{IN} = 3.8V to 20V, I_{LOAD} = 1mA			3.5	10	mV
	TL1963A	ΔV_{IN} = 2.21V to 20V, I_{LOAD} = 1mA			1.5	5	mV
Line Regulation, New Chip	TL1963A-18	ΔV_{IN} = 2.4V to 10V, I_{LOAD} = 1mA	T_J = –40°C to 125°C		1.25	7	mV
		ΔV_{IN} = 2.4V to 20V, I_{LOAD} = 1mA			2.5	7	mV
	TL1963A-33	ΔV_{IN} = 3.8V to 10V, I_{LOAD} = 1mA			2.0	10	mV
		ΔV_{IN} = 3.8V to 20V, I_{LOAD} = 1mA			2.5	10	mV
	TL1963A	ΔV_{IN} = 2.4V to 10V, I_{LOAD} = 1mA			1.0	5	mV
		ΔV_{IN} = 2.4V to 20V, I_{LOAD} = 1mA			1.0	5	mV
Load Regulation, Legacy Device	TL1963A-18	V_{IN} = 2.8V, ΔI_{LOAD} = 1mA to 1.5A	T_J = 25°C		2	10	mV
			T_J = –40°C to 125°C			20	mV
	TL1963A-33	V_{IN} = 4.3V, ΔI_{LOAD} = 1mA to 1.5A	T_J = 25°C		3	20	mV
			T_J = –40°C to 125°C			70	mV
	TL1963A	V_{IN} = 2.5V, ΔI_{LOAD} = 1mA to 1.5A	T_J = 25°C		2	8	mV
			T_J = –40°C to 125°C			18	mV
Load Regulation, New Chip	TL1963A-18	V_{IN} = 2.8V, ΔI_{LOAD} = 1mA to 1.5A	T_J = 25°C			3.5	mV
			T_J = –40°C to 125°C			9	mV
	TL1963A-33	V_{IN} = 4.3V, ΔI_{LOAD} = 1mA to 1.5A	T_J = 25°C			6.5	mV
			T_J = –40°C to 125°C			16.5	mV
	TL1963A	V_{IN} = 2.4V, ΔI_{LOAD} = 1mA to 1.5A	T_J = 25°C			2.5	mV
			T_J = –40°C to 125°C			6	mV
		V_{IN} = 2.4V, ΔI_{LOAD} = 1mA to 1.5A	T_J = –40°C to 125°C	-0.5		0.5	%

5.5 Electrical Characteristics: TL1963A (for DCQ, KTT package) (continued)

Specified at V_{IN} = V_{OUT} + 1V, V_{EN} = 5V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{IN} = 1µF and T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
V_{DO} Dropout voltage	TL1963A: V_{IN} ≥ 2.4V, V_{ADJ} = 0.9 × V_{REF} TL1963A-33: V_{IN} = 3.3V	I_{LOAD} = 1mA	T_J = 25°C		0.0015	0.06	V
			T_J = –40°C to 125°C			0.1	V
		I_{LOAD} = 100mA	T_J = 25°C		0.025	0.17	V
			T_J = –40°C to 125°C			0.22	V
		I_{LOAD} = 500mA	T_J = 25°C		0.12	0.27	V
			T_J = –40°C to 125°C			0.35	V
		I_{LOAD} = 1.5A	T_J = 25°C		0.34	0.45	V
			T_J = –40°C to 125°C			0.55	V
I_{GND} GND pin current, V_{IN} = $V_{OUT\ (NOMINAL)}$ + 1, Legacy Device	I_{LOAD} = 0mA		T_J = –40°C to 125°C		1	1.5	mA
	I_{LOAD} = 1mA				1.1	1.6	mA
	I_{LOAD} = 100mA				3.8	5.5	mA
	I_{LOAD} = 500mA				15	25	mA
	I_{LOAD} = 1.5A				80	120	mA
I_{GND} GND pin current, V_{IN} = $V_{OUT\ (NOMINAL)}$ + 1, New Device	I_{LOAD} = 0A		T_J = –40°C to 125°C			1.2	mA
	I_{LOAD} = 1mA					1.2	mA
	I_{LOAD} = 100mA					1.2	mA
	I_{LOAD} = 500mA					1.2	mA
	I_{LOAD} = 1.5A					1.25	mA
e_N Output voltage noise, Legacy device	C_{OUT} = 10µF, I_{LOAD} = 1.5A, B_W = 10Hz to 100kHz, V_{OUT} = V_{ADJ}		T_J = 25°C		14		μV_{RMS}
e_N Output voltage noise, New Chip	C_{OUT} = 10µF, I_{LOAD} = 1.5A, B_W = 10Hz to 100kHz, V_{OUT} = V_{ADJ}		T_J = 25°C		23		μV_{RMS}
I_{ADJ} ADJ pin bias current			T_J = 25°C		3	10	µA
Shutdown threshold	V_{OUT} = OFF to ON		T_J = –40°C to 125°C		0.9	2	V
	V_{OUT} = ON to OFF			0.25	0.75		V
I_{SHDN} SHDN pin current	V_{SHDN} = 0V		T_J = 25°C		0.01	1	µA
	V_{SHDN} = 20V				3	30	µA
$I_{Q\ SHDN}$ Quiescent current in shutdown, Legacy Device	V_{IN} = 6V, V_{SHDN} = 0V		T_J = 25°C		0.01	1	µA
$I_{Q\ SHDN}$ Quiescent current in shutdown, New Chip	V_{IN} = 6V, V_{SHDN} = 0V		T_J = 25°C			1.5	µA
Ripple Rejection, Legacy Chip	V_{IN} - V_{OUT} = 1.5V (avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 0.75A	V_{IN} - V_{OUT} = 1.5V (avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 0.75A	T_J = 25°C	55	63		dB
Ripple Rejection, New Chip	V_{IN} - V_{OUT} = 1.5V (avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 0.75A		T_J = 25°C	53	60		dB
I_{LIMIT} Current Limit, Legacy Device	V_{IN} = 7V, V_{OUT} = 0V		T_J = 25°C		2		A
	V_{IN} = $V_{OUT(NOMINAL)}$ + 1V		T_J = –40°C to 125°C	1.6			A

5.5 Electrical Characteristics: TL1963A (for DCQ, KTT package) (continued)

Specified at V_{IN} = V_{OUT} + 1V, V_{EN} = 5V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{IN} = 1µF and T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
I_{LIMIT} Current Limit, New Chip	V_{OUT} forced at 0.9*$V_{OUT\ (NOMINAL)}$		T_J = 25°C		2		A
I_{LIMIT} Current Limit, New Chip			T_J = –40°C to 125°C	1.6			A
I_{IL} Input reverse leakage current, Legacy Device	V_{IN} = -20V, V_{OUT} = 0V		T_J = –40°C to 125°C			1	µA
I_{RO} Reverse output current, Legacy Device	TL1963A-15	V_{OUT} = 1.5V, V_{IN} < 1.5V	T_J = 25°C		600	1200	µA
I_{RO} Reverse output current, Legacy Device	TL1963A-25	V_{OUT} = 2.5V, V_{IN} < 2.5V	T_J = 25°C		600	1200	µA
I_{RO} Reverse output current, Legacy Device	TL1963A-18	V_{OUT} = 1.8V, V_{IN} < 1.8V	T_J = 25°C		600	1200	µA
	TL1963A-33	V_{OUT} = 3.3V, V_{IN} < 3.3V			600	1200	µA
	TL1963A	V_{OUT} = 1.21V, V_{IN} < 1.21V			300	600	µA
$I_{RC\ (Steady\ State)}$, New Chip	Steady State reverse current	V_{OUT} = 7V, V_{IN} = 2.4V	T_J = –40°C to 125°C			250	µA
I_R, New Chip	Reverse current detection	V_{OUT} – V_{IN} at which reverse current is detected, and protection kicks in, with V_{OUT} rising, V_{IN} = 6V	T_J = –40°C to 125°C		25		mV
I_R, New Chip	Reverse current protection response time	V_{IN} = 6V, V_{OUT} rising, V_{OUT} - V_{IN} = 300mV	T_J = –40°C to 125°C		5		µS
T_{SD+}	Thermal shutdown temperature increasing			150	161		°C
$T_{SD–}$	Thermal shutdown temperature decreasing			130	141		°C

5.6 Electrical Characteristics: TL1963A (for DCY Package)

Specified at V_{IN} = V_{OUT} + 1V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{IN} = 1µF and T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
V_{IN} Minimum Input Voltage, Legacy Device	I_{LOAD} = 0.5A		T_J = 25°C		1.9		V
	I_{LOAD} = 1.5A		T_J = –40°C to 125°C		2.1	2.5	V
V_{IN} Minimum Input Voltage, New Chip	I_{LOAD} = 0.5A		T_J = 25°C			2.4	V
	I_{LOAD} = 1.5A		T_J = –40°C to 125°C			2.4	V
$V_{UVLO\ (RISING)}$, New Chip	V_{IN} rising, I_{OUT} = 10mA		T_J = –40°C to 125°C	2	2.2	2.3	V
$V_{UVLO\ (FALLING)}$, New Chip	V_{IN} falling, I_{OUT} = 10mA		T_J = –40°C to 125°C	1.85	2.05	2.15	V
$V_{UVLO\ (HYST)}$, New Chip			T_J = –40°C to 125°C		150		mV
V_{OUT} Regulated output voltage, Legacy Device	TL1963A-18	V_{IN} = 2.3V, I_{LOAD} = 1mA	T_J = 25°C	1.773	1.8	1.827	V
		V_{IN} = 2.8V to 20V, I_{LOAD} = 1mA to 1.5A	T_J = –40°C to 125°C	1.737	1.8	1.854	V
	TL1963A-33	V_{IN} = 3.8V, I_{LOAD} = 1mA	T_J = 25°C	3.25	3.3	3.35	V
		V_{IN} = 4.3V to 20V, I_{LOAD} = 1mA to 1.5A	T_J = –40°C to 125°C	3.2	3.3	3.4	V

5.6 Electrical Characteristics: TL1963A (for DCY Package) (continued)

Specified at V_{IN} = V_{OUT} + 1V, I_{OUT} = 1mA, C_{OUT} = 10μF, C_{IN} = 1μF and T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
V_{OUT} Regulated output voltage, New Chip, DCY Package	TL1963A-18	V_{IN} = 2.4V, I_{LOAD} = 1mA	T_J = 25°C	1.77	1.8	1.836	V
		V_{IN} = 2.8V to 20V, I_{LOAD} = 1mA to 1.5A	T_J = –40°C to 125°C	1.764	1.8	1.854	V
	TL1963A-33	V_{IN} = 3.8V, I_{LOAD} = 1mA	T_J = 25°C	3.246	3.3	3.37	V
		V_{IN} = 4.3V to 20V, I_{LOAD} = 1mA to 1.5A	T_J = –40°C to 125°C	3.234	3.3	3.4	V
Line Regulation, Legacy Device	TL1963A-18	ΔV_{IN} = 2.3V to 20V, I_{LOAD} = 1mA	T_J = –40°C to 125°C		2.5	7	mV
	TL1963A-33	ΔV_{IN} = 3.8V to 20V, I_{LOAD} = 1mA	T_J = –40°C to 125°C		3.5	10	mV
Line Regulation, New Chip	TL1963A-18	ΔV_{IN} = 2.4V to 10V, I_{LOAD} = 1mA	T_J = –40°C to 125°C		0.25	1.2	mV
		ΔV_{IN} = 2.4V to 20V, I_{LOAD} = 1mA	T_J = –40°C to 125°C		4.5	6	mV
	TL1963A-33	ΔV_{IN} = 3.8V to 10V, I_{LOAD} = 1mA	T_J = –40°C to 125°C		0.35	1.65	mV
		ΔV_{IN} = 3.8V to 20V, I_{LOAD} = 1mA	T_J = –40°C to 125°C		7.5	11.55	mV
Load Regulation, Legacy Device	TL1963A-18	V_{IN} = 2.8V, ΔI_{LOAD} = 1mA to 1.5A	T_J = 25°C		2	10	mV
			T_J = –40°C to 125°C			20	mV
	TL1963A-33	V_{IN} = 4.3V, ΔI_{LOAD} = 1mA to 1.5A	T_J = 25°C		3	20	mV
			T_J = –40°C to 125°C			70	mV
Load Regulation, New Chip, DCY Package	TL1963A-18	V_{IN} = 2.8V, ΔI_{LOAD} = 1mA to 1.5A	T_J = 25°C		1.0	1.8	mV
		V_{IN} = 2.8V, ΔI_{LOAD} = 1mA to 1.5A	T_J = –40°C to 125°C			2.4	mV
	TL1963A-33	V_{IN} = 4.3V, ΔI_{LOAD} = 1mA to 1.5A	T_J = 25°C		1.2	2.5	mV
		V_{IN} = 4.3V, ΔI_{LOAD} = 1mA to 1.5A	T_J = –40°C to 125°C			3.3	mV
V_{DO} Dropout voltage	TL1963A-33: V_{IN} = 3.3V	I_{LOAD} = 1mA	T_J = 25°C		0.002	0.005	V
			T_J = –40°C to 125°C			0.007	V
		I_{LOAD} = 100mA	T_J = 25°C		0.022	0.027	V
			T_J = –40°C to 125°C			0.036	V
		I_{LOAD} = 500mA	T_J = 25°C		0.12	0.13	V
			T_J = –40°C to 125°C			0.18	V
		I_{LOAD} = 1.5A	T_J = 25°C		0.34	0.40	V
			T_J = –40°C to 125°C			0.53	V

5.6 Electrical Characteristics: TL1963A (for DCY Package) (continued)

Specified at V_{IN} = V_{OUT} + 1V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{IN} = 1µF and T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
I_{GND} GND pin current, V_{IN} = $V_{OUT\ (NOMINAL)}$ + 1, Legacy Device	I_{LOAD} = 0mA		T_J = –40°C to 125°C		1	1.5	mA
	I_{LOAD} = 1mA		T_J = –40°C to 125°C		1.1	1.6	mA
	I_{LOAD} = 100mA		T_J = –40°C to 125°C		3.8	5.5	mA
	I_{LOAD} = 500mA		T_J = –40°C to 125°C		15	25	mA
	I_{LOAD} = 1.5A		T_J = –40°C to 125°C		80	120	mA
I_{GND} GND pin current, V_{IN} = $V_{OUT\ (NOMINAL)}$ + 1, New Device	I_{LOAD} = 0A		T_J = –40°C to 125°C			1.1	mA
	I_{LOAD} = 1mA		T_J = –40°C to 125°C			1.1	mA
	I_{LOAD} = 100mA		T_J = –40°C to 125°C			1.1	mA
	I_{LOAD} = 500mA		T_J = –40°C to 125°C			1.1	mA
	I_{LOAD} = 1.5A		T_J = –40°C to 125°C			1.1	mA
e_N Output voltage noise, Legacy device	C_{OUT} = 10µF, I_{LOAD} = 1.5A, B_W = 10Hz to 100kHz, V_{OUT} = V_{ADJ}		T_J = 25°C		14		μV_{RMS}
e_N Output voltage noise, New Chip	C_{OUT} = 10µF, I_{LOAD} = 1.5A, B_W = 10Hz to 100kHz, V_{OUT} = V_{ADJ}		T_J = 25°C		23		μV_{RMS}
Ripple Rejection, Legacy Device	V_{IN} - V_{OUT} = 1.5V (avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 0.75A	V_{IN} - V_{OUT} = 1.5V (avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 0.75A	T_J = 25°C	55	63		dB
Ripple Rejection, New Chip	V_{IN} - V_{OUT} = 1.5V (avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 0.75A		T_J = 25°C	53	60		dB
I_{LIMIT} Current Limit, Legacy Device	V_{IN} = 7V, V_{OUT} = 0V		T_J = 25°C		2		A
	V_{IN} = $V_{OUT\ (NOMINAL)}$ + 1		T_J = –40°C to 125°C	1.6			A
I_{LIMIT} Current Limit, New Chip	V_{OUT} forced at 0.9 × $V_{OUT\ (NOMINAL)}$		T_J = 25°C		2.2		A
			T_J = –40°C to 125°C	1.65		2.75	A
I_{IL} Input reverse leakage current, Legacy Device	V_{IN} = -20V, V_{OUT} = 0V		T_J = –40°C to 125°C			1	µA
I_{RO} Reverse output current, Legacy Device	TL1963A-15	V_{OUT} = 1.5V, V_{IN} < 1.5V	T_J = 25°C		600	1200	µA
I_{RO} Reverse output current, Legacy Device	TL1963A-25	V_{OUT} = 2.5V, V_{IN} < 2.5V	T_J = 25°C		600	1200	µA
I_{RO} Reverse output current, Legacy Device	TL1963A-18	V_{OUT} = 1.8V, V_{IN} < 1.8V	T_J = 25°C		600	1200	µA
	TL1963A-33	V_{OUT} = 3.3V, V_{IN} < 3.3V	T_J = 25°C		600	1200	µA
I_R (Steady State), New Chip	Reverse Current at V_{IN}	V_{IN} = 0V, V_{OUT} ≤ 7V	T_J = –40°C to 125°C			10	µA
I_R, New Chip	Reverse current detection	V_{OUT} – V_{IN} at which reverse current is detected, and protection kicks in, with V_{OUT} rising, V_{IN} = 6V	T_J = –40°C to 125°C		25		mV

5.6 Electrical Characteristics: TL1963A (for DCY Package) (continued)

Specified at V_{IN} = V_{OUT} + 1V, I_{OUT} = 1mA, C_{OUT} = 10μF, C_{IN} = 1μF and T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
I_R, New Chip	Reverse current protection response time	V_{IN} = 6V, V_{OUT} rising, , V_{OUT} - V_{IN} = 300mV	T_J = –40°C to 125°C		5		μS
T_{SD+}	Thermal shutdown temperature increasing			150	161		°C
$T_{SD–}$	Thermal shutdown temperature decreasing			130	141		°C

5.7 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or 2.4V (whichever is greater), I_{OUT} = 1mA, C_{IN} = 10µF, and C_{OUT} = 10µF (unless otherwise noted).

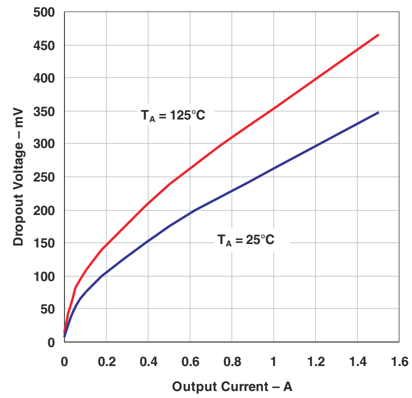


Figure 5-1. Dropout Voltage vs Output Current (Legacy Chip)

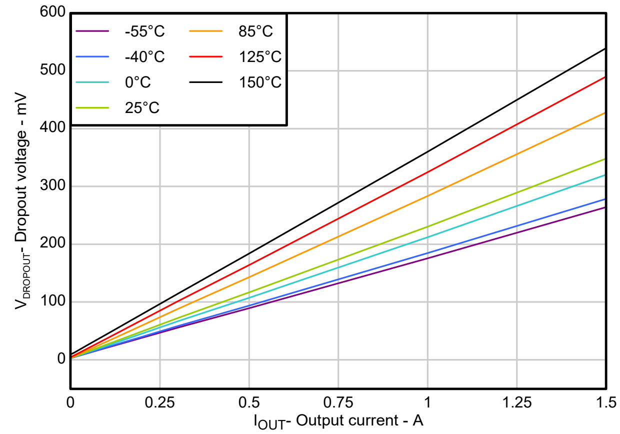


Figure 5-2. Dropout Voltage vs Output Current (New Chip)

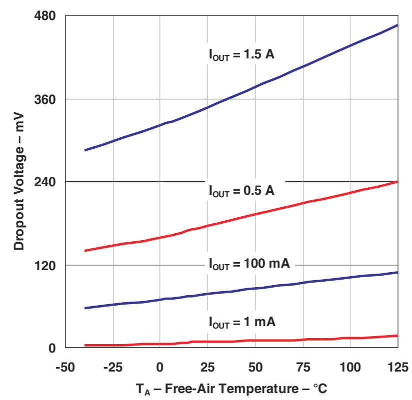
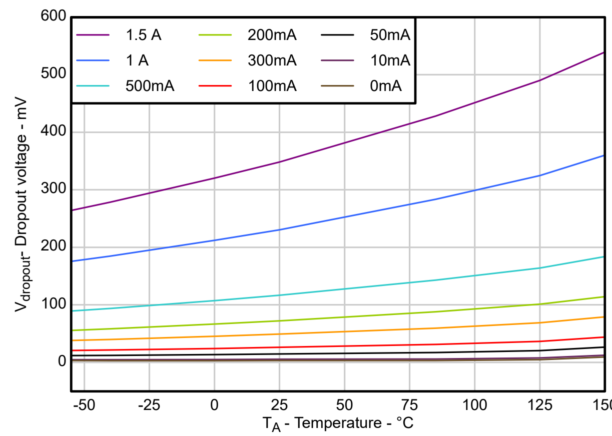


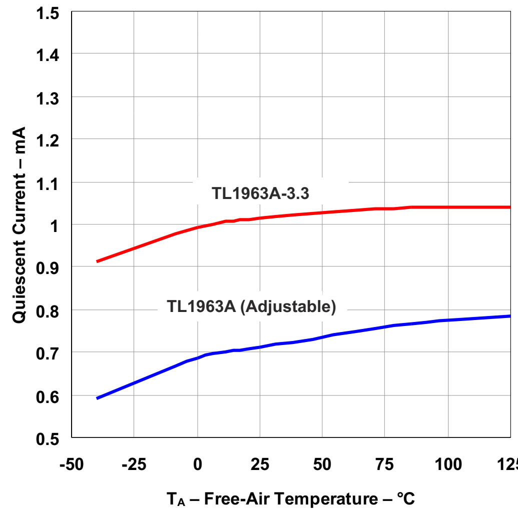
Figure 5-3. Dropout Voltage vs Temperature (Legacy Chip)



For TL1963A-3.3

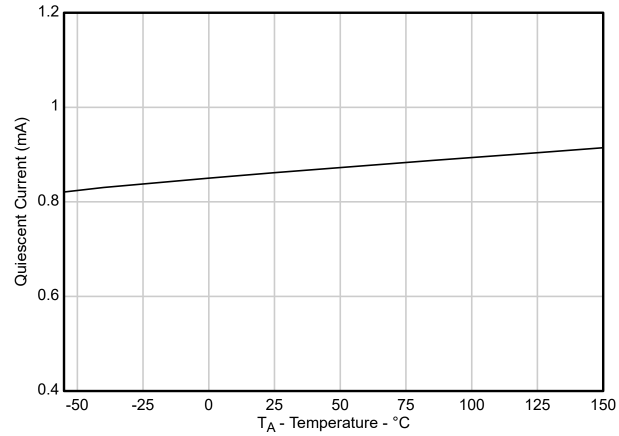
(V_{OUT} = 3.3V)

Figure 5-4. Dropout Voltage vs Temperature (New Chip)



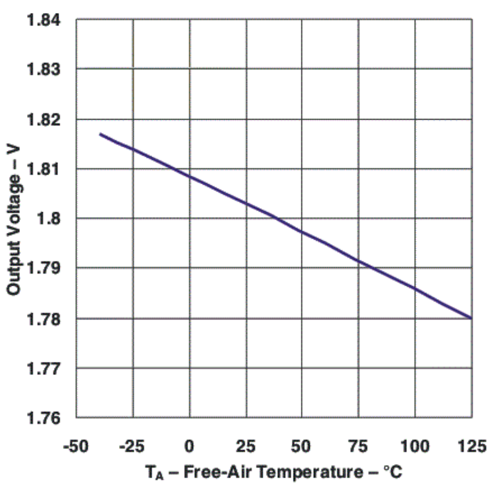
V_{IN} = 6V I_{OUT} = 0A V_{SHDN} = VIN

Figure 5-5. Quiescent Current vs Temperature (Legacy Chip)



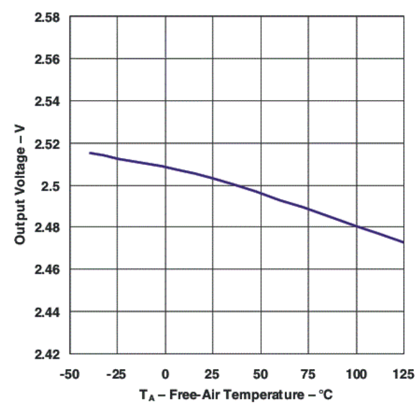
TL1963A-3.3 (V_{OUT} = 3.3V) I_{OUT} = 0A

Figure 5-6. Quiescent Current vs Temperature vs Temperature (New Chip)



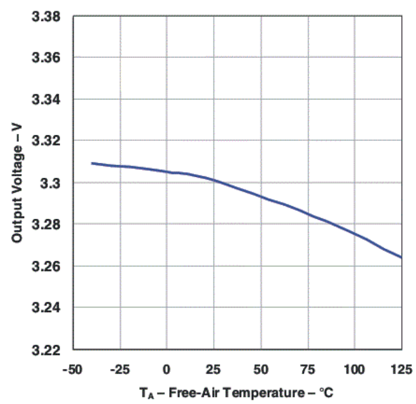
I_{OUT} = 1mA TL1963A-18

Figure 5-7. TL1963A-18 Output Voltage vs Temperature (Legacy Chip)



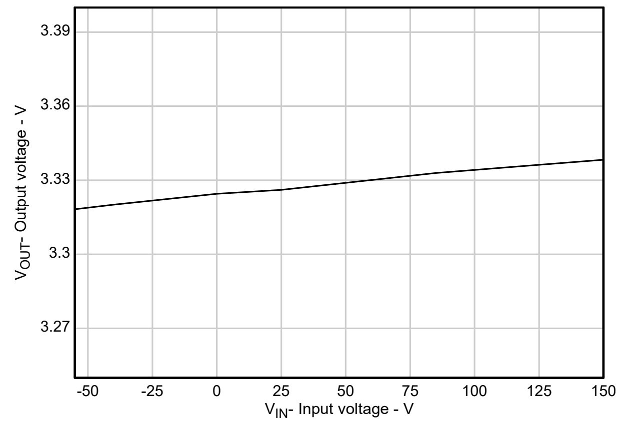
I_{OUT} = 1mA TL1963A-25

Figure 5-8. TL1963A-25 Output Voltage vs Temperature (Legacy Chip)



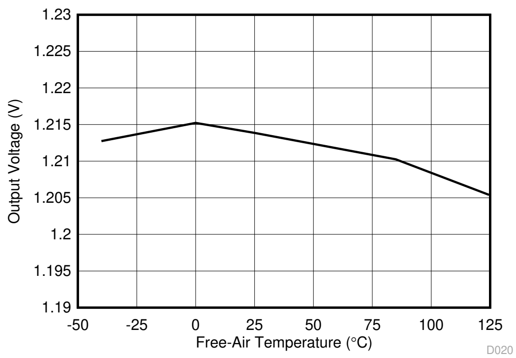
I_{OUT} = 1mA TL1963A-33

Figure 5-9. TL1963A-33 Output Voltage vs Temperature (Legacy Chip)



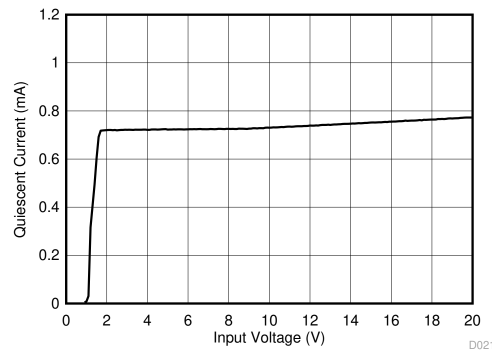
I_{OUT} = 1mA TL1963A-33

Figure 5-10. TL1963A-33 Output Voltage vs Temperature (New Chip)



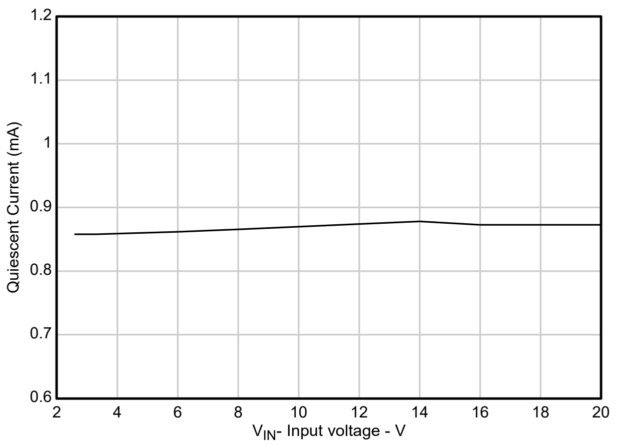
I_{OUT} = 1mA V_{IN} = 6V

Figure 5-11. TL1963A Output Voltage vs Temperature (Legacy Chip)



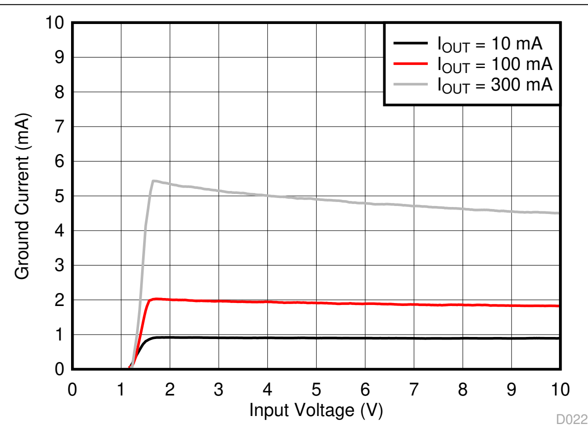
T_J = 25°C R_{OUT} = 4.3kΩ V_{SHDN} = V_{IN}

Figure 5-12. Quiescent Current vs Input Voltage (Legacy Chip)



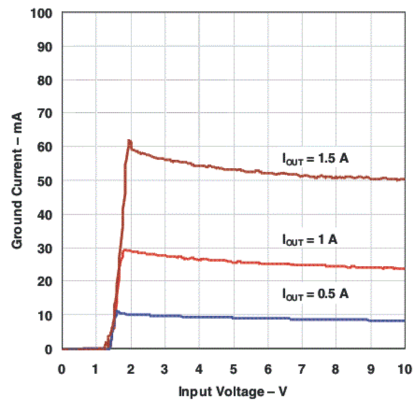
T_J = 25°C R_{OUT} = 4.3kΩ V_{SHDN} = V_{IN}

Figure 5-13. Quiescent Current vs Input Voltage (New Chip)



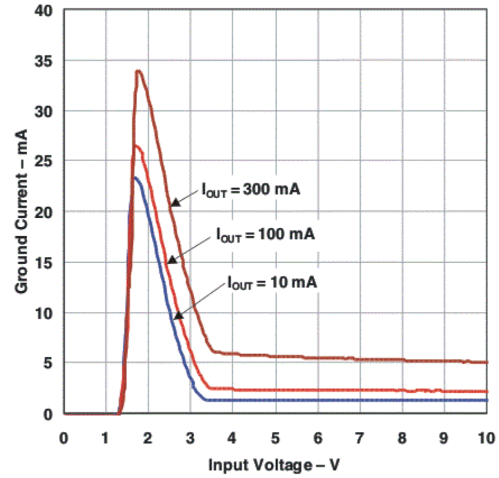
T_J = 25°C V_{OUT} = 1.21V V_{SHDN} = V_{IN}

Figure 5-14. TL1963A Ground Current vs Input Voltage (Legacy Chip)



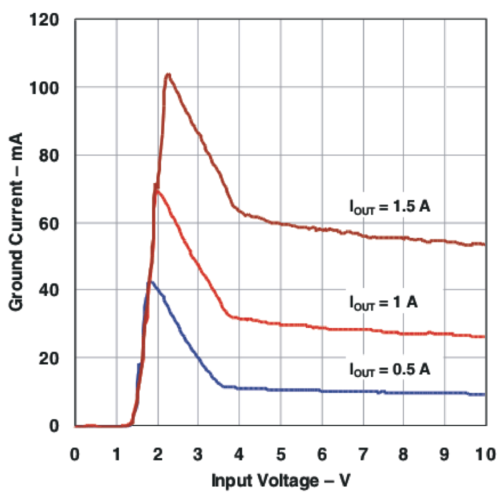
T_J = 25°C V_{OUT} = 1.21V V_{SHDN} = V_{IN}

Figure 5-15. TL1963A Ground Current vs Input Voltage (Legacy Chip)



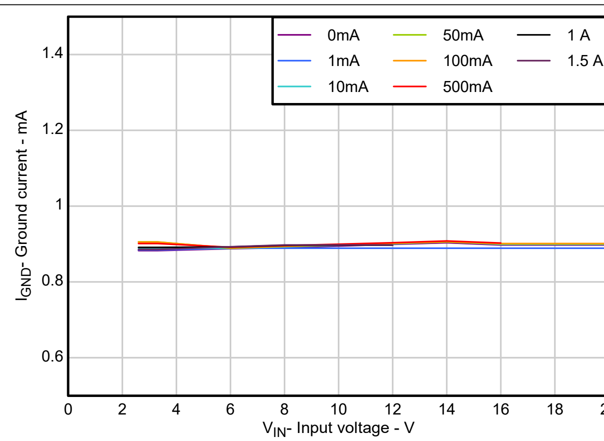
T_J = 25°C V_{SHDN} = V_{IN}

Figure 5-16. TL1963A-33 Ground Current vs Input Voltage (Legacy Chip)



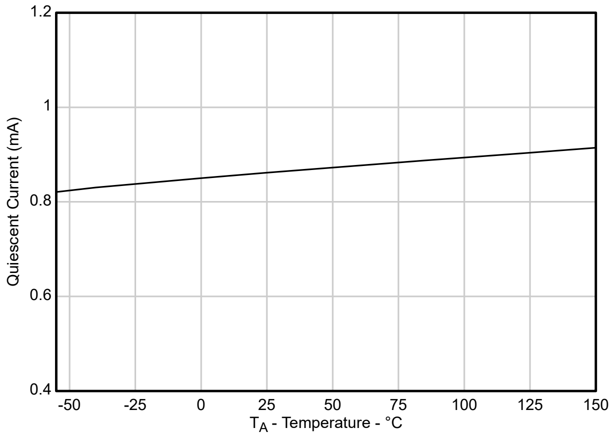
T_J = 25°C V_{SHDN} = V_{IN}

Figure 5-17. TL1963A-33 Ground Current vs Input Voltage (Legacy Chip)



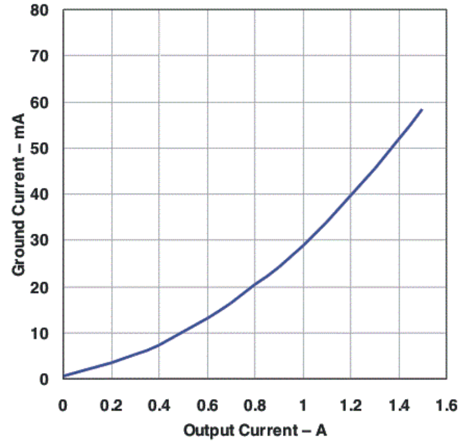
T_J = 25°C V_{SHDN} = V_{IN}

Figure 5-18. TL1963A-33 Ground Current vs Input Voltage (New Chip)



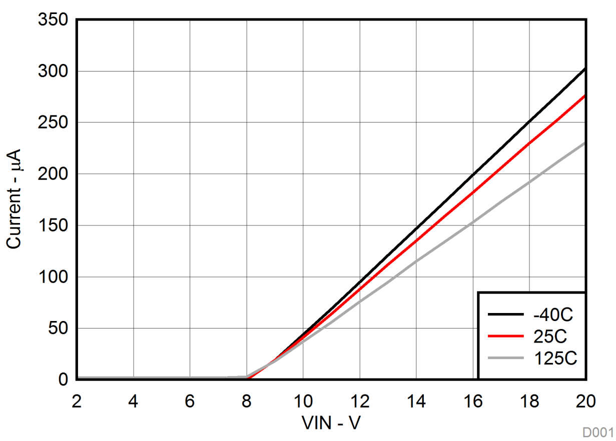
T_J = 25°C V_{SHDN} = V_{IN}

Figure 5-19. TL1963A-33 Quiescent current vs Temperature (New Chip)



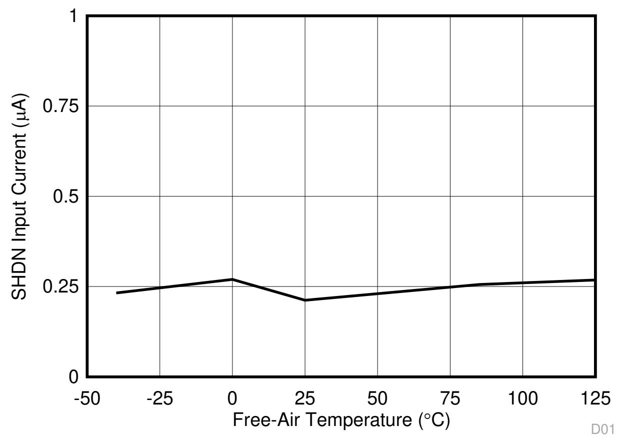
V_{IN} = V_{OUT}(nom) + 1

Figure 5-20. Ground Current vs Output Current (Legacy Chip)



V_{SHDN} = 0V

Figure 5-21. Quiescent Current in Shutdown vs Input Voltage (Legacy Chip)



V_{SHON} = 0V

Figure 5-22. $\overline{SHDN}$ Pin Current (I_{SHDN}) vs Temperature (Legacy Chip)

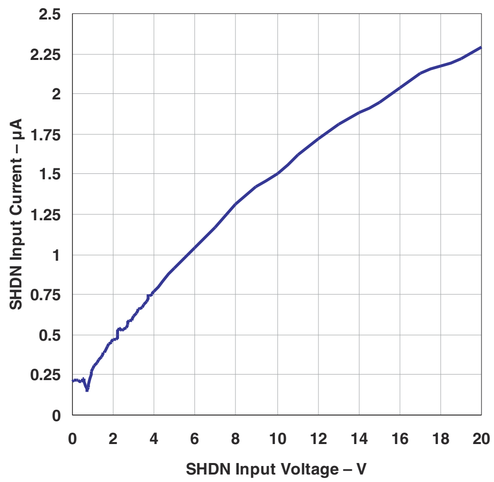
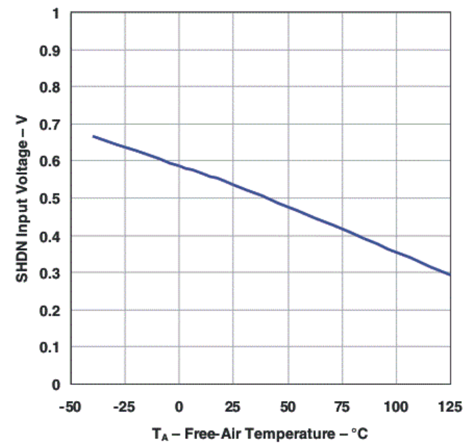
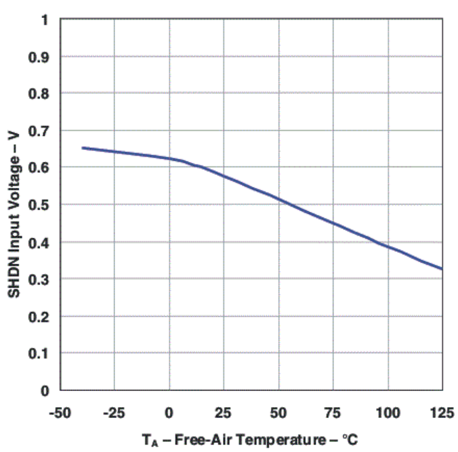


Figure 5-23. $\overline{\text{SHDN}}$ Pin Current (I_{SHDN}) vs $\overline{\text{SHDN}}$ Input Voltage (Legacy Chip)



I_{OUT} = 1mA

Figure 5-24. $\overline{\text{SHDN}}$ Threshold (OFF to ON) vs Temperature (Legacy Chip)



I_{OUT} = 1mA

Figure 5-25. $\overline{\text{SHDN}}$ Threshold (ON to OFF) vs Temperature (Legacy Chip)

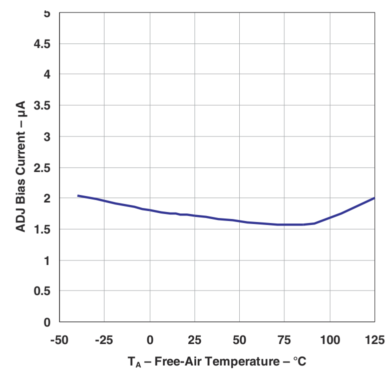
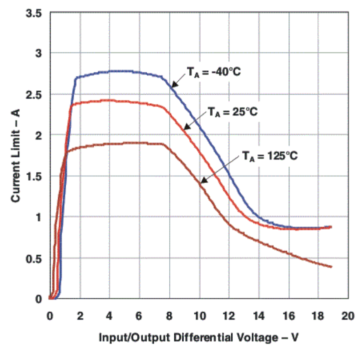
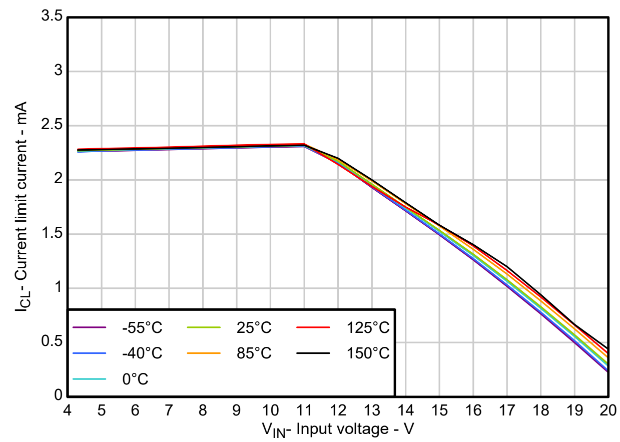


Figure 5-26. ADJ Bias Current vs Temperature (Legacy Chip)



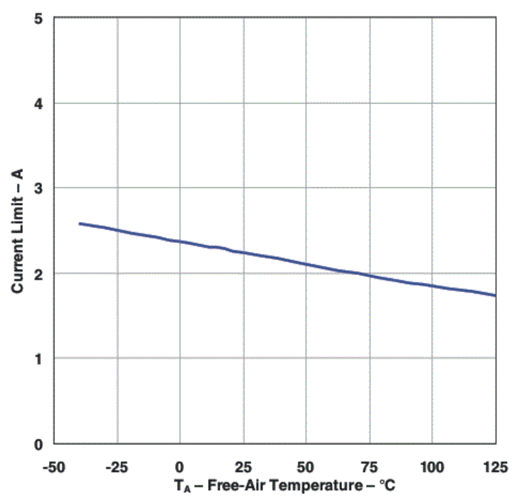
ΔV_{OUT} = 100mV

Figure 5-27. Current Limit vs Input-to-Output Differential Voltage (Legacy Chip)



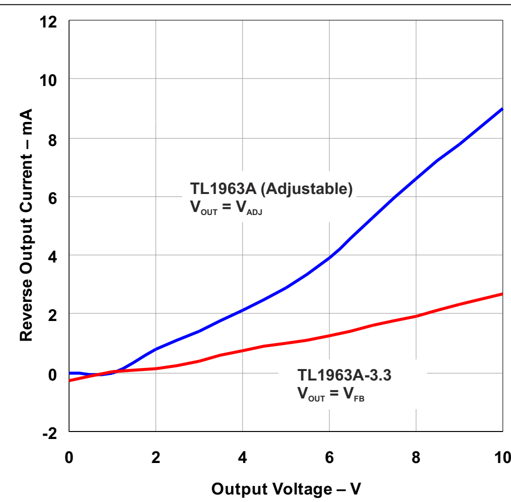
ΔV_{OUT} = 100mV

Figure 5-28. Current Limit vs Input-to-Output Differential Voltage (New Chip)



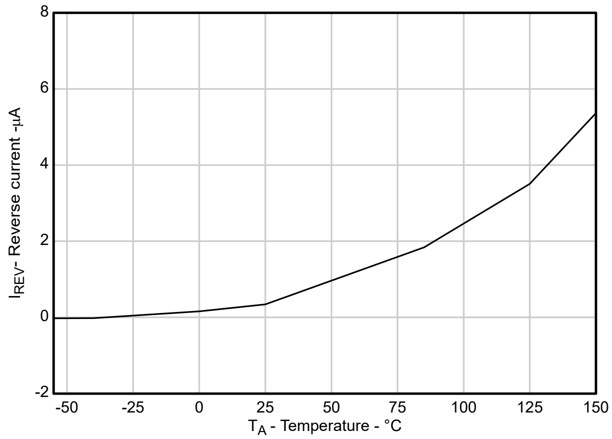
V_{IN} = 7V V_{OUT} = 0V

Figure 5-29. Current Limit vs Temperature (Legacy Chip)



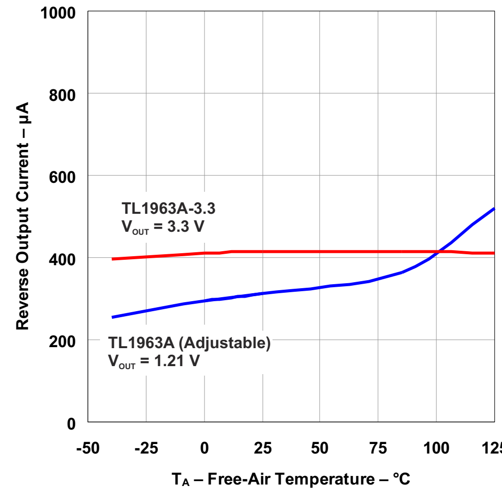
T_J = 25°C V_{IN} = 0V
Current flows into OUT pin

Figure 5-30. Reverse Output Current vs Output Voltage (Legacy Chip)



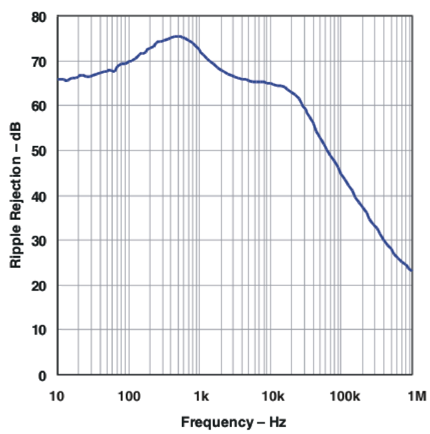
T_J = 25°C V_{IN} = 0V
Current flows into OUT pin

Figure 5-31. Reverse Output Current vs Temperature (New Chip)



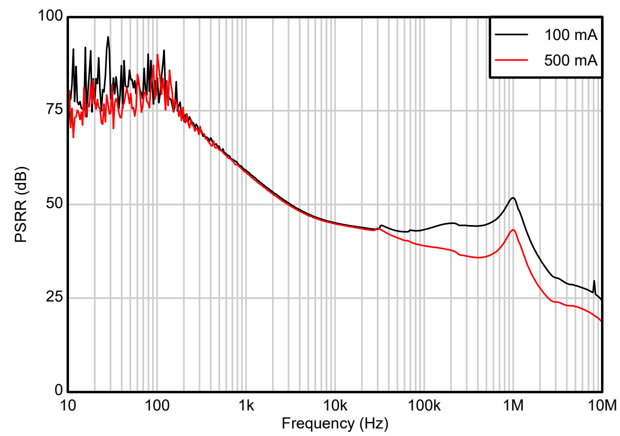
V_{IN} = 0V

Figure 5-32. Reverse Output Current vs Temperature (Legacy Chip)



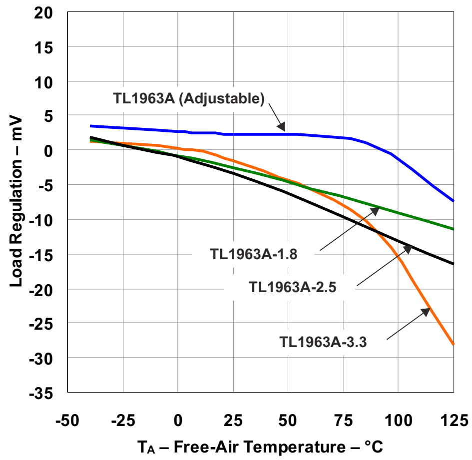
V_{RIPPLE} = 0.05V_{PP} V_{IN} = 2.7V C_{IN} = 0 C_{OUT} = 10µF (ceramic) T_A = 25°C

Figure 5-33. Ripple Rejection vs Frequency (Legacy Chip)



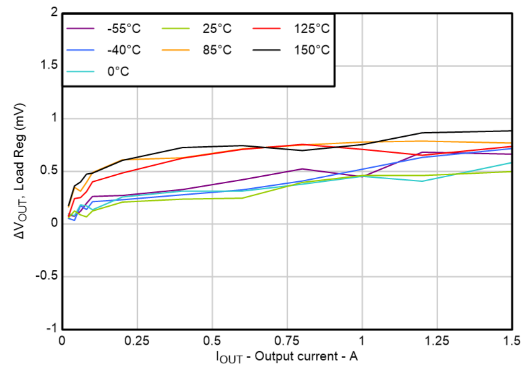
C_{OUT} = 10µF (ceramic) V_{IN} = 4.3V, V_{OUT} = 3.3V

Figure 5-34. Ripple Rejection vs Frequency (New chip)



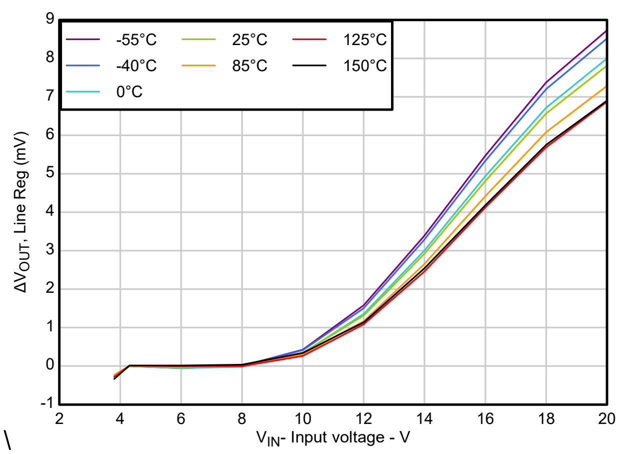
I_{OUT} = 1mA to 1.5A

Figure 5-35. Load Regulation vs Temperature (Legacy Chip)



I_{OUT} = 1mA to 1.5A

Figure 5-36. Load Regulation vs Temperature (New Chip)



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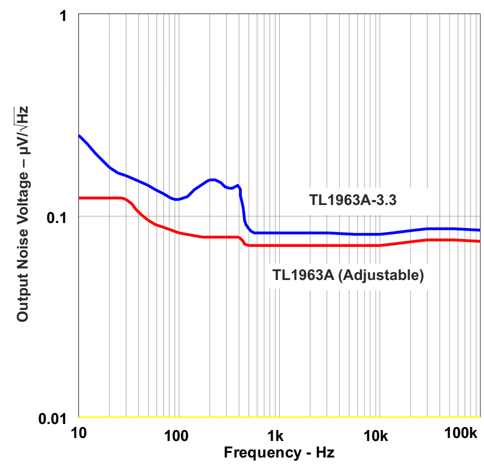
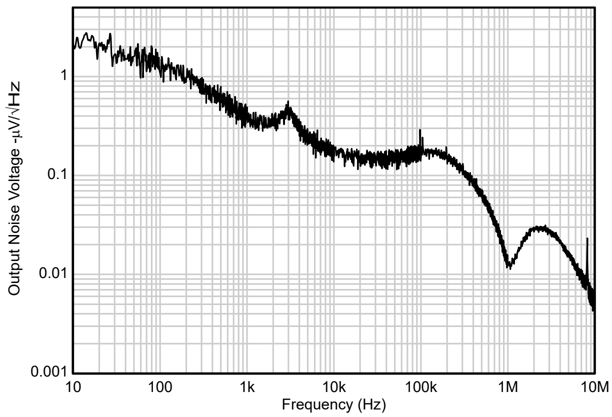
V_{IN} = 2.8V to 20V

Figure 5-37. Line Regulation vs Temperature (New Chip)



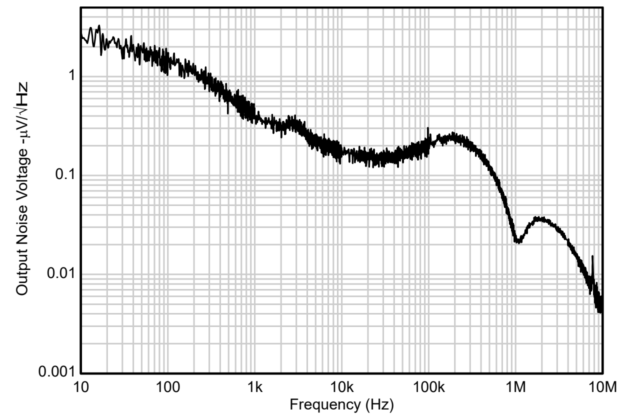
C_{OUT} = 10µF (ceramic)
I_{OUT} = 1.5A

Figure 5-38. Output Noise Voltage vs Frequency (Legacy Chip)



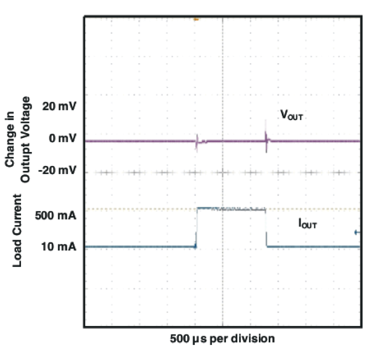
C_{OUT} = 10µF (ceramic) I_{OUT} = 0.3A

Figure 5-39. Output Noise Voltage vs Frequency (New chip)



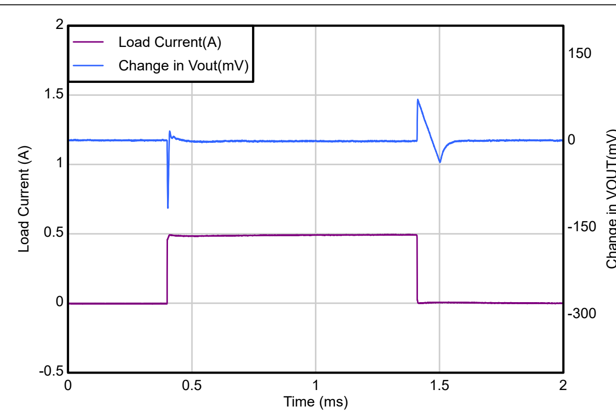
C_{OUT} = 10µF (ceramic) I_{OUT} = 1.5A

Figure 5-40. Output Noise Voltage vs Frequency (New chip)



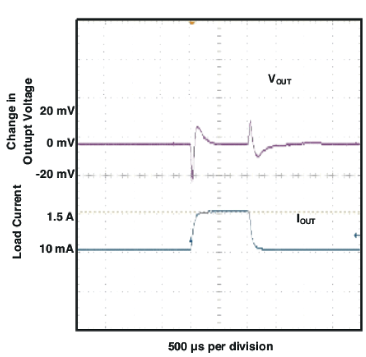
V_{IN} = 4.3V C_{IN} = 10µF
C_{OUT} = 10µF (ceramic)

Figure 5-41. Load Transient Response (Legacy Chip)



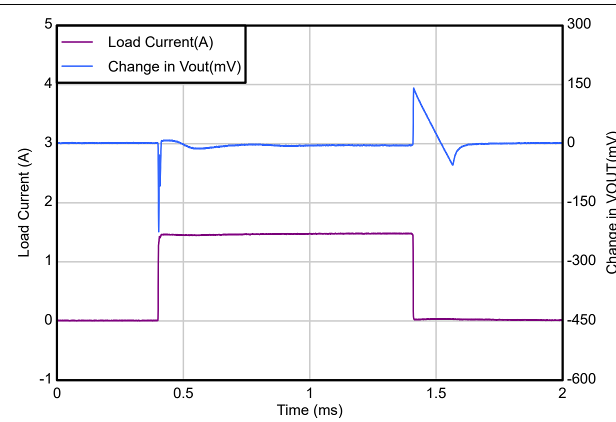
V_{IN} = 4.3V C_{IN} = 10µF
C_{OUT} = 10µF (ceramic)

Figure 5-42. Load Transient Response (New Chip)



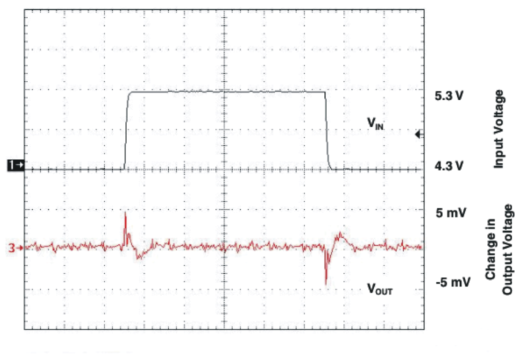
V_{IN} = 4.3V C_{IN} = 10µF
C_{OUT} = 10µF (ceramic)

Figure 5-43. Load Transient Response (Legacy Chip)



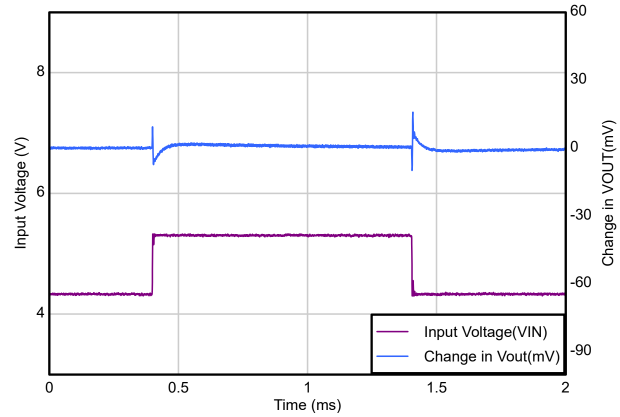
V_{IN} = 4.3V C_{IN} = 10µF
C_{OUT} = 10µF (ceramic)

Figure 5-44. Load Transient Response (New Chip)



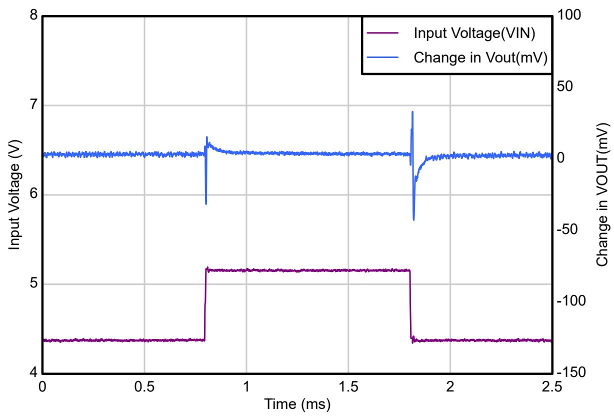
I_{OUT} = 1.5A C_{IN} = 10µF
C_{OUT} = 10µF (ceramic)

Figure 5-45. Line Transient Response (Legacy Chip)



I_{OUT} = 0.3A C_{IN} = 10µF
C_{OUT} = 10µF (ceramic)

Figure 5-46. Line Transient Response (Legacy Chip)



I_{OUT} = 1.5A C_{IN} = 10µF
C_{OUT} = 10µF (ceramic)

Figure 5-47. Line Transient Response (Legacy Chip)

6 Detailed Description

6.1 Overview

The TL1963A-xx series are 1.5A low-dropout regulators optimized for fast transient response. The devices can supply 1.5A of output current with a dropout voltage of 340mV (typical) and supports wide output range (from 1.21V to 20V) in adjustable configuration. Very low dropout, wider output range and fast transient performance makes these devices an excellent choice for supplying power to variety of power-hungry applications. In addition to the low quiescent current, the TL1963A-xx regulators (both legacy and new chip) incorporate several protection features such as over current, over temperature (thermal shutdown) and reverse current protection. In battery-backup applications where the output is held up by a backup battery when the input is pulled to ground, the TL1963A-xx acts as if it has a diode in series with the output and prevents reverse-current flow. The legacy chip of TL1963A-xx also includes reverse-battery protection.

6.2 Functional Block Diagram

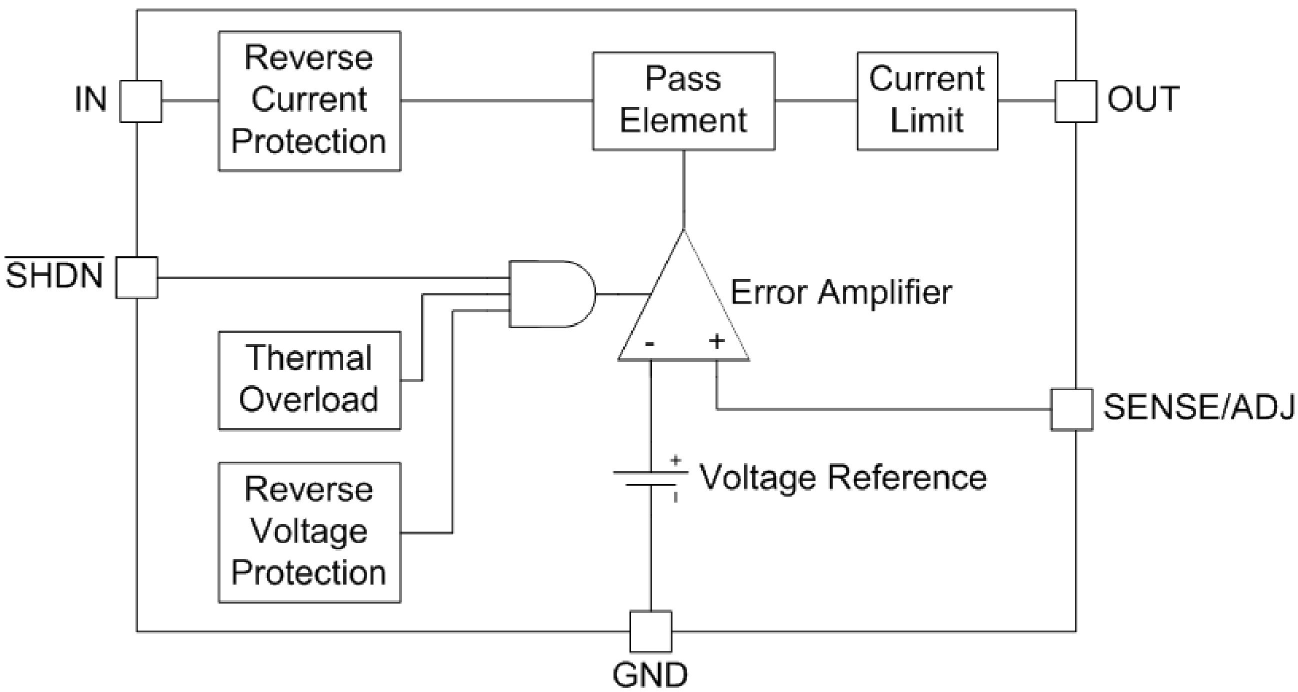


Figure 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 $\overline{\text{SHDN}}$

The $\overline{\text{SHDN}}$ pin for the device is an active-high pin. The output voltage enables when the voltage of the $\overline{\text{SHDN}}$ pin is greater than the high-level input voltage (Shutdown threshold, V_{OUT} = OFF to ON) of the $\overline{\text{SHDN}}$ pin and disabled with the $\overline{\text{SHDN}}$ pin voltage is less than the low-level input voltage (Shutdown threshold, V_{OUT} = ON to OFF) of the $\overline{\text{SHDN}}$ pin. The *Electrical Characteristics: TL1963A (for DCQ, KTT package)* lists the high and low thresholds. If independent control of the output voltage is not needed, connect the $\overline{\text{SHDN}}$ pin to the input of the device.

The $\overline{\text{SHDN}}$ pin can be driven either by 5V logic or open-collector logic with a pullup resistor. The pullup resistor is required to supply the pullup current of the open-collector gate, and the $\overline{\text{SHDN}}$ pin current, listed in the *Electrical Characteristics: TL1963A (for DCQ, KTT package)*. The $\overline{\text{SHDN}}$ pin also has a weak internal pull-down and the device disables when $\overline{\text{SHDN}}$ pin is not connected or floating.

6.3.2 Dropout Voltage

The definition of dropout voltage (V_{DO}) is the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor determines the dropout voltage. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.3 Undervoltage Lockout

For the new chip version, TL1963A-xx device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has in-built hysteresis. The *Electrical Characteristics: TL1963A (for DCY Package)/Electrical Characteristics: TL1963A (for DCQ, KTT package)* table specifies the UVLO limits ($V_{UVLO(RISING)}$ and $V_{UVLO(FALLING)}$).

6.3.4 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to T_{SD+} (typical). Thermal shutdown hysteresis verifies that the device resets (turns on) when the temperature falls to T_{SD-} (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed the operational specifications. Although the design of the internal protection circuitry protects against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.3.5 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{LIMIT}). *Electrical Characteristics: TL1963A (for DCY Package)/ Electrical Characteristics: TL1963A (for DCQ, KTT package)* lists I_{LIMIT}.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{LIMIT}]. If thermal shutdown triggers, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Current Limit shows a diagram of the foldback current limit.

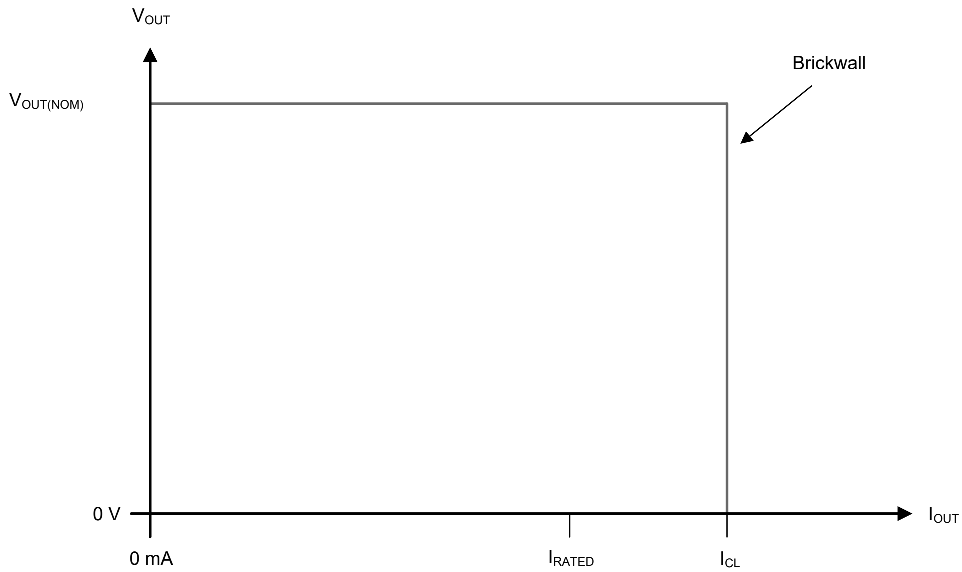


Figure 6-2. Current Limit

The TL1963A-xx devices also have an internal over-power limit circuit that limits the power dissipated across the LDO with-in the internal SOA (safe operating area) limits. The SOA limits for the LDO factors in safe operation for both silicon components, and bondwires used in packaging. These limits verify reliable operation of the device and prevent the device failure from overheating, breakdown, or other damaging effects. For more details, see the Overload Recovery.

6.3.6 Overload Recovery

Like many IC power regulators, the TL1963A-xx has safe operating area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The design of the protection provides some output current at all values of input-to-output voltage up to the device breakdown.

The voltage drop across LDO (V_{IN} - V_{OUT}) and load current (I_L) flowing through define the power dissipated (P_{Dissip}) across the LDO.

$$P_{Dissip} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

The power limiting circuit, monitors both the voltage drop (headroom, V_{IN} - V_{OUT}) across LDO and output load current (I_{OUT}) flowing through. If P_{Dissip} crosses the defined SOA limits, the power limiting circuit, limits the load current (I_{OUT}) flowing through.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so it is not unique to the TL1963A-xx.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after the removal of a short circuit or when the shutdown pin is pulled high after the input voltage has already been turned on. The load line for such a load can intersect the output current curve at two points. If this occurs, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

6.3.7 Output Voltage Noise

The design of the TL1963A-xx regulators provide low output voltage noise over the 10Hz to 100kHz bandwidth while operating at full load. For the legacy chip, output voltage noise is typically $35nV/\sqrt{Hz}$ over this frequency bandwidth for the TL1963A (adjustable version). For higher output voltages (generated by using a resistor divider), the output voltage noise accordingly gains up. This results in RMS noise over the 10Hz to 100kHz bandwidth of $14\mu V_{RMS}$ for the TL1963A (adjustable configuration), increasing to $38\mu V_{RMS}$ for the TL1963A-33 for legacy chip and $23\mu V_{RMS}$ for the TL1963A (adjustable configuration) for new chip.

Measure the higher values of output voltage noise when care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the TL1963A-xx. Consider the power-supply ripple rejection. The TL1963A-xx regulators do not have unlimited power-supply rejection and pass a small portion of the input noise through to the output.

6.3.8 Protection Features

The TL1963A-xx regulators incorporate several protection features which make the regulators an excellent choice for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, ***the legacy chip version*** of the devices are protected against reverse input voltages, and reverse output voltages. Both legacy chip and new chip version of the devices also support reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature must not exceed 125°C.

6.3.8.1 For Legacy Chip Only

The input of the device withstands reverse voltages of 20V. Current flow into the device is limited to less than 1 mA (typically less than 100 µA), and no negative voltage appears at the output. The device protects both itself and the load. This provides protection against batteries that can be plugged in backward.

The output of the TL1963A-xx can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20V. For fixed voltage versions, the output acts like a large resistor, typically 5kΩ or higher, limiting current flow to typically less than 600µA. For adjustable versions, the output acts like an open circuit; no current flows out of the pin. If the input is powered by a voltage source, the output sources the short-circuit current of the device and protects itself by thermal limiting. In this case, grounding the $\overline{SHDN}$ pin turns off the device and stops the output from sourcing the short-circuit current.

The ADJ pin of the adjustable device can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open circuit or grounded, the ADJ pin acts like an open circuit when pulled below ground and like a large resistor (typically 5 kΩ) in series with a diode when pulled above ground.

In situations where the ADJ pin is connected to a resistor divider that would pull the ADJ pin above its 7V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5 mA. For example, a resistor divider is used to provide a regulated 1.5V output from the 1.21V reference when the output is forced to 20 V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5 mA when the ADJ pin is at 7 V. The 13V difference between OUT and ADJ divided by the 5mA maximum current into the ADJ pin yields a minimum top resistor value of 2.6kΩ.

6.3.8.2 For Both Legacy and New Chip

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage can be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit.

When the IN pin of the TL1963A-xx is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current typically drops to less than 2µA (for legacy chip only). I_{RO} (reverse output current) for legacy chip and $I_{RC(steady\ state)}$ for new chip defines the steady state current that flows in the OUT pin and out of the GND pin, captured in Electrical Characteristics: TL1963A (for DCY Package) table. This can happen if the input of the device connects to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the $\overline{SHDN}$ pin has no effect on the reverse output current when the output is pulled above the input.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics: TL1963A (for DCY Package)*/*Electrical Characteristics: TL1963A (for DCQ, KTT package)* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	$V_{\overline{SHDN}}$ (only for DCQ, KTT)	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{\overline{SHDN}}$ > $\overline{SHDN}$ threshold, V_{OUT} = OFF to ON	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{\overline{SHDN}}$ > $\overline{SHDN}$ threshold, V_{OUT} = OFF to ON	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{\overline{SHDN}}$ < $\overline{SHDN}$ threshold, V_{OUT} = ON to OFF	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is greater than –40°C and less than +125°C
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- For DCQ, KTT package, The $\overline{SHDN}$ voltage has previously exceeded the $\overline{SHDN}$ turning-on threshold voltage and has not yet decreased to less than the $\overline{SHDN}$ turning-off threshold

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.4 Disabled

For DCQ and KTT package, the output of the device can be shutdown by forcing the voltage of the $\overline{SHDN}$ pin to less than the maximum $\overline{SHDN}$ pin turning off input voltage (see the *Electrical Characteristics: TL1963A (for DCQ, KTT package)* table). Also, for all packages DCY, DCQ and KTT in the new cho[, the LDO can also be shutdown by forcing the input to LDO lower than the UVLO threshold. When disabled, the pass transistor is turned off, and internal circuits are also shutdown, reducing the quiescent current consumption.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

7.1.1 Input/Output Capacitance and Transient Response

The design of the TL1963A-xx regulators establish stability with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. TI recommends a minimum output capacitor of 10μF with an ESR of 3Ω or less to prevent oscillations. Larger values of output capacitance can decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TL1963A-xx, increase the effective output capacitor value.

Give extra consideration when using ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior overtemperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients. When used with a 5V regulator, a 10μF Y5V capacitor can exhibit an effective value as low as 1μF to 2μF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more appropriate for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

7.1.2 Reverse Current

The TL1963A-xx has integrated reverse current protection. Reverse current protection prevents the flow of current from the OUT pin to the IN pin when output voltage is higher than input voltage. It can happen in scenarios when the output voltage is held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit. The reverse current protection circuitry places the power path in high impedance when the output voltage is higher than the input voltage. This setting reduces leakage current from the output to the input. The reverse current protection is always active regardless of the $\overline{\text{SHDN}}$ pin logic state or if the OUT pin voltage is greater than 1.8V (for legacy chip only). I_{RO} (reverse output current) for legacy chip and $I_{RC(steady\ state)}$ for new chip defines the steady state current that flows in the OUT pin and out of the GND pin, captured in *Electrical Characteristics: TL1963A (for DCY Package)*/*Electrical Characteristics: TL1963A (for DCQ, KTT package)* table.

7.1.3 Feed-Forward Capacitor

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can connect from the OUT pin to the ADJ pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. The *Recommended Operating Conditions* table lists the recommended C_{FF} values. When using a higher capacitance C_{FF}, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, while C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. Calculate the C_{FF} zero and pole frequencies from the following equations:

$$f_Z = \frac{1}{[2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)]} \tag{3}$$

$$f_P = \frac{1}{[2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)]} \tag{4}$$

7.1.4 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \Psi_{JT} \times P_D \tag{5}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \Psi_{JB} \times P_D \tag{6}$$

where

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.1.5 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{7}$$

Note

The correct selection of the system voltage rails can minimize power dissipation and therefore achieve greater efficiency. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

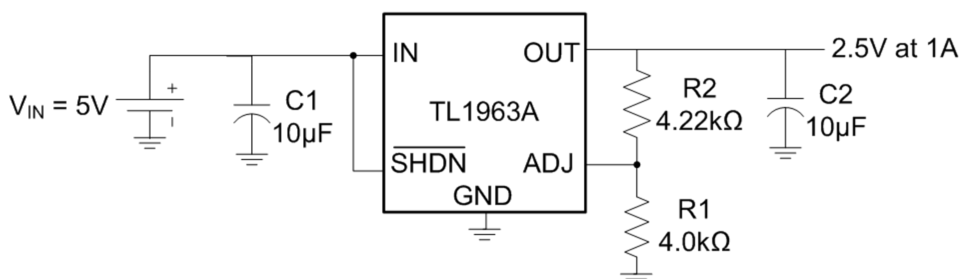
For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{θJA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (8)$$

Thermal resistance ($R_{θJA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The JEDEC standard PCB and copper-spreading area determine the junction-to-ambient thermal resistance listed in the *Thermal Information* table and are used as a relative measure of package thermal performance.

7.2 Typical Applications



A. All capacitors are ceramic.

Figure 7-1. Adjustable Output Voltage Operation

Use the TL1963A-xx in a fixed voltage configuration. Connect the SENSE/ADJ pin to OUT for proper operation as in Figure 7-2. For a fixed output voltage of 1.21V, use the TL1963A.

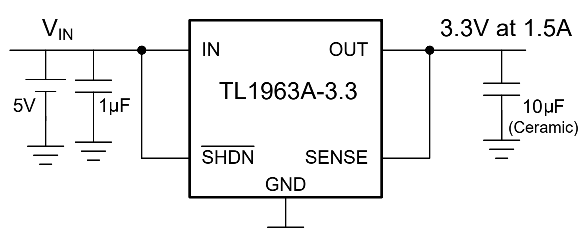


Figure 7-2. 4.3V to 3.3V Regulator

7.2.1 Kelvin Sense Connection with SENSE pin

Optimum regulation is obtained at the point where the SENSE pin connects to the OUT pin of the regulator. In critical applications, the resistance (R_P) of PC traces between the regulator and the load cause small voltage drops. During fixed voltage operation, use the SENSE/ADJ pin for a Kelvin connection if routed separately to the load. This allows the regulator to compensate for voltage drop across parasitic resistances (RP) between the output and the load. This becomes more crucial with higher load currents. Note that the voltage drop across the external PCB traces adds to the dropout voltage of the regulator.

The SENSE pin bias current is captured as I_{SENSE} in Electrical Characteristics: TL1963A (for DCQ, KTT package). For legacy chip, pull the SENSE pin below ground (as in a dual supply system in which the regulator load is returned to a negative supply) and still allow the device to start and operate.

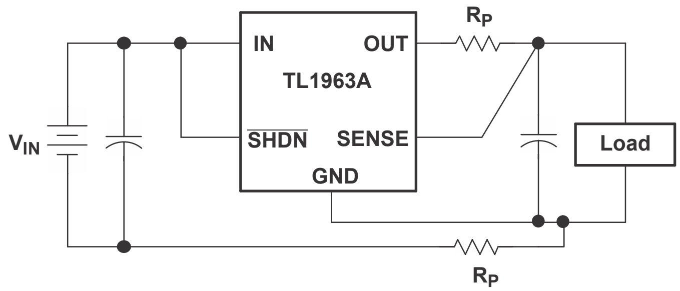


Figure 7-3. Kelvin Sense Connection

7.2.2 Design Requirements

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (V_{IN})	5.0V
Output Voltage (V_{OUT})	2.5V
Output Current (I_{OUT})	0A to 1A
Load Regulation	1%

7.2.3 Detailed Design Procedure

The TL1963A has an adjustable output voltage range from 1.21V to 20V. The ratio of two external resistors R1 and R2 as shown in Figure 7-1 sets the output voltage. The device maintains the voltage at the ADJ pin at 1.21V referenced to ground. The current in R1 is then equal to (1.21V/R1), and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, I_{ADJ} (captured in Electrical Characteristics: TL1963A (for DCQ, KTT package)), flows through R2 into the ADJ pin. Calculate the output voltage using Equation 9.

$$V_{OUT} = 1.21V\left[1 + \frac{R2}{R1}\right] + I_{ADJ} \times R2 \tag{9}$$

The value of R1 must be less than 4.17kΩ to minimize errors the ADJ pin bias current (I_{ADJ}) causes in the output voltage. Note that in shutdown the output is turned off, and the divider current is zero. For an output voltage of 2.50V, R1 is set to 4.0kΩ. R2 is then found to be 4.22kΩ using the equation above.

$$V_{OUT} = 1.21V\left[1 + \frac{4.22k\Omega}{4.0k\Omega}\right] + 3\mu A \times 4.22k\Omega \tag{10}$$

$$V_{OUT} = 2.50V \tag{11}$$

The adjustable device is tested and specified with the ADJ pin tied to the OUT pin for an output voltage of 1.21V. Specifications for output voltages greater than 1.21V are proportional to the ratio of the desired output voltage to 1.21V: V_{OUT}/1.21V. For example, load regulation for an output current change from 1mA to 1.5A is –2mV (typical) at V_{OUT} = 1.21V. At V_{OUT} = 2.50V, the typical load regulation is:

$$\left[\frac{2.50V}{1.21V}\right][-2mV] = -4.13mV \tag{12}$$

For legacy chip, Figure 7-4 shows the actual change in output is approximately 3mV for a 1A load step. The maximum load regulation at 25°C is –8mV. At V_{OUT} = 2.50V, the maximum load regulation is:

$$\left[\frac{2.50\text{V}}{1.21\text{V}}\right][-8\text{mV}] = -16.53\text{mV} \quad (13)$$

Since 16.53mV is only 0.7% of the 2.5V output voltage, the load regulation meets the design requirements.

7.2.4 Application Curve

At operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or 2.4V (whichever is greater), I_{OUT} = 1mA, C_{IN} = 10µF, and C_{OUT} = 10µF (unless otherwise noted).

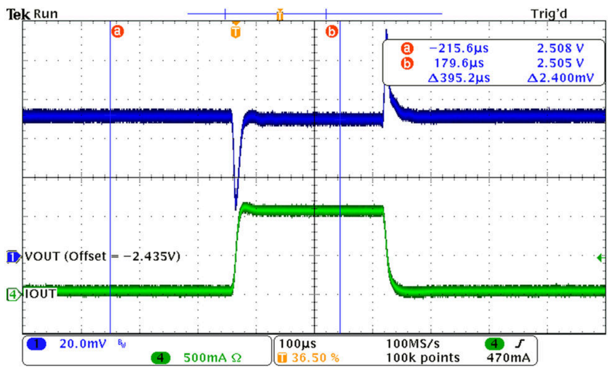
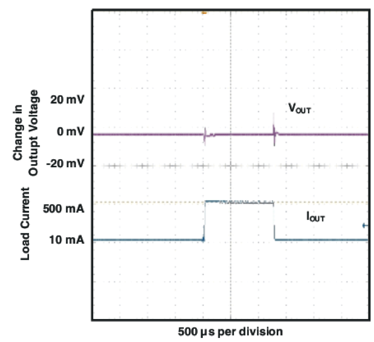


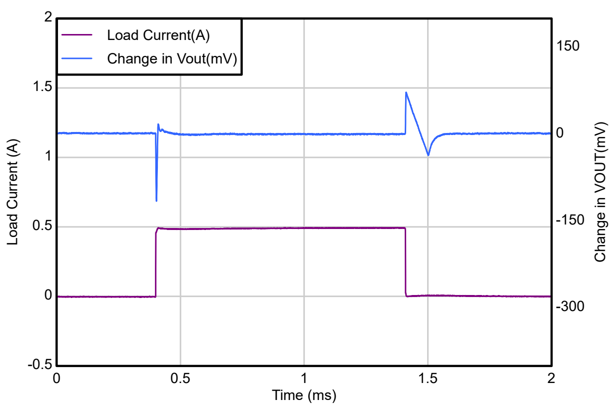
Figure 7-4. 1A Load Transient Response (C_{OUT} = 10uF) (Legacy chip)



V_{IN} = 4.3V C_{IN} = 10 µF

C_{OUT} = 10 µF (ceramic)

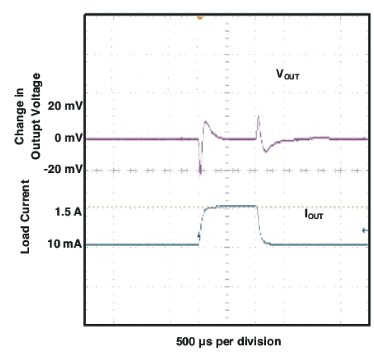
Figure 7-5. Load Transient Response (Legacy Chip)



V_{IN} = 4.3V C_{IN} = 10 µF

C_{OUT} = 10 µF (ceramic)

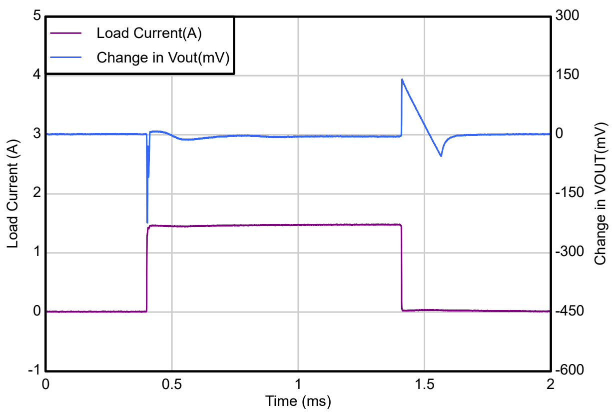
Figure 7-6. Load Transient Response (New Chip)



V_{IN} = 4.3V C_{IN} = 10 µF

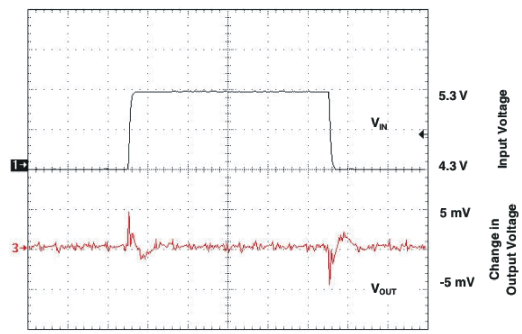
C_{OUT} = 10 µF (ceramic)

Figure 7-7. Load Transient Response (Legacy Chip)



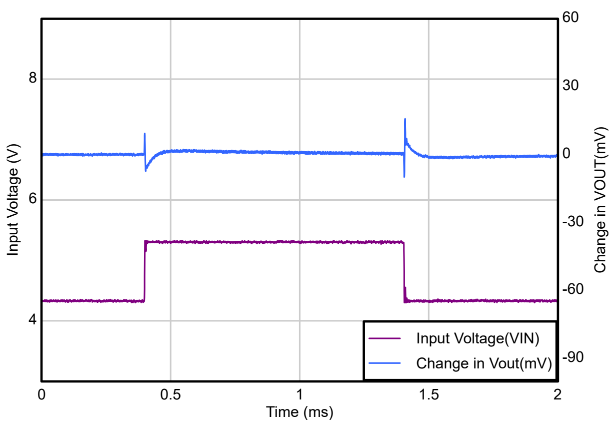
V_{IN} = 4.3V C_{IN} = 10 µF
C_{OUT} = 10 µF (ceramic)

Figure 7-8. Load Transient Response (New Chip)



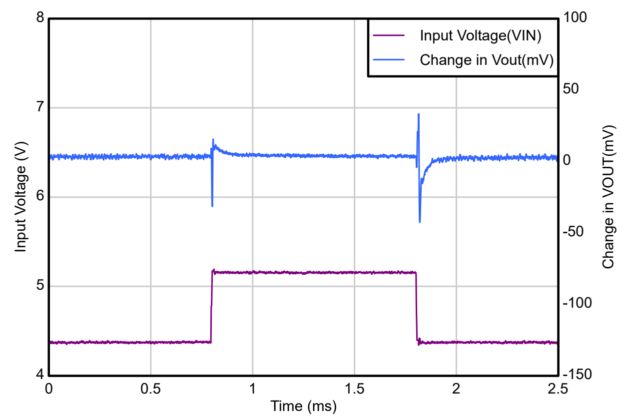
I_{OUT} = 1.5A C_{IN} = 10 µF
C_{OUT} = 10 µF (ceramic)

Figure 7-9. Line Transient Response (Legacy Chip)



I_{OUT} = 0.3A C_{IN} = 10 µF
C_{OUT} = 10 µF (ceramic)

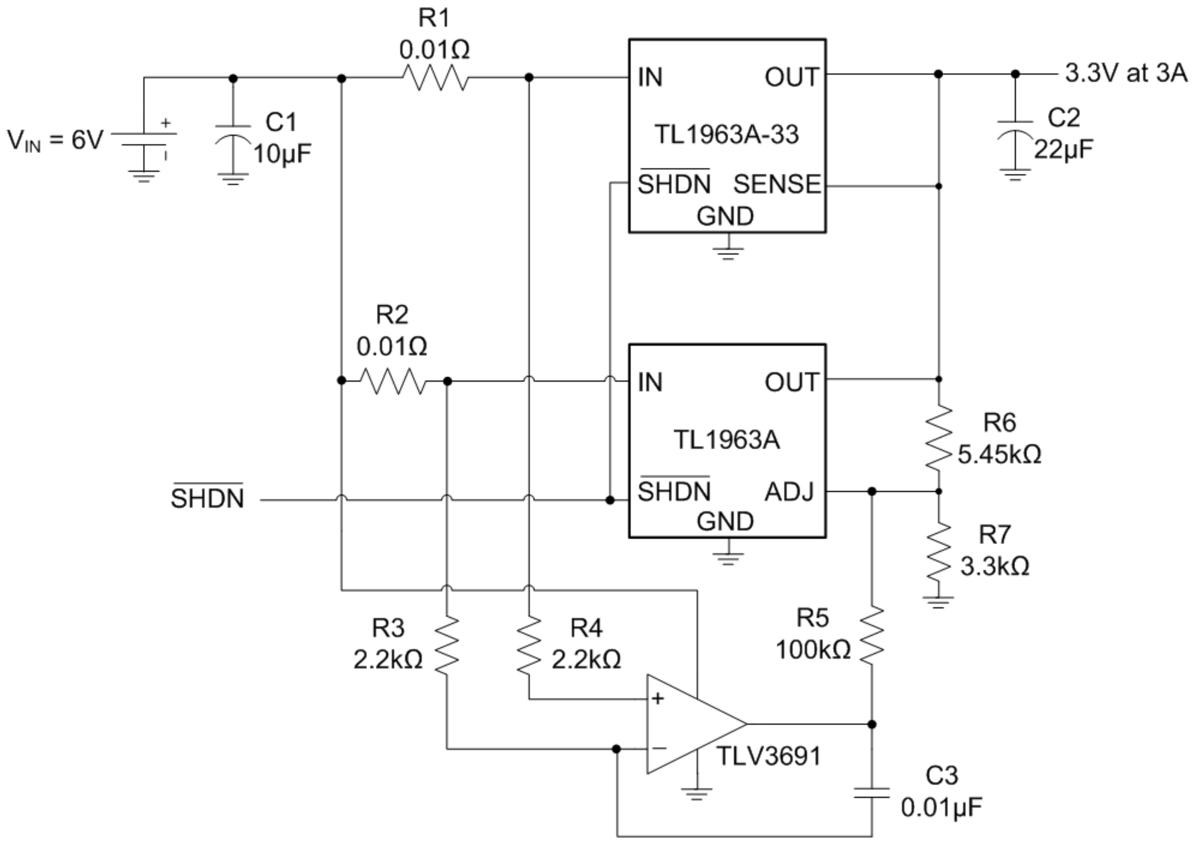
Figure 7-10. Line Transient Response (Legacy Chip)



I_{OUT} = 1.5A C_{IN} = 10 µF
C_{OUT} = 10 µF (ceramic)

Figure 7-11. Line Transient Response (Legacy Chip)

7.2.5 Paralleling Regulators for Higher Output Current (Legacy chip only)



A. All capacitors are ceramic.

Figure 7-12. Paralleling Regulators for Higher Output Current

7.2.5.1 Design Requirements

Table 7-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (V_{IN})	6.0V
Output Voltage (V_{OUT})	3.3V
Output Current (I_{OUT})	3.0A

7.2.5.2 Detailed Design Procedure (Legacy chip only)

In an application requiring higher output current, place an adjustable output regular in parallel with a fixed output regulator to increase the current capacity. Use two sense resistors and a comparator to control the feedback loop of the adjustable regulator to balance the current between the two regulators.

In Paralleling Regulators for Higher Output Current (Legacy chip only) resistors R1 and R2 are used to sense the current flowing into each regulator and must have a very low resistance to avoid unnecessary power loss. R1 and R2 must have the same value and a tolerance of 1% or better so the current is shared equally between the regulators. This example uses a value of 0.01Ω.

The TLV3691 rail-to-rail nanopower comparator output alternates between VIN and GND depending on the currents flowing into each of the two regulators. To design this control circuit, begin by looking at the case where the two output currents are approximately equal and the comparator output is low. In this case, the output of the TL1963A must be set the same as the fixed voltage regulator. The TL1963A-33 has a 3.3V fixed output, so this is the set point for the adjustable regulator. Begin by selecting a R7 value less than 4.17kΩ. This example uses 3.3kΩ. R5 must have a high resistance to satisfy Equation 18. This example uses100kΩ. Then find the parallel resistance of R5 and R7 since R5 and R7 are both connected from the ADJ pin to GND using Equation 14.

$$[R5 \parallel R7] = \frac{R5 \times R7}{R5 + R7} = 3.19k\Omega \tag{14}$$

Once the R5 and R7 parallel resistance in calculated, the value for R6 can be found using Equation 15.

$$R6 = \frac{V_{OUT}}{1.22V}[R5 \parallel R7] - [R5 \parallel R7] \tag{15}$$

$$R6 = \frac{3.3V}{1.22V}[3.19k\Omega] - [3.19k\Omega] \tag{16}$$

$$R6 = 5.45k\Omega \tag{17}$$

In the case where the TL1963A-33 is sourcing more current than TL1963A, the comparator output goes high. This lowers the voltage at the ADJ pin causing the TL1963A to try and raise the output voltage by sourcing more current. The TL1963A-33 then reacts by sourcing less current to try and keep the output from rising. When the current through the TL1963A-33 becomes less than the TL1963A, the comparator output returns to GND. For this to happen, satisfy Equation 18:

$$V_{IN}\left[\frac{R7}{R5 + R7}\right] + [V_{IN} - V_{OUT}]\left[\frac{R6}{R5 + R6}\right] < Vref \tag{18}$$

$$6V\left[\frac{3.3k\Omega}{100k\Omega + 3.3k\Omega}\right] + [2.7V]\left[\frac{5.45k\Omega}{100k\Omega + 5.45k\Omega}\right] < 1.21V \tag{19}$$

$$0.19V + 0.14V < 1.21V \tag{20}$$

$$0.33V < 1.21V \tag{21}$$

7.2.5.3 Application Curve

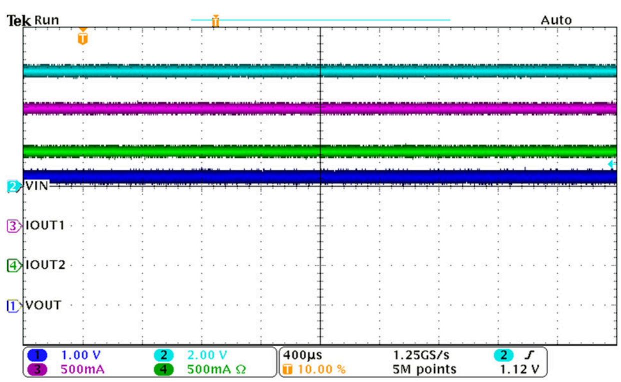


Figure 7-13. Parallel Regulators Sharing Load Current (Legacy chip only)

7.3 Power Supply Recommendations

The device is designed to operate with an input voltage supply up to 20V. The minimum input voltage must provide adequate headroom greater than the dropout voltage for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, follow the guidelines in this section. Place all circuit components on the same side of the printed circuit board (PCB) and as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. Do not use vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or resistor divider. This practice negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to provide accuracy of the output voltage and shield the LDO from noise. To improve the thermal performance of the device, and to maximize the current output at high ambient temperature, spread the copper under the thermal pad as far as possible and place enough thermal vias on the copper under the thermal pad. Connect the tab of the DCQ package to ground. Connect the exposed thermal pad of the KTT package to a wide ground plane for effective heat dissipation.

7.4.2 Layout Example

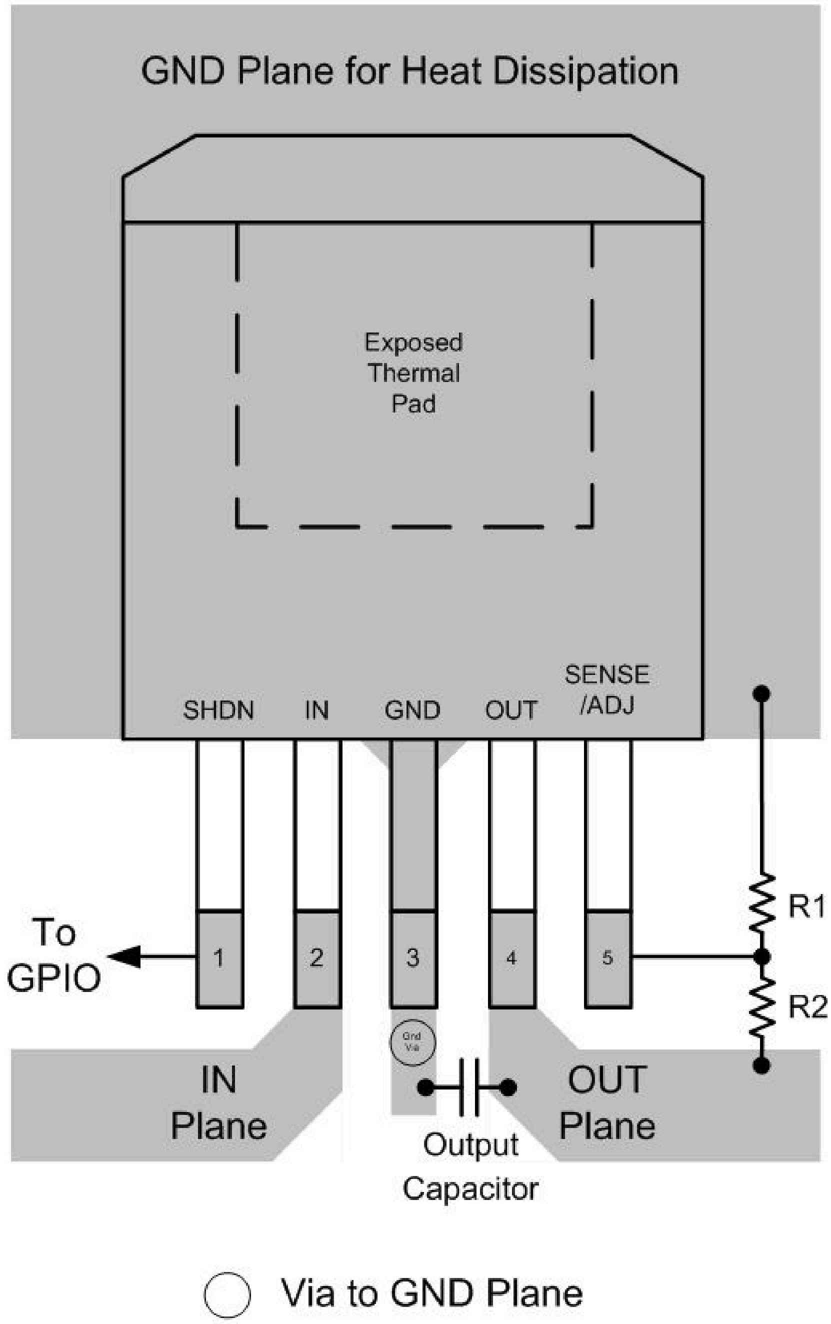


Figure 7-14. TO-263 Layout Example (KTT)

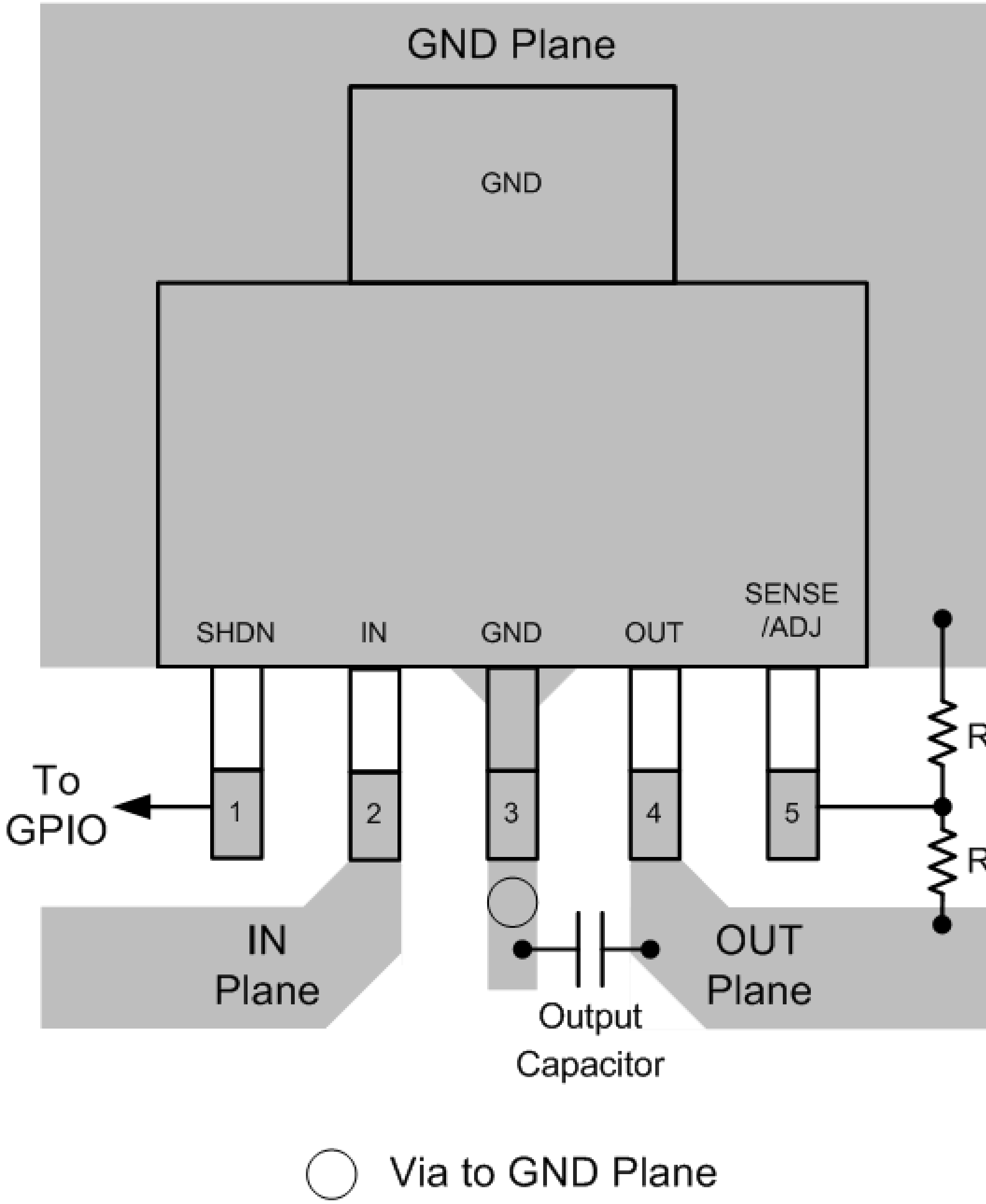


Figure 7-15. 6SOT-223 Layout Example (DCQ)

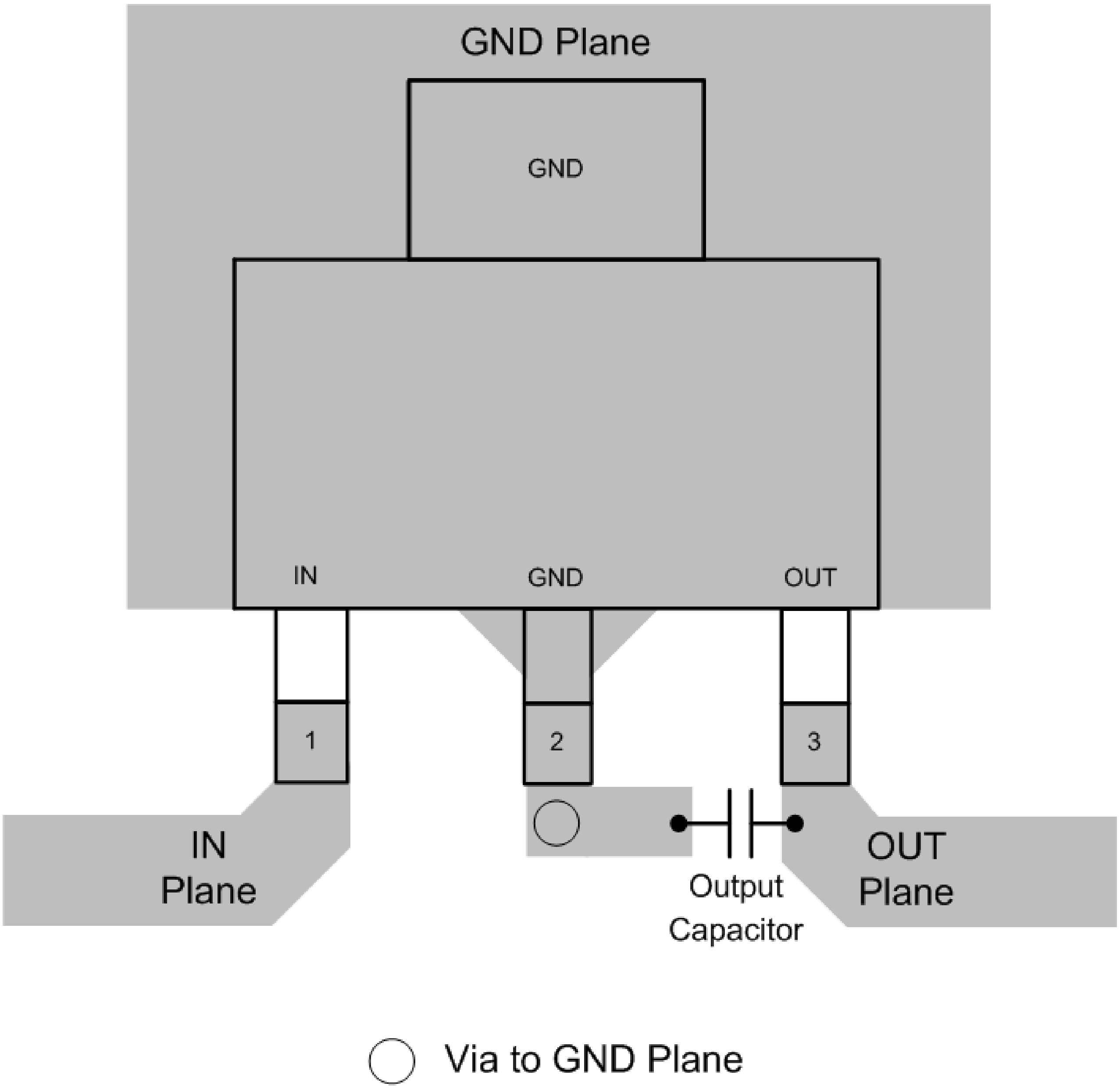


Figure 7-16. 4SOT-223 Layout Example (DCY)

7.4.3 Thermal Considerations

The recommended maximum operating junction temperature (125°C) limits the power handling capability of the device. The power the device dissipates is comprised of two components:

- Output current multiplied by the input/output voltage differential: $I_{OUT}(V_{IN} – V_{OUT})$
- GND pin current multiplied by the input voltage: $I_{GND}V_{IN}$

The GND pin current can be found using the GND Pin Current graphs in *Section 5.7*. Power dissipation is equal to the sum of the two components listed above.

The TL1963A-xx series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the recommended maximum operating junction temperature is

125°C. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Also consider additional heat sources mounted nearby.

For surface-mount devices, accomplish heat sinking by using the heat-spreading capabilities of the PC board and its copper traces. Use copper board stiffeners and plated through-holes to spread the heat generated by power devices.

Table 7-3 of the legacy chip lists thermal resistance for several different board sizes and copper areas. All measurements are taken in still air on 1/16" FR-4 board with 1oz copper.

Table 7-3. Thermal Data for KTT Package (5-Pin TO-263) [Legacy chip]

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION TO AMBIENT)
TOPSIDE(1)	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	23°C/W
1000mm^2	2500mm^2	2500mm^2	25°C/W
125mm^2	2500mm^2	2500mm^2	33°C/W

(1) Device is mounted on topside.

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TL1963A-xx. The TL1963A-33EVM EVM (and related user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT[(1)]	DESCRIPTION
TL1963A-**xx yyy z** TL1963A**yyy z**	xx is nominal output voltage (for example, 18 = 1.8V, 33 = 3.3V). yyy is package designator. z is package quantity. TL1963A**yyy z** represents the adjustable device. This device either ships with the legacy chip (CSO: SHE) or the new chip (CSO: RFB), which uses the latest manufacturing flow. The reel packaging label provides CSO information to distinguish which chip is used. Device performance for new and legacy chips is denoted throughout the document.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, *PCB thermal calculator*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Trademarks

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2015) to Revision H (June 2026) — **Page**

- Updated the *Features* section to include comparison between Legacy and New chip performance (input, output range, output voltage accuracy and package thermal details)............ 1
- Updated Absolute maximum ratings, ESD, Recommended Operating Conditions, Thermal and Electrical Characteristics tables to show performance comparison between legacy and new chip............ 5
- Updated Overview section to highlight key features of legacy and new chip............ 24

- Updated *Overload Recovery*, *Output voltage noise* and *Protection features* section for comparison between legacy and new chip and better readability to customers and added details about $\overline{SHDN}$, *Undervoltage Lockout (UVLO)*, *Thermal shutdown* and *Current limit* sections..24
- Updated Protection Features to create For Legacy Chip Only and For Both Legacy and New chip sections. 27
- Updated *Device Functional Modes* section for better readability of the datasheet..28
- Updated Application Information sections for better datasheet readability and added *Reverse Current, Feed-forward Capacitor, Estimating Junction Temperature and Power Dissipation (P_D)* sections........................... 29
- Updated Typical Applications section for better readability and comparison between legacy and new chip... 31
- Added Load and Line Transient plots for Legacy and New chip in the *Application curve* section....................33
- Moved Power Supply Recommendations to Application and Implementation section.....................................36
- Moved Layout to Application and Implementation section... 37
- Added Device support section and updated EVM details for TL1963A-xx devices...42
- Added Device nomenclature section with details about legacy and new chip..42

Changes from Revision F (January 2014) to Revision G (January 2015) **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL1963A-15DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-15
TL1963A-15DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-15
TL1963A-15DCQT	Active	Production	SOT-223 (DCQ) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-15
TL1963A-15DCQT.A	Active	Production	SOT-223 (DCQ) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-15
TL1963A-15DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TF
TL1963A-15DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TF
TL1963A-15DCYT	Active	Production	SOT-223 (DCY) | 4	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TF
TL1963A-15DCYT.A	Active	Production	SOT-223 (DCY) | 4	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TF
TL1963A-15KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TL1963A-15
TL1963A-15KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TL1963A-15
TL1963A-18DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-18
TL1963A-18DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-18
TL1963A-18DCQT	Active	Production	SOT-223 (DCQ) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-18
TL1963A-18DCQT.A	Active	Production	SOT-223 (DCQ) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-18
TL1963A-18DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TG
TL1963A-18DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TG
TL1963A-18KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TL1963A-18
TL1963A-18KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TL1963A-18
TL1963A-25DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-25
TL1963A-25DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-25
TL1963A-25DCQT	Active	Production	SOT-223 (DCQ) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-25
TL1963A-25DCQT.A	Active	Production	SOT-223 (DCQ) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-25
TL1963A-25DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TH
TL1963A-25DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TH
TL1963A-25DCYT	Active	Production	SOT-223 (DCY) | 4	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TH
TL1963A-25DCYT.A	Active	Production	SOT-223 (DCY) | 4	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TH

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL1963A-25KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TL1963A-25
TL1963A-25KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TL1963A-25
TL1963A-33DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-33
TL1963A-33DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-33
TL1963A-33DCQRG4	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-33
TL1963A-33DCQRG4.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-33
TL1963A-33DCQT	Active	Production	SOT-223 (DCQ) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-33
TL1963A-33DCQT.A	Active	Production	SOT-223 (DCQ) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-33
TL1963A-33DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TJ
TL1963A-33DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TJ
TL1963A-33KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TL1963A-33
TL1963A-33KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TL1963A-33
TL1963ADCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1963A
TL1963ADCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1963A
TL1963ADCQRG4	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1963A
TL1963ADCQRG4.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1963A
TL1963ADCQT	Active	Production	SOT-223 (DCQ) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1963A
TL1963ADCQT.A	Active	Production	SOT-223 (DCQ) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL1963A
TL1963AKTTR	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TL1963A
TL1963AKTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TL1963A
TL1963AKTTRG3	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TL1963A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL1963A :

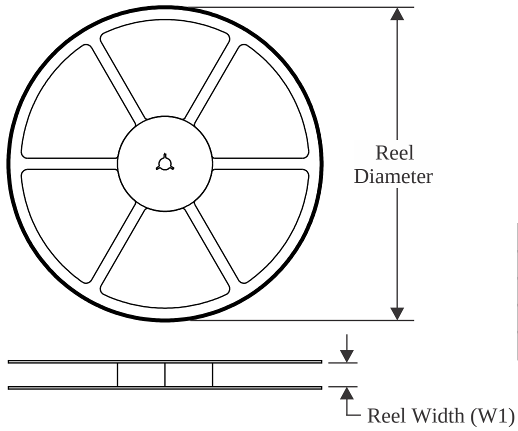
- Automotive : TL1963A-Q1

NOTE: Qualified Version Definitions:

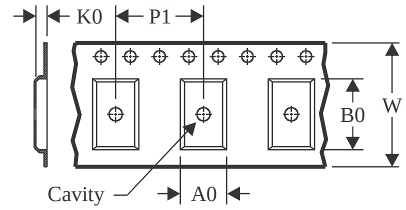
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

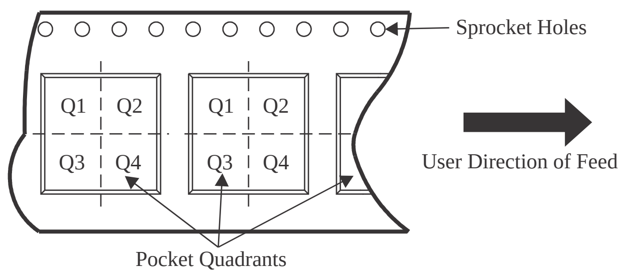


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

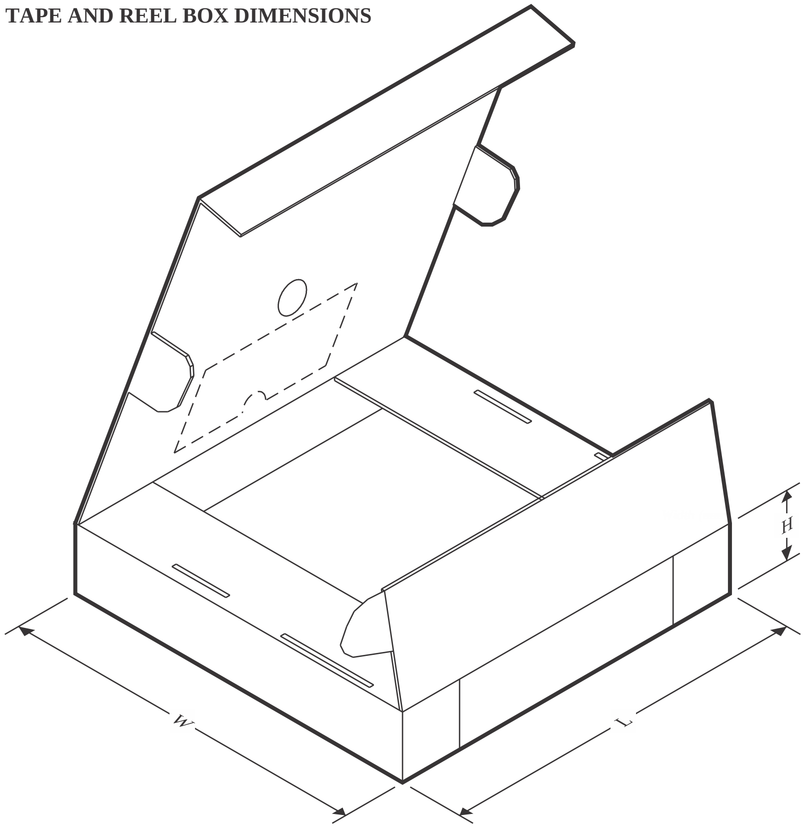


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL1963A-15DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-15DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-15DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TL1963A-15DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TL1963A-15KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TL1963A-18DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-18DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-18DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TL1963A-18KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TL1963A-25DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-25DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-25DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TL1963A-25DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TL1963A-25KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL1963A-33DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-33DCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-33DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-33DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TL1963A-33KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TL1963ADCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963ADCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963ADCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963AKTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

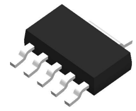
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL1963A-15DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TL1963A-15DCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TL1963A-15DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TL1963A-15DCYT	SOT-223	DCY	4	250	190.0	190.0	30.0
TL1963A-15KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TL1963A-18DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TL1963A-18DCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TL1963A-18DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TL1963A-18KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TL1963A-25DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TL1963A-25DCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TL1963A-25DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TL1963A-25DCYT	SOT-223	DCY	4	250	190.0	190.0	30.0
TL1963A-25KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TL1963A-33DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TL1963A-33DCQRG4	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TL1963A-33DCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TL1963A-33DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0

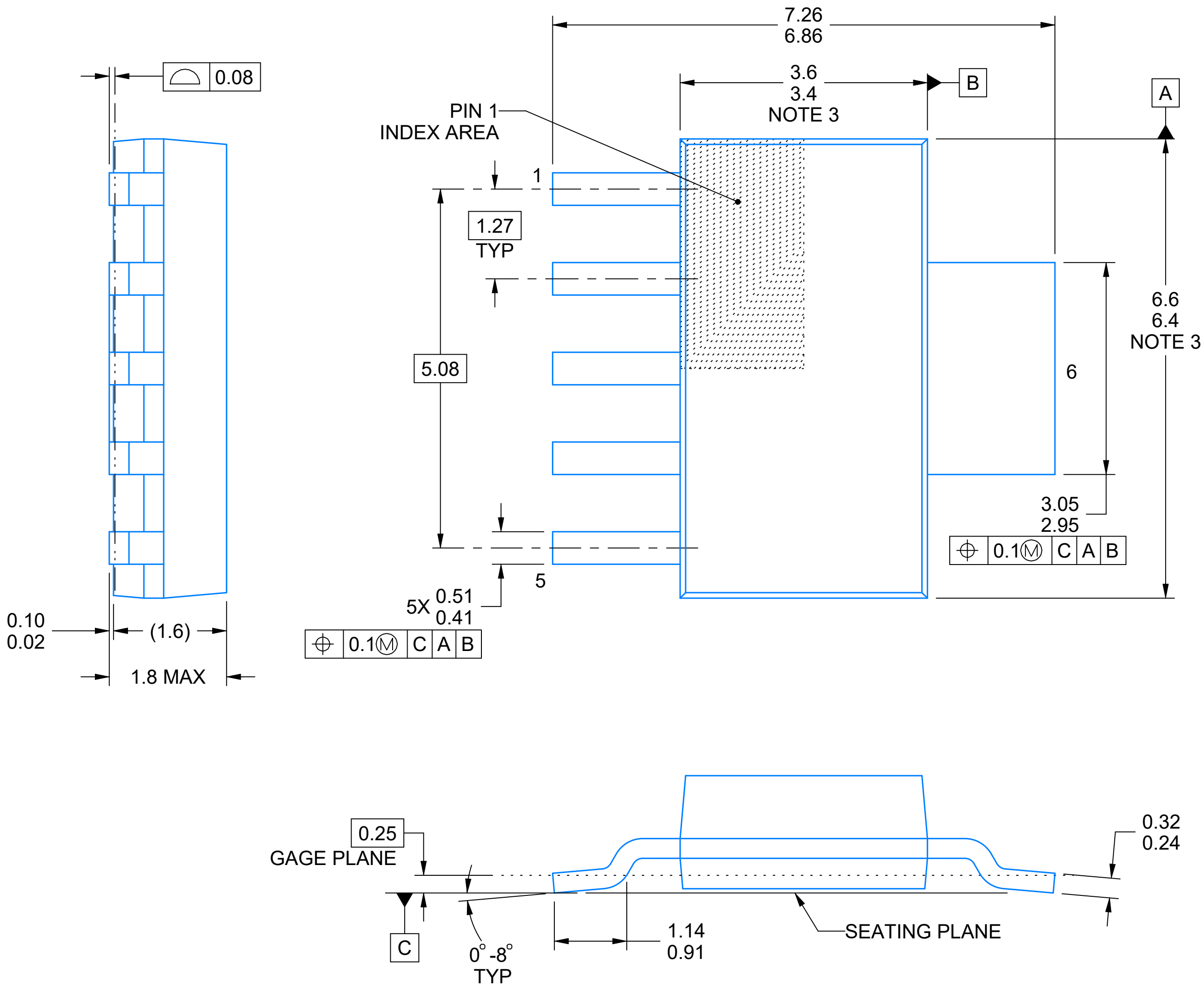
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL1963A-33KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TL1963ADCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TL1963ADCQRG4	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TL1963ADCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TL1963AKTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0



PACKAGE OUTLINE

SOT - 1.8 mm max height

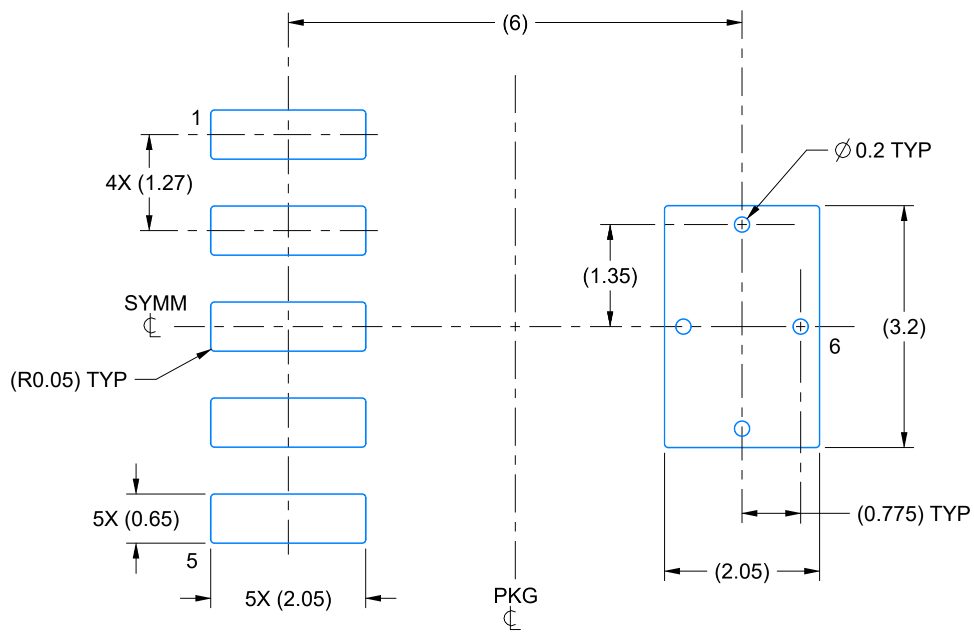
PLASTIC SMALL OUTLINE



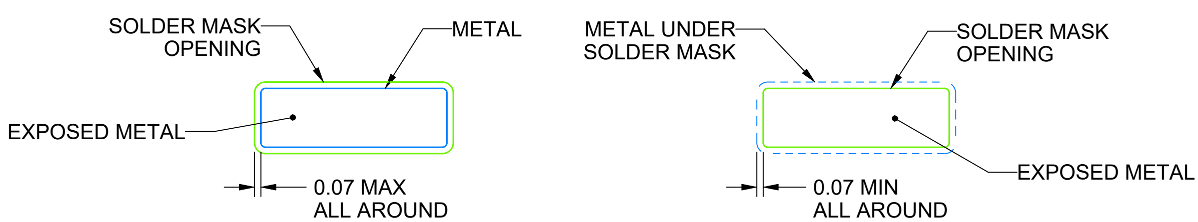
4214845/C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

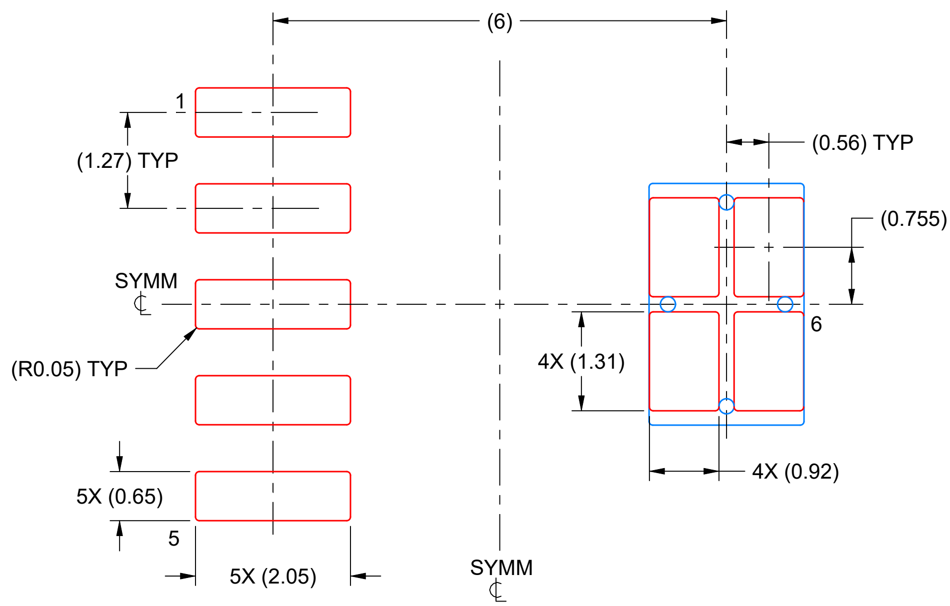


SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



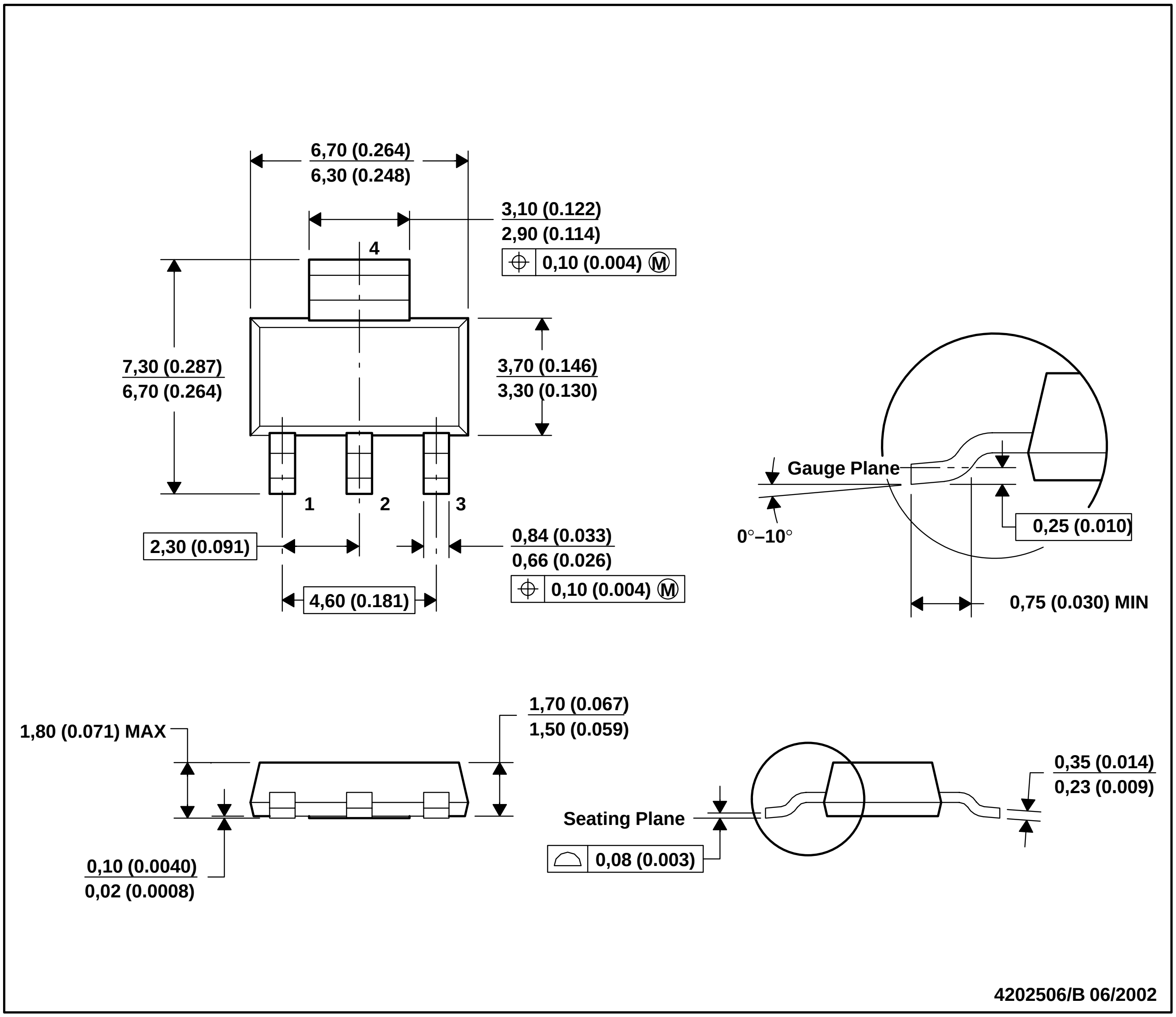
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

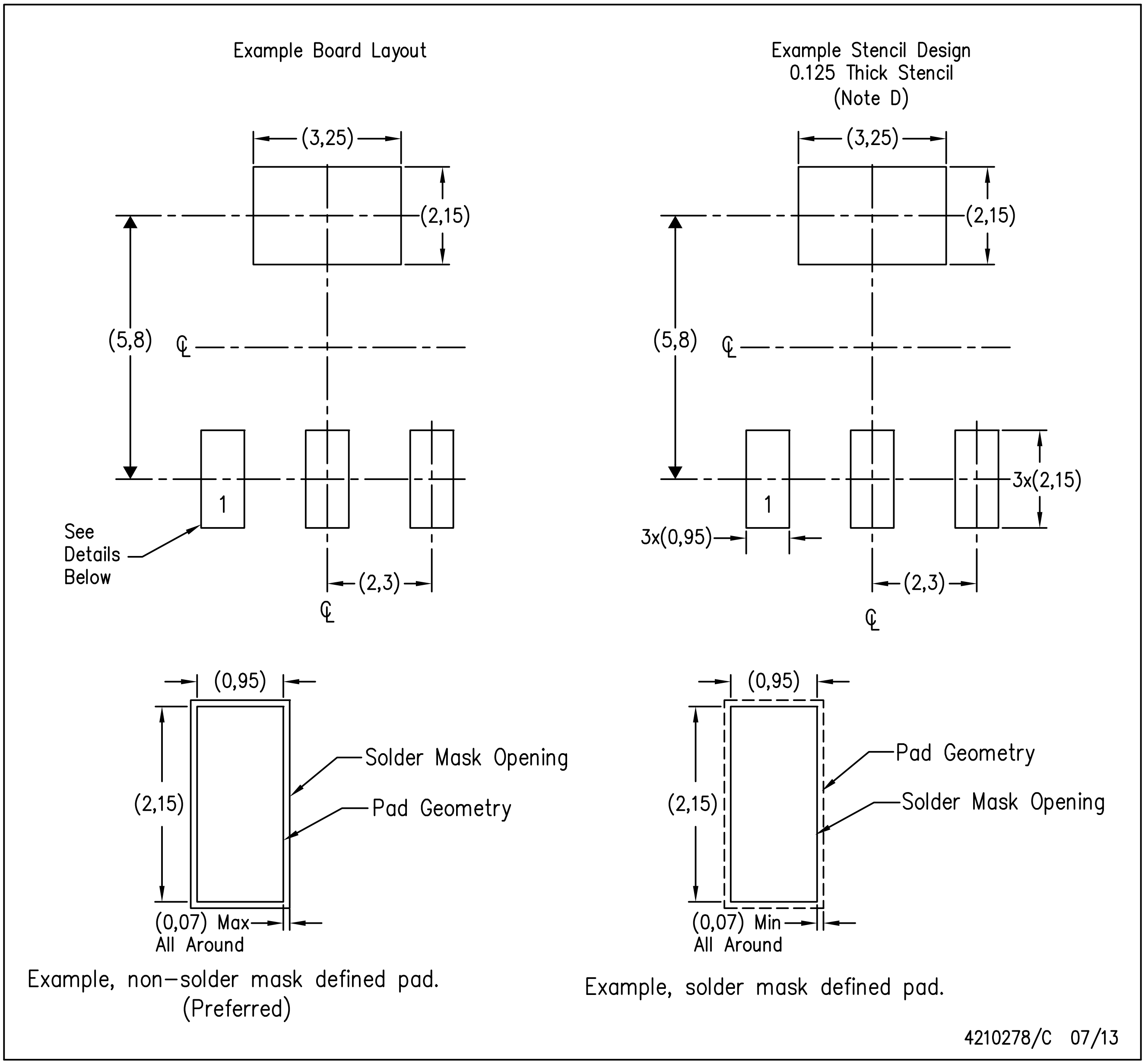
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



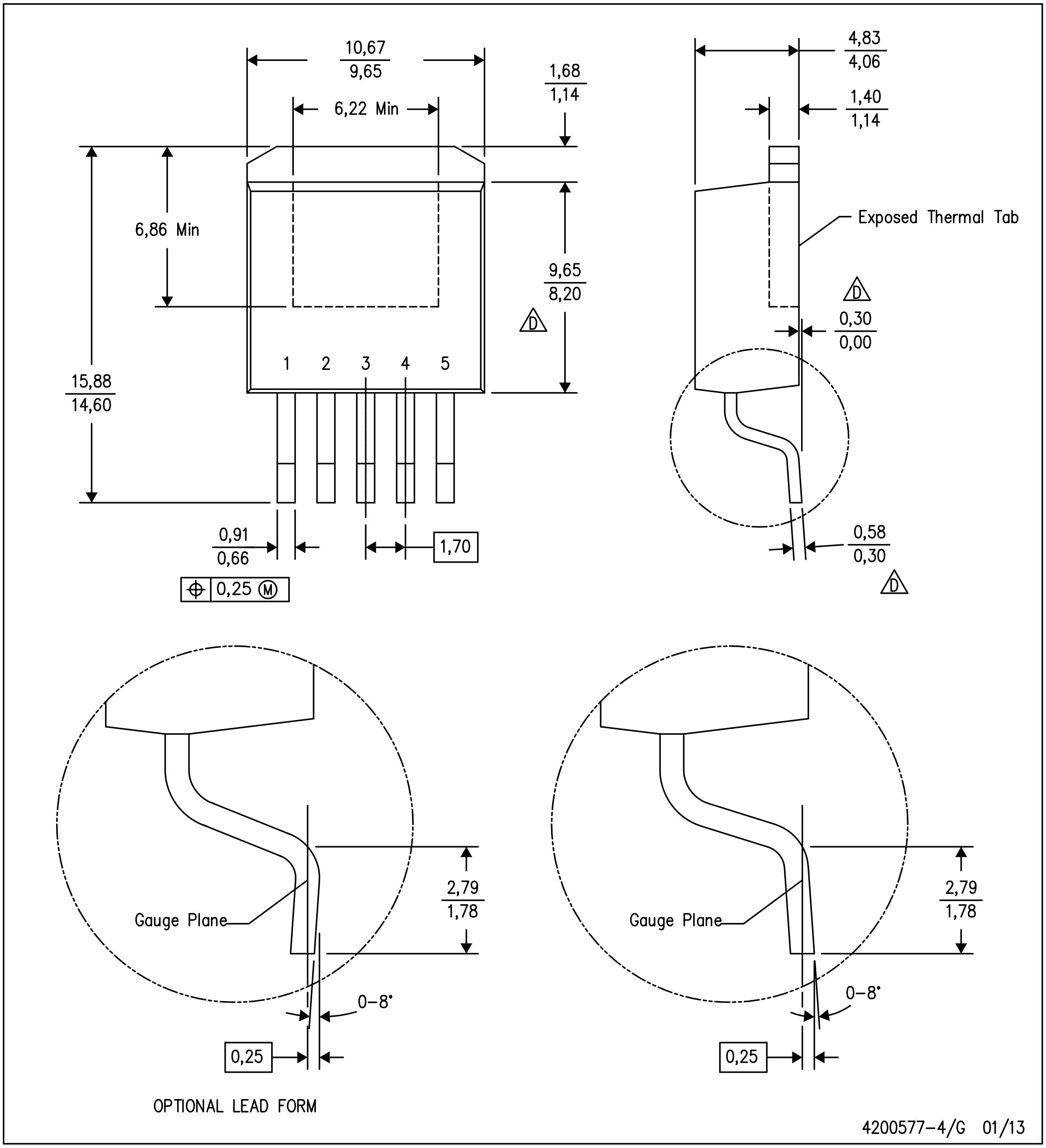
NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



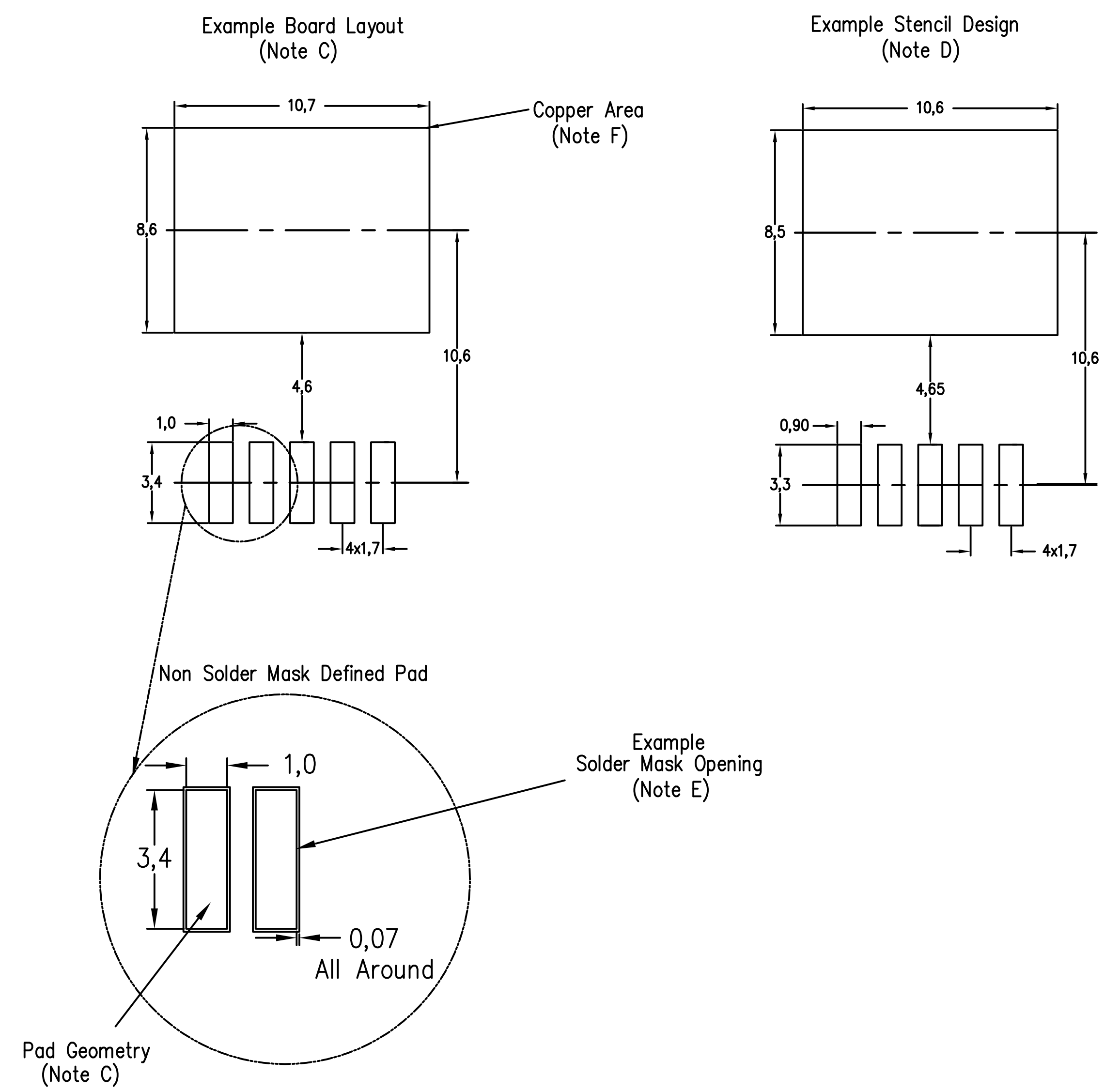
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

KTT (R-PSFM-G5) PLASTIC FLANGE-MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO-263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



4208208–3/C 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–SM–782 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.