TLC27Lx Precision, Dual Operational Amplifiers

1 Features

- Input offset voltage drift: typically 0.1µV/month, including the first 30 days
- Wide range of supply voltages over specified temperature range:
  - 0°C to 70°C: 3V to 16V
  - −40°C to +85°C: 4V to 16V
  - −55°C to +125°C: 4V to 16V
- Single-supply operation
- Common-mode input voltage range extends below the negative rail (C-suffix, I-suffix types)
- Ultra-low power: 95µW at 25°C (typical), V_{DD} = 5V
- Output voltage range includes negative rail
- High input impedance: $10^{12}\Omega$ (typical)
- ESD-protection circuitry
- Small-outline package option also available in tape and reel
- Designed-in latch-up immunity

2 Applications

- Smoke and heat detector
- Field transmitter and sensor
  - Flow transmitter
  - Pressure transmitter
  - Temperature transmitter
  - Level transmitter
- Motion detector

3 Description

The TLC27L2x and TLC27L7 dual op amps combine a wide range of input offset-voltage grades with low offset-voltage drift, high input impedance, extremely low power, and high gain. These devices use the Texas Instruments silicon-gate LinCMOS™ technology, providing offset-voltage stability far exceeding the stability with conventional metal-gate processes.

Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L2 (10mV) to the high-precision TLC27L7 (1000µV). The extremely high input impedance and low bias currents, along with good common-mode rejection and supply-voltage rejection, and low power consumption, make these devices a good choice for new state-of-the-art designs and upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC27Lx. The devices also exhibit low-voltage and single-supply operation, making them an excellent choice for remote and inaccessible battery-powered applications. The common-mode input-voltage range includes the negative rail.

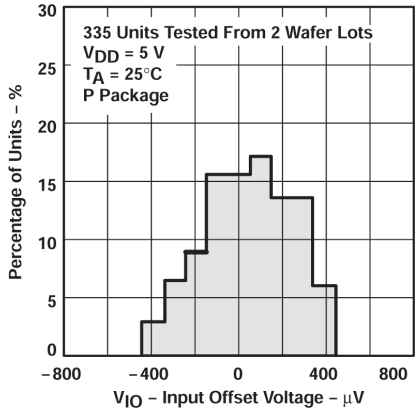
The TLC27Lx incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000V as tested under MIL-STD-883C, Method 3015.2. Exercise care when handling these devices because exposure to ESD potentially degrades device parametric performance.

C-suffix devices are characterized for operation from 0°C to 70°C, I-suffix devices from −40°C to +85°C, and M-suffix devices over the full military temperature range of −55°C to +125°C.

Device Information

PART NUMBER	V_{IOmax} at 25°C	PACKAGE(1)
TLC27L2	10mV	D (SOIC, 8)
		P (PDIP, 8)
		PS (SOP, 8)
		PW (TSSOP, 8)
TLC27L2M	10mV	D (SOIC, 8)
TLC27L2A	5mV	D (SOIC, 8)
		P (PDIP, 8)
		PS (SOP, 8)
TLC27L2B	2mV	D (SOIC, 8)
		P (PDIP, 8)
TLC27L7	1mV	D (SOIC, 8)
		P (PDIP, 8)
		PS (SOP, 8)

(1) For all available packages, see Section 10.



Distribution of TLC27L7 Input Offset Voltage

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4 Pin Configuration and Functions

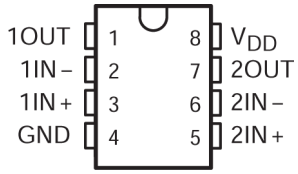


Figure 4-1. D (8-Pin SOIC), P (8-Pin PDIP), PS (8-Pin SOP), or PW (8-Pin TSSOP) Packages (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN+	3	Input	Noninverting input, channel 1
1IN–	2	Input	Inverting input, channel 1
1OUT	1	Output	Output, channel 1
2IN+	5	Input	Noninverting input, channel 2
2IN–	6	Input	Inverting input, channel 2
GND	4	Ground	Ground or negative (lowest) power supply
V_{DD}	8	Power	Positive (highest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted(1)

			MIN	MAX	UNIT
V_{DD} (2)	Supply voltage			18	V
V_{ID} (3)	Differential input voltage			$\pm V_{DD}$	V
V_I	Input voltage (any input)		−0.3	V_{DD}	V
I_I	Input current			±5	mA
I_O	Output current (each output)			±30	mA
	Total current into V_{DD}			45	mA
	Total current out of GND			45	mA
	Duration of short-circuit current at (or less than) T_A = 25°C(4)		Unlimited		
	Continuous total power dissipation		See *Dissipation Ratings*		
T_A	Operating free-air temperature	C suffix	0	70	°C
		I suffix	−40	85	°C
		M suffix	−55	125	°C
T_{stg}	Storage temperature		−65	150	°C
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground.
(3) Differential voltages are at the IN+ of a given channel, with respect to IN− for that same channel.
(4) The output is able to be shorted to either supply. Limit temperature, supply voltages, or both to not exceed the maximum dissipation ratings (see Section 7.1.6).

5.2 Dissipation Ratings

PACKAGE	$T_A \le 25°C$ POWER RATING	$T_A > 25°C$ DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8 mW/°C	640 mW	520 mW

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{DD}	Supply voltage	C suffix	3	16	V
		I suffix and M suffix	4	16	
V_{IC}	Common-mode input voltage	V_{DD} = 5V, C suffix and I suffix	–0.2	3.5	V
		V_{DD} = 5V, M suffix	0	3.5	
		V_{DD} = 10V, C suffix and I suffix	–0.2	8.5	
		V_{DD} = 10V, M suffix	0	8.5	
T_A	Operating free-air temperature	C suffix	0	70	°C
		I suffix	–40	85	
		M suffix	–55	125	

5.4 Electrical Characteristics, V_{DD} = 5V, C Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	TLC27L2C, TLC27L2AC, TLC27L2BC, TLC27L7C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		1.1	10	mV
				0°C to 70°C			12	
		TLC27L2AC	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		0.9	5	
				0°C to 70°C			6.5	
		TLC27L2BC	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		240	2000	µV
				0°C to 70°C			3000	
		TLC27L7C	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		210	1000	
				0°C to 70°C			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1		µV/°C
I_{IO}	Input offset current(1) (2)		V_O = 2.5V, V_{IC} = 2.5V	25°C		0.5	60	pA
				70°C		7	300	
I_{IB}	Input bias current(1) (2)		V_O = 2.5V, V_{IC} = 2.5V	25°C		0.6	60	pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range(3)			25°C	−0.2 to 4	−0.2 to 4.2		V
				0°C to 70°C	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100mV, R_L = 1MΩ	25°C	3.2	4.1		V
				0°C	3	4.1		
				70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100mV, I_{OL} = 0mA	25°C		1	50	mV
				0°C		1	50	
				70°C		1	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25V to 2V, R_L = 1MΩ	25°C	50	700		V/mV
				0°C	50	700		
				70°C	50	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	87		dB
				0°C	60	85		
				70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5V to 10V, V_O = 1.4V	25°C	70	97		dB
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5V, V_{IC} = 2.5V, no load	25°C		20	34	µA
				0°C		24	42	
				70°C		16	28	

(1) Typical values of input bias current and input offset current less than 5pA determined mathematically.
(2) Values specified by characterization.
(3) This range also applies to each input individually.

5.5 Operating Characteristics, V_{DD} = 5V, C Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLC27L2C, TLC27L2AC, TLC27L2BC, TLC27L7C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1MΩ, C_L = 20pF, see Figure 6-1	$V_{I(PP)}$ = 1V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			$V_{I(PP)}$ = 2.5V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2		25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1MΩ, C_L = 20pF, see Figure 6-1		25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10mV, C_L = 20pF, see Figure 6-3		25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_I = 10mV, C_L = 20pF, f = B_1, see Figure 6-3		25°C		34°		°
				0°C		36°		
				70°C		30°		

5.6 Electrical Characteristics, V_{DD} = 10V, C Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	TLC27L2C, TLC27L2AC, TLC27L2BC, TLC27L7C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		1.1	10	mV
				0°C to 70°C			12	
		TLC27L2AC	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		0.9	5	
				0°C to 70°C			6.5	
		TLC27L2BC	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		235	2000	μV
				0°C to 70°C			3000	
		TLC27L7C	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		210	1000	
				0°C to 70°C			1900	
αV_{IO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1		μV/°C
I_{IO}	Input offset current(1) (2)		V_O = 5V, V_{IC} = 5V	25°C		0.5	60	pA
				70°C		8	300	
I_{IB}	Input bias current(1) (2)		V_O = 5V, V_{IC} = 5V	25°C		0.7	60	pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range(3)			25°C	−0.2 to 9	−0.2 to 9.2		V
				0°C to 70°C	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100mV, R_L = 1MΩ	25°C	8	8.9		V
				0°C	7.8	8.9		
				70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100mV, I_{OL} = 0mA	25°C		5	50	mV
				0°C		5	50	
				70°C		5	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1V to 6V, R_L = 1MΩ	25°C	50	860		V/mV
				0°C	50	1025		
				70°C	50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	94		dB
				0°C	60	93		
				70°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5V to 10V, V_O = 1.4V	25°C	70	97		dB
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5V, V_{IC} = 5V, no load	25°C		29	46	μA
				0°C		36	66	
				70°C		22	40	

(1) Typical values of input bias current and input offset current less than 5pA determined mathematically.
(2) Values specified by characterization.
(3) This range also applies to each input individually.

5.7 Operating Characteristics, V_{DD} = 10V, C Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLC27L2C, TLC27L2AC, TLC27L2BC, TLC27L7C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1MΩ, C_L = 20pF, see Figure 6-1	$V_{I(PP)}$ = 1V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			$V_{I(PP)}$ = 5.5V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2		25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1MΩ, C_L = 20pF, see Figure 6-1		25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10mV, C_L = 20pF, see Figure 6-3		25°C		110		kHz
				0°C		110		
				70°C		90		
ϕ_m	Phase margin	V_I = 10mV, C_L = 20pF, f = B_1, see Figure 6-3		25°C		38°		°
				0°C		40°		
				70°C		34°		

5.8 Electrical Characteristics, V_{DD} = 5V, I Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	TLC27L2I, TLC27L2AI, TLC27L2BI, TLC27L7I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		1.1	10	mV
				–40°C to +85°C			13	
		TLC27L2AI	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		0.9	5	
				–40°C to +85°C			7	
		TLC27L2BI	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		240	2000	μV
				–40°C to +85°C			3500	
		TLC27L7I	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		210	1000	
				–40°C to +85°C			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1		μV/°C
I_{IO}	Input offset current(1) (2)		V_O = 2.5V, V_{IC} = 2.5V	25°C		0.5	60	pA
				85°C		24	1000	
I_{IB}	Input bias current(1) (2)		V_O = 2.5V, V_{IC} = 2.5V	25°C		0.6	60	pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range(3)			25°C	−0.2 to 4	−0.2 to 4.2		V
				–40°C to +85°C	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100mV, R_L = 1MΩ	25°C	3.2	4.1		V
				−40°C	3	4.1		
				85°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100mV, I_{OL} = 0mA	25°C		1	50	mV
				−40°C		1	50	
				85°C		1	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25V to 2V, R_L = 1MΩ	25°C	50	480		V/mV
				−40°C	50	900		
				85°C	50	330		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	87		dB
				−40°C	60	85		
				85°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5V to 10V, V_O = 1.4V	25°C	70	97		dB
				−40°C	60	97		
				85°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5V, V_{IC} = 2.5V, no load	25°C		20	34	μA
				−40°C		31	54	
				85°C		15	26	

(1) Typical values of input bias current and input offset current less than 5pA determined mathematically.
(2) Values specified by characterization.
(3) This range also applies to each input individually.

5.9 Operating Characteristics, V_{DD} = 5V, I Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLC27L2I, TLC27L2AI, TLC27L2BI, TLC27L7I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1MΩ, C_L = 20pF, see Figure 6-1	$V_{I(PP)}$ = 1V	25°C		0.03		V/µs
				−40°C		0.04		
				85°C		0.03		
			$V_{I(PP)}$ = 2.5V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2		25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1MΩ, C_L = 20pF, see Figure 6-1		25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10mV, C_L = 20pF, see Figure 6-3		25°C		85		kHz
				−40°C		110		
				85°C		55		
ϕ_m	Phase margin	V_I = 10mV, C_L = 20pF, f = B_1, see Figure 6-3		25°C		34°		°
				−40°C		38°		
				85°C		29°		

5.10 Electrical Characteristics, V_{DD} = 10V, I Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	TLC27L2I, TLC27L2AI, TLC27L2BI, TLC27L7I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		1.1	10	mV
				−40°C to +85°C			13	
		TLC27L2AI	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		0.9	5	
				−40°C to +85°C			7	
		TLC27L2BI	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		235	2000	µV
				−40°C to +85°C			3500	
		TLC27L7I	V_O = 1.4V, R_s = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		210	1000	
				−40°C to +85°C			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1		µV/°C
I_{IO}	Input offset current(1) (2)		V_O = 5V, V_{IC} = 5V	25°C		0.5	60	pA
				85°C		26	1000	
I_{IB}	Input bias current(1) (2)		V_O = 5V, V_{IC} = 5V	25°C		0.7	60	pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range(3)			25°C	−0.2 to 9	−0.2 to 9.2		V
				−40°C to +85°C	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100mV, R_L = 1MΩ	25°C	8	8.9		V
				−40°C	7.8	8.9		
				85°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100mV, I_{OL} = 0mA	25°C		5	50	mV
				−40°C		5	50	
				85°C		5	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1V to 6V, R_L = 1MΩ	25°C	50	860		V/mV
				−40°C	50	1550		
				85°C	50	585		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	94		dB
				−40°C	60	93		
				85°C	60	93		
k_{SVR}	Supply-voltage rejection ratio (ΔVDD/ΔVIO)		V_{DD} = 5V to 10V, V_O = 1.4V	25°C	70	97		dB
				−40°C	60	97		
				85°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5V, V_{IC} = 5V, no load	25°C		29	46	µA
				−40°C		49	86	
				85°C		20	36	

(1) Typical values of input bias current and input offset current less than 5pA determined mathematically.
(2) Values specified by characterization.
(3) This range also applies to each input individually.

5.11 Operating Characteristics, V_{DD} = 10V, I Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLC27L2I, TLC27L2AI, TLC27L2BI, TLC27L7I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1MΩ, C_L = 20pF, see Figure 6-1	$V_{I(PP)}$ = 1V	25°C		0.05		V/µs
				−40°C		0.06		
				85°C		0.03		
			$V_{I(PP)}$ = 5.5V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2		25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1MΩ, C_L = 20pF, see Figure 6-1		25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_I = 10mV, C_L = 20pF, see Figure 6-3		25°C		110		kHz
				−40°C		110		
				85°C		80		
ϕ_m	Phase margin	V_I = 10mV, C_L = 20pF, f = B_1, see Figure 6-3		25°C		38°		°
				−40°C		42°		
				85°C		32°		

5.12 Electrical Characteristics, V_{DD} = 5V, M Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC27L2M			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		1.1	10	mV
			−55°C to +125°C			12	
αV_{IO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current(1) (2)	V_O = 2.5V, V_{IC} = 2.5V	25°C		0.5	60	pA
			125°C		1.4	15	nA
I_{IB}	Input bias current(1) (2)	V_O = 2.5V, V_{IC} = 2.5V	25°C		0.6	60	pA
			125°C		9	35	nA
V_{ICR}	Common-mode input voltage range(3)		25°C	0 to 4	−0.2 to 4.2		V
			−55°C to +125°C	0 to 3.5			V
V_{OH}	High-level output voltage	V_{ID} = 100mV, R_L = 1MΩ	25°C	3.2	4.1		V
			−55°C	3	4.1		
			125°C	3	4.2		
V_{OL}	Low-level output voltage	V_{ID} = −100mV, I_{OL} = 0mA	25°C		1	50	mV
			−55°C		1	50	
			125°C		1	50	
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25V to 2V, R_L = 1MΩ	25°C	50	500		V/mV
			−55°C	25	1000		
			125°C	25	200		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	87		dB
			−55°C	60	85		
			125°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5V to 10V, V_O = 1.4V	25°C	70	97		dB
			−55°C	60	97		
			125°C	60	98		
I_{DD}	Supply current (two amplifiers)	V_O = 2.5V, V_{IC} = 2.5V, no load	25°C		20	34	µA
			−55°C		35	60	
			125°C		14	24	

(1) Typical values of input bias current and input offset current less than 5pA determined mathematically.
(2) Values specified by characterization.
(3) This range also applies to each input individually.

5.13 Operating Characteristics, V_{DD} = 5V, M Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLC27L2M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1MΩ, C_L = 20pF, see Figure 6-1	$V_{I(PP)}$ = 1V	25°C		0.03		V/µs
				−55°C		0.04		
				125°C		0.02		
			$V_{I(PP)}$ = 2.5V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2		25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1MΩ, C_L = 20pF, see Figure 6-1		25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_I = 10mV, C_L = 20pF, see Figure 6-3		25°C		85		kHz
				−55°C		110		
				125°C		45		
ϕ_m	Phase margin	V_I = 10mV, C_L = 20pF, f = B1, see Figure 6-3		25°C		34°		°
				−55°C		39°		
				125°C		25°		

5.14 Electrical Characteristics, V_{DD} = 10V, M Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC27L2M			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4V, R_S = 50Ω, V_{IC} = 0V, R_L = 1MΩ	25°C		1.1	10	mV
			−55 °C to +125°C			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current(1) (2)	V_O = 5V, V_{IC} = 5V	25°C		0.5	60	pA
			125°C		1.8	15	nA
I_{IB}	Input bias current(1) (2)	V_O = 5V, V_{IC} = 5V	25°C		0.7	60	pA
			125°C		10	35	nA
V_{ICR}	Common-mode input voltage range(3)		25°C	0 to 9	−0.2 to 9.2		V
			−55 °C to +125°C	0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100mV, R_L = 1MΩ	25°C	8	8.9		V
			−55°C	7.8	8.8		
			125°C	7.8	9		
V_{OL}	Low-level output voltage	V_{ID} = −100mV, I_{OL} = 0mA	25°C		5	50	mV
			−55°C		5	50	
			125°C		5	50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1V to 6V, R_L = 1MΩ	25°C	50	860		V/mV
			−55°C	25	1750		
			125°C	25	380		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	94		dB
			−55°C	60	93		
			125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5V to 10V, V_O = 1.4V	25°C	70	97		dB
			−55°C	60	97		
			125°C	60	98		
I_{DD}	Supply current (two amplifiers)	V_O = 5V, V_{IC} = 5V, no load	25°C		29	46	µA
			−55°C		56	96	
			125°C		18	30	

(1) Typical values of input bias current and input offset current less than 5pA determined mathematically.
(2) Values specified by characterization.
(3) This range also applies to each input individually.

5.15 Operating Characteristics, V_{DD} = 10V, M Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLC27L2M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1MΩ, C_L = 20pF, see Figure 6-1	$V_{I(PP)}$ = 1V	25°C		0.05		V/µs
				−55°C		0.06		
				125°C		0.03		
			$V_{I(PP)}$ = 5.5V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2		25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1MΩ, C_L = 20pF, see Figure 6-1		25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_I = 10mV, C_L = 20pF, see Figure 6-3		25°C		110		kHz
				−55°C		110		
				125°C		70		
ϕ_m	Phase margin	V_I = 10mV, C_L = 20pF, f = B_1, see Figure 6-3		25°C		38°		°
				−55°C		43°		
				125°C		29°		

5.16 Typical Characteristics

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Table 5-1. Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	Figure 5-1, Figure 5-2
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	Figure 5-3, Figure 5-4
V_{OH}	High-level output voltage	vs High-level output current	Figure 5-5, Figure 5-6
		vs Supply voltage	Figure 5-7
		vs Free-air temperature	Figure 5-8
V_{OL}	Low-level output voltage	vs Differential input voltage	Figure 5-9, Figure 5-11
		vs Free-air temperature	Figure 5-10, Figure 5-12
		vs Low-level output current	Figure 5-13, Figure 5-14
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	Figure 5-15
		vs Free-air temperature	Figure 5-16
		vs Frequency	Figure 5-25, Figure 5-26
I_{IB}	Input bias current	vs Free-air temperature	Figure 5-17
I_{IO}	Input offset current	vs Free-air temperature	Figure 5-17
V_{IC}	Common-mode input voltage	vs Supply voltage	Figure 5-18
I_{DD}	Supply current	vs Supply voltage	Figure 5-19
		vs Free-air temperature	Figure 5-20
SR	Slew rate	vs Supply voltage	Figure 5-21
		vs Free-air temperature	Figure 5-22
	Normalized slew rate	vs Free-air temperature	Figure 5-23
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	Figure 5-24
ϕ_m	Phase margin	vs Supply voltage	Figure 5-27
		vs Free-air temperature	Figure 5-28
		vs Capacitive Load	Figure 5-29
V_n	Equivalent input noise voltage	vs Frequency	Figure 5-30
	Phase shift	vs Frequency	Figure 5-25, Figure 5-26

5.16 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

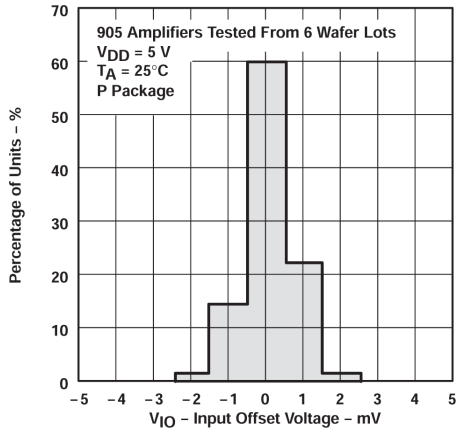


Figure 5-1. Distribution of TLC27L2 Input Offset Voltage

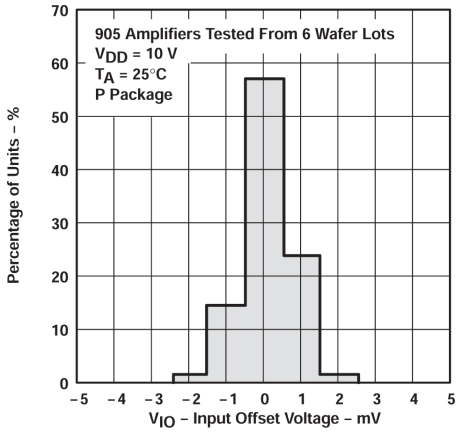


Figure 5-2. Distribution of TLC27L2 Input Offset Voltage

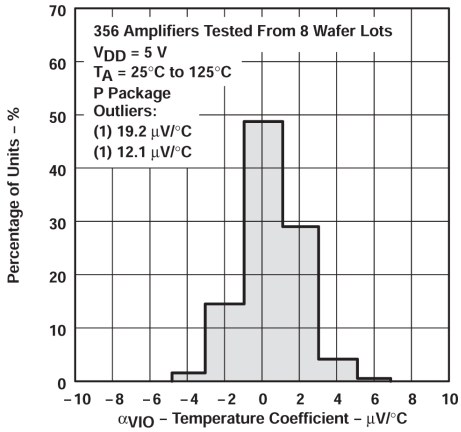


Figure 5-3. Distribution of TLC27LC and TLC27L7 Input Offset Voltage Temperature Coefficient

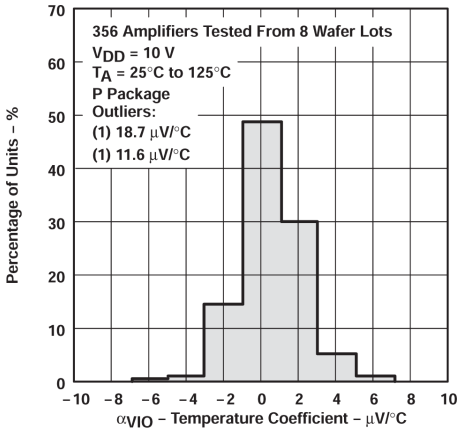


Figure 5-4. Distribution of TLC27LC and TLC27L7 Input Offset Voltage Temperature Coefficient

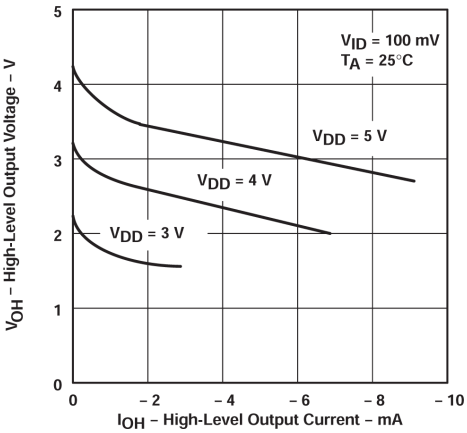


Figure 5-5. High-level Output Voltage vs High-level Output Current

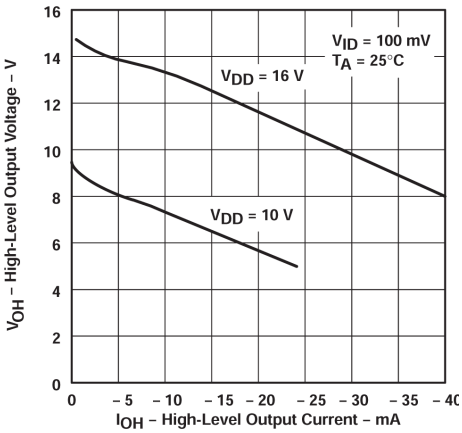


Figure 5-6. High-level Output Voltage vs High-level Output Current

5.16 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

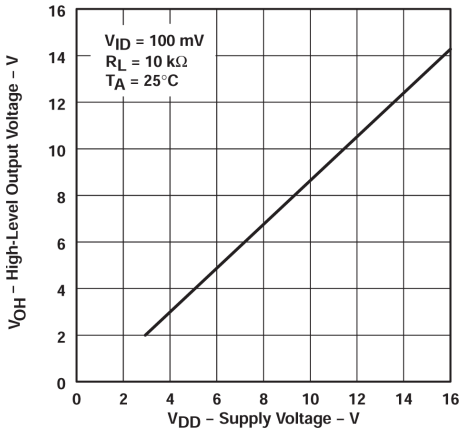


Figure 5-7. High-level Output Voltage vs Supply Voltage

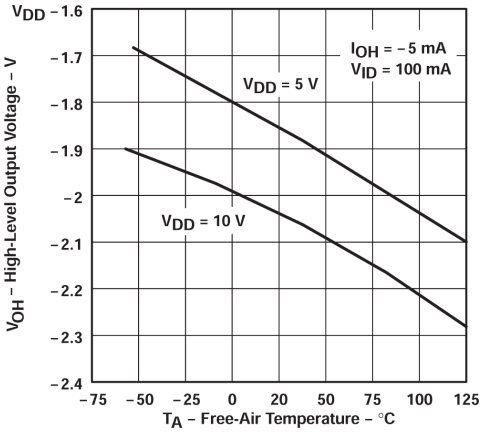


Figure 5-8. High-level Output Voltage vs Free-air Temperature

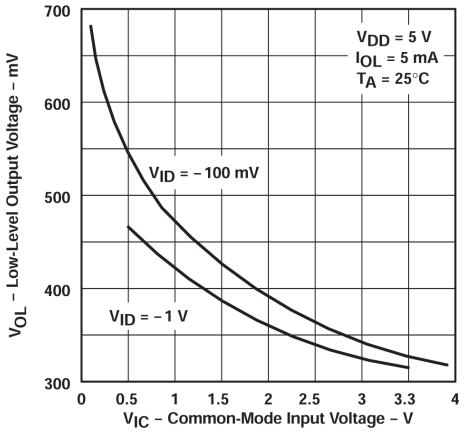


Figure 5-9. Low-level Output Voltage vs Differential Input Voltage

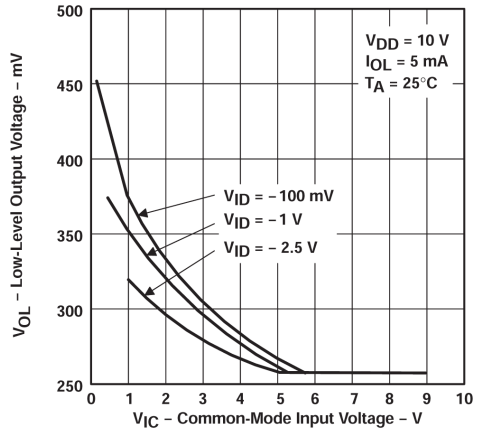


Figure 5-10. Low-level Output Voltage vs Free-air Temperature

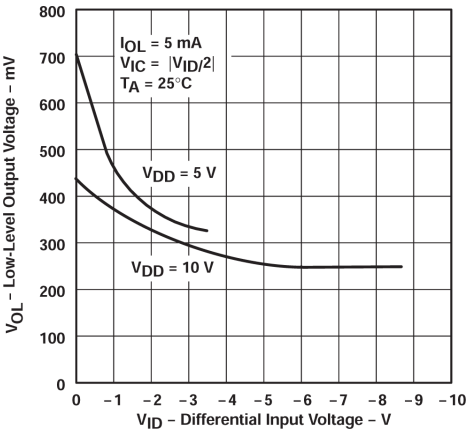


Figure 5-11. Low-level Output Voltage vs Differential Input Voltage

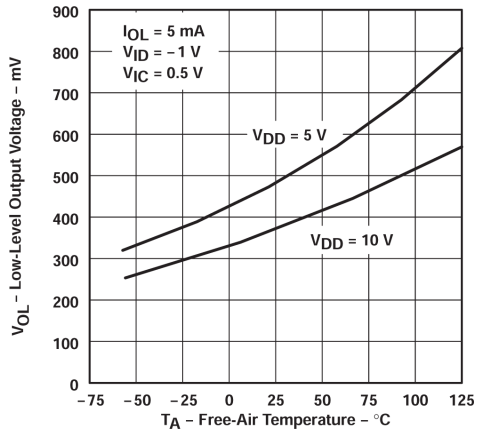


Figure 5-12. Low-level Output Voltage vs Free-air Temperature

5.16 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

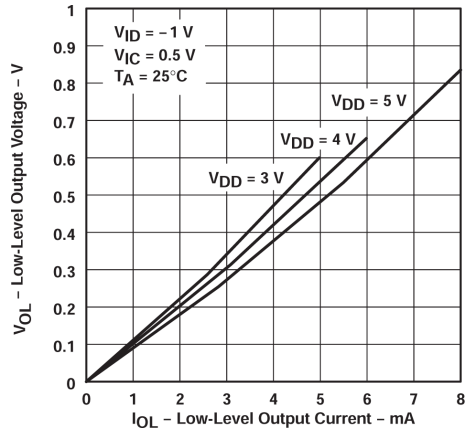


Figure 5-13. Low-level Output Voltage vs Low-level Output Current

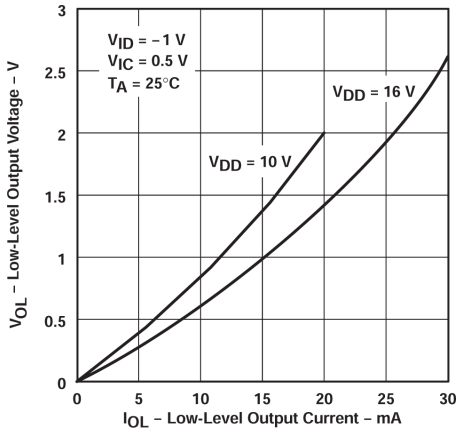


Figure 5-14. Low-level Output Voltage vs Low-level Output Current

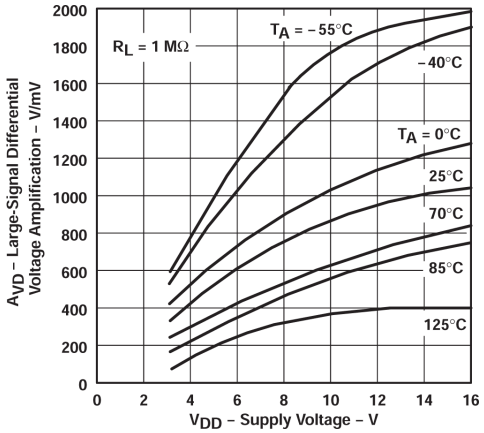


Figure 5-15. Large-signal Differential Voltage Amplification vs Supply Voltage

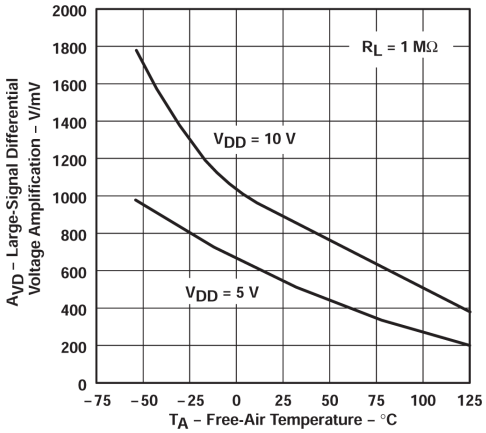
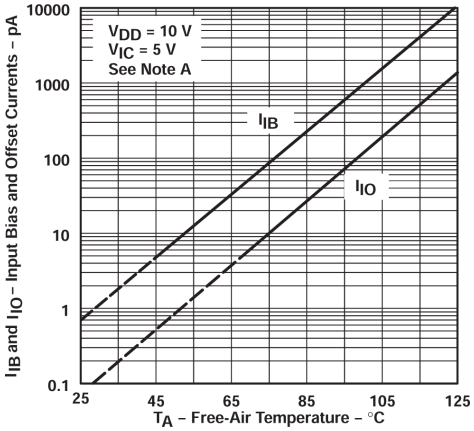


Figure 5-16. Large-signal Differential Voltage Amplification vs Free-air Temperature



Typical values of input bias current and input offset current less than 5pA determined mathematically.

Figure 5-17. Input Bias Current and Input Offset Current vs Free-air Temperature

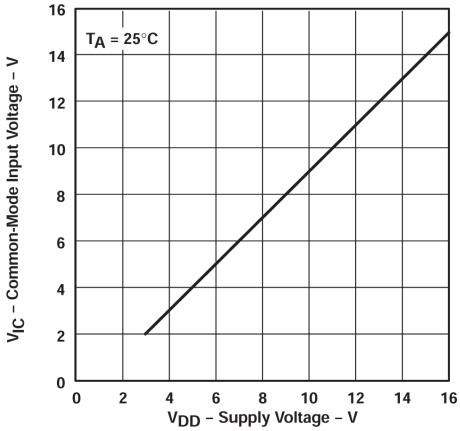


Figure 5-18. Common-mode Input Voltage Positive Limit vs Supply Voltage

5.16 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

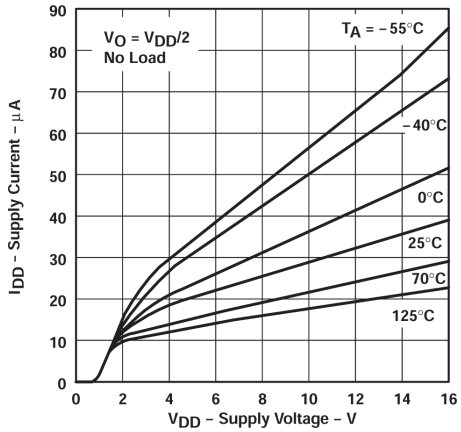


Figure 5-19. Supply Current vs Supply Voltage

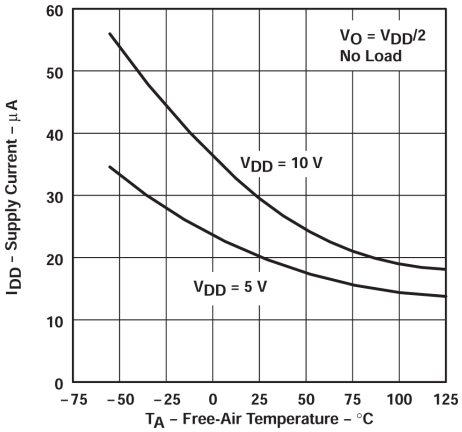


Figure 5-20. Supply Current vs Free-air Temperature

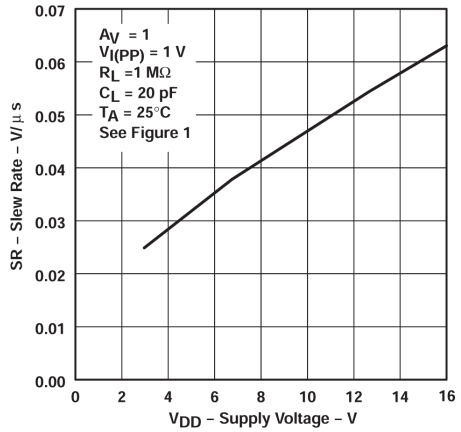


Figure 5-21. Slew Rate vs Supply Voltage

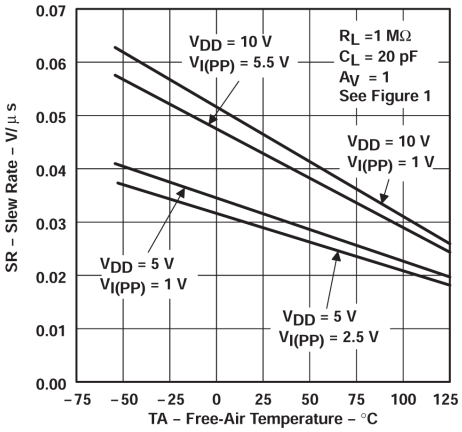


Figure 5-22. Slew Rate vs Free-air Temperature

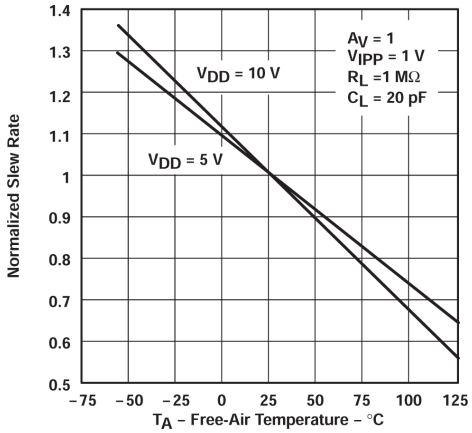


Figure 5-23. Normalized Slew Rate vs Free-air Temperature

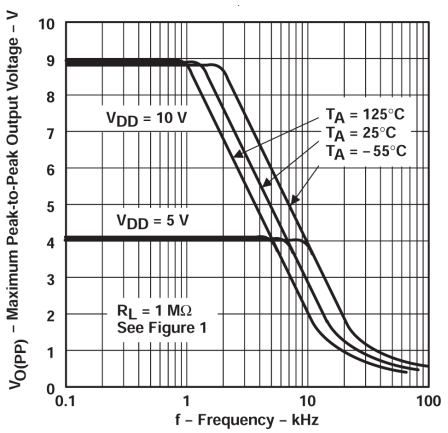


Figure 5-24. Maximum-peak-to-peak Output Voltage vs Frequency

5.16 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

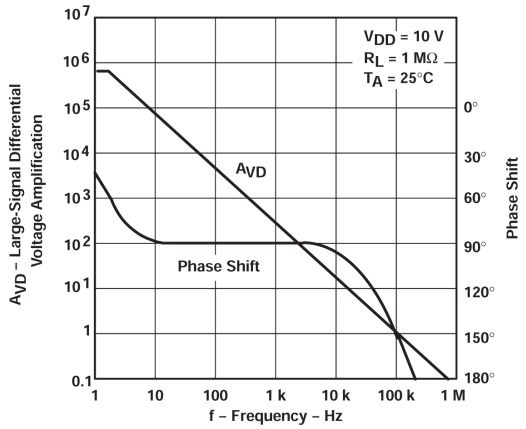


Figure 5-25. Large-signal Differential Voltage Amplification and Phase Shift vs Frequency

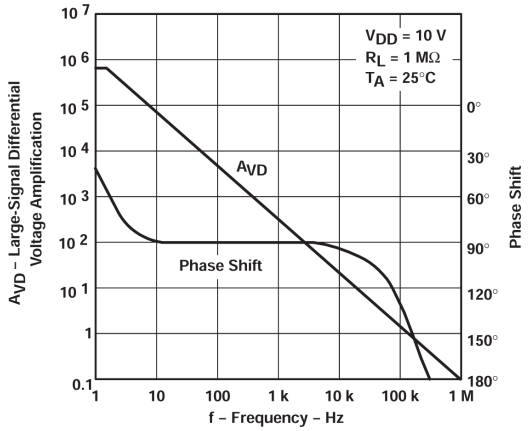


Figure 5-26. Large-signal Differential Voltage Amplification and Phase Shift vs Frequency

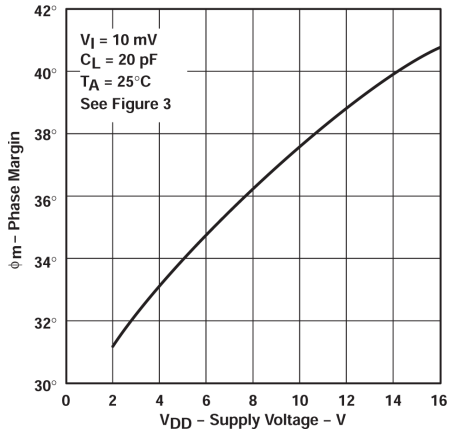


Figure 5-27. Phase Margin vs Supply Voltage

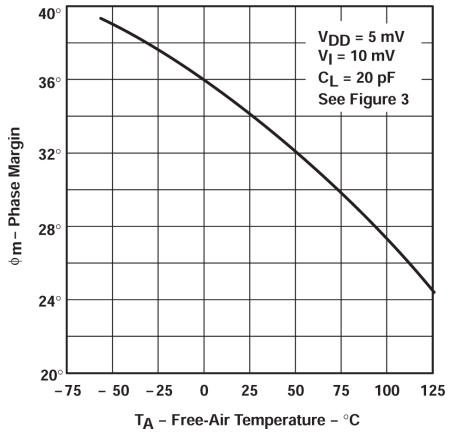


Figure 5-28. Phase Margin vs Free-air Temperature

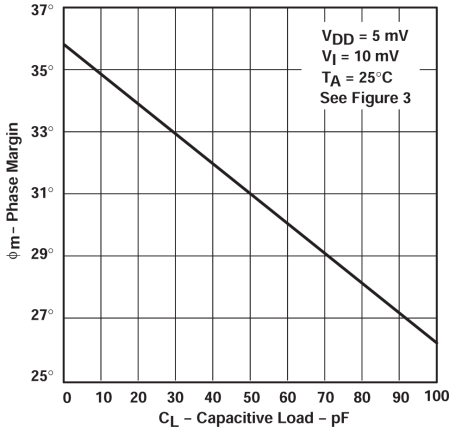


Figure 5-29. Phase Margin vs Capacitive Load

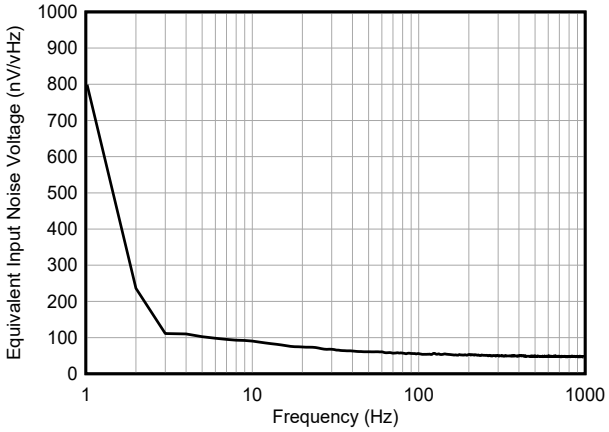


Figure 5-30. Equivalent Input Noise Voltage vs Frequency

6 Parameter Measurement Information

6.1 Single-Supply Versus Split-Supply Test Circuits

The TLC27Lx are optimized for single-supply operation. Circuit configurations used for the various tests often present some inconvenience because in many cases, the input signal is offset from ground. Avoid this inconvenience by testing the device with split supplies and the output load tied to the negative rail. The following figures show a comparison of single-supply versus split-supply test circuits. The use of either circuit gives the same result.

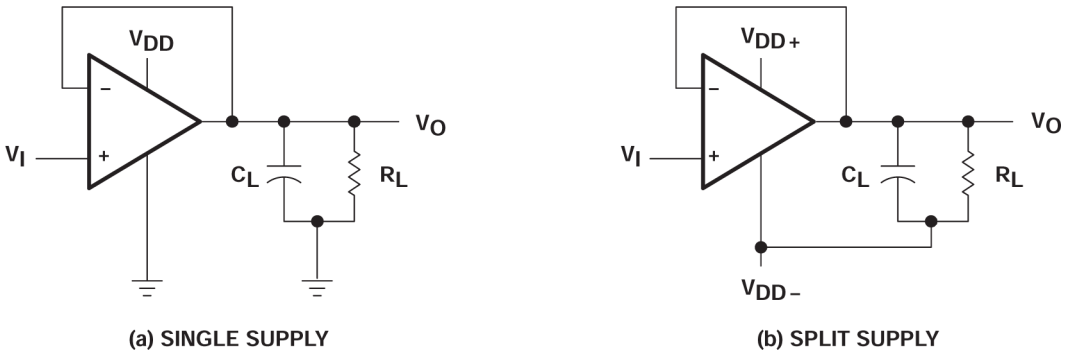


Figure 6-1. Unity-Gain Amplifier

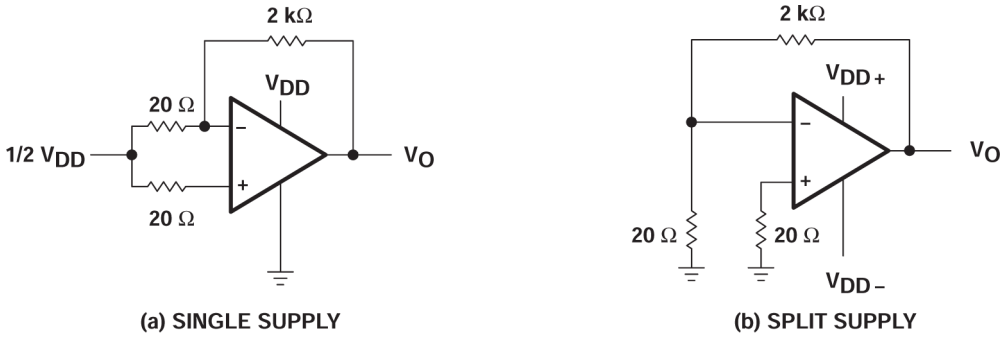


Figure 6-2. Noise-Test Circuit

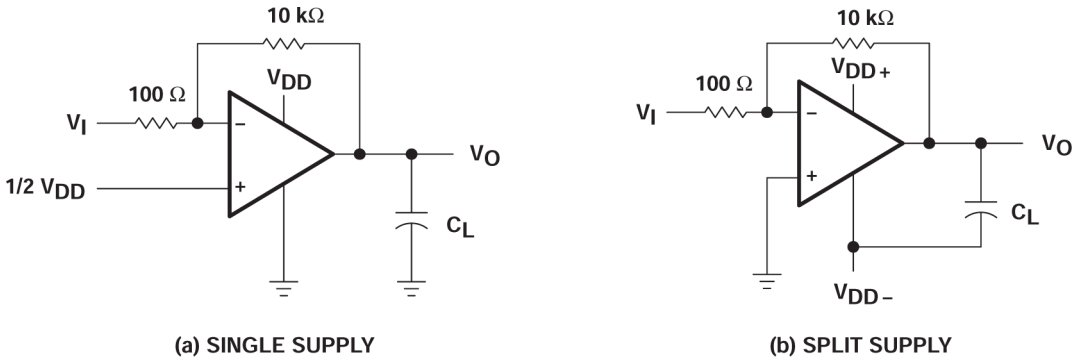


Figure 6-3. Gain-of-100 Inverting Amplifier

6.2 Input Bias Current

Because of the high input impedance of the TLC27Lx operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 6-4). Leakages that can otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

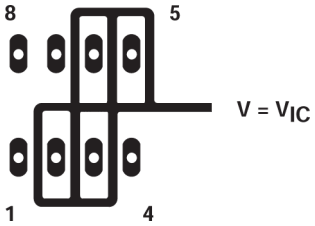


Figure 6-4. Isolation Metal around Device Inputs (P Package)

6.3 Low-Level Output Voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, observe these two conditions. If conditions other than these are to be used, see the *Typical Characteristics* in Section 5.16.

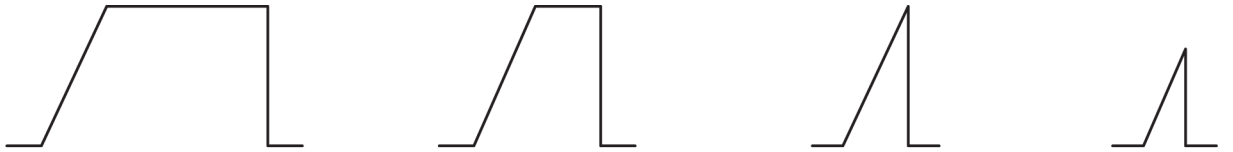
6.4 Input Offset Voltage Temperature Coefficient

Erroneous readings often result from attempts to measure the temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is less than freezing, moisture is able to collect on both the device and the test socket. This moisture results in leakage and contact resistance that potentially causes erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage because the moisture also covers the isolation metal, thereby rendering the techniques useless. Perform these measurements at temperatures greater than freezing to minimize error.

6.5 Full-Power Response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is typically measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal. When the output shows significant distortion, the input frequency is noted as the full-linear bandwidth. The full-peak response is defined as the maximum output frequency, without regard to distortion, at which the full peak-to-peak output swing is maintained. When the output frequency is greater than the full-peak response bandwidth, or maximum output-swing bandwidth, the full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet, and is measured using the circuit in Figure 6-1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 6-5). A square wave allows a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 100 kHz (b) B_{OM} > f > 100 kHz (c) f = B_{OM} (d) f > B_{OM}

Figure 6-5. Full-Power-Response Output Signal

6.6 Test Time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than bipolar and BiFET devices. The problem becomes more pronounced with reduced supply levels and lower temperatures.

7 Application and Implementation

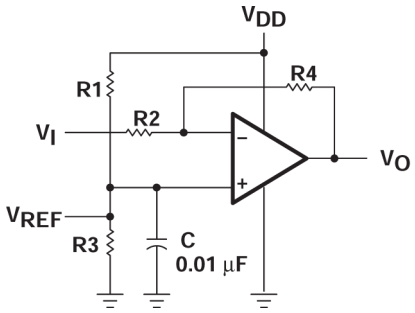
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Single-Supply Operation

While the TLC27Lx perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This optimization includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS. For maximum dynamic range, 16V single-supply operation is recommended.



$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

Figure 7-1. Inverting Amplifier with Voltage Reference

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is typically sufficient to establish this reference level (see Figure 7-1). The low-input bias-current consumption of the TLC27Lx permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27Lx work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, take the following recommended precautions:

1. Power linear devices from separate bypassed supply lines (see Figure 7-2); otherwise, linear device supply rails potentially fluctuate as a result of voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling is probably necessary in high-frequency applications.

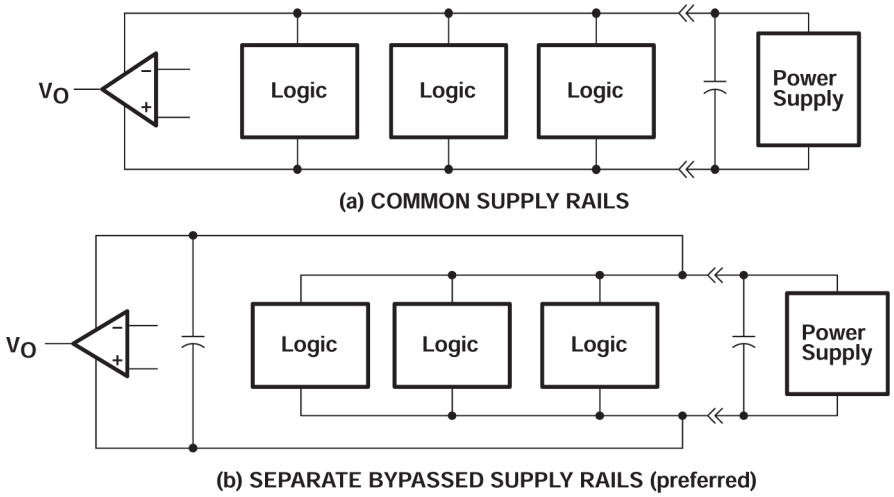


Figure 7-2. Common Versus Separate Supply Rails

7.1.2 Input Characteristics

The TLC27Lx are specified with a minimum and a maximum input voltage that, if exceeded at either input, possibly causes the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} − 1V at T_A = 25°C and at V_{DD} − 1.5V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the legacy TLC27Lx very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time is calculated to be typically 0.1μV/month, including the first month of operation.

Migration from the legacy 150mm LinCMOS process to a 300mm diameter wafer process has brought associated improvements to input offset voltage precision. The new silicon also features improved slew rate, supply-voltage rejection ratio, and voltage noise. However, this change does introduce a new crossover region, where shifts in input offset (typically 300μV–400μV) occur as the input common-mode voltage approaches the V_{DD} rail. Figure 7-3 and Figure 7-4 plot the mean and standard deviation of this characteristic at various temperatures for a 10V supply.

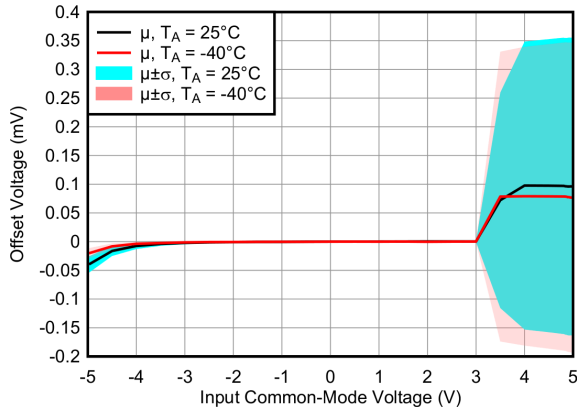


Figure 7-3. Offset Voltage vs Input Common-mode Voltage

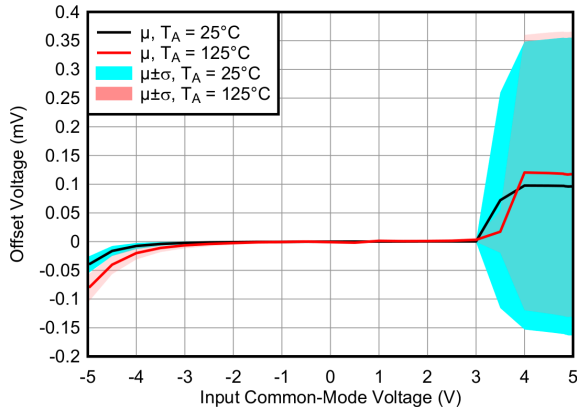


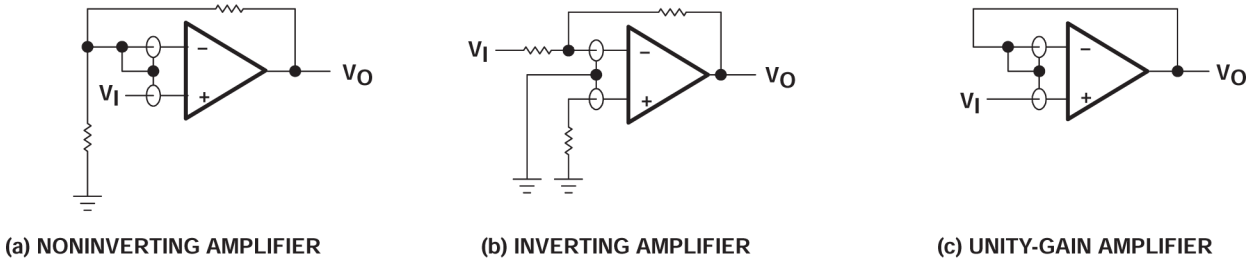
Figure 7-4. Offset Voltage vs Input Common-mode Voltage

Because of the extremely high input impedance and resulting low bias-current requirements, the TLC27Lx are an excellent choice for low-level signal processing. However, leakage currents on printed-circuit boards and sockets sometimes easily exceed bias-current requirements and cause a degradation in device performance. As best practice, include guard rings around inputs (similar to those of Figure 6-4 in the *Parameter Measurement Information* section). Drive these guards from a low-impedance source at the same voltage level as the common-mode input (see Figure 7-5).

Tie the inputs of any unused amplifiers to ground to avoid possible oscillation.

7.1.3 Noise Performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias-current requirements of the TLC27Lx result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50kΩ because bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 7-5. Guard-Ring Schemes

7.1.4 Feedback

Operational amplifier circuits almost always employ feedback, and because feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 7-6). The value of this capacitor is optimized empirically.

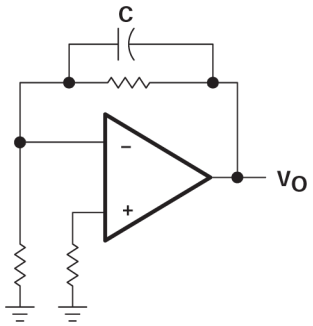


Figure 7-6. Compensation for Input Capacitance

7.1.5 Electrostatic Discharge Protection

The TLC27Lx incorporate an internal electrostatic-discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000V as tested under MIL-STD-883C, Method 3015.2. However, exercise care when handling these devices as exposure to ESD potentially results in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

7.1.6 Latch-Up

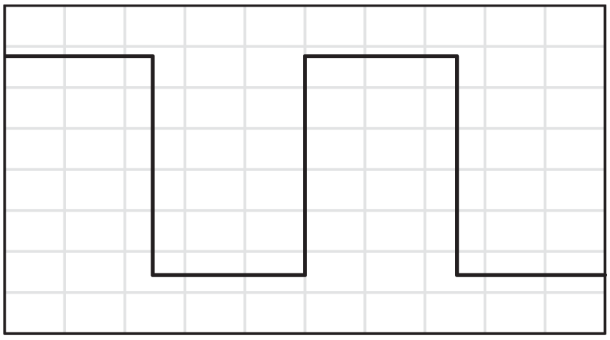
CMOS devices are susceptible to latch-up due to inherent parasitic thyristors. With this in mind, the TLC27Lx inputs and output are designed to withstand −100mA surge currents without sustaining latch-up. However, use best practices to reduce the chance of latch-up whenever possible. Do not forward bias internal-protection diodes. Do not exceed the supply voltage by more than 300mV for applied input and output voltages. Exercise care when using capacitive coupling on pulse generators. Shunt supply transients by using decoupling capacitors (0.1µF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is typically between the positive supply rail and ground, and is triggered by surges on the supply lines, voltages on either the output or inputs that exceed the supply voltage, or both. After latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and typically results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

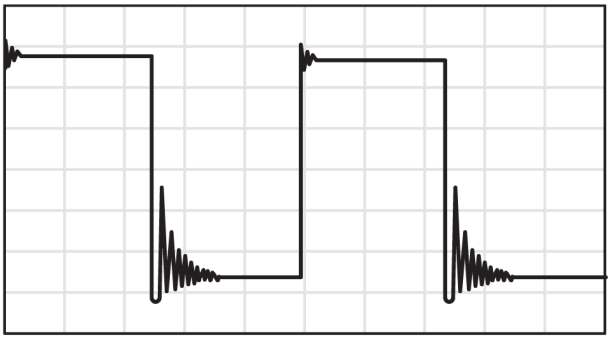
7.1.7 Output Characteristics

The output stage of the TLC27Lx is designed to sink and source relatively high amounts of current (see also Typical Characteristics). If the output is subjected to a short-circuit condition, the high-current capability is able to cause device damage under certain conditions. Output current capability increases with supply voltage.

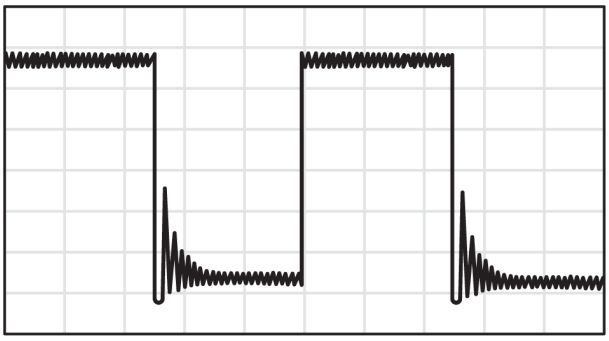
All operating characteristics of the TLC27Lx were measured using a 20pF load. The devices drive higher capacitive loads. However, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 7-7). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.



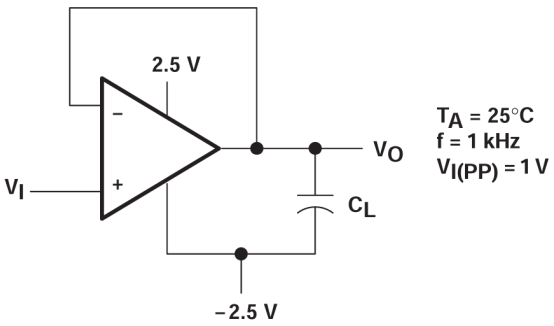
(a) C_L = 20 pF, R_L = NO LOAD



(b) C_L = 260 pF, R_L = NO LOAD



(c) C_L = 310 pF, R_L = NO LOAD



(d) TEST CIRCUIT

Figure 7-7. Effect of Capacitive Loads and Test Circuit

Although the TLC27Lx possess excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 7-8). There are two disadvantages to using this circuit. First, the NMOS pulldown transistor must sink a comparatively large amount of current. In this circuit, the pulldown transistor behaves like a linear resistor with an on-resistance between approximately 60Ω and 180Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to the pulldown resistor, and the gain of the operational amplifier is reduced at output voltage levels where the corresponding pullup resistor is not supplying the output current.

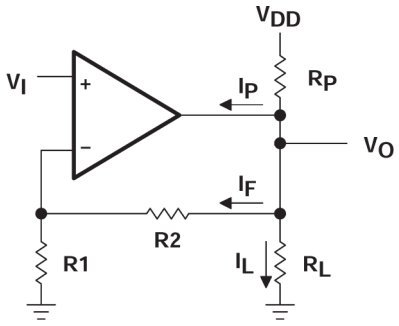


Figure 7-8. Resistive Pullup to Increase V_{OH}

7.1.8 Typical Applications

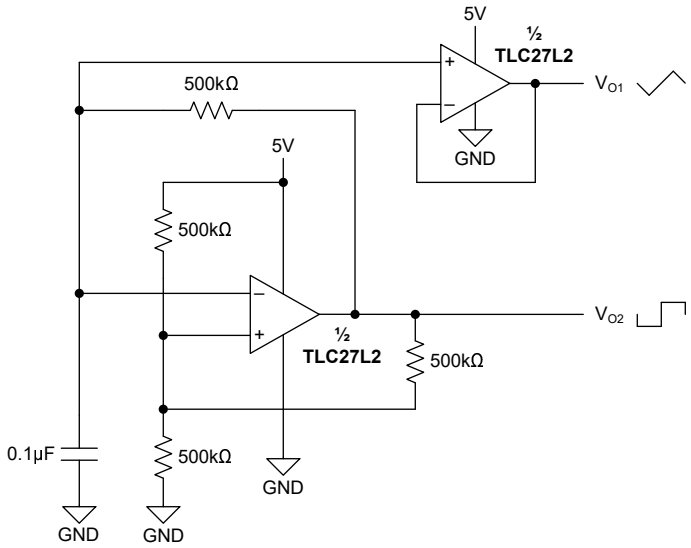


Figure 7-9. Multivibrator

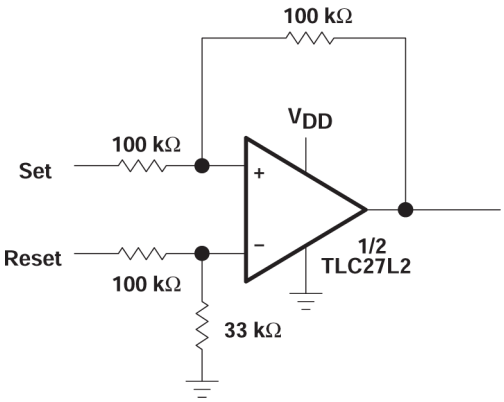
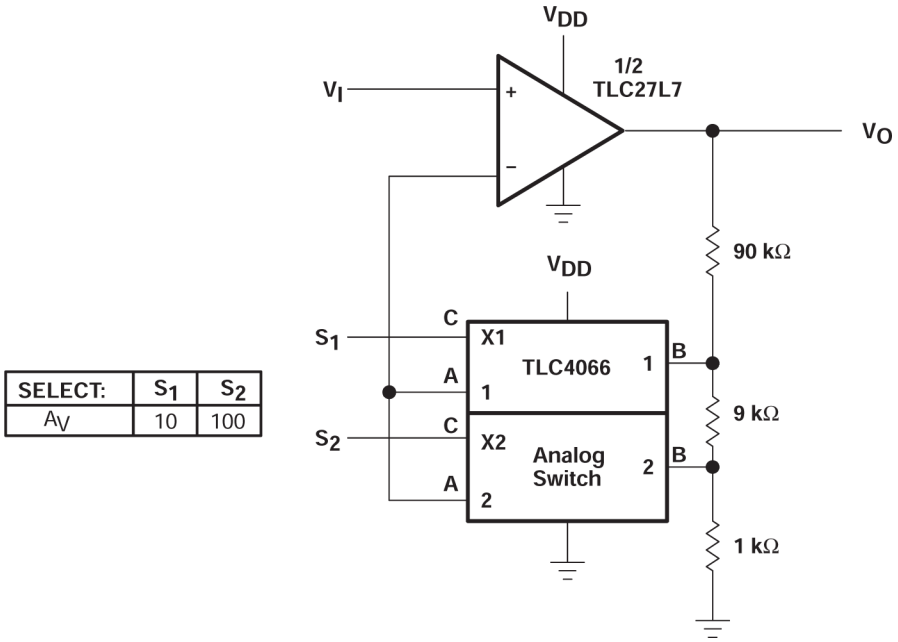


Figure 7-10. Set/Reset Flip-Flop, V_{DD} = 5V to 12V



SELECT:	S_1	S_2
A_V	10	100

Figure 7-11. Amplifier with Digital Gain Selection, V_{DD} = 5V to 16V

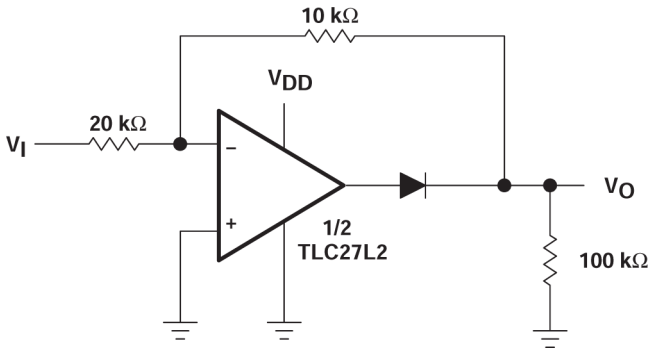


Figure 7-12. Full-Wave Rectifier, Normalized to f_c = 1kHz and R_L = 10kΩ

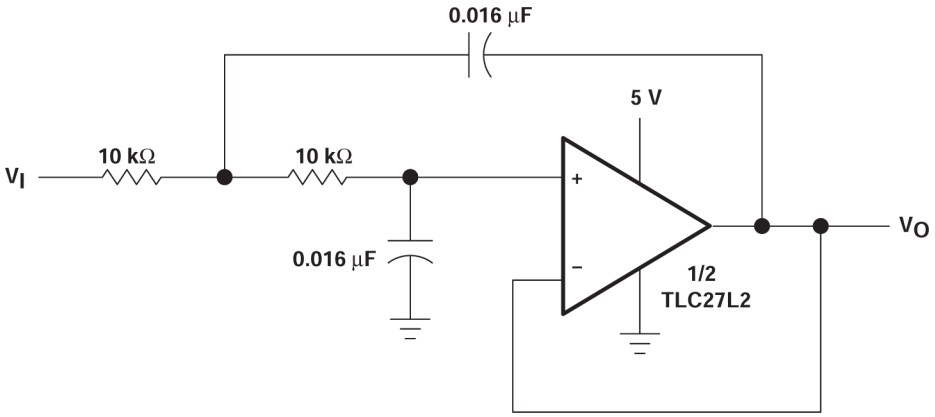
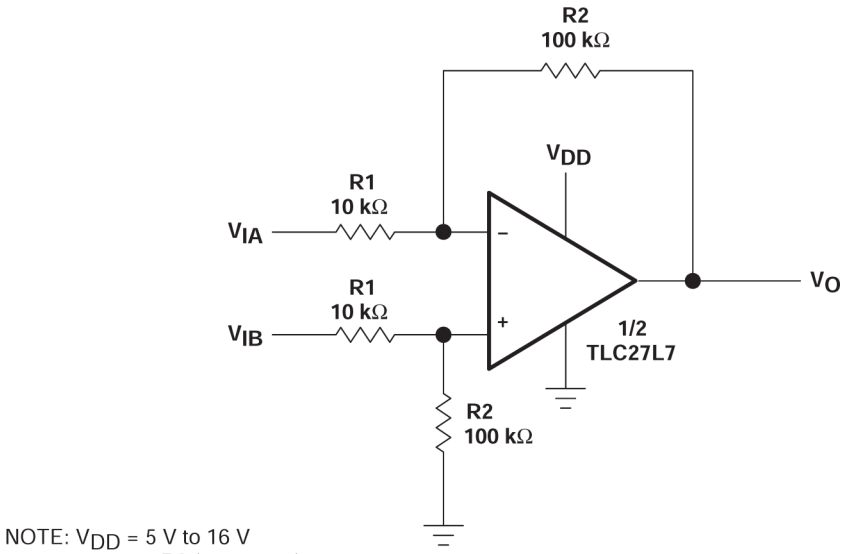


Figure 7-13. Two-Pole Low-Pass Butterworth Filter, V_{DD} = 5V to 16V



NOTE: V_{DD} = 5 V to 16 V

$$V_O = \frac{R2}{R1}\left(V_{IB} - V_{IA}\right)$$

Figure 7-14. Difference Amplifier

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

LinCMOS™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2005) to Revision E (July 2025)	Page
• Deleted obsolete TLC27L2M FK (LCCC) and JG (CDIP) packages and associated content from document	1
• Deleted obsolete TLC27L7M device and associated content from document	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *Applications*, *Pin Configuration and Functions*, *Application and Implementation*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Deleted *Equivalent Schematic* section	2
• Added *Pin Configuration and Functions* section with pin descriptions	2
• Changed typical offset voltage from 170µV to 210µV and maximum offset voltage from 500µV to 1000µV for TLC27L7C at T_A = 25°C	4
• Changed typical offset voltage from 204µV to 240µV for TLC27L2BC at T_A = 25°C	4
• Added table note that input bias current and input offset current are specified by characterization	4
• Changed typical input offset current from 0.1pA to 0.5pA	4
• Changed typical minimum input common-mode voltage for T_A = 25°C from −0.3V to −0.2V	4
• Changed typical low-level output voltage from 0mV to 1mV	4
• Changed typical CMRR at T_A = 25°C from 94dB to 87dB	4
• Changed typical CMRR at T_A = 0°C and T_A = 70°C from 95dB to 85dB	4
• Changed typical offset voltage from 190µV to 210µV and maximum offset voltage from 800µV to 1000µV for TLC27L7C at T_A = 25°C	6
• Added table note that input bias current and input offset current are specified by characterization	6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC27L2ACD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	27L2AC
TLC27L2ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2AC
TLC27L2ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2AC
TLC27L2ACP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27L2AC
TLC27L2ACP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27L2AC
TLC27L2ACPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L2A
TLC27L2ACPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L2A
TLC27L2ACPSG4	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L2A
TLC27L2AID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	27L2AI
TLC27L2AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2AI
TLC27L2AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2AI
TLC27L2AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLC27L2AIP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27L2AI
TLC27L2AIP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27L2AI
TLC27L2BCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2BC
TLC27L2BCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2BC
TLC27L2BCDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TLC27L2BCP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27L2BC
TLC27L2BCP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27L2BC
TLC27L2BID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	27L2BI
TLC27L2BIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2BI
TLC27L2BIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2BI
TLC27L2BIP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27L2BI
TLC27L2BIP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27L2BI
TLC27L2CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	27L2C
TLC27L2CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2C
TLC27L2CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L2C
TLC27L2CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27L2CP
TLC27L2CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27L2CP

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC27L2CPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
TLC27L2CPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L2
TLC27L2CPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L2
TLC27L2CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L2
TLC27L2CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L2
TLC27L2CPSR.B	Active	Production	SO (PS) | 8	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLC27L2CPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L2
TLC27L2CPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L2
TLC27L2ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	27L2I
TLC27L2IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2I
TLC27L2IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L2I
TLC27L2IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27L2IP
TLC27L2IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27L2IP
TLC27L2IPW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 85	Y27L2
TLC27L2IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y27L2I
TLC27L2IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y27L2I
TLC27L2MD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-55 to 125	
TLC27L2MDG4	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-	
TLC27L2MDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	27L2M
TLC27L2MDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	27L2M
TLC27L7CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	27L7C
TLC27L7CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L7C
TLC27L7CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L7C
TLC27L7CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27L7CP
TLC27L7CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27L7CP
TLC27L7CPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L7
TLC27L7CPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L7
TLC27L7CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L7
TLC27L7CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L7
TLC27L7ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	27L7I
TLC27L7IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L7I

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC27L7IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L7I
TLC27L7IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLC27L7IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27L7IP
TLC27L7IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27L7IP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLC27L2, TLC27L2M :

- Catalog : TLC27L2

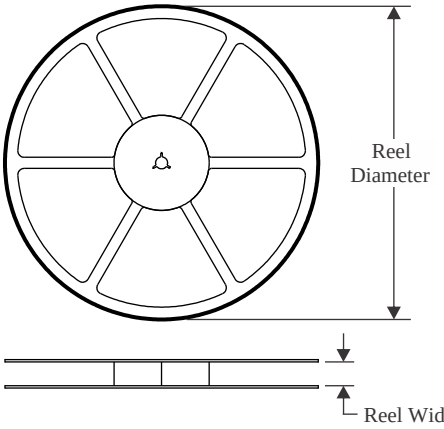
- Military : TLC27L2M

NOTE: Qualified Version Definitions:

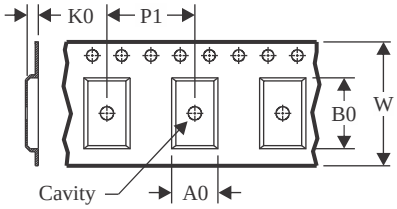
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

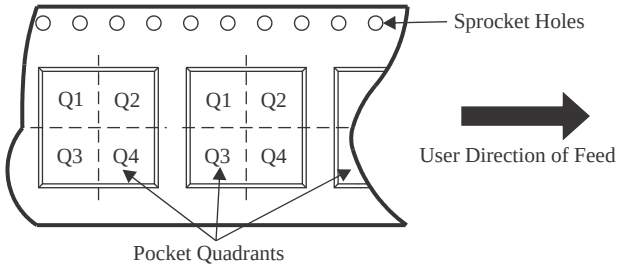


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

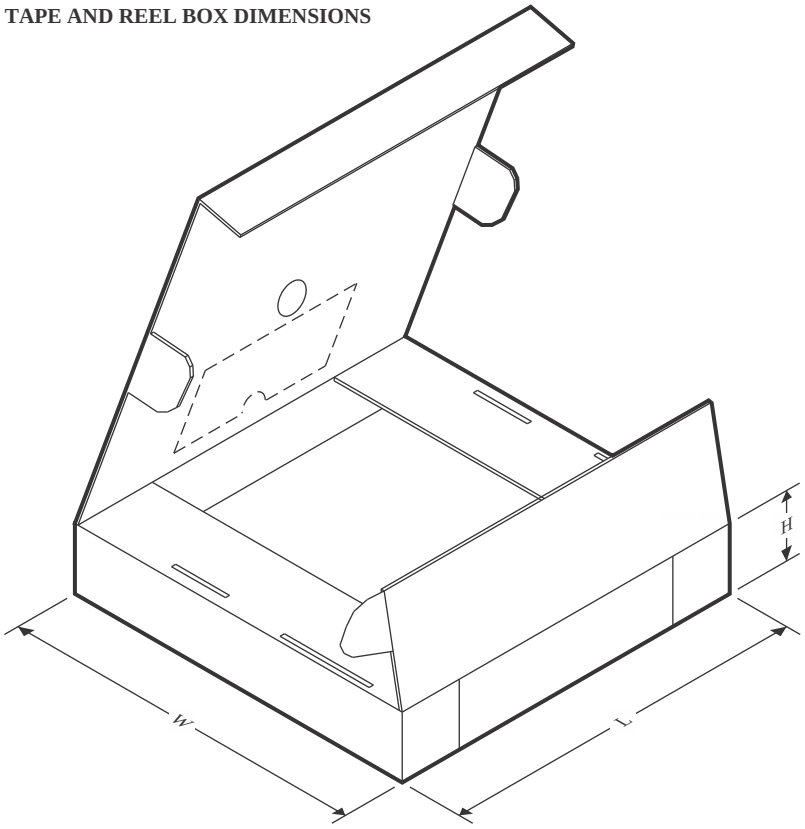


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC27L2ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TLC27L2CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC27L2IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L2IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC27L2MDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L7CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L7CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L7CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC27L7IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L7IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

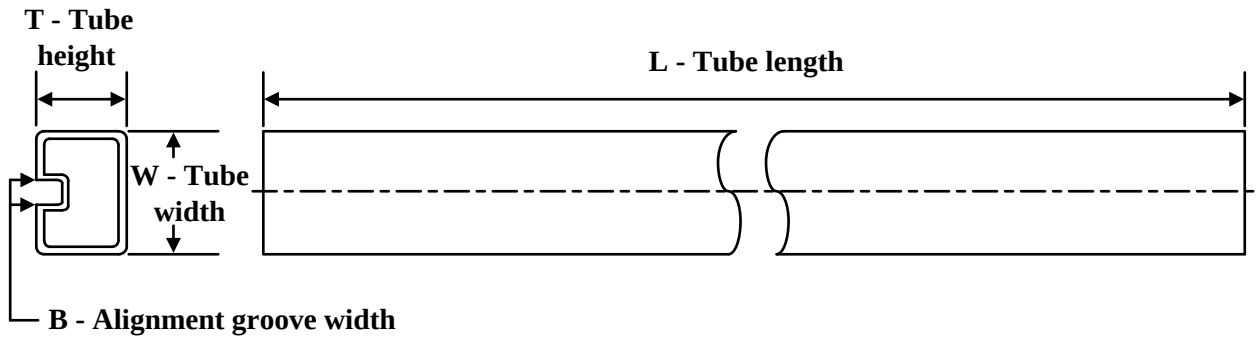
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

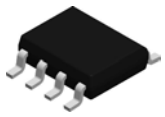
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC27L2ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC27L2ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC27L2AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27L2BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27L2BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC27L2BIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27L2BIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27L2CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27L2CPSR	SO	PS	8	2000	353.0	353.0	32.0
TLC27L2CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC27L2IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27L2IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC27L2MDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TLC27L7CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27L7CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC27L7CPSR	SO	PS	8	2000	353.0	353.0	32.0
TLC27L7IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27L7IDR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC27L2ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2ACPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC27L2ACPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC27L2ACPSG4	PS	SOP	8	80	530	10.5	4000	4.1
TLC27L2AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2AIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2BCP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2BIP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2BIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC27L2CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC27L2IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L2IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L7CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L7CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L7CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC27L7CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC27L7IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L7IP.A	P	PDIP	8	50	506	13.97	11230	4.32

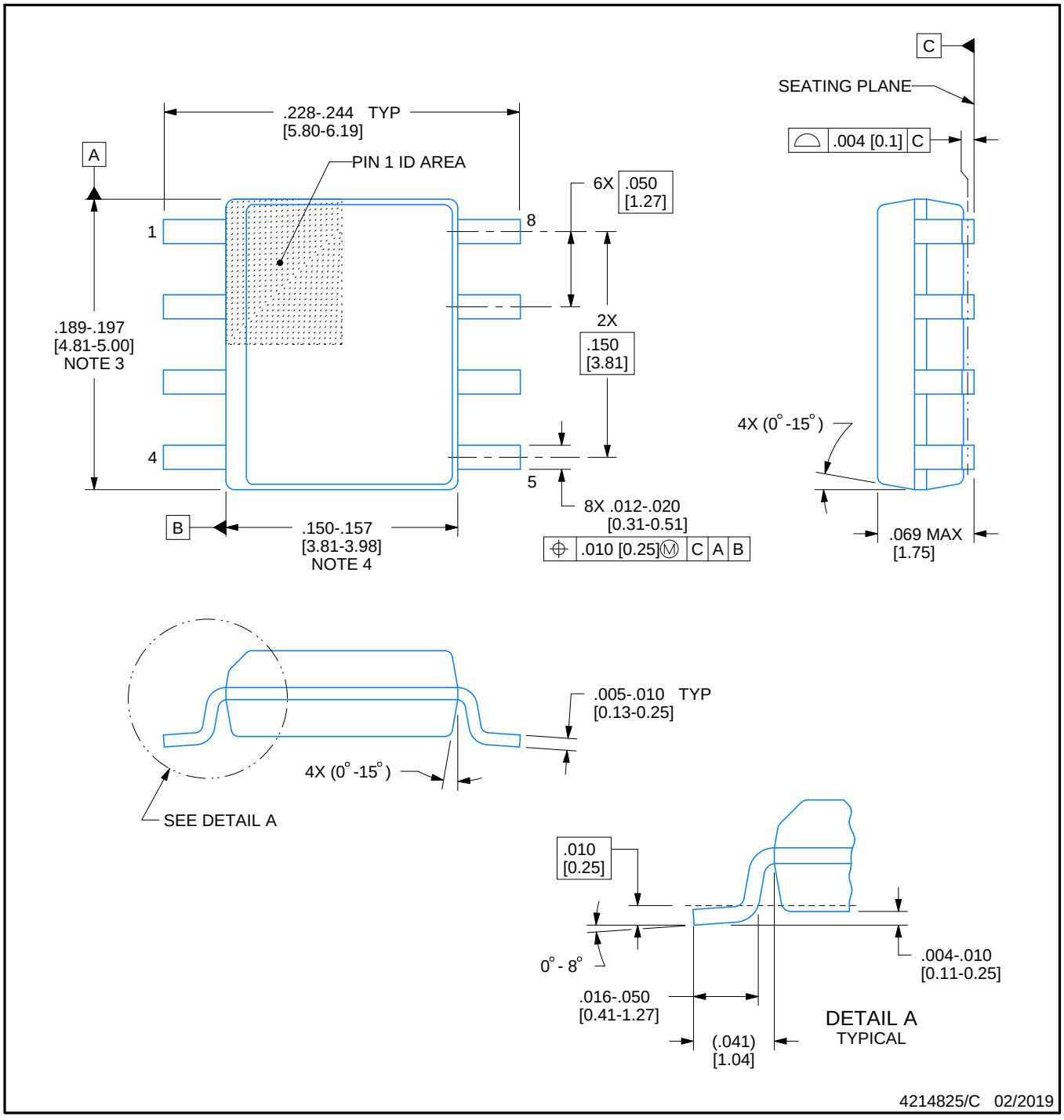


PACKAGE OUTLINE

D0008A

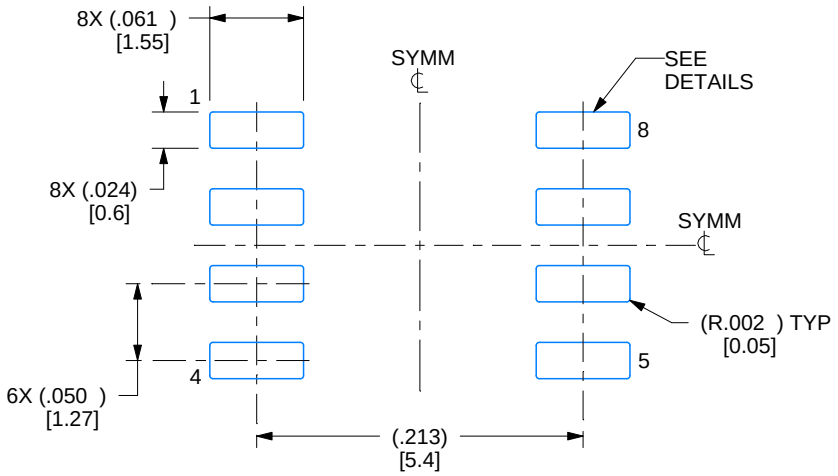
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

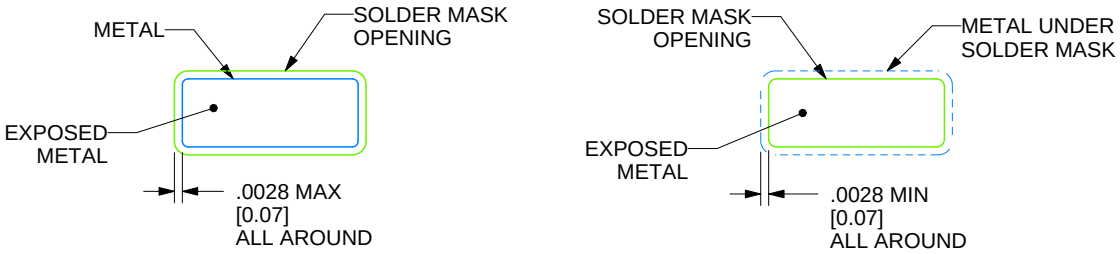


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

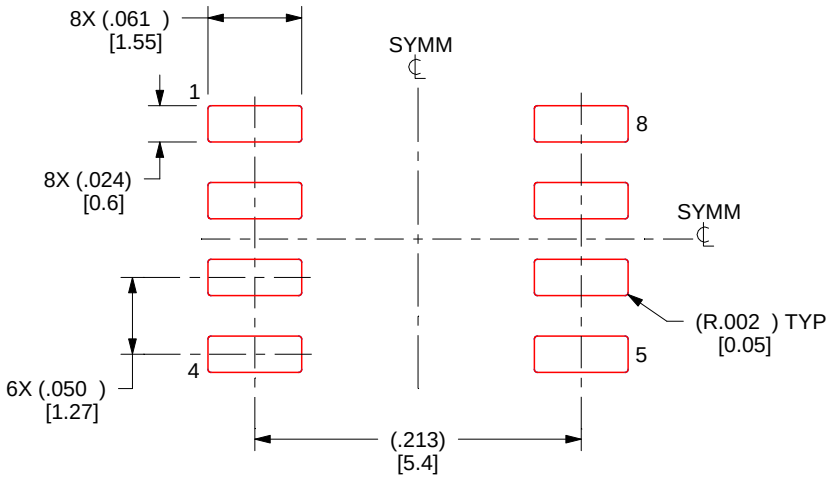
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

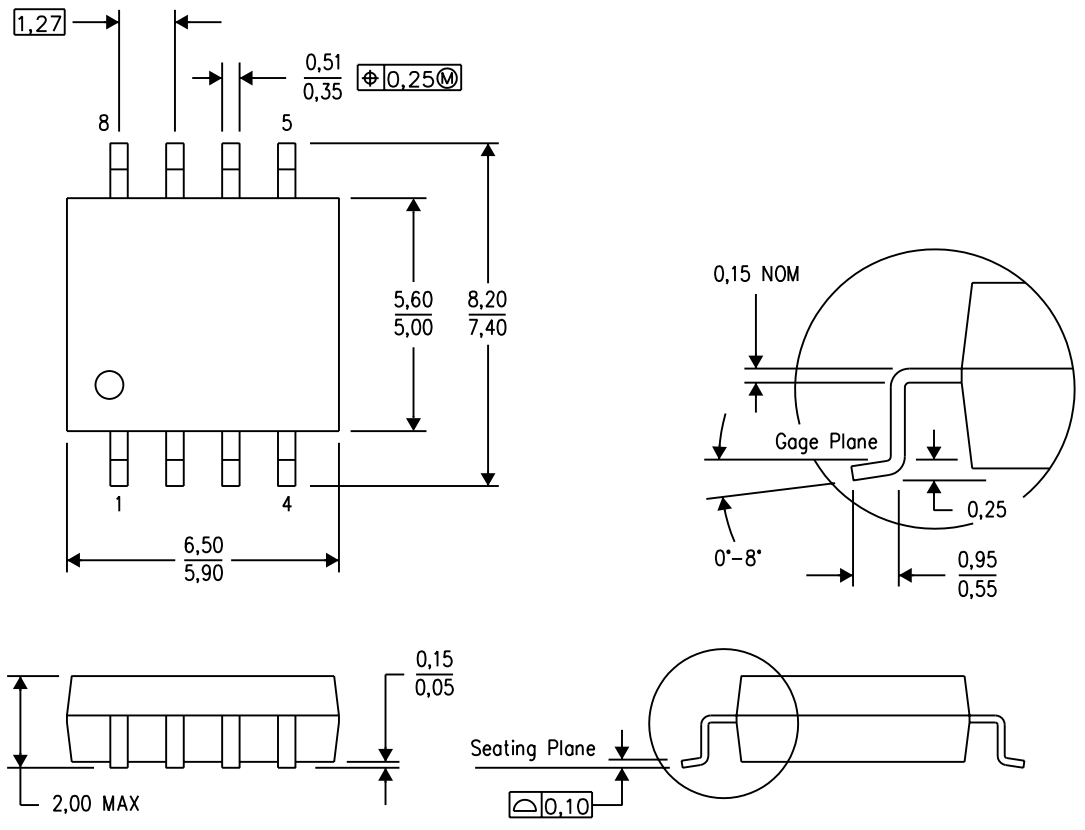
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

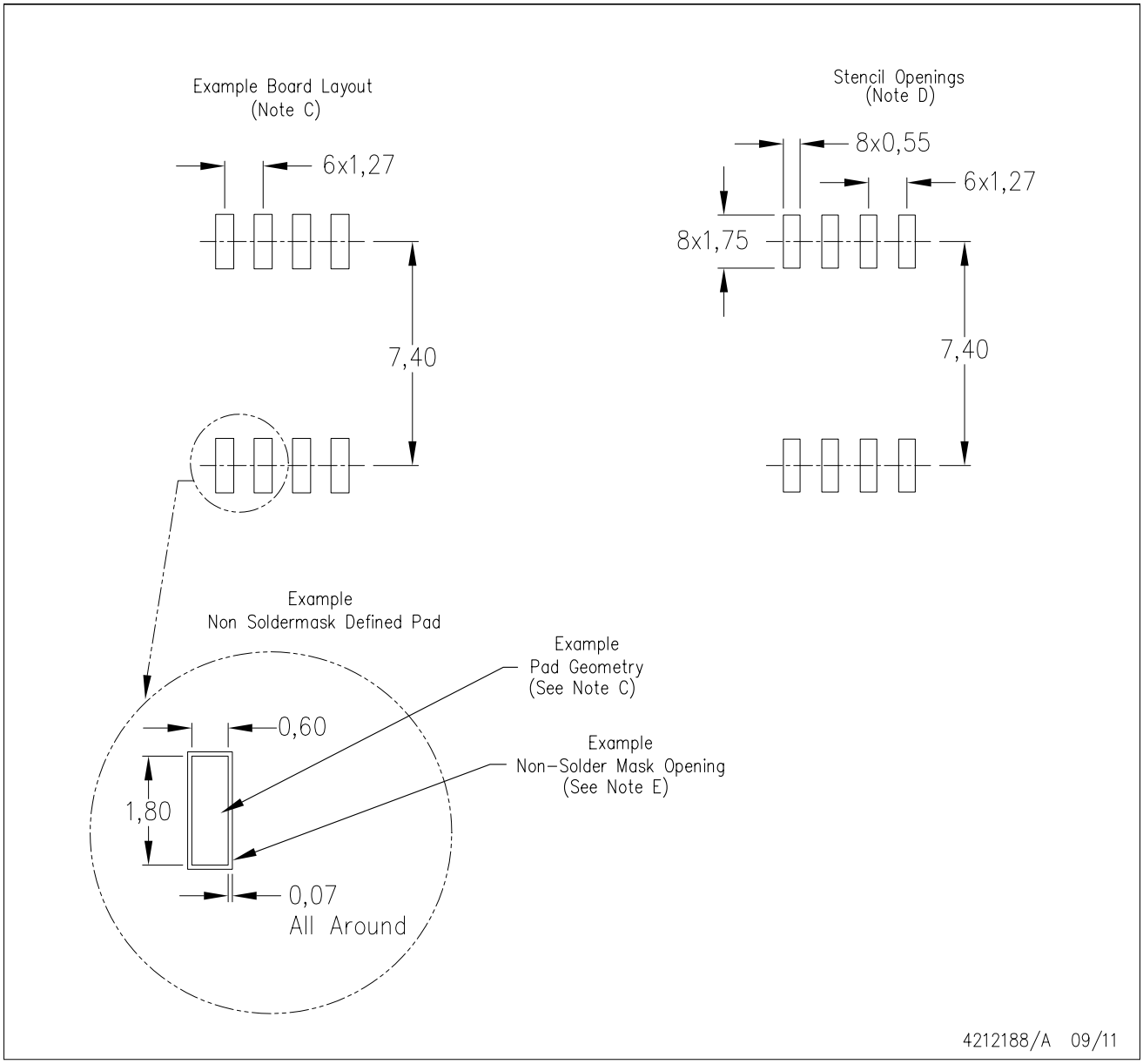
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

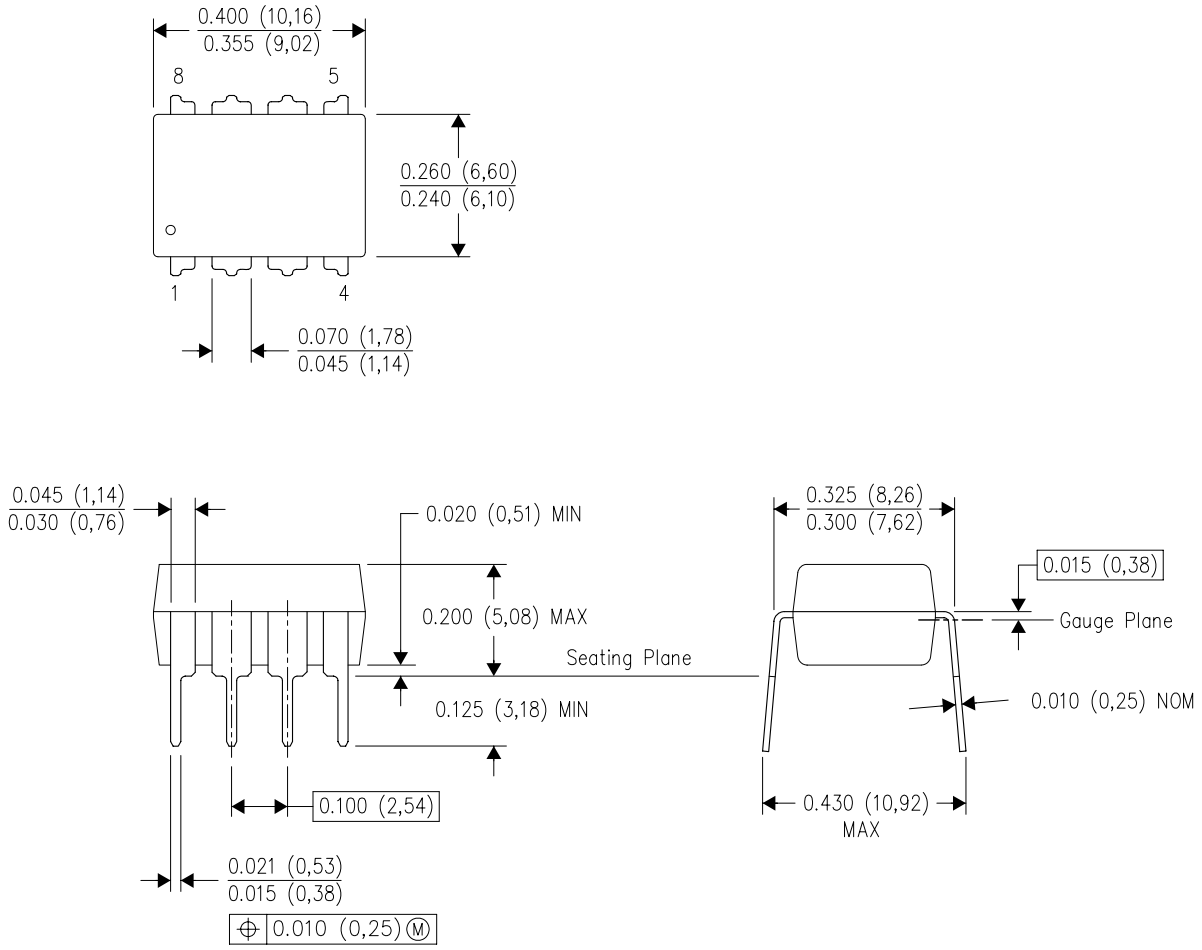
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



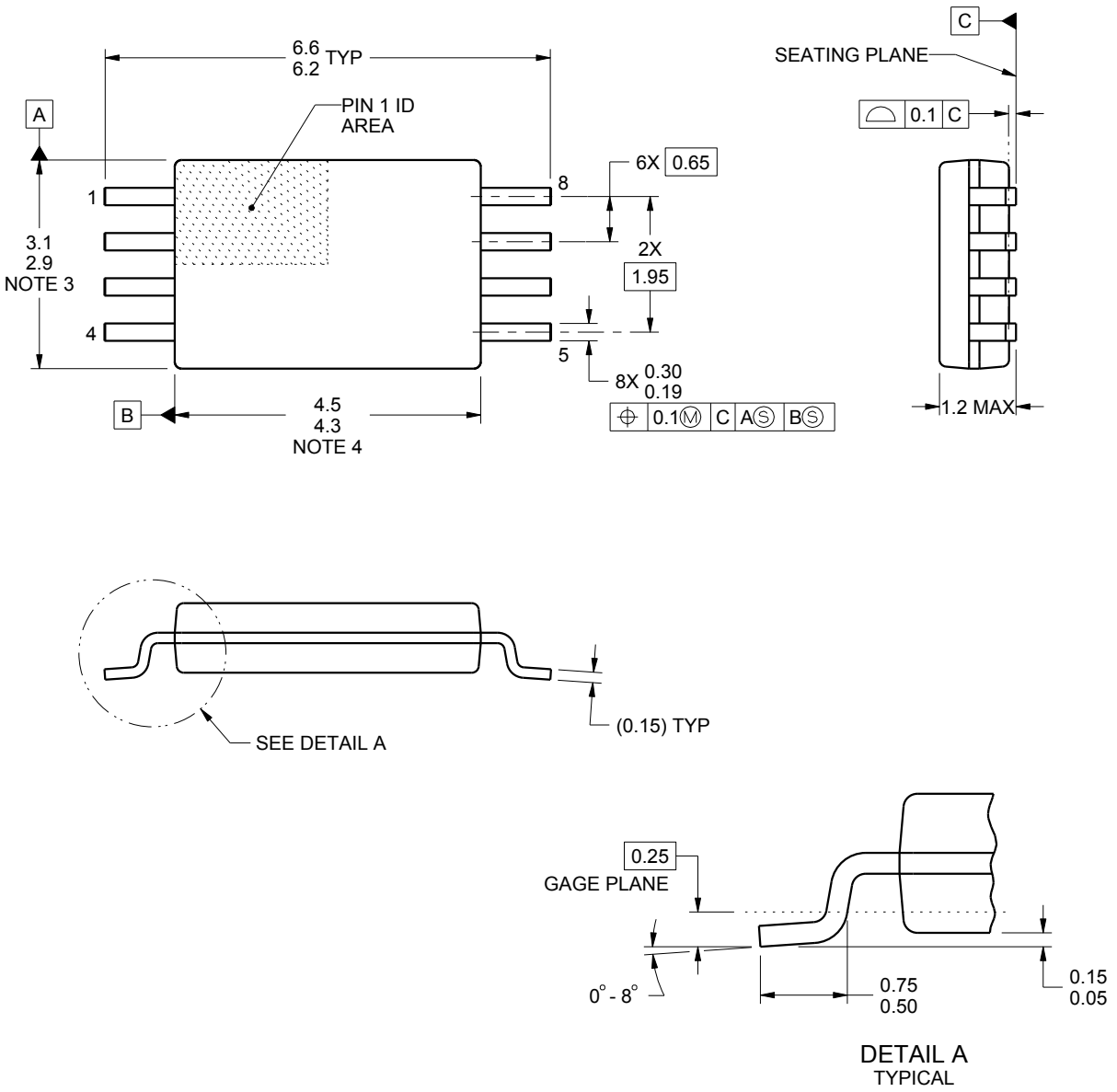
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

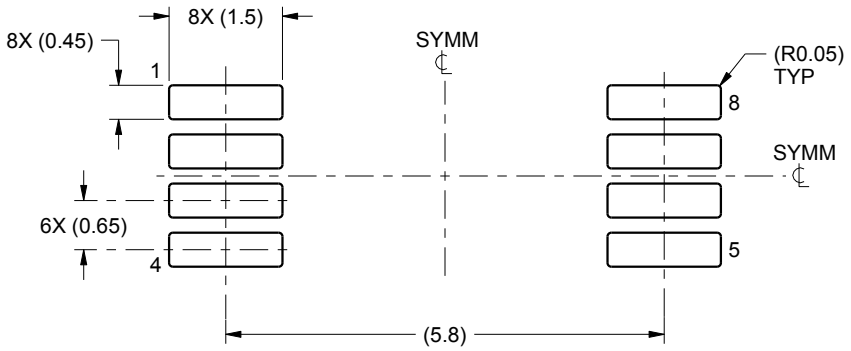
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

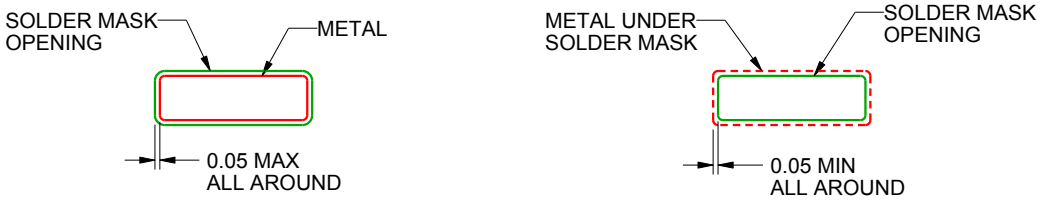


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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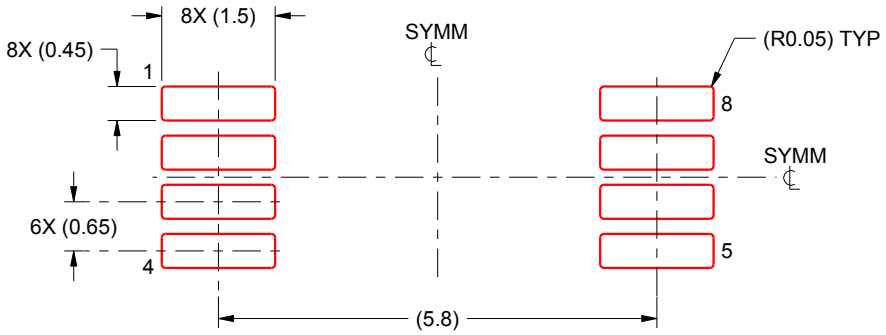
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025