

Precision Dual Operational, Low Offset Voltage, Low Power Op Amp

1 Features

- Trimmed offset voltage: $\pm 300\mu\text{V}$ max at 25°C , $V_{\text{DD}} = 5\text{V}$
- Low offset voltage drift: $\pm 0.6\mu\text{V}/^\circ\text{C}$
- Low noise: typically $32\text{nV}/\sqrt{\text{Hz}}$ at $f = 1\text{kHz}$
- Wide range of supply voltages over specified temperature ranges:
 - 0°C to 70°C : 3V to 16V
 - -40°C to 85°C : 4V to 16V
 - -55°C to 125°C : 4V to 16V
- Low Quiescent Current: typically $120\mu\text{A}$ at 25°C , $V_{\text{DD}} = 5\text{V}$
- Output voltage range includes negative rail
- High input impedance: $6\text{T}\Omega$ typ
- ESD-protection circuitry
- Designed-in latch-up immunity

2 Applications

- [Multiplexed data-acquisition systems](#)
- [Test and measurement equipment](#)
- [Motor drive: power stage and control modules](#)
- [Power delivery: UPS, server, and merchant network power](#)
- [ADC driver and reference buffer amplifier](#)
- [Programmable logic controllers](#)
- [Analog input and output modules](#)
- [High-side and low-side current sensing](#)
- [High precision comparator](#)

3 Description

The TLC27M2 and TLC27M7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose bipolar devices.

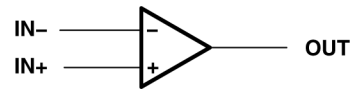
The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices designed for industrial applications.

General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27M2 and TLC27M7. The devices also exhibit low voltage single-supply operation, making them designed for remote and inaccessible battery-powered applications.

Device Information

PART NUMBER ⁽¹⁾	PACKAGE	PACKAGE SIZE ⁽²⁾
TLC27M2	PDIP (8)	9.81mm × 9.43mm
	SOIC (8)	4.9mm × 6mm
	SOP (8)	6.2mm × 7.8mm
	TSSOP (8)	3mm × 6.4mm
TLC27M7	PDIP (8)	9.81mm × 9.43mm
	SOIC (8)	4.9mm × 6mm
	SOP (8)	6.2mm × 7.8mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Symbol (Each Amplifier)



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4 Device Comparison

Table 4-1. Device Information ⁽¹⁾

T _A	V _{IOmax} max at 25°C	PACKAGE		
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)
0°C to 70°C	500mV	TLC27M7CD	TLC27M7CP	
	2mV	TLC27M2BCD	TLC27M2BCP	
	5mV	TLC27M2ACD	TLC27M2ACP	
	10mV	TLC27M2CD	TLC27M2CP	TLC27M2CPW
-40°C to 85°C	500mV	TLC27M7ID	TLC27M7IP	
	2mV	TLC27M2BID	TLC27M2BIP	
	5mV	TLC27M2AID	TLC27M2AIP	
	10mV	TLC27M2ID	TLC27M2IP	TLC27M2IPW
-55°C to 125°C	10mV	TLC27M2MD		

- (1) The D and PW package are available taped and reeled. Add R suffix to the device type (for example, TLC27M7CDR). For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

5 Pin Configuration and Functions

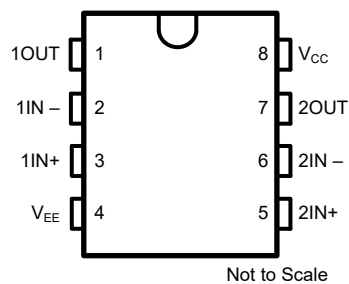


Figure 5-1. TLC27Mx D, P, or PW package (Top View)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{DD}	Supply voltage ⁽²⁾		18	V	
V _{ID}	Differential input voltage ⁽³⁾		±V _{DD}		
V _I	Input voltage range	-0.3	V _{DD}	V	
I _I	Input current		±5	mA	
I _O	Output short circuit		Continuous		
	Duration of short-circuit current at (or below) 25°C ⁽⁴⁾		Unlimited		
T _A	Operating free-air temperature	C suffix	0	70	°C
		I suffix	-40	85	
		M suffix	-55	125	
	Storage temperature range	-65	150		
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	D or P package	260	°C	
	Lead temperature 1.6mm (1/16 inch) from case for 60 seconds	JG package	300	°C	

- (1) Stresses beyond those listed under “absolute maximum ratings” can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) The output can be shorted to either supply. Temperature and/or supply voltages must be limited to make sure that the maximum dissipation rating is not exceeded (see [Section 8.1](#)).

6.2 Dissipation Rating Table

THERMAL METRIC ⁽¹⁾		TLC27Mxx		UNIT
		D, P (SOIC)	PW (TSSOP)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	138.7	188.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	78.7	77.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	82.2	119.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	27.8	14.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	81.4	117.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note, [SPRA953](#).

6.3 Recommended Operating Conditions

			C SUFFIX		I SUFFIX		M SUFFIX		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{DD}	Supply voltage		3	16	4	16	4	16	V
V _{IC}	Common-mode input voltage	V _{DD} = 5 V	-0.2	3.5	-0.2	3.5	0	3.5	V
		V _{DD} = 10 V	-0.2	8.5	-0.2	8.5	0	8.5	
T _A	Operating free-air temperature		0	70	-40	85	-55	125	°C

6.4 Electrical Characteristics

at specified free-air temperature, $V_{DD} = 5V$, $V_{CM} = 2.5V$, $R_L = 10k\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A ⁽¹⁾	TLC27M2C, TLC27M2AC, TLC27M2BC, TLC27M7C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M2C		25°C	±0.3	10	mV	
				Full range		12		
		TLC27M2AC		25°C	±0.3	5		
				Full range		6.5		
		TLC27M2BC		25°C	±300	2000	µV	
				Full range		3000		
TLC27M7C		25°C	±300	1500				
		Full range		1750				
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C	±0.6		µV/°C	
I_{IO}	Input offset current ⁽²⁾			25°C	±5	60	pA	
				70°C	7	300		
I_{IB}	Input bias current ⁽²⁾			25°C	±10	60	pA	
				70°C	40	600		
V_{CM}	Common-mode input voltage range ⁽³⁾			25°C	-0.2 to 5.2		V	
				Full range		-0.2 to 3.5	V	
V_{OH}	High-level output voltage	$V_{ID} = 100mV$		25°C	3.2	4.95	V	
				0°C	3	4.95		
				70°C	3	4.95		
V_{OL}	Low-level output voltage	$V_{ID} = -100mV$	$I_{OL} = 0$	25°C	0	50	mV	
				0°C	0	50		
				70°C	0	50		
A_{VD}	Large-signal differential voltage amplification	$V_O = 0.25V$ to 2V		25°C	25	1000	V/mV	
				0°C	15			
				70°C	15			
CMRR	Common-mode rejection ratio	$V_{CM} = -0.1V < V_{CM} < 2V$		25°C	65	80	dB	
				0°C	60			
				70°C	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5V$ to 10V	$V_O = 1.4V$	25°C	70	140	dB	
				0°C	60	120		
				70°C	60	120		
I_Q	Supply current (two amplifiers)	$I_O = 0A$		25°C	120	150	µA	
				0°C		160		
				70°C		160		

(1) Full range is 0°C to 70°C.

- (2) The typical values of input bias current and input offset current below 5pA is determined mathematically.
(3) This range also applies to each input individually.

6.5 Electrical Characteristics

at specified free-air temperature, $V_{DD} = 10V$, $V_{CM} = 5V$, $R_L = 10k\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A ⁽¹⁾	TLC27M2C, TLC27M2AC, TLC27M2BC, TLC27M7C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M2C		25°C	±0.3	10	mV	
				Full range		12		
		TLC27M2AC		25°C	±0.3	5		
				Full range		6.5		
		TLC27M2BC		25°C	±300	2000	µV	
				Full range		3000		
		TLC27M7C		25°C	±300	1500		
				Full range		1900		
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C	±0.75		µV/°C	
I_{IO}	Input offset current ⁽²⁾			25°C	±5	60	pA	
				70°C	7	300		
I_{IB}	Input bias current ⁽²⁾			25°C	±10	60	pA	
				70°C	50	600		
V_{CM}	Common-mode input voltage range ⁽³⁾			25°C	-0.2 to 9	-0.2 to 9.2	V	
				Full range		-0.2 to 8.5	V	
V_{OH}	High-level output voltage	$V_{ID} = 100mV$		25°C	8	9.95	V	
				0°C	7.8			
				70°C	7.8			
V_{OL}	Low-level output voltage	$V_{ID} = -100mV$	$I_{OL} = 0$	25°C	0	50	mV	
				0°C	0	50		
				70°C	0	50		
A_{VD}	Large-signal differential voltage amplification	$V_O = 1V$ to 6V		25°C	25	1000	V/mV	
				0°C	15			
				70°C	15			
CMRR	Common-mode rejection ratio	$V_{CM} = V_{CMmin}$		25°C	65	80	dB	
				0°C	60			
				70°C	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5V$ to 10V	$V_O = 1.4V$	25°C	70	140	dB	
				0°C	60	120		
				70°C	60	120		

6.5 Electrical Characteristics (continued)

at specified free-air temperature, $V_{DD} = 10V$, $V_{CM} = 5V$, $R_L = 10k\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC27M2C, TLC27M2AC, TLC27M2BC, TLC27M7C			UNIT
					MIN	TYP	MAX	
I_Q	Supply current (two amplifiers)	$V_O = 5V$, No load	$V_{IC} = 5V$	25°C	120	150	μA	
				0°C		160		
				70°C		160		

(1) Full range is 0°C to 70°C.

(2) The typical values of input bias current and input offset current below 5pA is determined mathematically.

(3) This range also applies to each input individually.

6.6 Electrical Characteristics

at specified free-air temperature, $V_{DD} = 5V$, $V_{CM} = 2.5V$, $R_L = 10k\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC27M2I, TLC27M2AI, TLC27M2BI, TLC27M7I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M2I		25°C	± 0.3	10	mV	
				Full range		13		
		TLC27M2AI		25°C	± 0.3	5	mV	
				Full range		7		
		TLC27M2BI		25°C	± 300	2000	μV	
				Full range		3500		
TLC27M7I		25°C	± 300	1500	μV			
		Full range		1750				
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C	± 0.6		$\mu V/^\circ C$	
I_{IO}	Input offset current ⁽²⁾			25°C	± 5	60	pA	
				70°C	200	1000		
I_{IB}	Input bias current ⁽²⁾			25°C	± 10	60	pA	
				70°C	40	2000		
V_{CM}	Common-mode input voltage range ⁽³⁾			25°C	-0.2 to 4	-0.2 to 5.2	V	
				Full range		-0.2 to 3.5	V	
V_{OH}	High-level output voltage		$V_{ID} = 100mV$	25°C	3.2	4.95	V	
				0°C	3	4.95		
				70°C	3	4.95		
V_{OL}	Low-level output voltage		$V_{ID} = -100mV$	$I_{OL} = 0$	25°C	0	50	mV
					0°C	0	50	
					70°C	0	50	

6.6 Electrical Characteristics (continued)

at specified free-air temperature, $V_{DD} = 5V$, $V_{CM} = 2.5V$, $R_L = 10k\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC27M2I, TLC27M2AI, TLC27M2BI, TLC27M7I			UNIT
					MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	$V_O = 0.25V$ to $2V$		25°C	25	1000	V/mV	
				0°C	15			
				70°C	15			
CMRR	Common-mode rejection ratio	$V_{CM} = -0.1V < V_{CM} < 2V$		25°C	65	80	dB	
				0°C	60			
				70°C	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5V$ to $10V$	$V_O = 1.4V$	25°C	70	140	dB	
				0°C	60	120		
				70°C	60	120		
I_Q	Supply current (two amplifiers)	$I_O = 0A$		25°C		120	150	μA
				0°C			160	
				70°C			160	

(1) Full range is $-40^\circ C$ to $85^\circ C$.

6.7 Electrical Characteristics

at specified free-air temperature, $V_{DD} = 10V$, $V_{CM} = 5V$, $R_L = 10k\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC27M2I, TLC27M2AI, TLC27M2BI, TLC27M7I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M2I		25°C	± 0.3	10	mV	
				Full range		12		
		TLC27M2AI		25°C	± 0.3	5		
				Full range		6.5		
		TLC27M2BI		25°C	± 300	2000	μV	
				Full range		3000		
TLC27M7I		25°C	± 300	1500				
		Full range		1900				
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C	± 0.75		$\mu V/^\circ C$	
I_{IO}	Input offset current ⁽²⁾			25°C	± 5	60	pA	
				70°C	7	300		
I_{IB}	Input bias current ⁽²⁾			25°C	± 10	60	pA	
				70°C	50	600		
V_{CM}	Common-mode input voltage range ⁽³⁾			25°C	-0.2 to 9	-0.2 to 9.2	V	
				Full range	-0.2 to 8.5		V	

6.7 Electrical Characteristics (continued)

at specified free-air temperature, $V_{DD} = 10V$, $V_{CM} = 5V$, $R_L = 10k\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC27M2I, TLC27M2AI, TLC27M2BI, TLC27M7I			UNIT
					MIN	TYP	MAX	
V_{OH}	High-level output voltage	$V_{ID} = 100mV$		25°C	8	9.95	V	
				0°C	7.8			
				70°C	7.8			
V_{OL}	Low-level output voltage	$V_{ID} = -100mV$	$I_{OL} = 0$	25°C		0 50	mV	
				0°C		0 50		
				70°C		0 50		
A_{VD}	Large-signal differential voltage amplification	$V_O = 1V$ to 6V		25°C	25	1000	V/mV	
				0°C	15			
				70°C	15			
CMRR	Common-mode rejection ratio	$V_{CM} = V_{CMmin}$		25°C	65	80	dB	
				0°C	60			
				70°C	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5V$ to 10V	$V_O = 1.4V$	25°C	70	140	dB	
				0°C	60	120		
				70°C	60	120		
I_Q	Supply current (two amplifiers)	$I_O = 0A$		25°C		120 150	μA	
				0°C		160		
				70°C		160		

(1) Full range is $-40^\circ C$ to $85^\circ C$.

6.8 Electrical Characteristics

at specified free-air temperature, $V_{DD} = 5V$, $V_{CM} = 2.5V$, $R_L = 10k\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC27M2M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M2M	$V_O = 1.4V$, $R_S = 50\Omega$	$V_{IC} = 0$, $R_L = 100k\Omega$	25°C	1.1	10	mV
					Full range		12	
		TLC27M7M	$V_O = 1.4V$, $R_S = 50\Omega$	$V_{IC} = 0$, $R_L = 100k\Omega$	25°C	185	500	
					Full range		3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C	1.7		$\mu V/^\circ C$	
I_{IO}	Input offset current ⁽²⁾	$V_O = 2.5V$	$V_{IC} = 2.5V$	25°C	0.1	60	pA	
				125°C	1.4	15	nA	
I_{IB}	Input bias current ⁽²⁾	$V_O = 2.5V$	$V_{IC} = 2.5V$	25°C	0.6	60	pA	
				125°C	9	35	nA	
V_{ICR}	Common-mode input voltage range ⁽³⁾			25°C	0 to 4	-0.3 to 4.2	V	
				Full range	0 to 3.5		V	

6.8 Electrical Characteristics (continued)

at specified free-air temperature, $V_{DD} = 5V$, $V_{CM} = 2.5V$, $R_L = 10k\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A ⁽¹⁾	TLC27M2M			UNIT
					MIN	TYP	MAX	
V_{OH}	High-level output voltage	$V_{ID} = 100mV$	$R_L = 100k\Omega$	25°C	3.2	3.9	V	
				-55°C	3	3.9		
				125°C	3	4		
V_{OL}	Low-level output voltage	$V_{ID} = -100 mV$	$I_{OL} = 0$	25°C		0	50	mV
				-55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification	$V_O = 0.25V$ to 2V	$R_L = 100k\Omega$	25°C	25	170	V/mV	
				-55°C	15	290		
				125°C	15	120		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		25°C	65	91	dB	
				-55°C	60	89		
				125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5V$ to 10V	$V_O = 1.4V$	25°C	70	93	dB	
				-55°C	60	91		
				125°C	60	94		
I_{DD}	Supply current (two amplifiers)	$V_O = 2.5V$, No load	$V_{IC} = 2.5V$	25°C		210	560	μA
				-55°C		340	880	
				125°C		140	360	

(1) Full range is -55°C to 125°C.

(2) The typical values of input bias current and input offset current below 5pA is determined mathematically.

(3) This range also applies to each input individually.

6.9 Electrical Characteristics

at specified free-air temperature, $V_{DD} = 10V$, $V_{CM} = 5V$, $R_L = 10k\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A ⁽¹⁾	TLC27M2M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M2M	$V_O = 1.4V$, $R_S = 50\Omega$	$V_{IC} = 0$, $R_L = 100k\Omega$	25°C	1.1	10	mV
					Full range		12	
		TLC27M7M	$V_O = 1.4V$, $R_S = 50\Omega$	$V_{IC} = 0$, $R_L = 100k\Omega$	25°C	190	800	
					Full range		4300	
a_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1	$\mu V/^\circ C$	
I_{IO}	Input offset current ⁽²⁾	$V_O = 5V$	$V_{IC} = 5V$	25°C	0.1	60	pA	
				125°C	1.8	15		
I_{IB}	Input bias current ⁽²⁾	$V_O = 5V$	$V_{IC} = 5V$	25°C	0.7	60	pA	
				125°C	10	35		
V_{ICR}	Common-mode input voltage range ⁽³⁾			25°C	0 to 9	-0.3 to 9.2	V	
				Full range	0 to 8.5		V	

6.9 Electrical Characteristics (continued)

at specified free-air temperature, $V_{DD} = 10V$, $V_{CM} = 5V$, $R_L = 10k\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A ⁽¹⁾	TLC27M2M			UNIT
					MIN	TYP	MAX	
V_{OH}	High-level output voltage	$V_{ID} = 100mV$	$R_L = 100k\Omega$	25°C	8	8.7	V	
				-55°C	7.8	8.6		
				125°C	7.8	8.8		
V_{OL}	Low-level output voltage	$V_{ID} = -100 mV$	$I_{OL} = 0$	25°C		0	50	mV
				-55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification	$V_O = 1V$ to 6V	$R_L = 100k\Omega$	25°C	25	275	V/mV	
				-55°C	15	420		
				125°C	15	190		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		25°C	65	94	dB	
				-55°C	60	93		
				125°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5V$ to 10V	$V_O = 1.4V$	25°C	70	93	dB	
				-55°C	60	91		
				125°C	60	94		
I_{DD}	Supply current (two amplifiers)	$V_O = 5V$, No load	$V_{IC} = 5V$	25°C		285	600	μA
				-55°C		490	1000	
				125°C		180	480	

(1) Full range is -55°C to 125°C.

(2) The typical values of input bias current and input offset current below 5pA are determined mathematically.

(3) This range also applies to each input individually.

6.10 Operating Characteristics

at specified free-air temperature, $V_{DD} = 5V$ to 10V, $V_{CM} = V_{DD} / 2$, $R_L = 10k\Omega$

PARAMETER		TEST CONDITIONS		T_A	TLC27M2C, TLC27M2AC, TLC27M2BC, TLC27M7C, TLC27M2I, TLC27M2AI, TLC27M2BI, TLC27M7I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 10k\Omega$ $C_L = 20pF$	$V_{I(PP)} = 100mV$	25°C	0.5			V/ μs
			$V_{I(PP)} = 1V$	25°C	4.5			
V_n	Equivalent input noise voltage	$f = 1kHz$	$R_S = 20\Omega$	25°C	32			nV/ \sqrt{Hz}
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10k\Omega$	$C_L = 20pF$	25°C	40			kHz
B_1	Unity-gain bandwidth	$V_I = 10mV$	$C_L = 20pF$	25°C	1.1			MHz
Φ_m	Phase margin	$V_I = 10mV$, $C_L = 20pF$	$f = B_1$	25°C	60°			

6.11 Operating Characteristics

at specified free-air temperature, $V_{DD} = 5V$

PARAMETER		TEST CONDITIONS		T_A	TLC27M2M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 100k\Omega$ $C_L = 20pF$	$V_{I(PP)} = 1V$	25°C		0.43	V/ μ s	
				-55°C		0.54		
				125°C		0.29		
			$V_{I(PP)} = 2.5V$	25°C		0.40		
				-55°C		0.49		
				125°C		0.28		
V_n	Equivalent input noise voltage	$f = 1kHz$	$R_S = 20\Omega$	25°C		32	nV/ \sqrt{Hz}	
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$ $R_L = 100k\Omega$	$C_L = 20pF$	25°C		55	kHz	
				-55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	$V_I = 10mV$	$C_L = 20pF$	25°C		525	kHz	
				-55°C		850		
				125°C		330		
Φ_m	Phase margin	$V_I = 10mV$, $C_L = 20pF$	$f = B_1$	25°C		40°		
				-55°C		44°		
				125°C		36°		

6.12 Operating Characteristics

at specified free-air temperature, $V_{DD} = 10V$

PARAMETER		TEST CONDITIONS		T_A	TLC27M2M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 100k\Omega$ $C_L = 20pF$	$V_{I(PP)} = 1V$	25°C		0.62	V/ μ s	
				-55°C		0.81		
				125°C		0.38		
			$V_{I(PP)} = 5.5V$	25°C		0.56		
				-55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	$f = 1kHz$	$R_S = 20\Omega$	25°C		32	nV/ \sqrt{Hz}	
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 100k\Omega$	$C_L = 20pF$	25°C		35	kHz	
				-55°C		50		
				125°C		20		
B_1	Unity gain bandwidth	$V_I = 10mV$	$C_L = 20pF$	25°C		635	kHz	
				-55°C		960		
				125°C		440		
Φ_m	Phase margin	$V_I = 10mV$, $C_L = 20pF$	$f = B_1$	25°C		43°		
				-55°C		47°		
				125°C		39°		

6.13 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{DD} = \pm 20\text{V}$, $V_{CM} = V_{DD} / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_{DD} / 2$, and $C_L = 10\text{pF}$ (unless otherwise noted)

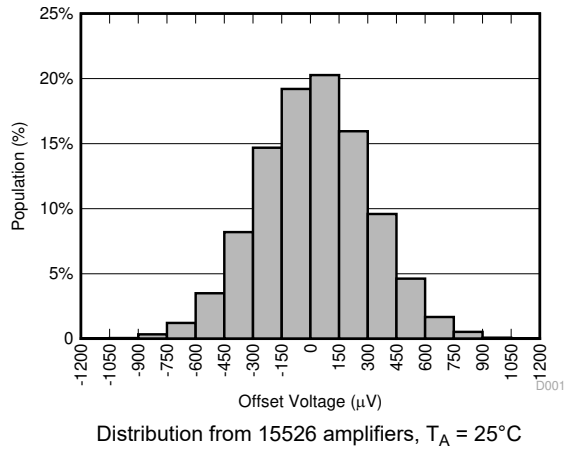


Figure 6-1. Offset Voltage Production Distribution

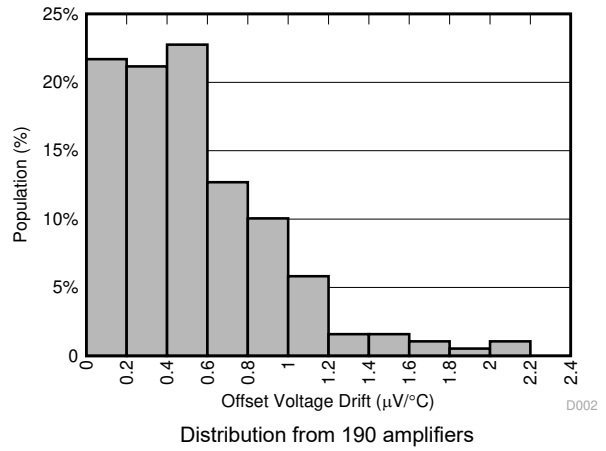


Figure 6-2. Offset Voltage Drift Distribution

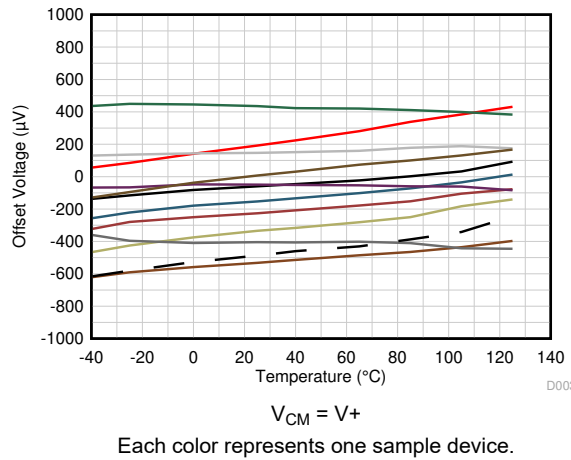


Figure 6-3. Offset Voltage vs Temperature

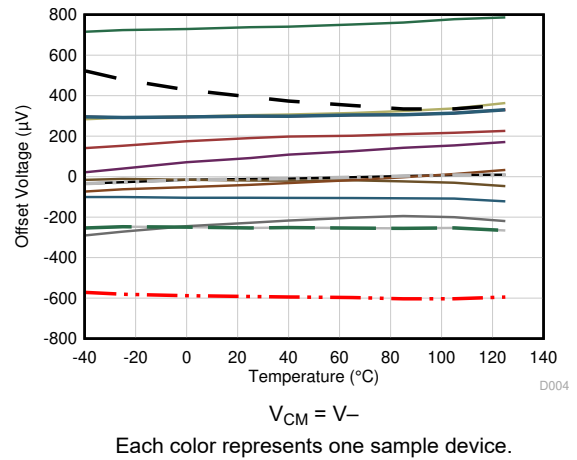


Figure 6-4. Offset Voltage vs Temperature

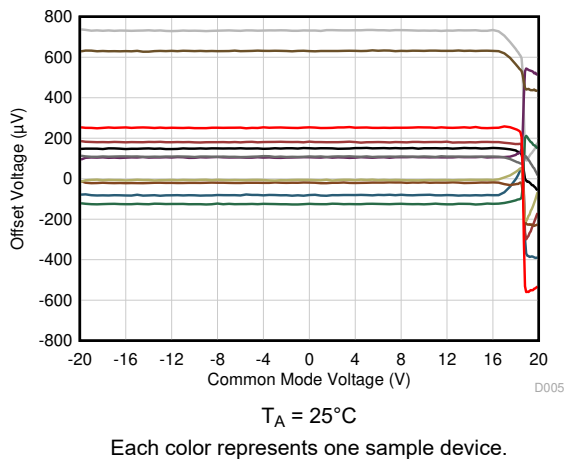


Figure 6-5. Offset Voltage vs Common-Mode Voltage

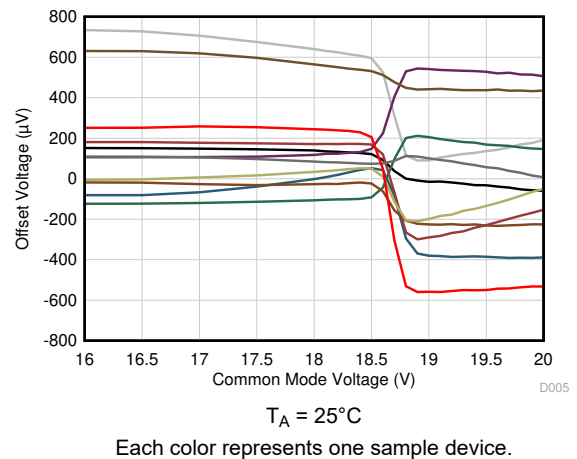


Figure 6-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

6.13 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = \pm 20\text{V}$, $V_{CM} = V_{DD} / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_{DD} / 2$, and $C_L = 10\text{pF}$ (unless otherwise noted)

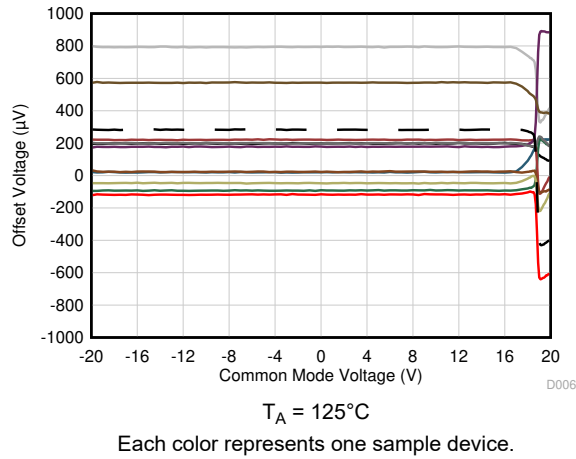


Figure 6-7. Offset Voltage vs Common-Mode Voltage

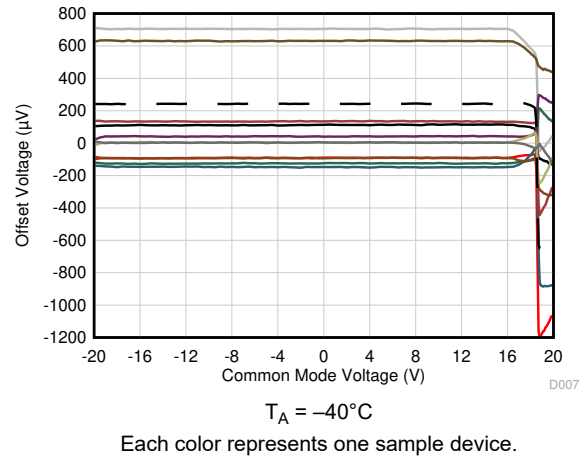


Figure 6-8. Offset Voltage vs Common-Mode Voltage

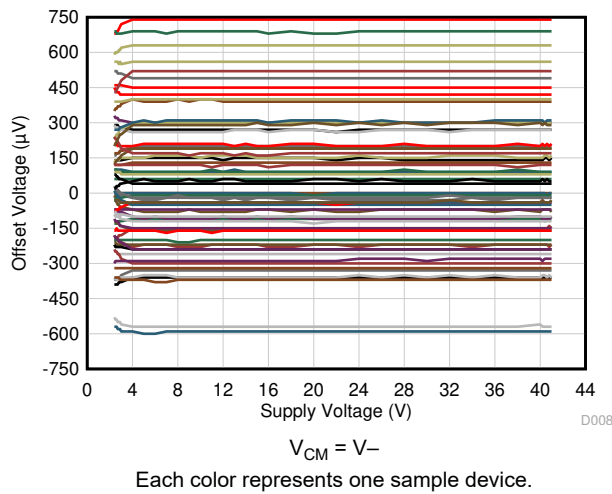


Figure 6-9. Offset Voltage vs Power Supply

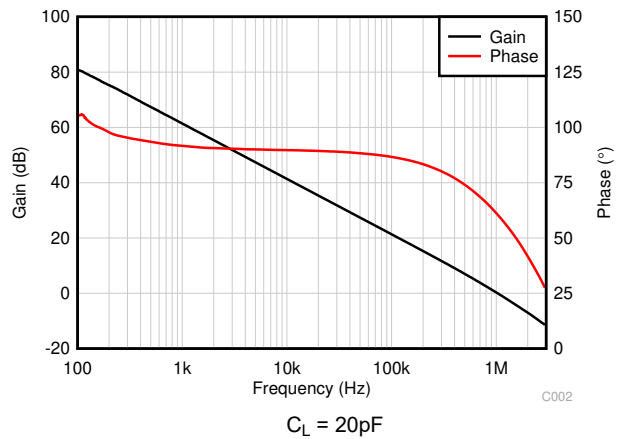


Figure 6-10. Open-Loop Gain and Phase vs Frequency

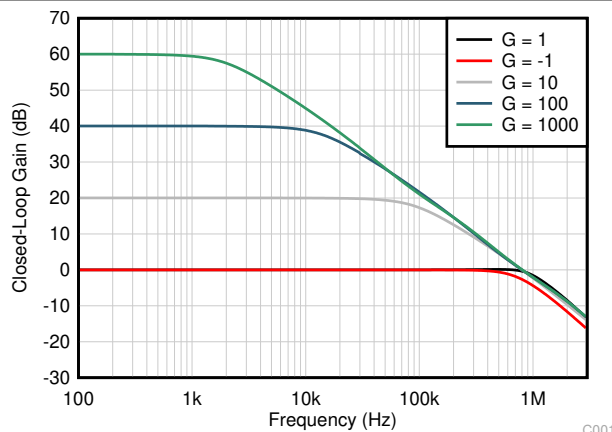


Figure 6-11. Closed-Loop Gain vs Frequency

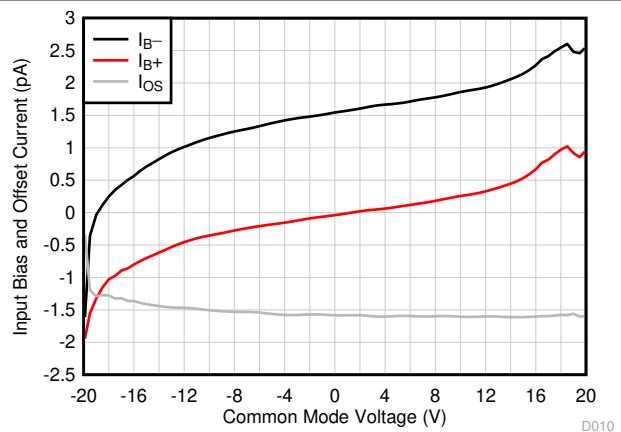


Figure 6-12. Input Bias Current vs Common-Mode Voltage

6.13 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = \pm 20\text{V}$, $V_{CM} = V_{DD} / 2$, $R_{LOAD} = 10\text{k}\Omega$ connected to $V_{DD} / 2$, and $C_L = 10\text{pF}$ (unless otherwise noted)

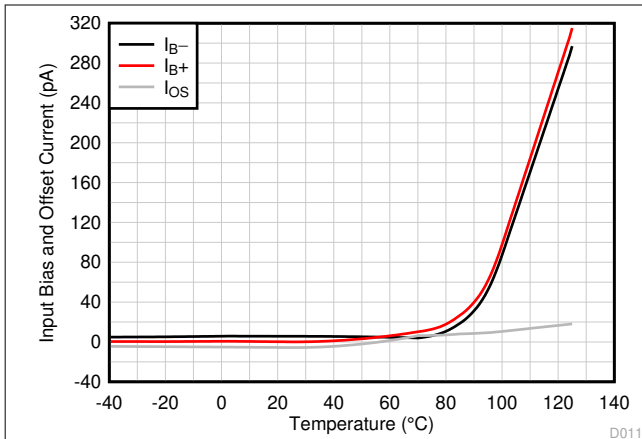


Figure 6-13. Input Bias Current vs Temperature

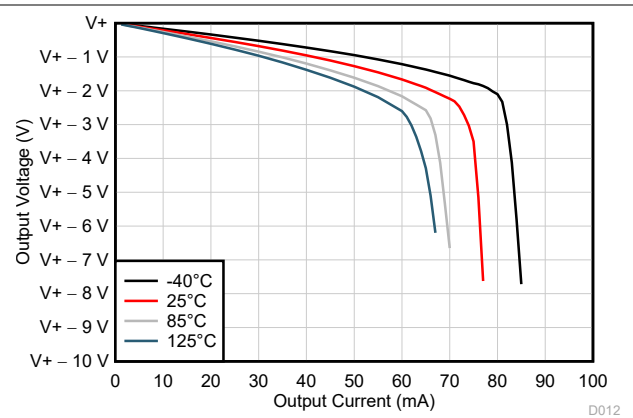


Figure 6-14. Output Voltage Swing vs Output Current (Sourcing)

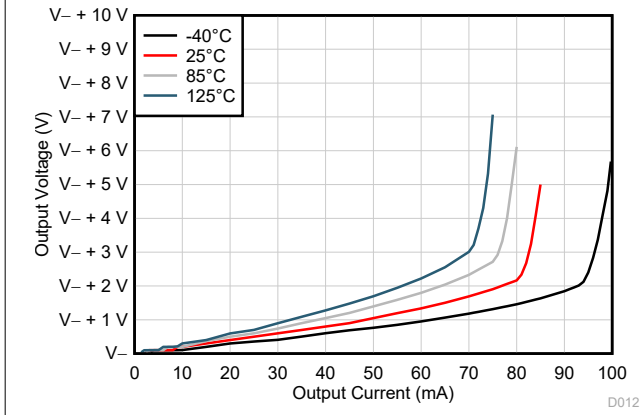


Figure 6-15. Output Voltage Swing vs Output Current (Sinking)

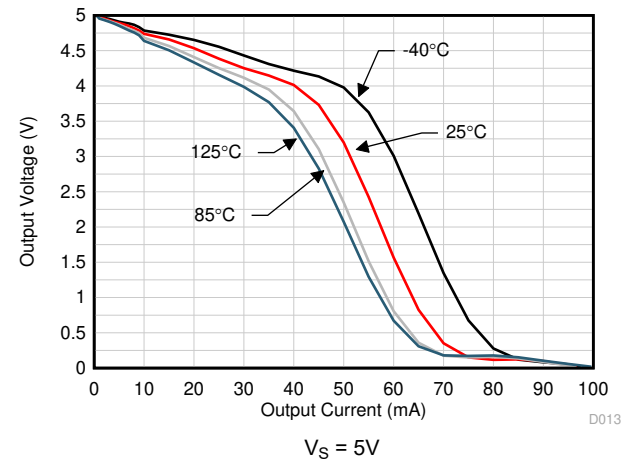


Figure 6-16. Output Voltage Swing vs Output Current (Sourcing)

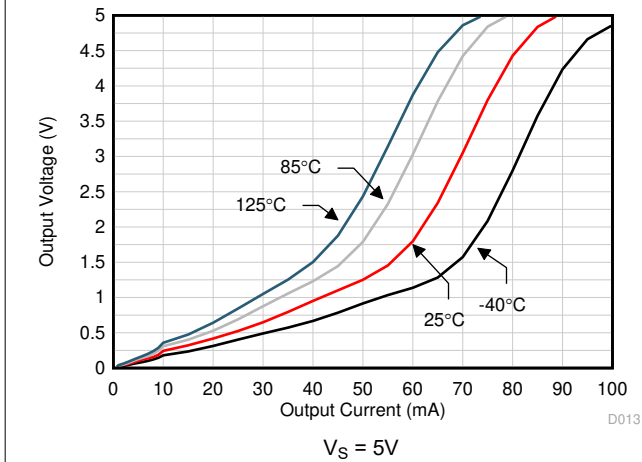


Figure 6-17. Output Voltage Swing vs Output Current (Sinking)

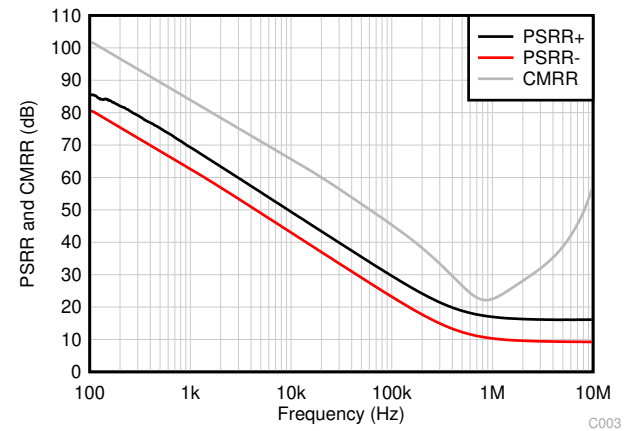


Figure 6-18. CMRR and PSRR vs Frequency

7 Parameter Measurement Information

7.1 Single-Supply versus Split-Supply Test Circuits

Because the TLC27M2 and TLC27M7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

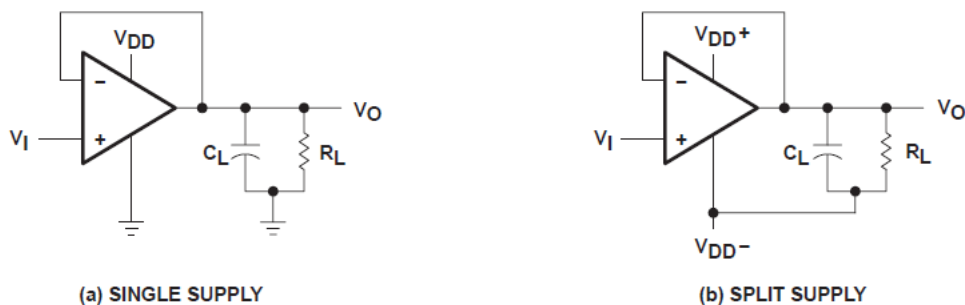


Figure 7-1. Unity-Gain Amplifier

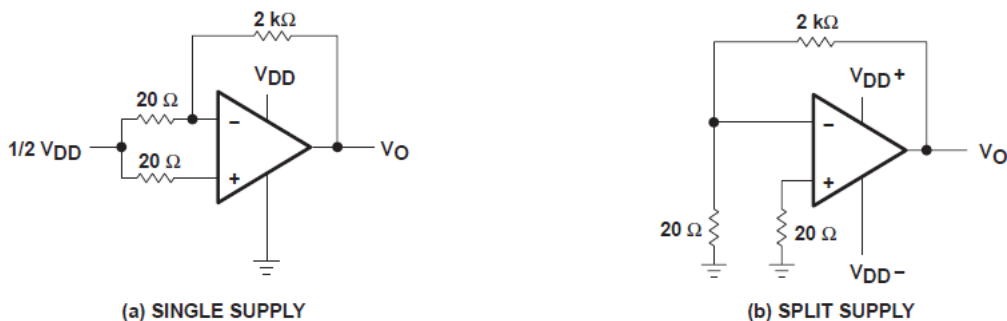


Figure 7-2. Noise-Test Circuit

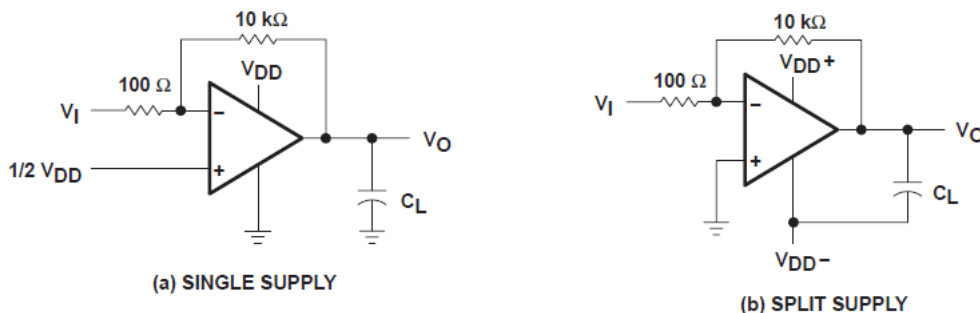


Figure 7-3. Gain-of-100 Inverting Amplifier

7.2 Input Bias Current

Because of the high input impedance of the TLC27M2 and TLC27M7 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see [Figure 7-4](#)). Leakages that can otherwise flow to the inputs are shunted away
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution—many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

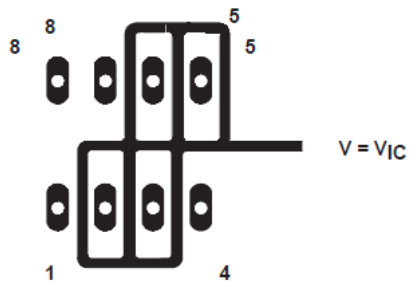


Figure 7-4. Isolation Metal Around Device Inputs (JG and P Packages)

7.3 Low-Level Output Voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions must be observed.

7.4 Input Offset Voltage Temperature Coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage, since the moisture also covers the isolation metal, thereby rendering the method useless. TI suggests that these measurements be performed at temperatures above freezing to minimize error.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Single-Supply Operation

While the TLC27M2 and TLC27M7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground, as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is typically sufficient to establish this reference level (see [Figure 8-1](#)). The low input bias current of the TLC27M2 and TLC27M7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27M2 and TLC27M7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see [Figure 8-2](#)); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications can require RC decoupling.

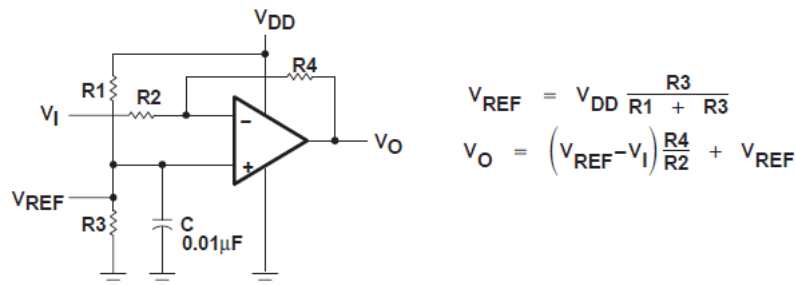


Figure 8-1. Inverting Amplifier With Voltage Reference

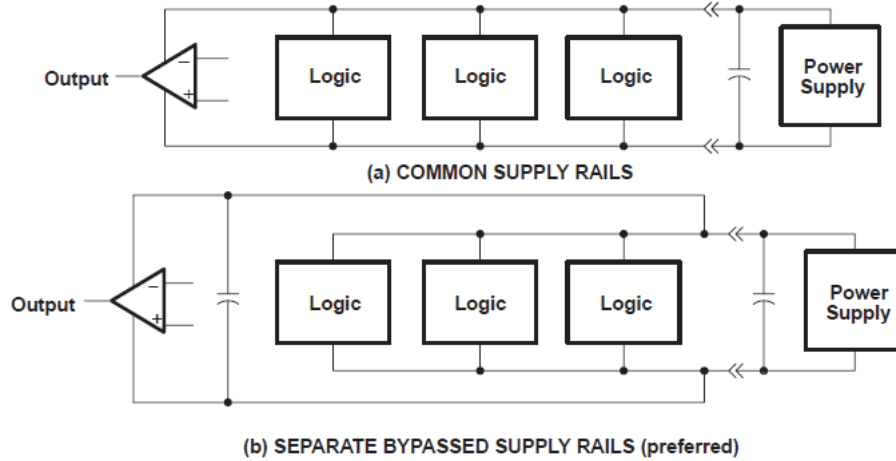


Figure 8-2. Common vs Separate Supply Rails

8.1.2 Input Characteristics

The TLC27M2 and TLC27M7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, can cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1\text{ V}$ at $T_A = 25^\circ\text{C}$ and at $V_{DD} - 1.5\text{ V}$ at all other temperatures.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M2 and TLC27M7 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. Including guard rings around inputs as in the Section 7 figure Figure 7-4 is a good practice. These guards can be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 8-3).

The inputs of any unused amplifiers must be tied to ground to avoid possible oscillation.

8.1.3 Noise Performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M2 and TLC27M7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than $50\text{ k}\Omega$, since bipolar devices exhibit greater noise currents.

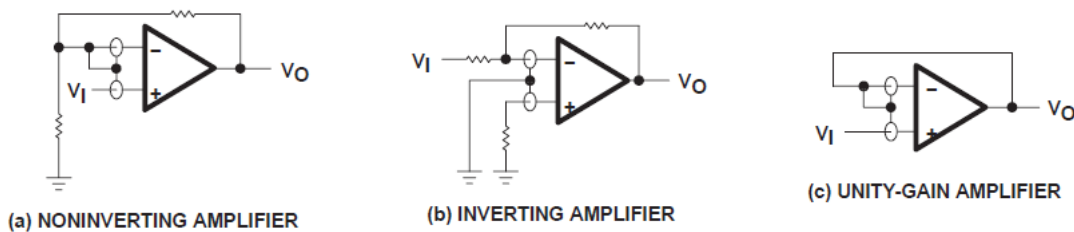


Figure 8-3. Guard-Ring Schemes

8.1.4 Output Characteristics

The output stage of the TLC27M2 and TLC27M7 is designed to sink and source relatively high amounts of current. If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

The TLC2M2 and TLC27M7 devices can drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even

oscillation. In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.

8.1.5 Feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see [Compensation for Input Capacitance](#)). The value of this capacitor is optimized empirically.

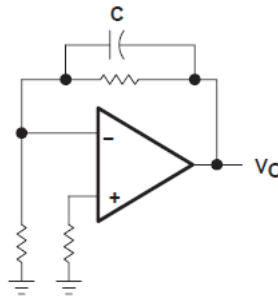


Figure 8-4. Compensation for Input Capacitance

8.1.6 Electrostatic-Discharge Protection

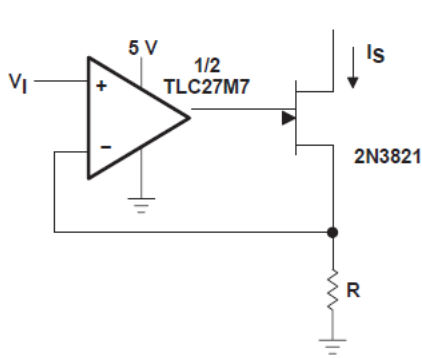
The TLC27M2 and TLC27M7 incorporate an internal electrostatic-discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

8.1.7 Latch-Up

Because CMOS devices are susceptible to latch-up due to the inherent parasitic thyristors, the TLC27M2 and TLC27M7 inputs and outputs are designed to withstand -100mA surge currents without sustaining latch-up; however, techniques can be used to reduce the chance of latch-up whenever possible. Internal protection diodes cannot, by design, be forward biased. Applied input and output voltage cannot exceed the supply voltage by more than 300mV. Care to be exercised when using capacitive coupling on pulse generators. Supply transients can be shunted by the use of decoupling capacitors ($0.1\mu\text{F}$ typical) located across the supply rails as close to the device as possible.

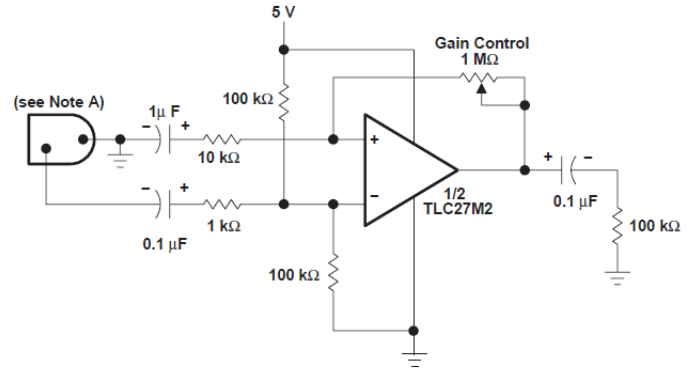
The current path established if latch-up occurs is typically between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and typically results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

8.2 Typical Application



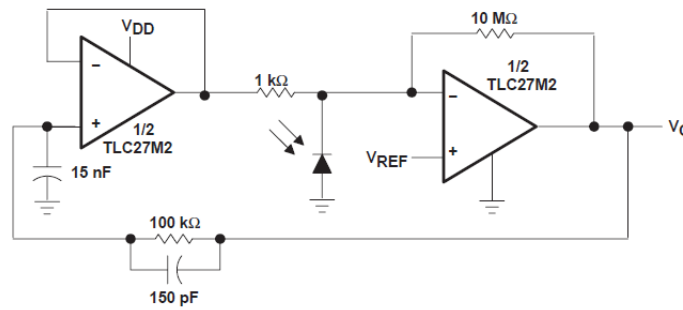
- A. $V_I = 0V$ to $3V$
- B. $I_S = \frac{V_I}{R}$

Figure 8-5. Precision Low-Current Sink



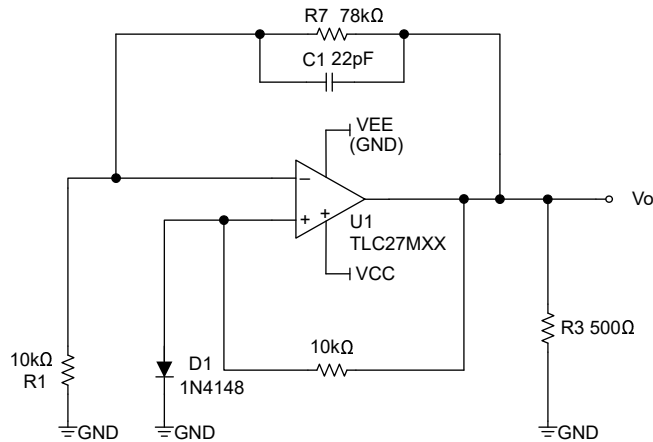
- A. Low to medium impedance dynamic mike.

Figure 8-6. Microphone Preamplifier



- A. $V_{DD} = 4V$ to $15V$
- B. $V_{ref} = 0V$ to $V_{DD} - 2V$

Figure 8-7. Photo-Diode Amplifier With Ambient Light Rejection



- A. $V_{DD} = 8V$ to $16V$
- B. $V_O = 5V, 10mA$

Figure 8-8. 5V Low-Power Voltage Regulator

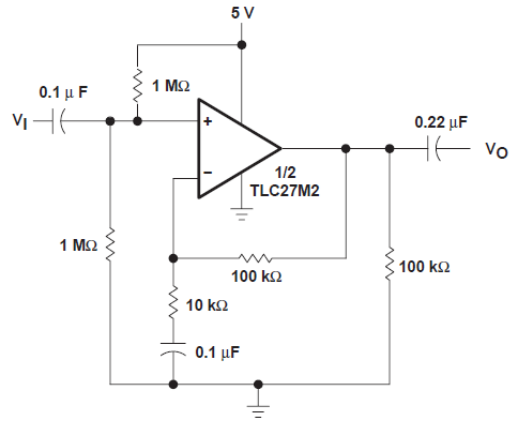


Figure 8-9. Single-Rail AC Amplifiers

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.2 Documentation Support

9.2.1 Related Documentation

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

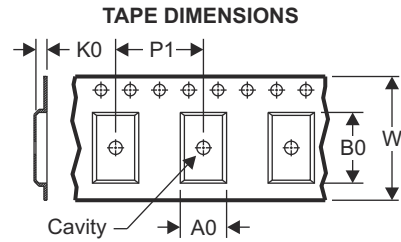
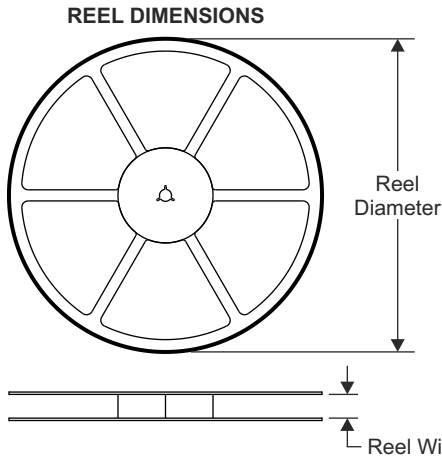
Changes from , to , (from Revision E (August 2008) to Revision F (February 2026))	Page
• Changed Trimmed offset voltage from $\pm 500\mu\text{V}$ to $\pm 300\mu\text{V}$	1
• Changed Low offset voltage drift from $\pm 500\mu\text{V}$ to $\pm 300\mu\text{V}$	1
• Changed Low power from mW to Quiescent Current $120\mu\text{A}$	1
• Changed High Input impedance from 1012Ω	1
• Deleted Common mode input voltage range.....	1
• Deleted Output voltage range includes negative rail.....	1
• Deleted small outline package option.....	1
• Updated Applications.....	1
• Updated Description.....	1
• Updated Device information.....	1
• Deleted Total current into V_{DD}	4
• Deleted Total current out of GND.....	4

• Deleted Continuous total dissipation.....	4
• Deleted Case temperature for 60 seconds.....	4
• Changed Output current from $\pm 30\text{mA}$ to output short circuit continuous.....	4
• Changed Input offset voltage for TLC27M2C from 1.1mV to $\pm 0.3\text{mV}$	5
• Changed Input offset voltage for TLC27M2AC from 0.9mV to $\pm 0.3\text{mV}$	5
• Changed Input offset voltage for TLC27M2BC from 224 μV to $\pm 300\mu\text{V}$	5
• Changed Input offset voltage for TLC27M7C typ from 190 μV to $\pm 300\mu\text{V}$	5
• Changed Input offset voltage for TLC27M7C max from 800 μV to 1500 μV	5
• Deleted Test conditions for V_{IO} , I_{IO} , I_{IB}	5
• Changed Common-mode rejection ratio from 91dB to 80dB, Supply-voltage rejection ratio.....	5
• Changed Supply-voltage rejection ratio from 93dB to 140dB at 25°C and 120dB at 0° and 70°C.....	5
• Changed Supply current from 210 μA to 20 μA	5
• Changed Average temperature coefficient of input voltage from 2.1 $\mu\text{V}/^\circ\text{C}$ to $\pm 0.75\mu\text{V}/^\circ\text{C}$	6
• Changed Input offset current from 0.1pA to $\pm 5\text{pA}$	6
• Changed Input bias current from 0.7pA to $\pm 10\text{pA}$	6
• Changed Common-mode input voltage range from -0.3V to -0.2V.....	6
• Changed High-level output voltage from 8.7V to 9.95V.....	6
• Changed Large-signal differential voltage amplification from 275V/mV to 1000V/mV.....	6
• Deleted $T_A = 0^\circ\text{C}$ and 70°C values	11
• Changed Slew rate from 0.43V/ s to 0.5V/ s at 100mV.....	11
• Changed Slew rate from 0.40V/ s to 4.5V/ s at 1V.....	11
• Changed RL in Slew rate from 100K Ω to 10K Ω	11
• Changed Maximum output-swing bandwidth from 55kHz to 40kHz.....	11
• Changed Phase margin from 40° to 60°.....	11
• Merged 5V and 10V operating characteristics tables.....	11
•	13
• Removed <i>Full Power Response</i> and <i>Test Time</i> section.....	17

11 Mechanical, Packaging, and Orderable Information

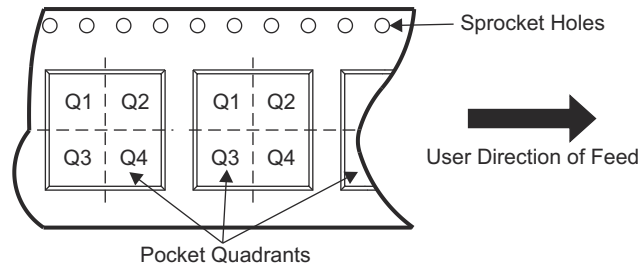
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information



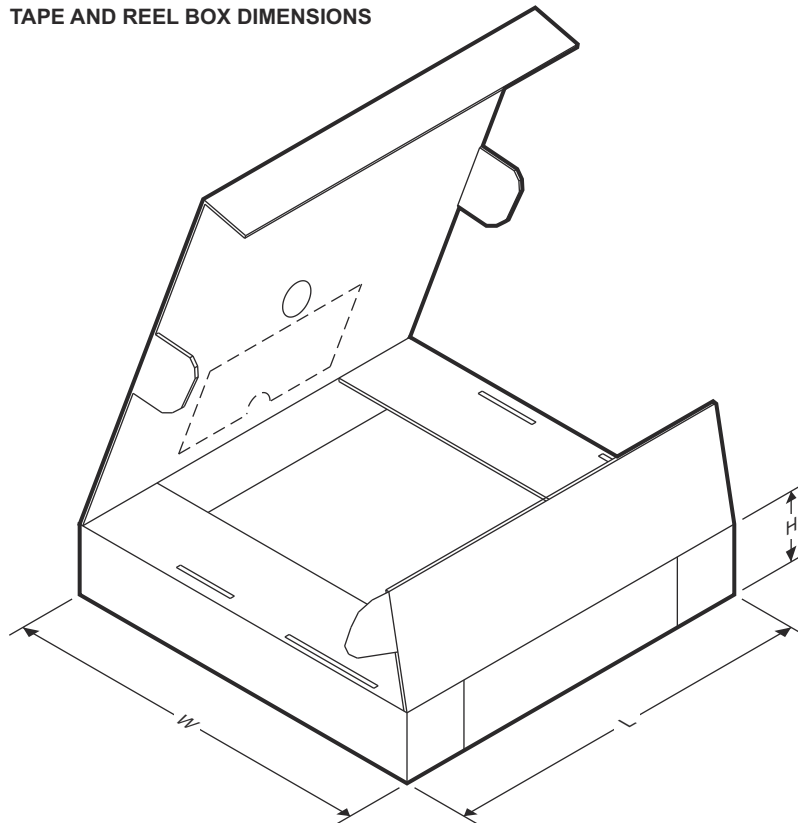
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
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11.2 Mechanical Data

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC27M2ACD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	0 to 70	27M2AC
TLC27M2ACDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27M2AC
TLC27M2ACDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27M2AC
TLC27M2ACP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27M2AC
TLC27M2ACP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27M2AC
TLC27M2ACPE4	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27M2AC
TLC27M2AID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	27M2AI
TLC27M2AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M2AI
TLC27M2AIDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M2AI
TLC27M2AIP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27M2AI
TLC27M2AIP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27M2AI
TLC27M2BCD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	0 to 70	27M2BC
TLC27M2BCDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27M2BC
TLC27M2BCDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27M2BC
TLC27M2BCDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M2BC
TLC27M2BCDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M2BC
TLC27M2BCP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27M2BC
TLC27M2BCP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27M2BC
TLC27M2BID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	27M2BI
TLC27M2BIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M2BI
TLC27M2BIDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M2BI
TLC27M2BIP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27M2BI
TLC27M2BIP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27M2BI
TLC27M2CD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	0 to 70	27M2C
TLC27M2CDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27M2C
TLC27M2CDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27M2C
TLC27M2CDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	27M2C
TLC27M2CDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	27M2C
TLC27M2CP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27M2CP

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC27M2CP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27M2CP
TLC27M2CPS	Active	Production	SO (PS) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27M2
TLC27M2CPS.A	Active	Production	SO (PS) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27M2
TLC27M2CPSR	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27M2
TLC27M2CPSR.A	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27M2
TLC27M2CPW	Obsolete	Production	TSSOP (PW) 8	-	-	Call TI	Call TI	0 to 70	P27M2
TLC27M2CPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27M2
TLC27M2CPWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27M2
TLC27M2ID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	27M2I
TLC27M2IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M2I
TLC27M2IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M2I
TLC27M2IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27M2IP
TLC27M2IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27M2IP
TLC27M2IPW	Obsolete	Production	TSSOP (PW) 8	-	-	Call TI	Call TI	-40 to 85	P27M2I
TLC27M2IPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	P27M2I
TLC27M2IPWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	P27M2I
TLC27M2IPWRG4	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	-	Call TI	Call TI	0 to 70	
TLC27M2MD	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	27M2M
TLC27M2MD.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	27M2M
TLC27M2MDG4	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	27M2M
TLC27M2MDG4.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	27M2M
TLC27M7CD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	0 to 70	27M7C
TLC27M7CDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27M7C
TLC27M7CDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27M7C
TLC27M7CP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27M7CP
TLC27M7CP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27M7CP
TLC27M7CPS	Active	Production	SO (PS) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27M7
TLC27M7CPS.A	Active	Production	SO (PS) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27M7
TLC27M7CPSR	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27M7
TLC27M7CPSR.A	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27M7
TLC27M7ID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	27M7I

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC27M7IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M7I
TLC27M7IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M7I
TLC27M7IDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M7I
TLC27M7IDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27M7I
TLC27M7IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27M7IP
TLC27M7IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC27M7IP

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

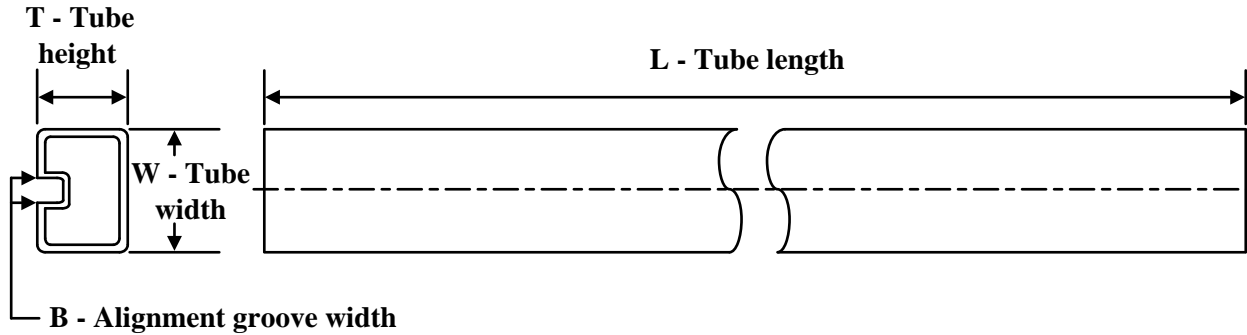

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC27M2ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27M2AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27M2BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27M2BCDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27M2BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27M2CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27M2CDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27M2CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TLC27M2CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC27M2IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27M2IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC27M7CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27M7CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TLC27M7IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27M7IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC27M2ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC27M2AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27M2BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27M2BCDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TLC27M2BIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27M2CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27M2CDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TLC27M2CPSR	SO	PS	8	2000	353.0	353.0	32.0
TLC27M2CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC27M2IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27M2IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC27M7CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC27M7CPSR	SO	PS	8	2000	353.0	353.0	32.0
TLC27M7IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC27M7IDRG4	SOIC	D	8	2500	340.5	338.1	20.6

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC27M2ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M2ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M2ACPE4	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M2AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M2AIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M2BCP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M2BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M2BIP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M2BIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M2CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M2CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M2CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC27M2CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC27M2IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M2IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M2MD	D	SOIC	8	75	505.46	6.76	3810	4
TLC27M2MD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC27M2MDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLC27M2MDG4.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC27M7CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M7CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M7CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC27M7CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC27M7IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27M7IP.A	P	PDIP	8	50	506	13.97	11230	4.32



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



PW0008A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

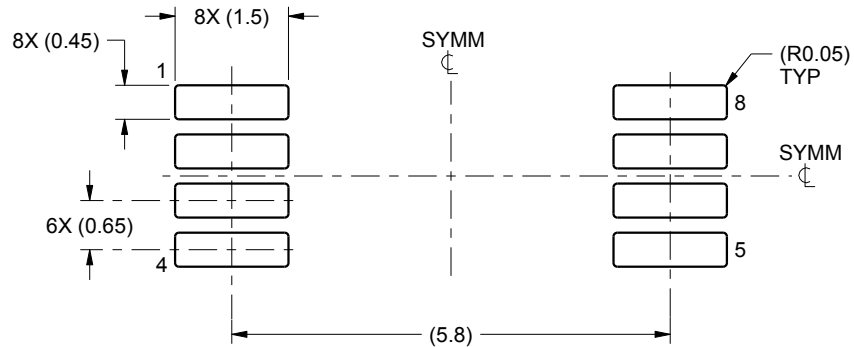
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

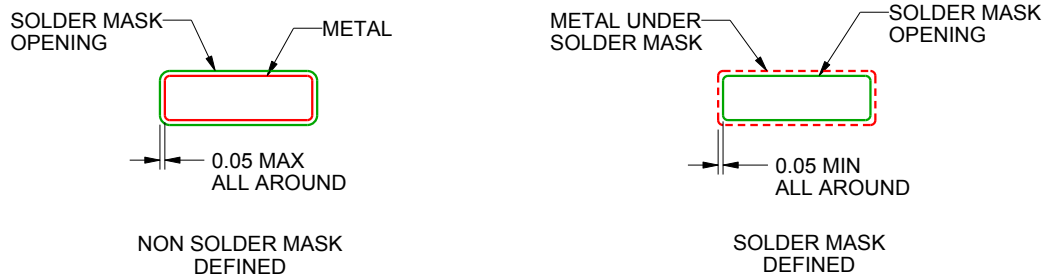
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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