10-BIT DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- **10-Bit CMOS Voltage Output DAC in an 8-Terminal Package**
- **5V Single Supply Operation**
- **3-Wire Serial Interface**
- **High-Impedance Reference Inputs**
- **Voltage Output Range: 2 Times the Reference Input Voltage**
- **Internal Power-On Reset**
- **Low Power Consumption: 1.75mW Max**
- **Update Rate of 1.21MHz**
- **Settling Time to 0.5LSB: 12.5μs Typ**
- **Monotonic Over Temperature**
- **Pin-Compatible With the Maxim MAX515**

APPLICATIONS

- **Battery-Powered Test Instruments**
- **Digital Offset and Gain Adjustment**
- **Battery Operated/Remote Industrial Controls**
- **Machine and Motion Control Devices**
- **Cellular Telephones**

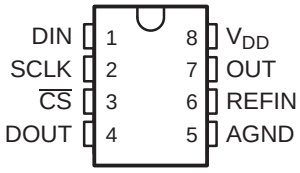
DESCRIPTION

The TLC5615 is a 10-bit voltage output digital-to-analog converter (DAC) with a buffered reference input (high impedance). The DAC has an output voltage range that is two times the reference voltage, and the DAC is monotonic. The device is simple to use, running from a single supply of 5V. A power-on-reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLC5615 is over a three-wire serial bus that is CMOS compatible and easily interfaced to industry standard microprocessor and microcontroller devices. The device receives a 16-bit data word to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™, and Microwire™ standards.

The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications. The TLC5615C is characterized for operation from 0°C to +70°C. The TLC5615I is characterized for operation from –40°C to +85°C.

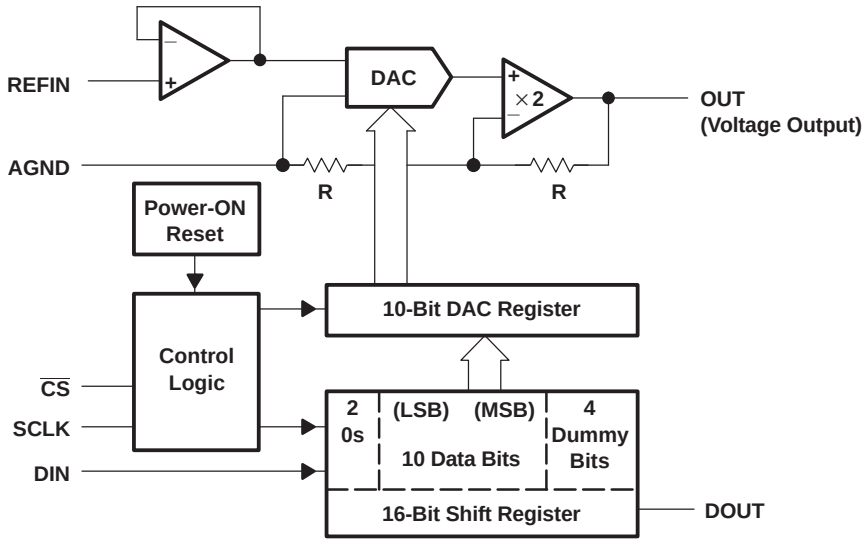
D, P, OR DGK PACKAGE
(TOP VIEW)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DIN	1	I	Serial data input
SCLK	2	I	Serial clock input
$\overline{CS}$	3	I	Chip select, active low
DOUT	4	O	Serial data output for daisy chaining
AGND	5		Analog ground
REFIN	6	I	Reference input
OUT	7	O	DAC analog voltage output
V_{DD}	8		Positive power supply

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Supply voltage (V_{DD} to AGND)		7V
Digital input voltage range to AGND		–0.3V to V_{DD} + 0.3V
Reference input voltage range to AGND		–0.3V to V_{DD} + 0.3V
Output voltage at OUT from external source		V_{DD} + 0.3V
Continuous current at any terminal		±20mA
Operating free-air temperature range, T_A	TLC5615C	0°C to +70°C
	TLC5615I	–40°C to +85°C
Storage temperature range, T_{stg}		–65°C to +150°C
Lead temperature 1,6mm (1/16 inch) from case for 10 seconds		+260°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	V
High-level digital input voltage, V_{IH}		2.4			V
Low-level digital input voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} to REFIN terminal		2	2.048	V_{DD}–2	V
Load resistance, R_L		2			kΩ
Operating free-air temperature, T_A	TLC5615C	0		70	°C
	TLC5615I	40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 5V ± 5%, V_{ref} = 2.048V (unless otherwise noted)

STATIC DAC SPECIFICATIONS							
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Resolution				10			bits
	Integral nonlinearity, end point adjusted (INL)		V_{ref} = 2.048V,	See (1)			±1	LSB
	Differential nonlinearity (DNL)		V_{ref} = 2.048V,	See (2)		±0.1	±0.5	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)		V_{ref} = 2.048V,	See (3)			±3	LSB
	Zero-scale-error temperature coefficient		V_{ref} = 2.048V,	See (4)		3		ppm/°C
E_G	Gain error		V_{ref} = 2.048V,	See (5)			±3	LSB
	Gain-error temperature coefficient		V_{ref} = 2.048V,	See (6)		1		ppm/°C
PSRR	Power-supply rejection ratio	Zero scale	See (7)(8)		80			dB
		Gain			80			
	Analog full scale output		R_L = 100kΩ			2V_{ref}(1023/1024)		V

(1) The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors (see text). Tested from code 3 to code 1024.
(2) The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code. Tested from code 3 to code 1024.
(3) Zero-scale error is the deviation from zero-voltage output when the digital input code is zero (see text).
(4) Zero-scale-error temperature coefficient is given by: E_{ZS} TC = [E_{ZS} (T_{max}) – E_{ZS} (T_{min})]/V_{ref} × 10^6/(T_{max}– T_{min}).
(5) Gain error is the deviation from the ideal output (V_{ref} – 1LSB) with an output load of 10kΩ excluding the effects of the zero-scale error.
(6) Gain temperature coefficient is given by: E_G TC = [E_G(T_{max}) – E_G (T_{min})]/V_{ref} × 10^6/(T_{max}– T_{min}).
(7) Zero-scale-error rejection ratio (EZS-RR) is measured by varying the V_{DD} from 4.5V to 5.5V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
(8) Gain-error rejection ratio (EG-RR) is measured by varying the V_{DD} from 4.5V to 5.5V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero-scale change.

VOLTAGE OUTPUT (OUT)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Voltage output range	R_L= 10kΩ		0		V_{DD}–0.4	V
	Output load regulation accuracy	$V_{O(OUT)}$ = 2V,	R_L = 2kΩ			0.5	LSB
I_{OSC}	Output short circuit current	OUT to V_{DD} or AGND			20		mA
$V_{OL(low)}$	Output voltage, low-level	$I_{O(OUT)}$≤ 5mA				0.25	V
$V_{OH(high)}$	Output voltage, high-level	$I_{O(OUT)}$≤– 5mA		4.75			V
REFERENCE INPUT (REFIN)							
V_I	Input voltage			0		V_{DD}–2	V
r_i	Input resistance			10			MΩ
C_i	Input capacitance				5		pF
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$)							
V_{IH}	High-level digital input voltage			2.4			V
V_{IL}	Low-level digital input voltage					0.8	V
I_{IH}	High-level digital input current	$V_I = V_{DD}$				±1	µA
I_{IL}	Low-level digital input current	V_I = 0				±1	µA
C_i	Input capacitance				8		pF
DIGITAL OUTPUT (DOUT)							
V_{OH}	Output voltage, high-level	I_O = –2mA		V_{DD}–1			V
V_{OL}	Output voltage, low-level	I_O = 2mA				0.4	V
POWER SUPPLY							
V_{DD}	Supply voltage			4.5	5	5.5	V
I_{DD}	Power supply current	V_{DD} = 5.5V, No load, All inputs = 0V or V_{DD}	V_{ref} = 0		150	250	µA
		V_{DD}= 5.5V, No load, All inputs = 0V or V_{DD}	V_{ref} = 2.048V		230	350	µA
ANALOG OUTPUT DYNAMIC PERFORMANCE							
	Signal-to-noise + distortion, S/(N+D)	V_{ref} = 1V_{PP} at 1kHz + 2.048Vdc, code = 11 1111 1111 (1)		60			dB

(1) The limiting frequency value at 1V_{PP} is determined by the output-amplifier slew rate.

DIGITAL INPUT TIMING REQUIREMENTS (See Figure 1)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{su(DS)}$	Setup time, DIN before SCLK high	45			ns
$t_{h(DH)}$	Hold time, DIN valid after SCLK high	0			ns
$t_{su(CSS)}$	Setup time, $\overline{CS}$ low to SCLK high	1			ns
$t_{su(CS1)}$	Setup time, $\overline{CS}$ high to SCLK high	50			ns
$t_{h(CSH0)}$	Hold time, SCLK low to $\overline{CS}$ low	1			ns
$t_{h(CSH1)}$	Hold time, SCLK low to $\overline{CS}$ high	0			ns
$t_{w(CS)}$	Pulse duration, minimum chip select pulse width high	20			ns
$t_{w(CL)}$	Pulse duration, SCLK low	25			ns
$t_{w(CH)}$	Pulse duration, SCLK high	25			ns

OUTPUT SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{pd(DOUT)}$	Propagation delay time, DOUT	C_L = 50pF			50	ns

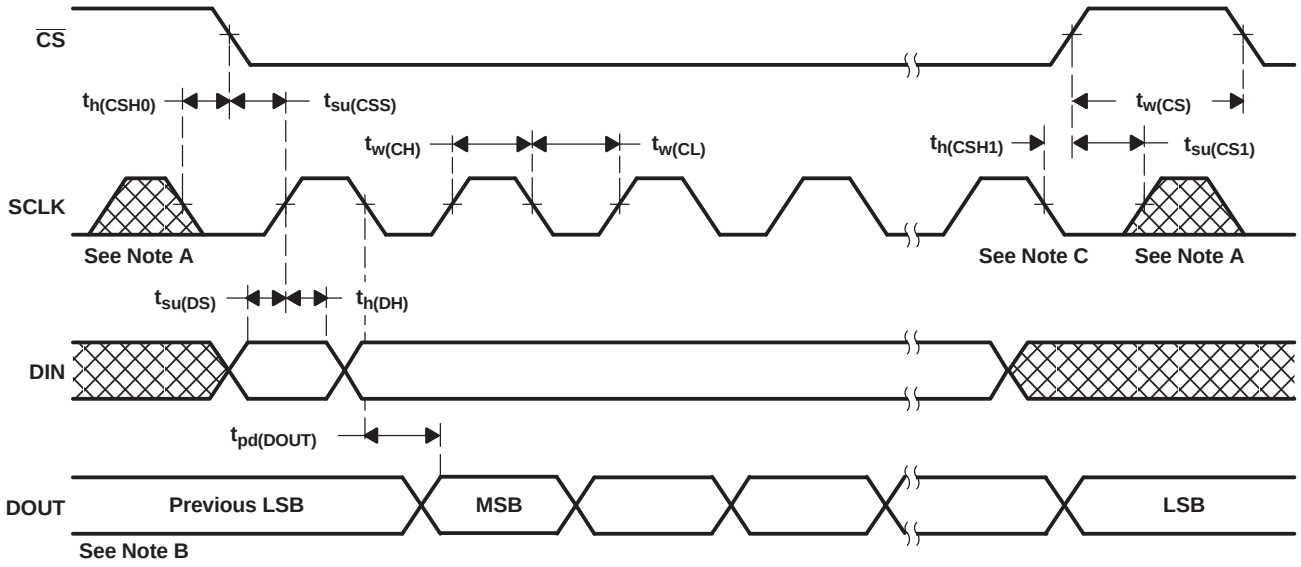
OPERATING CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 5V ±5%, V_{ref} = 2.048V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG OUTPUT DYNAMIC PERFORMANCE							
SR	Output slew rate	C_L = 100pF, T_A= +25°C	R_L = 10kΩ,	0.3	0.5		V/µs
t_s	Output settling time	To 0.5LSB, R_L = 10kΩ,	C_L = 100pF, (1)		12.5		µs
	Glitch energy	DIN = All 0s to all 1s			5		nV-s
REFERENCE INPUT (REFIN)							
	Reference feedthrough	REFIN = $1V_{PP}$ at 1kHz + 2.048Vdc (2)			–80		dB
	Reference input bandwidth (f–3dB)	REFIN = $0.2V_{PP}$ + 2.048Vdc			30		kHz

(1) Settling time is the time for the output signal to remain within ±0.5LSB of the final measured value for a digital input code change of 000 hex to 3FF hex or 3FF hex to 000 hex.
(2) Reference feedthrough is measured at the DAC output with an input code = 000 hex and a V_{ref} input = 2.048Vdc + $1V_{pp}$ at 1kHz.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input clock, applied at the SCLK terminal, should be inhibited low when $\overline{CS}$ is high to minimize clock feedthrough.
B. Data input from preceeding conversion cycle.
C. Sixteenth SCLK falling edge

Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

OUTPUT SINK CURRENT
vs
OUTPUT PULLDOWN VOLTAGE

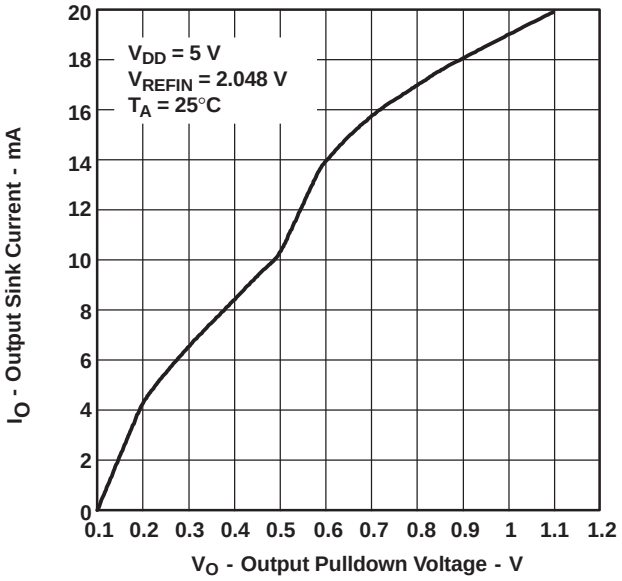


Figure 2.

OUTPUT SOURCE CURRENT
vs
OUTPUT PULLUP VOLTAGE

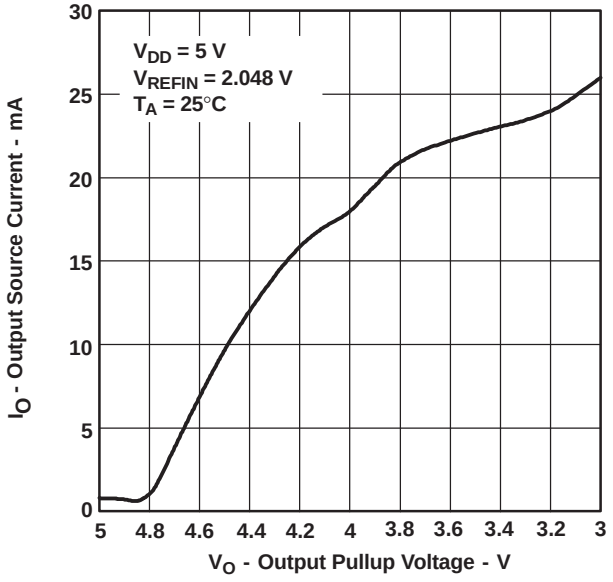


Figure 3.

SUPPLY CURRENT
vs
TEMPERATURE

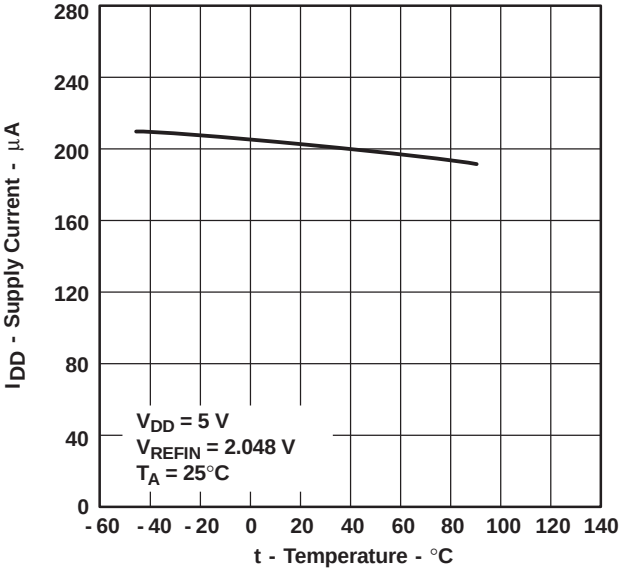


Figure 4.

V_{REFIN} TO $V_{(OUT)}$ RELATIVE GAIN
vs
INPUT FREQUENCY

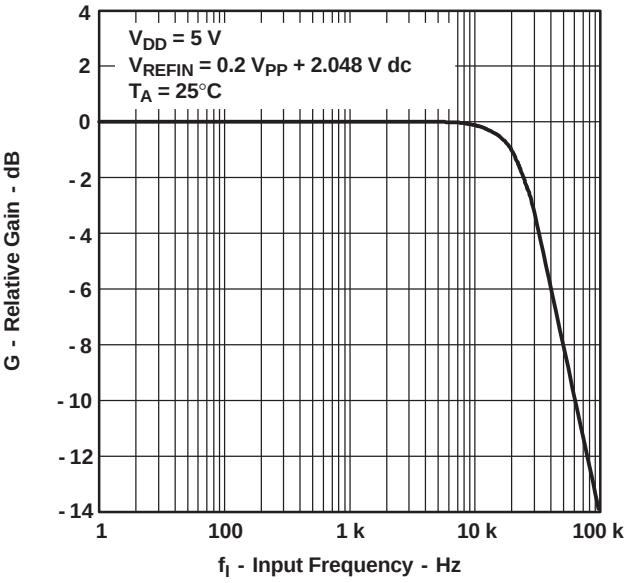


Figure 5.

TYPICAL CHARACTERISTICS (continued)

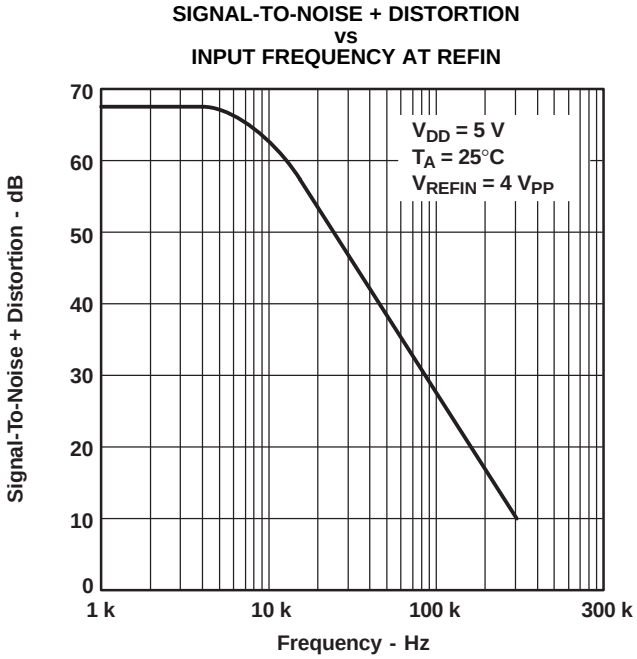


Figure 6.

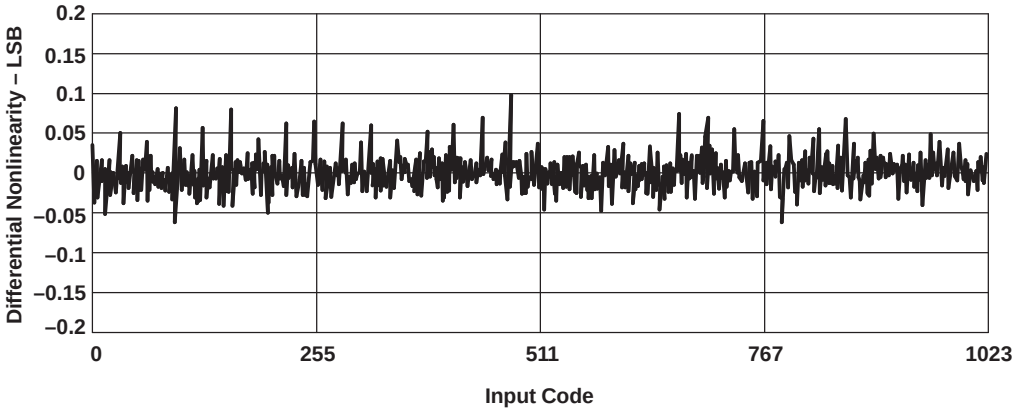


Figure 7. Differential Nonlinearity With Input Code

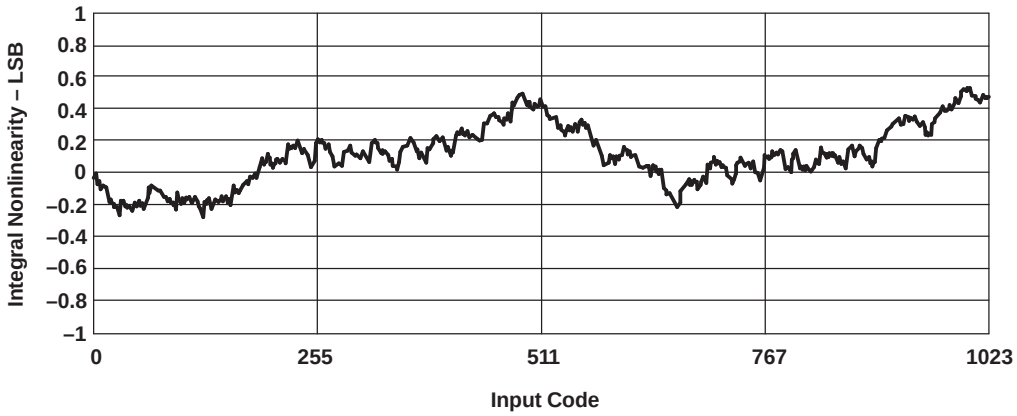


Figure 8. Integral Nonlinearity With Input Code

APPLICATION INFORMATION

GENERAL FUNCTION

The TLC5615 uses a resistor string network buffered with an op amp in a fixed gain of 2 to convert 10-bit digital data to analog voltage levels (see functional block diagram and Figure 9). The output of the TLC5615 is the same polarity as the reference input (see Table 1).

An internal circuit resets the DAC register to all zeros on power up.

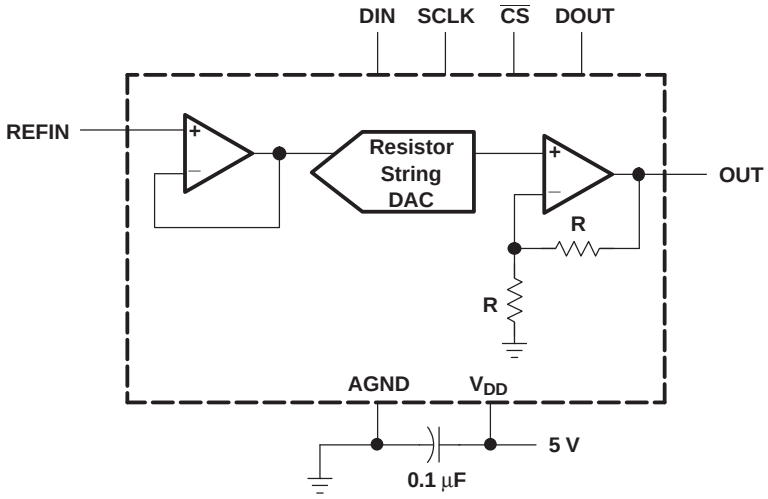


Figure 9. TLC5615 Typical Operating Circuit

Table 1. Binary Code Table (0V to 2V_{REFIN}Output), Gain = 2

INPUT[1]			OUTPUT
1111	1111	11(00)	$2\left(V_{REFIN}\right)\frac{1023}{1024}$
	:		:
1000	0000	01(00)	$2\left(V_{REFIN}\right)\frac{513}{1024}$
1000	0000	00(00)	$2\left(V_{REFIN}\right)\frac{512}{1024} = V_{REFIN}$
0111	1111	11(00)	$2\left(V_{REFIN}\right)\frac{511}{1024}$
	:		:
0000	0000	01(00)	$2\left(V_{REFIN}\right)\frac{1}{1024}$
0000	0000	00(00)	0 V

(1) A 10-bit data word with two bits below the LSB bit (sub-LSB) with 0 values must be written since the DAC input latch is 12 bits wide.

BUFFER AMPLIFIER

The output buffer has a rail-to-rail output with short circuit protection and can drive a 2kΩ load with a 100pF load capacitance. Settling time is 12.5µs typical to within 0.5LSB of final value.

EXTERNAL REFERENCE

The reference voltage input is buffered, which makes the DAC input resistance not code dependent. Therefore, the REFIN input resistance is 10MΩ and the REFIN input capacitance is typically 5pF independent of input code. The reference voltage determines the DAC full-scale output.

LOGIC INTERFACE

The logic inputs function with either TTL or CMOS logic levels. However, using rail-to-rail CMOS logic achieves the lowest power dissipation. The power requirement increases by approximately 2 times when using TTL logic levels.

SERIAL CLOCK AND UPDATE RATE

Figure 1 shows the TLC5615 timing. The maximum serial clock rate is:

$$f_{(SCLK)max} = \frac{1}{t_{w(CH)} + t_{w(CL)}}$$

or approximately 14MHz. The digital update rate is limited by the chip-select period, which is:

$$t_{p(CS)} = 16 \times \left(t_{w(CH)} + t_{w(CL)} \right) + t_{w(CS)}$$

and is equal to 820ns which is a 1.21MHz update rate. However, the DAC settling time to 10 bits of 12.5µs limits the update rate to 80kHz for full-scale input step transitions.

SERIAL INTERFACE

When chip select ($\overline{CS}$) is low, the input data is read into a 16-bit shift register with the input data clocked in most significant bit first. The rising edge of the SLCK input shifts the data into the input register.

The rising edge of $\overline{CS}$ then transfers the data to the DAC register. When $\overline{CS}$ is high, input data cannot be clocked into the input register. All $\overline{CS}$ transitions should occur when the SCLK input is low.

If the daisy chain (cascading) function (see daisy-chaining devices section) is not used, a 12-bit input data sequence with the MSB first can be used as shown in Figure 10:

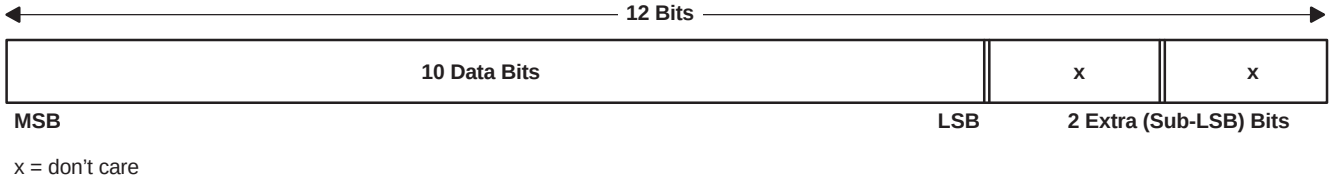


Figure 10. 12-Bit Input Data Sequence

or 16 bits of data can be transferred as shown in Figure 11 with the 4 upper dummy bits first.

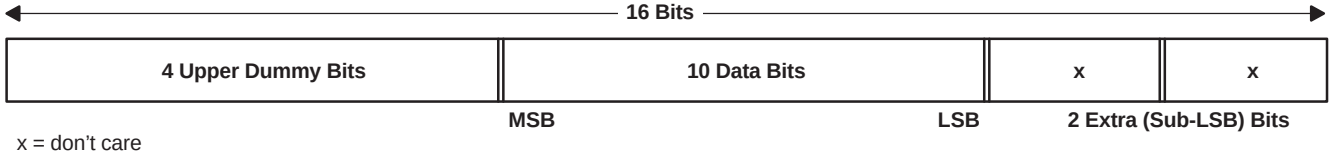


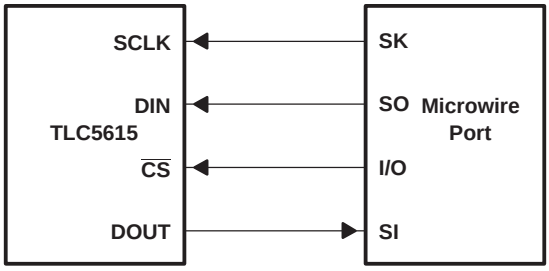
Figure 11. 16-Bit Input Data Sequence

The data from DOUT requires 16 falling edges of the input clock and, therefore, requires an extra clock width. When daisy chaining multiple TLC5615 devices, the data requires 4 upper dummy bits because the data transfer requires 16 input-clock cycles plus one additional input-clock falling edge to clock out the data at the DOUT terminal (see Figure 1).

The two extra (sub-LSB) bits are always required to provide hardware and software compatibility with 12-bit data converter transfers.

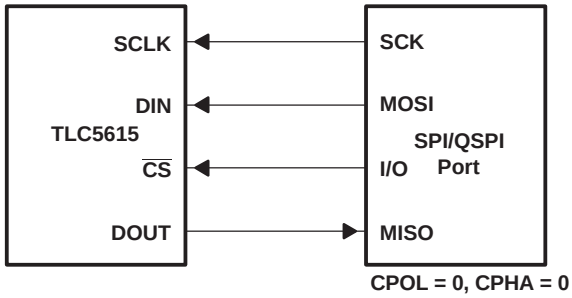
The TLC5615 three-wire interface is compatible with the SPI, QSPI, and Microwire serial standards. The hardware connections are shown in Figure 12 and Figure 13.

The SPI and Microwire interfaces transfer data in 8-bit bytes; therefore, two write cycles are required to input data to the DAC. The QSPI interface, which has a variable input data length from 8 to 16 bits, can load the DAC input register in one write cycle.



NOTE A: The DOUT-SI connection is not required for writing to the TLC5615 but may be used for verifying data transfer if desired.

Figure 12. Microwire Connection



NOTE A: The DOUT-MISO connection is not required for writing to the TLC5615 but may be used for verifying data transfer.

Figure 13. SPI/QSPI Connection

DAISY-CHAINING DEVICES

DACs can be daisy-chained by connecting the DOUT terminal of one device to the DIN of the next device in the chain, providing that the setup time, $t_{su(CSS)}$ ($\overline{CS}$ low to SCLK high), is greater than the sum of the setup time, $t_{su(DS)}$, plus the propagation delay time, $t_{pd(DOUT)}$, for proper timing (see digital input timing requirements section). The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. DOUT is a totem-poled output for low power. DOUT changes on the SCLK falling edge when $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT remains at the value of the last data bit and does not go into a high-impedance state.

LINEARITY, OFFSET, AND GAIN ERROR USING SINGLE-ENDED SUPPLIES

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 14.

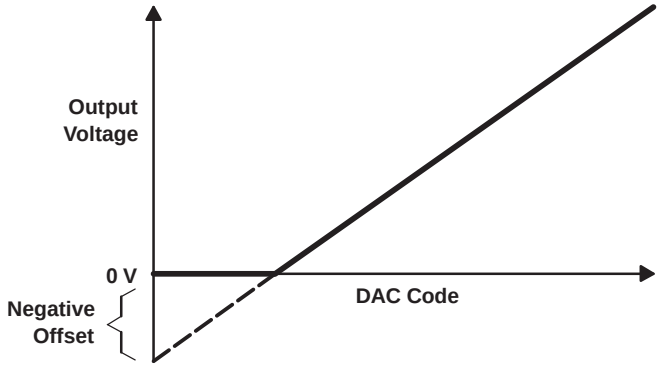


Figure 14. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs '0') and full-scale code (all inputs '1') after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. For the TLC5615, the zero-scale (offset) error is ±3LSB maximum. The code is calculated from the maximum specification for the negative offset.

POWER-SUPPLY BYPASSING AND GROUND MANAGEMENT

Printed circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1μF ceramic-capacitor bypass should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 15 shows the ground plane layout and bypassing technique.

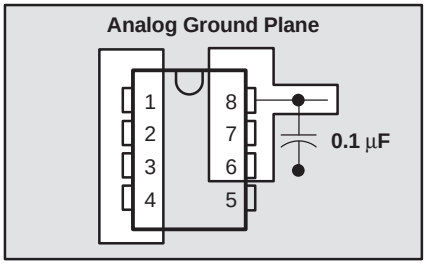


Figure 15. Power-Supply Bypassing

SAVING POWER

Setting the DAC register to all 0s minimizes power consumption by the reference resistor array and the output load when the system is not using the DAC.

AC CONSIDERATIONS

Digital Feedthrough

Even with $\overline{CS}$ high, high-speed serial data at any of the digital input or output terminals may couple through the DAC package internal stray capacitance and appear at the DAC analog output as digital feedthrough. Digital feedthrough is tested by holding $\overline{CS}$ high and transmitting 0101010101 from DIN to DOUT.

Analog Feedthrough

Higher frequency analog input signals may couple to the output through internal stray capacitance. Analog feedthrough is tested by holding $\overline{CS}$ high, setting the DAC code to all 0s, sweeping the frequency applied to REFIN, and monitoring the DAC output.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from D Revision (August 2003) to E Revision	Page
• Added ESD statement.	2
• Changed —moved package option table from front page.	2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC5615CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5615C
TLC5615CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5615C
TLC5615CDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5615C
TLC5615CDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AEM
TLC5615CDGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AEM
TLC5615CDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AEM
TLC5615CDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	AEM
TLC5615CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5615C
TLC5615CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5615C
TLC5615CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC5615CP
TLC5615CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC5615CP
TLC5615ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5615I
TLC5615ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5615I
TLC5615IDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AEN
TLC5615IDGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AEN
TLC5615IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5615I
TLC5615IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5615I
TLC5615IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC5615IP
TLC5615IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC5615IP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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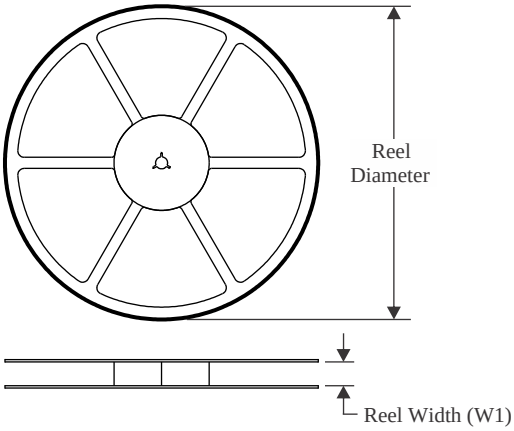
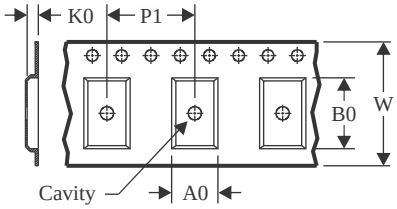
TAPE AND REEL INFORMATION

REEL DIMENSIONS

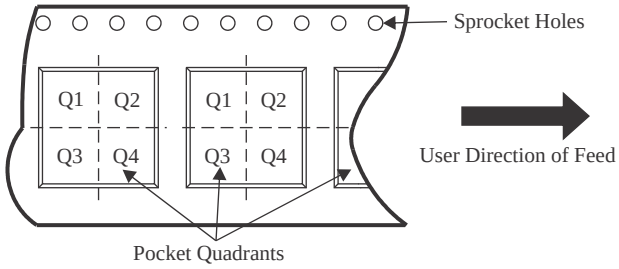


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

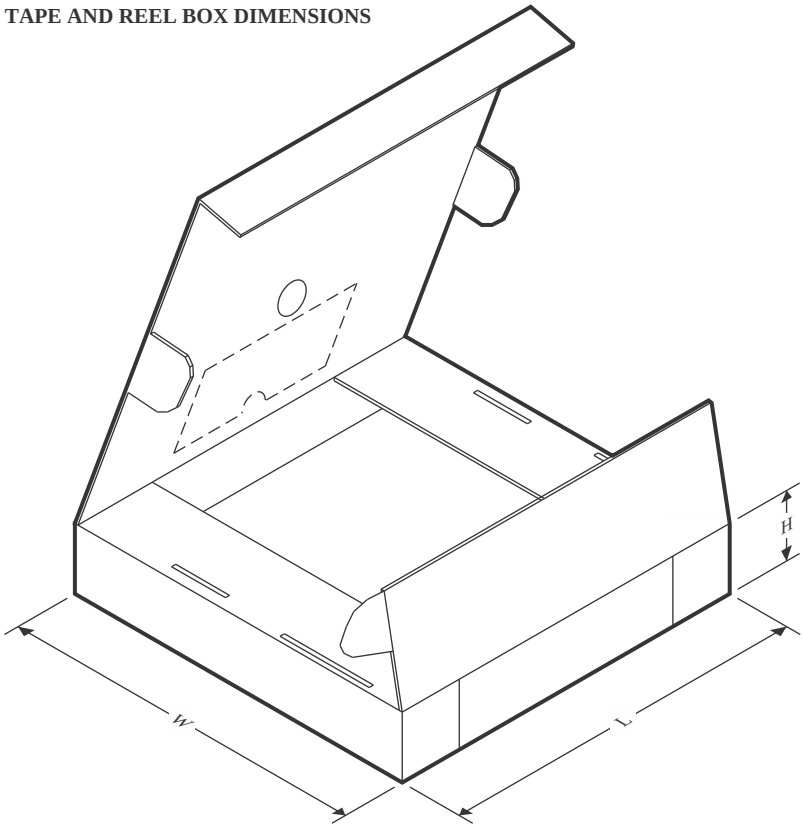
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5615CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLC5615CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC5615IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

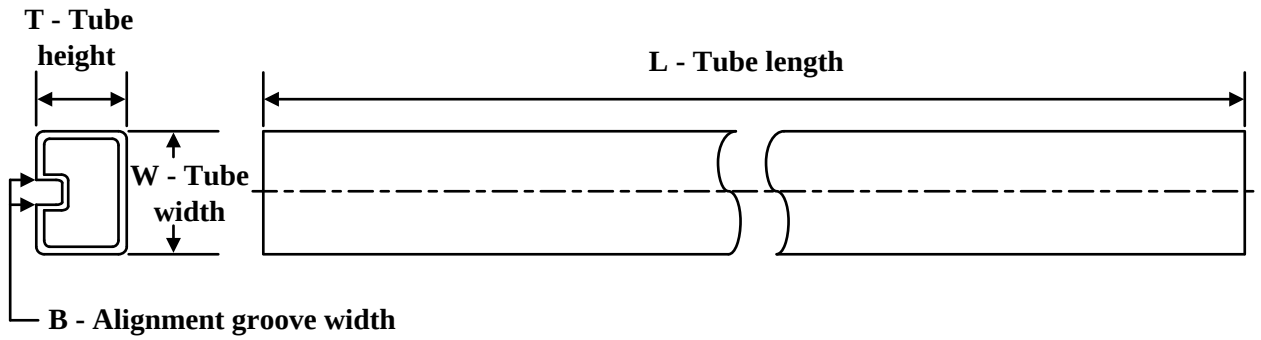
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

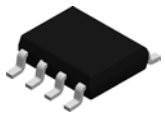
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5615CDGKR	VSSOP	DGK	8	2500	350.0	350.0	43.0
TLC5615CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC5615IDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC5615CD	D	SOIC	8	75	505.46	6.76	3810	4
TLC5615CD	D	SOIC	8	75	507	8	3940	4.32
TLC5615CD.A	D	SOIC	8	75	507	8	3940	4.32
TLC5615CD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC5615CDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLC5615CDG4	D	SOIC	8	75	507	8	3940	4.32
TLC5615CDGK	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
TLC5615CDGK.A	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
TLC5615CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC5615CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC5615ID	D	SOIC	8	75	505.46	6.76	3810	4
TLC5615ID	D	SOIC	8	75	507	8	3940	4.32
TLC5615ID.A	D	SOIC	8	75	507	8	3940	4.32
TLC5615ID.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC5615IDGK	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
TLC5615IDGK.A	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
TLC5615IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC5615IP.A	P	PDIP	8	50	506	13.97	11230	4.32

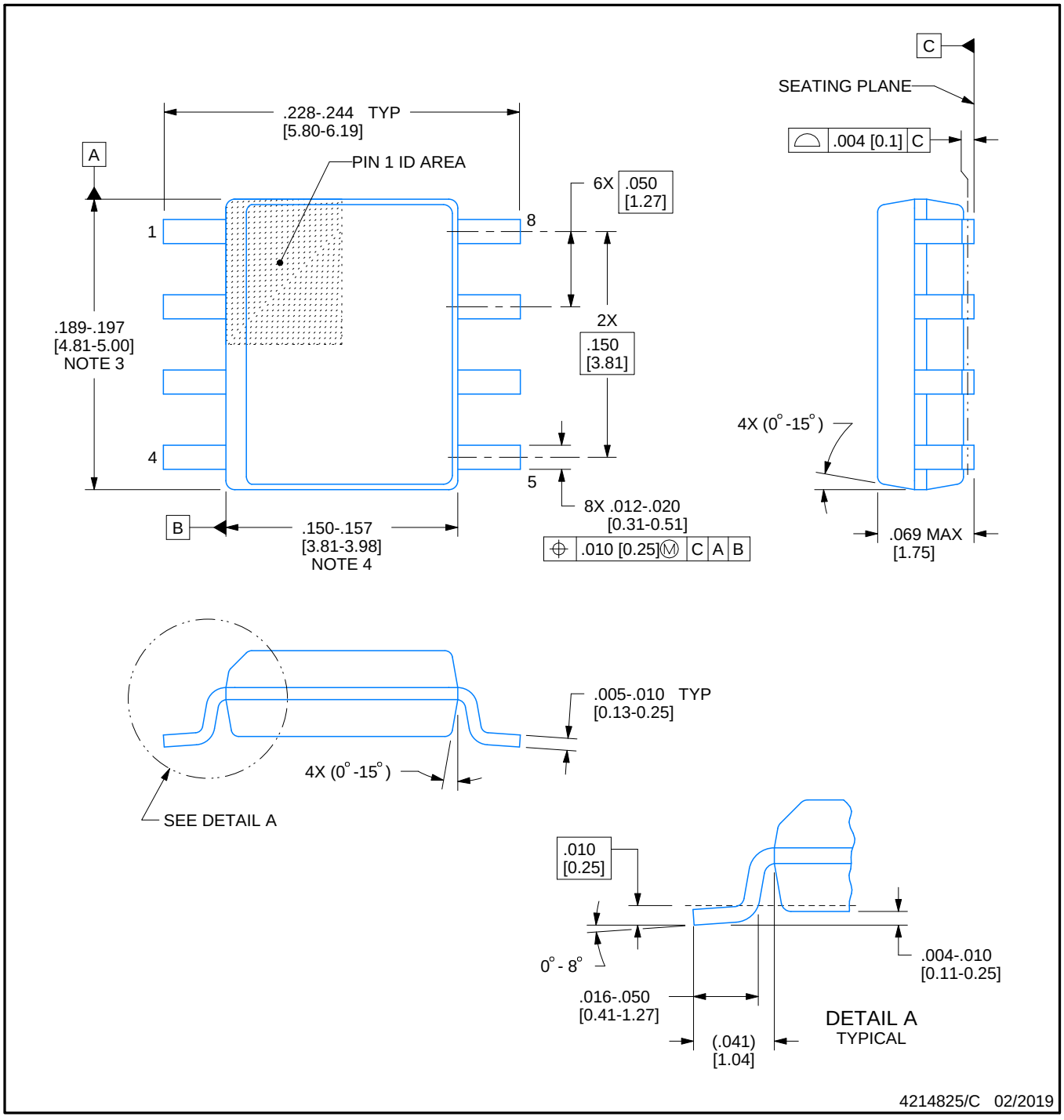


PACKAGE OUTLINE

D0008A

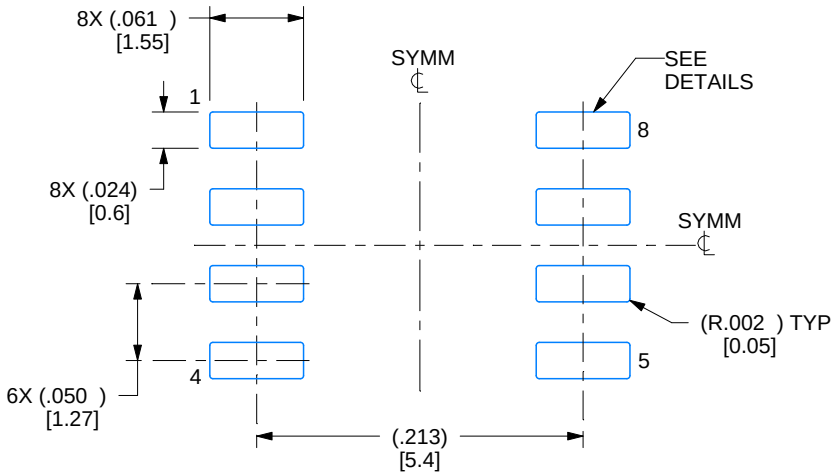
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

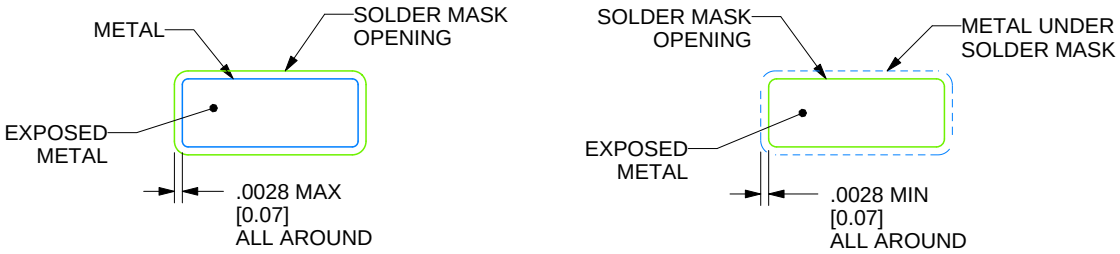


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

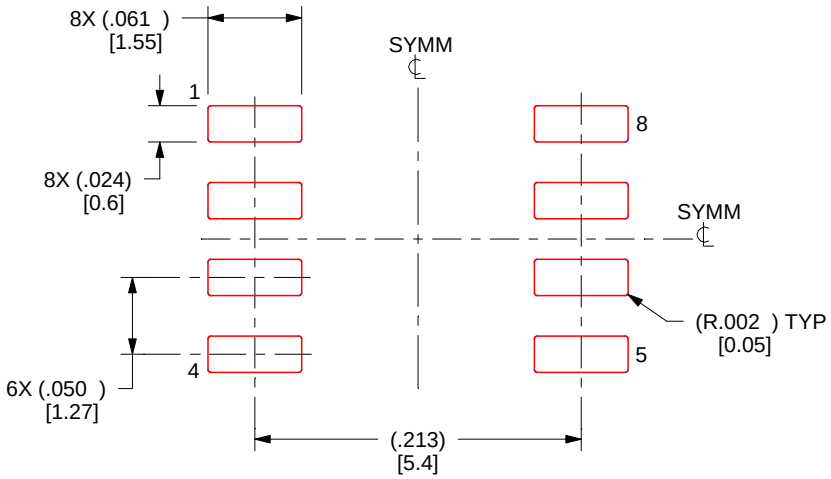
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



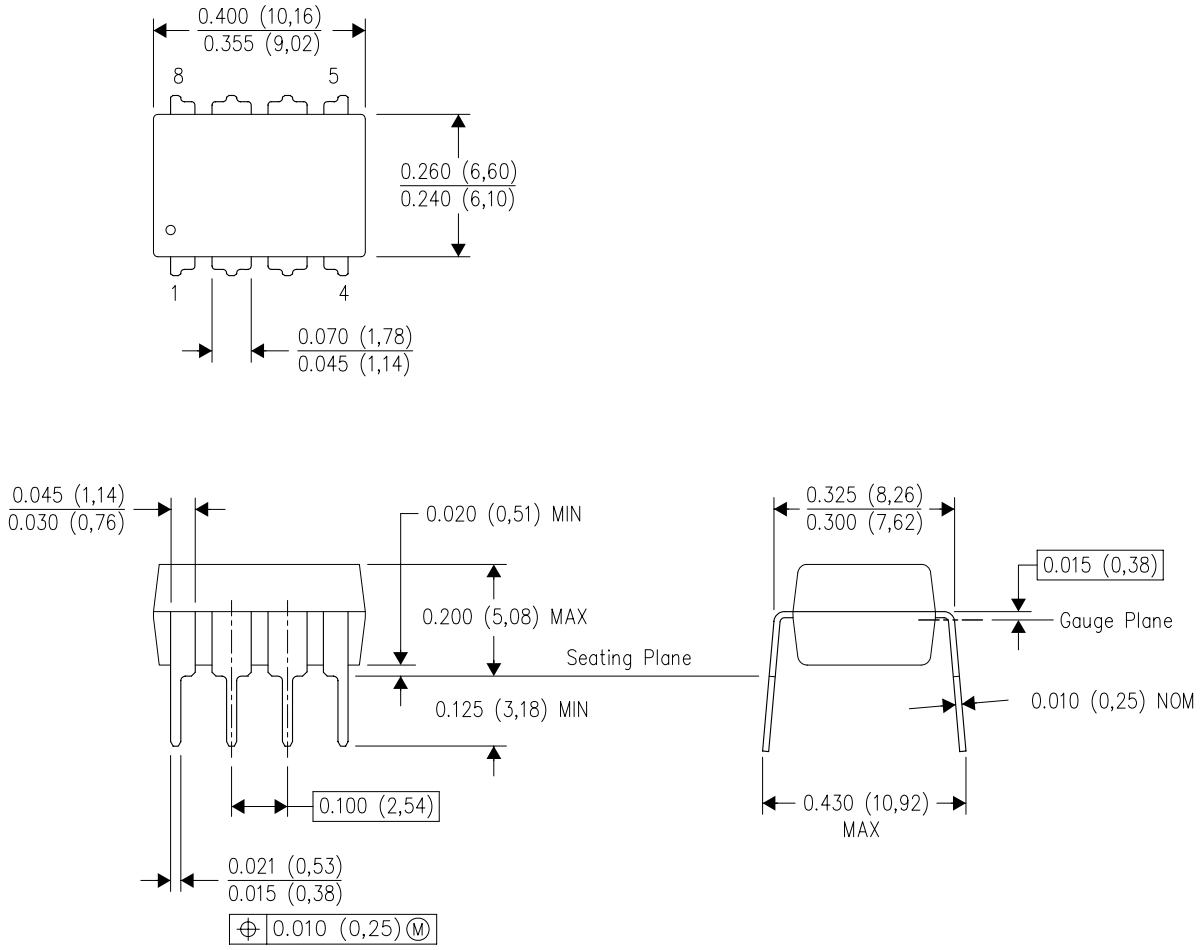
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



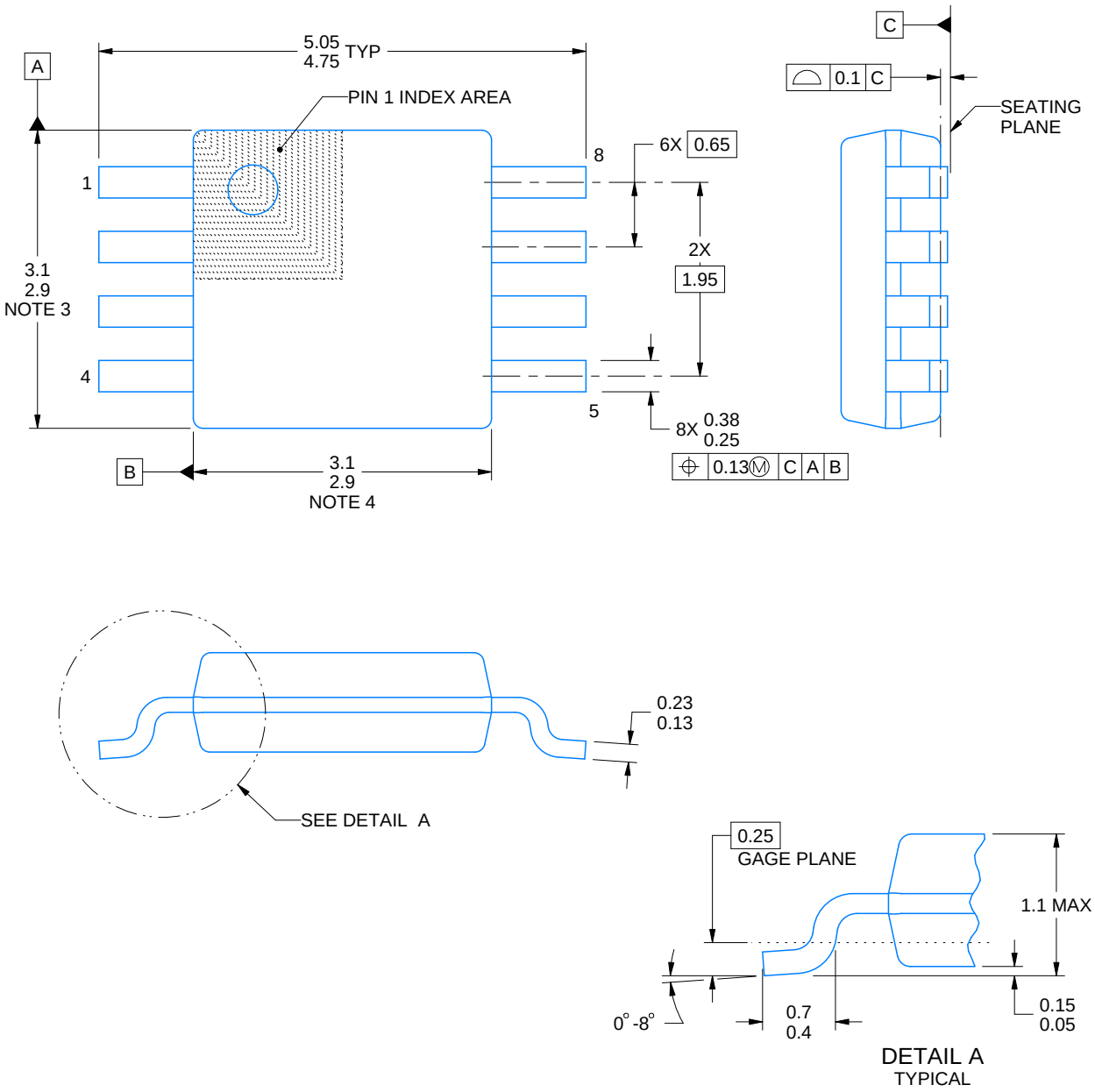
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

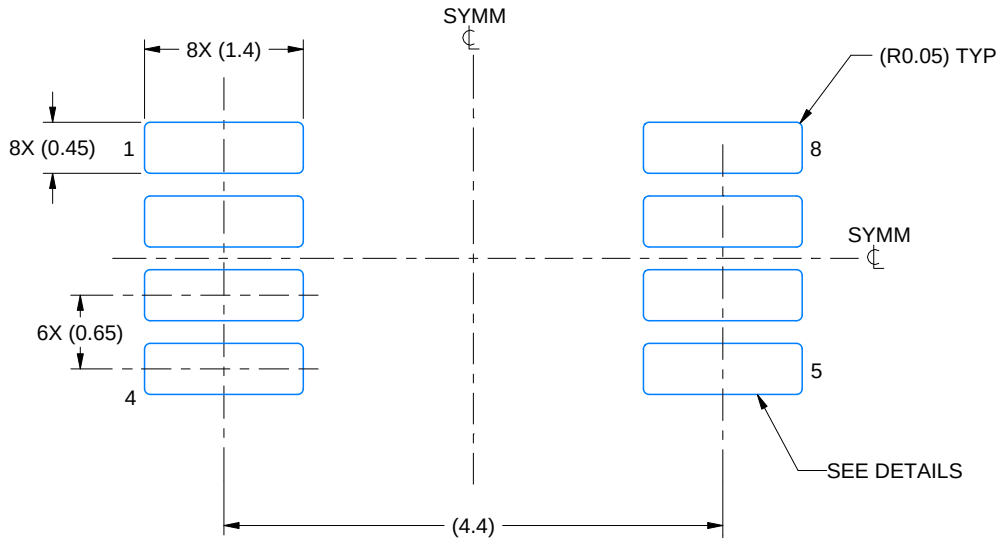
SMALL OUTLINE PACKAGE



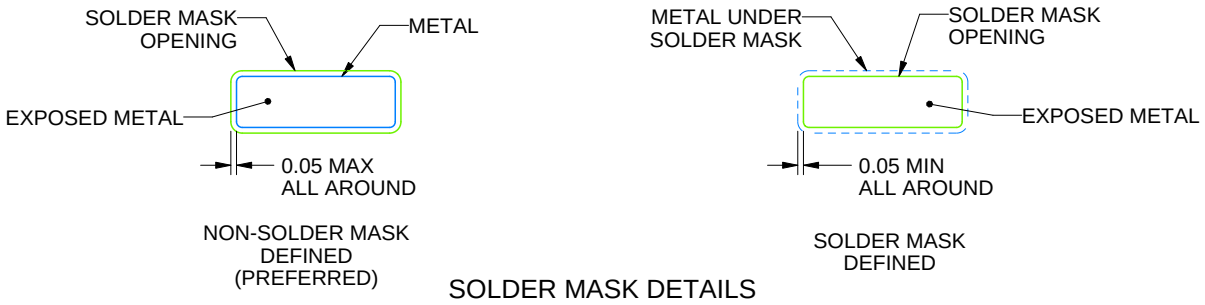
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

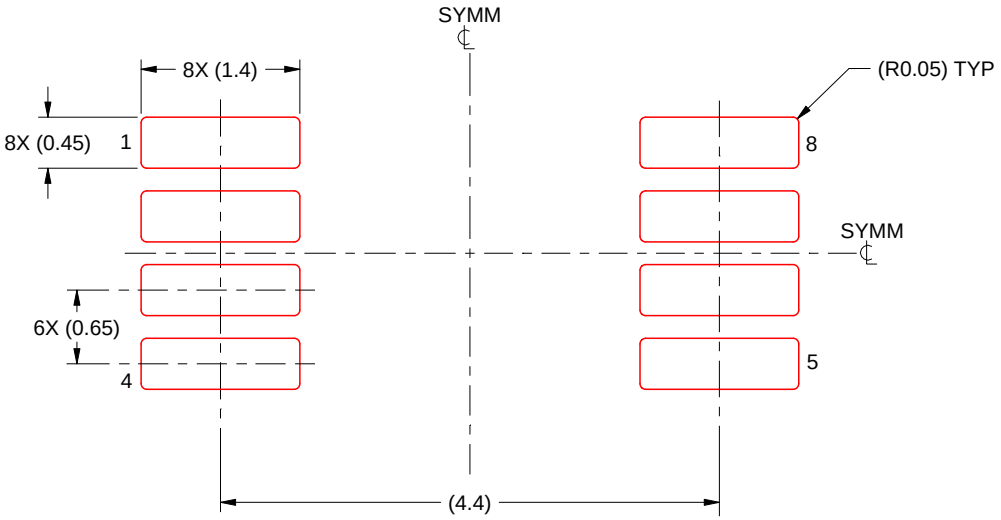


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025