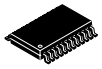


SLLS528 – MARCH 2002

12–CHANNEL LED DRIVER

FEATURES

- **0.2-mA to 40-mA (Constant-Current Sink) Drive Capability x 12 Bits Output Count into 24-Pin HTSSOP Package**
- **1024 Gray-Scale Display (PWM Control 1024 Steps) with Max 25-MHz Clock Frequency**
- **3-Way Brightness Adjustment**
  - **Plane Brightness Adjustment for 64 Steps (40% to 100%)**
  - **Frequency Division for 16 Steps (6.3% to 100%)**
  - **Dot Correction for 256 Steps (0% to 100%)**
- **DS–Link Data Input/Output (Data Rate Max 20 Mbps) with Packet Operation**
- **5 Error Information Types and 2 Gray–Scale Clock Modes**
- **3.3-V V_{CC} and LVTTL Interface**

APPLICATION

- **Full- or Multi-Color LED Display**

DESCRIPTION

The TLC5930 is a constant-current sink driver with an adjustable current value, and 1024 gray scale display that uses pulse width control. The output current is 0.2 mA to 40 mA with 12 bits of RGBx4. The maximum current value of the constant-current output can be set by one external resistor.

The TLC5930 includes three kinds of brightness adjustment functions: one adjusts the plane brightness between devices, changing the current values of all outputs uniformly. The second adjusts the frequency division to controls overall panel brightness, and the third adjusts the dot correction per LED, changing the current values of independent output.

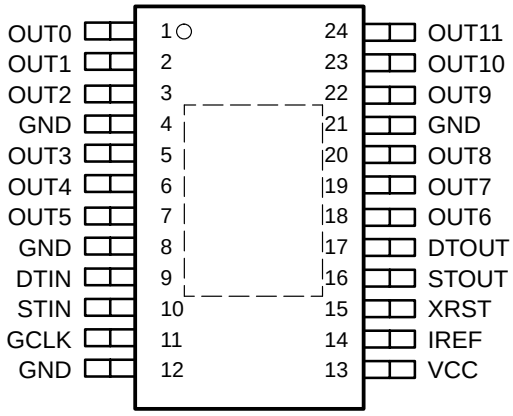
The TLC5930 also includes color–tone correction function for correcting color per dot (pixel) and OVM function for constant-current output terminals used for LED failure detection.

Other features include the thermal error flag (TEF). The active wire-check (AWC) to check the communication between the controller and the device. The LED leakage-detect (LKD) to detect the reverse leakage on the LED. The GCLK error flag (GEF) and the HSYNC error flag (HEF) by monitoring the gray-scale clock count, and the dual source gray-scale clock (DSG) function to switch the gray-scale clock to the external input clock or to switch the internally-generated clock.

The TLC5930 requires three signals for standard operation: data input and gray-scale clock. Only three-signal line and 24-pin HTSSOP package reduce board area and total cost.

PowerPAD is a trademark of Texas Instruments Incorporated.

PWP PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	PACKAGE
	PowerPad TSSOP (PWP)
–20°C to 85°C	TLC5930PWP

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, VCC . . . . . –0.3 V to 4.0 V
Output current (dc), $I_{O(LC)}$ . . . . . 45 mA
Input voltage range, V_{IN} . . . . . –0.3 V to VCC
Output voltage range, V_{DTOUT}, V_{STOUT} . . . . . –0.3 V to (VCC – 0.2 V)
V_{OUT0} – V_{OUT11}, (when off) . . . . . –0.3 V to 17 V
V_{OUT0} – V_{OUT11}, (when on) . . . . . –0.3 V to 10 V
Storage temperature range, T_{stg} . . . . . –40°C to 125°C
Power dissipation rating at (or above) T_A = 25°C . . . . . 3.7 W

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages values are with respsect to GND terminal.
2. At operating temperature range over 25°C, dependent on derating factor of 41 mW/°C.

electrical characteristics, MIN/MAX: V_{CC} = 3.0 V to 3.6 V, T_A = – 20°C to 85°C, TYP: V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 1 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA			0.4	V
I_I	Input current	V_{IN} = V_{CC} or GND			± 1	µA
I_{CC}	Supply current	Input signal is static, V_{OUT} = 1 V, R_{IREF} = 5.1 kΩ, LL output bits off		16	21	mA
		Input signal is static, V_{OUT} = 1 V, R_{IREF} = 5.1 kΩ, LL output bits on		40	50	mA
$I_{O(LC)}$	Constant-current output current	V_{OUTn} = 1.0 V, R_{IREF} = 5.1 kΩ, LL output bits on	35	40	45	mA
I_{LKG}	Output leakage current	OUT0 to OUT11 ($V_{(OUTn)}$ = 15 V)			0.1	µA
ΔI_{OLC}	Constant-current outout error between bits	OUT0 to OUT11 ($V_{(OUTn)}$ = 1 V), R_{IREF} = 5.1 kΩ			± 4%	
ΔI_{OLC1}	Changes in constant output current depend on supply voltage	V_{REF} = 1.23 V			± 3	%/V
ΔI_{OLC2}	Changes in constant output current depend on output voltage	V_{OUT} = 1 V to 3 V, R_{IREF} = 5.1 kΩ, V_{IREF} = 1.23 V, 1 bit light on			± 1	%/V
ΔI_{OLC3}	Changes in constant output current depend on brightness data	V_{OUT} = 1.3 V, R_{IREF} = 5.1 kΩ, V_{IREF} = 1.23 V, 1 bit light on			± 2	%/V
T_{TSD}	TEF detection temperature	Junction temperature	150	160	170	°C
V_{IREF}	Reference voltage	R_{IREF} = 5.1 kΩ		1.23		V

switching characteristics, C_L = 15 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time	DTOUT, STOUT		12	15	ns
t_F	Fall time	DTOUT, STOUT		10	13	ns
		OUT*n*, See Figure 1		15	40	ns
t_{PD}	Propagation delay time	GCLK – OUT0 on		90	110	ns
		GCLK – OUT0 off		35	60	ns
		[(OUT*n* + 1) – OUT*n*]		25	40	ns
		DTIN – OUT0, STIN – OUT0			60	ns
		DTIN – DTOUT, DTIN, STOUT STIN – DTOUT, STIN, STOUT(1)		18	25	ns
		Operation mode setting (all output force off) – OUT0 off		60	90	ns
t_{EDGE}	Duty deviation between edge of DTIN and STIN	DTOUT/STOUT, STOUT/DTOUT	–10	± 1	10	ns

(1) This specification shows the delay of edge for DATA/STROBE, but data appears in the output with 2 bits delay. (Data propagation delay time is 2 bits + $t_{D\ [D/STIN – D/STOUT]}$)

recommended operating conditions

dc characteristics

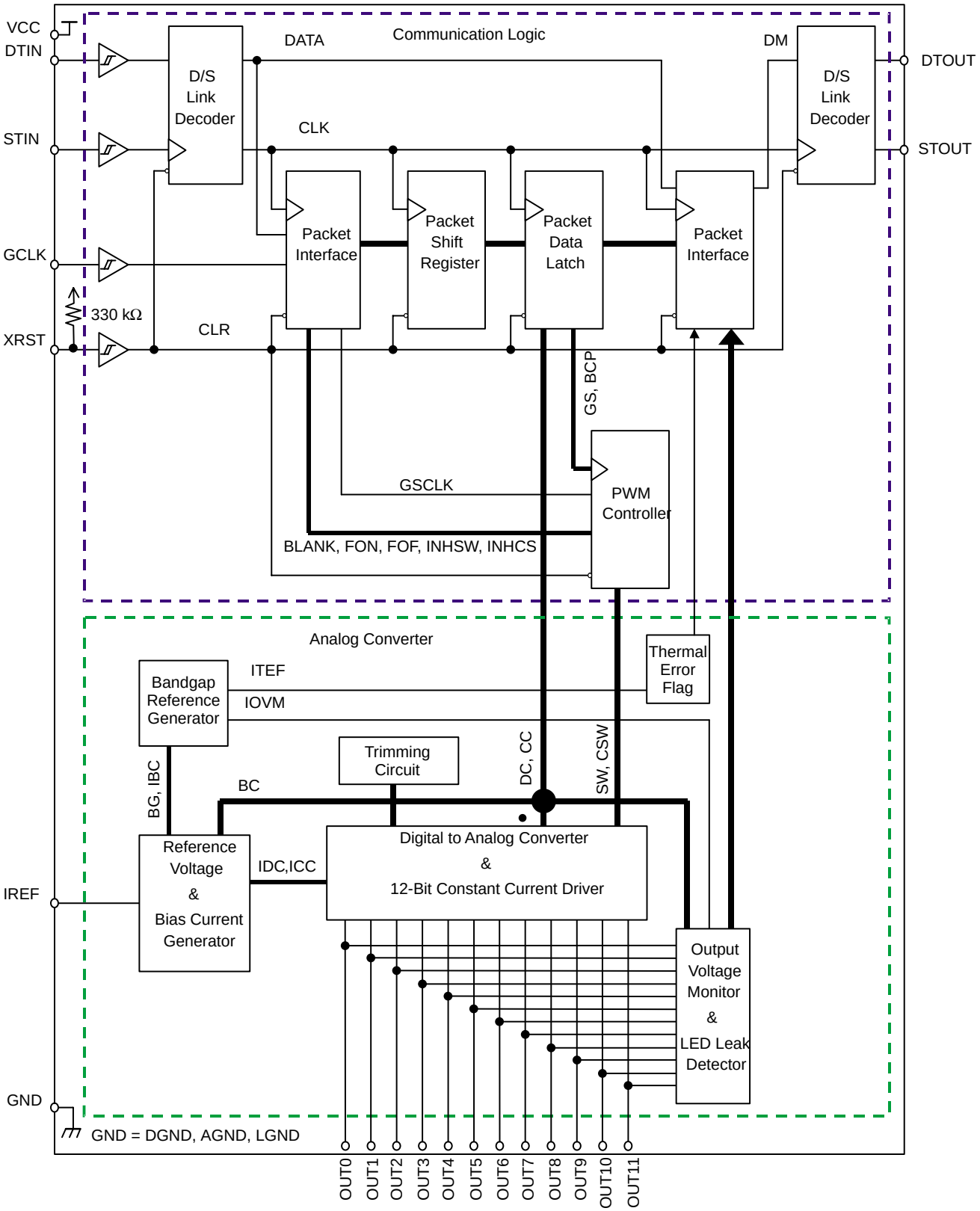
PARAMETER	CONDITIONS	MIN	MAX	UNIT
Supply voltage, V_{CC}		3.0	3.6	V
Voltage applied to constant-current output, V_O	OUT0 to OUT11 off		15	V
	OUT0 to OUT11 on		10	V
High-level input voltage, V_{IH}		2.0	VCC	V
Low-level input voltage, V_{IL}		GND	0.8	V
High-level output current, I_{OH}	V_{CC} = 3.1 V @ DTOUT, STOUT		– 1.0	mA
Low-level output current, I_{OL}	V_{CC} = 3.1 V @ DTOUT, STOUT		1.0	mA
Constant output current, $I_{O(LC)}$	OUT0 to OUT11		40	mA
Operating free-air temperature range, T_A		– 20	85	°C

ac characteristics, V_{CC} = 3.1 V to 3.5 V, T_A = –20°C to 85°C (unless otherwise noted)

PARAMETER		CONDITIONS		MIN	MAX	UNIT
$f_{(GCLK)}$	GCLK clock frequency(1)	2 gray scale inputs	$I_{O(LC)}$ = 40 mA		25	MHz
$t_{(EDGE)}$	Time between edges	DTIN – STIN,	STIN – DTIN	30		ns
$t_{w(H)}/t_{w(L)}$	GCLK pulse duration			20		ns
$t_{w(L)}$	XRST reset pulse duration			1		ms
$t_{(DATA)}$	Data transfer rate				20	Mb/s
t_{SU}	Setup time	HSYNC – GCLK			6.5	ns

(1) This is the frequency when any output is obtailed at two or more than gray-scale entered.

functional block diagram

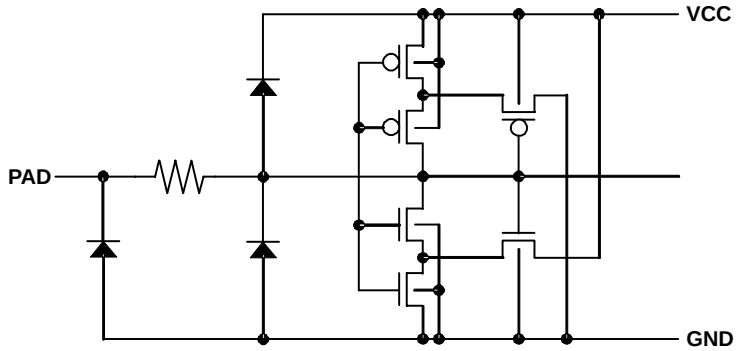


Terminal Functions

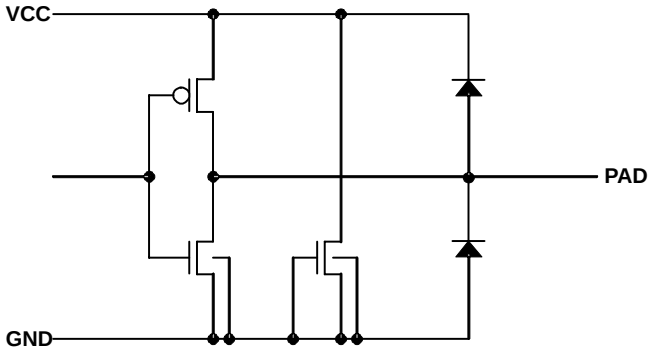
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DTIN	9	I	DS–link data input
DTOUT	17	O	DS–link data output
GCLK	11	I	Clock input for gray scale. The gray scale display is accomplished by lighting the LED until the number of the gray-scale clock counted is equal to the data latched.
GND	4, 8, 12, 21	–	Ground
IREF	14	I/O	Constant-current value setting. LED current is set to the desired value by connecting an external resistor between IREF and GND. The 168 times current compared to current across the external resistor flows through the constant-current output terminals.
OUT0	1	O	Constant-current output.
OUT1	2		
OUT2	3		
OUT3	5		
OUT4	6		
OUT5	7		
OUT6	18		
OUT7	19		
OUT8	20		
OUT9	22		
OUT10	23		
OUT11	24		
STIN	10	I	DS–link strobe input
STOUT	16	O	DS–link strobe output
VCC	13	I	Power supply
XRST	15	I	Reset signal. This signal is used to initialize the device reset is accomplished by pulling this pin low (internally pulled up with a 330-kΩ resistor). If not used, this terminal should be left open or connect to V_{CC}.

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

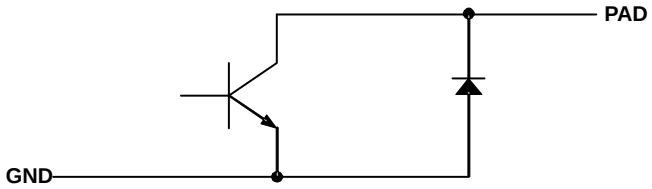
DTIN, STIN, GCLK



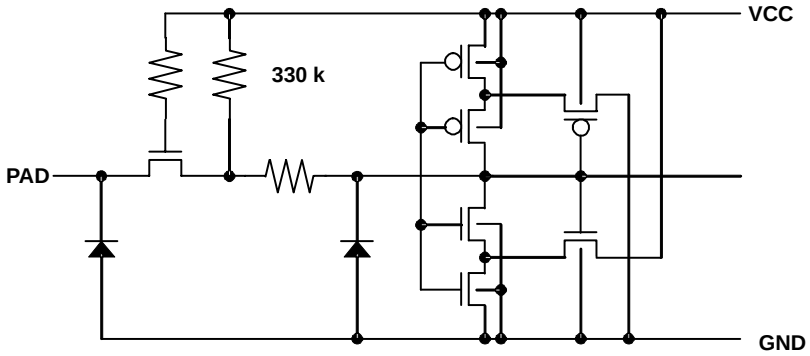
DTOUT, STOUT



OUTn



XRST



TIMING DIAGRAMS

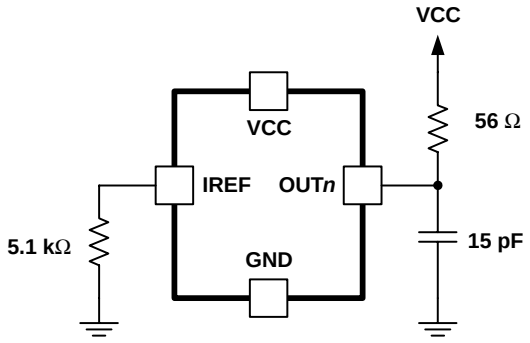


Figure 1. Rise Time and Fall Time Test Circuit for OUT*n*

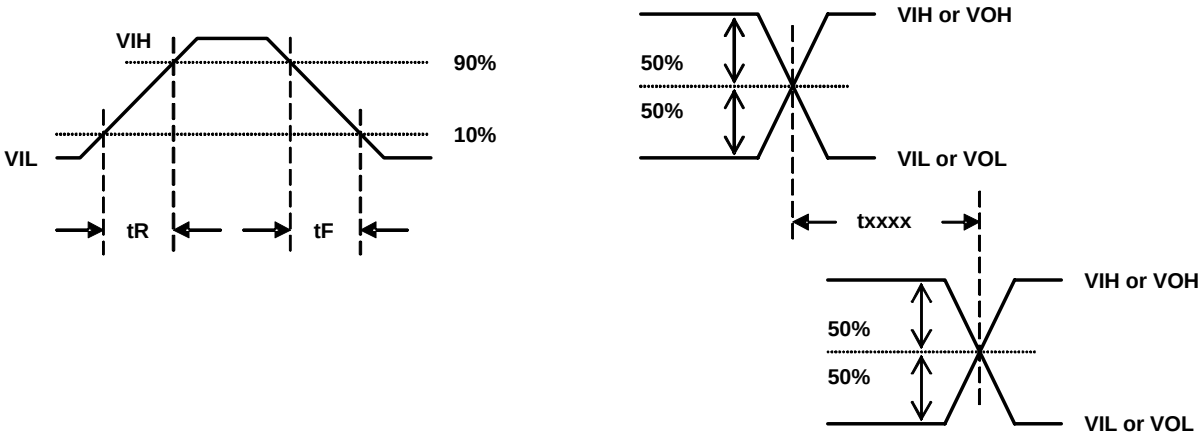


Figure 2. Timing Requirements

PRINCIPLES OF OPERATION

setting for constant output current value

On the constanct current output terminals (OUT0 to OUT11), approximately 168 times the current that flows through the external resistor, R_{IREF}, (connected between IREF and GND) can flow. The external resistor value is calculated using the following equation:

$$R_{(IREF)}\,(\Omega) = \frac{168 \times 1.23\ V}{I_{O(LC)}\,(A)} \quad (1)$$

where $R_{(IREF)}$ should be $\leq 4.88\ k\Omega$

Note that more current flows if IREF is connected directly to GND.

PRINCIPLES OF OPERATION

command packet list

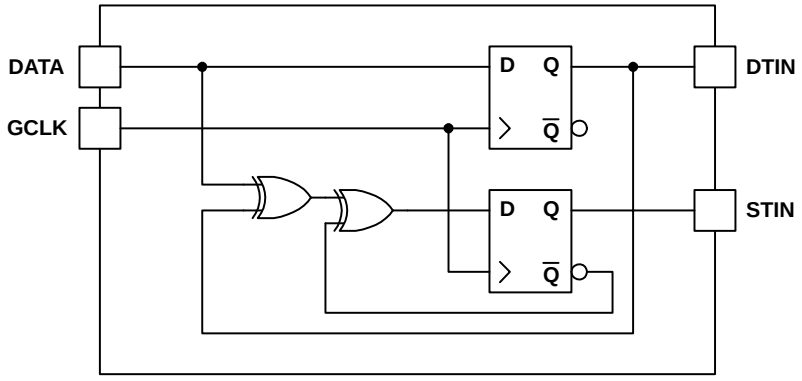
FUNCTION	ID			COMMAND		NO. OF DATA BITS	NO. OF PACKET BITS	MODE
	HEX	CONTROL		HEX	BIN			
		COMMON	INDIVIDUAL					
Internal reset	00	X		00	00000000	8(03h)	24	Write
Gray scale data setting	00or01.FF	X	X	02	00000010	10x12 output	136	Write
Dot correction data setting	00or01.FF	X	X	04	00000100	8x12 output	112	Write
Color tone correction data setting	00or01.FF	X	X	08	00001000	8x4set	48	Write
Plane brightness adjustment data setting	00or01.FF	X	X	10	00010000	16	32	Write
Color tone correction control setting	00or01.FF	X	X	20	00100000	8	24	Write
Operation mode setting	00or01.FF	X	X	40	01000000	16	32	Write
OVM information read	00or01.FF	X	X	50	01010000	16	32	Read
Failure monitor information read	00or01.FF	X	X	60	01100000	8	24	Read
Automatical ID setting	00	X		70	01110000	16(min)	32(min)	Write
HSYNC synchronization	00	X		80	10000000	16	32	Wr/Rd

NOTE Common control is applied to all the devices connected. Indidual control is applied to the device specified by ID.

basic packet configuration

MSB					LSB
ID (8 bit)		CMD (8 bit)		DATA (0 to 120 bit)	
MSB	LSB	MSB	LSB	MSB	LSB

data configuration



UDG–02058

Figure 3. DS LINK Configuration

PRINCIPLES OF OPERATION

packet operation

Data output is performed with delay of two bits from input. In other words, by using the edge of the input, data before two bits appear in the output terminal. Figure 4 shows the concept for data transfer when some TLC5930s are connected in a cascade, where data A–Z indicates valid data, and the asterisk (*) marks invalid data. Also, data A is a first data input from controller, and there is assumed to be no data transition for DATA/STROBE between [H and I] and [S and T] in the IC1 input data.

Invalid data is clocked out corresponding to the input edge to ensure that no data exists before data A. After that, data A is clocked out with a time delay of two bits plus $t_{D(D/STIN–D/STOUT)}$ using the input edge for data C. Once data output is started, data before two bits from current input is sequentially clocked out using the input edge. It should be noted that data output stays during no transition of DATA/STROBE, since no input edge makes the output edge. Figure 4 shows that the output of IC1 remains in data F and does not go to data G until the edge of input data I is entered (after IC1 clocked out data F, although the input data of IC1 is continued from A to H.)

If data A to H are included in one packet, the data output for each output of the device in data H, (which indicates the completion of packet operation), is performed out at the edge establishing data J for IC1, data L for IC2, data O for IC3, and data Q for IC4 from the view of controller. In other words, in order to complete the packet operation for all the devices connected in cascades, additional bit data equivalent to two times the number of devices cascaded is needed to be clocked in.

Additionally, since each device has the time delay, $T_{D(D/STIN–D/STOUT)}$, from input to output, the controller views that output having a time delay exceeding two bits against a virtual input to IC1. In this example, while, in practice, the output data H for IC4 is established by the input edge of data Q, it appears to be synchronized with data S for IC1.

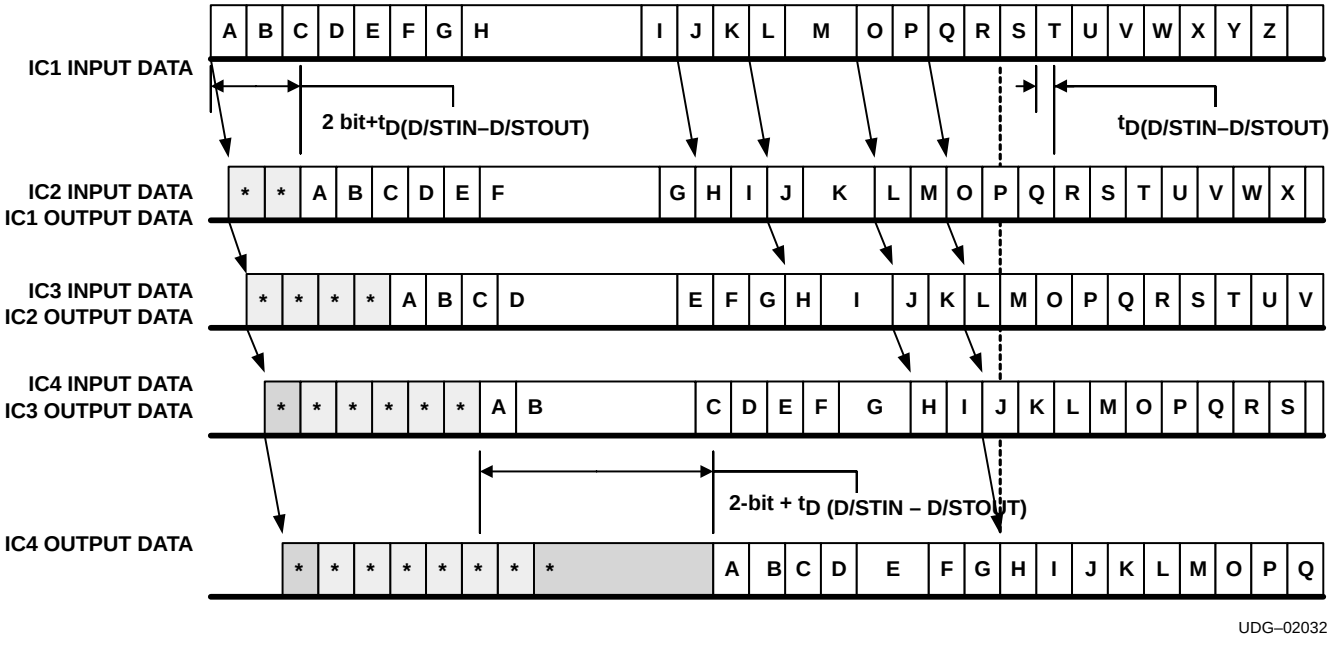


Figure 4. Data Transfer Concept in Cascade Connection

PRINCIPLES OF OPERATION

As shown in Figure 4, in order for all the cascade-connected devices to complete one packet operation, additional bit data to input to the first stage equivalent to two times the number of devices cascaded is required to be clocked in. But, in practice, sending just any data is not acceptable, and some packets with bits corresponding to two times the number of devices connected are needed for synchronization to be successful. For example, in the case that 16 ICs are connected in cascade, since 16 x 2 = 32 bits are needed to complete the packet operation of sixteenth IC, OVM information reading packet as a dummy, which does not write any data to the device, is desirable. Or, an alternative method to send any packet such as use of unused ID (e.g. FFh) is available.

Figure 5 shows the concept for normal lighting-ON operation (based on pulse-width control method). Internal BLANK goes high on the falling edge of the 21st bit in the HSYNC packet. If the constant-current output is ON at that time, it is turned off (except for force on mode), and the data for which the latch flag is set in the HSYNC packet is latched during internal BLANK high-level. Internal BLANK goes low on the rising edge of the gray-scale clock (GCLK) after the edge of LSB (32nd bit) for HSYNC packet, and the TLC5930 goes into the status that can be turned on by the constant-current output. The constant-current output is turned on by the next rising edge of the gray-scale clock.

During power up, the initial value of BLANK is at a high level, therefore, operation for BLANK and constant-current output when HSYNC packet is entered for the first time as a normal operation is different from the example shown in Figure 5.

In addition, since BLANK and the gray-scale clock are ignored in the force-ON mode, the timing to be lighted on is also different from the example shown in Figure 5.

PRINCIPLES OF OPERATION

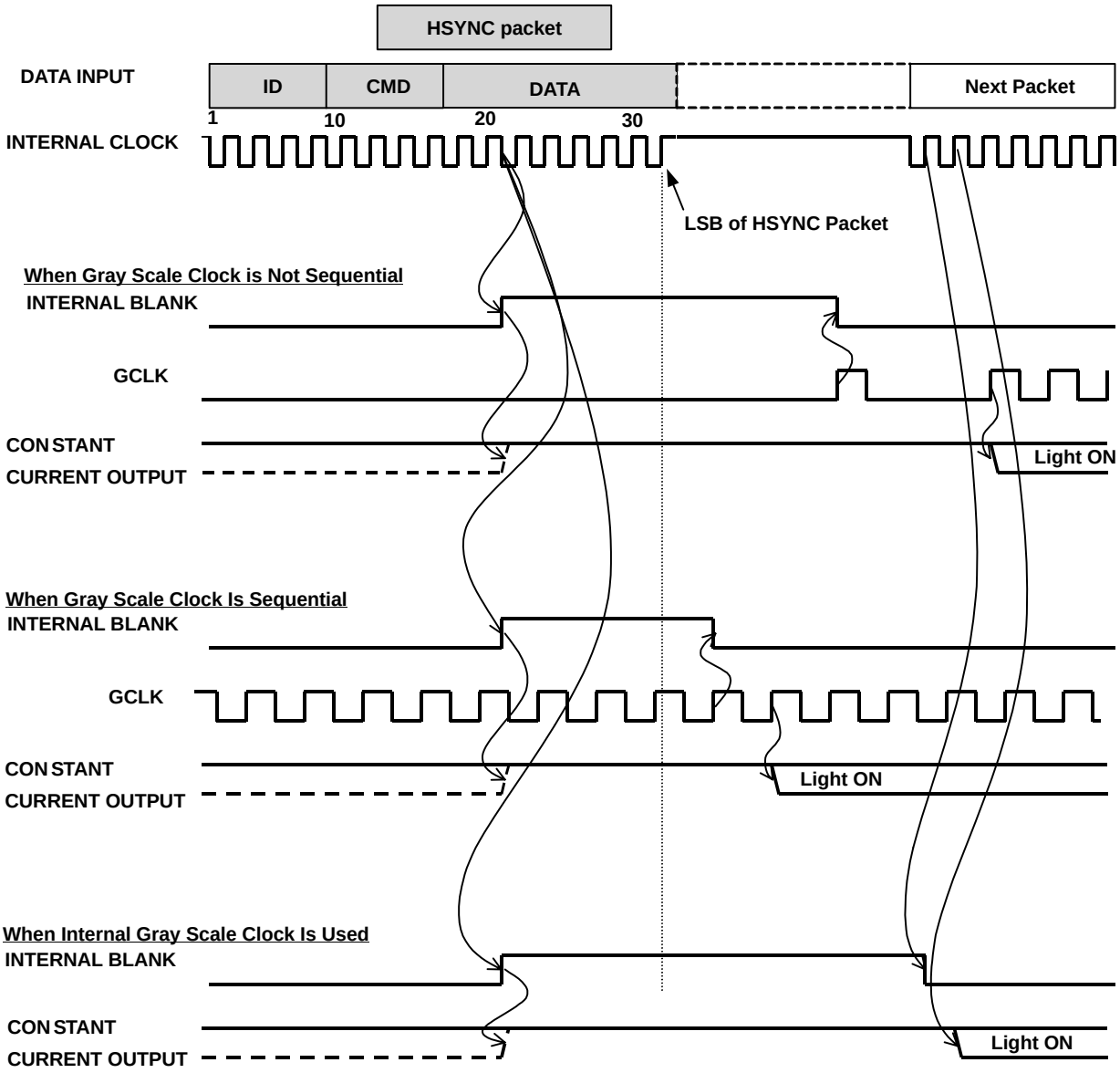


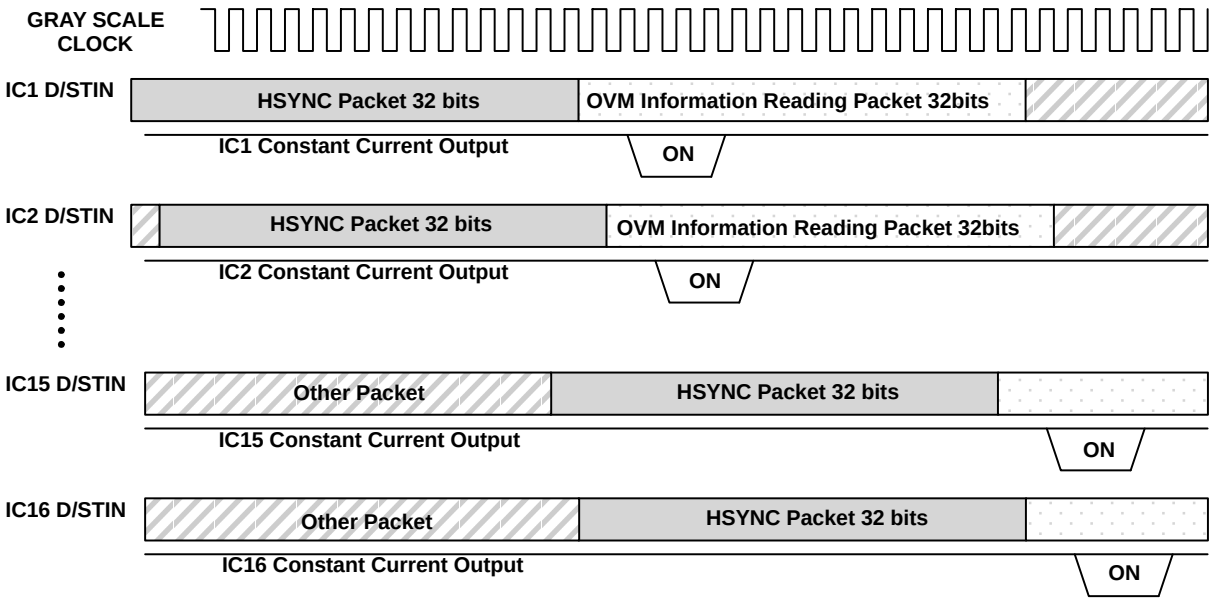
Figure 5. Normal Lighting-ON Operation

PRINCIPLES OF OPERATION

There are two different methods available as shown in Figure 6 for entering the gray-scale clock when in light-ON mode. When the gray-scale clock is sequential, lighting-ON by the device is initiated after the HSYNC packet operation for each device has been completed. When the external clock is used as gray-scale clock, all the devices can be lighted-ON simultaneously by entering the gray scale clock after the HSYNC packet is entered for the last device (in this example, just after OVM information reading packet has entered to IC1).

When Light-ON in a 4 Gray Scale With 16 ICs

When Gray Scale Clock Is Sequential (Including Use of Internally Generated Gray-Scale Clock)



When Gray Scale Clock Is Not Sequential (External Input Only)

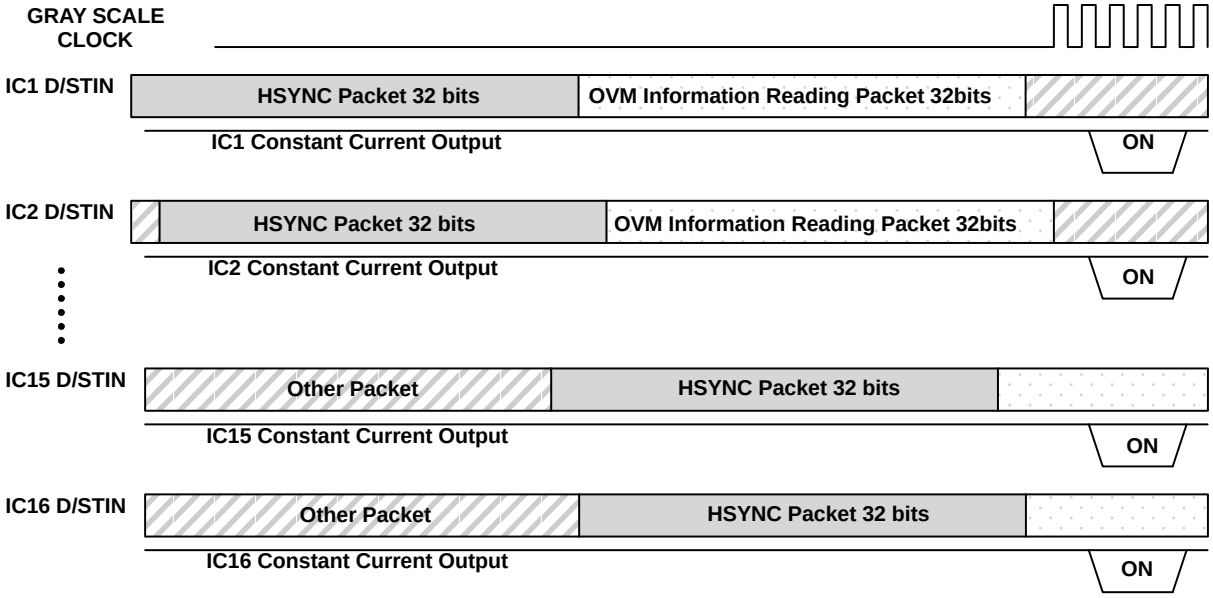


Figure 6. Lighting-ON Operation With 16 Devices

PRINCIPLES OF OPERATION

command packet and operation

internal reset

By sending this packet once, the internal register within all the devices connected is set to the default value and synchronized with the controller. Note that individual reset for the device is not available.

packet configuration

ID (bin)	CMD (bin)	CMD (bin)
00000000	00000000	00000011

default value

REGISTER	DEFAULT VALUE		COMMENTS
ID	xxxxxxxx	Indeterminate (no write)	Automatic ID setting
Plane brightness	111111 (bin)	100%	Plane brightness adjustment data setting
Frequency division ratio	0000 (bin)	1/1 (no frequency division)	Plane brightness correction data setting
Dot correction	11111111 (bin) × 12 (output)	100%	Dot correction data setting
Color tone correction	00000000 (bin) × 4	0%	Color tone correction setting
Gray scale	0000000000 (bin) × 12 (output)	0	Gray scale data setting
CCEN–2 (color tone correction ON/OFF)	000 (bin)	Color tone correction disable	Color tone correction control
FORCE OFF	0	Normal operation	Operation mode setting
FORCE ON	0	Normal operation	Operation mode setting
DCEN	0	Dot correction disable	Operation mode setting
BCEN	0	Brightness control disable	Operation mode setting
LKDEN	0	LKD disable	Operation mode setting
DSGSL	0	Use GCLK terminal	Operation mode setting
OVM comparator voltage	0000 (bin)	0.3 V	Operation mode setting
OVMF, OVMFA, GEF, HEF, TEF	1		HSYNC, fault information reading

initialization

During power up, the device is in an indeterminate condition. To fully reset the device after power up, it is necessary to send an internal reset packet after entering the reset pulse to the XRST terminal or after sending a 0 to each device 256 times as a dummy and then 03h.

Table 1. Input Configuration After Power-Up When Using XRST (reset pulse + 24 bit)

XRST	INTERNAL RESET PACKET		
RESET (NEGATIVE PULSE)	00000000	00000000	00000011

(03000003h)

Note: Both DTIN and STIN should be 0 during XRST 0.

Table 2. Input Configuration After Power-Up When Not Using XRST (256 bit × devices + 24 bit)

DUMMY (bin)	DATA (bin)	INTERNAL RESET PACKET		
0 (256 × devices)	00000011	00000000	00000000	00000011

(00h [256 bits × *n*] + 03000003h)

PRINCIPLES OF OPERATION

gray scale data

Using this packet, the same gray-scale data can be written to all the connected devices simultaneously or different gray-scale data can be written to each device.

The constant-current output is turned on (constant-current flows), except that gray-scale data entered to gray-scale data latch is 0, synchronizing with the next rising edge of the gray-scale clock after the rising edge of the gray-scale clock with the time delay of t_{su} from the edge of DTIN/STIN of HSYNC packet LSB. Thereafter, the 10-bit gray-scale counter counts the number of rising edge of the gray-scale clock and outputs is matched to gray-scale data is turned off (constant-current flow stops).

The user can select either the gray scale clock using GCLK terminal input or the internally generated clock using DTIN/STIN terminal input. (See DSG function section for more detail)

Table 3. Packet Configuration (136-bit)

ID (bin)	CMD (bin)	DATA											
		OUT0	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7	OUT8	OUT9	OUT10	OUT11
xxxxxxxx	00000010	10 bit	10 bit	10 bit	10 bit	10 bit	10 bit	10 bit	10 bit	10 bit	10 bit	10 bit	10 bit

OUT*n*										
dt [9]	dt [8]	dt [7]	dt [6]	dt [5]	dt [4]	dt [3]	dt [2]	dt [1]	dt [0]	GRAY SCALE DATA
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	1
										. . .
1	1	1	1	1	1	1	1	1	0	1023
1	1	1	1	1	1	1	1	1	1	1024

(xx02xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxh) After ID and CMD, 10 bit data continues 12 output

PRINCIPLES OF OPERATION

dot correction data

Using this packet, the same dot correction data can be written to all connected devices simultaneously, or different dot correction data can be written to each device.

The dot correction register latch is configured with 12 output x 8 bit; the current value on each constant output current can be adjusted in 256 steps as 1 step of 0.4% of current ratio between 100% and 0% when output current is set to 100% by adjusting external resistor and brightness adjustment data. By using this function, brightness deviation due to brightness variation of LED can be reduced.

Table 4. Packet Configuration (112-bit)

ID (bin)	CMD (bin)	DATA											
		OUT0	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7	OUT8	OUT9	OUT10	OUT11
xxxxxxxx	00000100	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit

OUT*n*									
dt [7]	dt [6]	dt [5]	dt [4]	dt [3]	dt [2]	dt [1]	dt [0]	RELATIVE CURRENT RATIO (%)	I_{OLC} = 40 mA (mA)
0	0	0	0	0	0	0	0	0.0	0.0
0	0	0	0	0	0	0	1	0.4	0.16
								. . .	. . .
1	1	1	1	1	1	1	0	99.6	39.84
1	1	1	1	1	1	1	1	100	40.00

(xx04xxxxxxxxxxxxxxxxxxxxxxx xh) After ID and CMD, 8 bit data continues 12 output.

color tone correction data

Using this packet, the same color-tone correction data can be written to all the connected devices simultanoeously or different color tone correction data can be written to each device.

Color tone correction makes correction for color deviation by lighting-ON a little the color of the other LED simultaneously when wavelength of LED for each RGB is out of alignment from the color required essentially. The color tone correction function with TLC5930 is configured with color tone correction data packet setting fro current value corrected per pixel assuming OUT0–OUT2, OUT3–OUT5, OUT6–OUT8 and OUT9–OUT11 as four pixels, and with color tone correction control packet which controls ON/OFF by OUT0, OUT3, OUT6, OUT9, and OUT1, OUT4, OUT7, OUT10, and OUT2, OUT5, OUT8, and OUT11 assuming that same color is assigned for OUT0, OUT3, OUT6, OUT9 and OUT1, OUT4, OUT7, OUT10 and OUT2, OUT5, OUT8, and OUT11 respectively.

The current value for color tone correction set by this packet is set per pixel for OUT0–OUT2, OUT3–OUT5, OUT6–OUT8, and OUT9–OUT11. In other words, the current value for color tone correction is same in OUT0–OUT2, OUT3–OUT5, OUT6–OUT8, and OUT9–OUT11.

PRINCIPLES OF OPERATION

The color tone correction register latch is configured with a 4 pixel × 8 bit, and the current value for color tone correction by pixel can be adjusted between 50% and 0% when output current is set to 100% by adjusting external resistor and brightness adjustment data. The color tone correction is divided into the coarse adjustment with 2 bit / 4 steps and the fine adjustment with 6 bit / 64 steps. The current value for the coarse adjustment can be set to 6.25%, 12.5%, 25% or 50% when current is set to 100% by adjusting external resistor and brightness adjustment data. The current value for the fine adjustment can be adjusted in 64 steps as 1 step of 1.6% of current ratio between 100% and 0% when current set at the coarse adjustment is 100%. By using this function, color tone deviation for RGB can be individually corrected.

This packet sets the current value for color tone correction only, thus setting color tone correction control packet to ON/OFF is required for effective color tone correction.

Table 5. Packet Configuration (48-bit)

ID (bin)	CMD (bin)	DATA			
		PIXEL1 (OUT0, OUT1, OUT2)	PIXEL2 (OUT3, OUT4, OUT5)	PIXEL3 (OUT6, OUT7, OUT8)	PIXEL4 (OUT9, OUT10, OUT11)
xxxxxxxx	00001000	8 bit	8 bit	8 bit	8 bit

Pixel *n*									
MSB							LSB		
COARSE ADJ (2 bit)		FINE ADJUSTMENT (6 bit) CURRENT VALUE SET BY COARSE TO 0%							
dt [7]	dt [6]	dt [5]	dt [4]	dt [3]	dt [2]	dt [1]	dt [0]	RELATIVE CURRENT RATIO (%)	I_{OLC} = 40 mA COARSE ADJUSTMENT (3h) (mA)
1	1	0	0	0	0	0	0	0.0	0.0
1	1	0	0	0	0	0	1	1.6	0.3
. . .	. . .							. . .	. . .
1	1	1	1	1	1	1	0	98.4	19.7
1	1	1	1	1	1	1	1	100.0	20.0

		CURRENT VALUE AFTER PLANE BRIGHTNESS ADJUSTMENT (%)
0	0	6.25%
1	1	12.5%
1	0	25.0%
1	1	50.0%

(xx08xxxxxxxxh) After ID and CMD 8 bit data continues 4 set.

PRINCIPLES OF OPERATION

plane brightness adjustment data

Using this packet, the same brightness adjustment data and frequency division data can be written to all connected devices simultaneously, or different brightness adjustment data and frequency division data can be written to each device.

The brightness adjustment data latch is configured with 1 x 16 bit, and the current value on each constant output current can be adjusted in 64 steps as 1 step of 0.94% of current ratio between 100% and 40% when output current is set to 100% by adjusting external resistor. By using this function, brightness adjustment between devices can be accomplished by sending required the data from external even though these are mounted on printed circuit board.

The frequency division ratio register latch is configured with 1 x 4 bit, and the frequency division ratio can be adjusted in 16 steps between 1:1 and 1:16. This function means that brightness can be adjusted in 16 steps only by selecting the frequency division ratio, if gray scale clock is set to 16 times the clock (1024x16=16384) during horizontal scanning time. By using this function, the total panel brightness can be adjusted simultaneously, and applied to the brightness of day or night.

Table 6. Packet Configuration (32 bit)

ID (Bin)	CMD (Bin)	DATA															
						MSB			LSB			MSB					LSB
xxxxxxxx	00010000	RESERVED				FREQUENCY DIVISION DATA				RESERVED		BRIGHTNESS CONTROL DATA					

(xx100xxxh)

FREQUENCY DIVISION RATIO	RELATIVE BRIGHTNESS RATIO (%)	dt [3]	dt [2]	dt [1]	dt [0]
1:1	6.3	0	0	0	0
1:2	12.6	0	0	0	1
. . .	. . .	. . .			
1:15	93.8	1	1	1	0
1:16	100.0	1	1	1	1

RELATIVE CURRENT RATIO (%)	20 (mA)	40 (mA)	dt [5]	dt [4]	dt [3]	dt [2]	dt [1]	dt [0]
40.00	8.00	16.00	0	0	0	0	0	0
40.94	8.18	16.38	0	0	0	0	0	1
. . .	. . .	. . .	. . .					
99.06	19.82	39.62	1	1	1	1	1	0
100.00	20.00	40.00	1	1	1	1	1	1

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PRINCIPLES OF OPERATION

color tone correction control

Using this packet, the same color tone correction control data can be written to all the connected devices simultaneously or different color tone correction control data can be written to each device.

The current value set to OUT0–OUT2, OUT3–OUT5, OUT6–OUT8, and OUT9–OUT11 respectively by color tone correction data packet can be turned on and off per OUT0, OUT3, OUT6, OUT9 and OUT1, OUT4, OUT7, OUT10 and OUT2, OUT5, OUT8, OUT11 by this color tone correction control packet.

The color tone correction control register latch is configured with 1×3 bit, and can be selected from the following status.

1. To correct the LED color connected to OUT0, OUT3, OUT6, OUT9 (ROUT0, ROUT1, ROUT2, ROUT3) using small lighting-ON of LED connected to OUT1, OUT4, OUT7, OUT10 (GOUT0, GOUT1, GOUT2, GOUT3).
2. To correct the LED color connected to OUT0, OUT3, OUT6, OUT9 (ROUT0, ROUT1, ROUT2, ROUT3) using small lighting-ON of LED connected to OUT2, OUT5, OUT8, OUT11 (BOUT0, BOUT1, BOUT2, BOUT3).
3. To correct the LED color connected to OUT1, OUT4, OUT7, OUT10 (GOUT0, GOUT1, GOUT2, GOUT3) using small lighting-ON of LED connected to OUT0, OUT3, OUT6, OUT9 (ROUT0, ROUT1, ROUT2, ROUT3).
4. To correct the LED color connected to OUT1, OUT4, OUT7, OUT10 (GOUT0, GOUT1, GOUT2, GOUT3) using small lighting–ON of LED connected to OUT2, OUT5, OUT8, OUT11 (BOUT0, BOUT1, BOUT2, BOUT3).
5. To correct the LED color connected to OUT2, OUT5, OUT8, OUT11 (BOUT0, BOUT1, BOUT2, BOUT3) using small lighting-ON of LED connected to OUT0, OUT3, OUT6, OUT9 (ROUT0, ROUT1, ROUT2, ROUT3).
6. To correct the LED color connected to OUT2, OUT5, OUT8, OUT11 (BOUT0, BOUT1, BOUT2, BOUT3) using small lighting-ON of LED connected to OUT1, OUT4, OUT7, OUT10 GOUT0, GOUT1, GOUT2, GOUT3).
7. Does not perform color tone correction.

The constant-current output selected by this packet is lighted-ON with the current value set by the color tone data packet as many as gray-scale data set to constant-current output for target corrected in addition to gray scale data and current value set by itself. The current value in this status for lighing-ON equals the sum of the original display and the color tone correction value.

PRINCIPLES OF OPERATION

Table 7. Packet Configuration (24 bit)

ID (Bin)	CMD (Bin)	DATA							
		MSB							LSB
xxxxxxxx	00100000	RESERVED					CCEN2	CCEN1	CCEN0

CONSTANT CURRENT OUTPUT FOR COLOR TONE CORRECTION				
TURN ON	TARGETED			
COLOR TONE CORRECTION OFF		0	0	0
OUT1 (GOUT0)	OUT0 (ROUT0)	0	0	1
OUT4 (GOUT1)	OUT3 (ROUT1)			
OUT7 (GOUT2)	OUT6 (ROUT2)			
OUT10 (GOUT3)	OUT9 (ROUT3)			
OUT2 (BOUT0)	OUT0 (ROUT0)	0	1	0
OUT5 (BOUT1)	OUT3 (ROUT1)			
OUT8 (BOUT2)	OUT6 (ROUT2)			
OUT11 (BOUT3)	OUT9 (ROUT3)			
OUT0 (ROUT0)	OUT1 (GOUT0)	0	1	1
OUT3 (ROUT1)	OUT4 (GOUT1)			
OUT6 (ROUT2)	OUT7 (GOUT2)			
OUT9 (ROUT3)	OUT10 (GOUT3)			
OUT2 (BOUT0)	OUT1 (GOUT0)	1	0	0
OUT5 (BOUT1)	OUT4 (GOUT1)			
OUT8 (BOUT2)	OUT7 (GOUT2)			
OUT11 (BOUT3)	OUT10 (GOUT3)			
OUT0 (ROUT0)	OUT2 (BOUT0)	1	0	1
OUT3 (ROUT1)	OUT5 (BOUT1)			
OUT6 (ROUT2)	OUT8 (BOUT2)			
OUT9 (ROUT3)	OUT11 (BOUT3)			
OUT1 (GOUT0)	OUT2 (BOUT0)	1	1	0
OUT4 (GOUT1)	OUT5 (BOUT1)			
OUT7 (GOUT2)	OUT8 (BOUT2)			
OUT10 (GOUT3)	OUT11 (BOUT3)			
COLOR TONE CORRECTION OFF		1	1	1

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Only one combination is allowed to turn the color tone correction on or off in 1 HSYNC cycle. In other words, when multiple combinations of correction is required, repeated color tone correction with required number of gray scale display at one time is necessary. The following is example when all combinations for color tone correction are needed. Since the current value of the constant-current output for basic display is determined by the brightness adjustment data plus the dot correction data, the current value for color tone correction is determined per pixel by the color tone correction data packet based on the current value excluding the dot correction data after brightness adjustment, although it is different by the constant-current output depending on dot correction data. Accordingly, the current value for color tone correction is shown as follows.

OUT0 (ROUT0) = OUT1 (GOUT0) = OUT2 (BOUT0), OUT3 (ROUT1) = OUT4 (GOUT1) = OUT5 (BOUT1)

OUT6 (ROUT2) = OUT7 (GOUT2) = OUT8 (BOUT2), OUT9 (ROUT3) = OUT10 (GOUT3) = OUT11 (BOUT3)

PRINCIPLES OF OPERATION

The following example shows all the combinations of color tone correction control with 8 gray scale.

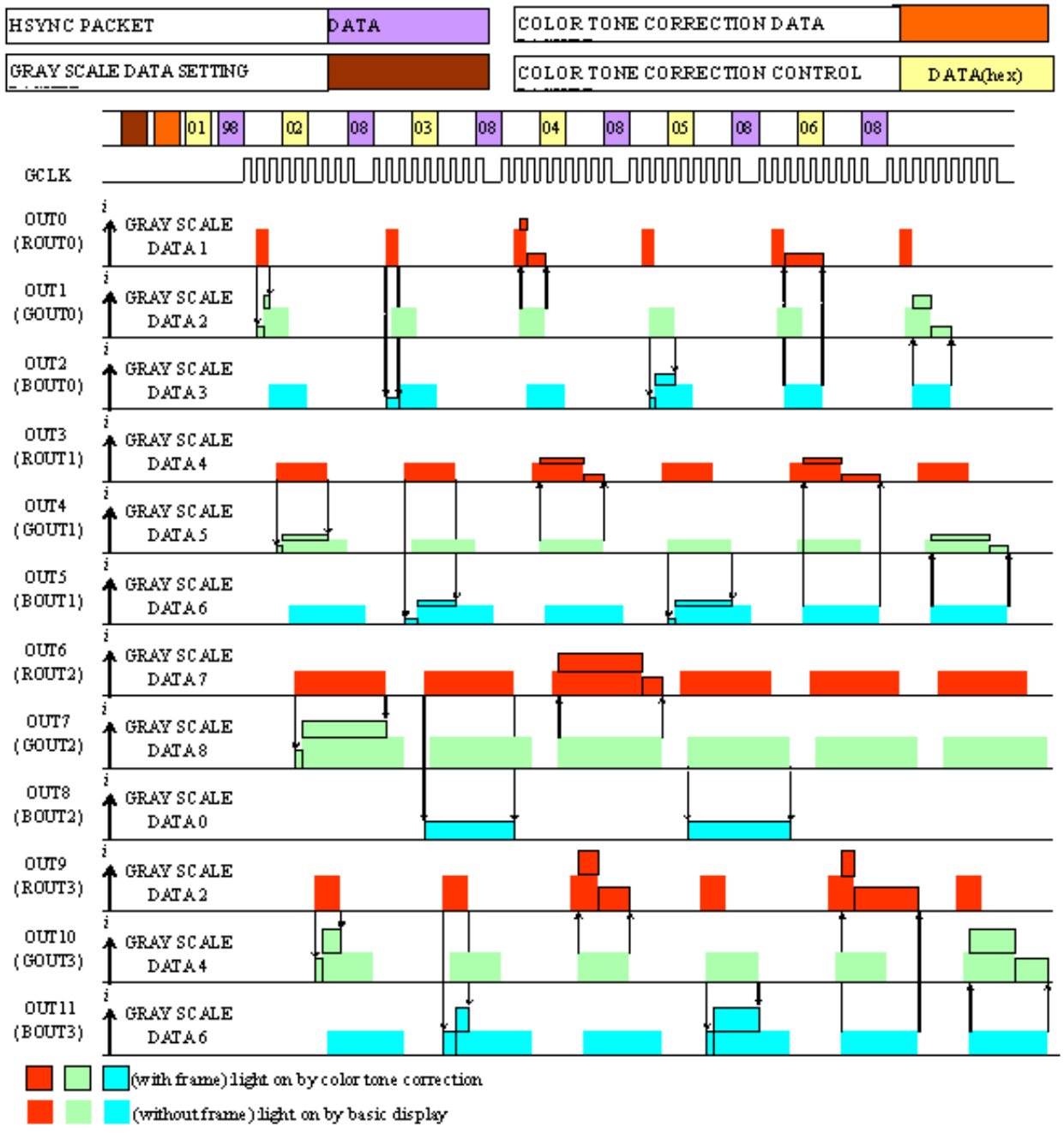

Figure 7. Color Tone Correction Control Combinations With 8–Bit Gray Scale

The timing of lighting-ON for the basic display to be turned on is delayed by $t_{D(OUTn+1–OUTn)}$ until OUT1–OUT11. The lighting-ON for color tone correction is turned on based on ON/OFF timing of output for color tone corrected.

PRINCIPLES OF OPERATION

operation mode setting

Using this packet, the same operation mode can be set to all the connected devices simultanoeously or different operation modes can be set to each device.

Table 8. Packet Configuration (32-bit)

ID (Bin)	CMD (Bin)	DATA														
		MSB														LSB
xxxxxxxx	01000000	RESERVED			DSGSL	LKDEN	DCEN	BCEN	RESERVED	FORCE OFF	FORCE ON	OVM DETECTION VOLTAGE SETTING				

0	0	0	0	0.3 V
0	0	0	1	0.1 V
0	0	1	0	0.2 V
0	0	1	1	0.3 V
0	1	0	0	0.4 V
0	1	0	1	0.5 V
0	1	1	0	0.6 V
0	1	1	1	0.7 V
1	0	0	0	0.8 V
1	0	0	1	0.9 V
1	0	1	0	1.0 V
1	0	1	1	1.1 V
1	1	0	0	1.2 V
1	1	0	1	1/2 VCC
1	1	1	0	2/3 VCC
1	1	1	1	NO UPDATE

0	0	NORMAL OPERATION
0	1	FORCE ALL OUTPUT ON
1	0	FORCE ALL OUTPUT OFF
1	1	INHIBIT

0	SET BRIGHTNESS ADJUSTMENT TO 111111 (100%)
1	COMPLY WITH VALUE SET BY LATCH

0	SET DOT CORRECTION TO 11111111 (100%)
1	COMPLY WITH VALUE SET BY LATCH

0	LKD FUNCTION OFF
1	LKD FUNCTION ON

0	USE INPUT CLOCK TO GCLK AS GRAY SCALE
1	USE INTERNAL CLOCK WITH INPUT CLOCK TO DTIN/STIN

UDG–02037

PRINCIPLES OF OPERATION

This packet allows DSG function, LKD function, dot correction function, brightness adjustment function, flag setting for enable/disable to turn all the output on/off, and data setting for detection voltage set in the OVM function.

DSG function (dual source gray scale clock)

The DSG function selects gray-scale clock from the input clock to GCLK terminal or internally-generated clock using input to the DTIN/STIN terminals. By using the DSGSL flag in this packet, the signal used for the gray scale clock is switched as below from next HSYNC packet. By using this function, the number of signal lines for gray scale clock can be reduced, and display can be continued if DATA/STROBE lines are alive, even though the gray scale clock has stopped due to any failures such as disconnection when using GCLK terminal.

The GEF/HEF function informs of any failures that may occur on the gray scale clock.

DSGSL=0: input clock to GCLK terminal (maximum operating frequency: 20 MHz)

DSGSL=1: internally generated clock using data input to DTIN/STIN terminals (maximum operating frequency: 10 MHz)

LKD function

The LKD function supplies a constant-current of approximately 0.6 μA to the output terminal. When the power supply voltage for the LED is 0 V (GND), writing a 1 to the LKDEN flag allows current flow through LED subtracted leakage current of the device output transistor (below 0.1 μA) from 0.6 μA, and at this time the voltage on output terminal decreases if the reverse leakage current occurs on LED. In this function, since maximum applied voltage is 2.7 V, occurrence of reverse leakage current across LED can be found by reading the OVM detection result through OVM information reading packet by setting the OVM detection voltage to 2/3 VCC. This function should be used in combination with the FORCE OFF function to turn off all the constant-current outputs off. The example for this function is shown in Table 9 below.

Table 9. LKD Function Sequence Example

1	Set LED power supply to 0 V (GND)	
2	Set operation mode setting packet to force ON=0, force OFF = 1 and LKDEN = 1	Set OVM detection voltage and force all outputs OFF and LKD functions ON
3	Wait at least 1 μs	
4	Read OVM result through OVM information reading packet	Demand detection result
5	Set operation mode setting paclet to force ON = 0, force OFF = 0 and LKDEN = 0	LKD function OFF and return to normal operation

DCEN/BCEN

By writing 0 to the flag, the corresponding data (plane brightness data or dot correction data) is set to 100% default value. By writing 1 to the flag, corresponding data is complied with the value set by data setting packet. When both DCEN and BCEN are 0, the current value will be 100% of the value set by R_{IREF}.

The function by flag setting becomes effective from next HSYNC packet after this packet, and in addition, when both BCEN and DCEN flags are 1, the value set by respective data setting packets does not become effective unless BCL and DCL flags in HSYNC packet are set to 1.

Setting both BCEN and DCEN flags to 0, doesn't affect the latch flags in the HSYNC packet. This function writes the default 1 to internal latch and the shift register is not updated. Therefore, unless the value for shift register is updated in respective data setting packet, when plane brightness and dot correction functions are used next, the previous status can be returned by latching the value of shift register into internal latch by setting BCL/DCL flag in HSYNC packet after setting this packet.

PRINCIPLES OF OPERATION

all output force off

By writing 0 to force-ON flag and 1 to force-OFF flag in this packet, all the outputs can be turned off simultaneaously. Also, in this mode, by writing 0 to force-ON flag and 0 to force-OFF flag, it returns to the normal operation.

all output force on

By writing 1 to force-ON flag and 0 to force-OFF flag in this packet, all the output are turned on independent of the gray scale data from next HSYNC packet after this packet. At this time, the current value depends on the plane brightness adjustment data and dot correction data. However, when both DCEN and BCEN are 0, it is 100% of the current value set by R_{IREF}. Also, in this mode, by writing 0 to force-ON flag and 0 to force-OFF flag, it returns to the normal operation after sending the HSYNC packet.

Table 10. All Outputs Forced ON Sequence Example

1	Plane brightness, dot corection data setting packet	Set desired value for output current.
2	Operation mode setting packet: force ON = 1 and force OFF = 0	Demand all output force ON.
3	HSYNC synchronization packet	Al outputs force ON.
4	Operation mode setting packet: force ON = 0 and force OFF = 0	Demand return to normal operation
5	HSYNC synchronization packet	Return to normal operation

Figure 8 shows the operation concept for this mode. All the constant-current outputs are turned on with the current value set independent of the gray-scale data by HSYNC packet after writing 1 to force-ON flag and 0 to force-OFF flag in operation mode setting packet (these are not turned on if the dot correction value is 0). It remains in that state independent of gray scale clock until all output force off mode in the packet is sent or HSYNC packet is sent after writing 0 to force-ON flag and 0 to force-OFF flag in the packet.

PRINCIPLES OF OPERATION

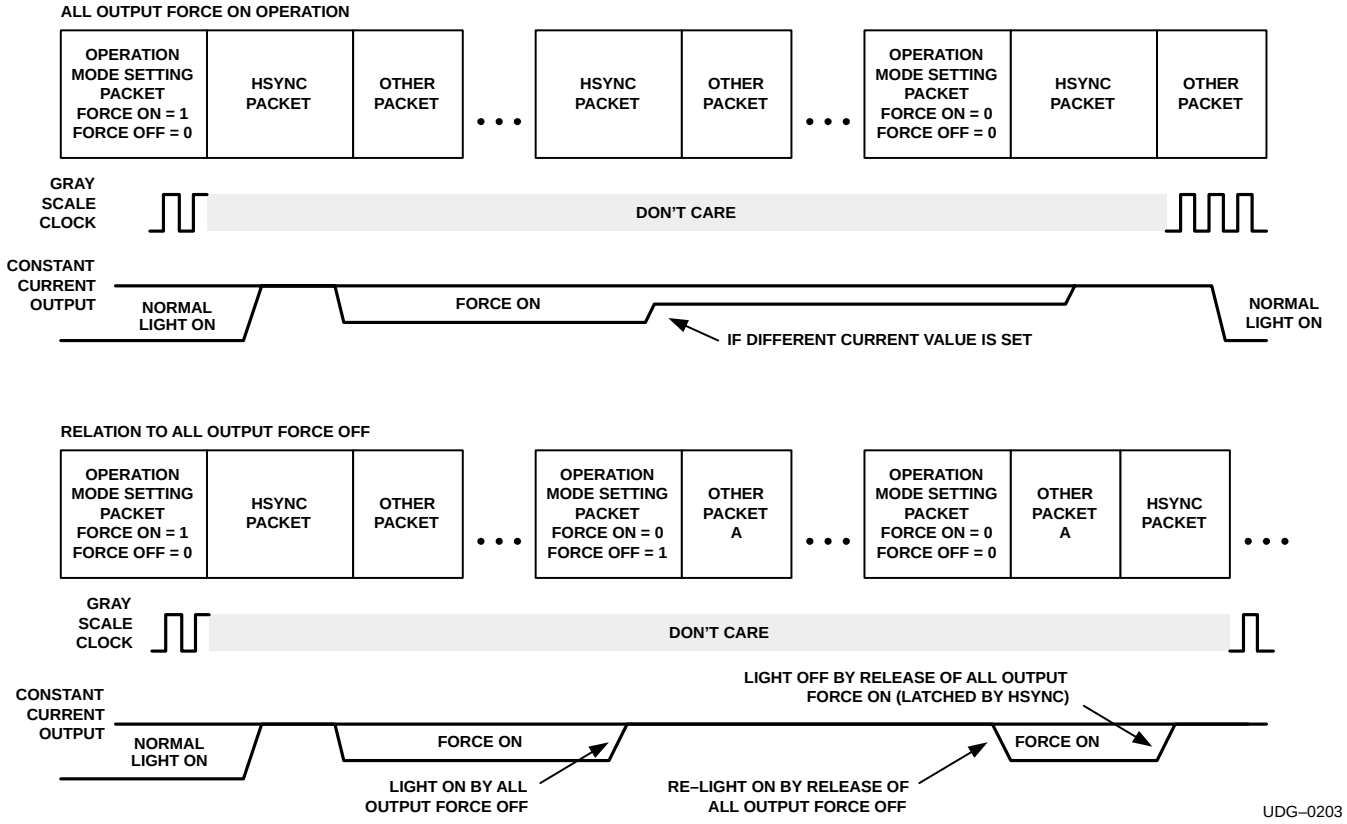

Figure 8. All Output Force ON Operation

Note that, in relation to all output force off shown in Figure 8, when the HSYNC packet is between the other packet and operation mode setting packet with force-ON = 0 / force-OFF = 0, no re-light-ON happens by release of all the output force-OFF.

OVM function

The OVM function is to compare the voltage across the constant-current output terminals (OUT0 to OUT11) with the detection voltage set by this packet, and to output 0 as a comparison result if voltage across terminal is higher than detection voltage and 1 if lower. The TLC5930 has one comparator per output as shown in Figure 9.

The comparison result input ORed with all the output appears in OVMFA of failure monitor information reading, and result per output appears in OVM information reading data OVMF[0:11]. By using this function, where LED disconnection (the voltage across output falls below 0.3 V) or LED short (the voltage across output goes extremely high) has occurred can be detected. Also, the voltage across the constant-current output terminals can be known when it is being turned on by changing the setting value of detection voltage, and heat-up from the device can be minimized by controlling the voltage applied to the anode of the LED to minimize the voltage across constant-current output (approximately 0.4 V at I_O = 40 mA) based on the resulting voltage.

PRINCIPLES OF OPERATION

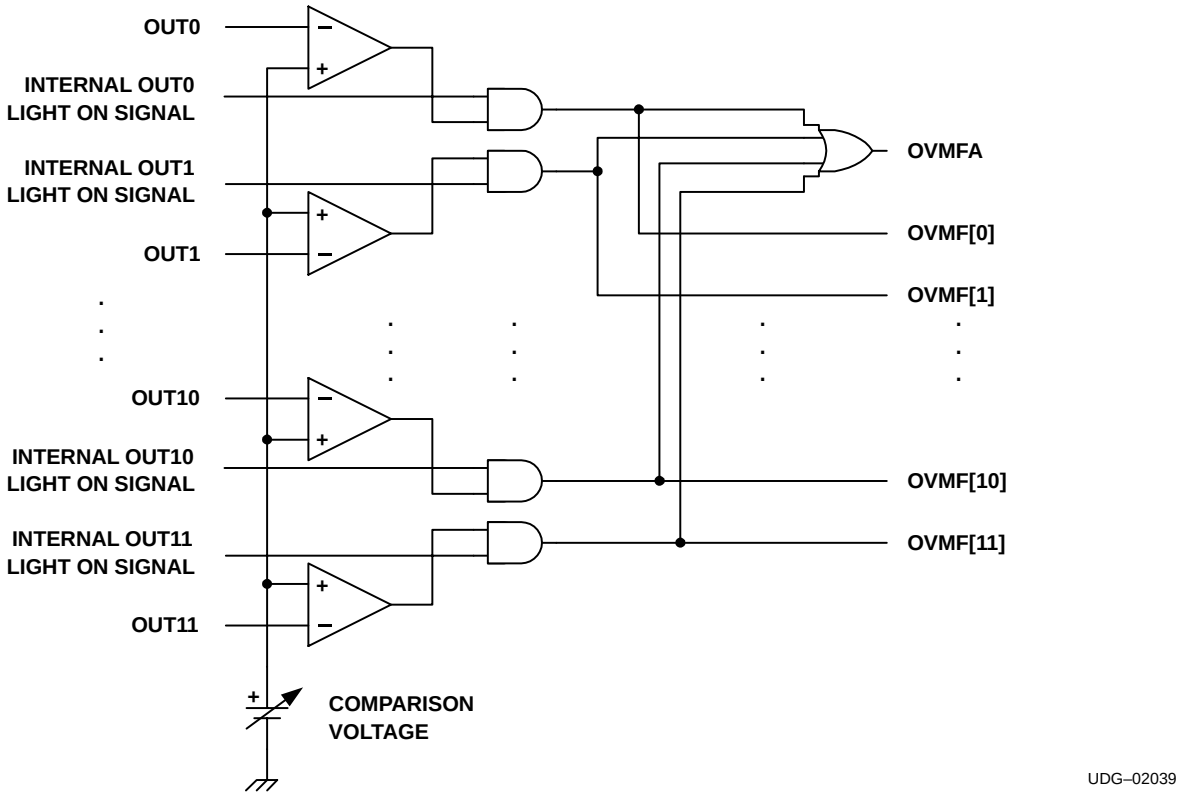

Figure 9. OVM Function

The comparator works so that if a flag is set when read in its operation, voltage across the constant-current output terminals is lower than the comparison voltage. However, the constant-current output is needed to be turned on approximately 1 μs continuously until the comparator starts working. For this reason, the following sequence is recommended to ensure the proper result.

Table 11. OVM Function Sequence Example

1	Gray-scale data, dot correction data setting packet	Set the desired value for output current.
2	Operation mode setting packet: force ON = 1 and force OFF = 0	Set OVM detection voltage and demand all output force ON.
3	HSYNC synchronization packet	Al outputs force ON.
4	Wait at least 1 μs	
5	OVM information reading packet or failure monitor information reading packet	Read OVM comparison result.
6	Operation mode setting packet; force ON = 0 and force OFF = 0	Demand return to normal operation.
7	HSYNC synchronization packet	Return to normal operation

PRINCIPLES OF OPERATION

OVM information read

Using this packet, the comparison results between OVM detection voltage set by operation mode setting packet and the each voltage across constant-current output terminal can be read by the individual constant-current output terminals.

For individual IDs, each flag is information for each constant-current output for each specified device ID. However for common ID devices, the ORed information for constant-current output terminals of devices is connected in series. Data sent from the controller should be 0 as a dummy data except for ID and CMD. If the flag is 1, it is passed through.

Table 12. Packet Configuration (32-bit)

ID (Bin)	CMD (Bin)	DATA																
		MSB																LSB
xxxxxxxx	01010000	RESERVED				OVMF [11]	OVMF [10]	OVMF [9]	OVMF [8]	OVMF [7]	OVMF [6]	OVMF [5]	OVMF [4]	OVMF [3]	OVMF [2]	OVMF [1]	OVMF [0]	

OUT11 RESULT
OUT10 RESULT
OUT9 RESULT
OUT8 RESULT
OUT7 RESULT
OUT6 RESULT
OUT5 RESULT
OUT4 RESULT
OUT3 RESULT
OUT2 RESULT
OUT1 RESULT
OUT0 RESULT

(xx500000h. PACKET SENT FROM CONTROLLER)

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PRINCIPLES OF OPERATION

failure monitor information read

Using this packet, information is ORed when all outputs for OVM detection results, error flags for HEF, GEF, TEF, and AWC flag can be read out. For individual IDs, each flag is information for each device, and for common IDs, the information is ORed for devices connected in series. Although defective devices cannot be detected, problems can be detected only by sending this packet periodically. Data other than AWC sent from controller should be 0 as a dummy except ID and CMD. When the failure monitor information is 0, the input data (except AWC) passes through. OVMFA and TEF are sent when this packet is sent. However, HEF and GEF are sent when the HSYNC packet before this packet has been sent.

Table 13. Packet Configuration (24-bit)

ID (Bin)	CMD (Bin)	DATA							
		MSB							LSB
xxxxxxxx	01100000	RESERVED			OVMFA	HEF	GEF	TEF	AWC

(xx6000h.PACKET SENT FROM CONTROLLER)

UDG–02041

The default value for all the information is 1, so, note that 1 may be read out until normal lighting-ON starts after the reset packet is sent.

OVMFA

The information ORed with detection results for all constant-current output in OVM function appears in this flag. Although defective constant-current output cannot be identified by reading this flag, the OVM function detects output errors.

HEF function (HSYNC Error Flag)

This function is to set 0 to HEF flag if the input number of gray-scale clock per 1 HSYNC cycle is more than 1024, and 1 if less than 1025, at the time when the next HSYNC packet is sent. For example, when, despite the normal gray-scale clock, the sending period of the HSYNC packet is shortened for any reason and the number of gray-scale clock in 1 HSYNC cycle is less than 1025, that is, when the HSYNC packet is entered with the number of gray-scale clock than 1025, HEF is set to 1. In other words, by using this function, one can know failure in the HSYNC cycle. This function is assumed to use the TLC5930 for 1024 gray scale, and if use it less than 1025 such as 256 gray scale, this flag should be neglected even though it is always set to 1.

Regarding the number of the gray-scale clock needed for lighting-ON, a gray-scale clock total of 1025, equivalent to 1024 plus 1, is needed to complete lighting on with 1024 gray-scale clock, since lighting on starts with second rising edge of gray-scale clock after LSB input of the HSYNC packet.

GEF function (GCLK Error Flag)

This function is to set 0 to GEF flag if the number of gray-scale clock meet the requied number of gray-scale per 1 HSYNC cycle, and 1 if not, at the time when the next HSYNC packet is sent. For example, when the gray-scale data for given constant-current output is 100, and the gray-scale clock is entered between 2 and 100 for each HSYNC cycle, the correcponding constant-current output remains in an on–state until the next HSYNC packet is sent. When the clock is less than 2, the output is not turned on. In this case, if lighting-ON for the number of gray-scale clock is not done, GEF is set to 1 assumed as failure. In other words, by using this function, one can know whether the gray scale clock is normally sent or 1 HSYNC cycle meet the lighting-ON time desired.

Notes that this flag is set to 1 independent of the status of the gray-scale clock during one HSYNC cycle after all outputs are forced on.

PRINCIPLES OF OPERATION

failure monitor information read (continued)

TEF function (thermal error flag)

This function, is used to determine when the junction temperature of the device exceeds its limit. This function sets 0 to the TEF flag if the junction temperature is less than 160°C, and set it to 1 if the temperature is greater than 160°C.

AWC function (active wire check)

This function is used to check that the communication between controller and driver is performing normally. The TLC5930 clocks out the inverted data from written data into bits when this packet is entered. For individual IDs, the inverted data from the controller output returns to the controller. For common IDs, the same data as the controller output returns to the controller if the number of devices connected in series is even, but returns to the inverted data if it is odd.

read information output

For failure monitor information reading (including OVM information reading, failure monitor information flags in the HSYNC packet), for individual IDs or common IDs, it is set to 1 if an error is indicated. Input data is passed through if there is no error detected. For AWC, for both individual and common IDs, the inverted data from input data is clocked out. When the ID is neither common nor matched, the data including AWC is passed through.

Table 16 shows four connected device. Bold bits indicates the reading information output from the device.

Table 14. Read Information Output

DEVICE NUMBER	CONDITION	ID NO.	DATA BIT 111111111122222222223333 .12345678901234567890123456789012 3
IC1 INPUT (CONTROLLER OUTPUT)		COMMON	x000000000110000000000000xxxxxxxxx
IC1 OUTPUT (IC2 INPUT)	IC1: OVM fail		xxx000000000110000000010001xxxxxxx
IC2OUTPUT (IC3 INPUT)	IC2: ALL PASS		xxxxx000000000110000000010000xxxxx
IC3 OUTPUT (IC4 INPUT)	IC3: HEF, GEF fail		xxxxxxx000000000110000000011101xxx
IC4 OUTPUT (CONTROLLER INPUT)	IC4: ALL PASS		xxxxxxxxx000000000110000000011100x

DEVICE NUMBER	ID NO.	DATA BIT 111111111122222222223333 .12345678901234567890123456789012 3	ID NO.	DATA BIT 111111111122222222223333 .12345678901234567890123456789012 3
IC1 INPUT	1	x000000010110000000000000xxxxxxxxx	2	x000000100110000000000000xxxxxxxxx
IC1 OUTPUT		xxx000000010110000000010001xxxxxxx		xxx000000100110000000000000xxxxxxx
IC2 OUTPUT		xxxxx000000010110000000010001xxxxx		xxxxx000000100110000000000001xxxxx
IC3 OUTPUT		xxxxxxx000000010110000000010001xxx		xxxxxxx000000100110000000000001xxx
IC4 OUTPUT		xxxxxxxxx000000010110000000010001x		xxxxxxxxx000000100110000000000001x

DEVICE NUMBER	ID NO.	DATA BIT 111111111122222222223333 .12345678901234567890123456789012 3	ID NO.	DATA BIT 111111111122222222223333 .12345678901234567890123456789012 3
IC1 INPUT	3	x000000110110000000000000xxxxxxxxx	4	x000001000110000000000000xxxxxxxxx
IC1 OUTPUT		xxx000000110110000000000000xxxxxxx		xxx000001000110000000000000xxxxxxx
IC2 OUTPUT		xxxxx000000110110000000000000xxxxx		xxxxx000001000110000000000000xxxxx
IC3 OUTPUT		xxxxxxx000000110110000000011101xxx		xxxxxxx000001000110000000000000xxx
IC4 OUTPUT		xxxxxxxxx000000110110000000001101x		xxxxxxxxx000001000110000000000001x

PRINCIPLES OF OPERATION

automatic ID setting

The device that receives this packet stops DTOUT and STOUT for 8 bits (ID portion in below packet configuration) after CMD, and recognizes the 8 bits as its own ID. Next, 8 bits data with recognized ID plus 1 bit is clocked out, and dummy data sent is passed through until 03h data is entered. When the device receives 03h data, it recognizes the ID setting completion and is ready to receive the next command. During reception of the next 8 bits each device receives, DATA/STROBE output is inhibited, so the controller must send dummy data (0) with bit counts of at least minimum device number times 8 bit after ID/CMD/DATA(ID) until this packet operation is completed including DTOUT/STOUT output.

Table 15. Packet Configuration (32-bit + 8-bit (IC–1))

ID (Bin)	CMD (Bin)	DATA (BIN)		
		ID	DUMMY	END
00000000	01110000	xxxxxxxx	00000000 × IC NUMBER	00000011

(0070xxh + 00h × IC NUMBER + 03h)

UDG–02043

The following is a sequence example for automatic ID setting (in the case of one device and four devices). In this example, IC1 input indicates output from the controller, while the last device output indicates the input for the controller. Since the blank portion in the example does not recognize the input in DS-LINK, input to controller is continuous ID/CMD/DATA(DATA=number of devices + 1). There are two different methods to send DATA(END) 03h;

- Calculate and send the number of dummy data as the number of devices times 8 bits.
- Stop the dummy data output synchronizing with receiving the ID/CMD/DATA(DATA=number of devices + 1) at the controller input and send DATA 03h.

The latter case is useful when the number of connected devices is unknown (for automatic recognition). The number of devices connected that can be known from that DATA(ID) received by the controller shows the number of devices plus 1. In any case, dummy data should be an 8-bit base.

Table 16. One IC (No Dummy Data)

IC NUMBER DATA BIT	1111111111222222222233333333334444 .....12345678901234567890123456789012345678901234567890123.....
IC1 INPUT	xxxxx00000000011100000000000100000011000000011xxxxx
IC1 OUTPUT	xxxxxxx0000000001110000 0000001000000011xxx

Table 17. Four ICs (24-bit Dummy Data)

IC NUMBER DATA BIT	11111111112222222222333333333344444444455555555556666666667 .....12345678901234567890123456789012345678901234567890123456789012345678901..
IC1 INPUT	xxxxx00000000011100000000000100000000000000000000000000000000000011xxxxxxxxx
IC1 OUTPUT (IC2 INPUT)	xxxxxxx0000000001110000 00000010000000000000000000000000000011xxxxxxx
IC2 OUTPUT (IC3 INPUT)	xxxxxxxxx00000000011100 00 00000011000000000000000000000011xxxxx
IC3 OUTPUT (IC4 INPUT)	xxxxxxxxxxx000000000111 00 00 000001000000000000000011xxx
IC4 OUTPUT	xxxxxxxxxxxxx0000000001 11 00 00 0000010100000011x

PRINCIPLES OF OPERATION

HSYNC synchronization

The constant-current output is turned on, synchronizing with this packet. In addition, for common IDs, the failure monitor information flag is read out through the 5 LSB of DATA within the packet (see *failure monitor information read* section), and data written in the internal register within gray scale data setting packet, plane brightness adjustment data setting packet, dot correction data setting packet, color tone correction setting packet, and color tone correction control setting packet are latched, depending on the status of the register latch flag of 5 MSB of DATA. Since each flag in the register latch flag is independent, writing a 1 allows the respective packet data to be latched. Writing a 0 to the flag allows no latch. By using this function, gray scale data, plane brightness adjustemnt data , dot correction data, color–tone correction, and correction control setting packets can be sent asynchronously with the HSYNC cycle.

Note that no lighting-ON occurs when the gray-scale clock is entered before this HSYNC packet of normal lighting-ON operation (including use of internally generated clock) during the first normal lighting-ON operation (PWM operation) after power up. Normal operation occurs after the second operation.

Table 18. Packet Configuration (32-bit)

ID (Bin)	CMD (Bin)	REGISTER LATCH FLAG					DATA						FAILURE MONITOR FLAG				
		MSB															LSB
00000000	10000000	GSL	BCL	DCL	CCL	CSL	RESERVED						OVMFA	HEF	GEF	TEF	AWC
													REFER FAILURE MONITOR READ				
						1	LATCH COLOR TONE CORRECTION CONTROL DATA										
					1		LATCH COLOR TONE CORRECTION DATA										
				1			LATCH DOT CORRECTION DATA										
			1				LATCH PLANE BRIGHTNESS ADJUSTMENT DATA										
		1					LATCH GRAY SCALE DATA										
		0	0	0	0	0	NO LATCH										

(0080xxh.PACKET SENT FORM CONTROLLER)

UDG–02044

Table 21 shows the relationship between failure monitor information reading packet, HSYNC packet, and other various error flags.

Table 19. Error Flag Relationships

TIME												
	FAIL	FAILURE PACKET	HSYNC PACKET	FAIL	FAILURE PACKET	HSYNC PACKET	FAIL	HSYNC PACKET	FAILURE PACKET	FAIL	HSYNC PACKET	FAILURE PACKET
OVMFA	OCCUR	1	1	RELEASE	0	0	OCCUR	1	1	RELEASE	0	0
HEF		0	1		1	0		1	1		0	0
GEF		0	1		1	0		1	1		0	0
TEF		1	1		0	0		1	1		0	0

PRINCIPLES OF OPERATION

calculating constant-current output

The current value of constant-current output can be calculated using the following expression.

$$I_{OLC\,(n)} = 42\left(I_{DC\,(n)} + I_{CC\,(n)}\right) \quad (2)$$

Where I_{DC} is main current (except color tone correction), I_{CC} is color tone correction current. Both currents are referenced with reference current, $I_{(IREF)}$, and $I_{(DC)}$ is established by dot correction data and gray scale data. I_{CC} from color tone correction data and color tone correction control data. *n* is output terminal number, 0 to 11.

reference current

The reference current I_{IREF} can be calculated with external resistor, R_{IREF}, voltage reference, V_{IREF}, and plane brightness data, r_{BC}, using the following expression.

$$I_{IREF} = 4\left(\frac{V'_{IREF}}{R_{IREF}}\right) \quad (3)$$

$$V'_{IREF} = \left[0.4 + \left(\frac{0.6\left(r_{BC} + 1\right)}{64}\right)\right] \times V_{IREF} \quad (4)$$

main current

The main current, I_{DC}, can be calculated with dot correction data, r_{DC}, logic signal, S_{MAIN}, established by gray scale data, and reference current, I_{IREF}, using the following expression.

$$I_{DC\,(n)} = \frac{\left(r_{DC\,(n)}\right)}{256} \times S_{MAIN\,(n)} \times I_{IREF} \quad (5)$$

Where S_{MAIN}, is set to following value depending on gray scale data, r_{GC}.

$$S_{MAIN\,(n)} = \begin{cases} 1: r_{GC\,(n)} > 0 \\ 0: r_{GC\,(n)} = 0 \end{cases}$$

PRINCIPLES OF OPERATION

color tone correction current

The color tone correction current, I_{CC}, can be calculated with I'_{CC} established by color tone correction data, and logic signal, S_{CC}, for color tone correction current switch established by the combination of color tone correction control data with logic signal for main current switch, using the following expression.

I'_{CC} is expressed depending on color tone correction data r_{CC1} through r_{CC4} as follows.

$$I'_{CC(0)} = I'_{CC(1)} = I'_{CC(2)} = \frac{1}{2\left(4 - r_{CC1[7:6]}\right)} \times \frac{r_{CC1[5:0]}}{64} \times I_{IREF} \quad (6)$$

$$I'_{CC(3)} = I'_{CC(4)} = I'_{CC(5)} = \frac{1}{2\left(4 - r_{CC2[7:6]}\right)} \times \frac{r_{CC2[5:0]}}{64} \times I_{IREF} \quad (7)$$

$$I'_{CC(6)} = I'_{CC(7)} = I'_{CC(8)} = \frac{1}{2\left(4 - r_{CC3[7:6]}\right)} \times \frac{r_{CC3[5:0]}}{64} \times I_{IREF} \quad (8)$$

$$I'_{CC(9)} = I'_{CC(10)} = I'_{CC(11)} = \frac{1}{2\left(4 - r_{CC4[7:6]}\right)} \times \frac{r_{CC4[5:0]}}{64} \times I_{IREF} \quad (9)$$

S_{CC} is set up by color tone correction control switch, S_{CCEN}, established by color tone correction control data r_{CCEN} and S_{MAIN}. S_{CCEN} is expressed as follows:

$$S_{CCEN1} = \begin{cases} 1: r_{CCEN} = 0\ 0\ 1 \text{ (bin)} \\ 0: \text{except the above} \end{cases}$$

$$S_{CCEN2} = \begin{cases} 1: r_{CCEN} = 0\ 1\ 0 \text{ (bin)} \\ 0: \text{except the above} \end{cases}$$

$$S_{CCEN3} = \begin{cases} 1: r_{CCEN} = 0\ 1\ 1 \text{ (bin)} \\ 0: \text{except the above} \end{cases}$$

$$S_{CCEN4} = \begin{cases} 1: r_{CCEN} = 1\ 0\ 0 \text{ (bin)} \\ 0: \text{except the above} \end{cases}$$

$$S_{CCEN5} = \begin{cases} 1: r_{CCEN} = 1\ 0\ 1 \text{ (bin)} \\ 0: \text{except the above} \end{cases}$$

$$S_{CCEN6} = \begin{cases} 1: r_{CCEN} = 1\ 1\ 0 \text{ (bin)} \\ 0: \text{except the above} \end{cases}$$

PRINCIPLES OF OPERATION

$$S_{CC[0]} = \begin{cases} 1: (S_{CCEN3} \text{ and } S_{MAIN[1]}) \text{ or } (S_{CCEN5} \text{ and } S_{MAIN[2]}) = \text{TRUE} \\ 0: \text{except the above} \end{cases}$$

$$S_{CC[1]} = \begin{cases} 1: (S_{CCEN1} \text{ and } S_{MAIN[0]}) \text{ or } (S_{CCEN6} \text{ and } S_{MAIN[2]}) = \text{TRUE} \\ 0: \text{except the above} \end{cases}$$

$$S_{CC[2]} = \begin{cases} 1: (S_{CCEN2} \text{ and } S_{MAIN[0]}) \text{ or } (S_{CCEN4} \text{ and } S_{MAIN[1]}) = \text{TRUE} \\ 0: \text{except the above} \end{cases}$$

$$S_{CC[3]} = \begin{cases} 1: (S_{CCEN3} \text{ and } S_{MAIN[4]}) \text{ or } (S_{CCEN5} \text{ and } S_{MAIN[5]}) = \text{TRUE} \\ 0: \text{except the above} \end{cases}$$

$$S_{CC[4]} = \begin{cases} 1: (S_{CCEN1} \text{ and } S_{MAIN[3]}) \text{ or } (S_{CCEN6} \text{ and } S_{MAIN[5]}) = \text{TRUE} \\ 0: \text{except the above} \end{cases}$$

$$S_{CC[5]} = \begin{cases} 1: (S_{CCEN2} \text{ and } S_{MAIN[3]}) \text{ or } (S_{CCEN4} \text{ and } S_{MAIN[4]}) = \text{TRUE} \\ 0: \text{except the above} \end{cases}$$

$$S_{CC[6]} = \begin{cases} 1: (S_{CCEN3} \text{ and } S_{MAIN[7]}) \text{ or } (S_{CCEN5} \text{ and } S_{MAIN[8]}) = \text{TRUE} \\ 0: \text{except the above} \end{cases}$$

$$S_{CC[7]} = \begin{cases} 1: (S_{CCEN1} \text{ and } S_{MAIN[6]}) \text{ or } (S_{CCEN6} \text{ and } S_{MAIN[8]}) = \text{TRUE} \\ 0: \text{except the above} \end{cases}$$

$$S_{CC[8]} = \begin{cases} 1: (S_{CCEN2} \text{ and } S_{MAIN[6]}) \text{ or } (S_{CCEN4} \text{ and } S_{MAIN[7]}) = \text{TRUE} \\ 0: \text{except the above} \end{cases}$$

$$S_{CC[9]} = \begin{cases} 1: (S_{CCEN3} \text{ and } S_{MAIN[10]}) \text{ or } (S_{CCEN5} \text{ and } S_{MAIN[11]}) = \text{TRUE} \\ 0: \text{except the above} \end{cases}$$

$$S_{CC[10]} = \begin{cases} 1: (S_{CCEN1} \text{ and } S_{MAIN[9]}) \text{ or } (S_{CCEN6} \text{ and } S_{MAIN[11]}) = \text{TRUE} \\ 0: \text{except the above} \end{cases}$$

$$S_{CC[11]} = \begin{cases} 1: (S_{CCEN2} \text{ and } S_{MAIN[9]}) \text{ or } (S_{CCEN4} \text{ and } S_{MAIN[10]}) = \text{TRUE} \\ 0: \text{except the above} \end{cases}$$

PRINCIPLES OF OPERATION

Table 20. Register Term Summary

DATA	FUNCTION
r_{BC}	Plane brightness adjustment data set by plane brightness adjustment data setting packet
r_{DC}	Dot correction data set by dot correction data setting packet
r_{GC}	Gray scale data set by gray scale data setting packet
r_{CC1}	Color tone correction data for pixel 1 set by color tone correction data setting packet
r_{CC2}	Color tone correction data for pixel 2 set by color tone correction data setting packet
r_{CC3}	Color tone correction data for pixel 3 set by color tone correction data setting packet
r_{CC4}	Color tone correction data for pixel 4 set by color tone correction data setting packet
r_{CCEN}	Color tone correction control flag set by color tone correction control setting packet

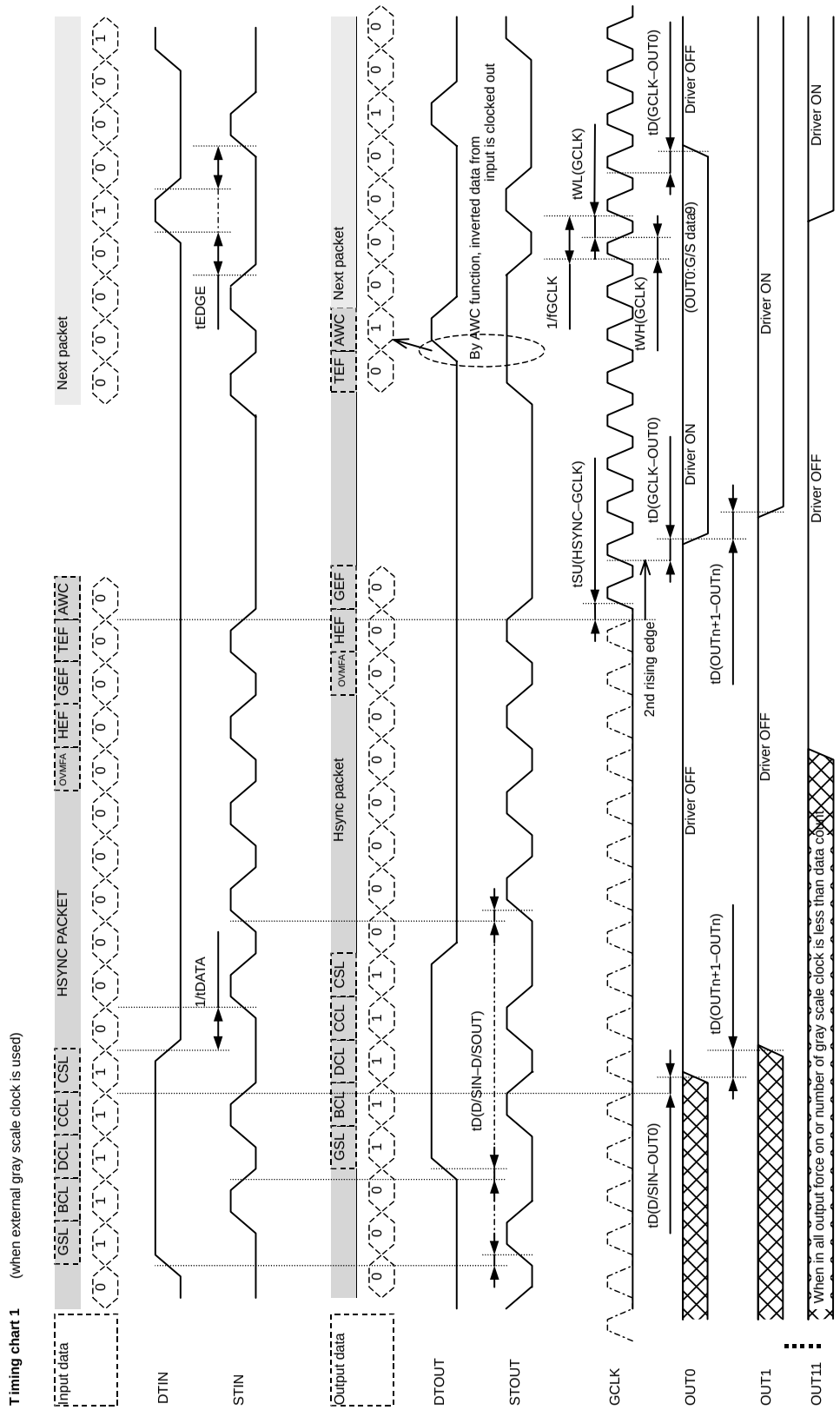


Figure 10. Timing Diagrams (External Gray-Scale CLock)

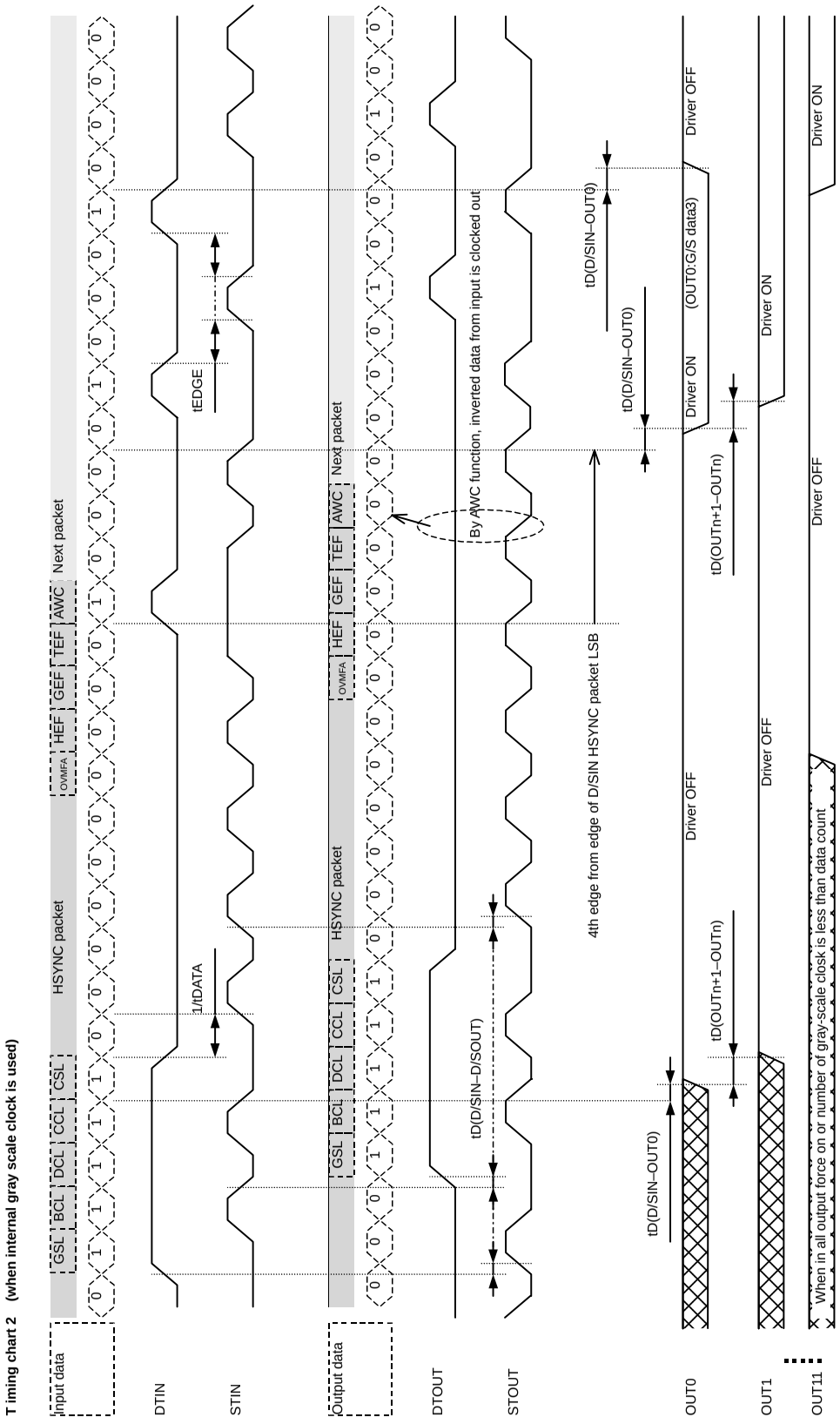
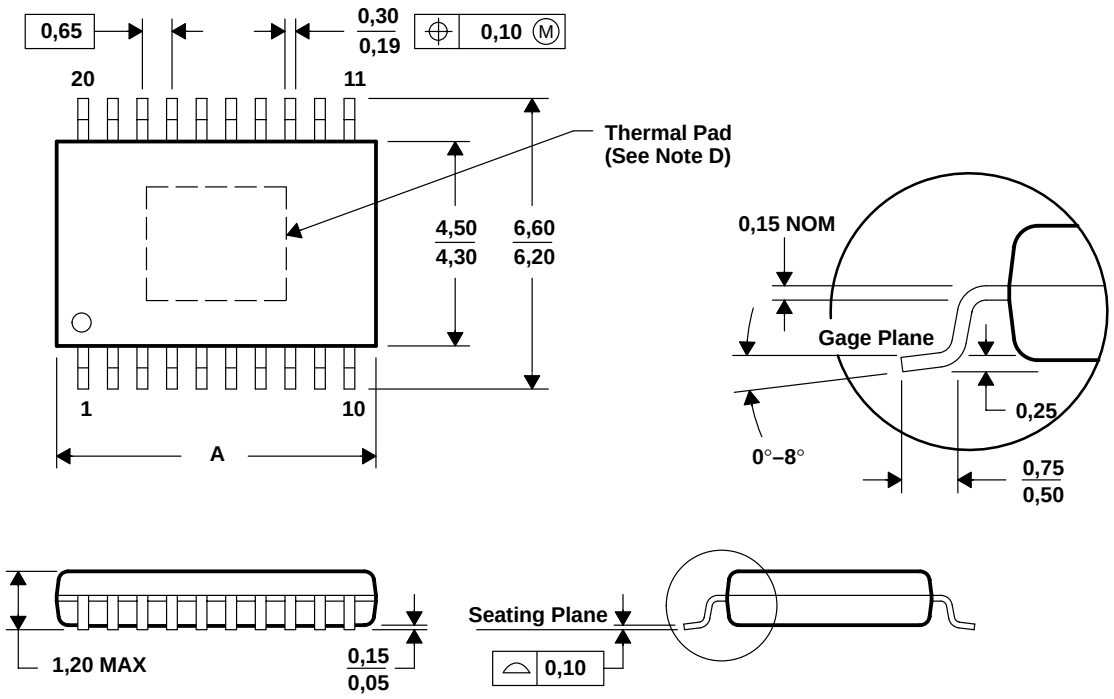


Figure 11. Timing Diagrams (Internal Gray-Scale Clock)

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC5930PWP	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	P5930
TLC5930PWP.B	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	P5930
TLC5930PWPG4	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	P5930
TLC5930PWPG4.B	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 85	P5930

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

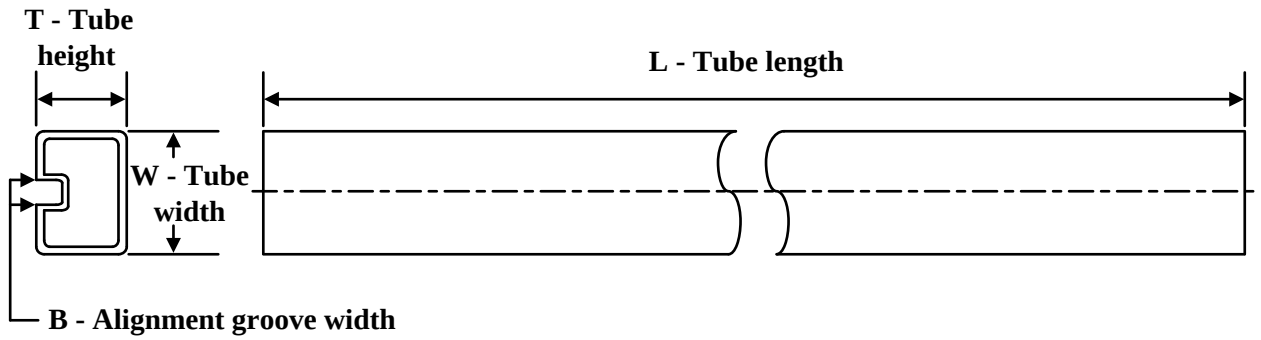
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC5930PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TLC5930PWP.B	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TLC5930PWPG4	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TLC5930PWPG4.B	PWP	HTSSOP	24	60	530	10.2	3600	3.5

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