TLE202x-Q1 Automotive, High-Speed, Low-Power, Bipolar Precision Operational Amplifiers

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature: –40°C to +125°C, T_A
- ESD Protection Exceeds 1000V Per MIL-STD-883, Method 3015
- Supply current: 300µA (maximum)
- High unity-gain bandwidth: 2MHz (typical)
- High slew rate: 0.45V/µs (minimum)
- Minimal supply-current change over full temperature range
- Specified for 5V single-supply and ±15V operation
- Phase-reversal protection
- High open-loop gain: 6.5V/µV (136dB) (typical)
- Low offset voltage: 100µV (maximum)
- Low input bias current: 50nA (maximum)
- Low noise voltage: 19nV/$\sqrt{\text{Hz}}$ (typical)

2 Applications

- Automotive lighting
- Body electronics
- Automotive head unit
- Inverter and motor control
- On-board (OBC) and DC/DC converter
- Battery management system (BMS)

3 Description

The TLE2021-Q1, TLE2022-Q1, TLE2024-Q1 and TLE2021A-Q1, TLE2022A-Q1 devices (all referred to in this data sheet as TLE202x-Q1) are precision, high-speed, low-power operational amplifiers using a new Texas Instruments bipolar process. The A-suffix devices offer improved dc specifications over the non-A-suffix devices, such as input offset voltage. These devices combine the best features of the OP21 with highly improved slew rate and unity-gain bandwidth.

The addition of a bias circuit in conjunction with this process results in extremely stable parameters with both time and temperature. Therefore, a precision device remains a precision device even with changes in temperature and over years of use.

This combination of excellent dc performance with a common-mode input voltage that includes the negative rail makes these devices an excellent choice for low-level signal conditioning applications in either single-supply or split-supply configurations. In addition, these devices offer phase-reversal protection circuitry that eliminates an unexpected change in output states when one of the inputs is less than the negative supply rail.

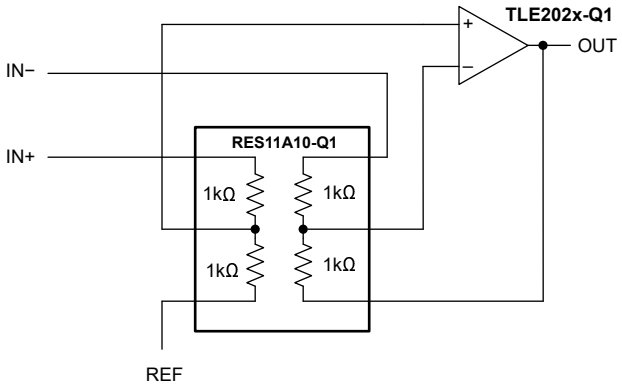
A variety of available options includes small-outline versions for high-density systems applications.

These devices are characterized for operation over the full automotive temperature range of −40°C to +125°C.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
TLE2021-Q1	Single	D (SOIC, 8)
TLE2021A-Q1		
TLE2022-Q1	Dual	D (SOIC, 8)
TLE2022A-Q1		
TLE2024-Q1	Quad	DW (SOIC, 16)

(1) For more information, see Section 9.



Difference Amplifier Application With the RES11A-Q1

Table of Contents

4 Pin Configuration and Functions

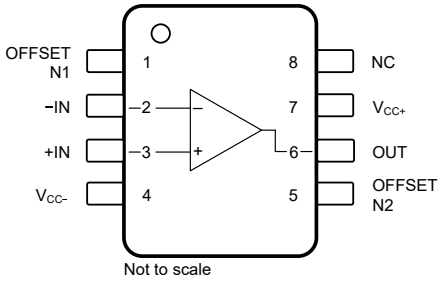


Figure 4-1. TLE2021-Q1: D Package, 8-Pin SOIC, (Top View)

Table 4-1. Pin Functions: TLE2021-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN	2	Input	Inverting input
+IN	3	Input	Noninverting input
NC	8	—	No connection. Float this pin.
OFFSET N1	1	_	External input offset voltage adjustment
OFFSET N2	2	_	External input offset voltage adjustment
OUT	6	Output	Output
V–	4	Power	Negative (lowest) power supply
V+	7	Power	Positive (highest) power supply

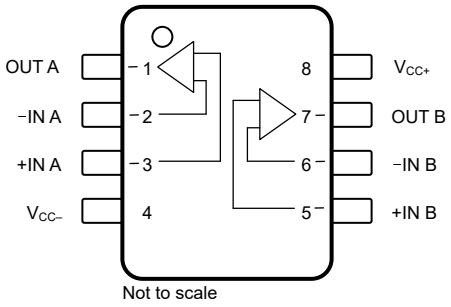


Figure 4-2. TLE2022-Q1: D Package, 8-Pin SOIC (Top View)

Table 4-2. Pin Functions: TLE2022-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
–IN B	6	Input	Inverting input channel B
+IN A	3	Input	Noninverting input channel A
+IN B	5	Input	Noninverting input channel B
NC	—	—	No connection. Float this pin.
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
V–	4	Power	Negative supply
V+	8	Power	Positive supply

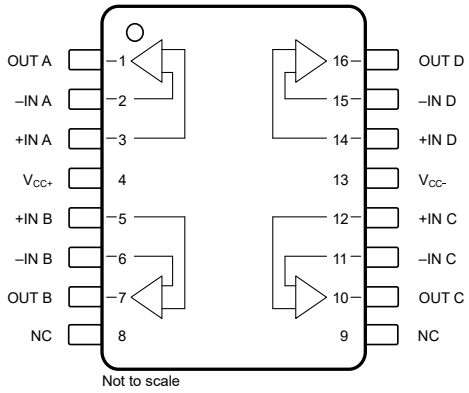


Figure 4-3. TLE2024-Q1: DW Package, 16-Pin SOIC (Top View)

Table 4-3. Pin Functions: TLE2024-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
–IN B	6	Input	Inverting input channel B
–IN C	11	Input	Inverting input channel C
–IN D	15	Input	Inverting input channel D
+IN A	3	Input	Noninverting input channel A
+IN B	5	Input	Noninverting input channel B
+IN C	12	Input	Noninverting input channel C
+IN D	14	Input	Noninverting input channel D
NC	8, 9	—	No internal connection. Float this pin.
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
OUT C	10	Output	Output channel C
OUT D	16	Output	Output channel D
V–	13	Power	Negative supply
V+	4	Power	Positive supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage $V_{CC} = (V_{CC+}) - (V_{CC-})$	Positive, V_{CC+} (2)		20	V
		Negative, V_{CC-} (2)	–20		
V_{ID}	Differential input voltage(3)			±0.6	V
V_I	Input voltage range (any input)		V_{CC-}	V_{CC+}	V
I_I	Input current (each input)			±1	mA
I_O	Output current	TLE2021-Q1		±20	mA
		TLE2022-Q1		±30	
		TLE2024-Q1		±40	
	Total power supply current	Into V_{CC+}		80	mA
		Out of V_{CC-}		80	
	Duration of short-circuit current at (or below) 25°C(4)		Unlimited		
T_J	Junction temperature(5)			150	°C
T_{stg}	Storage temperature		–65	150	°C
	Lead temperature 1.6mm (1/16 inch) from case for 3 seconds: D or PW package			300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at +IN with respect to −IN. Excessive current flows if a differential input voltage in excess of approximately ±600mV is applied between the inputs unless some limiting resistance is used.
(4) Do not short output to V+. Limit temperature, supply voltage, or both to not exceed the maximum dissipation rating.
(5) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage $V_{CC} = (V_{CC+}) - (V_{CC-})$	Dual Supply	±2		±20	V
		Single Supply	4		40	
V_{IC}	Common-mode input voltage	V_{CC+} = 5V	0		3.2	V
		V_{CC+} = 15V, V_{CC-} = –15V	–15		13.2	
T_A	Operating free-air temperature		–40		125	°C

5.3 Thermal Information for TLE2021-Q1

THERMAL METRIC[1]		TLE2021-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	68.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.4 Thermal Information for TLE2022-Q1

THERMAL METRIC[1]		TLE2022-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	61.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information for TLE2024-Q1

THERMAL METRIC[1]		TLE2024-Q1 DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	28.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics for TLE2021-Q1, V_{CC} = ±15V

at T_A = 25°C, V_{CC} = ±15V, and V_{IC} = V_{OUT} = V_{CC} / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V_{IO}	Input offset voltage	TLE2021-Q1 R_S = 50Ω			±120	±500	µV
			T_A = –40°C to +125°C			±700	
		TLE2021A-Q1 R_S = 50Ω			±80	±300	
			T_A = –40°C to +125°C			±450	
dV_{IO}/dT	Input offset voltage drift	R_S = 50Ω, T_A = –40°C to +125°C			±2		µV/°C
I_{IB}	Input bias current	R_S = 50Ω			25	70	nA
			T_A = –40°C to +125°C			90	
I_{IO}	Input offset current	R_S = 50Ω			0.2	6	nA
			T_A = –40°C to +125°C			10	
PSRR	Power-supply rejection ratio	$V_{CC±}$ = ±2.5V to ±15V		105	120		dB
			T_A = –40°C to +125°C	100			
A_{VD}	Large signal voltage gain	V_O = ±10V, R_L = 10kΩ		1	6.5		V/µV
			T_A = –40°C to +125°C	0.5			
V_{ICR}	Common-mode input voltage range	To positive rail R_S = 50Ω		13.5	14		V
			T_A = –40°C to +125°C	13.2			
		To negative rail R_S = 50Ω			–15.3	–15	
			T_A = –40°C to +125°C			–15	
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50Ω		100	115		dB
			T_A = –40°C to +125°C	96			
V_O	Output voltage swing	To positive rail R_L = 10kΩ		14	14.3		V
			T_A = –40°C to +125°C	13.8			
		To negative rail R_L = 10kΩ			–14.1	–13.7	
			T_A = –40°C to +125°C			–13.6	
I_{CC}	Supply current	No load			200	350	µA
			T_A = –40°C to +125°C			350	
AC SPECS							
SR	Slew rate	V_O = ±10V, G = 1			0.65		V/µs
V_n	Input voltage noise density	f = 10Hz			19		nV/√Hz
		f = 1kHz			15		
V_N	Input voltage noise	f = 0.1Hz to 1Hz			0.16		$µV_{PP}$
		f = 0.1Hz to 10Hz			0.47		
I_n	Input current noise density				0.09		pA/√Hz
B_1	Gain bandwidth				2		MHz
$Θ_m$	Phase margin				46°		

5.7 Electrical Characteristics for TLE2021-Q1, V_{CC} = 5V

at T_A = 25°C, V_{CC+} = 5V, V_{CC-} = 0V, and V_{IC} = V_{OUT} = V_{CC+} / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V_{IO}	Input offset voltage	TLE2021-Q1 R_S = 50Ω			±120	±600	µV
			T_A = –40°C to +125°C			±800	
		TLE2021A-Q1 R_S = 50Ω			±100	±400	
			T_A = –40°C to +125°C			±550	
dV_{IO}/dT	Input offset voltage drift	R_S = 50Ω, T_A = –40°C to +125°C			±2		µV/°C
I_{IB}	Input bias current	R_S = 50Ω			25	70	nA
			T_A = –40°C to +125°C			90	
I_{IO}	Input offset current	R_S = 50Ω			0.2	6	nA
			T_A = –40°C to +125°C			10	
PSRR	Power-supply rejection ratio	V_{CC} = 5V to 30V		105	120		dB
			T_A = –40°C to +125°C	100			
A_{VD}	Large signal voltage gain	R_L = 10kΩ, V_O = 1.4V to 4V		0.3	1.5		V/µV
			T_A = –40°C to +125°C	0.1			
V_{ICR}	Common-mode input voltage range	To positive rail R_S = 50Ω		3.5	4		V
			T_A = –40°C to +125°C	3.2			
		To negative rail R_S = 50Ω			–0.3	0	
			T_A = –40°C to +125°C			0	
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50Ω		85	110		dB
			T_A = –40°C to +125°C	80			
V_O	Output voltage swing	To positive rail R_L = 10kΩ		4	4.3		V
			T_A = –40°C to +125°C	3.8			
		To negative rail R_L = 10kΩ			0.7	0.8	
			T_A = –40°C to +125°C			0.95	
I_{CC}	Supply current	No load			170	300	µA
			T_A = –40°C to +125°C			300	
AC SPECS							
SR	Slew rate	V_O = ±10V, G = 1			0.5		V/µs
V_n	Input voltage noise density	f = 10Hz			21		nV/√Hz
		f = 1kHz			17		
V_N	Input voltage noise	f = 0.1Hz to 1Hz			0.16		$µV_{PP}$
		f = 0.1Hz to 10Hz			0.47		
I_n	Input current noise density				0.9		pA/√Hz
B_1	Gain bandwidth				1.2		MHz
$Θ_m$	Phase margin				42°		

5.8 Electrical Characteristics for TLE2022-Q1, V_{CC} = ±15V

at T_A = 25°C, V_{CC} = ±15V, and V_{IC} = V_{OUT} = V_{CC} / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V_{IO}	Input offset voltage	TLE2022-Q1 R_S = 50Ω			±150	±500	µV
			T_A = –40°C to +125°C			±700	
		TLE2022A-Q1 R_S = 50Ω			±120	±300	
			T_A = –40°C to +125°C			±450	
dV_{IO}/dT	Input offset voltage drift	R_S = 50Ω, T_A = –40°C to +125°C			±2		µV/°C
I_{IB}	Input bias current	TLE2022-Q1 R_S = 50Ω			35	70	nA
			T_A = –40°C to +125°C			90	
		TLE2022A-Q1 R_S = 50Ω			33	70	
			T_A = –40°C to +125°C			90	
I_{IO}	Input offset current	TLE2022-Q1 R_S = 50Ω			0.5	6	nA
			T_A = –40°C to +125°C			10	
		TLE2022A-Q1 R_S = 50Ω			0.4	6	
			T_A = –40°C to +125°C			10	
PSRR	Power supply rejection ratio	TLE2022-Q1 $V_{CC±}$ = ±2.5V to ±15V		100	115		dB
			T_A = –40°C to +125°C	95			
		TLE2022-Q1 $V_{CC±}$ = ±2.5V to ±15V		103	118		
			T_A = –40°C to +125°C	98			
A_{VD}	Large signal voltage gain	TLE2022-Q1 V_O = ±10V, R_L = 10kΩ		0.8	4		V/µV
			T_A = –40°C to +125°C	0.8			
		TLE2022A-Q1 V_O = ±10V, R_L = 10kΩ		1	7		
			T_A = –40°C to +125°C	1			
V_{ICR}	Common-mode input voltage range	To positive rail R_S = 50Ω		13.5	14		V
			T_A = –40°C to +125°C	13.2			
		To negative rail R_S = 50Ω			–15.3	–15	
			T_A = –40°C to +125°C			–15	
CMRR	Common-mode rejection ratio	TLE2022-Q1 V_{IC} = V_{ICR}min, R_S = 50Ω		95	106		dB
			T_A = –40°C to +125°C	91			
		TLE2022A-Q1 V_{IC} = V_{ICR}min, R_S = 50Ω		97	109		
			T_A = –40°C to +125°C	93			
V_O	Output voltage swing	To positive rail R_L = 10kΩ		14	14.3		V
			T_A = –40°C to +125°C	13.8			
		To negative rail R_L = 10kΩ			–14.1	–13.7	
			T_A = –40°C to +125°C			–13.6	
I_{CC}	Supply current	No load			550	700	µA
			T_A = –40°C to +125°C			700	
AC SPECS							
SR	Slew rate	V_O = ±10V, G = 1			0.65		V/µs
V_n	Input voltage noise density	f = 10Hz			19		nV/√Hz
		f = 1kHz			15		
V_N	Input voltage noise	f = 0.1Hz to 1Hz			0.16		$µV_{PP}$
		f = 0.1Hz to 10Hz			0.47		$µV_{PP}$
I_n	Input current noise density				0.1		pA/√Hz
B_1	Gain bandwidth				2.8		MHz
$Θ_m$	Phase margin				52°		

5.9 Electrical Characteristics for TLE2022-Q1, V_{CC} = 5V

at T_A = 25°C, V_{CC+} = 5V, V_{CC-} = 0V, and V_{IC} = V_{OUT} = V_{CC+} / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V_{IO}	Input offset voltage	TLE2022-Q1 R_S = 50Ω				±600	µV
			T_A = –40°C to +125°C			±800	µV
		TLE2022A-Q1 R_S = 50Ω				±400	µV
			T_A = –40°C to +125°C			±550	µV
dV_{IO}/dT	Input offset voltage drift	R_S = 50Ω, T_A = –40°C to +125°C			±2		µV/°C
I_{IB}	Input bias current	TLE2022-Q1 R_S = 50Ω			35	70	nA
			T_A = –40°C to +125°C			90	
		TLE2022A-Q1 R_S = 50Ω			33	70	
			T_A = –40°C to +125°C			90	
I_{IO}	Input offset current	TLE2022-Q1 R_S = 50Ω			0.5	6	nA
			T_A = –40°C to +125°C			10	
		TLE2022A-Q1 R_S = 50Ω			0.4	6	
			T_A = –40°C to +125°C			10	
PSRR	Power-supply rejection ratio	TLE2022-Q1 V_{CC} = 5V to 30V		100	115		dB
			T_A = –40°C to +125°C	95			
		TLE2022A-Q1 V_{CC} = 5V to 30V		103	118		
			T_A = –40°C to +125°C	98			
A_{VD}	Large signal voltage gain	TLE2022-Q1 V_O = 1.4V to 4V, R_L = 10kΩ		0.3	1.5		V/µV
			T_A = –40°C to +125°C	0.1			
		TLE2022A-Q1 V_O = 1.4V to 4V, R_L = 10kΩ		0.4	1.5		
			T_A = –40°C to +125°C	0.1			
V_{ICR}	Common-mode input voltage range	To positive rail R_S = 50Ω		3.5	4		V
			T_A = –40°C to +125°C	3.2			
		To negative rail R_S = 50Ω			–0.3	0	
			T_A = –40°C to +125°C			0	
CMRR	Common-mode rejection ratio	TLE2022-Q1 V_{IC} = V_{ICR}min, R_S = 50Ω		85	100		dB
			T_A = –40°C to +125°C	80			
		TLE2022A-Q1 V_{IC} = V_{ICR}min, R_S = 50Ω		87	102		
			T_A = –40°C to +125°C	82			
V_O	Output voltage swing	To positive rail R_L = 10kΩ		4	4.3		V
			T_A = –40°C to +125°C	3.8			
		To negative rail R_L = 10kΩ			0.7	0.8	
			T_A = –40°C to +125°C			0.95	
I_{CC}	Supply current	No load			450	600	µA
			T_A = –40°C to +125°C			600	
AC SPECS							
SR	Slew rate	V_O = 1V to 3V, G = 1			0.5		V/µs
V_n	Input voltage noise density	f = 10Hz			21		nV/√Hz
		f = 1kHz			17		
V_N	Input voltage noise	f = 0.1Hz to 1Hz			0.16		$µV_{PP}$
		f = 0.1Hz to 10Hz			0.47		
I_n	Input current noise density				0.1		pA/√Hz
B_1	Gain bandwidth				1.7		MHz
$Θ_m$	Phase margin				47°		

5.10 Electrical Characteristics for TLE2024-Q1, V_{CC} = ±15V

at T_A = 25°C, V_{CC} = ±15V, and V_{IC} = V_{OUT} = V_{CC} / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V_{IO}	Input offset voltage	TLE2024-Q1 R_S = 50Ω				±1000	µV
			T_A = –40°C to +125°C			±1200	
		TLE2024A-Q1 R_S = 50Ω				±750	
			T_A = –40°C to +125°C			±950	
dV_{IO}/dT	Input offset voltage drift	R_S = 50Ω, T_A = –40°C to +125°C			±2		µV/°C
I_{IB}	Input bias current	TLE2024-Q1 R_S = 50Ω			50	70	nA
			T_A = –40°C to +125°C			90	
		TLE2024A-Q1 R_S = 50Ω			45	70	
			T_A = –40°C to +125°C			90	
I_{IO}	Input offset current	TLE2024-Q1 R_S = 50Ω			0.6	6	nA
			T_A = –40°C to +125°C			10	
		TLE2024A-Q1 R_S = 50Ω			0.2	6	
			T_A = –40°C to +125°C			10	
PSRR	Power supply rejection ratio	TLE2024-Q1 $V_{CC±}$ = ±2.5V to ±15V		98	112		dB
			T_A = –40°C to +125°C	93			
		TLE2024A-Q1 $V_{CC±}$ = ±2.5V to ±15V		100	115		
			T_A = –40°C to +125°C	95			
A_{VD}	Large signal voltage gain	TLE2024-Q1 V_O = ±10V, R_L = 10kΩ		0.4	2		V/µV
			T_A = –40°C to +125°C	0.4			
		TLE2024A-Q1 V_O = ±10V, R_L = 10kΩ		0.8	4		
			T_A = –40°C to +125°C	0.8			
V_{ICR}	Common-mode input voltage range	To positive rail R_S = 50Ω		13.5	14		V
			T_A = –40°C to +125°C	13.2			
		To negative rail R_S = 50Ω			–15.3	–15	
			T_A = –40°C to +125°C			–15	
CMRR	Common-mode rejection ratio	TLE2024-Q1 V_{IC} = V_{ICR}min, R_S = 50Ω		92	102		dB
			T_A = –40°C to +125°C	88			
		TLE2024A-Q1 V_{IC} = V_{ICR}min, R_S = 50Ω		94	105		
			T_A = –40°C to +125°C	90			
V_O	Output voltage swing	To positive rail R_L = 10kΩ		13.8	14.1		V
			T_A = –40°C to +125°C	13.7			
		To negative rail R_L = 10kΩ			–14.1	–13.7	
			T_A = –40°C to +125°C			–13.6	
I_{CC}	Supply current	No load			1050	1400	µA
			T_A = –40°C to +125°C			1400	
AC SPECS							
SR	Slew rate	V_O = ±10V, G = 1			0.7		V/µs
V_n	Input voltage noise density	f = 10Hz			19		nV/√Hz
		f = 1kHz			15		
V_N	Input voltage noise	f = 0.1Hz to 1Hz			0.16		$µV_{PP}$
		f = 0.1Hz to 10Hz			0.47		
I_n	Input current noise density				0.1		pA/√Hz
B_1	Gain bandwidth				2.8		MHz
$Θ_m$	Phase margin				52°		

5.11 Electrical Characteristics for TLE2024-Q1, V_{CC} = 5V

at T_A = 25°C, V_{CC+} = 5V, V_{CC-} = 0V, and V_{IC} = V_{OUT} = V_{CC+} / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V_{IO}	Input offset voltage	TLE2024-Q1 R_S = 50Ω				±1100	µV
			T_A = –40°C to +125°C			±1300	
		TLE2024A-Q1 R_S = 50Ω				±850	
			T_A = –40°C to +125°C			±1050	
dV_{IO}/dT	Input offset voltage drift	R_S = 50Ω, T_A = –40°C to +125°C			±2		µV/°C
I_{IB}	Input bias current	TLE2024-Q1 R_S = 50Ω			45	70	nA
			T_A = –40°C to +125°C			90	
		TLE2024A-Q1 R_S = 50Ω			40	70	
			T_A = –40°C to +125°C			90	
I_{IO}	Input offset current	TLE2024-Q1 R_S = 50Ω			0.6	6	nA
			T_A = –40°C to +125°C			10	
		TLE2024A-Q1 R_S = 50Ω			0.5	6	
			T_A = –40°C to +125°C			10	
PSRR	Power supply rejection ratio	TLE2024-Q1 $V_{CC±}$ = ±2.5V to ±15V		98	112		dB
			T_A = –40°C to +125°C	93			
		TLE2024-Q1 $V_{CC±}$ = ±2.5V to ±15V		100	115		
			T_A = –40°C to +125°C	95			
A_{VD}	Large signal voltage gain	TLE2024-Q1 V_O = 1.4V to 4V, R_L = 10kΩ		0.2	1.5		V/µV
			T_A = –40°C to +125°C	0.1			
		TLE2024A-Q1 V_O = 1.4V to 4V, R_L = 10kΩ		0.3	1.5		
			T_A = –40°C to +125°C	0.1			
V_{ICR}	Common-mode input voltage range	To positive rail R_S = 50Ω		3.5	4		V
			T_A = –40°C to +125°C	3.2			
		To negative rail R_S = 50Ω			–0.3	0	
			T_A = –40°C to +125°C			0	
CMRR	Common-mode rejection ratio	TLE2024-Q1 V_{IC} = V_{ICR}min, R_S = 50Ω		80	90		dB
			T_A = –40°C to +125°C	80			
		TLE2024A-Q1 V_{IC} = V_{ICR}min, R_S = 50Ω		82	92		
			T_A = –40°C to +125°C	82			
V_O	Output voltage swing	To positive rail R_L = 10kΩ		3.9	4.2		V
			T_A = –40°C to +125°C	3.7			
		To negative rail R_L = 10kΩ			0.7	0.8	
			T_A = –40°C to +125°C			0.95	
I_{CC}	Supply current	No load			800	1200	µA
			T_A = –40°C to +125°C			1200	
AC SPECS							
SR	Slew rate	V_O =1V to 3V, G = 1			0.5		V/µs
V_n	Input voltage noise density	f = 10Hz			21		nV/√Hz
		f = 1kHz			17		
V_N	Input voltage noise	f = 0.1Hz to 1Hz			0.16		$µV_{PP}$
		f = 0.1Hz to 10Hz			0.47		$µV_{PP}$
I_n	Input current noise density				0.1		pA/√Hz
B_1	Gain bandwidth				1.7		MHz
$Θ_m$	Phase margin				47°		

5.12 Typical Characteristics

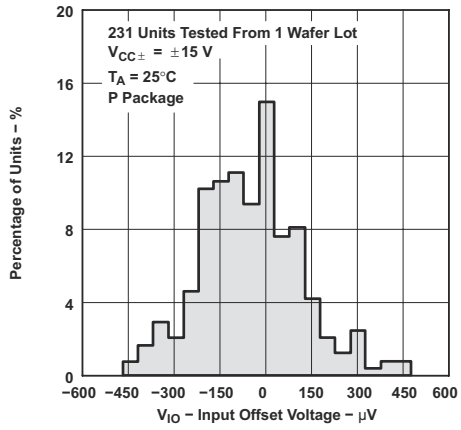


Figure 5-1. Distribution of TLE2021-Q1 Input Offset Voltage

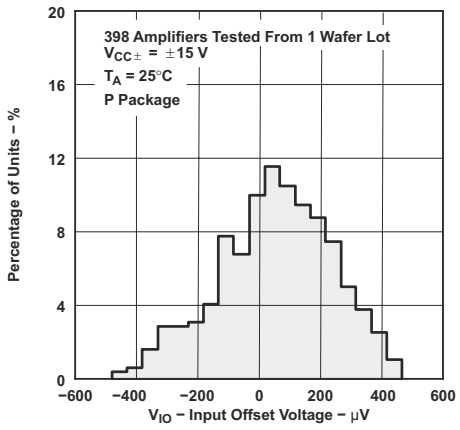


Figure 5-2. Distribution of TLE2022-Q1 Input Offset Voltage

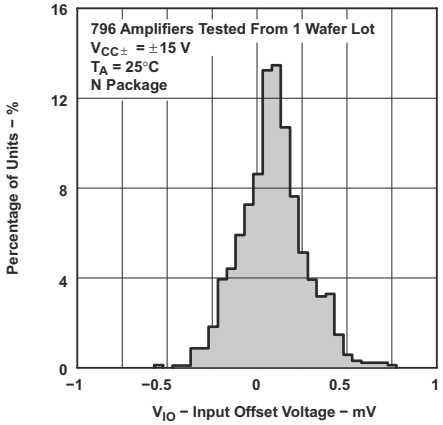


Figure 5-3. Distribution of TLE2024-Q1 Input Offset Voltage

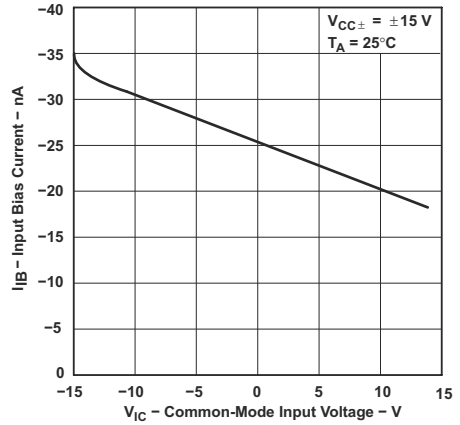


Figure 5-4. TLE2021-Q1 Input Bias Current vs Common-Mode Input Voltage

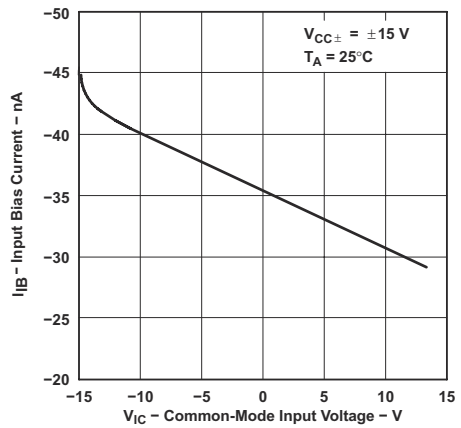


Figure 5-5. TLE2022-Q1 Input Bias Current vs Common-Mode Input Voltage

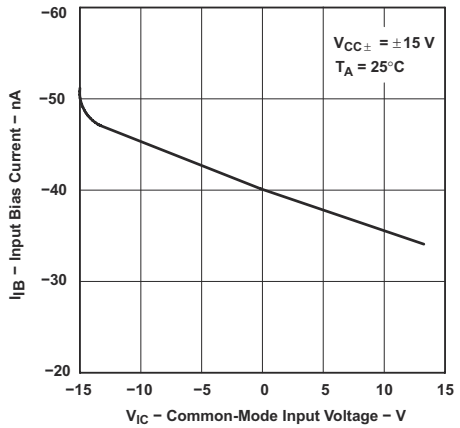
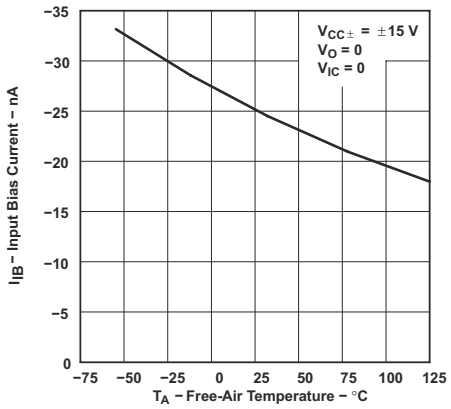


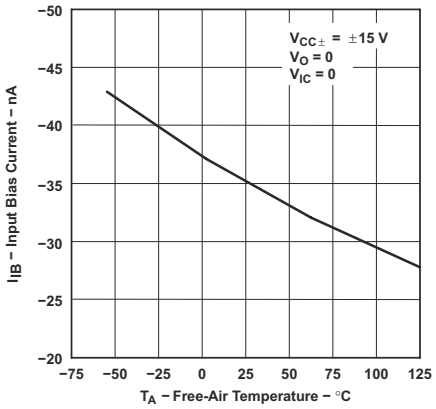
Figure 5-6. TLE2024-Q1 Input Bias Current vs Common-Mode Input Voltage

5.12 Typical Characteristics (continued)



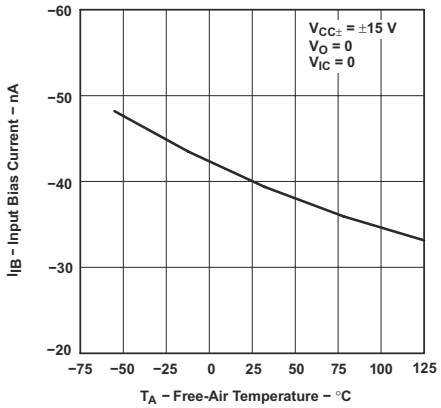
Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 5-7. TLE2021-Q1 Input Bias Current vs Free-Air Temperature



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 5-8. TLE2022-Q1 Input Bias Current vs Free-Air Temperature



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 5-9. TLE2024-Q1 Input Bias Current vs Free-Air Temperature

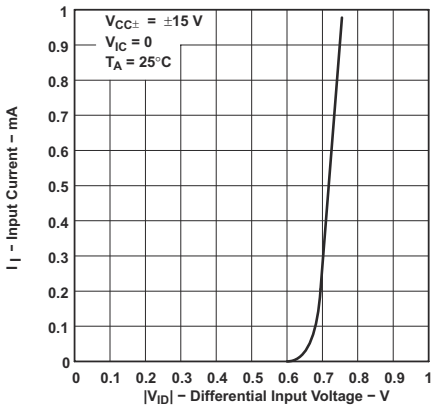


Figure 5-10. Input Current vs Differential Input Voltage

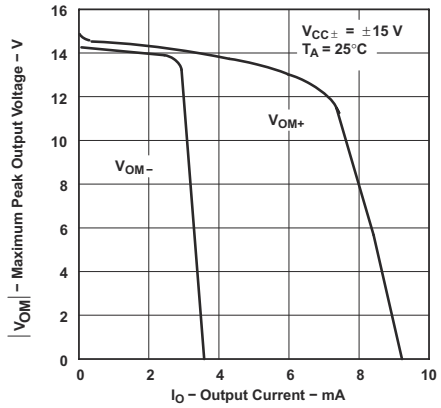


Figure 5-11. TLE2021-Q1 Maximum Peak Output Voltage vs Output Current

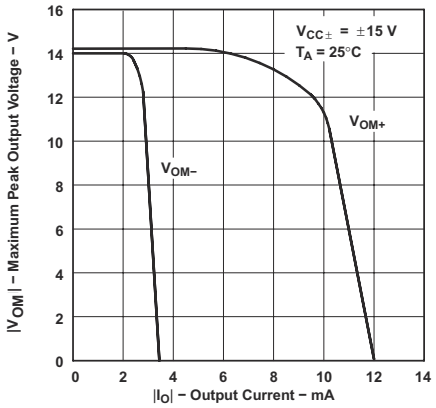


Figure 5-12. TLE2022-Q1 Maximum Peak Output Voltage vs Output Current

5.12 Typical Characteristics (continued)

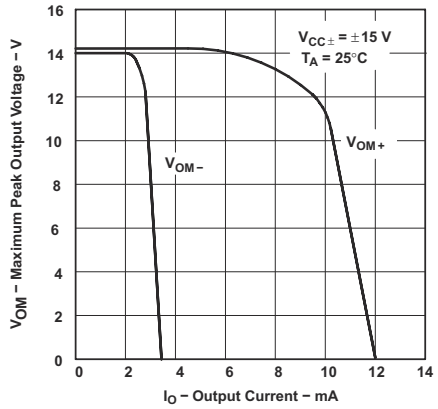
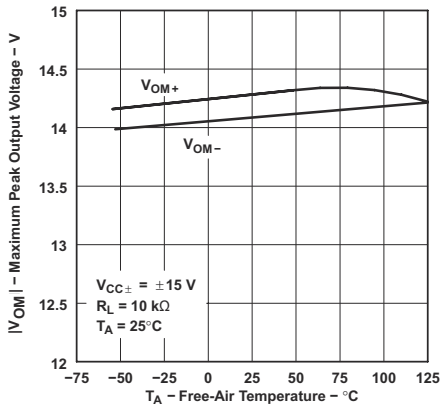


Figure 5-13. TLE2024-Q1 Maximum Peak Output Voltage vs Output Current



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 5-14. Maximum Peak Output Voltage vs Free-Air Temperature

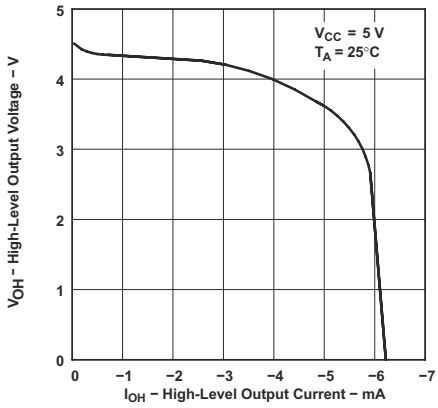


Figure 5-15. TLE2021-Q1 High-Level Output Voltage vs High-Level Output Current

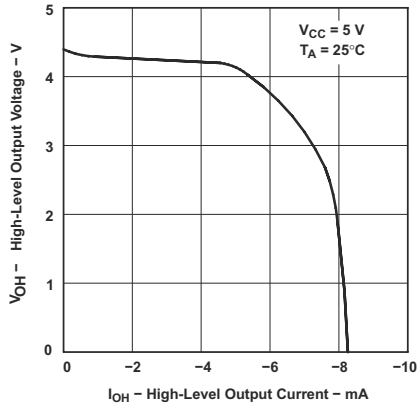
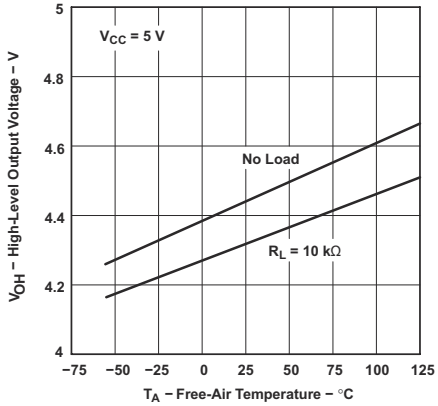


Figure 5-16. TLE2022-Q1 and TLE2024-Q1 High-Level Output Voltage vs High-Level Output Current



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 5-17. High-Level Output Voltage vs Free-Air Temperature

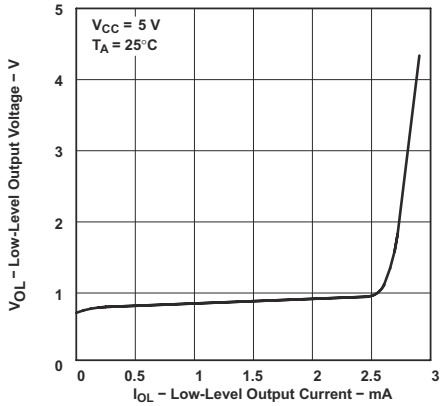
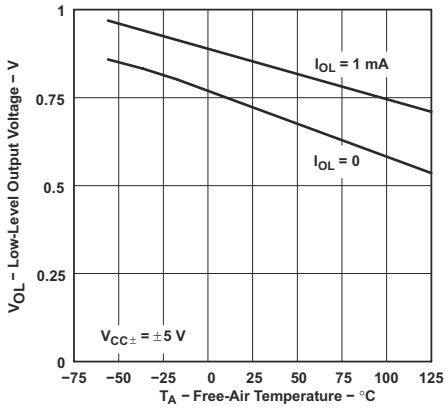


Figure 5-18. Low-Level Output Voltage vs Low-Level Output Current

5.12 Typical Characteristics (continued)



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 5-19. Low-Level Output Voltage vs Free-Air Temperature

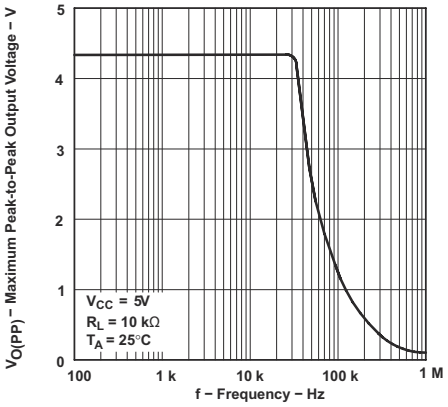


Figure 5-20. Maximum Peak-to-Peak Output Voltage Vs Frequency

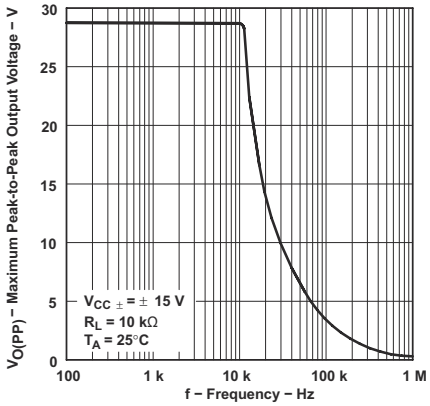


Figure 5-21. Maximum Peak-to-Peak Output Voltage vs Frequency

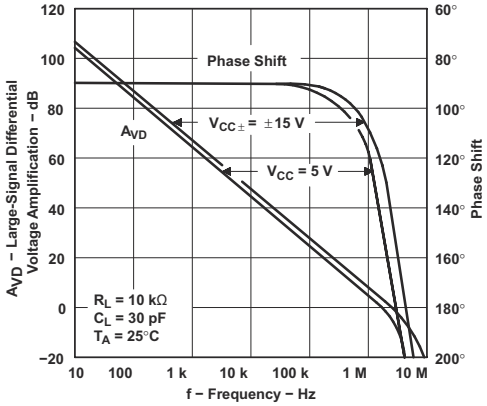
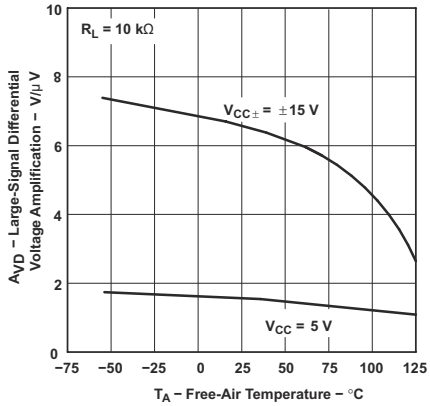
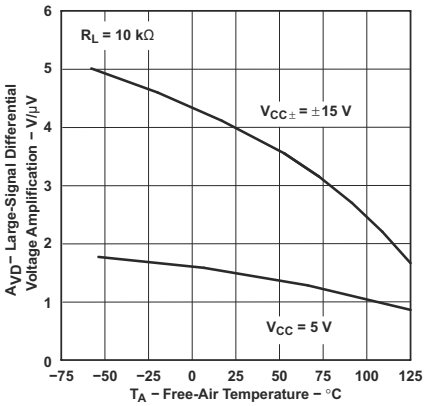


Figure 5-22. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

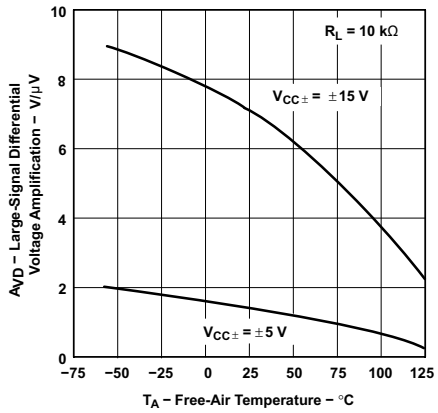
Figure 5-23. TLE2021-Q1 Large-Scale Differential Voltage Amplification vs Free-Air Temperature



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 5-24. TLE2022-Q1 Large-Signal Differential Voltage Amplification vs Free-Air Temperature

5.12 Typical Characteristics (continued)



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 5-25. TLE2024-Q1 Large-Scale Differential Voltage Amplification vs Free-Air Temperature

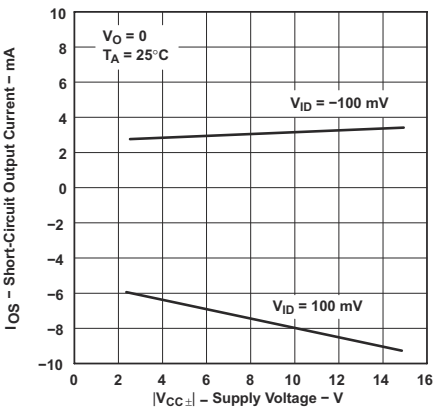


Figure 5-26. TLE2021-Q1 Short-Circuit Output Current vs Supply Voltage

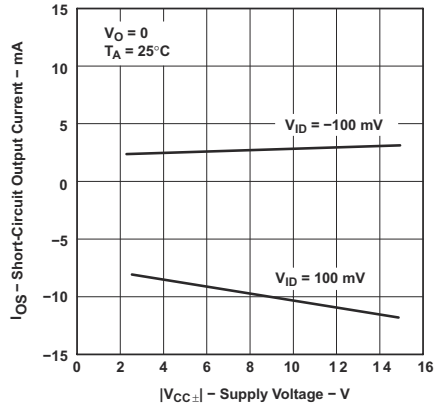


Figure 5-27. TLE2022-Q1 and TLE2024-Q1 Short-Circuit Output Current vs Supply Voltage

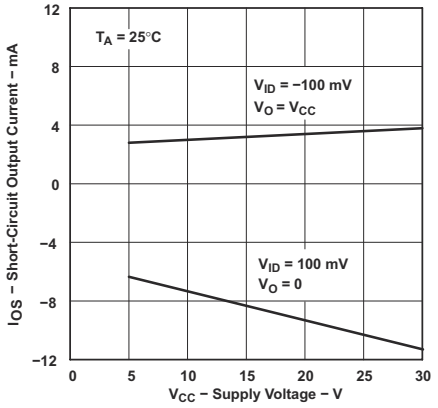
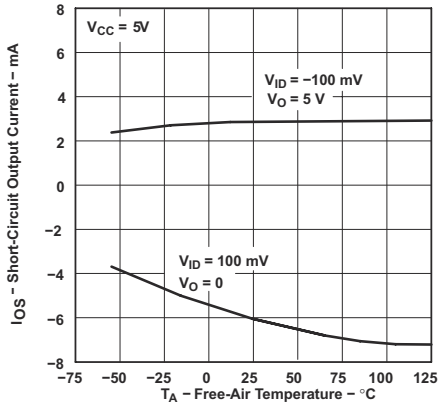


Figure 5-28. TLE2021-Q1 Short-Circuit Output Current vs Supply Voltage



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 5-29. TLE2021-Q1 Short-Circuit Output Current vs Free-Air Temperature

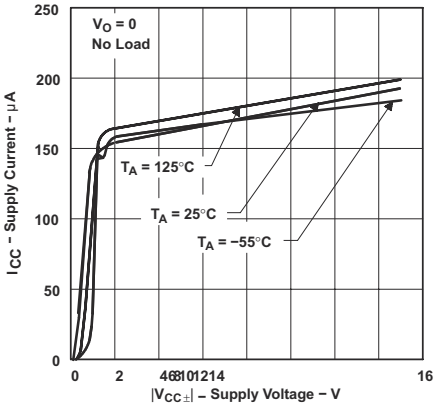


Figure 5-30. TLE2021-Q1 Supply Current vs Supply Voltage

5.12 Typical Characteristics (continued)

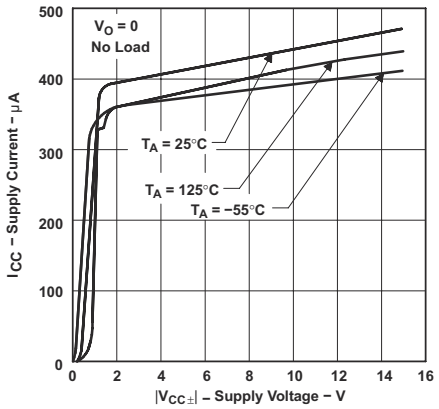


Figure 5-31. TLE2022-Q1 Supply Current vs Supply Voltage

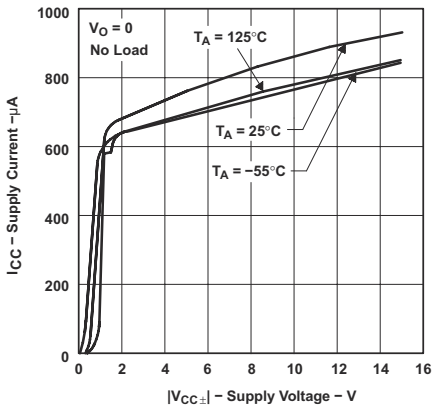
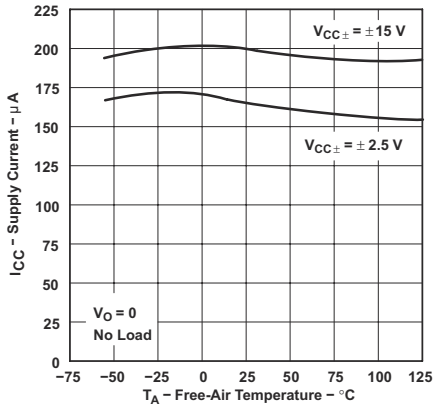
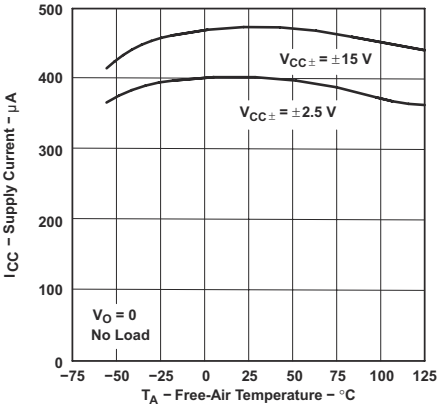


Figure 5-32. TLE2024-Q1 Supply Current vs Supply Voltage



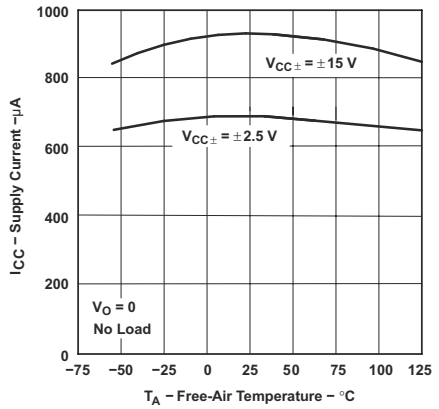
Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 5-33. TLE2021-Q1 Supply Current vs Free-Air Temperature



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 5-34. TLE2022-Q1 Supply Current vs Free-Air Temperature



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 5-35. TLE2024-Q1 Supply Current vs Free-Air Temperature

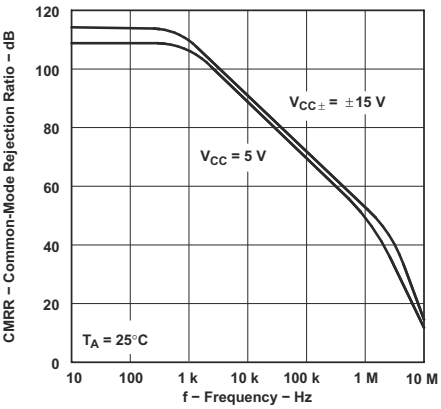


Figure 5-36. TLE2021-Q1 Common-Mode Rejection Ratio vs Frequency

5.12 Typical Characteristics (continued)

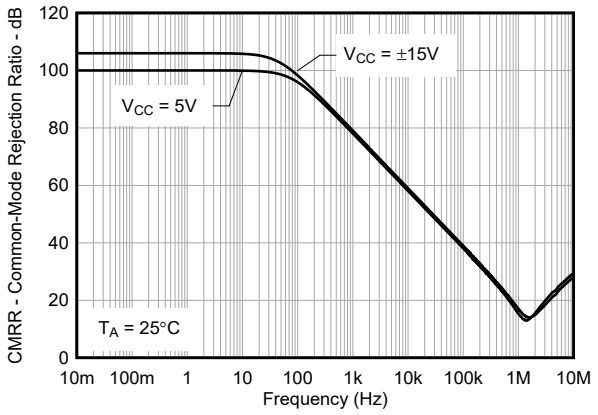


Figure 5-37. TLE2022-Q1 Common-Mode Rejection Ratio vs Frequency

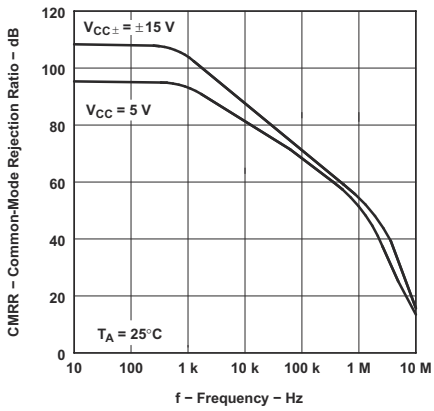


Figure 5-38. TLE2024-Q1 Common-Mode Rejection Ratio vs Frequency

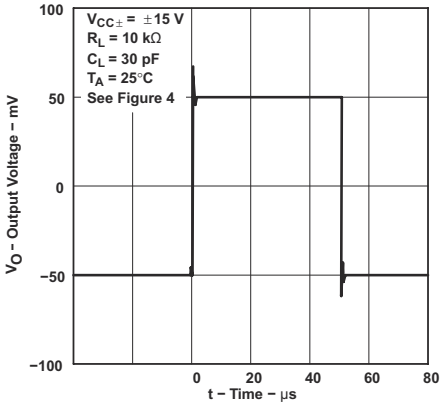


Figure 5-39. Voltage-Follower Small-Signal Pulse Response

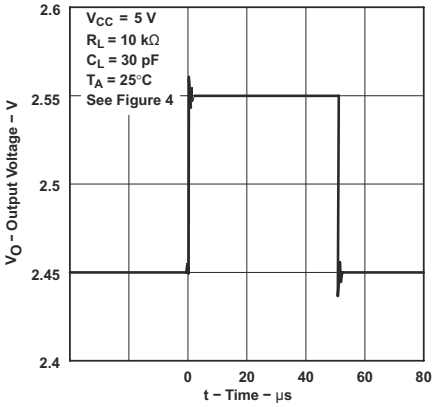


Figure 5-40. Voltage-Follower Small-Signal Pulse Response

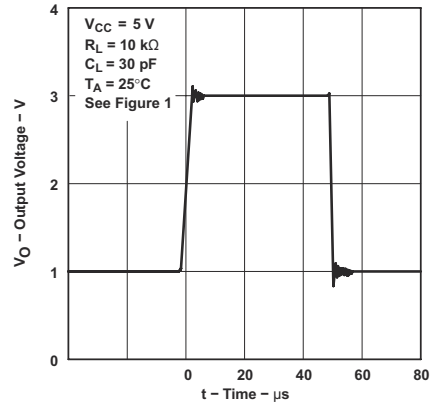


Figure 5-41. TLE2021-Q1 Voltage-Follower Large-Signal Pulse Response

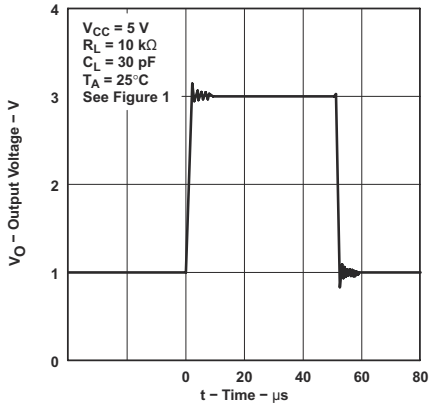


Figure 5-42. TLE2022-Q1 Voltage-Follower Large-Signal Pulse Response

5.12 Typical Characteristics (continued)

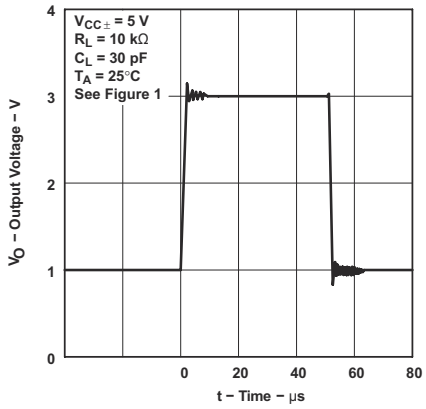


Figure 5-43. TLE2024-Q1 Voltage-Follower Large-Scale Pulse Response

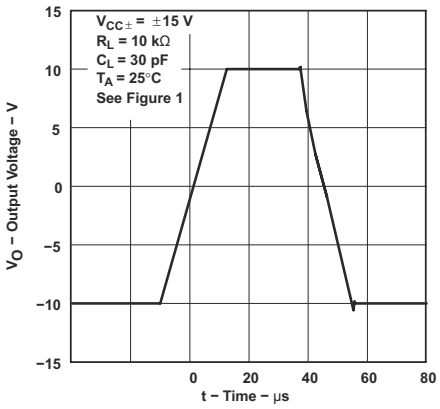


Figure 5-44. TLE2021-Q1 Voltage-Follower Large-Signal Pulse Response

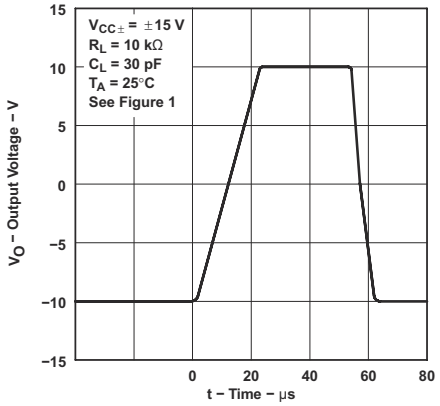


Figure 5-45. TLE2022-Q1 Voltage-Follower Large-Signal Pulse Response

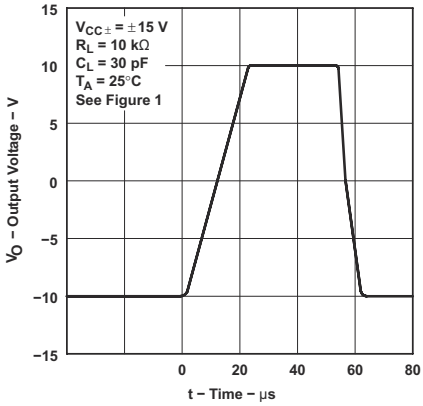


Figure 5-46. TLE2024-Q1 Voltage-Follower Large-Signal Pulse Response

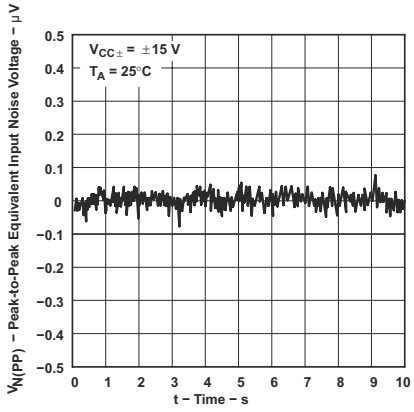


Figure 5-47. Peak-to-Peak Equivalent Input Noise Voltage 0.1Hz to 1Hz

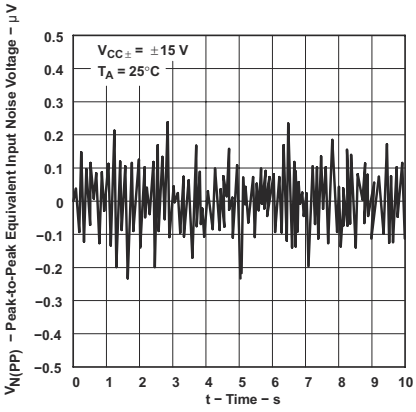


Figure 5-48. Peak-to-Peak Equivalent Input Noise Voltage 0.1Hz to 10Hz

5.12 Typical Characteristics (continued)

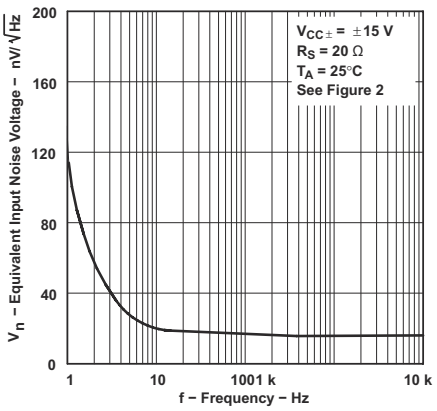


Figure 5-49. Equivalent Input Noise Voltage vs Frequency

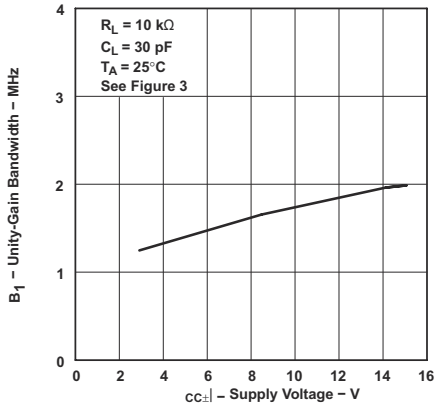


Figure 5-50. TLE2021-Q1 Unity-Gain Bandwidth vs Supply Voltage

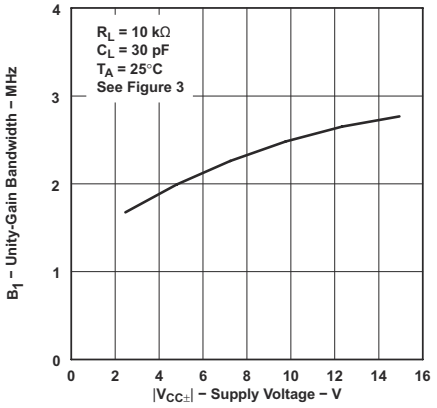


Figure 5-51. TLE2022-Q1 and TLE2024-Q1 Unity-Gain Bandwidth vs Supply Voltage

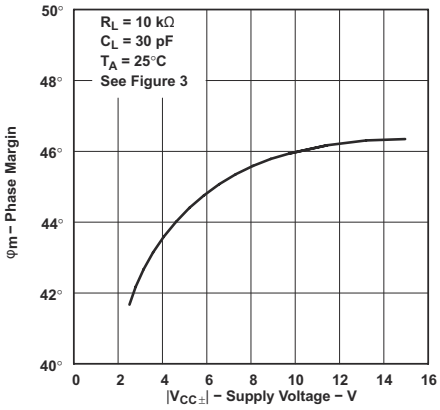


Figure 5-52. TLE2021-Q1 Phase Margin vs Supply Voltage

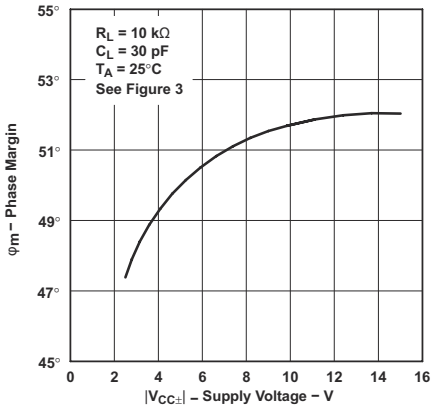


Figure 5-53. TLE2022-Q1 and TLE2024-Q1 Phase Margin vs Supply Voltage

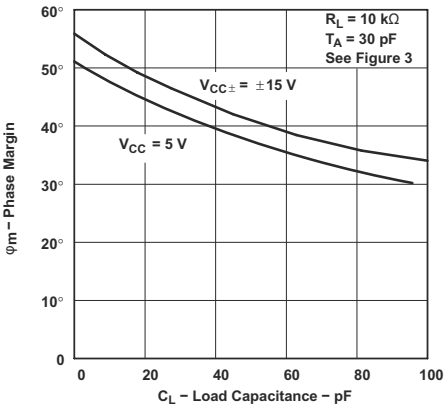


Figure 5-54. TLE2021-Q1 Phase Margin vs Load Capacitance

5.12 Typical Characteristics (continued)

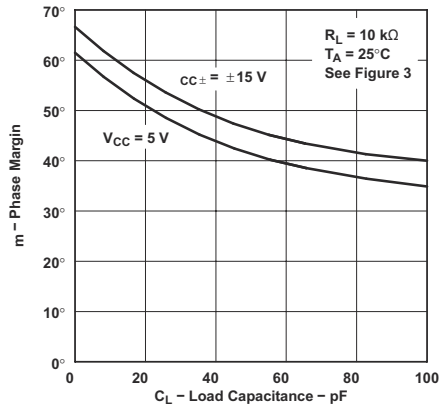


Figure 5-55. TLE2022-Q1 and TLE2024-Q1 Phase Margin vs Load Capacitance

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

6.1.1 Voltage-Follower Applications

The TLE202x-Q1 circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition sometimes occurs when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. Use a feedback resistor to limit the current to a maximum of 1mA to prevent degradation of the device. This feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10kΩ, this pole degrades the amplifier phase margin. Figure 6-1 shows that to alleviate this problem, add a capacitor (20pF to 50pF) in parallel with the feedback resistor.

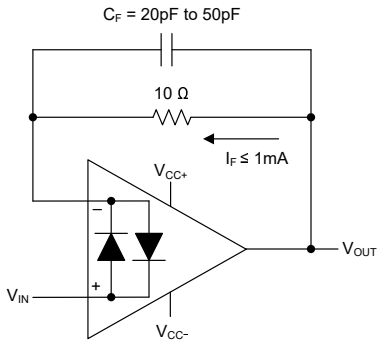


Figure 6-1. Voltage Follower

6.1.2 Input Offset Voltage Null

The TLE202x-Q1 series offers external null pins that further reduce the input offset voltage. Figure 6-2 shows how to connect the circuit if this feature is desired. Adjust the external resistance value to achieve desired performance. When external null is not needed, leave the null pins disconnected. Only use this adjustment to null the offset of the operational amplifier. Do not use this adjustment to compensate for offsets created elsewhere in a system because of the possible introduction of additional temperature drift.

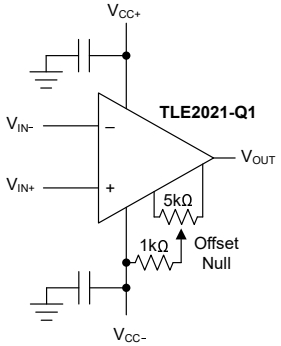


Figure 6-2. Input Offset Voltage Null Circuit

Internal resistances vary; unexpected results are sometimes produced when using fixed resistors to null the offset of the amplifier.

6.2 Layout

6.2.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

1. Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V_{CC+} to ground is applicable for single-supply applications. Noise propagates into analog circuitry through the power pins of the circuit as a whole, as well as through the individual op amp. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
2. Physically separate digital and analog grounds, paying special attention to the ground-current flow. Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
3. To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
4. Place the external components as close to the device as possible. Figure 6-4 shows how to keep RF and RG close to the inverting input to minimize parasitic capacitance.
5. Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
6. Consider a driven, low-impedance guard ring around the critical traces. Use a guard ring to significantly reduce leakage currents from nearby traces that are at different potentials.
7. Clean the PCB following board assembly for best performance.
8. Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

6.2.2 Layout Example

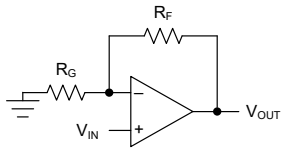


Figure 6-3. Schematic Representation

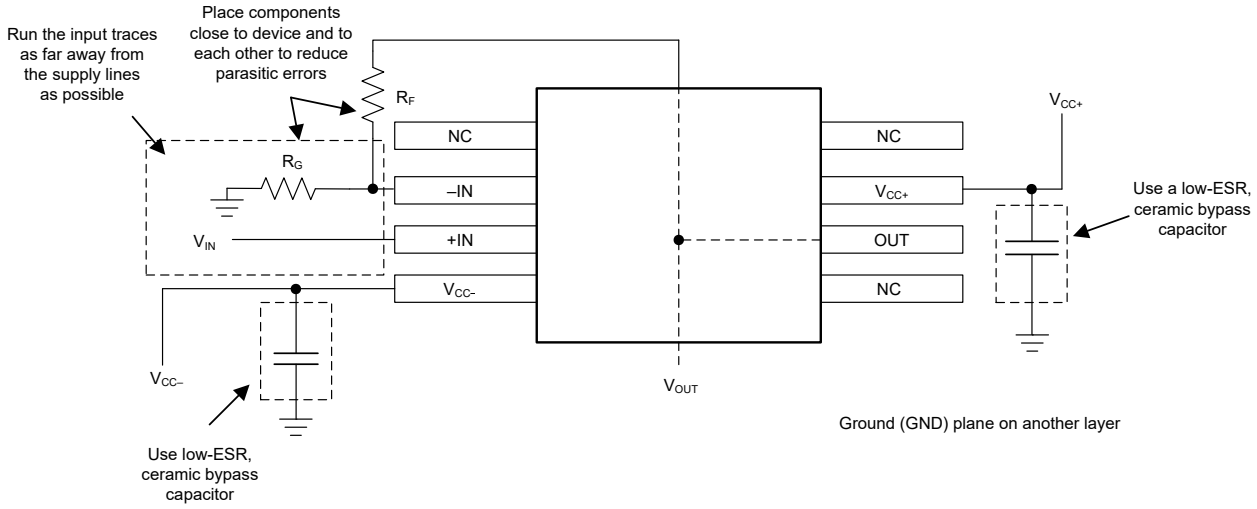


Figure 6-4. Operational Amplifier Board Layout for Noninverting Configuration

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2008) to Revision C (July 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *Applications*, *Specifications*, *Pin Configuration and Functions*, *Specifications*, *Thermal Information*, *Application and Implementation*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Updated data sheet title	1
• Deleted all references to Excalibur process	1
• Deleted PW (TSSOP) package and associated content from data sheet	1
• Updated *Features*	1
• Deleted machine model information from *Features*	1
• Added *Applications*	1
• Updated *Description*	1
• Deleted content related to long-term input offset drift from data sheet	1
• Deleted *Equivalent Schematic (Each Amplifier)*	3
• Updated pin names in *Pin Functions* tables in *Pin Configurations and Functions*	3
• Updated format of all specifications tables	5
• Updated input voltage range in *Absolute Maximum Ratings*	5
• Updated note 4 in *Absolute Maximum Ratings*	5
• Deleted note 5 in *Absolute Maximum Ratings*	5
• Moved package thermal impedance from *Absolute Maximum Ratings* to *Thermal Information*	5

- Deleted operating free air temperature range from *Absolute Maximum Ratings* 5
- Changed common-mode input voltage condition from V_{CC} = ±5V to V_{CC+} = 5V (typo) in *Recommended Operating Conditions* 5
- Updated parameter names and symbols for clarity in all *Electrical Characteristics* tables..... 7
- Added ± on input offset voltage and input offset voltage drift to all *Electrical Characteristics* tables..... 7
- Deleted input offset voltage long-term drift from all *Electrical Characteristics* tables..... 7
- Deleted note 4 from all *Electrical Characteristics* tables..... 7
- Moved common-mode voltage (to negative rail) from MIN to MAX in all *Electrical Characteristics* tables..... 7
- Moved voltage output swing (negative) from MIN to MAX in *Electrical Characteristics* all tables..... 7
- Deleted supply current change over operating temperature range from all *Electrical Characteristics* tables.... 7
- Deleted slew rate at unity gain MIN from all V_{CC} = ±15V *Electrical Characteristics* tables..... 7
- Deleted slew rate at unity gain over temperature MIN from all V_{CC} = ±15V *Electrical Characteristics* tables....7
- Changed TLE2024A-Q1 output voltage swing TYP from 14.2V to 14.1V..... 11
- Deleted *Parameter Measurement Information* section..... 13
- Deleted Figures 34 to 37, Figures 47 to 49, Figures 63 to 64, and Figures 69 to 70..... 13
- Updated Figures 44 to 46 (*Common-Mode Rejection Ratio vs Frequency*)..... 13
- Updated Figure 6-1, *Voltage Follower* 23
- Deleted *Macromodel Information* 23
- Updated *Input Offset Voltage Nulling* description..... 23
- Updated Figure 6-2, *Input Offset Voltage Null Circuit* 23

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2021AQDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2021AQ
TLE2021AQDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2021AQ
TLE2021AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2021AQ
TLE2021AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2021AQ
TLE2021QDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2021Q1
TLE2021QDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2021Q1
TLE2021QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2021Q1
TLE2021QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2021Q1
TLE2022AQDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2022AQ
TLE2022AQDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2022AQ
TLE2022QDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2022Q1
TLE2022QDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2022Q1
TLE2022QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2022Q1
TLE2022QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2022Q1
TLE2024QDWRG4Q1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2024Q1
TLE2024QDWRG4Q1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2024Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLE2021-Q1, TLE2021A-Q1, TLE2022-Q1, TLE2022A-Q1, TLE2024-Q1 :

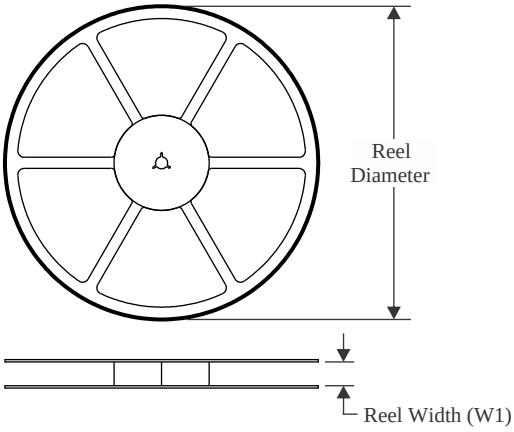
- Catalog : TLE2021, TLE2021A, TLE2022, TLE2022A, TLE2024
- Enhanced Product : TLE2021-EP, TLE2021A-EP, TLE2022-EP, TLE2022A-EP, TLE2024-EP
- Military : TLE2021M, TLE2021AM, TLE2022M, TLE2022AM, TLE2024M

NOTE: Qualified Version Definitions:

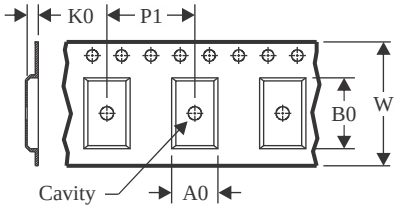
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

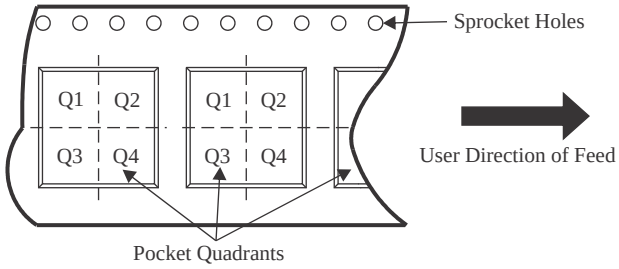


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

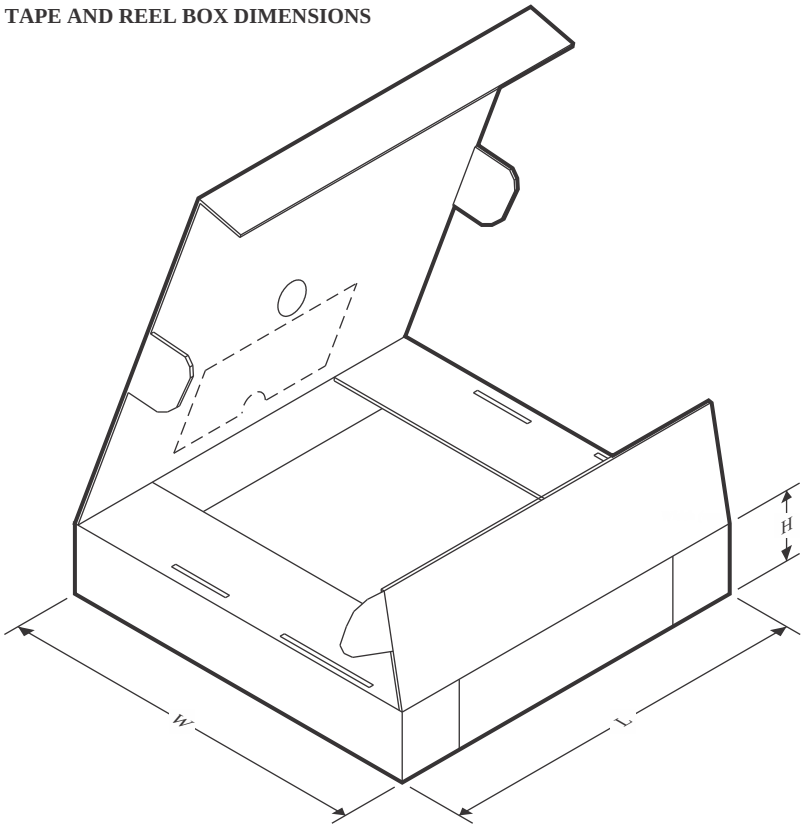
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2022AQDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022QDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2022AQDRG4Q1	SOIC	D	8	2500	353.0	353.0	32.0
TLE2022QDRG4Q1	SOIC	D	8	2500	353.0	353.0	32.0
TLE2022QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

GENERIC PACKAGE VIEW

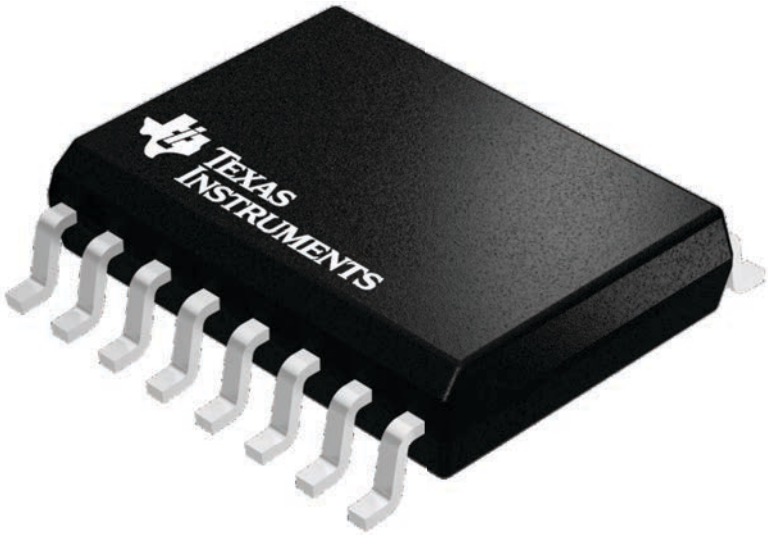
DW 16

SOIC - 2.65 mm max height

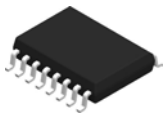
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

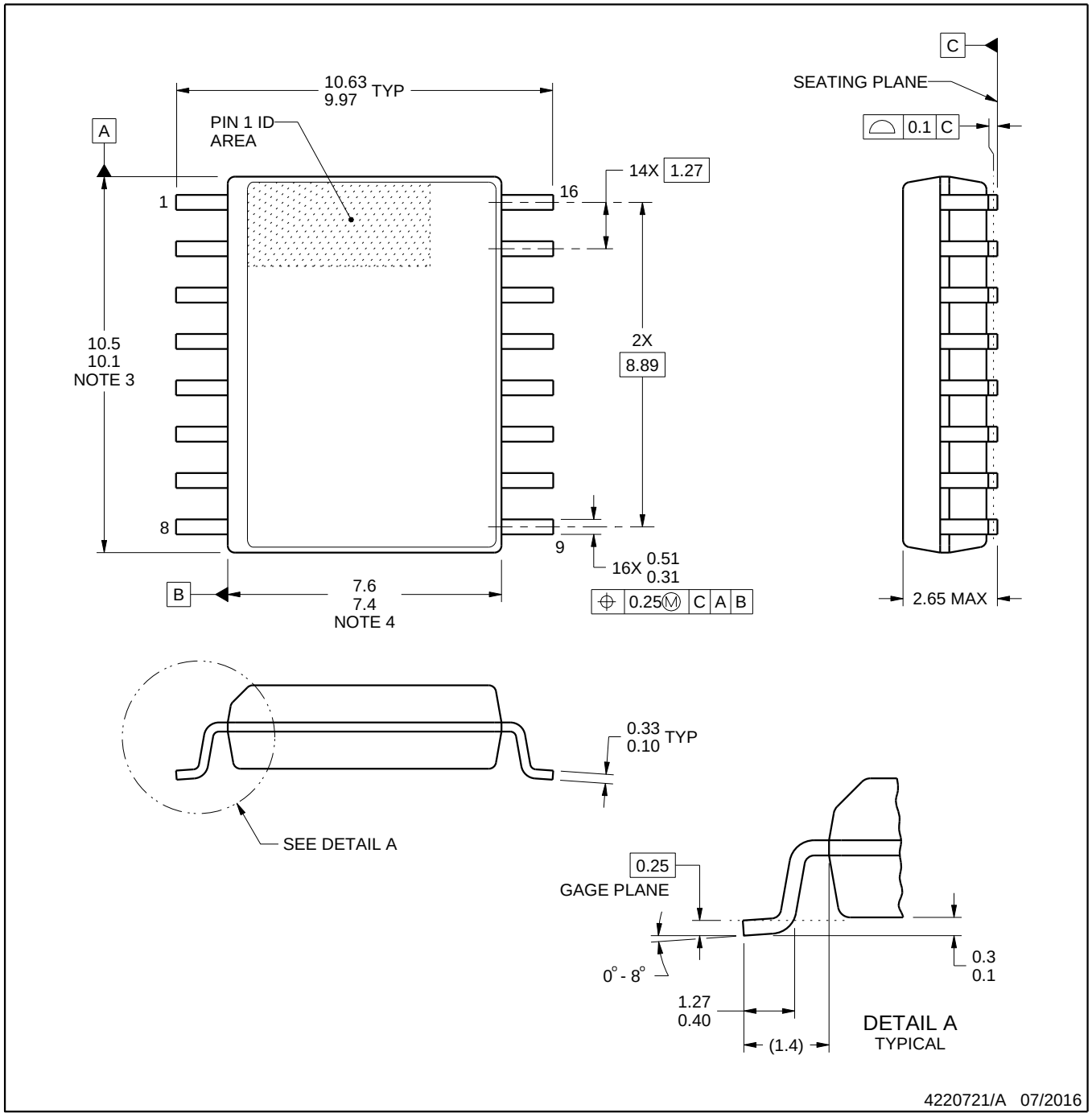


PACKAGE OUTLINE

DW0016A

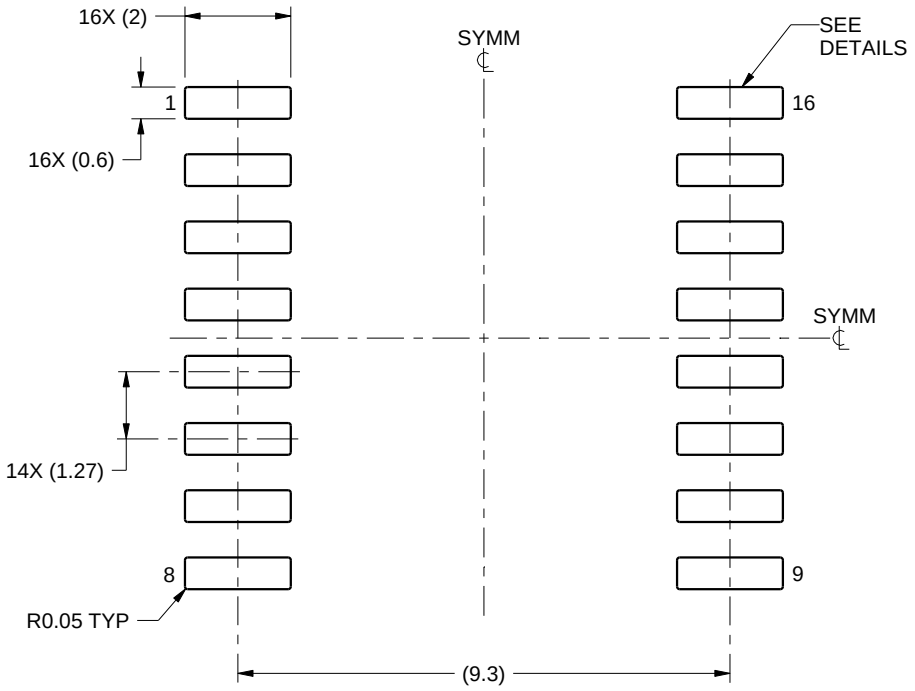
SOIC - 2.65 mm max height

SOIC

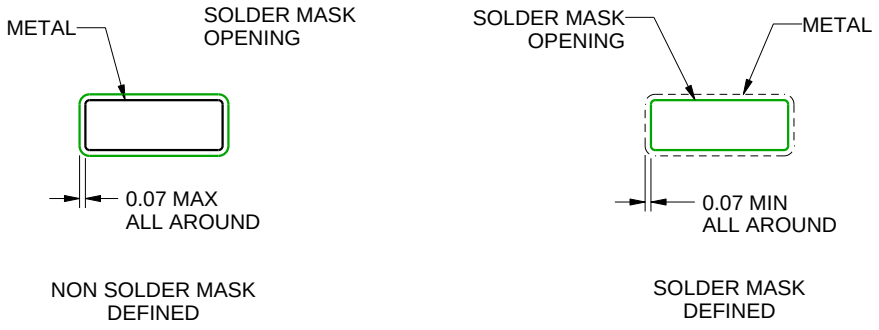


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

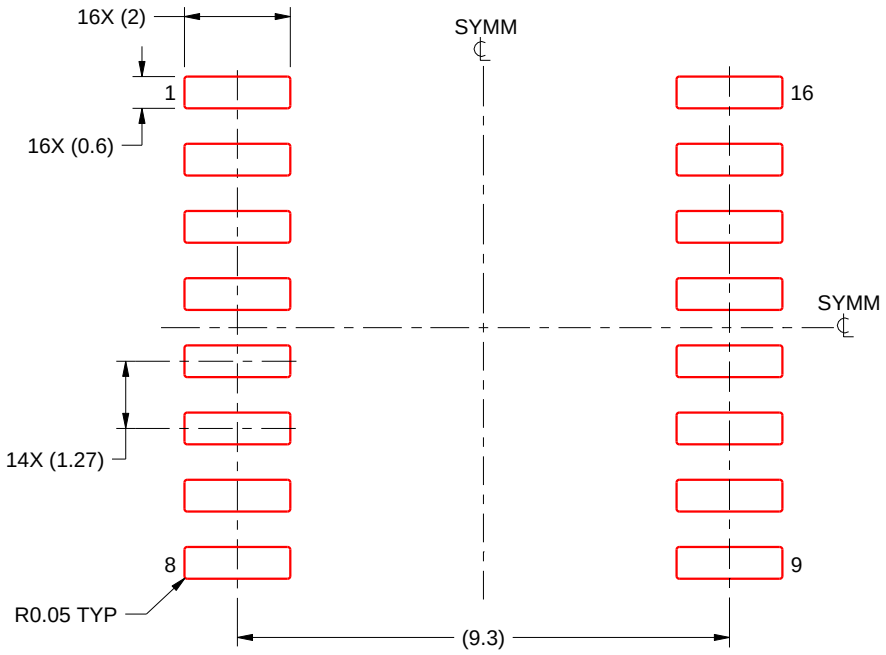


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

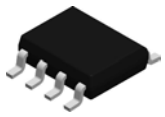


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

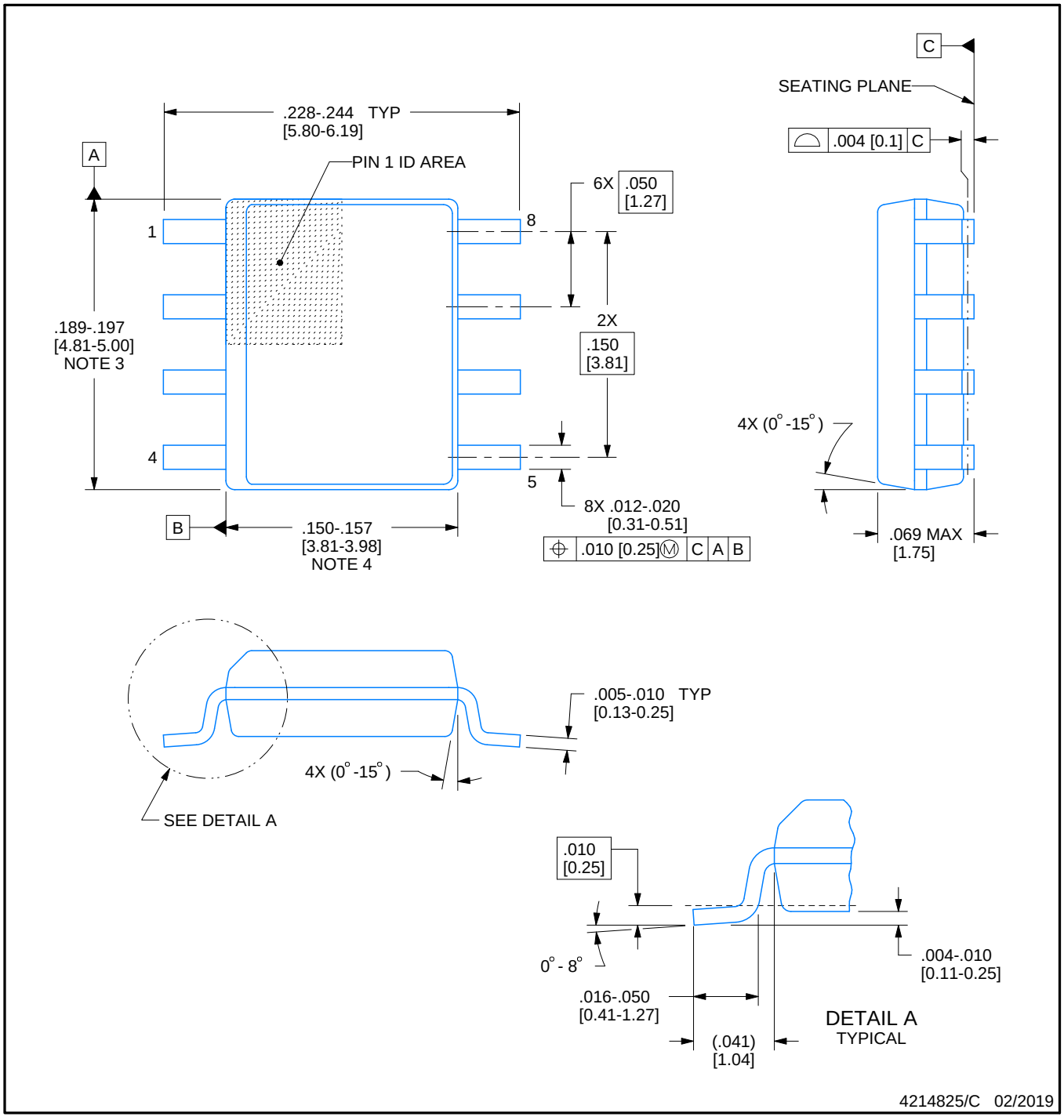


PACKAGE OUTLINE

D0008A

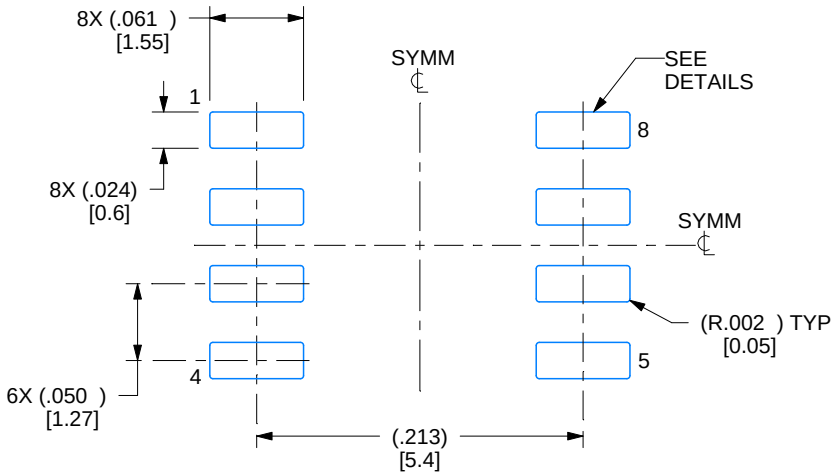
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

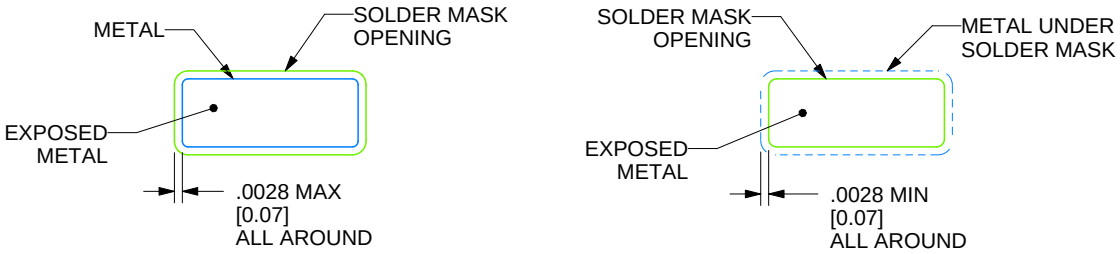


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

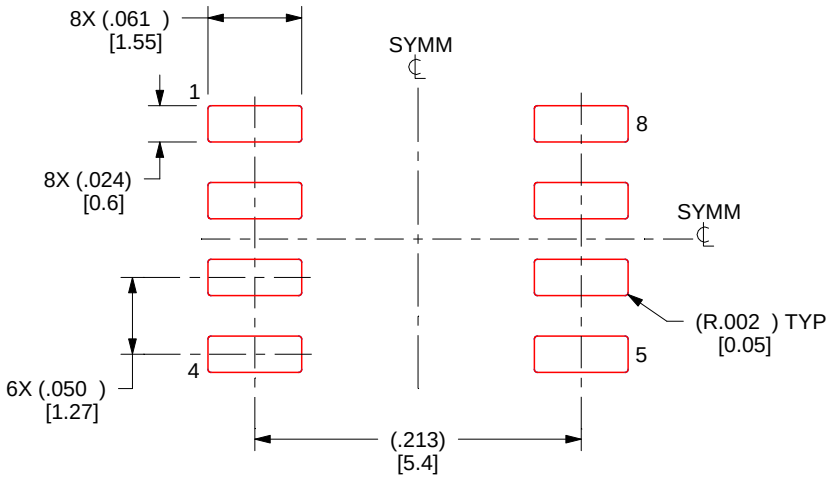
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025