

# TLV1812-EP and TLV1822-EP Enhanced Product 40V Rail-to-Rail Input Comparators with Push-Pull and Open-Drain Outputs

## 1 Features

- VID: V62/24628-01XE (TLV1812-EP)
- VID: V62/24628-02XE (TLV1822-EP)
- Supports Defense and Aerospace Applications
  - Controlled baseline
  - One fabrication site
  - One assembly/test site
  - Extended product life cycle
  - Product traceability
- Extended temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Wide supply range: 2.4V to 40V
- Rail-to-rail input
- Power-On Reset (POR) for known start-up
- Low input offset voltage:  $500\mu\text{V}$
- 420ns typical propagation delay
- Low quiescent current:  $5\mu\text{A}$  per channel
- Low input bias current:  $150\text{fA}$
- Push-pull output option (TLV1812-EP)
- Open-drain output option (TLV1822-EP)

## 2 Applications

- [Airborne BMS](#)
- [Airborne Radar](#)
- [Aircraft Cockpit Display](#)

## 3 Description

The TLV1812-EP and TLV1822-EP are 40V dual channel comparators with multiple output options. The family offers rail to-rail inputs with push-pull

or open-drain output options. These devices also have an excellent speed-to-power combination with a propagation delay of 420ns with a full supply voltage range of 2.4V to 40V and a quiescent supply current of only  $5\mu\text{A}$  per channel.

All devices include a Power-On Reset (POR) feature. This makes sure the output is in a known state until the minimum supply voltage has been reached before the output responds to the inputs, thus preventing false outputs during system power-up and powerdown.

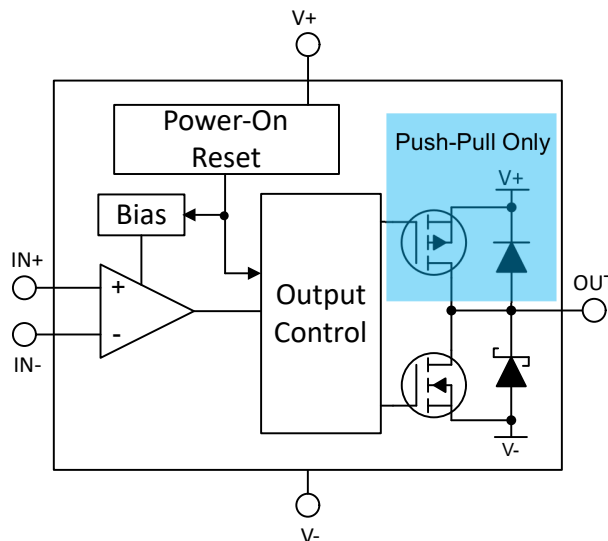
The TLV1812-EP device has a push-pull output stage capable of sinking and sourcing milliamps of current when controlling an LED or driving a capacitive load such as a MOSFET gate. The TLV1822-EP device has an open-drain output stage that can be pulled up to 40V independent of comparator supply voltage.

These comparators are available in the SOT23-8 packages and are specified for the extended temperature range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TLV1812-EP	DDF (SOT-23, 8)	2.9mm × 2.8mm
TLV1822-EP		

- (1) For all available packages, see [Section 10](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



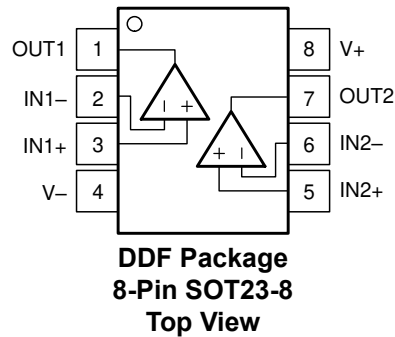
TLV18x2-EP Block Diagram



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## Pin Configuration and Functions



**Table 4-1. Pin Functions: TLV1812-EP and TLV1822-EP**

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Output pin of the comparator 1
IN1-	2	I	Inverting input pin of comparator 1
IN1+	3	I	Noninverting input pin of comparator 1
V-	4	—	Negative (low) supply
IN2+	5	I	Noninverting input pin of comparator 2
IN2-	6	I	Inverting input pin of comparator 2
OUT2	7	O	Output pin of the comparator 2
V+	8	—	Positive supply

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage: $V_S = (V+) - (V-)$	-0.3	42	V
Input pins (IN+, IN-) from (V-) <sup>(2)</sup>	-0.3	(V+) + 0.3	V
Current into Input pins (IN+, IN-)	-10	10	mA
Output (OUT) voltage (Open-Drain) from (V-) <sup>(3)</sup>	-0.3	42	V
Output (OUT) voltage (Push-Pull) from (V-)	-0.3	(V+) + 0.3	V
Output (OUT) current <sup>(4) (5) (6)</sup>	-10	10	mA
Junction temperature, $T_J$		150	°C
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Input terminals are diode-clamped to (V-). Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less.
- (3) Output (OUT) for open drain can be greater than (V+) and inputs (IN+, IN-) as long as within the -0.3V to 42V range
- (4) The output is diode-clamped to (V-) for both output options, and diode clamped to (V+) for the push-pull output option. The open drain version does not have a clamp to V+. Please see the *Outputs* and *ESD Protection* section of the *Application Information* Section for more information.
- (5) Output sinking and sourcing current is internally limited to <35mA when operating within the Absolute Maximum output voltage limits. The Absolute Maximum Output Current limit specified here is the maximum current through the clamp structure when exceeding the supply voltage below (V-) for both output options, or above (V+) for the push-pull option.
- (6) Short-circuit from output to (V-) or (V+). Continuous output short circuits at elevated supply voltages can result in excessive heating and exceeding the maximum allowed junction temperature, leading to eventual device destruction.

### 4.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500
			V

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage: $V_S = (V+) - (V-)$		2.4	40	V
Input voltage range from (V-)		-0.2	(V+) + 0.2	V
Output voltage range from (V-)	Open Drain	-0.2	40	V
Output voltage range from (V-)	Push Pull	-0.2	(V+) + 0.2	V
Ambient temperature, $T_A$	Ambient temperature, $T_A$	-55	125	°C

## 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLV18x2-EP	UNIT
		DDF (SOT-23)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	90.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	88.1	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	7.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	87.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) report.

## 4.5 Electrical Characteristics

For  $V_S$  (Total Supply Voltage) =  $(V+) - (V-) = 12V$ ,  $V_{CM} = V_S / 2$  at  $T_A = 25^\circ C$  (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage		-3	±0.5	3	mV
$V_{OS}$	Input offset voltage	$T_A = -55^\circ C$ to $+125^\circ C$	-4		4	mV
$dV_{IO}/dT$	Input offset voltage drift	$T_A = -55^\circ C$ to $+125^\circ C$		±1.2		$\mu V/^\circ C$
CMRR	Common mode rejection ratio	$V_S = (V-) \text{ to } (V+)$ , Rail to Rail		90		dB
PSRR	Power supply rejection ratio	$V_S = 2.4V \text{ to } 40V$ , $V_{CM} = (V-)$		100		dB
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent current per comparator, No Load	Output Low, $T_A = 25^\circ C$		6	7.5	$\mu A$
		No Load, Output Low $T_A = -55^\circ C$ to $+125^\circ C$			8.5	$\mu A$
		Output High, $T_A = 25^\circ C$		7	9	$\mu A$
		No Load, Output High $T_A = -55^\circ C$ to $+125^\circ C$			10	$\mu A$
$V_{POR}$	Power On Reset Voltage			1.7		V
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current			150		fA
$I_B$	Input bias current	$T_A = -55^\circ C$ to $+125^\circ C$	-1.2		1.2	nA
$I_{OS}$	Input offset current			10		fA
<b>INPUT CAPACITANCE</b>						
$C_{ID}$	Input Capacitance, Differential			2		pF
$C_{IC}$	Input Capacitance, Common Mode			8		pF
<b>INPUT COMMON MODE RANGE</b>						
$V_{CM-Range}$	Common-mode voltage range	$V_S = 2.4V \text{ to } 40V$ $T_A = -55^\circ C$ to $+125^\circ C$	$(V-) - 0.2$		$(V+) + 0.2$	V
<b>OUTPUT</b>						
$V_{OL}$	Voltage swing from $(V-)$	$I_{SINK} = 4mA$ $T_A = -55^\circ C$ to $+125^\circ C$			250	mV
$V_{OH}$	Voltage swing from $(V+)$ (for Push-Pull only)	$I_{SOURCE} = 4mA$ $T_A = -55^\circ C$ to $+125^\circ C$			250	mV
$I_{LKG}$	Open-drain output leakage current	$V_{ID} = +0.1V$ , $V_{PULLUP} = (V+)$ $T_A = -55^\circ C$ to $+125^\circ C$		0.1	20	nA
$I_{OL}$	Short-circuit current	Sinking	15	30		mA
$I_{OH}$	Short-circuit current	Sourcing (for Push-Pull only)	15	30		mA

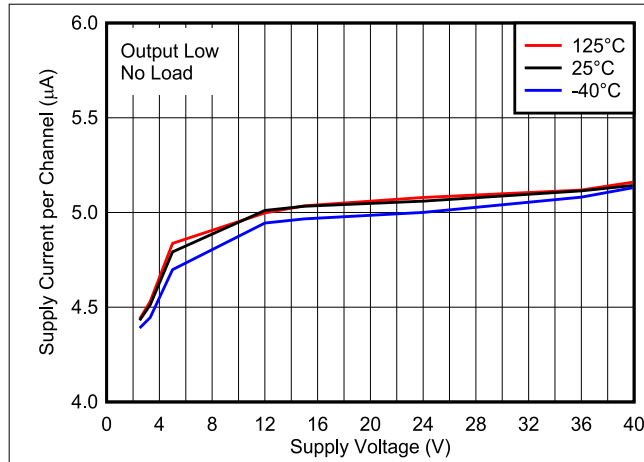
## 4.6 Switching Characteristics

For  $V_S$  (Total Supply Voltage) =  $(V+) - (V-)$  = 12V,  $V_{CM} = V_S / 2$  at  $T_A = 25^\circ\text{C}$  (Unless otherwise noted)

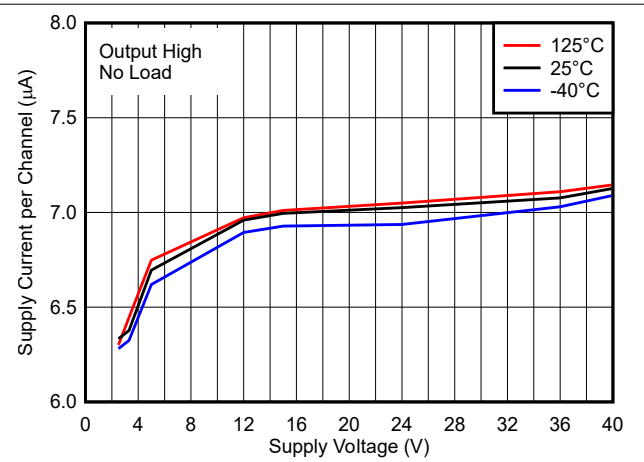
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT</b>						
$T_{PD-HL}$	Propagation delay time, high-to-low	$V_{OD} = 10\text{mV}$ , $C_L = 50\text{pF}$		900		ns
$T_{PD-HL}$	Propagation delay time, high-to-low	$V_{OD} = 100\text{mV}$ , $C_L = 50\text{pF}$		450		ns
$T_{PD-LH}$	Propagation delay time, low-to-high, push-pull output	$V_{OD} = 10\text{mV}$ , $C_L = 50\text{pF}$		900		ns
$T_{PD-LH}$	Propagation delay time, low-to-high, push-pull output	$V_{OD} = 100\text{mV}$ , $C_L = 50\text{pF}$		420		ns
$T_{RISE}$	Output Rise Time, 20% to 80%, push-pull output	$C_L = 50\text{pF}$		15		ns
$T_{FALL}$	Output Fall Time, 80% to 20%	$C_L = 50\text{pF}$		15		ns
$F_{TOGGLE}$	Toggle Frequency	$V_{ID} = 100\text{mV}$ , $C_L = 50\text{pF}$		500		kHz
<b>POWER ON TIME</b>						
$P_{ON}$	Power on-time			200		$\mu\text{s}$

## 5 Typical Characteristics

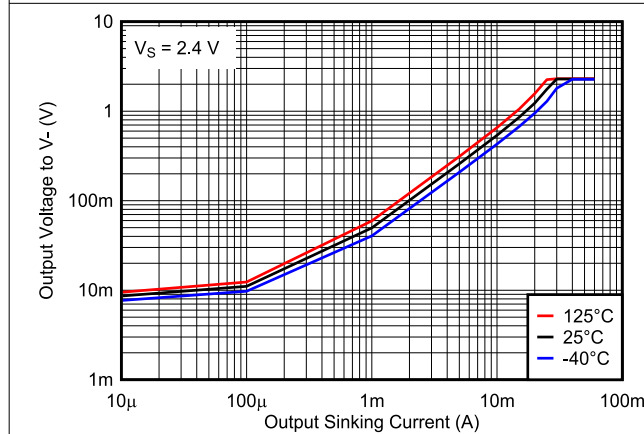
$T_A = 25^\circ\text{C}$ ,  $V_S = 12\text{V}$ ,  $R_{\text{PULLUP}} = 2.5\text{k}$ ,  $C_L = 20\text{pF}$ ,  $V_{\text{CM}} = 0\text{V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{mV}$  unless otherwise noted.



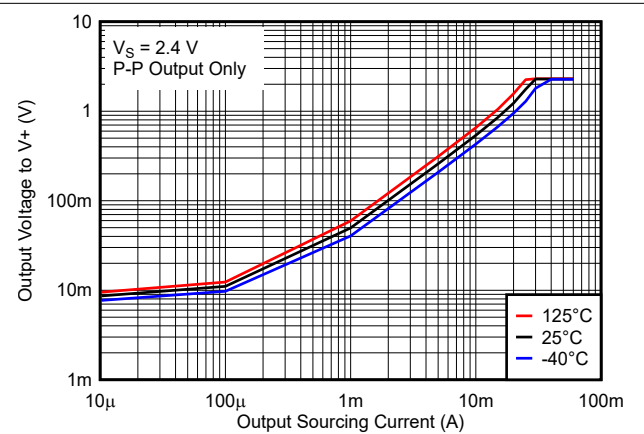
**Figure 5-1. Supply Current per Channel vs. Supply Voltage, Output Low**



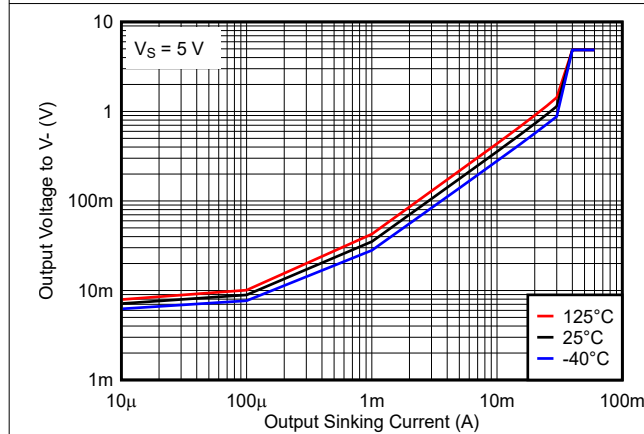
**Figure 5-2. Supply Current per Channel vs. Supply Voltage, Output High**



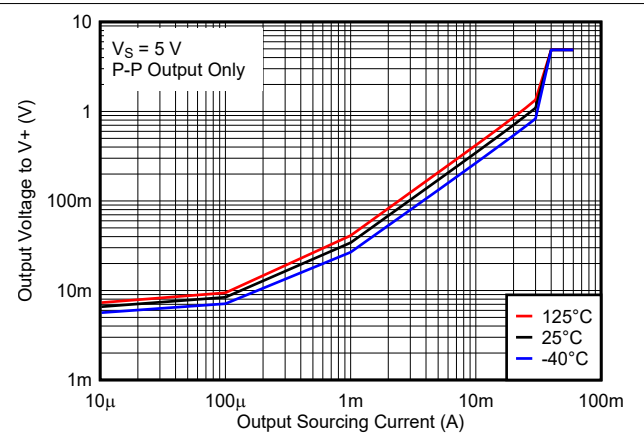
**Figure 5-3. Output Voltage vs. Output Sinking Current, 2.4V**



**Figure 5-4. Output Voltage vs. Output Sourcing Current, 2.4V**



**Figure 5-5. Output Voltage vs. Output Sinking Current, 5V**



**Figure 5-6. Output Voltage vs. Output Sourcing Current, 5V**

## 5 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_S = 12\text{V}$ ,  $R_{\text{PULLUP}} = 2.5\text{k}$ ,  $C_L = 20\text{pF}$ ,  $V_{\text{CM}} = 0\text{V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{mV}$  unless otherwise noted.

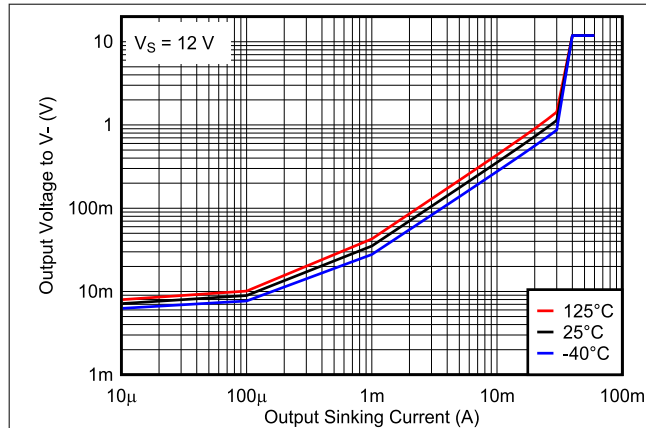


Figure 5-7. Output Voltage vs. Output Sinking Current, 12V

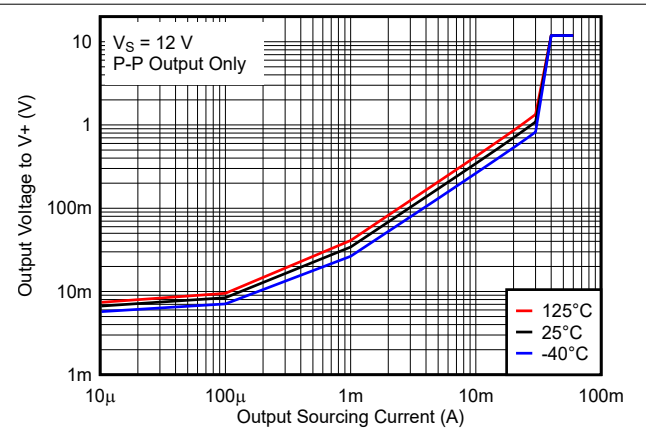


Figure 5-8. Output Voltage vs. Output Sourcing Current, 12V

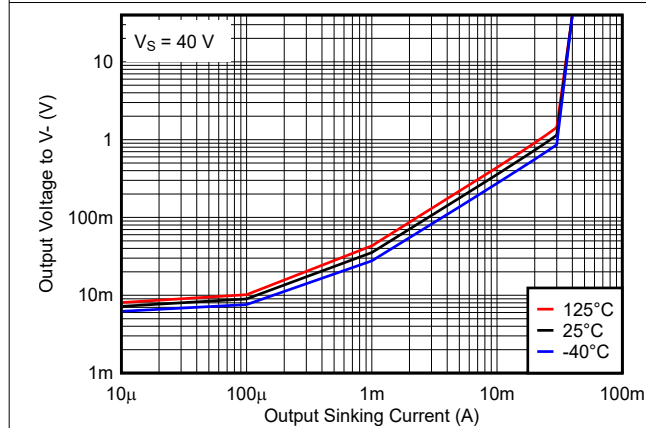


Figure 5-9. Output Voltage vs. Output Sinking Current, 40V

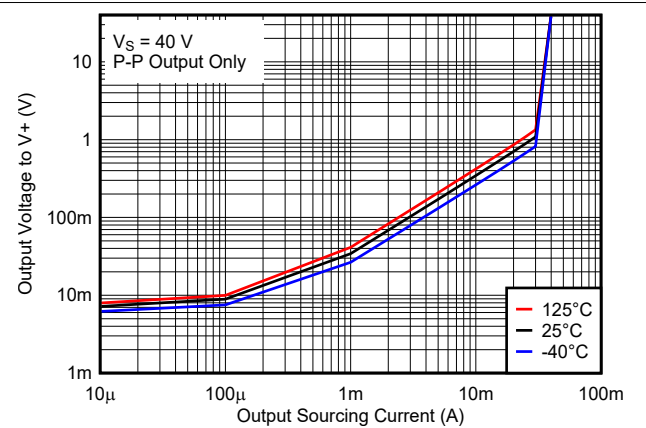


Figure 5-10. Output Voltage vs. Output Sourcing Current, 40V

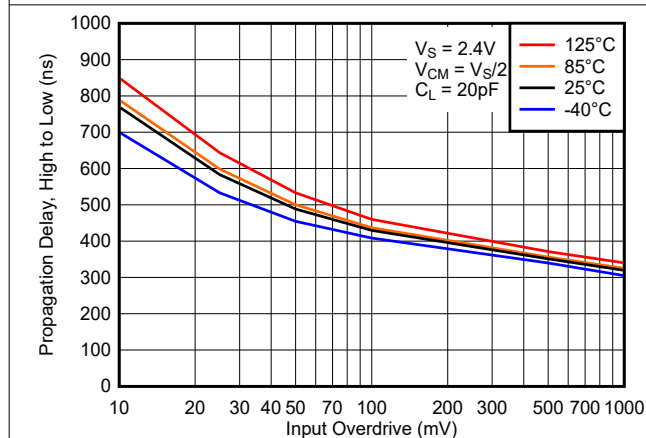


Figure 5-11. Propagation Delay, High to Low, 2.4V

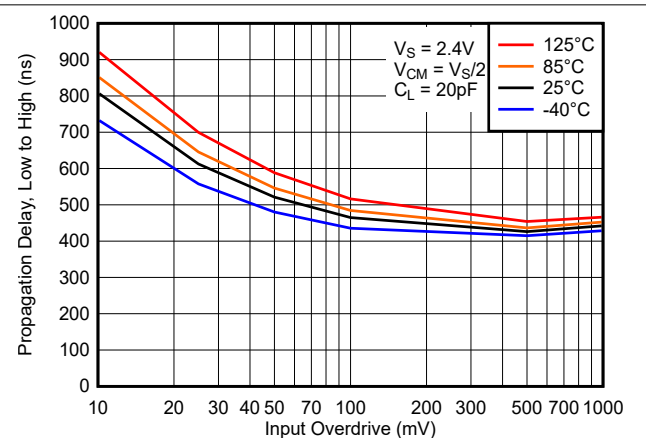


Figure 5-12. Propagation Delay, Low to High, 2.4V

## 5 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_S = 12\text{V}$ ,  $R_{\text{PULLUP}} = 2.5\text{k}$ ,  $C_L = 20\text{pF}$ ,  $V_{\text{CM}} = 0\text{V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{mV}$  unless otherwise noted.

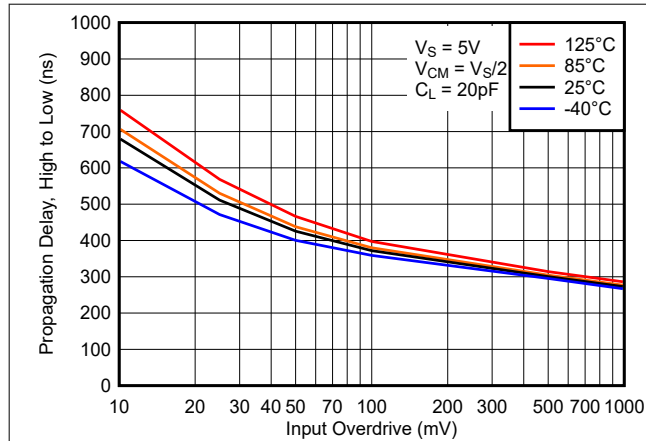


Figure 5-13. Propagation Delay, High to Low, 5V

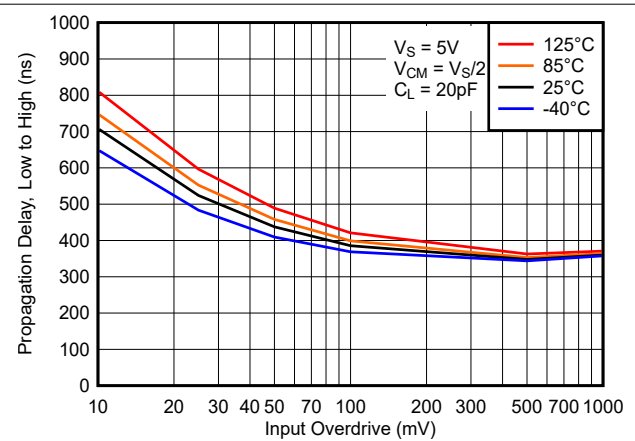


Figure 5-14. Propagation Delay, Low to High, 5V

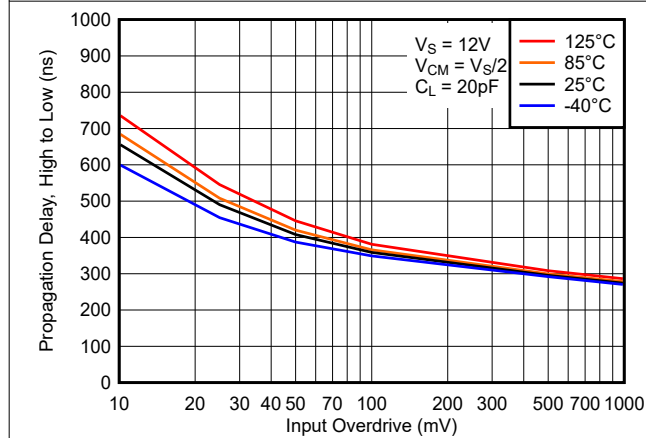


Figure 5-15. Propagation Delay, High to Low, 12V

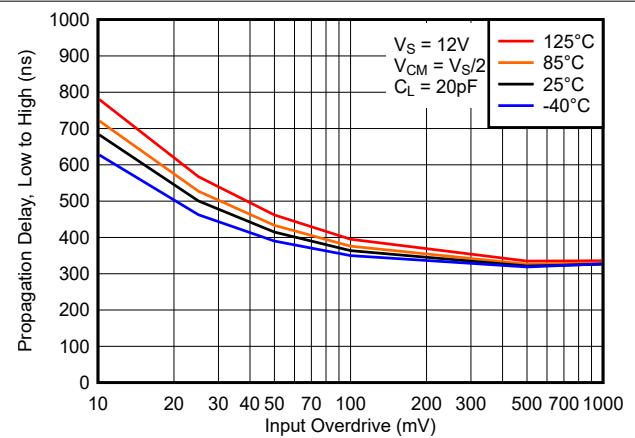


Figure 5-16. Propagation Delay, Low to High, 12V

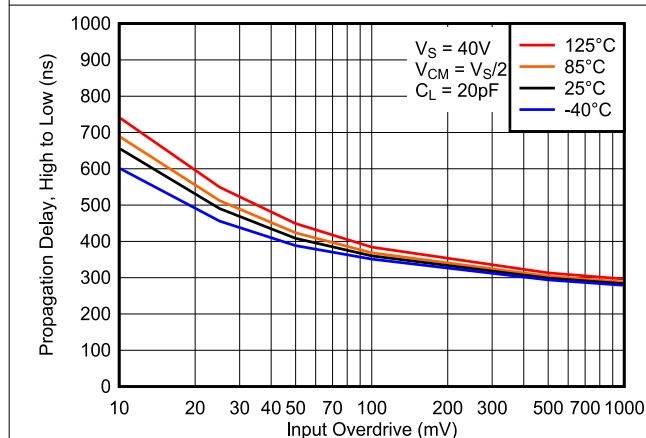


Figure 5-17. Propagation Delay, High to Low, 40V

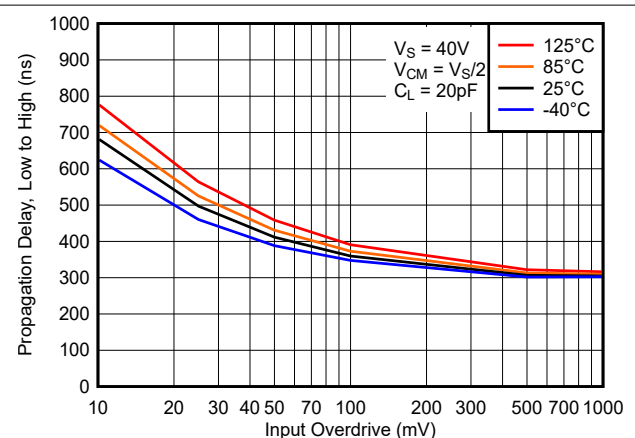


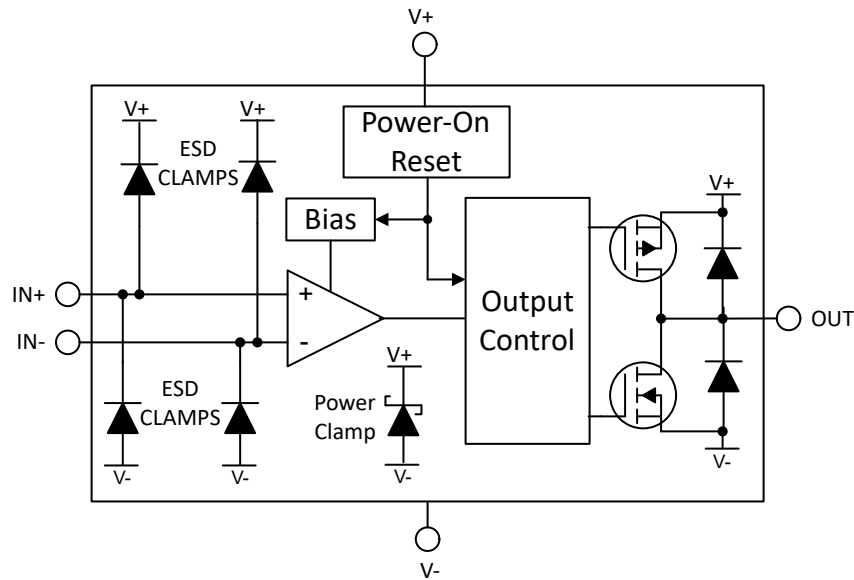
Figure 5-18. Propagation Delay, Low to High, 40V

## 6 Detailed Description

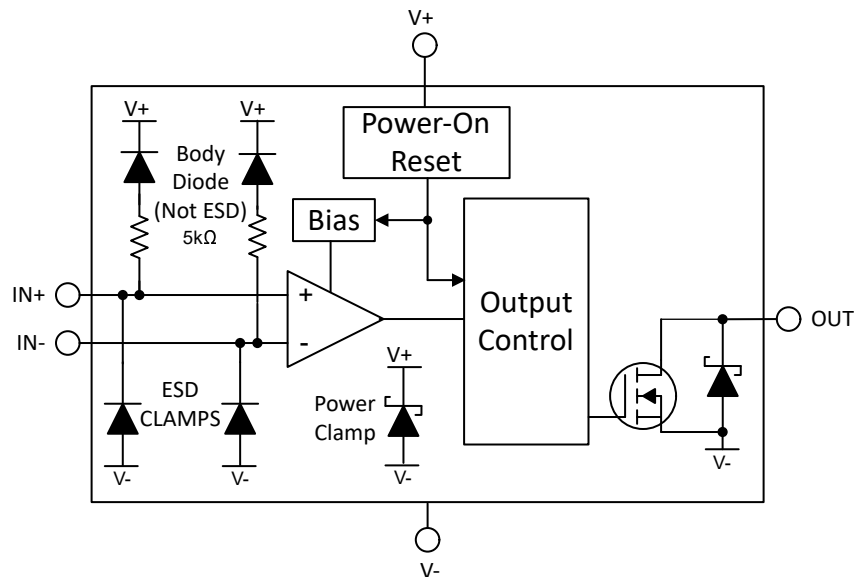
### 6.1 Overview

The TLV181x-EP and TLV182x-EP devices are micro-power comparators with push-pull and open-drain output options. Operating down to  $-55^{\circ}\text{C}$  while only consuming only  $5\mu\text{A}$  per channel, the TLV181x-EP and TLV182x-EP are well suited for power conscious systems and supply monitoring applications. An internal power-on reset circuit places the output in a known state during power-up and power-down.

### 6.2 Functional Block Diagrams



**Figure 6-1. TLV1812-EP Block Diagram**



**Figure 6-2. TLV1822-EP Block Diagram**

## 6.3 Feature Description

### TLV18x2-EP Family Options

The TLV18x2-EP family features 40V operation, micro-power 5 $\mu$ A supply currents, 420ns propagation delay, and a Power-On Reset (POR) function.

The TLV1812-EP has a **push-pull** (sink-source) output.

The TLV1822-EP has a **open-drain** (sink only) output, capable of being pulled-up to any voltage up to 40V, independent of comparator supply voltage.

## 6.4 Device Functional Modes

### 6.4.1 Inputs

#### 6.4.1.1 TLV18x2-EP Rail-to-Rail Input

The TLV18x2-EP input voltage range extends from 200mV below V<sub>-</sub> to 200mV above V<sub>+</sub>. The differential input voltage (V<sub>ID</sub>) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input voltages stay within the specified range.

For the TLV1812-EP (Push-Pull), the inputs have ESD clamps to the V<sub>+</sub> supply line and therefore the input voltages must not exceed the supply voltages by more than 200mV. Do not apply signals to the rail to rail inputs with no supply voltage.

For the TLV1822-EP (Open-Drain), the inputs have weak clamps to the V<sub>+</sub> supply line. Do not apply signals to the rail to rail inputs with no supply voltage.

#### 6.4.1.2 ESD Protection

The TLV1822-EP open-drain output ESD protection consists of a snapback ESD clamp between the output and V<sub>-</sub> to allow the output to be pulled above V<sub>+</sub> to a maximum of 40V. There is a "lower" ESD clamp between V<sub>-</sub> and the inputs. There are also a parasitic "upper" ESD soft-clamp diode between the input and V<sub>+</sub> with a 5k $\Omega$  equivalent resistance (as shown in Figure 5-2). These clamps are not traditional ESD cells thus current must be limited to 1mA or less across the this upper diode and resistance. External diode clamping is recommended if the input voltage exceeds V<sub>+</sub> during operation.

The TLV1812-EP push-pull output ESD protection contains a conventional diode-type "upper" ESD clamp between the output and V<sub>+</sub>, and a "lower" ESD clamp between the output and V<sub>-</sub>. The output must not exceed the supply rails by more than 200mV.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any currents when the clamps conduct. The current must be limited 10mA or less, though TI recommends limiting the current to 1mA or less. This series resistance can be part of any resistive input dividers or networks.

#### 6.4.1.3 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency chatter as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V<sub>+</sub> (as long as the input is directly connected to the V<sub>+</sub> pin to avoid transients).

### 6.4.2 Outputs

#### 6.4.2.1 TLV1812-EP Push-Pull Output

The TLV1812-EP features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the opposite supply rail ( $V+$  when output "low" or  $V-$  when output "High") can result in thermal runaway and eventual device destruction at high ( $>12V$ ) supply voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output.

#### 6.4.2.2 TLV1822-EP Open-Drain Output

The TLV1822-EP features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from  $0V$  up to  $40V$ , independent of the comparator supply voltage ( $V+$ ). The open-drain output allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between  $100\mu A$  and  $1mA$ . Lower value pull-up resistor values help increase the rising edge rise-time, but at the expense of increasing  $V_{OL}$  and higher power dissipation. The rise-time is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors ( $>1M\Omega$ ) creates an exponential rising edge due to the output RC time constant and increase the rise-time.

Directly shorting the output to  $V+$  can result in thermal runaway and eventual device destruction at high ( $>12V$ ) pull-up voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

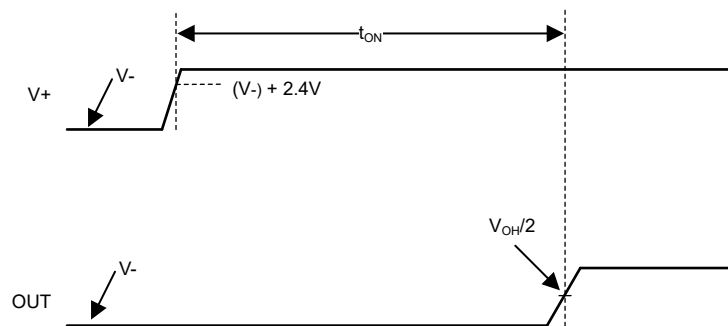
Unused open drain outputs can be left floating, or can be tied to the  $V-$  pin if floating pins are not desired.

#### 6.4.3 Power-On Reset (POR)

The TLV18x2-EP family has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply ( $V+$ ) is ramping up or ramping down, the POR circuitry is activated for up to  $200\mu s$  after the minimum supply voltage threshold of  $2.4V$  is crossed, or immediately when the supply voltage drops below  $2.4V$ . When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input ( $V_{ID}$ ).

**For the TLV1812-EP push-pull output devices, the output is held low during the POR period ( $t_{on}$ ).**

**For the TLV1822-EP open drain output option the POR circuit keeps the output high impedance (Hi-Z) during the POR period ( $t_{on}$ ).**



**Figure 6-3. Power-On Reset Timing Diagram**

Note: The output voltage rises with the pull-up voltage during the POR period.

#### 6.4.4 Hysteresis

The TLV18x2-EP family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, there is a possibility for the output to "chatter" when the absolute differential voltage is near zero as the comparator triggers on its own internal wideband noise. This is normal comparator behavior and is expected. TI recommends that the user add external hysteresis if slow moving signals are expected. See [Section 7.1.2](#) in the following section.

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 7.1 Application Information

#### 7.1.1 Basic Comparator Definitions

##### 7.1.1.1 Operation

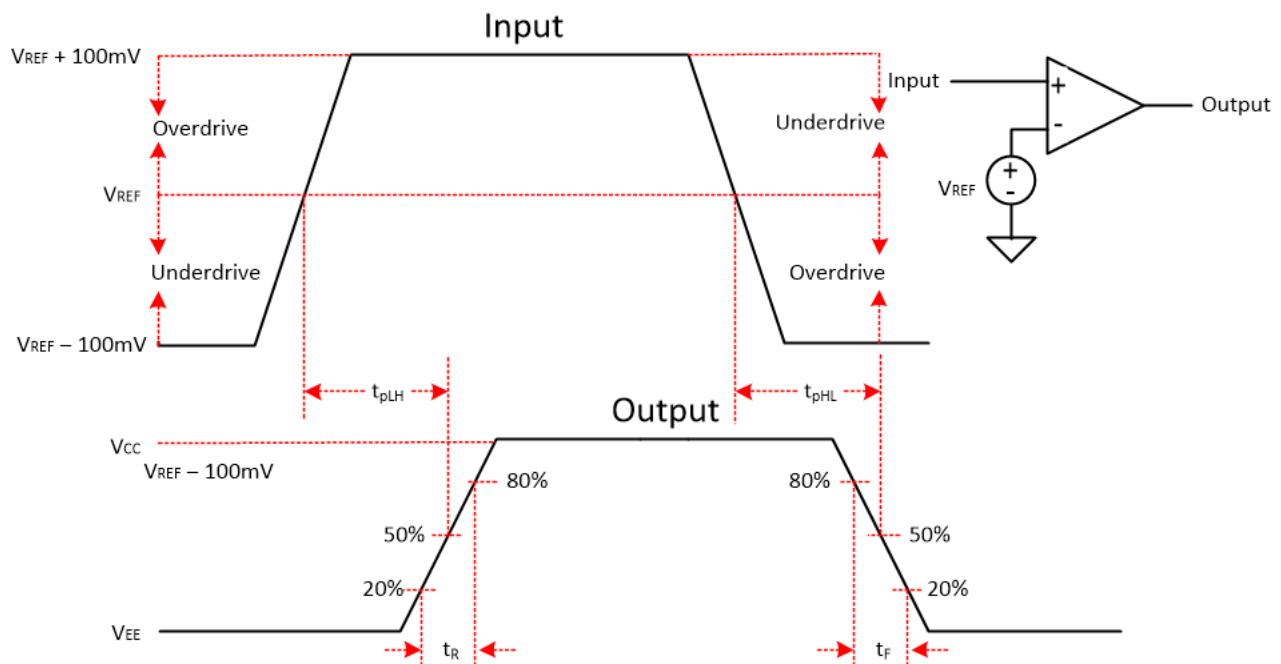
The basic comparator compares the input voltage ( $V_{IN}$ ) on one input to a reference voltage ( $V_{REF}$ ) on the other input. In the [Figure 7-1](#) example below, if  $V_{IN}$  is less than  $V_{REF}$ , the output voltage ( $V_O$ ) is logic low ( $V_{OL}$ ). If  $V_{IN}$  is greater than  $V_{REF}$ , the output voltage ( $V_O$ ) is at logic high ( $V_{OH}$ ). [Table 7-1](#) summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

**Table 7-1. Output Conditions**

Inputs Condition	Output
$IN+ > IN-$	HIGH ( $V_{OH}$ )
$IN+ = IN-$	Indeterminate (chatters - see <a href="#">Hysteresis</a> )
$IN+ < IN-$	LOW ( $V_{OL}$ )

##### 7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as  $t_{pLH}$  and  $t_{pHL}$  in [Figure 7-1](#) and is measured from the mid-point of the input to the midpoint of the output. Likewise, propagation varies with what is called Overdrive (VOD) and Underdrive (VUD) voltage levels (see section below).



**Figure 7-1. Comparator Timing Diagram**

### 7.1.1.3 Overdrive and Underdrive Voltage

The overdrive voltage,  $V_{OD}$ , is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the [Figure 7-1](#) example. The overdrive voltage can influence the propagation delay ( $t_p$ ). The smaller the overdrive voltage, the longer the propagation delay, particularly when  $<100\text{mV}$ . If the fastest speeds are desired, apply the highest amount of overdrive possible. Contrary to overdrive voltage, larger underdrive voltage causes  $t_p$  to increase. This is particularly important in applications where rail-to-rail input swings are present at the comparator inputs. The result can be skewed propagation delay (difference between  $t_{pLH}$  and  $t_{pHL}$ ). As a low power comparator, use of this comparator family is not recommended if variation in propagation delay is critical.

The risetime ( $t_r$ ) and falltime ( $t_f$ ) is the time from the 20% and 80% points of the output waveform.

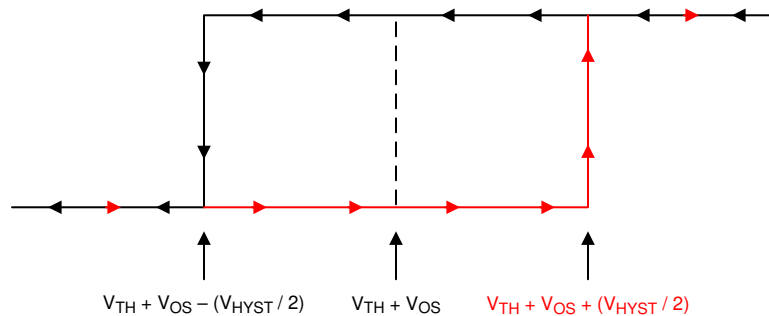
### 7.1.2 Hysteresis

The basic comparator configuration can oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This typically occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in [Figure 7-2](#). This curve is a function of three components:  $V_{TH}$ ,  $V_{OS}$ , and  $V_{HYST}$ :

- $V_{TH}$  is the actual set voltage or threshold trip voltage.
- $V_{OS}$  is the internal offset voltage between  $V_{IN+}$  and  $V_{IN-}$ . This voltage is added to  $V_{TH}$  to form the actual trip point at which the comparator must respond to change output states.
- $V_{HYST}$  is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

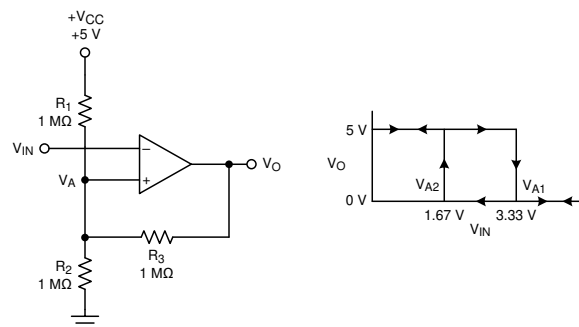


**Figure 7-2. Hysteresis Transfer Curve**

For more information, see the [Comparator with and without hysteresis circuit application note](#).

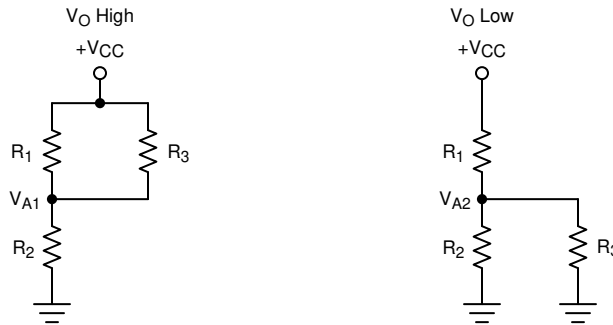
#### 7.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage ( $V_{CC}$ ), as shown in [Figure 7-3](#).



**Figure 7-3. TLV1812-EP in an Inverting Configuration With Hysteresis**

The equivalent resistor networks when the output is high and low are shown in [Figure 7-3](#).



**Figure 7-4. Inverting Configuration Resistor Equivalent Networks**

When  $V_{IN}$  is less than  $V_A$ , the output voltage is high (for simplicity, assume  $V_O$  switches as high as  $V_{CC}$ ). The three network resistors can be represented as  $R1 \parallel R3$  in series with  $R2$ , as shown in [Figure 7-4](#).

[Equation 1](#) below defines the high-to-low trip voltage ( $V_{A1}$ ).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When  $V_{IN}$  is greater than  $V_A$ , the output voltage is low. In this case, the three network resistors can be presented as  $R2 \parallel R3$  in series with  $R1$ , as shown in [Equation 2](#).

Use [Equation 2](#) to define the low to high trip voltage ( $V_{A2}$ ).

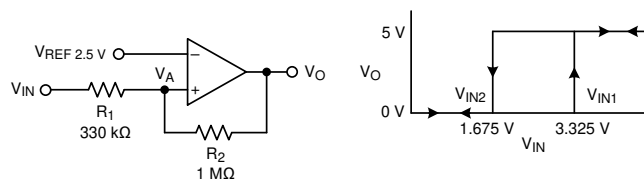
$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

[Equation 3](#) defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

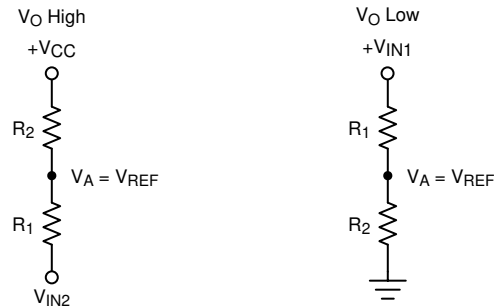
### 7.1.2.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference ( $V_{REF}$ ) at the inverting input, as shown in [Figure 7-5](#).



**Figure 7-5. TLV1812-EP in a Non-Inverting Configuration With Hysteresis**

The equivalent resistor networks when the output is high and low are shown in [Figure 7-6](#).



**Figure 7-6. Non-Inverting Configuration Resistor Networks**

When  $V_{IN}$  is less than  $V_{REF}$ , the output is low. For the output to switch from low to high,  $V_{IN}$  must rise above the  $V_{IN1}$  threshold. Use [Equation 4](#) to calculate  $V_{IN1}$ .

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \quad (4)$$

When  $V_{IN}$  is greater than  $V_{REF}$ , the output is high. For the comparator to switch back to a low state,  $V_{IN}$  must drop below  $V_{IN2}$ . Use [Equation 5](#) to calculate  $V_{IN2}$ .

$$V_{IN2} = \frac{V_{REF} (R1 + R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between  $V_{IN1}$  and  $V_{IN2}$ , as shown in [Equation 6](#).

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$

For more information, see the [Inverting comparator with hysteresis circuit application note](#) and the [Non-Inverting Comparator With Hysteresis Circuit application note](#).

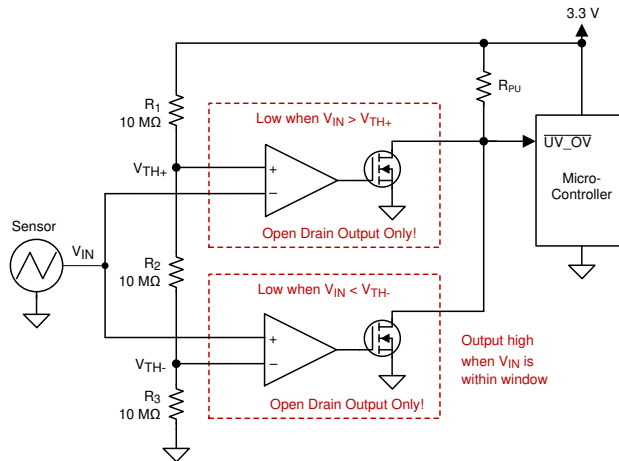
### 7.1.2.3 Inverting and Non-Inverting Hysteresis using Open-Drain Output

Using an open drain output device, such as the TLV1822-EP, is also possible but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as  $R2 + R_{PULLUP}$ . TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

## 7.2 Typical Applications

### 7.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. [Figure 7-7](#) shows a simple window comparator circuit. Window comparators require open drain outputs (TLV1822-EP) if the outputs are directly connected together.



**Figure 7-7. Window Comparator**

**7.2.1.1 Design Requirements**

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1V
- Alert (logic low output) when an input signal is greater than 2.2V
- Alert signal is active low
- Operate from a 3.3V power supply

**7.2.1.2 Detailed Design Procedure**

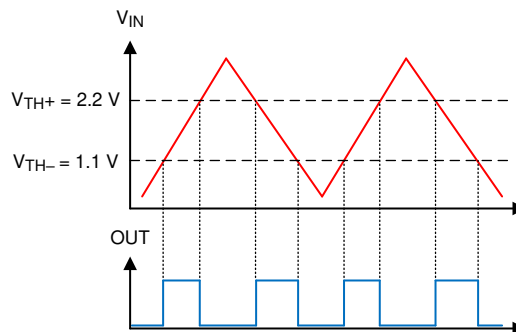
Configure the circuit as shown in [Figure 7-7](#). Connect  $V_{CC}$  to a 3.3V power supply and  $V_{EE}$  to ground. Make R1, R2 and R3 each 10MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator ( $V_{TH+}$  and  $V_{TH-}$ ).

With each resistor being equal,  $V_{TH+}$  is 2.2V and  $V_{TH-}$  is 1.1V. Large resistor values such as 10MΩ are used to minimize power consumption. The resistor values can be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs are low when the sensor is less than 1.1V or greater than 2.2V. The respective comparator outputs are high when the sensor is in the range of 1.1V to 2.2V (within the "window"), as shown in [Figure 7-8](#).

**7.2.1.3 Application Curve**

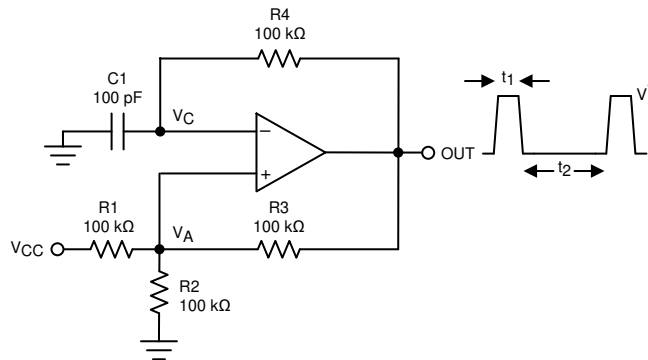


**Figure 7-8. Window Comparator Results**

For more information, see the [Window comparator circuit application note](#).

## 7.2.2 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source. A push-pull output (TLV1812-EP) is recommended for best symmetry.



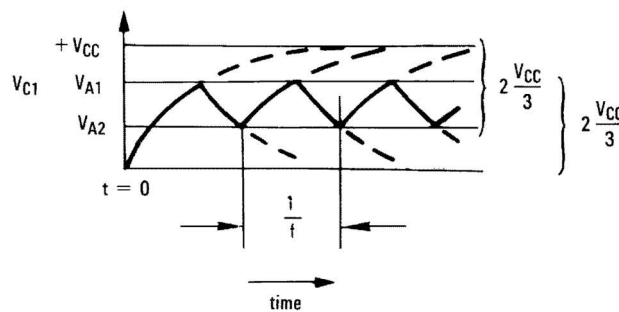
**Figure 7-9. Square-Wave Oscillator**

### 7.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor  $C_1$  and resistor  $R_4$ . The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which can help to reduce BOM cost and board space. TI recommends that  $R_4$  be over several kilo-ohms to minimize loading of the output.

### 7.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.



**Figure 7-10. Square-Wave Oscillator Timing Thresholds**

First consider the output of Figure [Figure 7-9](#) as high, which indicates the inverted input  $V_C$  is lower than the noninverting input ( $V_A$ ). This causes the  $C_1$  to be charged through  $R_4$ , and the voltage  $V_C$  increases until equal to the noninverting input. The value of  $V_A$  at the point is calculated by [Equation 7](#).

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \parallel R_3} \quad (7)$$

if  $R_1 = R_2 = R_3$ , then  $V_{A1} = 2V_{CC} / 3$

At this time the comparator output trips pulling down the output to the negative rail. The value of  $V_A$  at this point is calculated by [Equation 8](#).

$$V_{A2} = \frac{V_{CC}(R_2 \parallel R_3)}{R_1 + R_2 \parallel R_3} \quad (8)$$

if  $R_1 = R_2 = R_3$ , then  $V_{A2} = V_{CC}/3$

The  $C_1$  now discharges through the  $R_4$ , and the voltage  $V_{CC}$  decreases until reaching  $V_{A2}$ . At this point, the output switches back to the starting state. The oscillation period equals to the time duration for  $C_1$  from  $2V_{CC}/3$  to  $V_{CC}/3$  then back to  $2V_{CC}/3$ , which is given by  $R_4 C_1 \times \ln 2$  for each trip. Therefore, the total time duration is calculated as  $2 R_4 C_1 \times \ln 2$ .

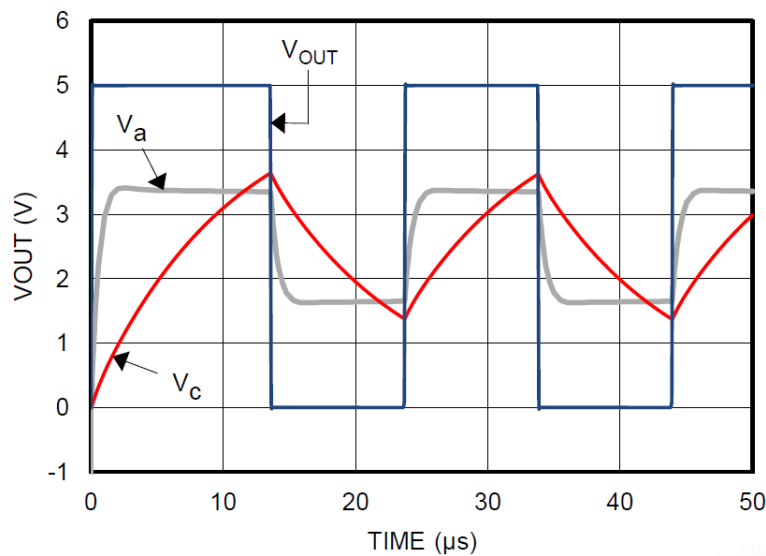
The oscillation frequency can be obtained by [Equation 9](#):

$$f = 1 / (2 R_4 \times C_1 \times \ln 2) \quad (9)$$

### 7.2.2.3 Application Curve

[Figure 7-11](#) shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100\text{k}\Omega$
- $C_1 = 100\text{pF}$ ,  $C_L = 20\text{pF}$
- $V_+ = 5\text{V}$ ,  $V_- = \text{GND}$
- $C_{\text{stray}}$  (not shown) from  $V_A$  TO GND =  $10\text{pF}$

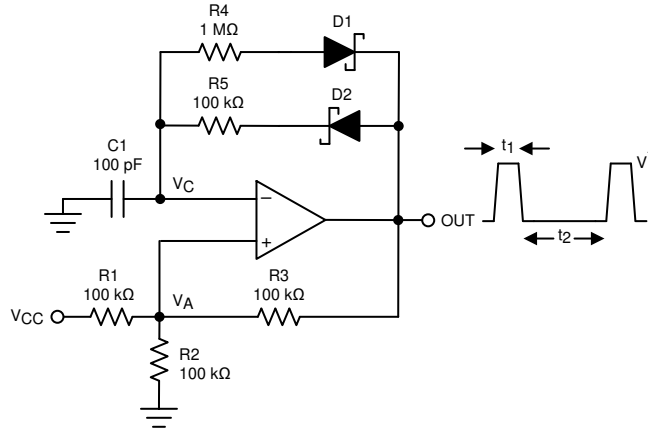


**Figure 7-11. Square-Wave Oscillator Output Waveform**

### 7.2.3 Adjustable Pulse Width Generator

[Figure 7-12](#) is a variation of the square wave oscillator (see [Figure 7-9](#)) that allows adjusting the pulse widths.

$R_4$  and  $R_5$  provide separate charge and discharge paths for the capacitor  $C$  depending on the output state.



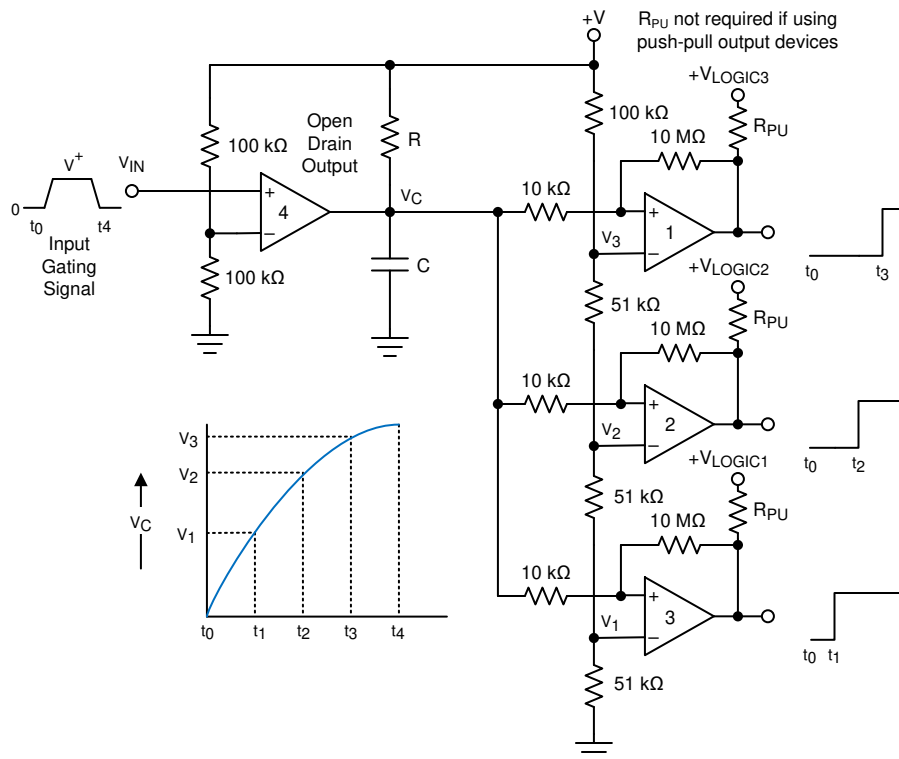
**Figure 7-12. Adjustable Pulse Width Generator**

The charge path is set through  $R_5$  and  $D_2$  when the output is high. Similarly, the discharge path for the capacitor is set by  $R_4$  and  $D_1$  when the output is low.

The pulse width  $t_1$  is determined by the RC time constant of  $R_5$  and  $C$ . Thus, the time  $t_2$  between the pulses can be changed by varying  $R_4$ , and the pulse width can be altered by  $R_5$ . The frequency of the output can be changed by varying both  $R_4$  and  $R_5$ . At low voltages, the effects of the diode forward drop (0.8V, or 0.15V for Shottky) must be taken into account by altering output high and low voltages in the calculations.

### 7.2.4 Time Delay Generator

The circuit shown in [Figure 7-13](#) provides output signals at a prescribed time interval from a time reference and automatically resets the output low when the input returns to 0V. This is useful for sequencing a "power on" signal to trigger a controlled start-up of power supplies.



**Figure 7-13. Time Delay Generator**

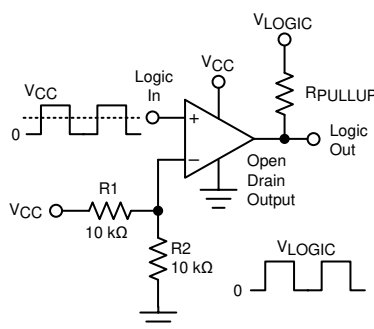
Consider the case of  $V_{IN} = 0$ . The output of comparator 4 is also at ground, "shorting" the capacitor and holding the capacitor at 0V. This implies that the outputs of comparators 1, 2, and 3 are also at 0V. When an input signal is applied, the output of open drain comparator 4 goes High-Z and C charges exponentially through R. This is indicated in the graph. The output voltages of comparators 1, 2, and 3 switch to the high state in sequence when  $V_C$  rises above the reference voltages  $V_1$ ,  $V_2$  and  $V_3$ . A small amount of hysteresis has been provided by the 10k $\Omega$  and 10M $\Omega$  resistors to insure fast switching when the RC time constant is chosen to give long delay times. A good starting point is  $R = 100\text{k}\Omega$  and  $C = 0.01\mu\text{F}$  to 1 $\mu\text{F}$ .

All outputs immediately go low when  $V_{IN}$  falls to 0V, due to the comparator output going low and immediately discharging the capacitor.

Comparator 4 must be a open-drain type output (TLV1822-EP), whereas comparators 1 through 3 can be either open drain or push-pull output, depending on system requirements.  $R_{PU}$  is not required for push-pull output devices.

### 7.2.5 Logic Level Shifter

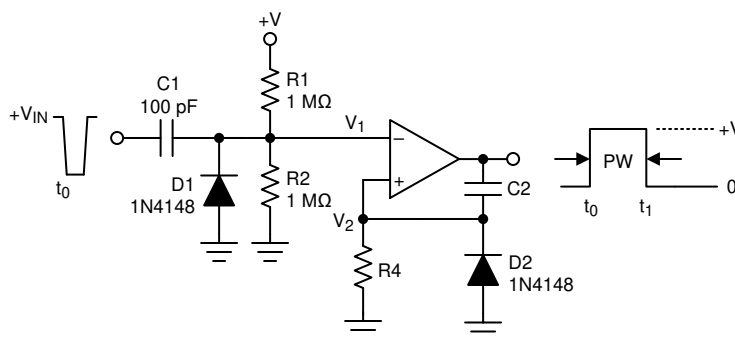
The output of the TLV1822-EP is the uncommitted drain of the output transistor. Many open-drain outputs can be tied together to provide an output OR'ing function if desired.



**Figure 7-14. Universal Logic Level Shifter**

The two 10k $\Omega$  resistors bias the input to half of the input logic supply level to set the threshold in the mid-point of the input logic levels. Only one shared output pull-up resistor is needed and can be connected to any pull-up voltage between 0V and 5.5V. The pullup voltage must match the driven logic input "high" level.

### 7.2.6 One-Shot Multivibrator



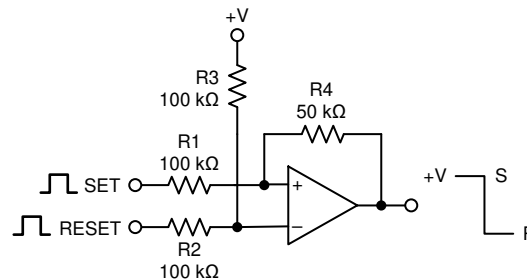
**Figure 7-15. One-Shot Multivibrator**

A monostable multivibrator has one stable state and can remain in that state indefinitely. The monostable multivibrator can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of  $C_2$  and  $R_4$ . The resistor divider of  $R_1$  and  $R_2$  can be used to determine the magnitude of the input trigger pulse. The output changes state when  $V_1 < V_2$ . Diode  $D_2$

provides a rapid discharge path for capacitor  $C_2$  to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

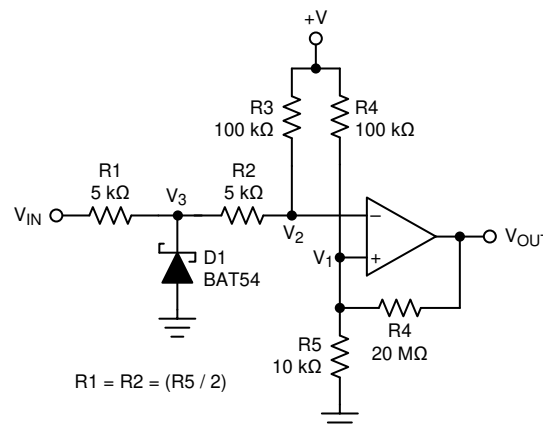
### 7.2.7 Bi-Stable Multivibrator



**Figure 7-16. Bi-Stable Multivibrator**

A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of  $R_2$  and  $R_3$ . A pulse applied to the SET terminal sets the output of the comparator high. The resistor divider of  $R_1$  and  $R_4$  now sets the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET toggles the output low.

### 7.2.8 Zero Crossing Detector



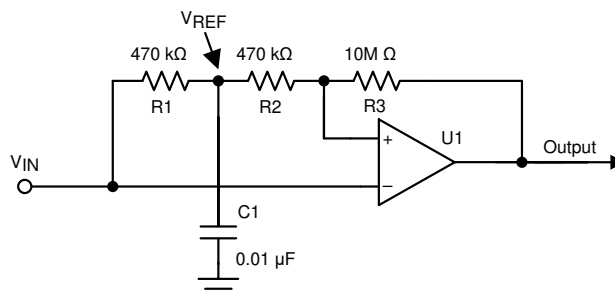
**Figure 7-17. Zero Crossing Detector**

A voltage divider of  $R_4$  and  $R_5$  establishes a reference voltage  $V_1$  at the non-inverting input. By making the series resistance of  $R_1$  and  $R_2$  equal to  $R_5$ , the comparator switches when  $V_{IN} = 0$ . Diode  $D_1$  insures that  $V_3$  clamps near ground. The voltage divider of  $R_2$  and  $R_3$  then prevents  $V_2$  from going below ground. A small amount of hysteresis is setup to facilitate rapid output voltage transitions.

### 7.2.9 Pulse Slicer

A Pulse Slicer is a variation of the Zero Crossing Detector and is used to detect the zero crossings on an input signal with a varying baseline level. This circuit works best with symmetrical waveforms. The RC network of  $R_1$  and  $C_1$  establishes an mean reference voltage  $V_{REF}$ , which tracks the mean amplitude of the  $V_{IN}$  signal. The non-inverting input is directly connected to  $V_{REF}$  through  $R_2$ .  $R_2$  and  $R_3$  are used to produce hysteresis to keep transitions free of spurious toggles. The time constant is a tradeoff between long-term symmetry and response time to changes in amplitude.

The data is recommended to be encoded in NRZ (Non-Return to Zero) format to maintain proper average baseline. Asymmetrical inputs can suffer from timing distortions caused by the changing  $V_{REF}$  average voltage.



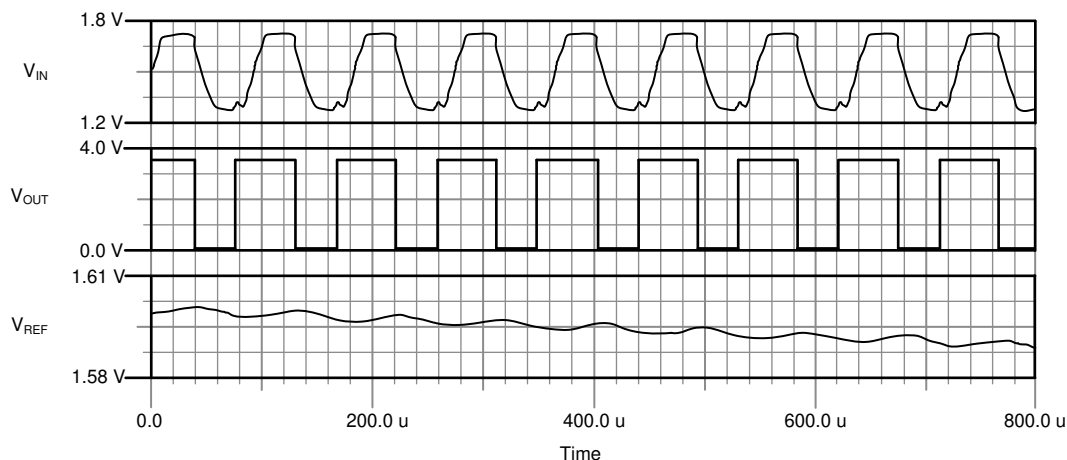
**Figure 7-18. Pulse Slicer**

For this design, follow these design requirements:

- The RC constant value ( $R_2$  and  $C_1$ ) must support the targeted data rate to maintain a valid tripping threshold.
- The hysteresis introduced with  $R_2$  and  $R_{43}$  helps to avoid spurious output toggles.

The TLV1822-EP can also be used, but with the addition of a pull-up resistor on the output (not shown for clarity).

Figure 7-19 shows the results of a 9600 baud data signal riding on a varying baseline.



**Figure 7-19. Pulse Slicer Waveforms**

### 7.3 Power Supply Recommendations

Due to the fast output edges, bypass capacitors are critical on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1 $\mu$ F ceramic bypass capacitor directly between  $V_{CC}$  pin and ground pins. Narrow, peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies ( $V+$  and  $V-$ ), or "single" supplies ( $V+$  and GND), with GND applied to the  $V-$  pin. Input signals must stay within the specified input range (between  $V+$  and  $V-$ ) for either type. Note that with a "split" supply the output swings "low" ( $V_{OL}$ ) to  $V-$  potential and not GND.

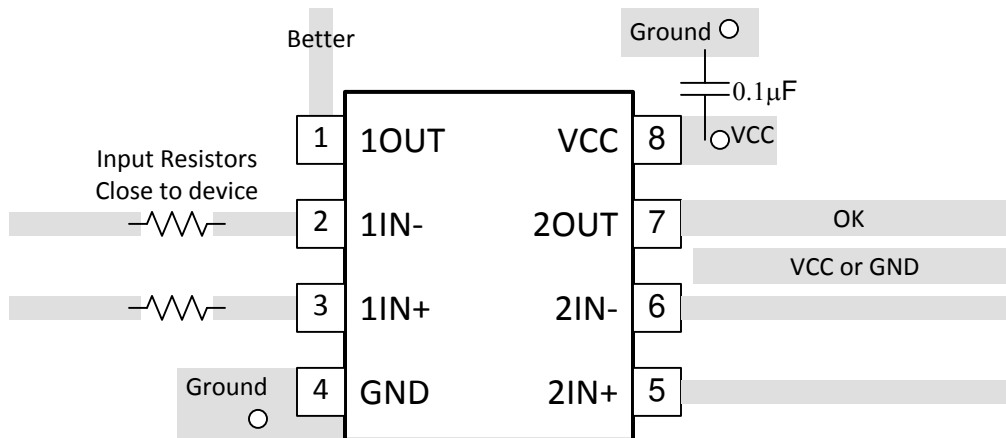
## 7.4 Layout

### 7.4.1 Layout Guidelines

For accurate comparator applications, maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the  $V_{CC}$  and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations can be used when routing long distances.

### 7.4.2 Layout Example



**Figure 7-20. Dual Layout Example**

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Analog Engineers Circuit Cookbook: Amplifiers e-book](#)
- Texas Instruments, [Precision Design, Comparator with Hysteresis design guide](#)
- Texas Instruments, [Window comparator circuit application note](#)
- Texas Instruments, [Reference Design, Window Comparator Reference Design design guide](#)
- Texas Instruments, [Comparator with and without hysteresis circuit application note](#)
- Texas Instruments, [Inverting comparator with hysteresis circuit application note](#)
- Texas Instruments, [Non-Inverting Comparator With Hysteresis Circuit application note](#)
- Texas Instruments, [Zero crossing detection using comparator circuit application note](#)
- Texas Instruments, [PWM generator circuit application note](#)
- Texas Instruments, [How to Implement Comparators for Improving Performance of Rotary Encoder in Industrial Drive Applications application note](#)
- Texas Instruments, [A Quad of Independently Func Comparators application note](#)

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2024) to Revision A (July 2025)	Page
• Added VID and Controlled Baseline information to <i>Features</i> .....	1
• Removed preview for TLV1812-EP/22 Dual SOIC Release.....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLV1812MDDFREP</a>	Active	Production	SOT-23-THIN (DDF)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T12EP
<a href="#">TLV1822MDDFREP</a>	Active	Production	SOT-23-THIN (DDF)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T22EP
<a href="#">V62/24628-01XE</a>	Active	Production	SOT-23-THIN (DDF)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T12EP
<a href="#">V62/24628-02XE</a>	Active	Production	SOT-23-THIN (DDF)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See TLV1822MDDFREP	T22EP

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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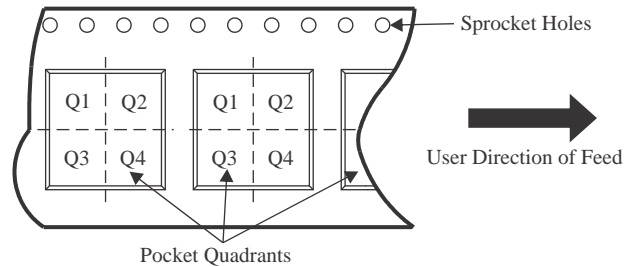
**OTHER QUALIFIED VERSIONS OF TLV1812-EP, TLV1822-EP :**

- Catalog : [TLV1812](#), [TLV1822](#)
- Automotive : [TLV1812-Q1](#), [TLV1822-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1812MDDFREP	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1822MDDFREP	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1812MDDFREP	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV1822MDDFREP	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

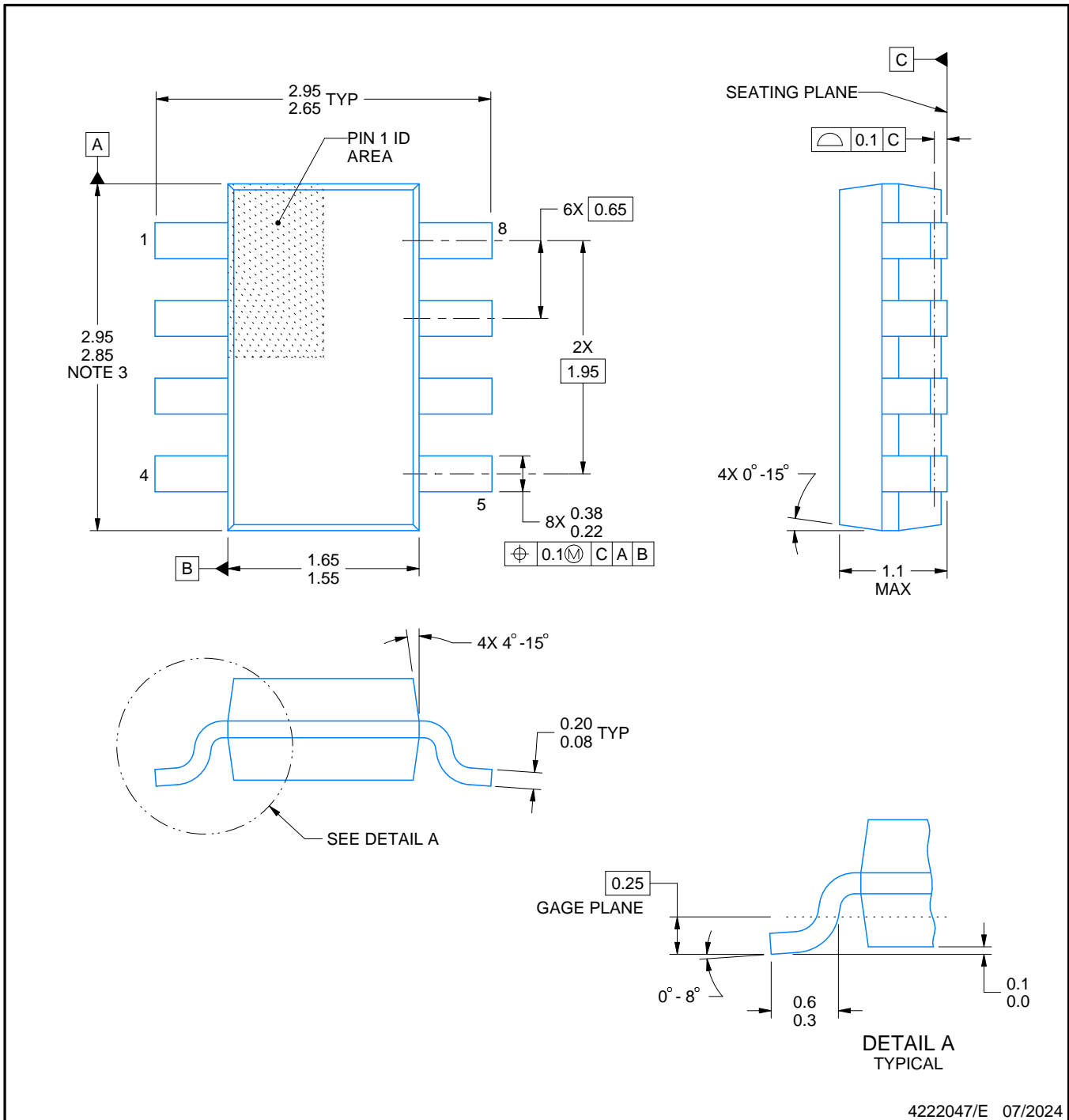
# DDF0008A



# PACKAGE OUTLINE

## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

### NOTES:

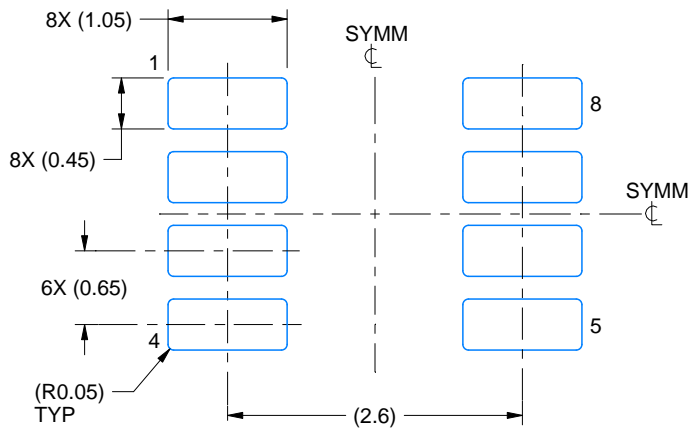
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

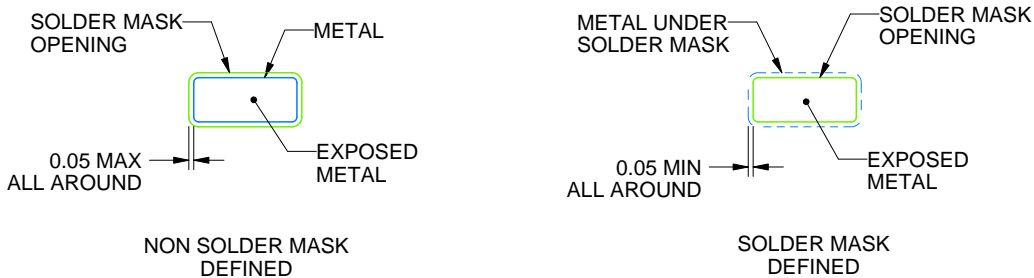
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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