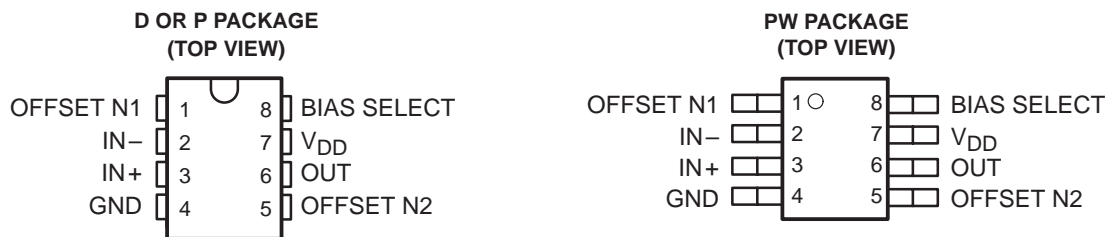


- **Wide Range of Supply Voltages Over Specified Temperature Range:**
 $T_A = -40^{\circ}\text{C}$ to 85°C . . . 2 V to 8 V
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to $V_{DD} - 1$ V at 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . $10^{12} \Omega$ Typ**
- **Low Noise . . . 25 nV/ $\sqrt{\text{Hz}}$ Typically at $f = 1$ kHz (High-Bias Mode)**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**
- **Bias-Select Feature Enables Maximum Supply Current Range From 17 μA to 1.5 mA at 25°C**



description

The TLV2341 operational amplifier has been specifically developed for low-voltage, single-supply applications and is fully specified to operate over a voltage range of 2 V to 8 V. The device uses the Texas Instruments silicon-gate LinCMOS™ technology to facilitate low-power, low-voltage operation and excellent offset-voltage stability. LinCMOS™ technology also enables extremely high input impedance and low bias currents allowing direct interface to high-impedance sources.

The TLV2341 offers a bias-select feature, which allows the device to be programmed with a wide range of different supply currents and therefore different levels of ac performance. The supply current can be set at 17 μA , 250 μA , or 1.5 mA, which results in slew-rate specifications between 0.02 and 2.1 V/ μs (at 3 V).

The TLV2341 operational amplifiers are especially well suited to single-supply applications and are fully specified and characterized at 3-V and 5-V power supplies. This low-voltage single-supply operation combined with low power consumption makes this device a good choice for remote, inaccessible, or portable battery-powered applications. The common-mode input range includes the negative rail.

The device inputs and outputs are designed to withstand -100-mA currents without sustaining latch-up. The TLV2341 incorporates internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD 883 C, Methods 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

AVAILABLE OPTIONS

T_A	V_{IOmax} AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
-40°C to 85°C	8 mV	TLV2341ID	TLV2341IP	TLV2341IPWLE	TLV2341Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2341IDR).
 The PW package is only available left-end taped and reeled (e.g., TLV2341IPWLE).

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



TLV2341, TLV2341Y LinCMOS™ PROGRAMMABLE LOW-VOLTAGE OPERATIONAL AMPLIFIERS

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bias-select feature

The TLV2342 offers a bias-select feature that allows the user to select any one of three bias levels, depending on the level of performance desired. The tradeoffs between bias levels involve ac performance and power dissipation (see Table 1).

Table 1. Effect of Bias Selection on Performance

TYPICAL PARAMETER VALUES $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$		MODE			UNIT
		HIGH BIAS $R_L = 10\text{ k}\Omega$	MEDIUM BIAS $R_L = 100\text{ k}\Omega$	LOW BIAS $R_L = 1\text{ M}\Omega$	
P_D	Power dissipation	975	195	15	μW
SR	Slew rate	2.1	0.38	0.02	$\text{V}/\mu\text{s}$
V_n	Equivalent input noise voltage at $f = 1\text{ kHz}$	25	32	68	$\text{nV}/\sqrt{\text{Hz}}$
B_1	Unity-gain bandwidth	790	300	27	kHz
ϕ_m	Phase margin	46°	39°	34°	
A_{VD}	Large-signal differential voltage amplification	11	83	400	V/mV

bias selection

Bias selection is achieved by connecting BIAS SELECT to one of three voltage levels (see Figure 1). For medium-bias applications, it is recommended that the bias-select pin be connected to the midpoint between the supply rails. This procedure is simple in split-supply applications since this point is ground. In single-supply applications, the medium-bias mode necessitates using a voltage divider as indicated in Figure 1. The use of large-value resistors in the voltage divider reduces the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint may be used if it is within the voltages specified in the following table.

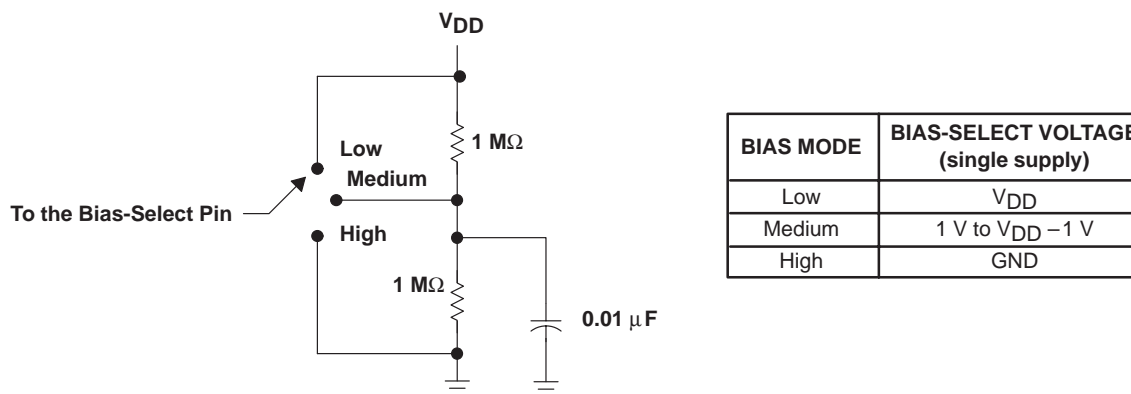


Figure 1. Bias Selection for Single-Supply Applications

high-bias mode

In the high-bias mode, the TLV2341 series feature low offset voltage drift, high input impedance, and low noise. Speed in this mode approaches that of BiFET devices but at only a fraction of the power dissipation.

medium-bias mode

The TLV2341 in the medium-bias mode features a low offset voltage drift, high input impedance, and low noise. Speed in this mode is similar to general-purpose bipolar devices but power dissipation is only a fraction of that consumed by bipolar devices.

low-bias mode

In the low-bias mode, the TLV2341 features low offset voltage drift, high input impedance, extremely low power consumption, and high differential voltage gain.

ORDER OF CONTENTS

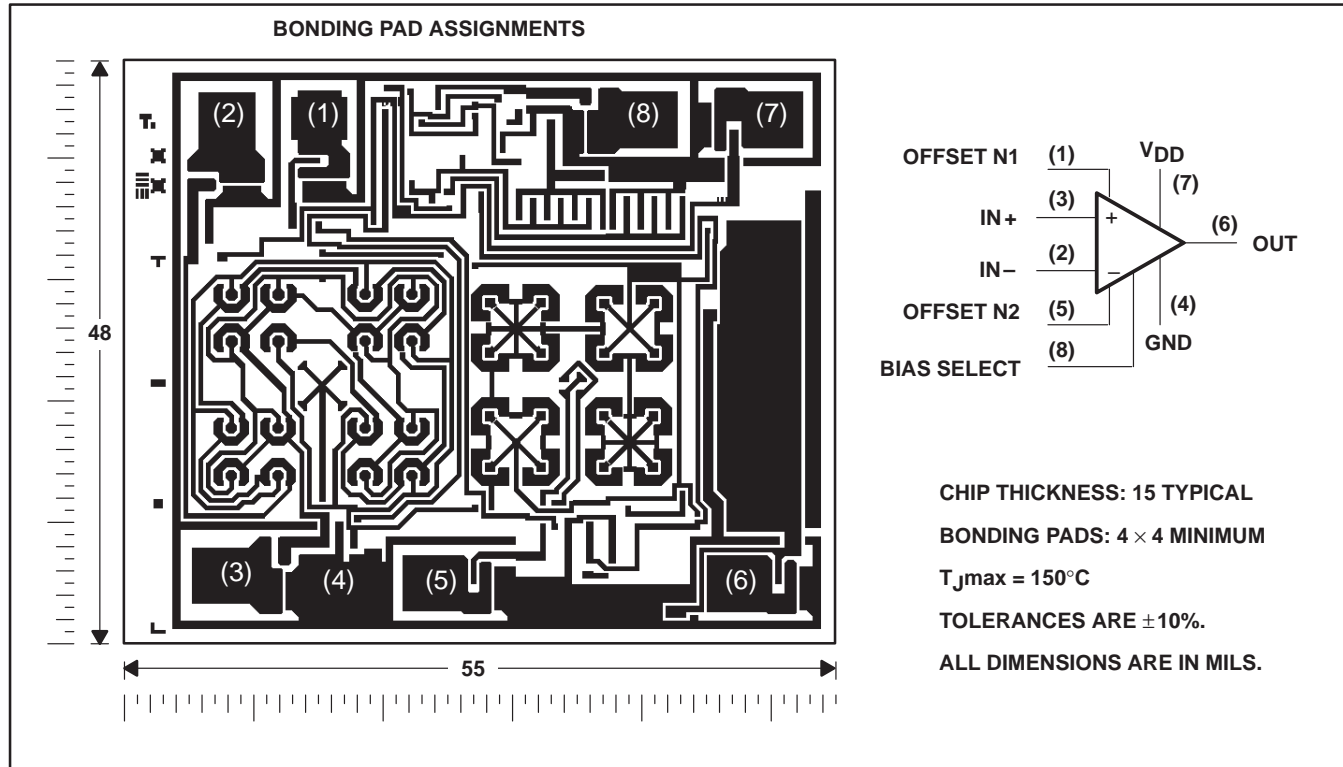
TOPIC	BIAS MODE
Schematic	all
Absolute maximum ratings	all
Recommended operating conditions	all
Electrical characteristics Operating characteristics Typical characteristics	high (Figures 2 – 31)
Electrical characteristics Operating characteristics Typical characteristics	medium (Figures 32 – 61)
Electrical characteristics Operating characteristics Typical characteristics	low (Figures 62 – 91)
Parameter measurement information	all
Application information	all

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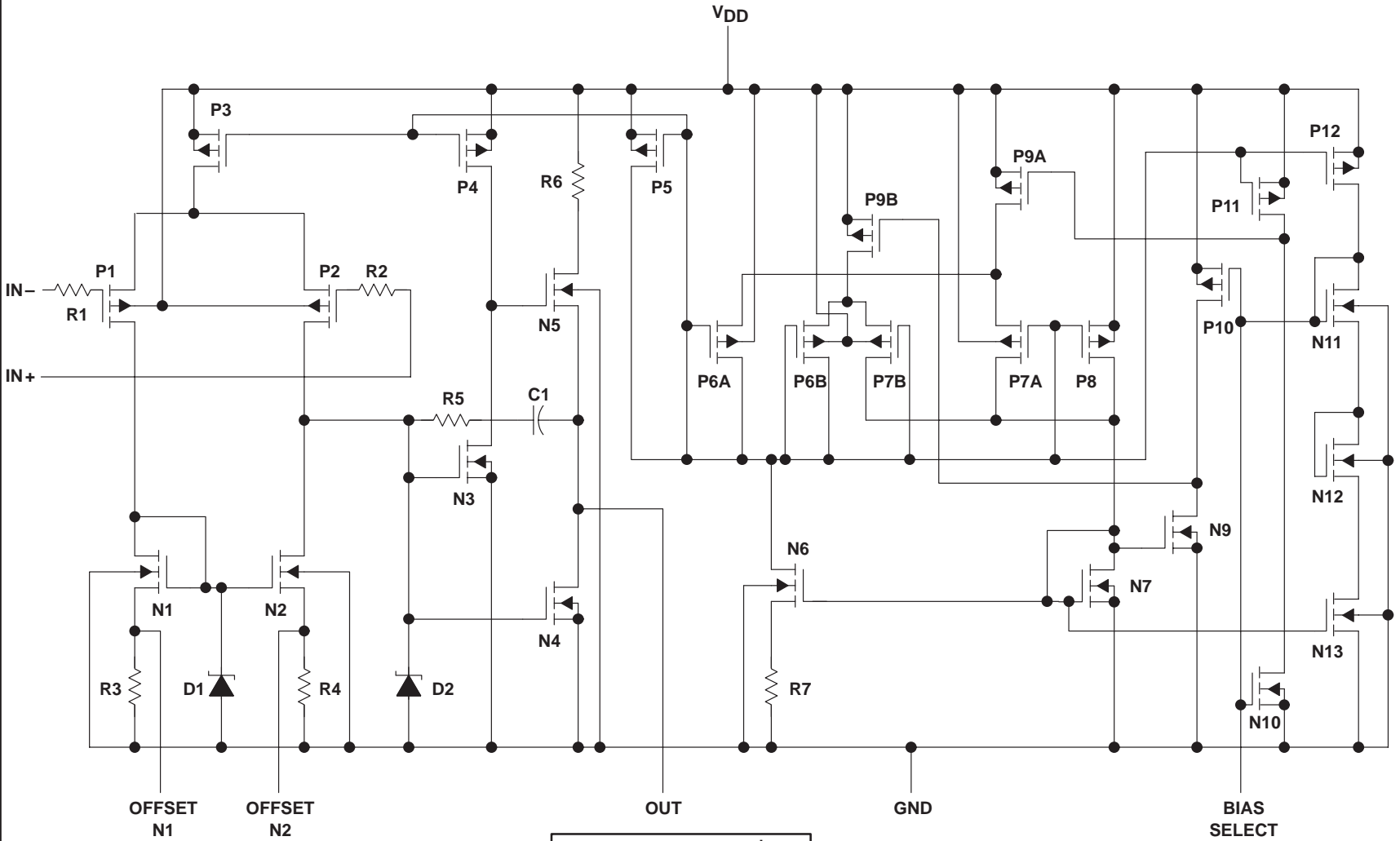
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TLV2341Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2341. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



equivalent schematic



COMPONENT COUNT†	
Transistors	27
Diodes	2
Resistors	7
Capacitors	1

† Includes the amplifier and all ESD, bias, and trim circuitry

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	8 V
Differential input voltage (see Note 2)	$V_{DD} \pm$
Input voltage range, V_I (any input)	-0.3 V to V_{DD}
Input current, I_I	± 5 mA
Output current, I_O	± 30 mA
Duration of short-circuit current at (or below) $T_A = 25^\circ\text{C}$ (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	-40°C to 85°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may effect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 2. Differential voltages are at the noninverting input with respect to the inverting input.
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/ $^\circ\text{C}$	377 mW
P	1000 mW	8.0 mW/ $^\circ\text{C}$	520 mW
PW	525 mW	4.2 mW/ $^\circ\text{C}$	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	$V_{DD} = 3$ V	-0.2	1.8	V
	$V_{DD} = 5$ V	-0.2	3.8	
Operating free-air temperature, T_A		-40	85	$^\circ\text{C}$



HIGH-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T _A †	TLV2341I						UNIT
			V _{DD} = 3 V			V _{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO} Input offset voltage	V _O = 1 V, V _{IC} = 1 V, R _S = 50 Ω, R _L = 10 kΩ	25°C	0.6		8	1.1		8	mV
		Full range			10			10	
α _{VIO} Average temperature of input offset voltage		25°C to 85°C	2.7			2.7			μV/°C
I _{IO} Input offset current (see Note 4)	V _O = 1 V, V _{IC} = 1 V	25°C	0.1			0.1			pA
		85°C	22	1000		24	1000		
I _{IB} Input bias current (see Note 4)	V _O = 1 V, V _{IC} = 1 V	25°C	0.6			0.6			pA
		85°C	175	2000		200	2000		
V _{ICR} Common-mode input voltage range (see Note 5)		25°C	-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2		V
		Full range	-0.2 to 1.8			-0.2 to 3.8			V
V _{OH} High-level output voltage	V _{IC} = 1 V, V _{ID} = 100 mV, I _{OH} = -1 mA	25°C	1.75	1.9		3.2	3.7		V
		Full range	1.7			3			
V _{OL} Low-level output voltage	V _{IC} = 1 V, V _{ID} = -100 mV, I _{OL} = 1 mA	25°C	120		150	90		150	mV
		Full range			190			190	
A _{VD} Large-signal differential voltage amplification	V _{IC} = 1 V, R _L = 10 kΩ, See Note 6	25°C	3	11		5	23		V/mV
		Full range	2			3.5			
CMRR Common-mode rejection ratio	V _O = 1 V, V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	65	78		65	80		dB
		Full range	60			60			
k _{SVR} Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{IC} = 1 V, V _O = 1 V, R _S = 50 Ω	25°C	70	95		70	95		dB
		Full range	65			65			
I _{I(SEL)} Bias select current	V _{I(SEL)} = 0	25°C	-1.2			-1.4			μA
I _{DD} Supply current	V _O = 1 V, V _{IC} = 1 V, No load	25°C	325	1500		675	1600		μA
		Full range			2000			2200	

† Full range is -40°C to 85°C.

- NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
 5. This range also applies to each input individually.
 6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

HIGH-BIAS MODE

operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	T_A	TLV2341I			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_{IC} = 1\text{ V}$, $R_L = 10\text{ k}\Omega$, See Figure 92	$V_{I(PP)} = 1\text{ V}$, $C_L = 20\text{ pF}$	25°C	2.1		V/ μs
			85°C	1.7		
V_n Equivalent input noise voltage	$f = \text{kHz}$, See Figure 93	$R_S = 20\ \Omega$	25°C	25		nV/ $\sqrt{\text{Hz}}$
BOM Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10\text{ k}\Omega$, See Figure 92	$C_L = 20\text{ pF}$	25°C	170		kHz
			85°C	145		
B ₁ Unity-gain bandwidth	$V_I = 10\text{ mV}$, $R_L = 10\text{ k}\Omega$, See Figure 94	$C_L = 20\text{ pF}$	25°C	790		kHz
			85°C	690		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$, See Figure 94	$f = B_1$, $R_L = 1\text{ M}\Omega$	-40°C	53°		
			25°C	49°		
			85°C	47°		

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A	TLV2341I			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_{IC} = 1\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 20\text{ pF}$, See Figure 92	$V_{I(PP)} = 1\text{ V}$	25°C	3.6		V/ μs
			85°C	2.8		
		$V_{I(PP)} = 2.5\text{ V}$	25°C	2.9		
			85°C	2.3		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 93	$R_S = 20\ \Omega$	25°C	25		nV/ $\sqrt{\text{Hz}}$
BOM Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10\text{ k}\Omega$, See Figure 92	$C_L = 20\text{ pF}$	25°C	320		kHz
			85°C	250		
B ₁ Unity-gain bandwidth	$V_I = 10\text{ mV}$, $R_L = 10\text{ k}\Omega$, See Figure 94	$C_L = 20\text{ pF}$	25°C	1.7		MHz
			85°C	1.2		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$, See Figure 94	$f = B_1$, $R_L = 10\text{ k}\Omega$	-40°C	49°		
			25°C	46°		
			85°C	43°		

HIGH-BIAS MODE

electrical characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLV2341I						UNIT
		$V_{DD} = 3\text{ V}$			$V_{DD} = 5\text{ V}$			
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 1\text{ V}$, $V_{IC} = 1\text{ V}$, $R_S = 50\ \Omega$, $R_L = 10\text{ k}\Omega$		0.6	8		1.1	8	mV
I_{IO} Input offset current (see Note 4)	$V_O = 1\text{ V}$, $V_{IC} = 1\text{ V}$		0.1			0.1		pA
I_{IB} Input bias current (see Note 4)	$V_O = 1\text{ V}$, $V_{IC} = 1\text{ V}$		0.6			0.6		pA
V_{ICR} Common-mode input voltage range (see Note 5)		-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2		V
V_{OH} High-level output voltage	$V_{IC} = 1\text{ V}$, $V_{ID} = 100\text{ mV}$, $I_{OH} = -1\text{ mA}$	1.75	1.9		3.2	3.7		V
V_{OL} Low-level output voltage	$V_{IC} = 1\text{ V}$, $V_{ID} = -100\text{ mV}$, $I_{OL} = 1\text{ mA}$		120	150		90	150	mV
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 1\text{ V}$, $R_L = 10\text{ k}\Omega$, See Note 6	3	11		50	23		V/mV
CMRR Common-mode rejection ratio	$V_O = 1\text{ V}$, $V_{IC} = V_{ICR\text{min}}$, $R_S = 50\ \Omega$	65	78		65	80		dB
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_O = 1\text{ V}$, $V_{IC} = 1\text{ V}$, $R_S = 50\ \Omega$	70	95		70	95		dB
$I_{I(SEL)}$ Bias select current	$V_{I(SEL)} = 0$		-1.2			-1.4		μA
I_{DD} Supply current	$V_O = 1\text{ V}$, $V_{IC} = 1\text{ V}$, No load		325	1500		675	1600	μA

- NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
 5. This range also applies to each input individually.
 6. At $V_{DD} = 5\text{ V}$, $V_O = 0.25\text{ V}$ to 2 V ; at $V_{DD} = 3\text{ V}$, $V_O = 0.5\text{ V}$ to 1.5 V .

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

Table of Graphs

		FIGURE	
V_{IO}	Input offset voltage	Distribution	2,3
α_{VIO}	Input offset voltage temperature coefficient	Distribution	4,5
V_{OH}	High-level output voltage	vs Output current	6
		vs Supply voltage	7
		vs Temperature	8
V_{OL}	Low-level output voltage	vs Common-mode input voltage	9
		vs Temperature	10, 12
		vs Differential input voltage	11
		vs Low-level output current	13
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	14
		vs Temperature	15
		vs Frequency	26, 27
I_{IB}	Input bias current	vs Temperature	16
I_{IO}	Input offset current	vs Temperature	16
V_{IC}	Common-mode input voltage	vs Supply voltage	17
I_{DD}	Supply current	vs Supply voltage	18
		vs Temperature	19
SR	Slew rate	vs Supply voltage	20
		vs Temperature	21
	Bias select current	vs Supply voltage	22
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	23
B_1	Unity-gain bandwidth	vs Temperature	24
		vs Supply voltage	25
ϕ_m	Phase margin	vs Supply voltage	28
		vs Temperature	29
		vs Load capacitance	30
V_n	Equivalent input noise voltage	vs Frequency	31
		Phase shift	26, 27

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

**DISTRIBUTION OF TLV2341
 INPUT OFFSET VOLTAGE**

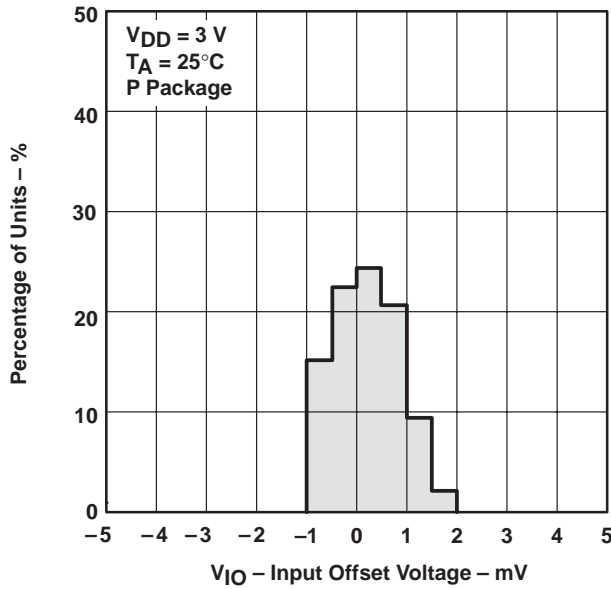


Figure 2

**DISTRIBUTION OF TLV2341
 INPUT OFFSET VOLTAGE**

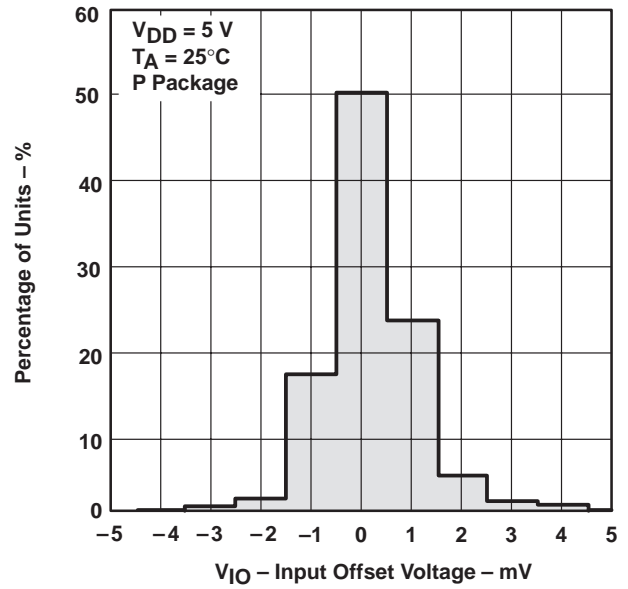


Figure 3

**DISTRIBUTION OF TLV2341
 INPUT OFFSET VOLTAGE
 TEMPERATURE COEFFICIENT**

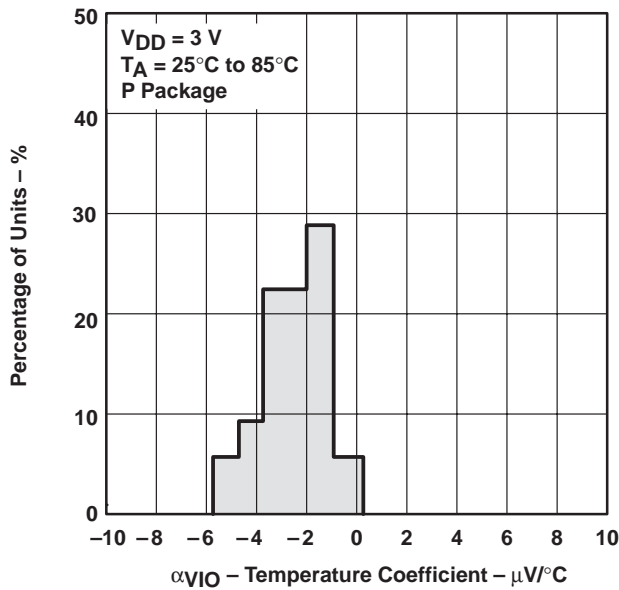


Figure 4

**DISTRIBUTION OF TLV2341
 INPUT OFFSET VOLTAGE
 TEMPERATURE COEFFICIENT**

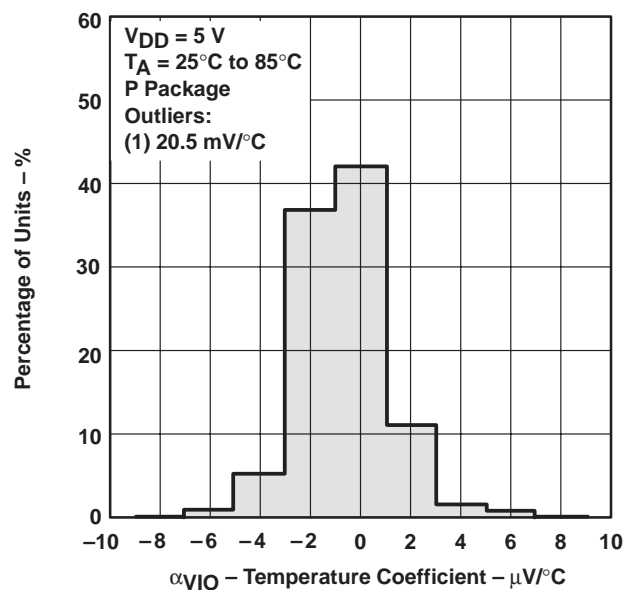
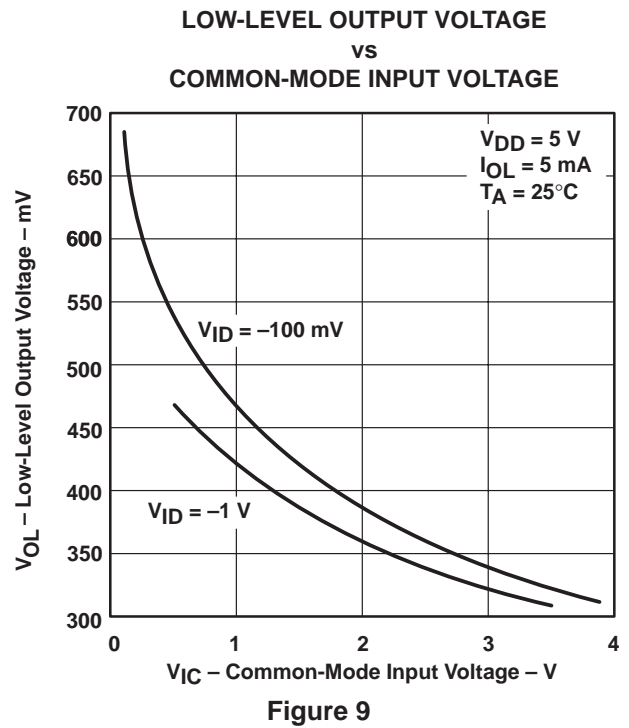
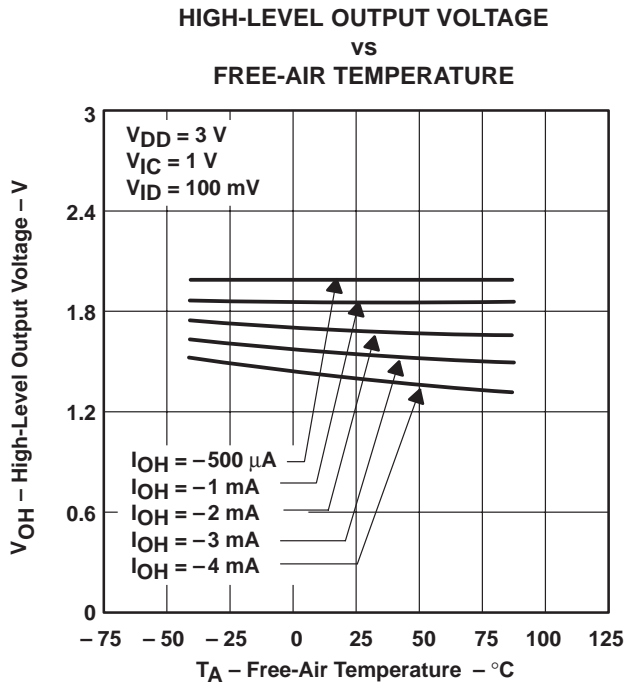
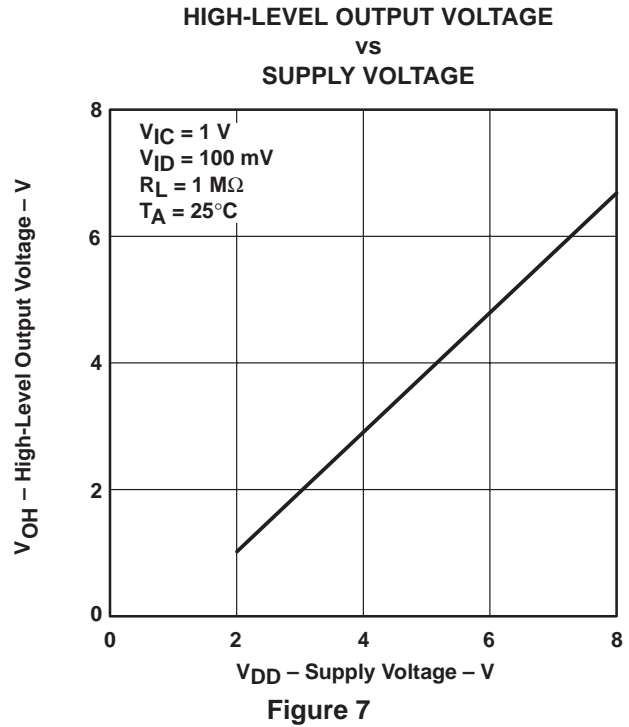
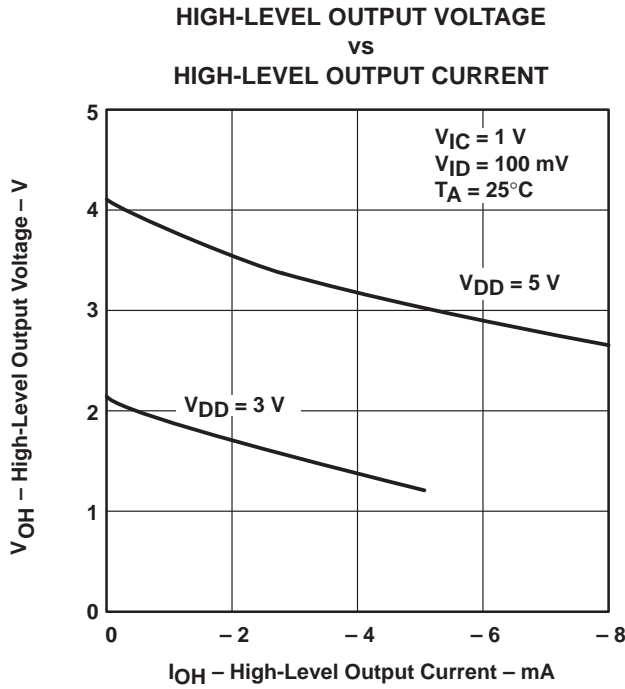


Figure 5

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)



TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

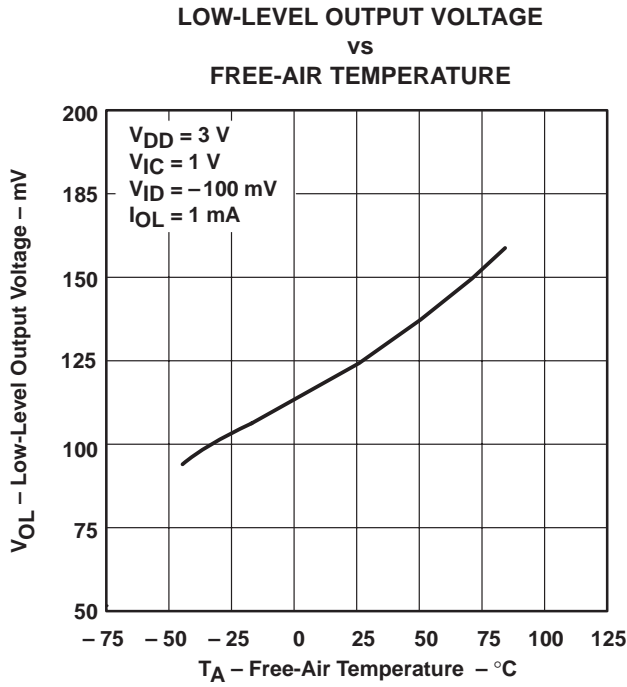


Figure 10

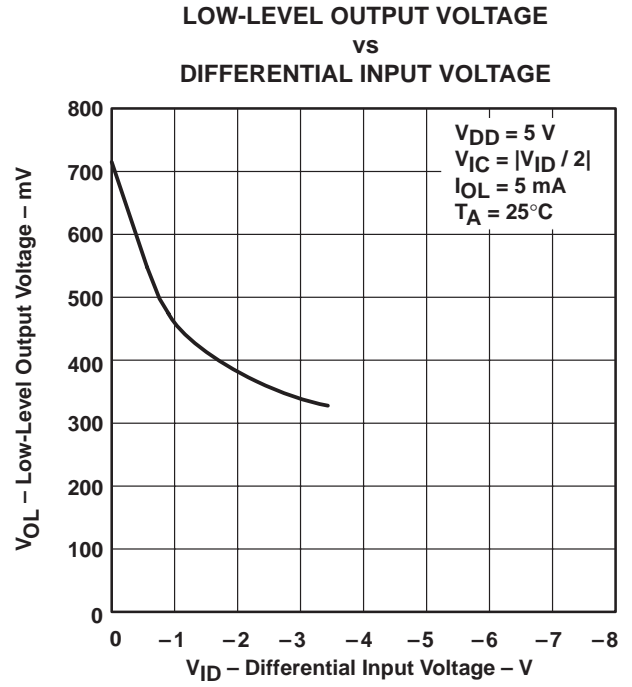


Figure 11

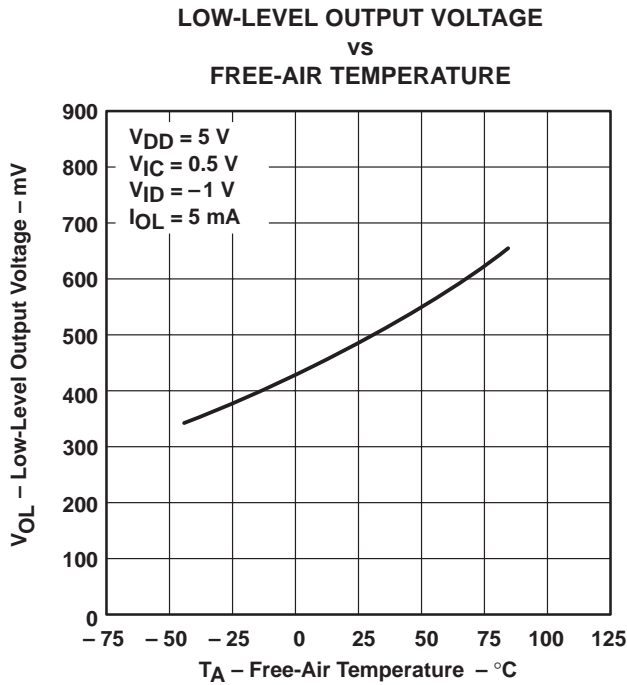


Figure 12

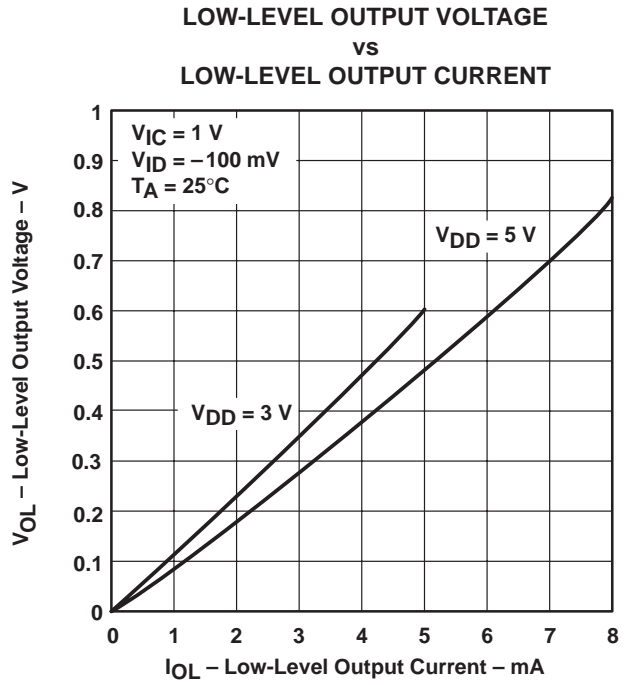


Figure 13

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VS SUPPLY VOLTAGE

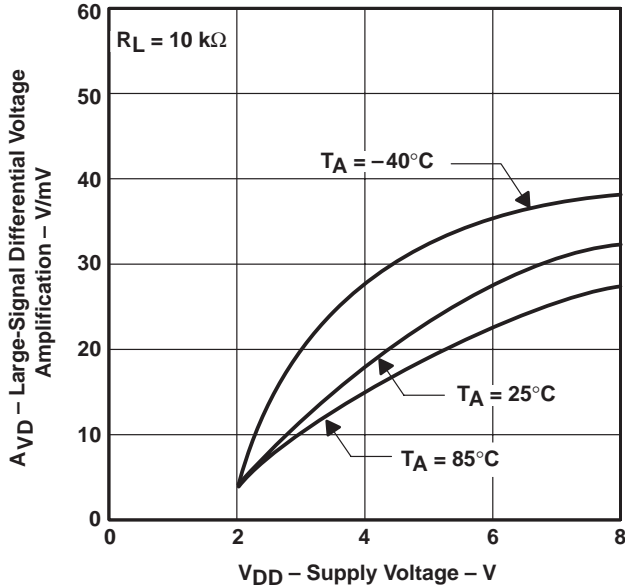


Figure 14

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VS FREE-AIR TEMPERATURE

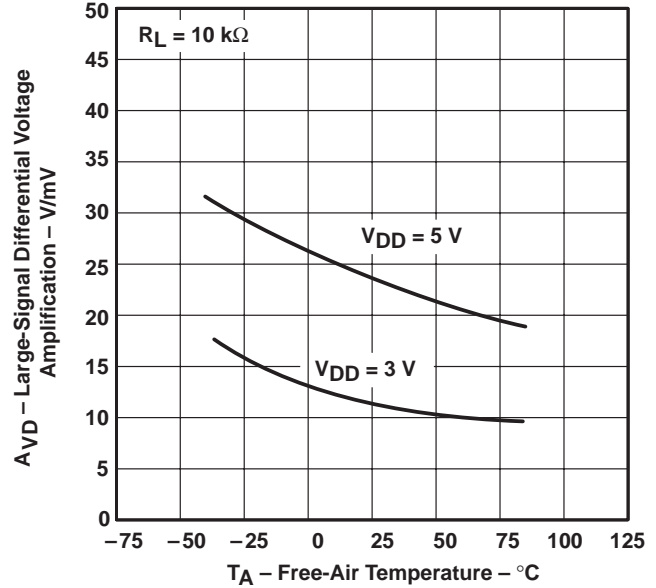


Figure 15

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT VS FREE-AIR TEMPERATURE

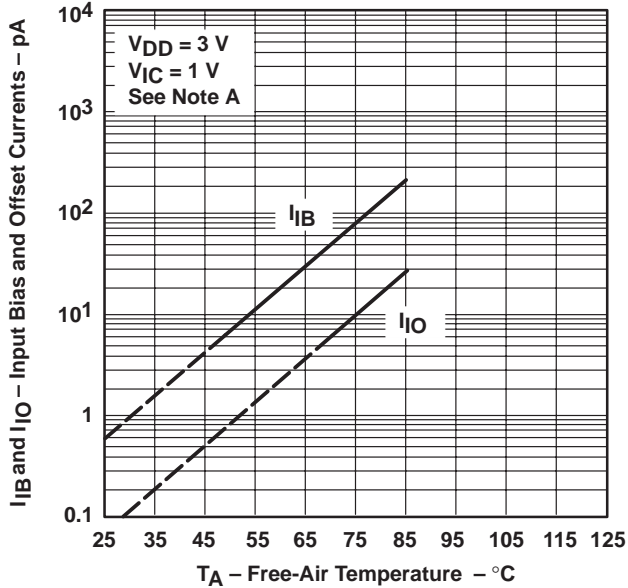


Figure 16

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT VS SUPPLY VOLTAGE

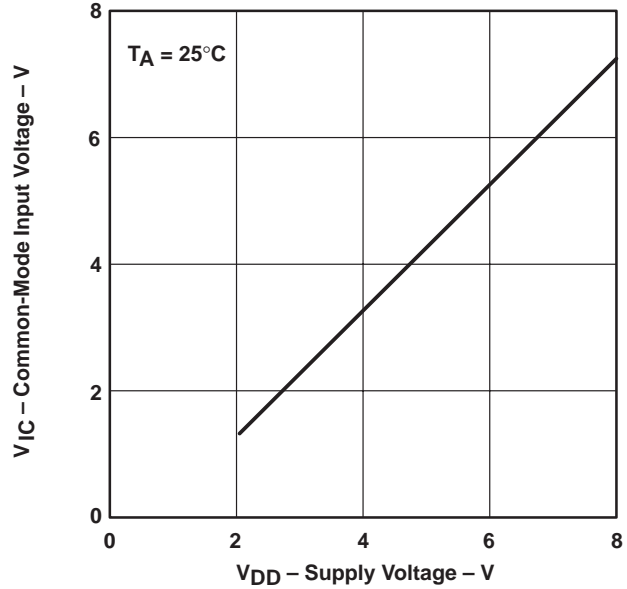


Figure 17

NOTE: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

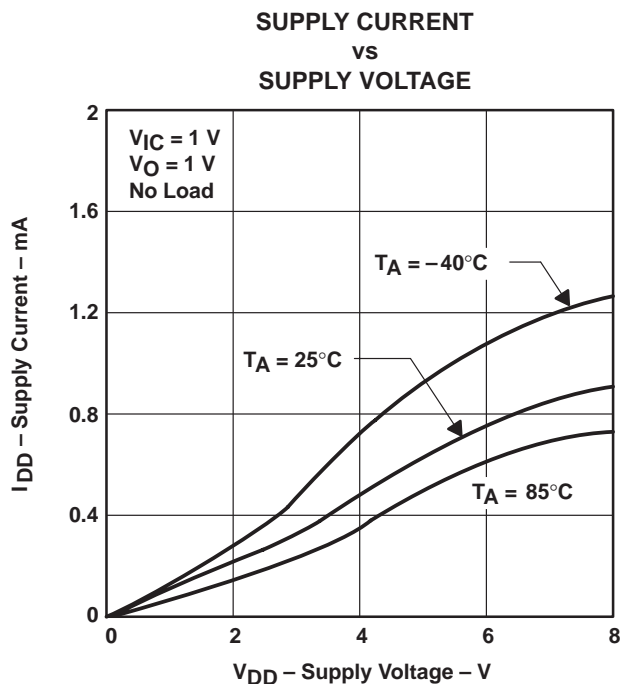


Figure 18

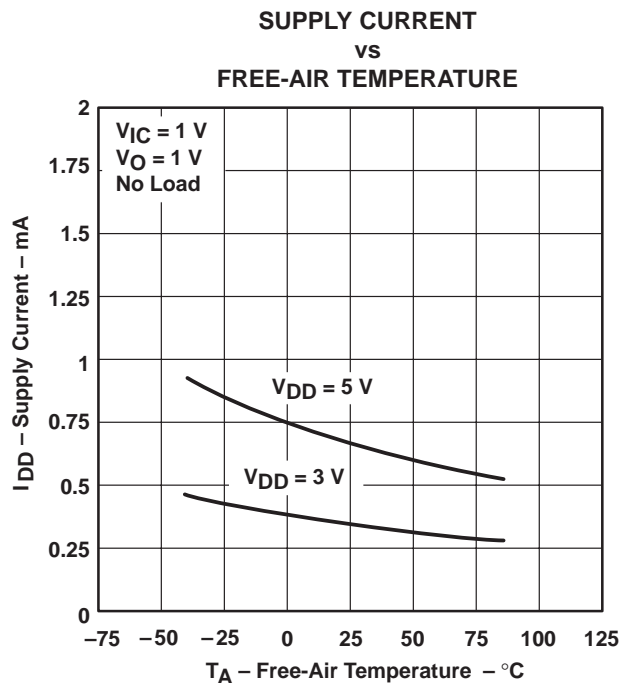


Figure 19

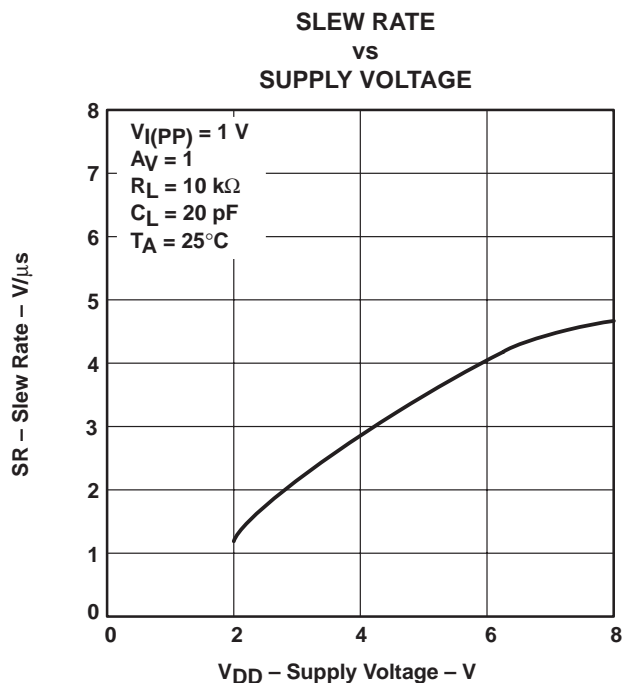


Figure 20

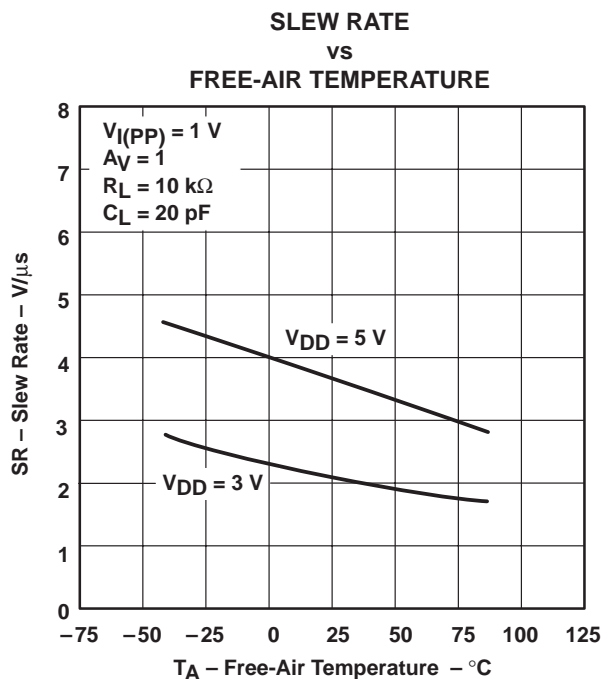


Figure 21

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

BIAS SELECT CURRENT
 vs
 SUPPLY VOLTAGE

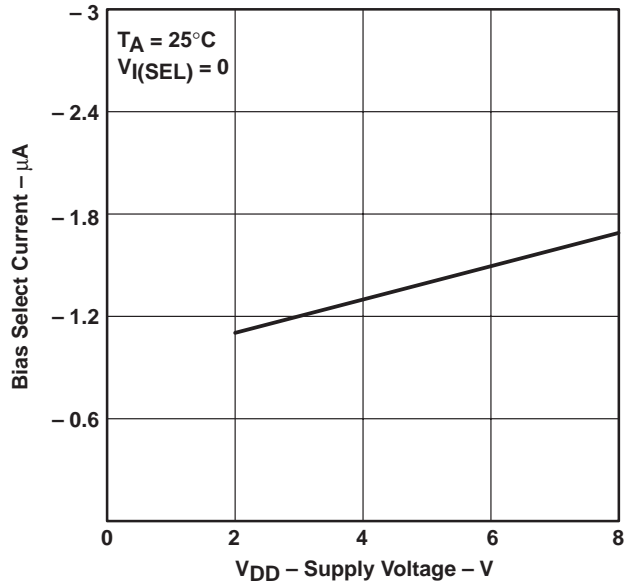


Figure 22

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
 vs
 FREQUENCY

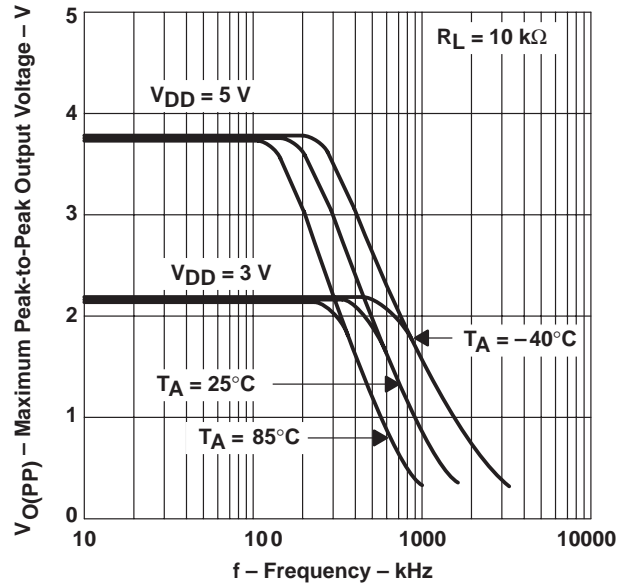


Figure 23

UNITY-GAIN BANDWIDTH
 vs
 FREE-AIR TEMPERATURE

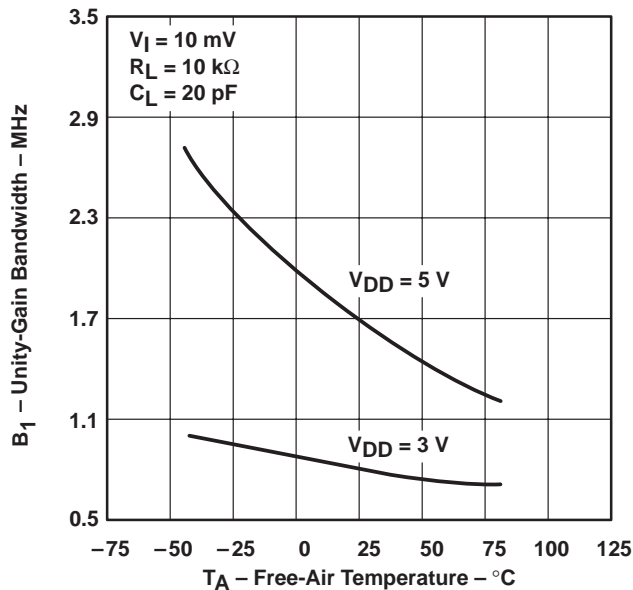


Figure 24

UNITY-GAIN BANDWIDTH
 vs
 SUPPLY VOLTAGE

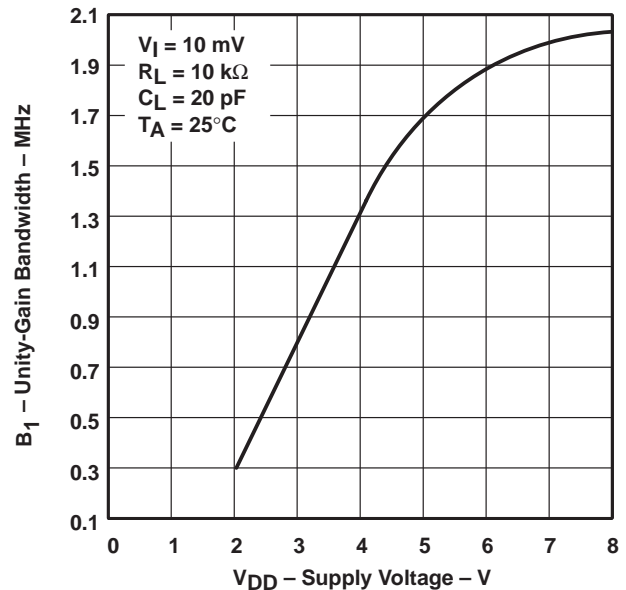
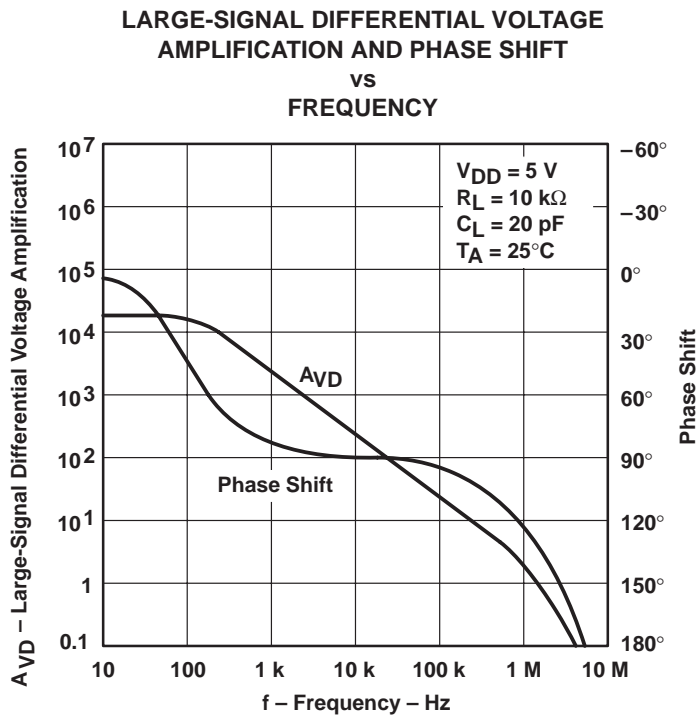
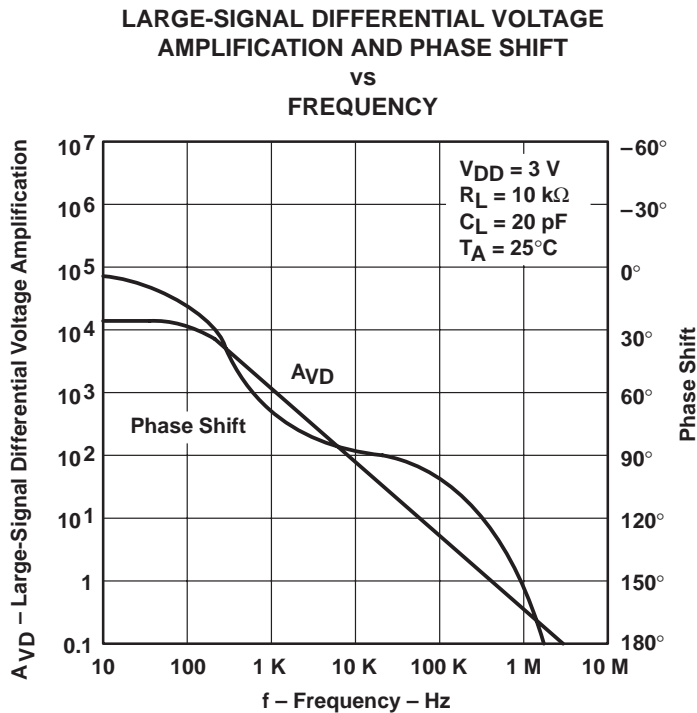


Figure 25

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)



TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

**PHASE MARGIN
 vs
 SUPPLY VOLTAGE**

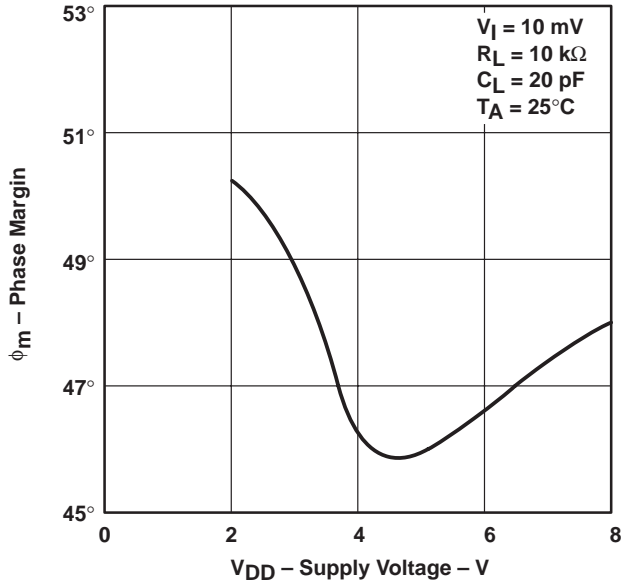


Figure 28

**PHASE MARGIN
 vs
 FREE-AIR TEMPERATURE**

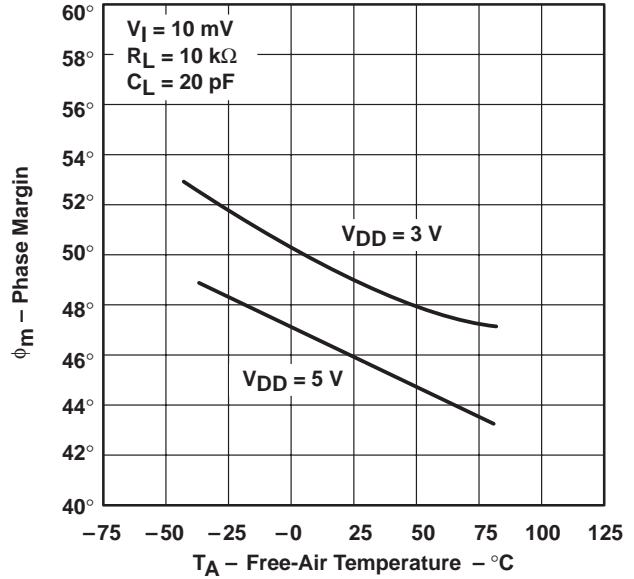


Figure 29

**PHASE MARGIN
 vs
 LOAD CAPACITANCE**

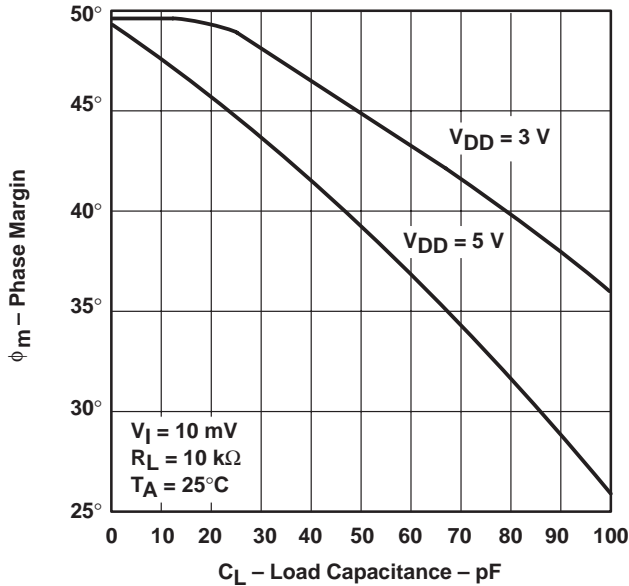


Figure 30

**EQUIVALENT INPUT NOISE VOLTAGE
 vs
 FREQUENCY**

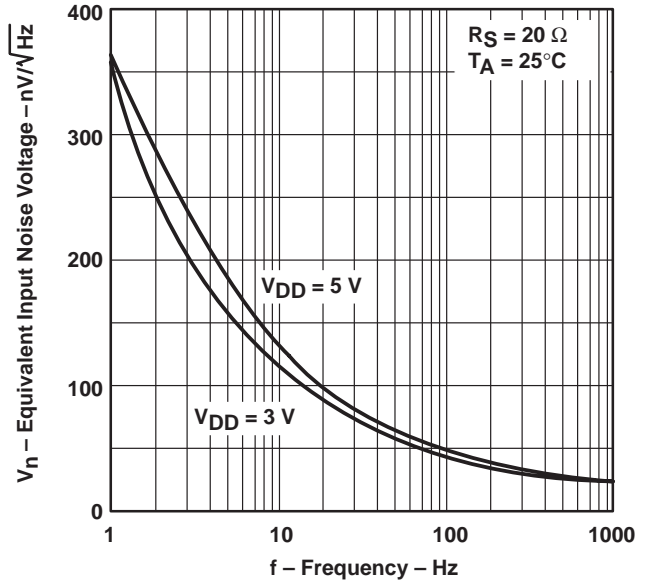


Figure 31

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T _A †	TLV2341I						UNIT
			V _{DD} = 3 V			V _{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO} Input offset voltage	V _O = 1 V, V _{IC} = 1 V, R _S = 50 Ω, R _L = 100 kΩ	25°C	0.6		8	1.1		8	mV
		Full range			10			10	
α _{VIO} Average temperature coefficient of input offset voltage		25°C to 85°C	1			1.7			μV/°C
I _{IO} Input offset current (see Note 4)	V _O = 1 V, V _{IC} = 1 V	25°C	0.1			0.1			pA
		85°C	22	1000		24	1000		
I _{IB} Input bias current (see Note 4)	V _O = 1 V, V _{IC} = 1 V	25°C	0.6			0.6			pA
		85°C	175	2000		200	2000		
V _{ICR} Common-mode input voltage range (see Note 5)		25°C	-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2		V
		Full range	-0.2 to 1.8			-0.2 to 3.8			V
V _{OH} High-level output voltage	V _{IC} = 1 V, V _{ID} = 100 mV, I _{OH} = -1 mA	25°C	1.75	1.9		3.2	3.9		V
		Full range	1.7			3			
V _{OL} Low-level output voltage	V _{IC} = 1 V, V _{ID} = -100 mV, I _{OL} = 1 mA	25°C	115		150	95		150	mV
		Full range	190			190			
A _{VD} Large-signal differential voltage amplification	V _{IC} = 1 V, R _L = 100 kΩ, See Note 6	25°C	25	83		25	170		V/mV
		Full range	15			15			
CMRR Common-mode rejection ratio	V _O = 1 V, V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	65	92		65	91		dB
		Full range	60			60			
k _{SVR} Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{IC} = 1 V, V _O = 1 V, R _S = 50 Ω	25°C	70	94		70	94		dB
		Full range	65			65			
I _{I(SEL)} Bias select current	V _{I(SEL)} = 0	25°C	-100			-130			nA
I _{DD} Supply current	V _O = 1 V, V _{IC} = 1 V, No load	25°C	65		250	105		280	μA
		Full range	360			400			

† Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.

5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TLV2341, TLV2341Y
LinCMOS™ PROGRAMMABLE LOW-VOLTAGE
OPERATIONAL AMPLIFIERS
 SLOS110A – MAY 1992 – REVISED AUGUST 1994

MEDIUM-BIAS MODE

operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	T_A	TLV2341I			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_{IC} = 1\text{ V}$, $R_L = 100\text{ k}\Omega$, See Figure 92	$V_{I(PP)} = 1\text{ V}$, $C_L = 20\text{ pF}$	25°C	0.38		$\text{V}/\mu\text{s}$
			85°C	0.29		
V_n Equivalent input noise voltage	$f = \text{kHz}$, See Figure 93	$R_S = 20\ \Omega$, 25°C	32			$\text{nV}/\sqrt{\text{Hz}}$
BOM Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 100\text{ k}\Omega$, See Figure 92	25°C	34		kHz	
		85°C	32			
B ₁ Unity-gain bandwidth	$V_I = 10\text{ mV}$, $R_L = 100\text{ k}\Omega$, See Figure 94	25°C	300		kHz	
		85°C	235			
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$, See Figure 94	$f = B_1$, $R_L = 100\text{ k}\Omega$, -40°C	42°			
		25°C	39°			
		85°C	36°			

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A	TLV2341I			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_{IC} = 1\text{ V}$, $R_L = 100\text{ k}\Omega$, $C_L = 20\text{ pF}$, See Figure 92	$V_{I(PP)} = 1\text{ V}$	25°C	0.43		$\text{V}/\mu\text{s}$
			85°C	0.35		
		$V_{I(PP)} = 2.5\text{ V}$	25°C	0.40		
			85°C	0.32		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 93	$R_S = 20\ \Omega$, 25°C	32			$\text{nV}/\sqrt{\text{Hz}}$
BOM Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 100\text{ k}\Omega$, See Figure 92	25°C	55		kHz	
		85°C	45			
B ₁ Unity-gain bandwidth	$V_I = 10\text{ mV}$, $R_L = 100\text{ k}\Omega$, See Figure 94	25°C	525		kHz	
		85°C	370			
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$, See Figure 94	$f = B_1$, $R_L = 100\text{ k}\Omega$, -40°C	43°			
		25°C	40°			
		85°C	38°			



MEDIUM-BIAS MODE

electrical characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLV2341I						UNIT
		$V_{DD} = 3\text{ V}$			$V_{DD} = 5\text{ V}$			
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 1\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 1\text{ V}$, $R_L = 100\text{ k}\Omega$		0.6	8		1.1	8	mV
I_{IO} Input offset current (see Note 4)	$V_O = 1\text{ V}$, $V_{IC} = 1\text{ V}$		0.1			0.1		pA
I_{IB} Input bias current (see Note 4)	$V_O = 1\text{ V}$, $V_{IC} = 1\text{ V}$		0.6			0.6		pA
V_{ICR} Common-mode input voltage range (see Note 5)		-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2		V
V_{OH} High-level output voltage	$V_{IC} = 1\text{ V}$, $I_{OH} = -1\text{ mA}$, $V_{ID} = 100\text{ mV}$	1.75	1.9		3.2	3.9		V
V_{OL} Low-level output voltage	$V_{IC} = 1\text{ V}$, $I_{OL} = 1\text{ mA}$, $V_{ID} = -100\text{ mV}$		115	150		95	150	mV
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 1\text{ V}$, $R_L = 100\text{ k}\Omega$, See Note 6	25	83		25	170		V/mV
CMRR Common-mode rejection ratio	$V_O = 1\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = V_{ICRmin}$	65	92		65	91		dB
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	$V_O = 1\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 1\text{ V}$	70	94		70	94		dB
$I_{I(SEL)}$ Bias select current	$V_{I(SEL)} = 0$		-100			-130		nA
I_{DD} Supply current	$V_O = 1\text{ V}$, No load, $V_{IC} = 1\text{ V}$		65	250		105	280	μA

- NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
 5. This range also applies to each input individually.
 6. At $V_{DD} = 5\text{ V}$, $V_O = 0.25\text{ V}$ to 2 V ; at $V_{DD} = 3\text{ V}$, $V_O = 0.5\text{ V}$ to 1.5 V .

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

Table of Graphs

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I_{IB}	Input bias current	vs Temperature	46
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V_{IC}	Common-mode input voltage	vs Supply voltage	47
I_{DD}	Supply current	vs Supply voltage	48
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SR	Slew rate	vs Supply voltage	50
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$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	53
B_1	Unity-gain bandwidth	vs Temperature	54
		vs Supply voltage	55
ϕ_m	Phase margin	vs Supply voltage	58
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		vs Load capacitance	60
V_n	Equivalent input noise voltage	vs Frequency	61
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TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

DISTRIBUTION OF TLV2341
 INPUT OFFSET VOLTAGE

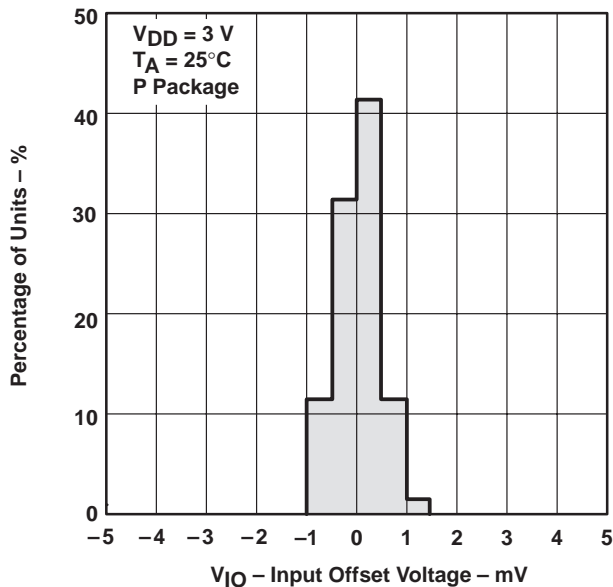


Figure 32

DISTRIBUTION OF TLV2341
 INPUT OFFSET VOLTAGE

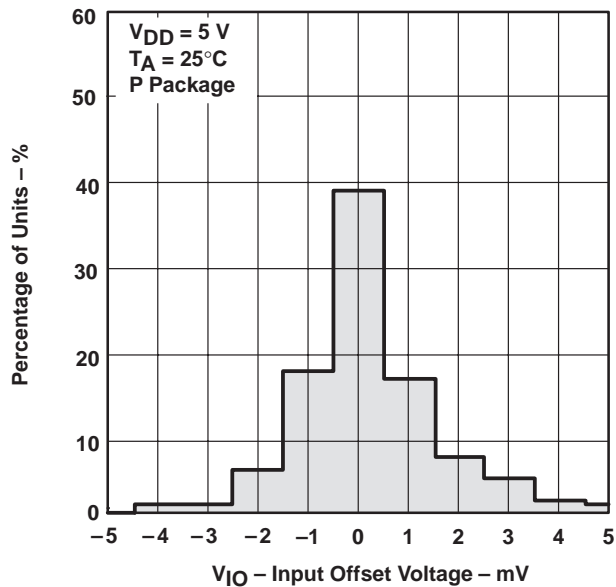


Figure 33

DISTRIBUTION OF TLV2341
 INPUT OFFSET VOLTAGE
 TEMPERATURE COEFFICIENT

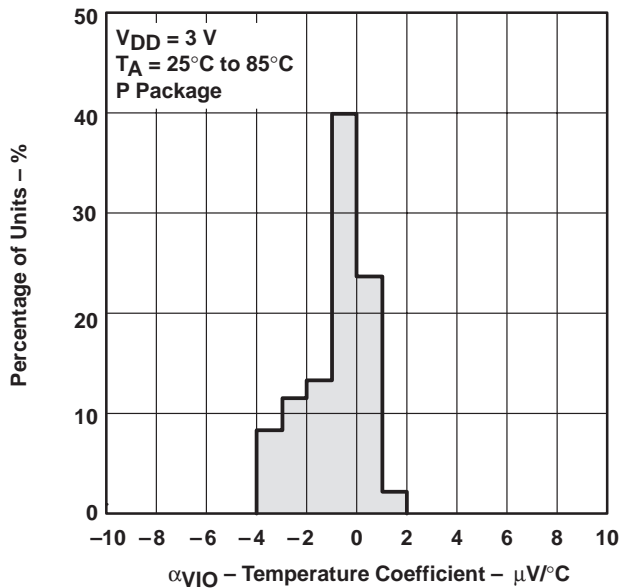


Figure 34

DISTRIBUTION OF TLV2341
 INPUT OFFSET VOLTAGE
 TEMPERATURE COEFFICIENT

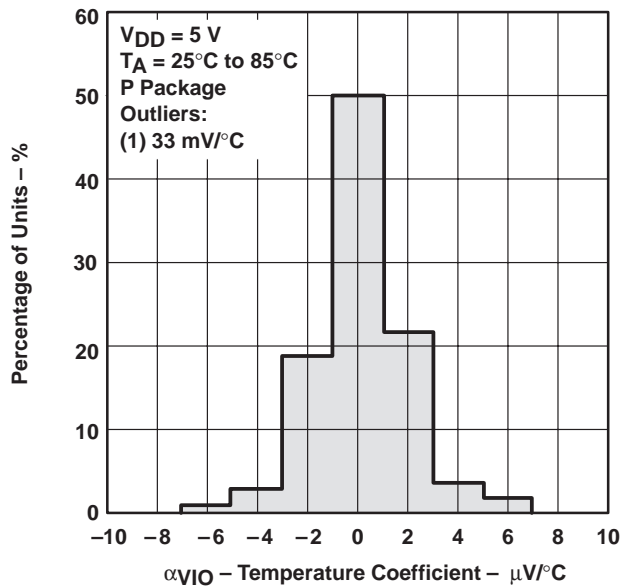


Figure 35

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

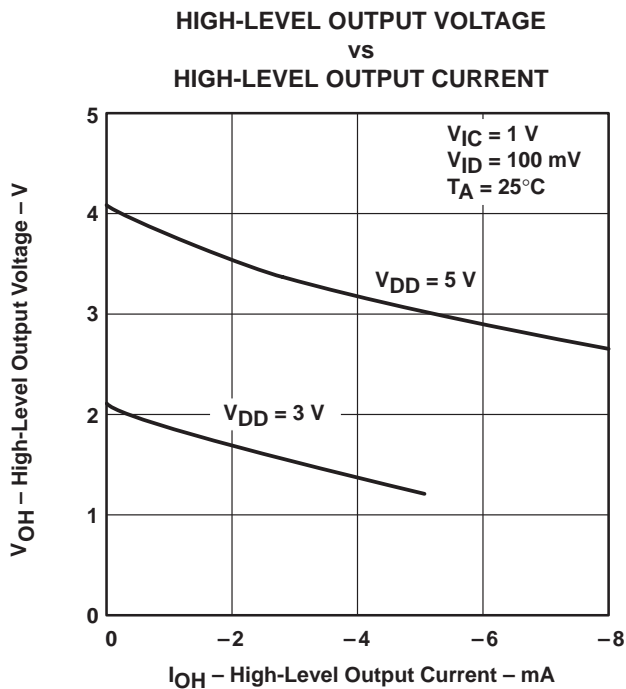


Figure 36

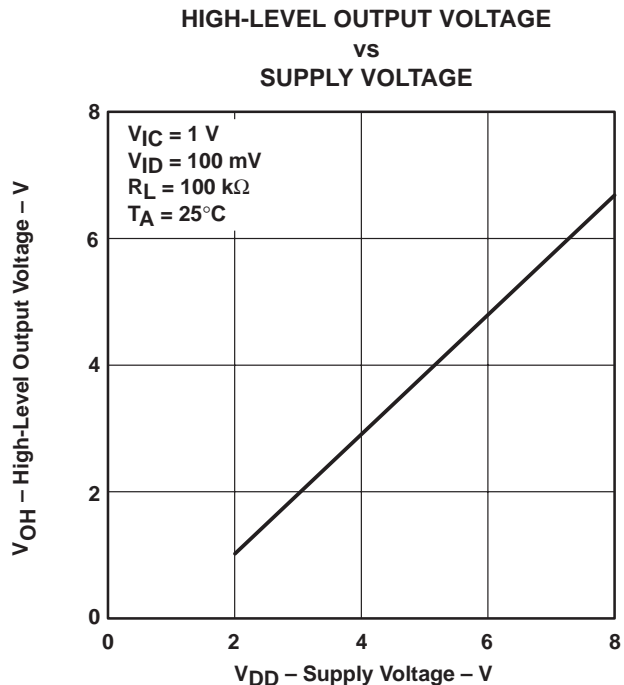


Figure 37

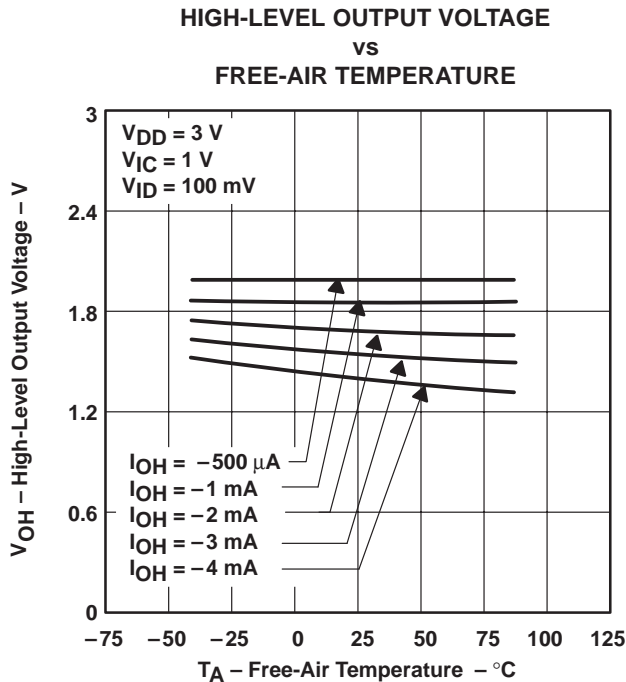


Figure 38

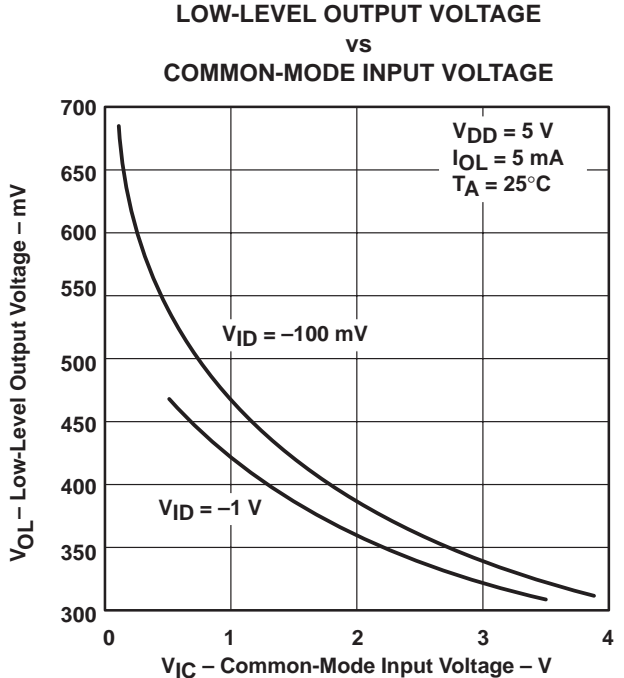


Figure 39

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

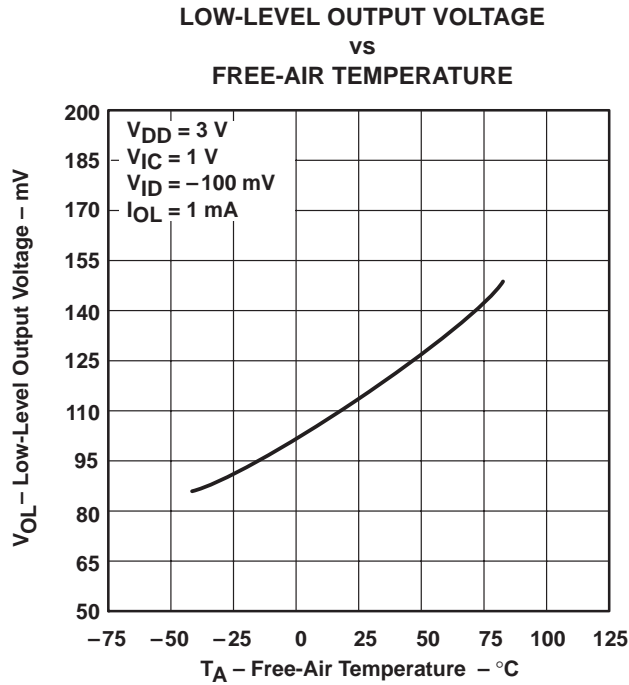


Figure 40

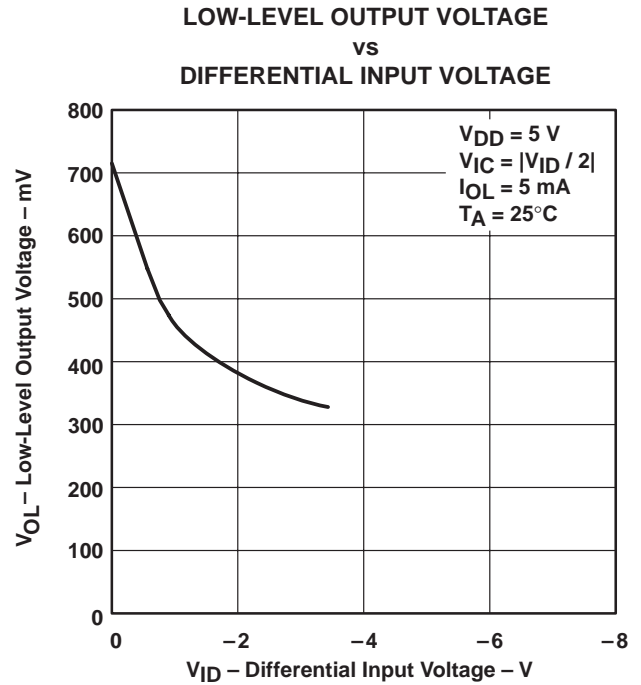


Figure 41

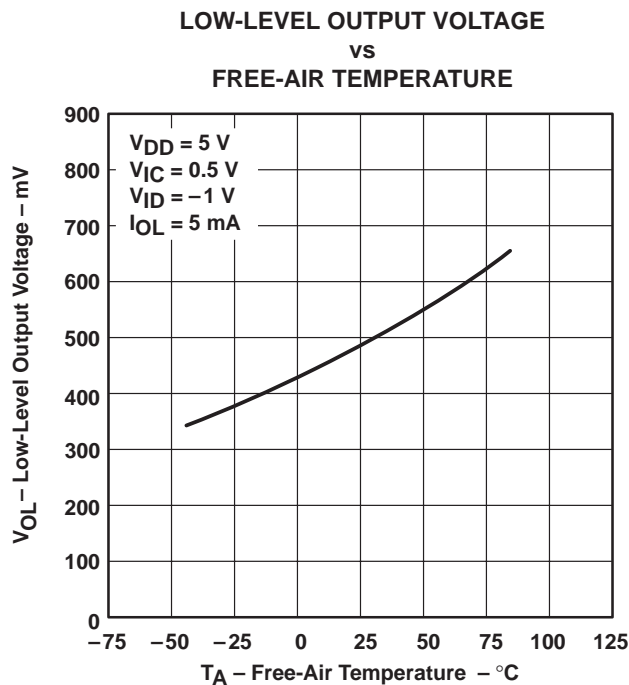


Figure 42

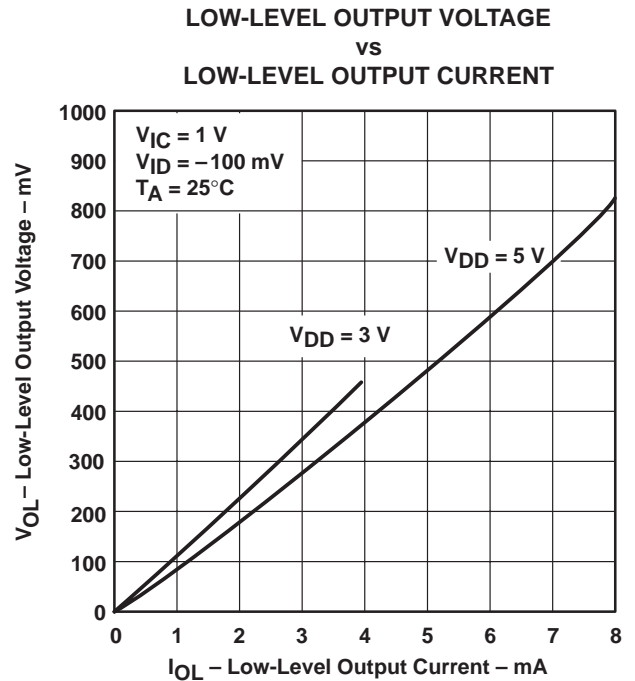


Figure 43

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

**LARGE-SIGNAL
 DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 SUPPLY VOLTAGE**

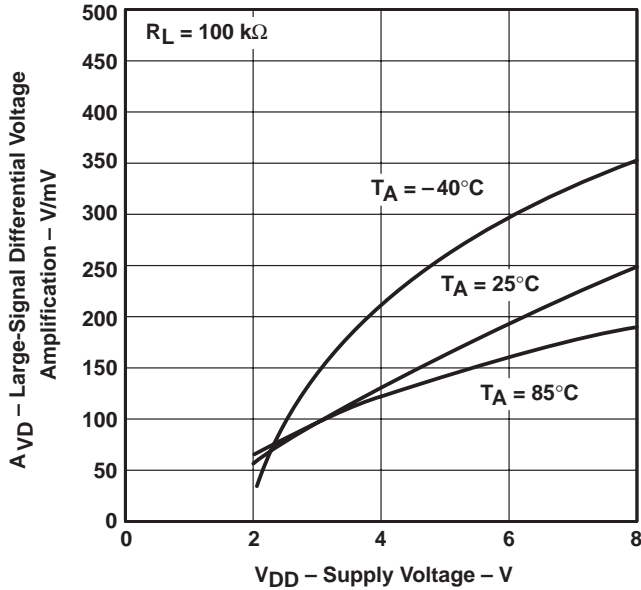


Figure 44

**LARGE-SIGNAL
 DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 FREE-AIR TEMPERATURE**

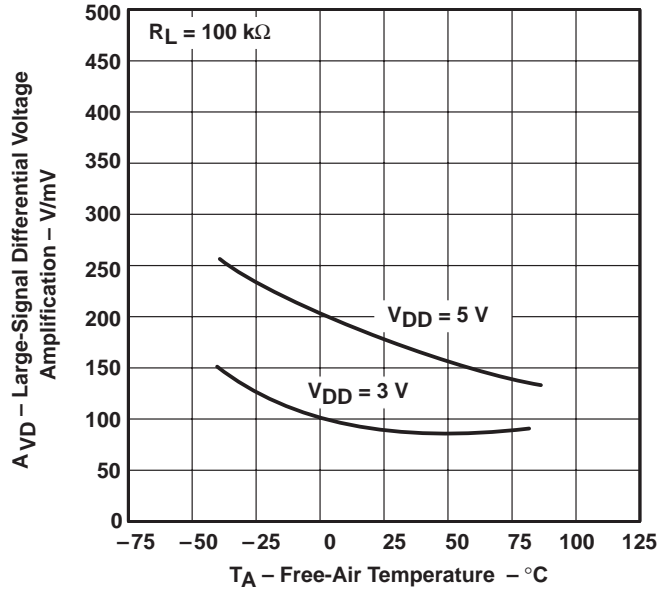


Figure 45

**INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
 vs
 FREE-AIR TEMPERATURE**

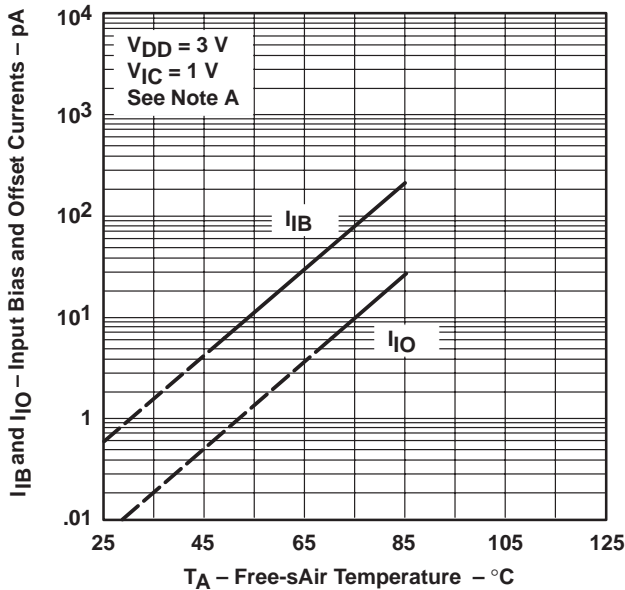


Figure 46

**COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT
 vs
 SUPPLY VOLTAGE**

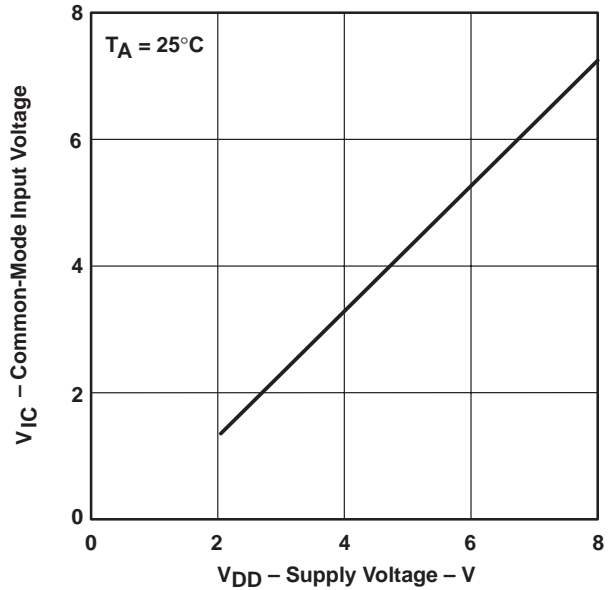


Figure 47

NOTE A: The typical values of input bias current and input offset current below 5 pA are determined mathematically.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

SUPPLY CURRENT
 vs
 SUPPLY VOLTAGE

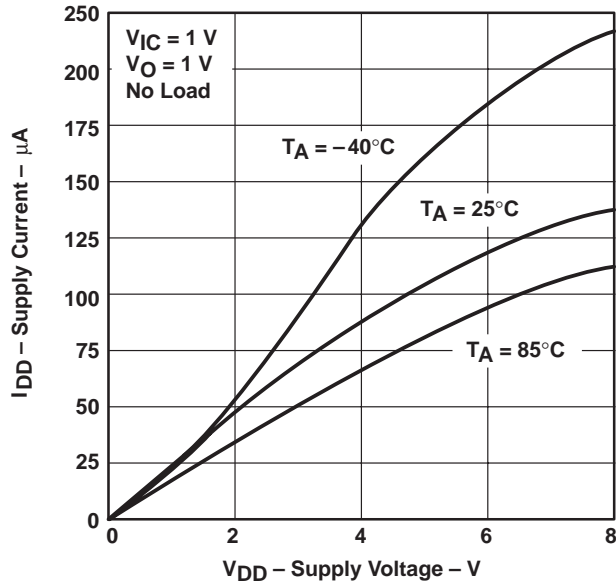


Figure 48

SUPPLY CURRENT
 vs
 FREE-AIR TEMPERATURE

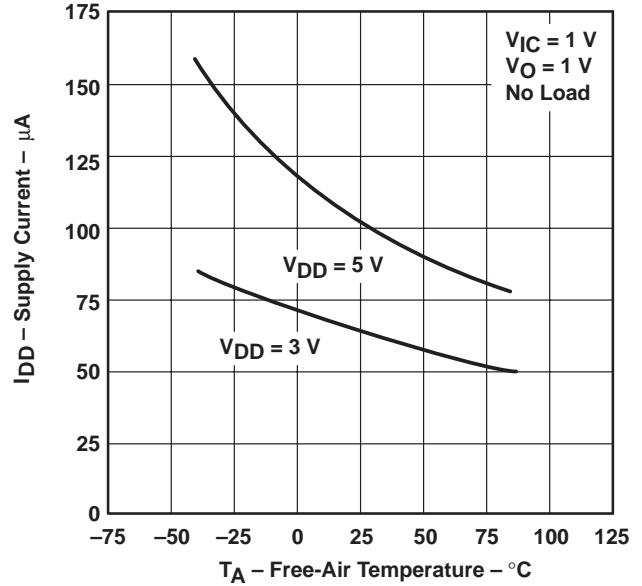


Figure 49

SLEW RATE
 vs
 SUPPLY VOLTAGE

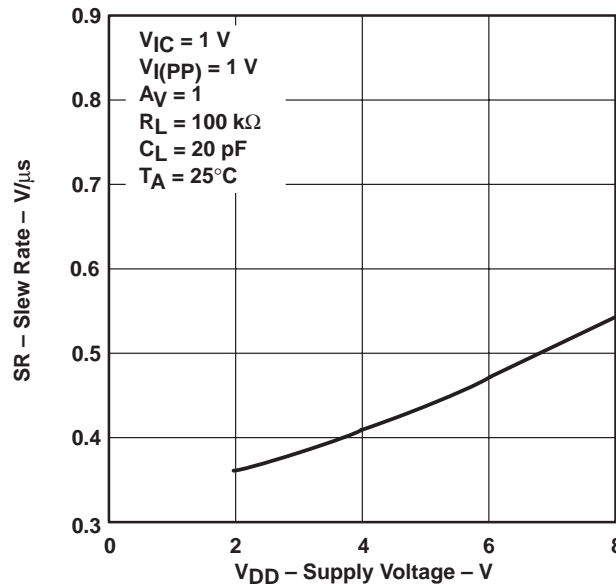


Figure 50

SLEW RATE
 vs
 FREE-AIR TEMPERATURE

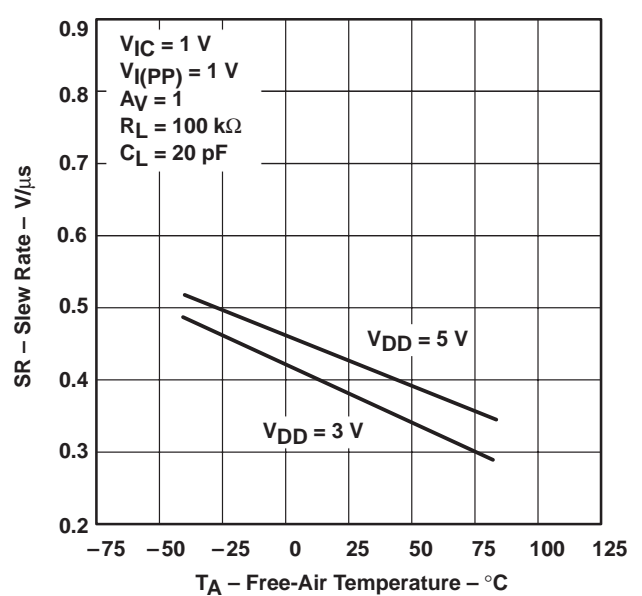


Figure 51

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

**BIAS SELECT CURRENT
 vs
 SUPPLY VOLTAGE**

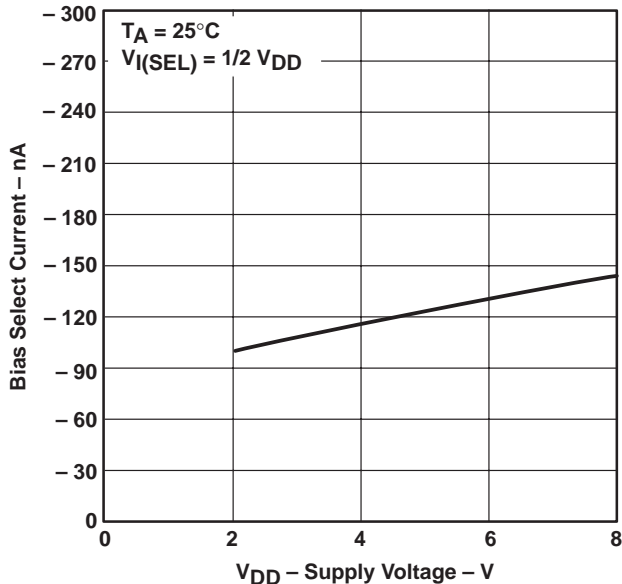


Figure 52

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
 vs
 FREQUENCY**

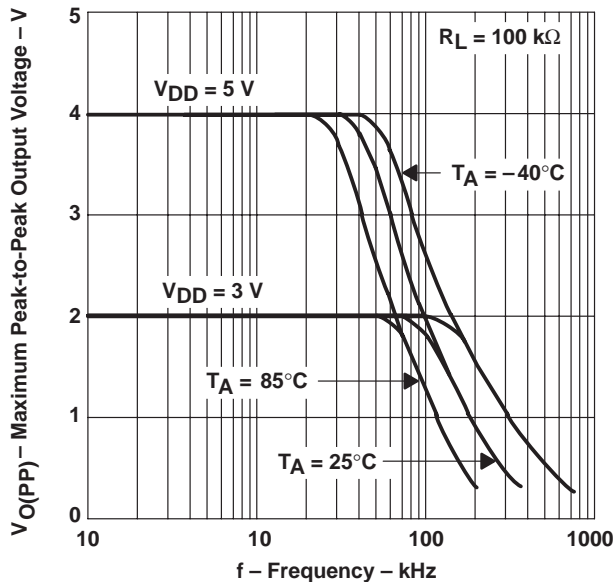


Figure 53

**UNITY-GAIN BANDWIDTH
 vs
 FREE-AIR TEMPERATURE**

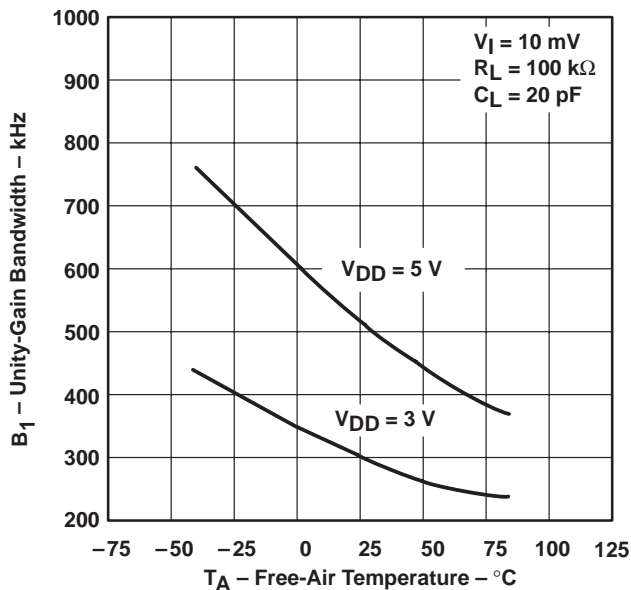


Figure 54

**UNITY-GAIN BANDWIDTH
 vs
 SUPPLY VOLTAGE**

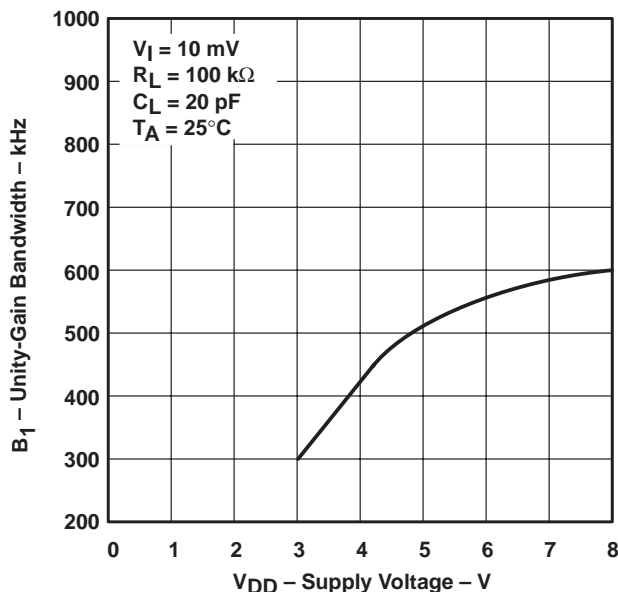


Figure 55

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

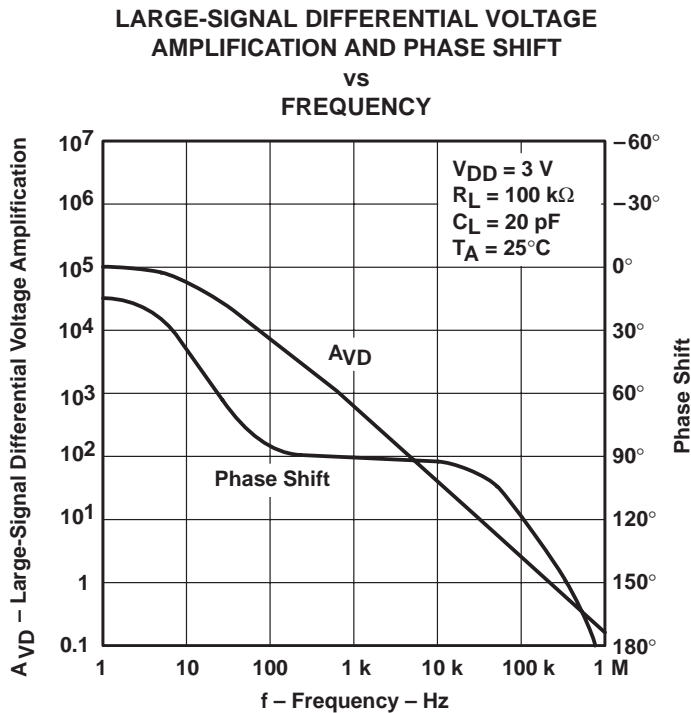


Figure 56

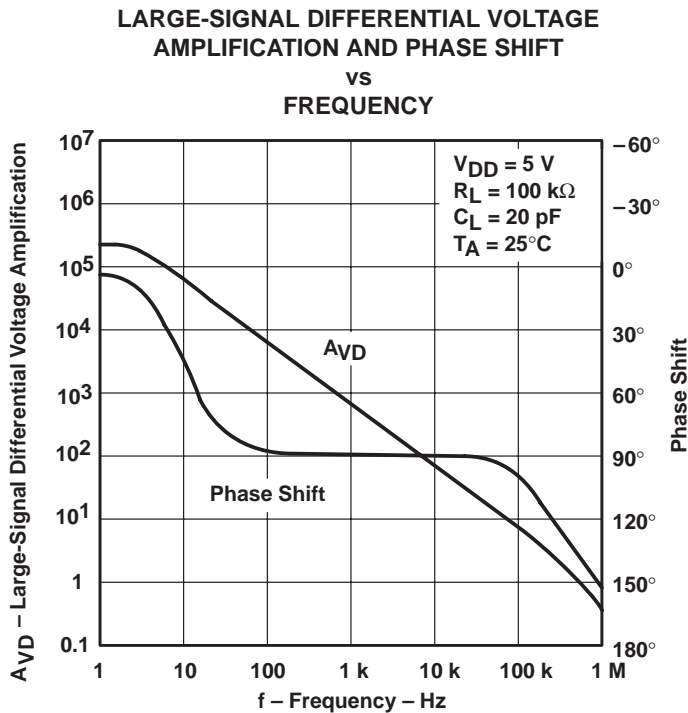


Figure 57

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

**PHASE MARGIN
 vs
 SUPPLY VOLTAGE**

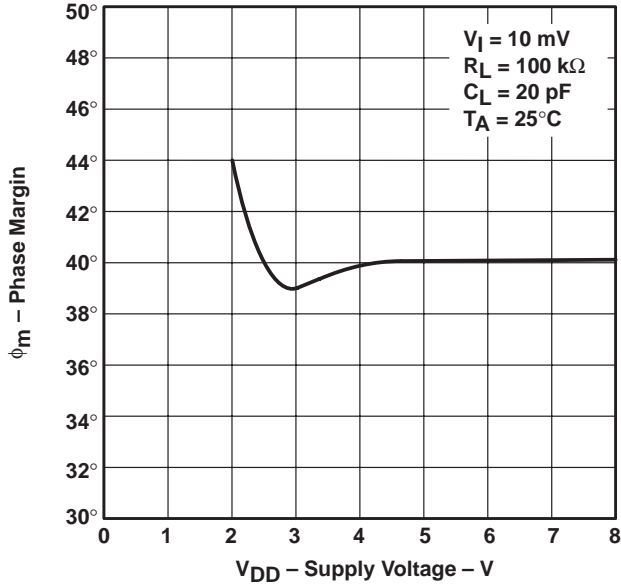


Figure 58

**PHASE MARGIN
 vs
 FREE-AIR TEMPERATURE**

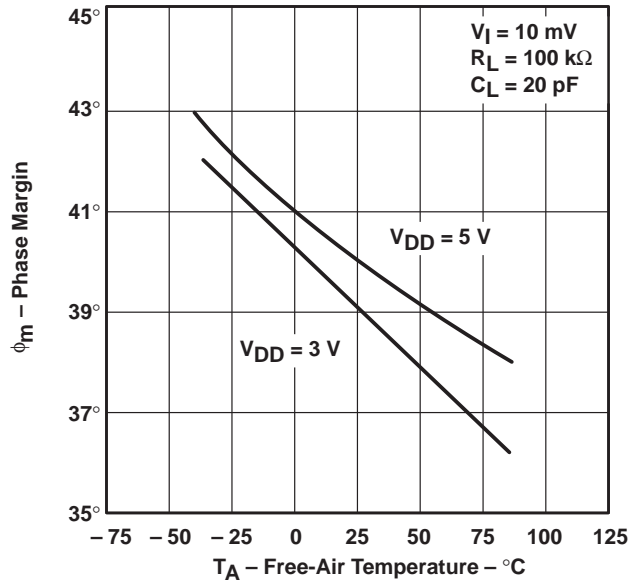


Figure 59

**PHASE MARGIN
 vs
 LOAD CAPACITANCE**

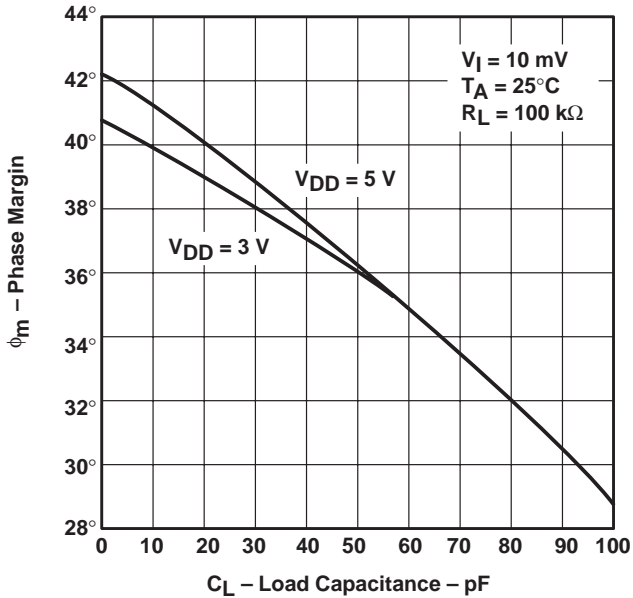


Figure 60

**EQUIVALENT INPUT NOISE VOLTAGE
 vs
 FREQUENCY**

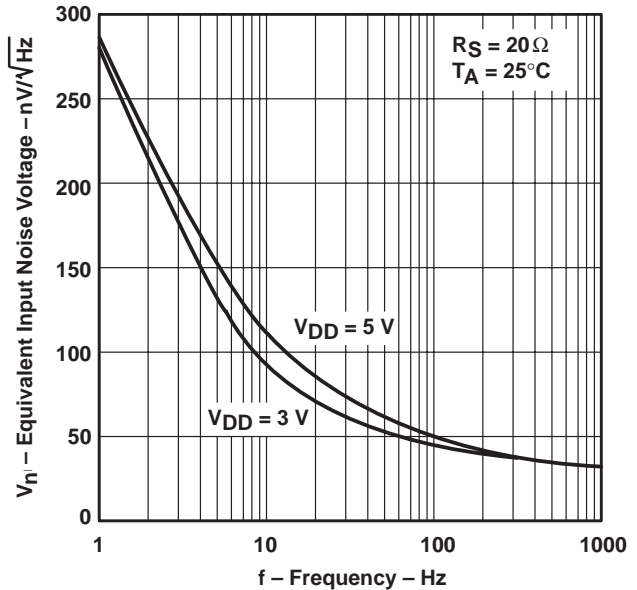


Figure 61

LOW-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T _A †	TLV2341I						UNIT
			V _{DD} = 3 V			V _{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO} Input offset voltage	V _O = 1 V, V _{IC} = 1 V, R _S = 50 Ω, R _L = 1 MΩ	25°C	0.6		8	1.1		8	mV
		Full range			10			10	
α _{VIO} Average temperature of input offset voltage		25°C to 85°C	1			1.1			μV/°C
I _{IO} Input offset current (see Note 4)	V _O = 1 V, V _{IC} = 1 V	25°C	0.1			0.1			pA
		85°C	22	1000		24	1000		
I _{IB} Input bias current (see Note 4)	V _O = 1 V, V _{IC} = 1 V	25°C	0.6			0.6			pA
		85°C	175	2000		200	2000		
V _{ICR} Common-mode input voltage range (see Note 5)		25°C	-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2		V
		Full range	-0.2 to 1.8			-0.2 to 3.8			V
V _{OH} High-level output voltage	V _{IC} = 1 V, V _{ID} = 100 mV, I _{OH} = -1 mA	25°C	1.75	1.9		3.2	3.8		V
		Full range	1.7			3			
V _{OL} Low-level output voltage	V _{IC} = 1 V, V _{ID} = -100 mV, I _{OL} = 1 mA	25°C	115		150	95		150	mV
		Full range			190			190	
A _{VD} Large-signal differential voltage amplification	V _{IC} = 1 V, R _L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
		Full range	50			50			
CMRR Common-mode rejection ratio	V _O = 1 V, V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	65	88		65	94		dB
		Full range	60			60			
k _{SVR} Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{IC} = 1 V, V _O = 1 V, R _S = 50 Ω	25°C	70	86		70	86		dB
		Full range	65			65			
I _{I(SEL)} Bias select current	V _{I(SEL)} = 0	25°C	10			65			nA
I _{DD} Supply current	V _O = 1 V, V _{IC} = 1 V, No load	25°C	5		17	10		17	μA
		Full range			27			27	

† Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.

5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_{O(PP)} = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

LOW-BIAS MODE

operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	T_A	TLV2341I			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_{IC} = 1\text{ V}$, $R_L = 1\text{ M}\Omega$, See Figure 92	$V_{I(PP)} = 1\text{ V}$, $C_L = 20\text{ pF}$, 25°C	0.02			V/ μs
		85°C	0.02			
V_n Equivalent input noise voltage	$f = \text{kHz}$, See Figure 93	$R_S = 20\ \Omega$, 25°C	68			nV/ $\sqrt{\text{Hz}}$
BOM Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 1\text{ M}\Omega$, See Figure 92	25°C	2.5			kHz
		85°C	2			
B ₁ Unity-gain bandwidth	$V_I = 10\text{ mV}$, $R_L = 1\text{ M}\Omega$, See Figure 94	25°C	27			kHz
		85°C	21			
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$, See Figure 94	$f = B_1$, $R_L = 1\text{ M}\Omega$, -40°C	39°			
		25°C	34°			
		85°C	28°			

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A	TLV2341I			UNIT	
			MIN	TYP	MAX		
SR Slew rate at unity gain	$V_{IC} = 1\text{ V}$, $R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$, See Figure 92	$V_{I(PP)} = 1\text{ V}$	25°C	0.03			V/ μs
			85°C	0.03			
		$V_{I(PP)} = 2.5\text{ V}$	25°C	0.03			
			85°C	0.02			
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 93	$R_S = 20\ \Omega$, 25°C	68			nV/ $\sqrt{\text{Hz}}$	
BOM Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 1\text{ M}\Omega$, See Figure 92	25°C	5			kHz	
		85°C	4				
B ₁ Unity-gain bandwidth	$V_I = 10\text{ mV}$, $R_L = 1\text{ M}\Omega$, See Figure 94	25°C	85			kHz	
		85°C	55				
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$, See Figure 94	$f = B_1$, $R_L = 1\text{ M}\Omega$, -40°C	38°				
		25°C	34°				
		85°C	28°				

LOW-BIAS MODE

electrical characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLV2341Y						UNIT
		$V_{DD} = 3\text{ V}$			$V_{DD} = 5\text{ V}$			
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 1\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 1\text{ V}$, $R_L = 1\text{ M}\Omega$		0.6	8		1.1	8	mV
I_{IO} Input offset current (see Note 4)	$V_O = 1\text{ V}$, $V_{IC} = 1\text{ V}$		0.1			0.1		pA
I_{IB} Input bias current (see Note 4)	$V_O = 1\text{ V}$, $V_{IC} = 1\text{ V}$		0.6			0.6		pA
V_{ICR} Common-mode input voltage range (see Note 5)		-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2		V
V_{OH} High-level output voltage	$V_{IC} = 1\text{ V}$, $I_{OH} = -1\text{ mA}$, $V_{ID} = 100\text{ mV}$,	1.75	1.9		3.2	3.8		V
V_{OL} Low-level output voltage	$V_{IC} = 1\text{ V}$, $I_{OL} = 1\text{ mA}$, $V_{ID} = -100\text{ mV}$,		115	150		95	150	mV
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 1\text{ V}$, See Note 6, $R_L = 1\text{ M}\Omega$,	50	400		50	520		V/mV
CMRR Common-mode rejection ratio	$V_O = 1\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = V_{ICRmin}$,	65	88		65	94		dB
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	$V_{DD} = 3\text{ V to } 5\text{ V}$, $V_O = 1\text{ V}$, $V_{IC} = 1\text{ V}$, $R_S = 50\ \Omega$	70	86		70	86		dB
$I_{I(SEL)}$ Bias select current	$V_{I(SEL)} = 0$		10			65		nA
I_{DD} Supply current	$V_O = 1\text{ V}$, No load, $V_{IC} = 1\text{ V}$,		5	17		10	17	μA

- NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
 5. This range also applies to each input individually.
 6. At $V_{DD} = 5\text{ V}$, $V_O = 0.25\text{ V to } 2\text{ V}$; at $V_{DD} = 3\text{ V}$, $V_O = 0.5\text{ V to } 1.5\text{ V}$.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

Table of Graphs

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V_{IC}	Common-mode input voltage	vs Supply voltage	77
I_{DD}	Supply current	vs Supply voltage	78
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SR	Slew rate	vs Supply voltage	80
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$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	83
B_1	Unity-gain bandwidth	vs Temperature	84
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ϕ_m	Phase margin	vs Supply voltage	88
		vs Temperature	89
		vs Load capacitance	90
V_n	Equivalent input noise voltage	vs Frequency	91
		Phase shift	86, 87

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

DISTRIBUTION OF TLV2341
 INPUT OFFSET VOLTAGE

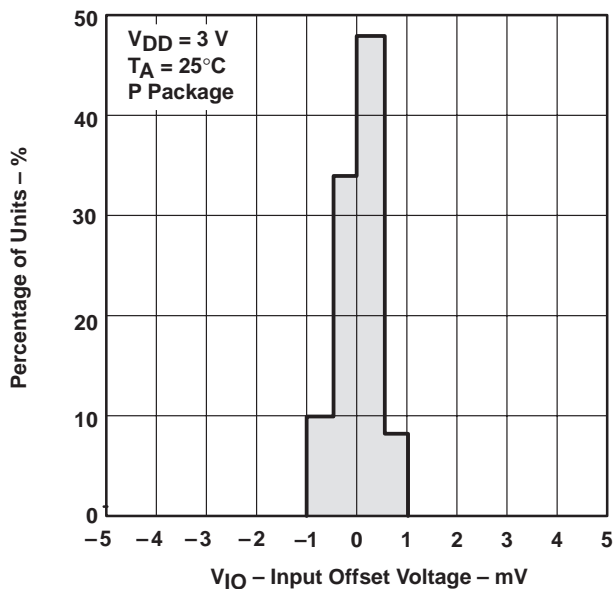


Figure 62

DISTRIBUTION OF TLV2341
 INPUT OFFSET VOLTAGE

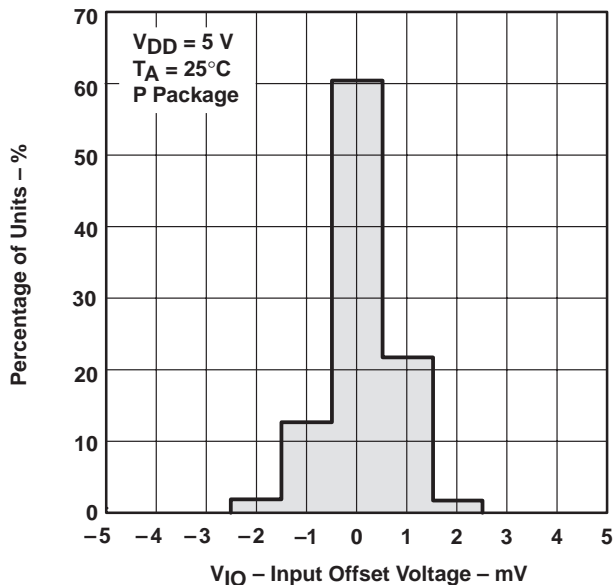


Figure 63

DISTRIBUTION OF TLV2341
 INPUT OFFSET VOLTAGE
 TEMPERATURE COEFFICIENT

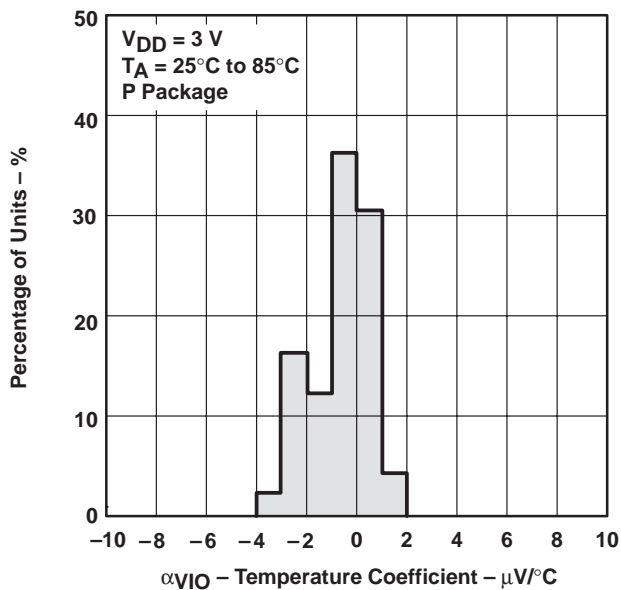


Figure 64

DISTRIBUTION OF TLV2341
 INPUT OFFSET VOLTAGE
 TEMPERATURE COEFFICIENT

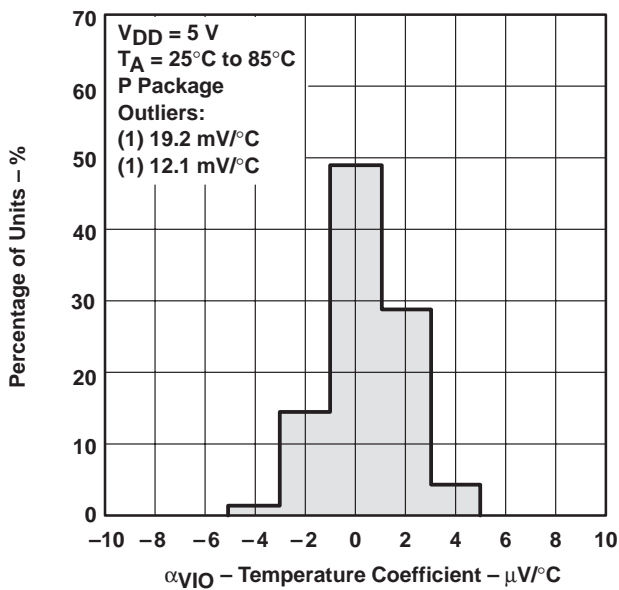
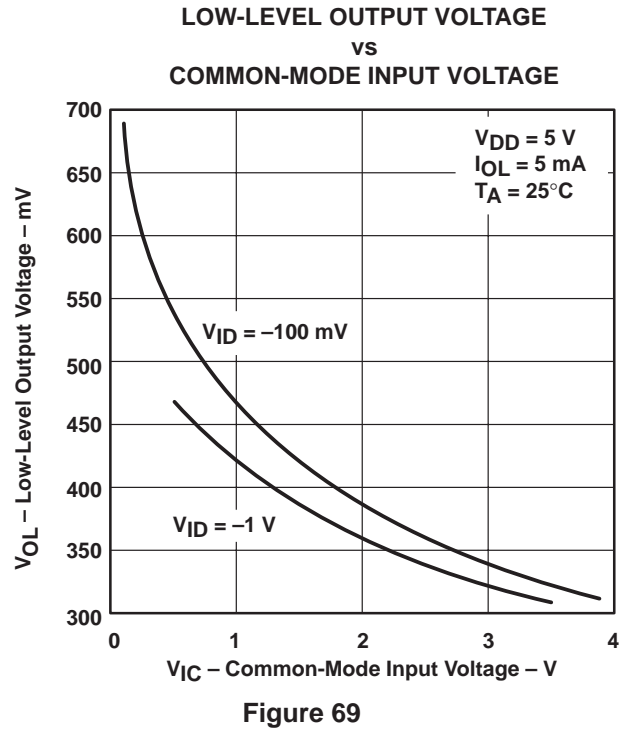
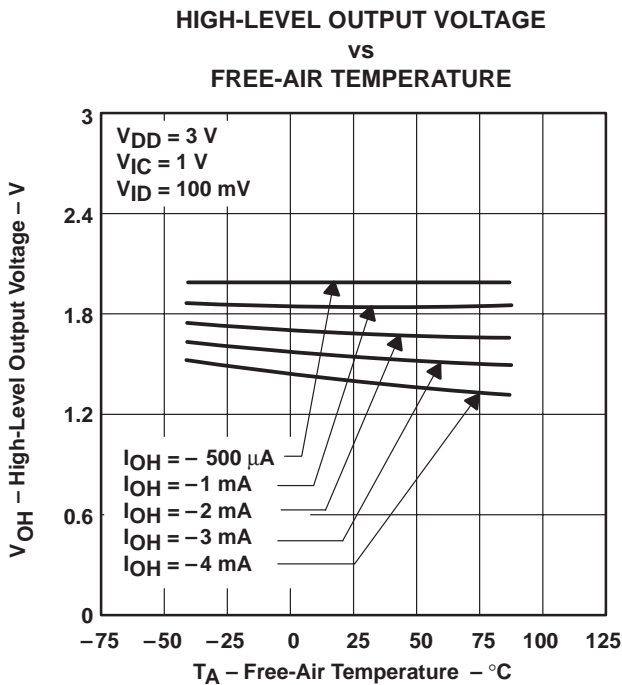
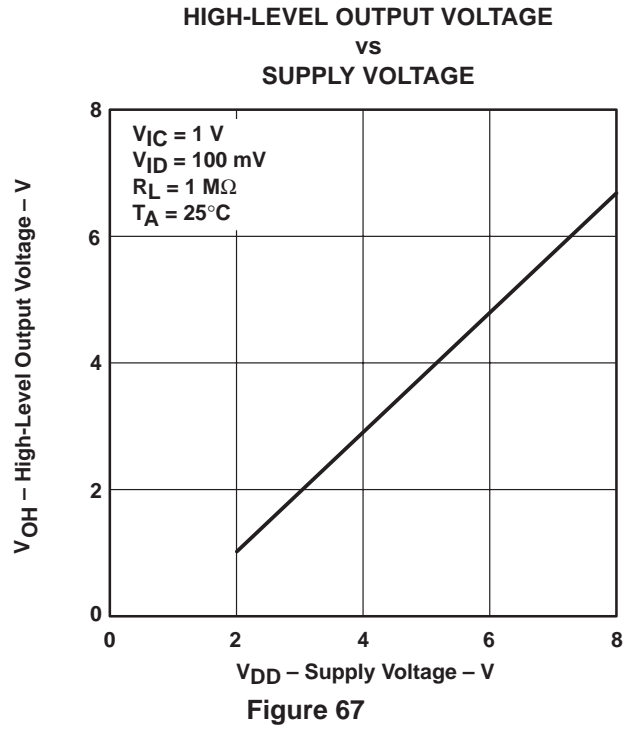
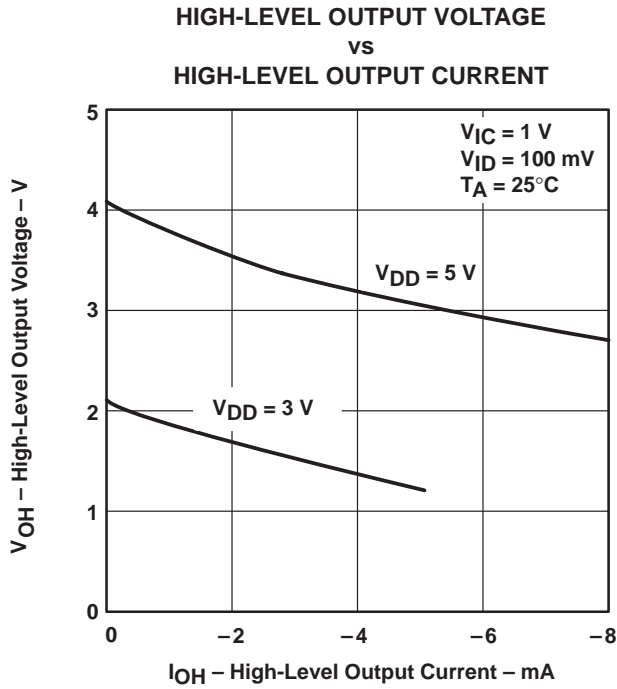


Figure 65

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)



TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

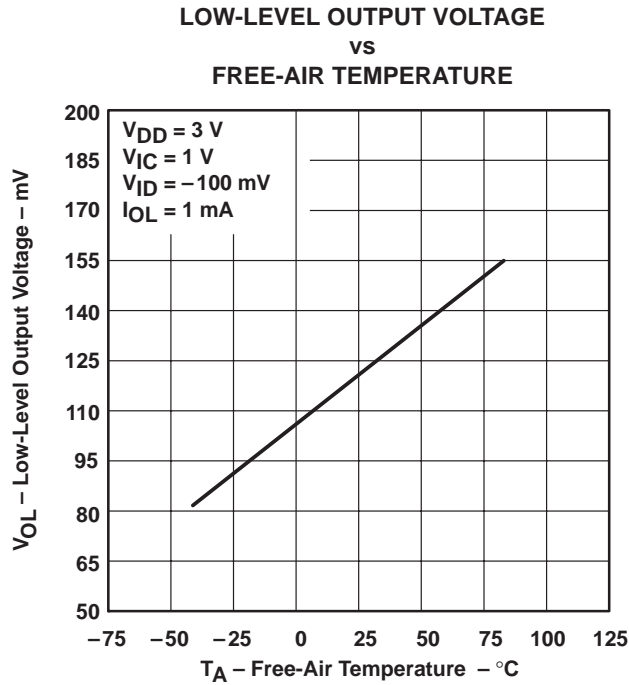


Figure 70

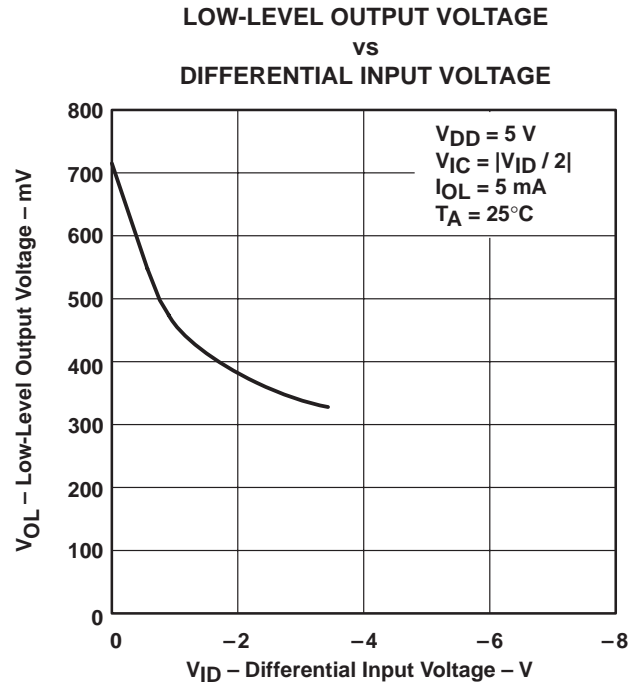


Figure 71

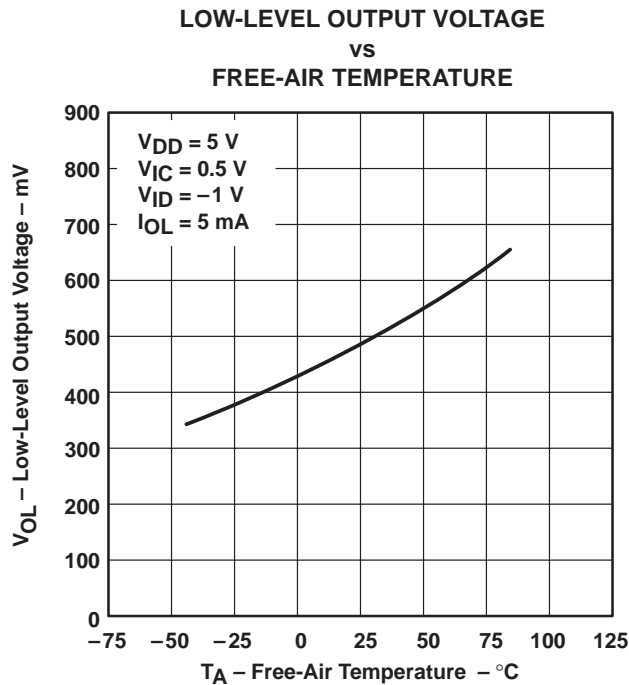


Figure 72

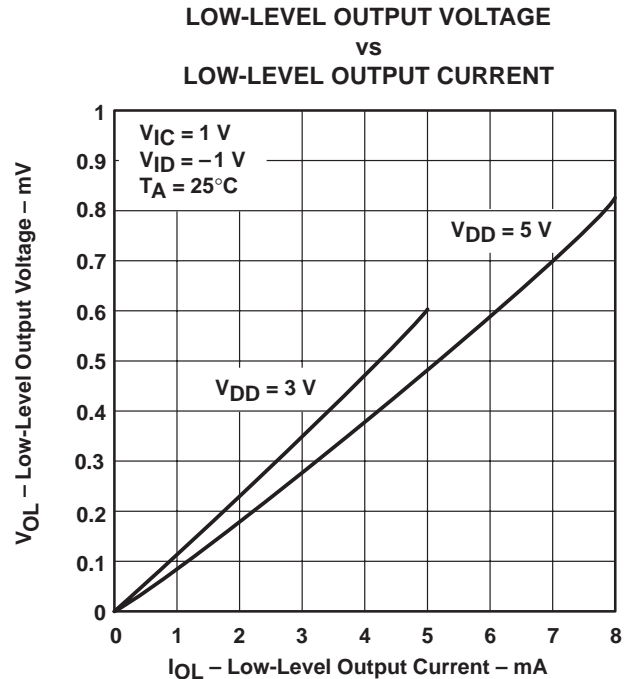


Figure 73

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

**LARGE-SIGNAL
 DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 SUPPLY VOLTAGE**

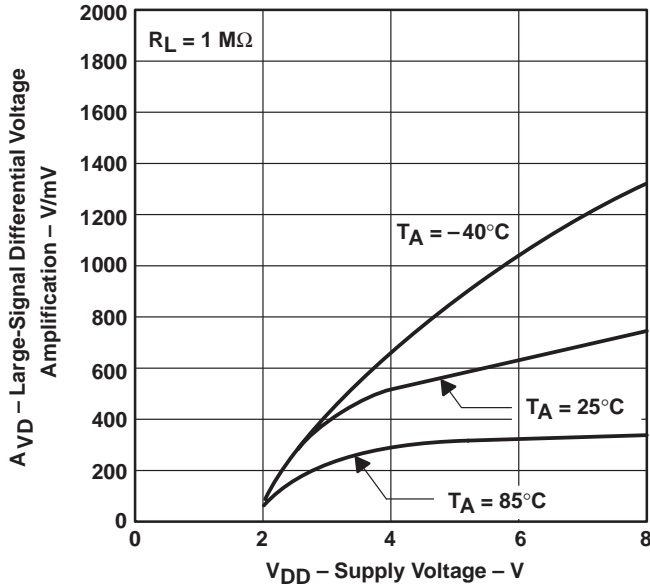


Figure 74

**LARGE-SIGNAL
 DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 FREE-AIR TEMPERATURE**

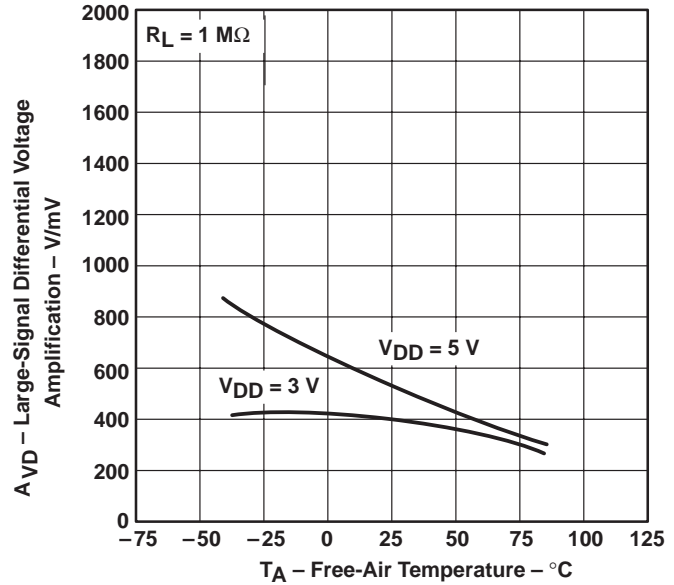


Figure 75

**INPUT BIAS CURRENT AND INPUT
 OFFSET CURRENT
 vs
 FREE-AIR TEMPERATURE**

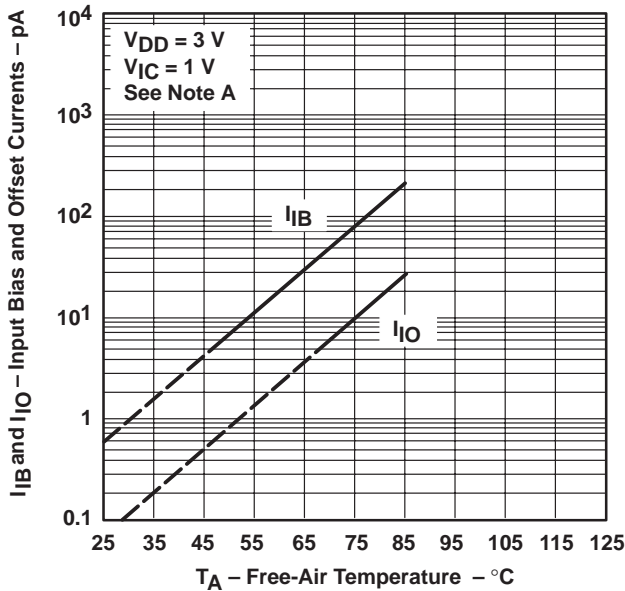


Figure 76

**COMMON-MODE INPUT VOLTAGE
 POSITIVE LIMIT
 vs
 SUPPLY VOLTAGE**

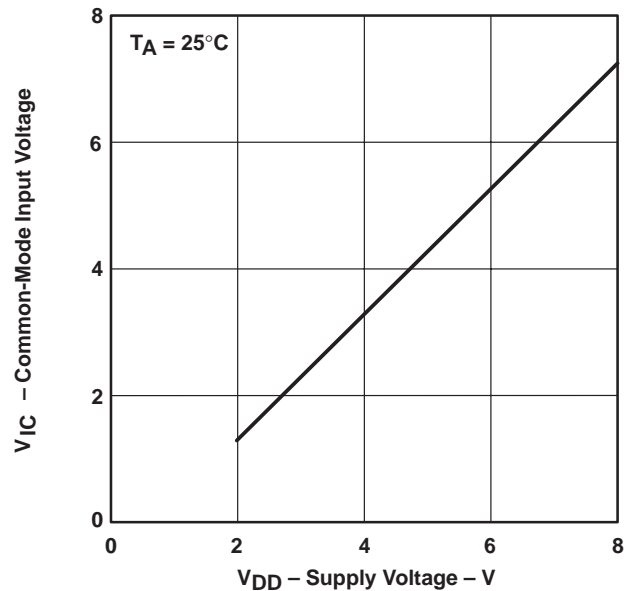


Figure 77

NOTE A: The typical values of input bias current and input offset current below 5 pA are determined mathematically.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

SUPPLY CURRENT
 vs
 SUPPLY VOLTAGE

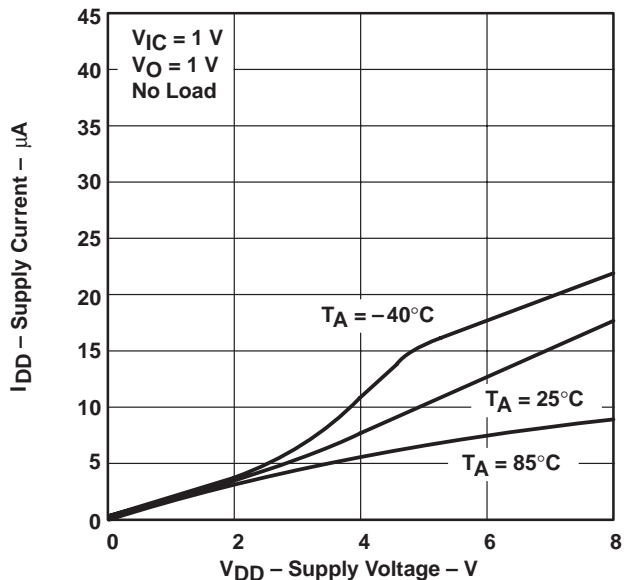


Figure 78

SUPPLY CURRENT
 vs
 FREE-AIR TEMPERATURE

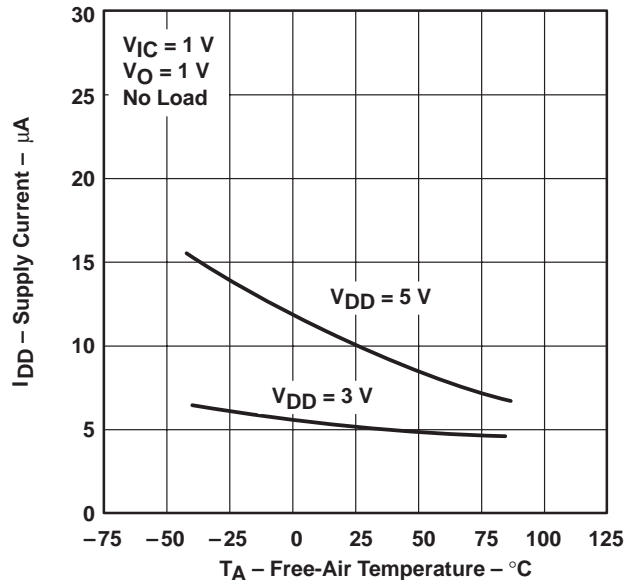


Figure 79

SLEW RATE
 vs
 SUPPLY VOLTAGE

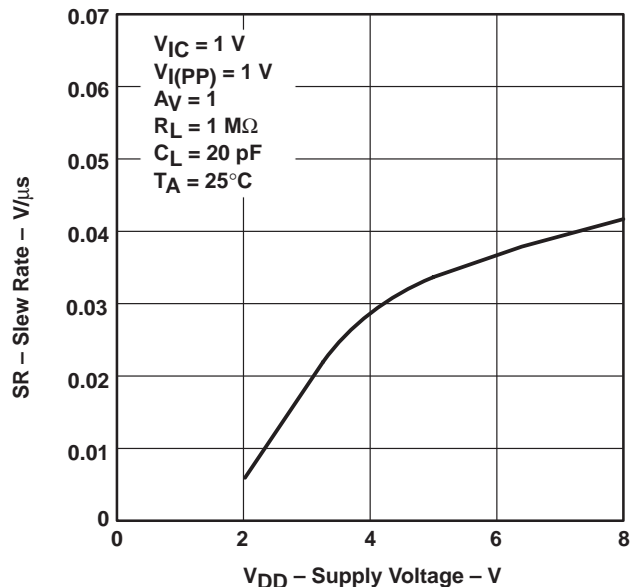


Figure 80

SLEW RATE
 vs
 FREE-AIR TEMPERATURE

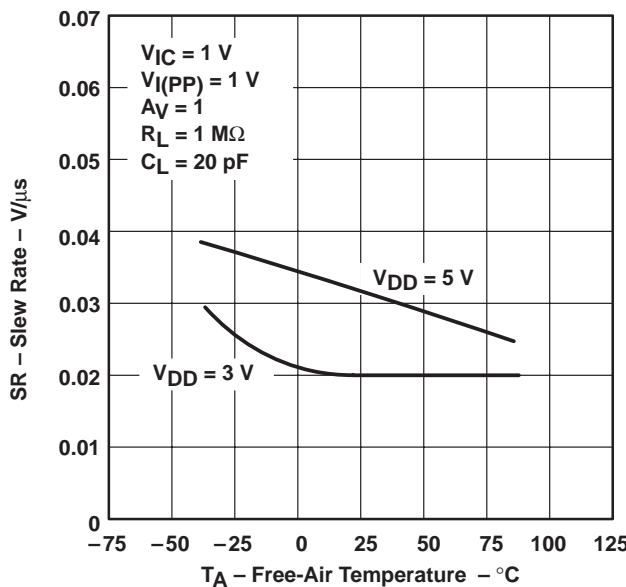


Figure 81

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

BIAS SELECT CURRENT
 vs
 SUPPLY VOLTAGE

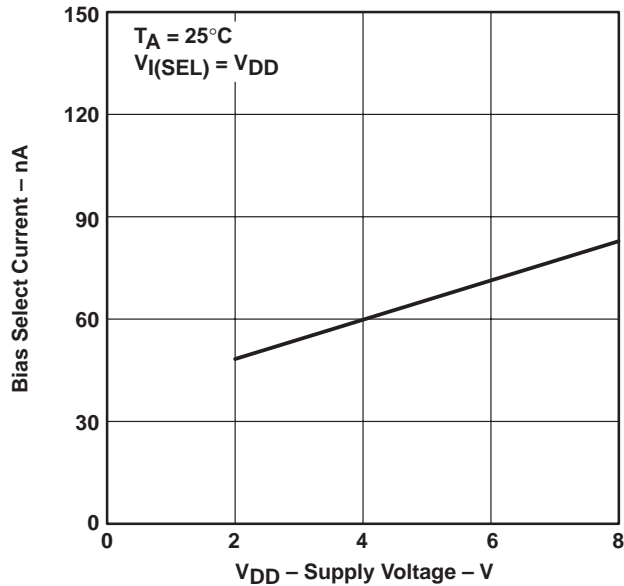


Figure 82

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
 vs
 FREQUENCY

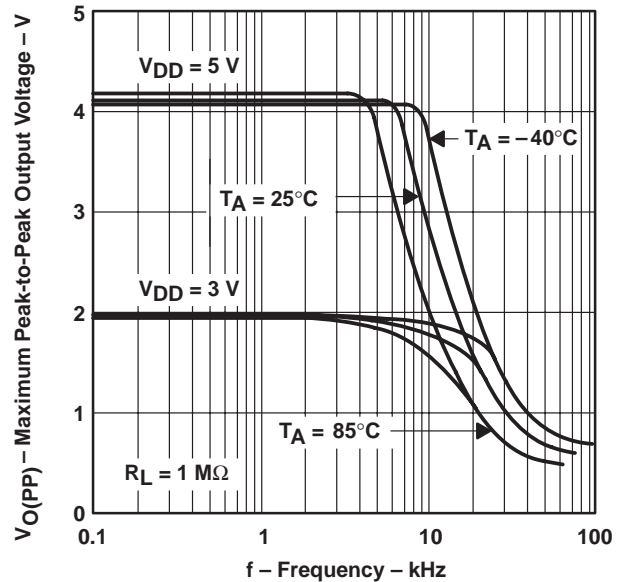


Figure 83

UNITY-GAIN BANDWIDTH
 vs
 FREE-AIR TEMPERATURE

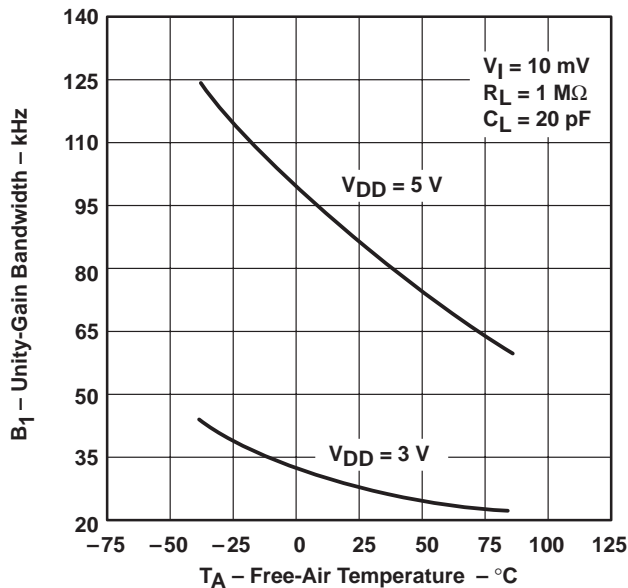


Figure 84

UNITY-GAIN BANDWIDTH
 vs
 SUPPLY VOLTAGE

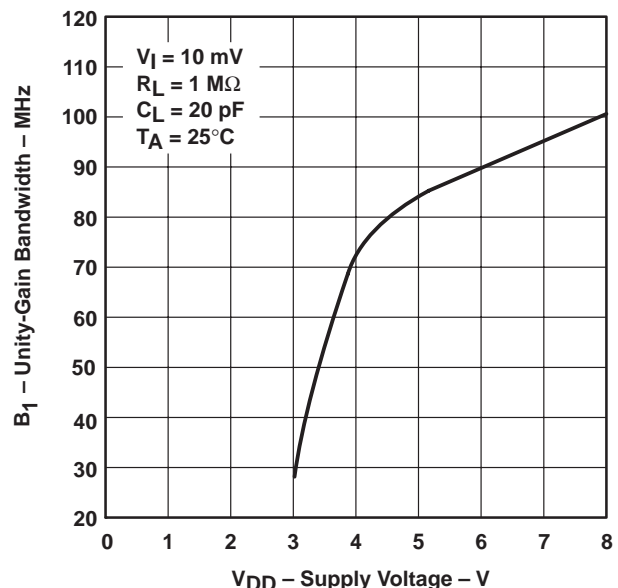


Figure 85

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

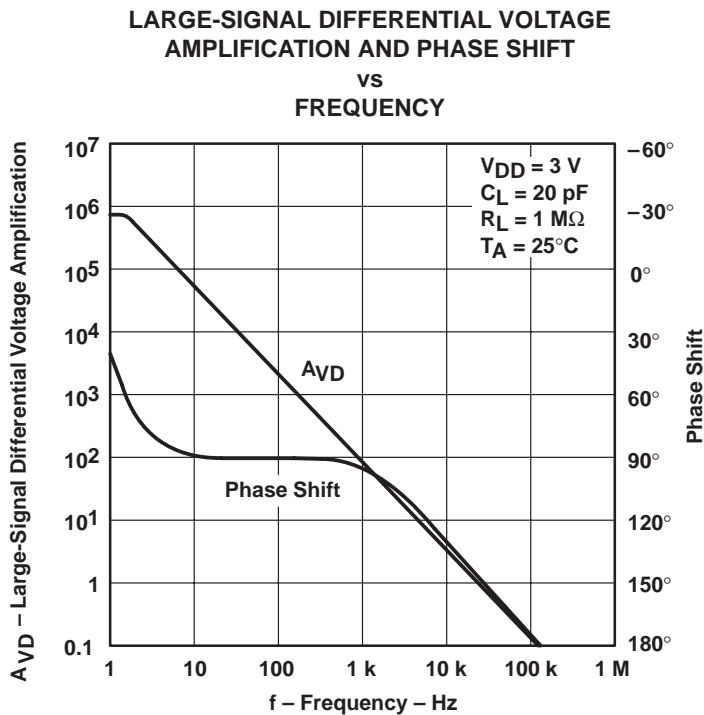


Figure 86

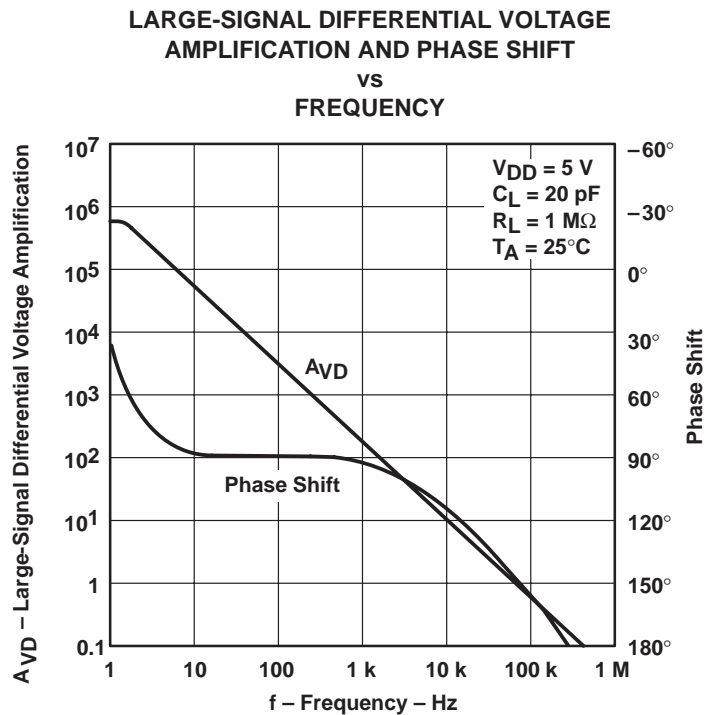


Figure 87

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

**PHASE MARGIN
 vs
 SUPPLY VOLTAGE**

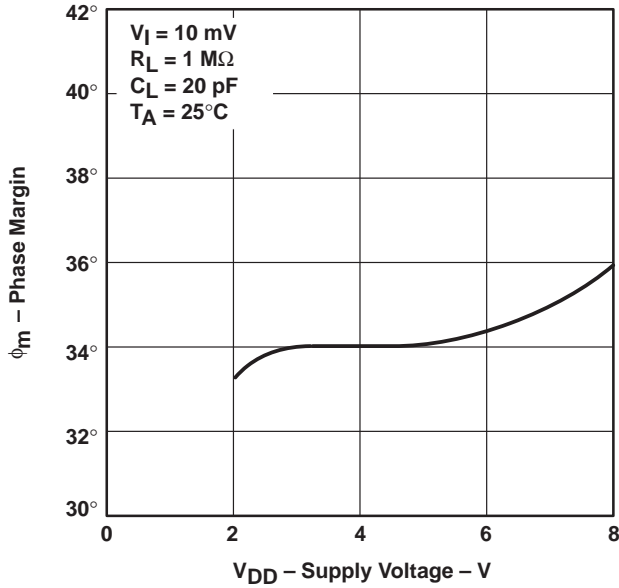


Figure 88

**PHASE MARGIN
 vs
 FREE-AIR TEMPERATURE**

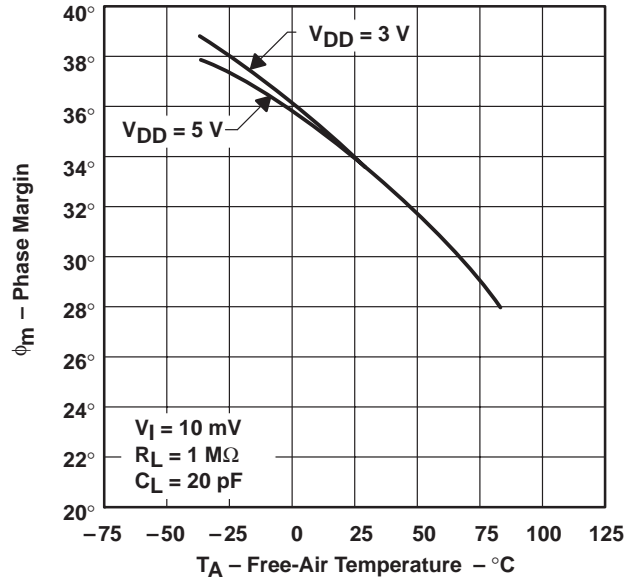


Figure 89

**PHASE MARGIN
 vs
 LOAD CAPACITANCE**

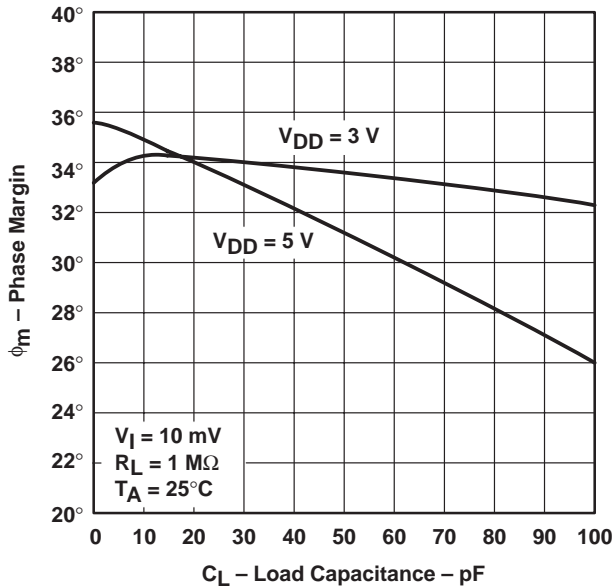


Figure 90

**EQUIVALENT INPUT NOISE VOLTAGE
 vs
 FREQUENCY**

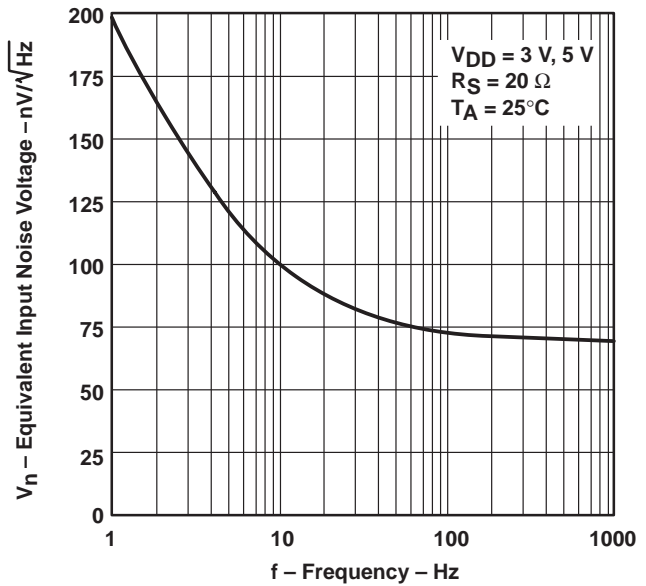


Figure 91

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2341 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

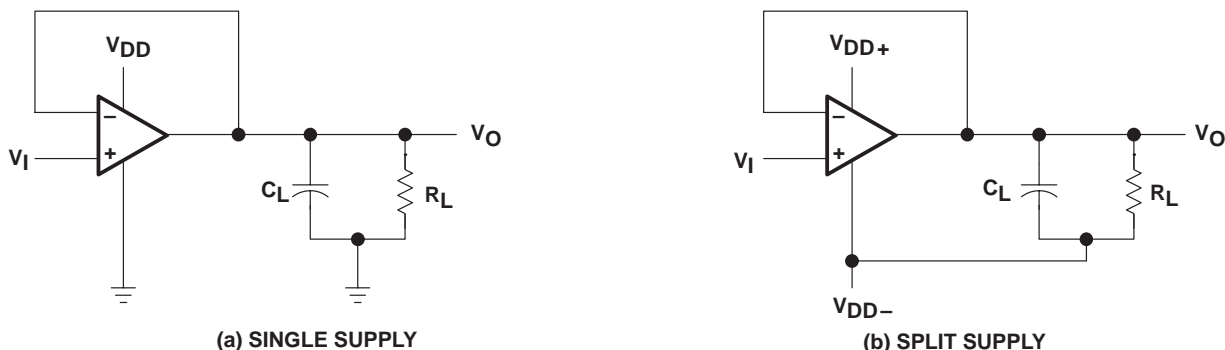


Figure 92. Unity-Gain Amplifier

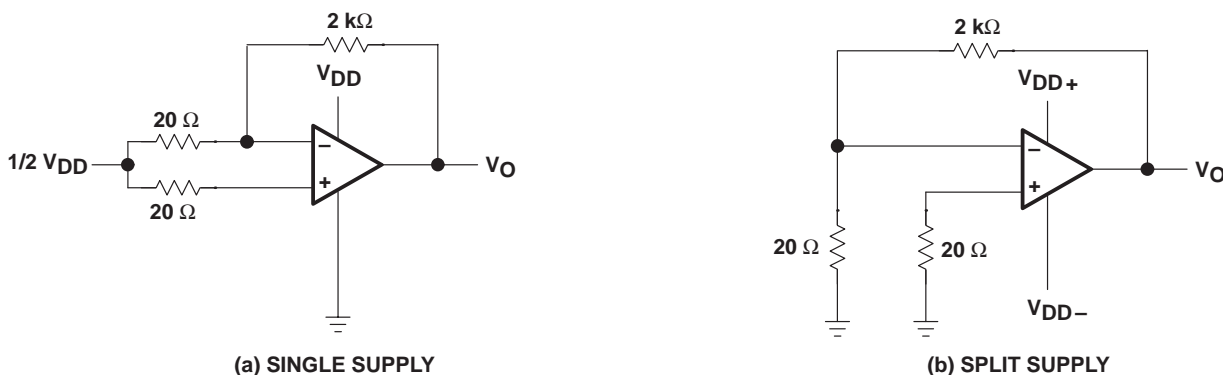


Figure 93. Noise-Test Circuits

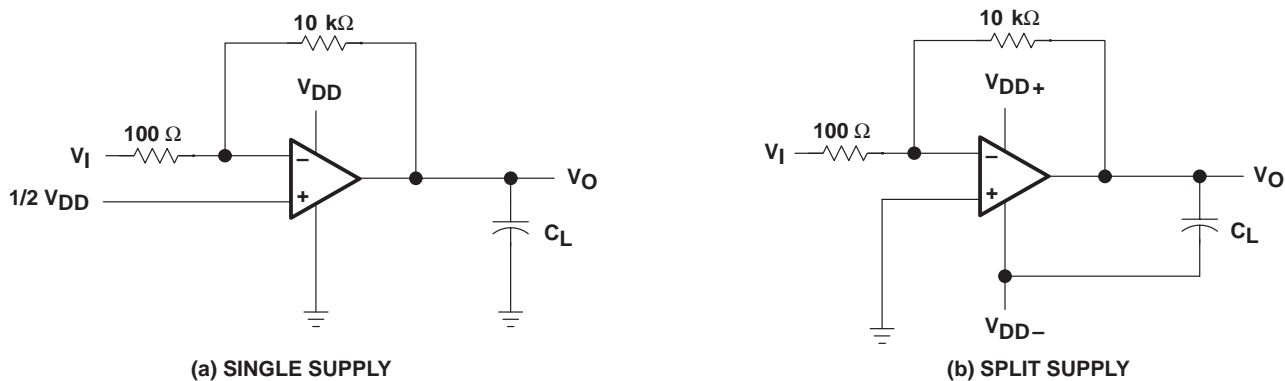


Figure 94. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2341 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 95). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

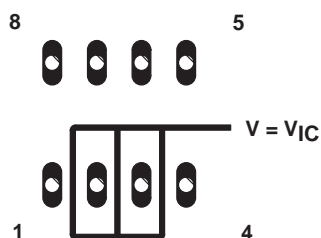


Figure 95. Isolation Metal Around Device Inputs (P package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 92. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 96). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

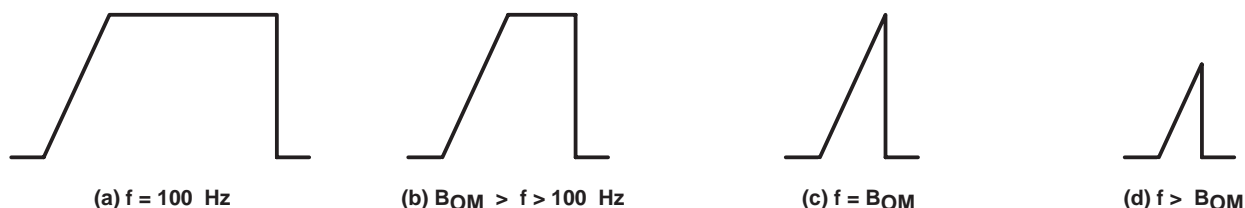


Figure 96. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2341 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

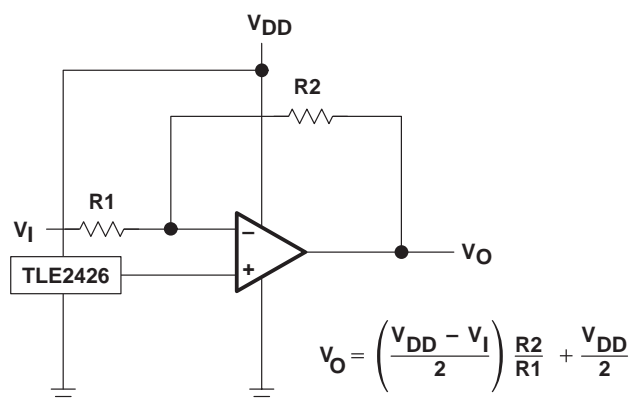


Figure 97. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2341 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 98); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

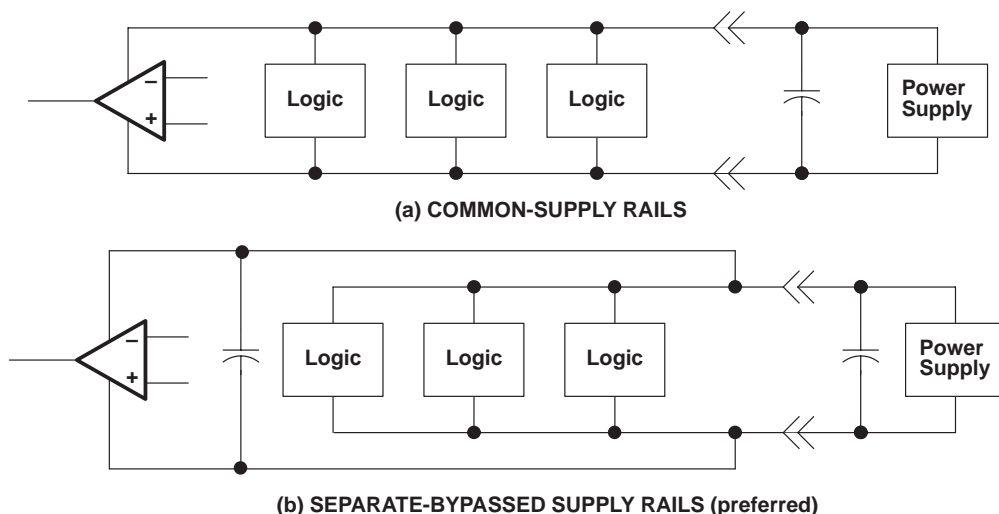


Figure 98. Common Versus Separate Supply Rails

input offset voltage nulling

The TLV2341 offers external input offset null control. Nulling of the input offset voltage can be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 99. The amount of nulling range varies with the bias selection. In the high-bias mode, the nulling range allows the maximum offset voltage specified to be trimmed to zero. In low-bias and medium-bias modes, total nulling may not be possible.

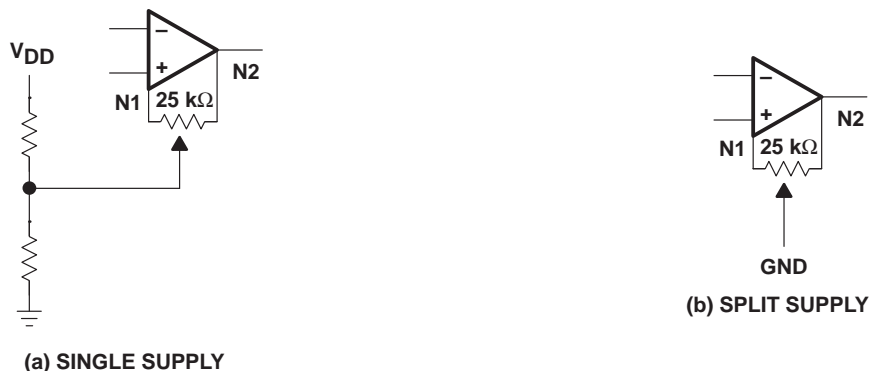


Figure 99. Input Offset Voltage Null Circuit

APPLICATION INFORMATION

bias selection

Bias selection is achieved by connecting the bias-select pin to one of the three voltage levels (see Figure 100). For medium-bias applications, it is recommended that the bias-select pin be connected to the midpoint between the supply rails. This is a simple procedure in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode necessitates using a voltage divider as indicated. The use of large-value resistors in the voltage divider reduces the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint may be used if it is within the voltages specified in the following table.

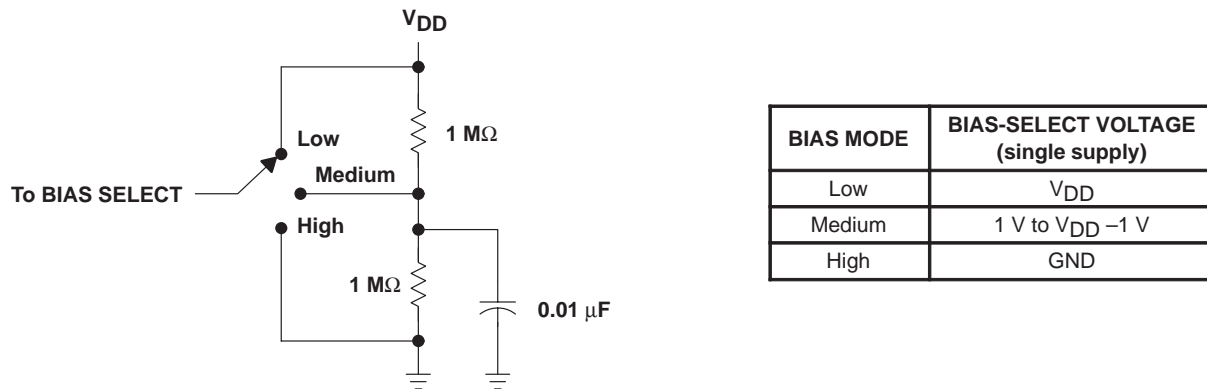


Figure 100. Bias Selection for Single-Supply Applications

input characteristics

The TLV2341 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25^\circ\text{C}$ and at $V_{DD} - 1.2$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLV2341 good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 $\mu\text{V}/\text{month}$, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2341 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 95 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 101).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

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input characteristics (continued)

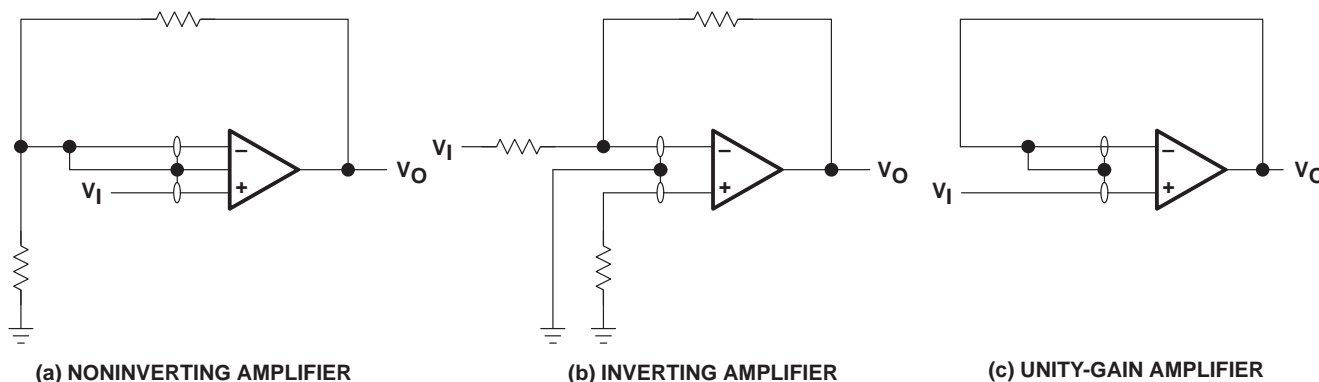


Figure 101. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifiers circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias-current requirements of the TLV2341 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 102). The value of this capacitor is optimized empirically.

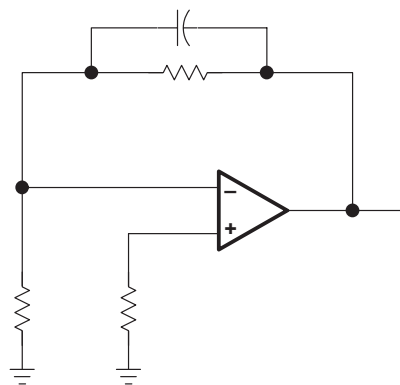


Figure 102. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2341 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2341 inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not be

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design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2341 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2341 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 103). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P , a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

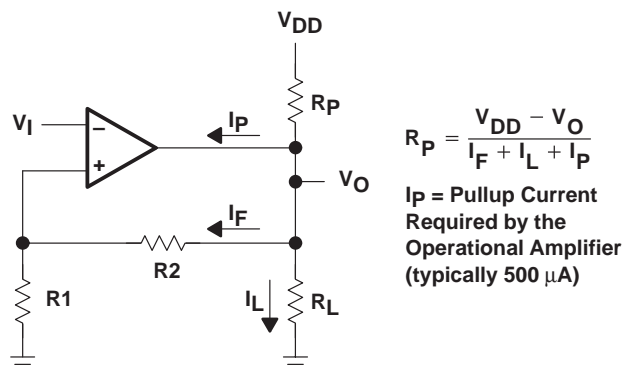


Figure 103. Resistive Pullup to Increase V_{OH}

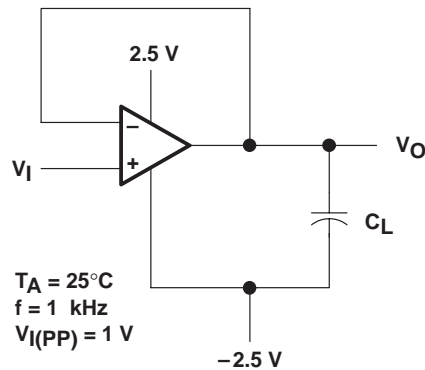


Figure 104. Test Circuit for Output Characteristics

All operating characteristics of the TLV2341 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figures 105, 106 and 107). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

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output characteristics (continued)

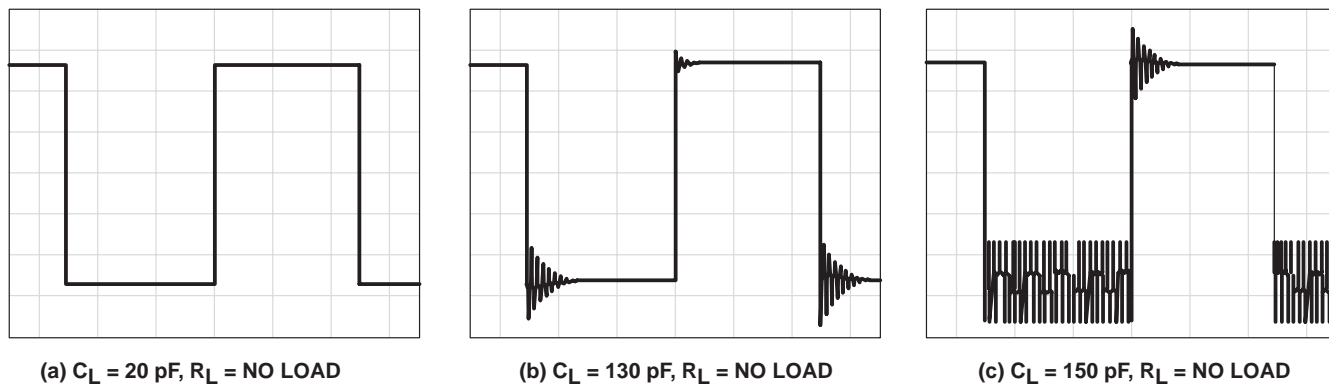


Figure 105. Effect of Capacitive Loads in High-Bias Mode

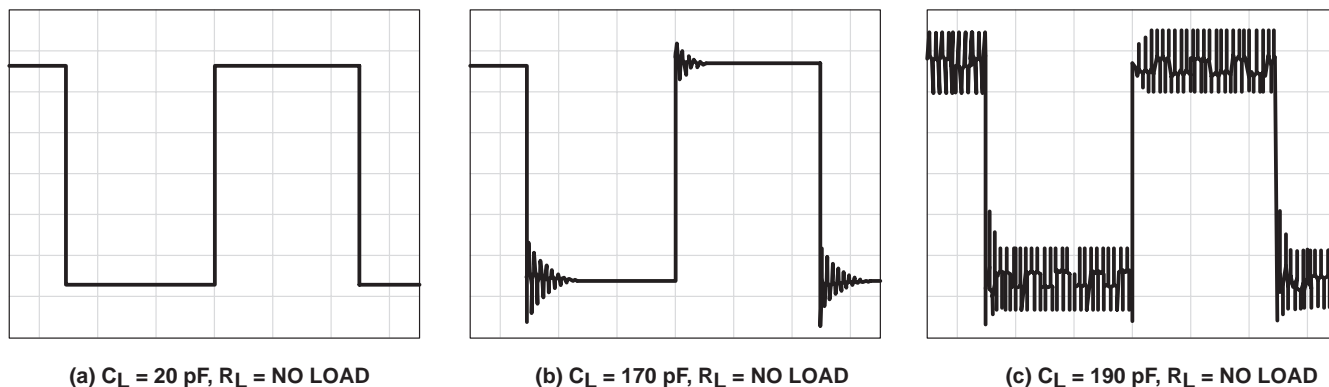


Figure 106. Effect of Capacitive Loads in Medium-Bias Mode

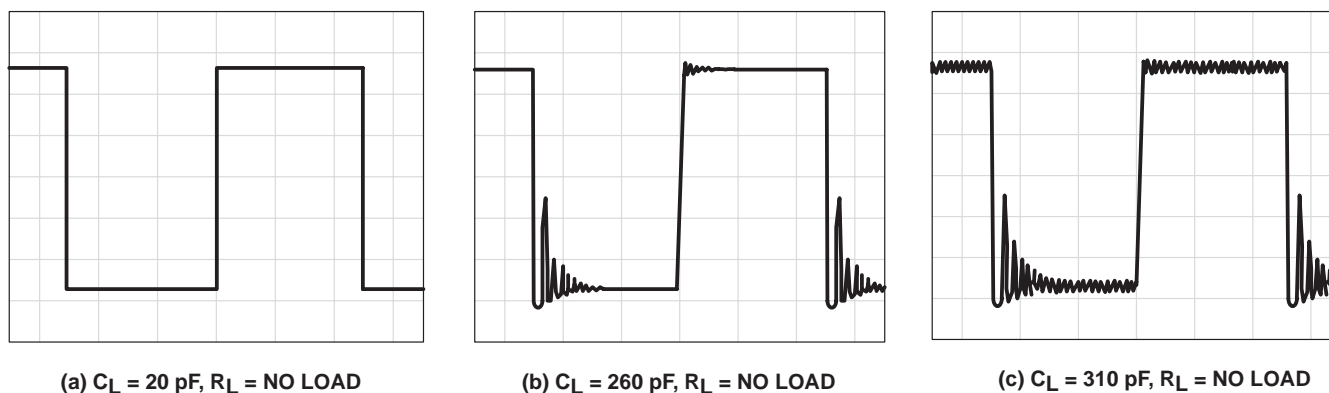


Figure 107. Effect of Capacitive Loads in Low-Bias Mode

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2341ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2341I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV2341ID	D	SOIC	8	75	507	8	3940	4.32
TLV2341ID	D	SOIC	8	75	505.46	6.76	3810	4

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