# Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT WIDE-INPUT-VOLTAGE OPERATIONAL AMPLIFIERS

## FEATURES

- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Output Swing Includes Both Supply Rails**
- **Extended Common-Mode Input Voltage Range: 0 V to 4.25 V (Min) at 5-V Single Supply**
- **No Phase Inversion**
- **Low Noise: 16 nV/$\sqrt{\text{Hz}}$ Typ at f = 1 kHz**
- **Low Input Offset Voltage: 950 μV Max at $T_A$ = 25°C (TLV244xA)**
- **Low Input Bias Current: 1 pA (Typ)**
- **600-Ω Output Drive**
- **High-Gain Bandwidth: 1.8 MHz (Typ)**
- **Low Supply Current: 750 μA Per Channel (Typ)**
- **Macromodel Included**

## DESCRIPTION

The TLV244x and TLV244xA are low-voltage operational amplifiers from Texas Instruments. The common-mode input voltage range of these devices has been extended over typical standard CMOS amplifiers, making them suitable for a wide range of applications. In addition, these devices do not phase invert when the common-mode input is driven to the supply rails. This satisfies most design requirements without paying a premium for rail-to-rail input performance. They also exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. This family is fully characterized at 3-V and 5-V supplies and is optimized for low-voltage operation. Both devices offer comparable ac performance while having lower noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLV244x has increased output drive over previous rail-to-rail operational amplifiers and can drive 600-Ω loads for telecommunications applications.

The other members in the TLV244x family are the low-power, TLV243x, and micro-power, TLV2422, versions.

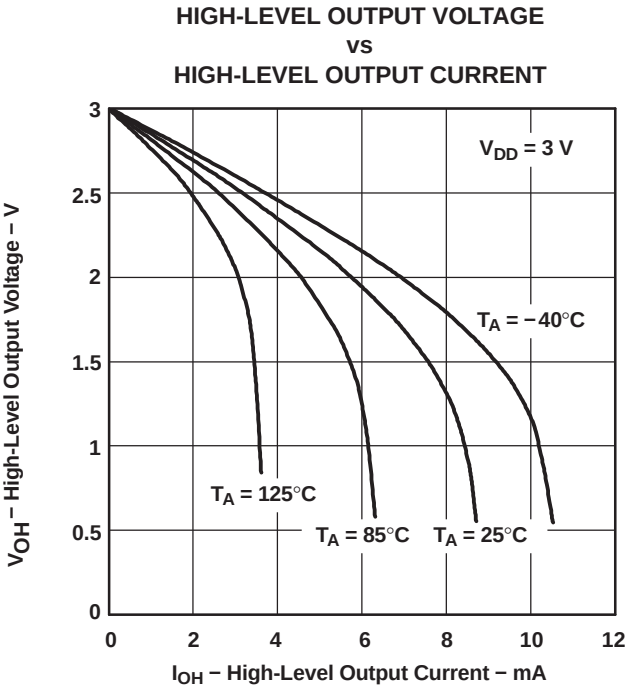



**Figure 1.**

The TLV244x, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels and low-voltage operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV244xA is available with a maximum input offset voltage of 950 μV.

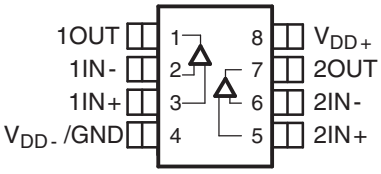
If the design requires single operational amplifiers, see the TI TLV2211/21/31. This is a family of rail-to-rail output operational amplifiers in the SOT-23 package. Their small size and low power consumption make them ideal for high-density battery-powered equipment.

## ORDERING INFORMATION(1)

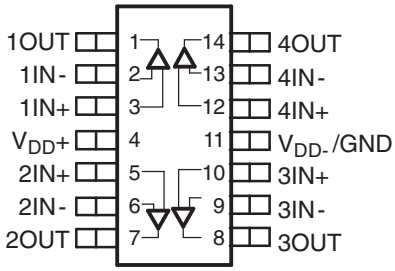
| $T_A$ | $V_{IO}$max AT 25 = C | PACKAGE(2) | | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|---|---|
| –40°C to 125°C | 950 µV | Dual | SOIC – D | Reel of 2500 | TLV2442AQDRQ1 | 2442AQ |
| | | | TSSOP – PW | Reel of 2000 | TLV2442AQPWRQ1 | 2442AQ |
| | 2.5 mV | Dual | MSOP – DGK | Reel of 2500 | TLV2442QDGKRQ1 | OBR |
| | | | SOIC – D | Reel of 2500 | TLV2442QDRQ1 | 2442Q1 |
| | | | TSSOP – PW | Reel of 2000 | TLV2442QPWRQ1 | 2442Q1 |
| | 950 µV | Quad | TSSOP – PW | Reel of 2000 | TLV2444AQPWRQ1 | 2444AQ |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

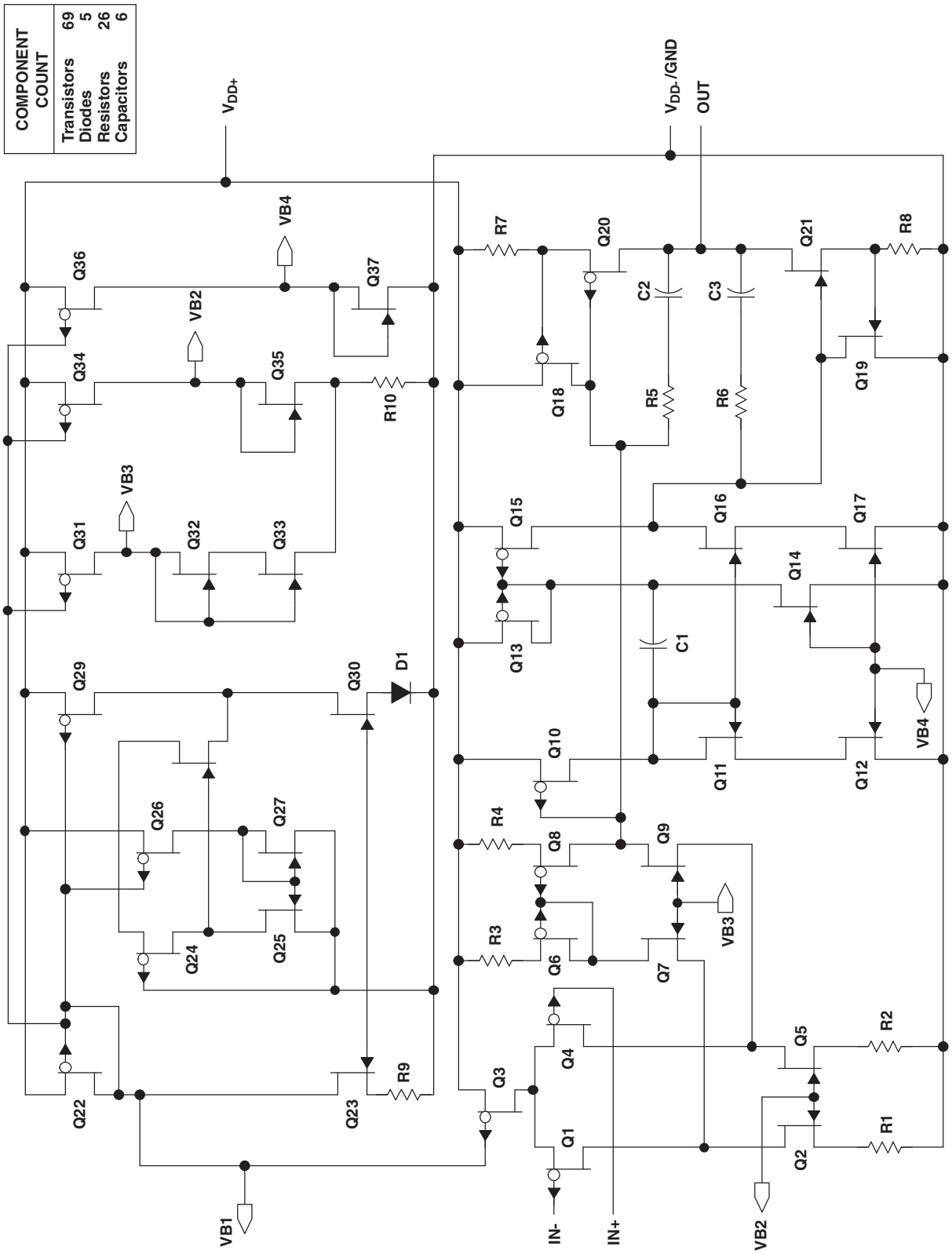
**TLV2442**
**D, DGK, OR PW PACKAGE**
**(TOP VIEW)**




**TLV2444**
**PW PACKAGE**
**(TOP VIEW)**



## EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | |
|---|---|---|
| $V_{DD}$ | Supply voltage(2) | 12 V |
| $V_{ID}$ | Differential input voltage(3) | $\pm V_{DD}$ |
| $V_I$ | Input voltage (any input)(2) | –0.3 V to $V_{DD}$ |
| $I_I$ | Input current (any input) | ±5 mA |
| $I_O$ | Output current | ±50 mA |
| | Total current into $V_{DD+}$ | ±50 mA |
| | Total current out of $V_{DD-}$ | ±50 mA |
| | Duration of short-circuit current at (or below) 25 = C(4) | Unlimited |
| | Continuous total dissipation | See Dissipation Rating Table |
| $T_A$ | Operating free-air temperature range | –40°C to 125°C |
| $T_{stg}$ | Storage temperature range | –65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between $V_{DD+}$ and $V_{DD-}$.
(3) Differential voltages are at IN+ with respect to IN–. Excessive current will flow if input is brought below $V_{DD-}$ – 0.3 V.
(4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

## DISSIPATION RATINGS

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|---|
| D (8 pin) | 725 mW | 5.8 mW/°C | 464 mW | 377 mW | 145 mW |
| DGK (8 pin) | 606 mW | 4.847 mW/°C | 388 mW | 315 mW | 121 mW |
| PW (8 pin) | 525 mW | 4.2 mW/°C | 336 mW | 273 mW | 105 mW |
| PW (14 pin) | 720 mW | 5.6 mW/°C | 634 mW | 547 mW | 317 mW |

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.7 | 10 | V |
| $V_I$ | Input voltage | $V_{DD-}$ | $V_{DD+} - 1$ | V |
| $V_{IC}$ | Common-mode input voltage | $V_{DD-}$ | $V_{DD+} - 1$ | V |
| $T_A$ | Operating free-air temperature | –40 | 125 | °C |

## ELECTRICAL CHARACTERISTICS

$V_{DD}$ = 3 V, at specified free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{IC}$ = 1.5 V, $V_O$ = 1.5 V, $R_S$ = 50 Ω | TLV244x | 25°C | | 300 | 2000 | µV |
| | | | | Full range | | | 2500 | |
| | | | TLV244xA | 25°C | | 300 | 950 | |
| | | | | Full range | | | 1600 | |
| $\alpha_{VIO}$ | Temperature coefficient of input offset voltage | $V_{IC}$ = 1.5 V, $V_O$ = 1.5 V, $R_S$ = 50 Ω | | 25°C to 85°C | | 2 | | µV/°C |
| | Input offset voltage long-term drift (2) | $V_{IC}$ = 1.5 V, $V_O$ = 1.5 V, $R_S$ = 50 Ω | | 25°C | | 0.002 | | µV/mo |
| $I_{IO}$ | Input offset current | $V_{IC}$ = 1.5 V, $V_O$ = 1.5 V, $R_S$ = 50 Ω | | 25°C | | 0.5 | | pA |
| | | | | Full range | | | 150 | |
| $I_{IB}$ | Input bias current | $V_{IC}$ = 1.5 V, $V_O$ = 1.5 V, $R_S$ = 50 Ω | | 25°C | | 1 | | pA |
| | | | | Full range | | | 260 | |
| $V_{ICR}$ | Common-mode input voltage range | $\|V_{IO}\|$ ≤ 8 mV, $R_S$ = 50 Ω | | 25°C | 0 to 2.25 | –0.25 to 2.5 | | V |
| | | | | Full range | 0.2 to 2 | | | |
| $V_{OH}$ | High-level output voltage | $I_O$ = –100 µA | | 25°C | | 2.98 | | V |
| | | $I_O$ = –3 mA | | 25°C | | 2.5 | | |
| | | | | Full range | 2.25 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{IC}$ = 1.5 V | $I_O$ = 100 µA | 25°C | | 0.02 | | V |
| | | | $I_O$ = 3 mA | 25°C | | 0.63 | | |
| | | | | Full range | | | 1 | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_O$ = 1 V to 2 V | $R_L$ = 600 Ω | 25°C | 0.7 | 1 | | V/mV |
| | | | | Full range | 0.4 | | | |
| | | | $R_L$ = 1 MΩ | 25°C | | 750 | | |
| $r_{id}$ | Differential input resistance | | | 25°C | | 1000 | | GΩ |
| $r_i$ | Common-mode input resistance | | | 25°C | | 1000 | | GΩ |
| $c_i$ | Common-mode input capacitance | f = 10 kHz | | 25°C | | 8 | | pF |
| $z_o$ | Closed-loop output impedance | f = 1 MHz, $A_V$ = 10 | | 25°C | | 130 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = $V_{ICR}$ MIN, $V_O$ = $V_{DD}$/2, $R_S$ = 50 Ω | | 25°C | 65 | 75 | | dB |
| | | | | Full range | 50 | | | |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$) | $V_{DD}$ = 2.7 V to 8 V, $V_{IC}$ = $V_{DD}$/2, No load | | 25°C | 80 | 95 | | dB |
| | | | | Full range | 80 | | | |
| $I_{DD}$ | Supply current (per channel) | $V_O$ = 1.5 V, No load | | 25°C | | 725 | 1100 | µA |
| | | | | Full range | | | 1100 | |

(1) Full range is –40°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A$ = 150°C extrapolated to $T_A$ = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

## OPERATING CHARACTERISTICS

$V_{DD}$ = 3 V, at specified free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SR | Slew rate at unity gain | $V_O$ = 1 V to 2 V, $R_L$ = 600 Ω, $C_L$ = 100 pF | | 25°C | 0.65 | 1.3 | | V/μs |
| | | | | Full range | 0.4 | | | |
| $V_n$ | Equivalent input noise voltage | f = 10 Hz | | 25°C | | 170 | | nV/√Hz |
| | | f = 1 kHz | | | | 18 | | |
| $V_{n(PP)}$ | Peak-to-peak equivalent input noise voltage | f = 0.1 Hz to 1 Hz | | 25°C | | 2.6 | | μV |
| | | f = 0.1 Hz to 10 Hz | | | | 5.1 | | |
| $I_n$ | Equivalent input noise current | | | 25°C | | 0.6 | | fA/√Hz |
| THD+N | Total harmonic distortion plus noise | $V_O$ = 0.5 V to 2.5 V, $R_L$ = 600 Ω, f = 1 kHz | $A_V$ = 1 | 25°C | | 0.08 | | % |
| | | | $A_V$ = 10 | | | 0.3 | | |
| | | | $A_V$ = 100 | | | 2 | | |
| | Gain-bandwidth product | f = 10 kHz, $R_L$ = 600 Ω, $C_L$ = 100 pF | | 25°C | | 1.75 | | MHz |
| BOM | Maximum output-swing bandwidth | $V_{O(PP)}$ = 1 V, $R_L$ = 600 Ω, $A_V$ = 1, $C_L$ = 100 pF | | 25°C | | 0.9 | | MHz |
| $t_s$ | Settling time | $A_V$ = –1, Step = –2.3 V to 2.3 V, $R_L$ = 600 Ω, $C_L$ = 100 pF | To 0.1% | 25°C | | 1.5 | | μs |
| | | | To 0.01% | | | 3.2 | | |
| $\phi_m$ | Phase margin at unity gain | $R_L$ = 600 Ω, $C_L$ = 100 pF | | 25°C | | 65 | | ° |
| | Gain margin | $R_L$ = 600 Ω, $C_L$ = 100 pF | | 25°C | | 9 | | dB |

(1) Full range is –40°C to 125°C.

## ELECTRICAL CHARACTERISTICS

$V_{DD}$ = 5 V, at specified free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{DD\pm}$ = ±2.5 V, $V_{IC}$ = 0, $V_O$ = 0, $R_S$ = 50 Ω | TLV244x | 25°C | | 300 | 2000 | µV |
| | | | | Full range | | | 2500 | |
| | | | TLV244xA | 25°C | | 300 | 950 | |
| | | | | Full range | | | 1600 | |
| $\alpha_{VIO}$ | Temperature coefficient of input offset voltage | $V_{DD\pm}$ = ±2.5 V, $V_{IC}$ = 0, $V_O$ = 0, $R_S$ = 50 Ω | | 25°C to 85°C | | 2 | | µV/°C |
| | Input offset voltage long-term drift (2) | $V_{DD\pm}$ = ±2.5 V, $V_{IC}$ = 0, $V_O$ = 0, $R_S$ = 50 Ω | | 25°C | | 0.002 | | µV/mo |
| $I_{IO}$ | Input offset current | $V_{DD\pm}$ = ±2.5 V, $V_{IC}$ = 0, $V_O$ = 0, $R_S$ = 50 Ω | | 25°C | | 0.5 | | pA |
| | | | | Full range | | | 150 | |
| $I_{IB}$ | Input bias current | $V_{DD\pm}$ = ±2.5 V, $V_{IC}$ = 0, $V_O$ = 0, $R_S$ = 50 Ω | | 25°C | | 1 | | pA |
| | | | | Full range | | | 260 | |
| $V_{ICR}$ | Common-mode input voltage range | $\|V_{IO}\|$ ≤ 5 mV, $R_S$ = 50 Ω | | 25°C | 0 to 4.25 | –0.25 to 4.5 | | V |
| | | | | Full range | 0 to 4 | | | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –100 µA | | 25°C | | 4.97 | | V |
| | | $I_{OH}$ = –5 mA | | 25°C | 4 | 4.35 | | |
| | | | | Full range | 4 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{IC}$ = 2.5 V | $I_{OL}$ = 100 µA | 25°C | | 0.01 | | V |
| | | | $I_{OL}$ = 5 mA | 25°C | | 0.8 | | |
| | | | | Full range | | | 1.25 | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_{IC}$ = 2.5 V, $V_O$ = 1 V to 4 V | $R_L$ = 600 Ω (3) | 25°C | 0.9 | 1.3 | | V/mV |
| | | | | Full range | 0.5 | | | |
| | | | $R_L$ = 1 MΩ (3) | 25°C | | 950 | | |
| $r_{id}$ | Differential input resistance | | | 25°C | | 1000 | | GΩ |
| $r_i$ | Common-mode input resistance | | | 25°C | | 1000 | | GΩ |
| $c_i$ | Common-mode input capacitance | f = 10 kHz | | 25°C | | 8 | | pF |
| $z_o$ | Closed-loop output impedance | f = 1 MHz, $A_V$ = 10 | | 25°C | | 140 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = $V_{ICR}$ MIN, $V_O$ = $V_{DD}$/2, $R_S$ = 50 Ω | | 25°C | 70 | 75 | | dB |
| | | | | Full range | 70 | | | |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD}$ = 4.4 V to 8 V, $V_{IC}$ = $V_{DD}$/2, No load | | 25°C | 80 | 95 | | dB |
| | | | | Full range | 80 | | | |
| $I_{DD}$ | Supply current (per channel) | $V_O$ = 2.5 V, No load | | 25°C | | 750 | 1100 | µA |
| | | | | Full range | | | 1100 | |

(1) Full range is –40°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A$ = 150°C extrapolated to $T_A$ = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(3) Referenced to 2.5 V

## OPERATING CHARACTERISTICS

$V_{DD}$ = 5 V, at specified free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SR | Slew rate at unity gain | $V_O$ = 0.5 V to 2.5 V, $R_L$ = 600 Ω (2), $C_L$ = 100 pF (2) | | 25°C | 0.75 | 1.4 | | V/μs |
| | | | | Full range | 0.5 | | | |
| $V_n$ | Equivalent input noise voltage | f = 10 Hz | | 25°C | | 130 | | nV/√Hz |
| | | f = 1 kHz | | | | 16 | | |
| $V_{n(PP)}$ | Peak-to-peak equivalent input noise voltage | f = 0.1 Hz to 1 Hz | | 25°C | | 1.8 | | μV |
| | | f = 0.1 Hz to 10 Hz | | | | 3.6 | | |
| $I_n$ | Equivalent input noise current | | | 25°C | | 0.6 | | fA/√Hz |
| THD+N | Total harmonic distortion plus noise | $V_O$ = 1.5 V to 3.5V, f = 1 kHz, $R_L$ = 600 Ω (2) | $A_V$ = 1 | 25°C | | 0.017 | | % |
| | | | $A_V$ = 10 | | | 0.17 | | |
| | | | $A_V$ = 100 | | | 1.5 | | |
| | Gain-bandwidth product | f = 10 kHz, $R_L$ = 600 Ω (2), $C_L$ = 100 pF (2) | | 25°C | | 1.81 | | MHz |
| BOM | Maximum output-swing bandwidth | $V_{O(PP)}$ = 2 V, $A_V$ = 1, $R_L$ = 600 Ω (2), $C_L$ = 100 pF (2) | | 25°C | | 0.5 | | MHz |
| $t_s$ | Settling time | $A_V$ = –1, Step = –0.5 V to 2.5 V, $R_L$ = 600 Ω (2), $C_L$ = 100 pF (2) | To 0.1% | 25°C | | 1.5 | | μs |
| | | | To 0.01% | | | 2.6 | | |
| $\phi_m$ | Phase margin at unity gain | $R_L$ = 600 Ω (2), $C_L$ = 100 pF (2) | | 25°C | | 68 | | ° |
| | Gain margin | $R_L$ = 600 Ω (2), $C_L$ = 100 pF (2) | | 25°C | | 8 | | dB |

(1) Full range is –40°C to 125°C.
(2) Referenced to 2.5 V

## TYPICAL CHARACTERISTICS

### Table of Graphs(1)

| | | | FIGURE |
|---|---|---|---|
| $V_{IO}$ | Input offset voltage | Distribution | 2, 3 |
| | | vs Common-mode input voltage | 4, 5 |
| $\alpha_{VIO}$ | Input offset voltage temperature coefficient | Distribution | 6, 7 |
| $I_{IB}/I_{IO}$ | Input bias and input offset currents | vs Free-air temperature | 8 |
| $V_{OH}$ | High-level output voltage | vs High-level output current | 9, 10 |
| $V_{OL}$ | Low-level output voltage | vs Low-level output current | 11, 12 |
| $V_{O(PP)}$ | Maximum peak-to-peak output voltage | vs Frequency | 13 |
| $I_{OS}$ | Short-circuit output current | vs Supply voltage | 14 |
| | | vs Free-air temperature | 15 |
| $V_O$ | Output voltage | vs Differential input voltage | 16, 17 |
| $A_{VD}$ | Differential voltage amplification | vs Load resistance | 18 |
| | Large-signal differential voltage amplification and phase margin | vs Frequency | 19, 20 |
| | Large-signal differential voltage amplification | vs Free-air temperature | 21, 22 |
| $z_o$ | Output impedance | vs Frequency | 23, 24 |
| CMRR | Common-mode rejection ratio | vs Frequency | 25 |
| | | vs Free-air temperature | 26 |
| $k_{SVR}$ | Supply-voltage rejection ratio | vs Frequency | 27, 28 |
| | | vs Free-air temperature | 29 |
| $I_{DD}$ | Supply current | vs Supply voltage | 30 |
| SR | Slew rate | vs Load capacitance | 31 |
| | | vs Free-air temperature | 32 |
| $V_O$ | Inverting large-signal pulse response | | 33, 34 |
| | Voltage-follower large-signal pulse response | | 35, 36 |
| | Inverting small-signal pulse response | | 37, 38 |
| | Voltage-follower small-signal pulse response | | 39, 40 |
| $V_n$ | Equivalent input noise voltage | vs Frequency | 41, 42 |
| | Noise voltage | Over a 10-second period | 43 |
| THD + N | Total harmonic distortion plus noise | vs Frequency | 44, 45 |
| | Gain-bandwidth product | vs Free-air temperature | 46 |
| | | vs Supply voltage | 47 |
| $\phi_m$ | Phase margin | vs Frequency | 19, 20 |
| | | vs Load capacitance | 48 |
| | Gain margin | vs Load capacitance | 49 |
| $B_1$ | Unity-gain bandwidth | vs Load capacitance | 50 |

(1) For all graphs where $V_{DD}$ = 5 V, all loads are referenced to 2.5 V.

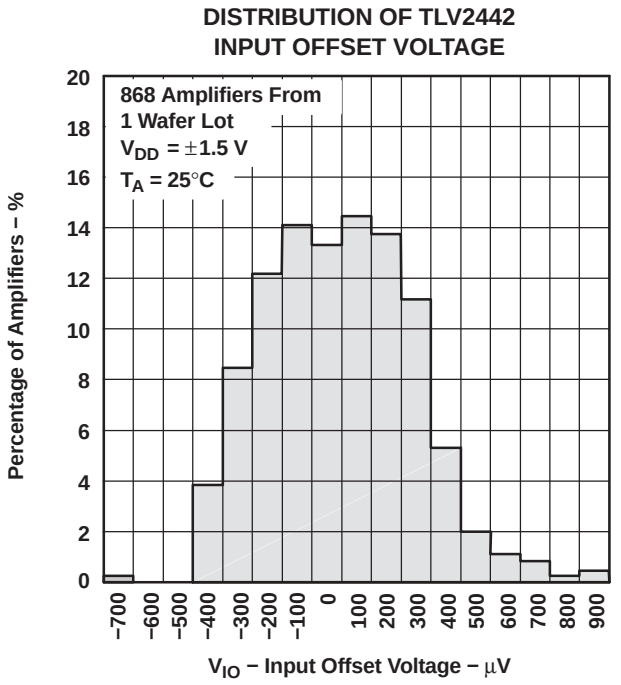



Figure 2.

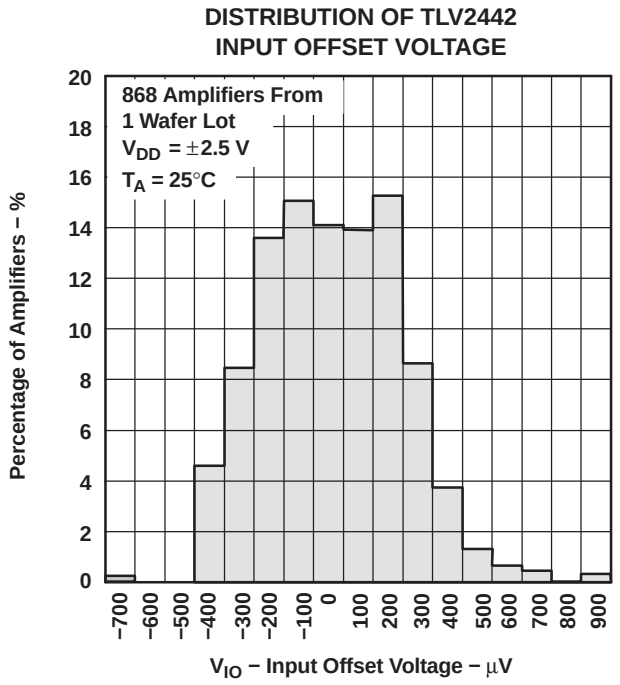



Figure 3.

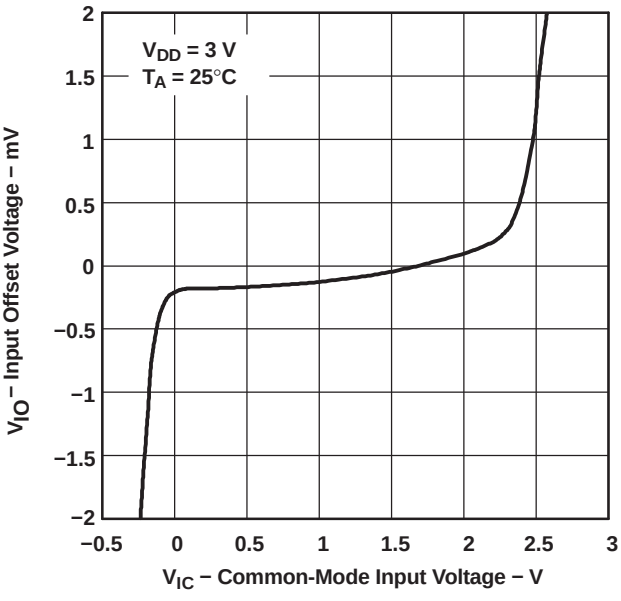



Figure 4.

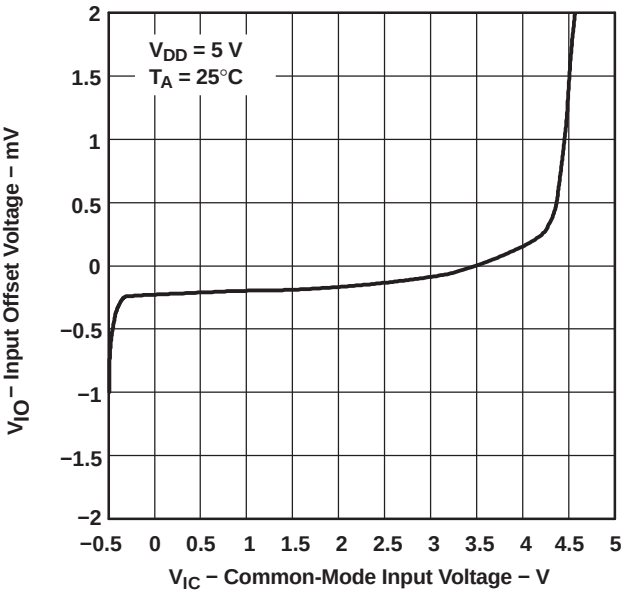



Figure 5.

DISTRIBUTION OF TLV2442 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

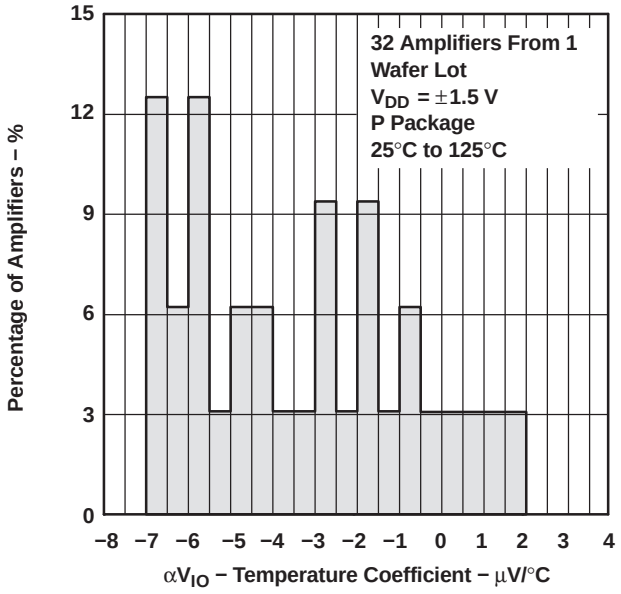



**Figure 6.**

DISTRIBUTION OF TLV2442 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

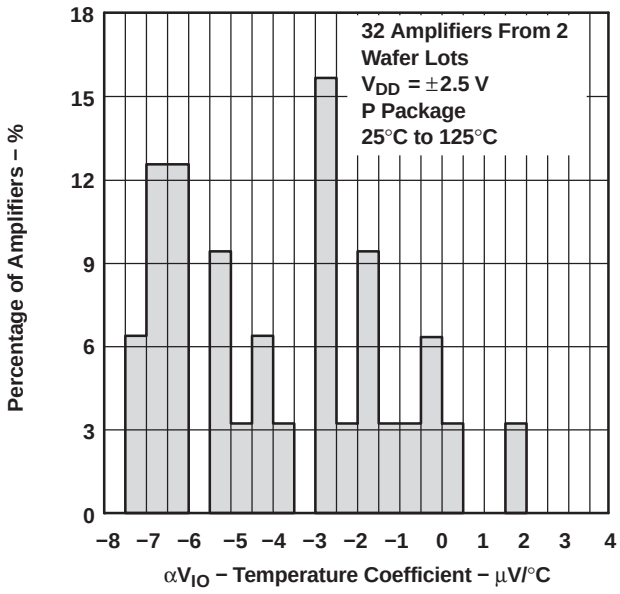



**Figure 7.**

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

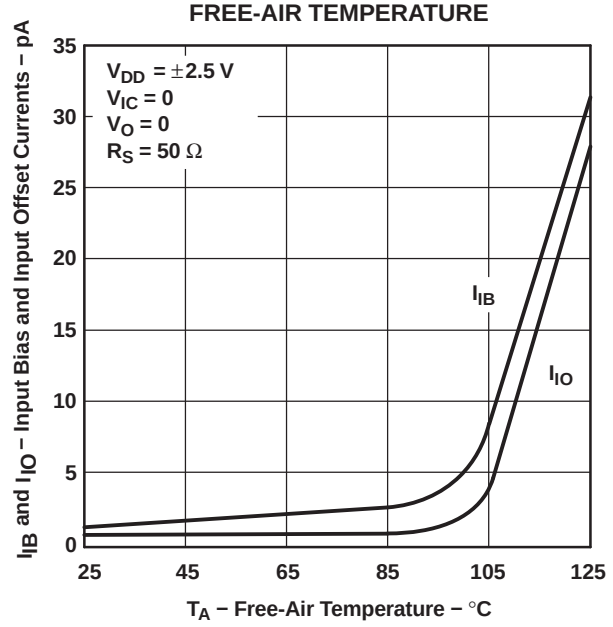



**Figure 8.**

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

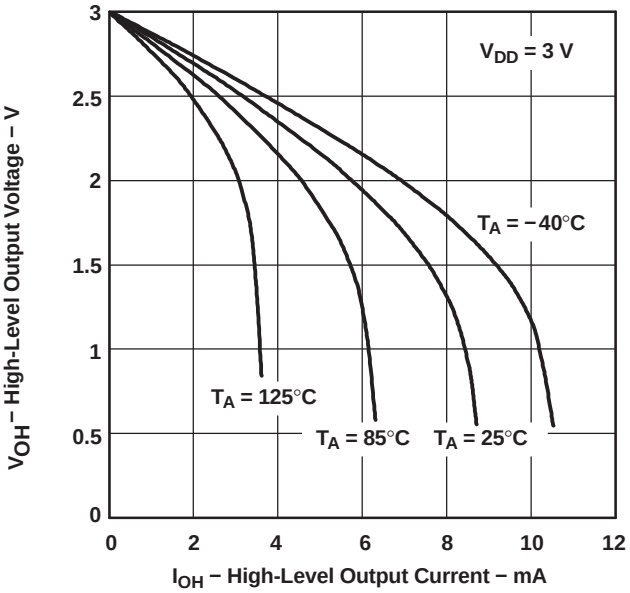



**Figure 9.**

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

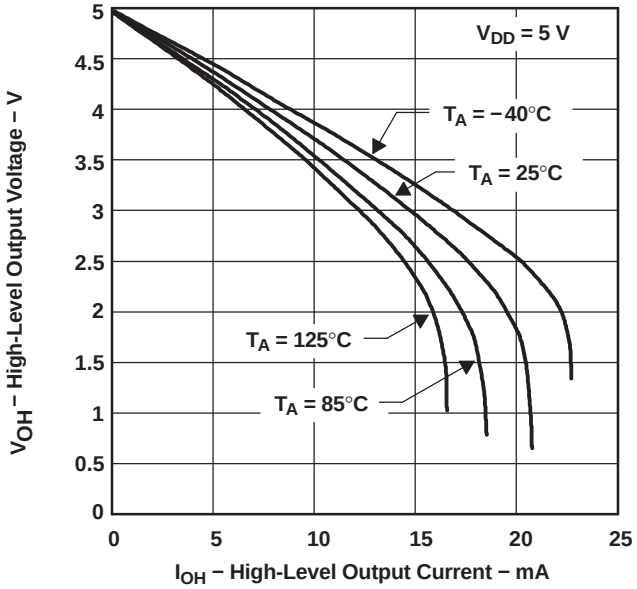



**Figure 10.**

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

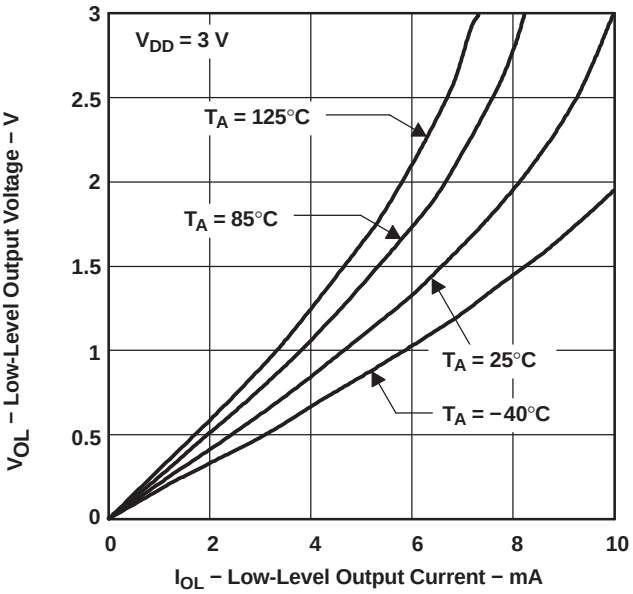



**Figure 11.**

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

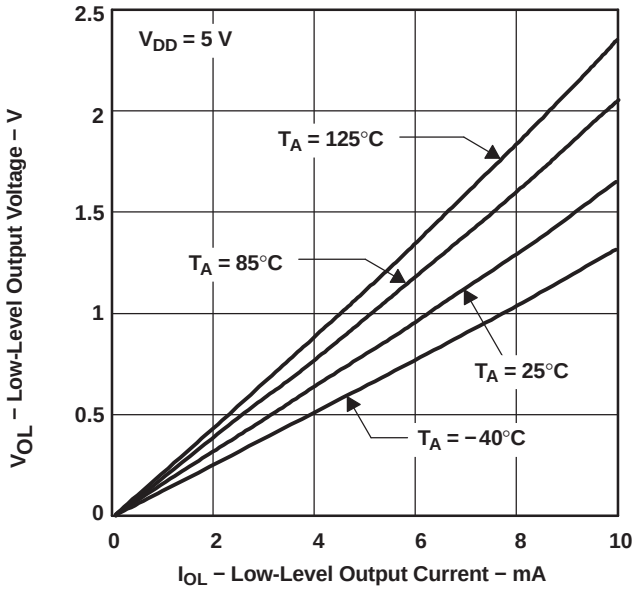



**Figure 12.**

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY**

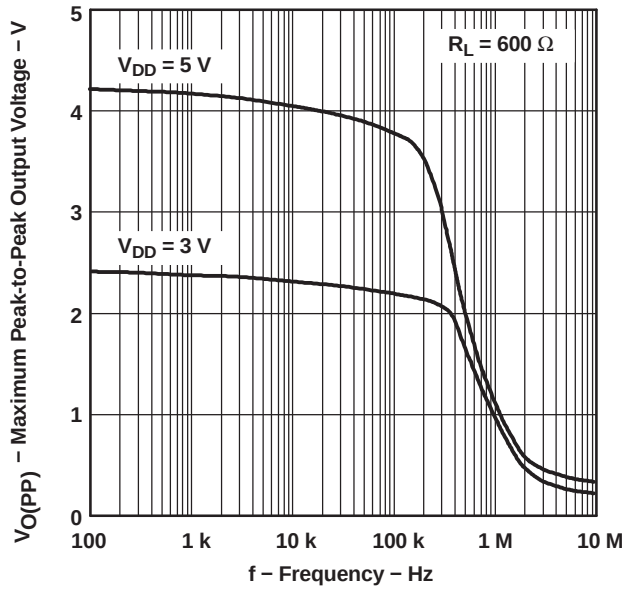



**Figure 13.**

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

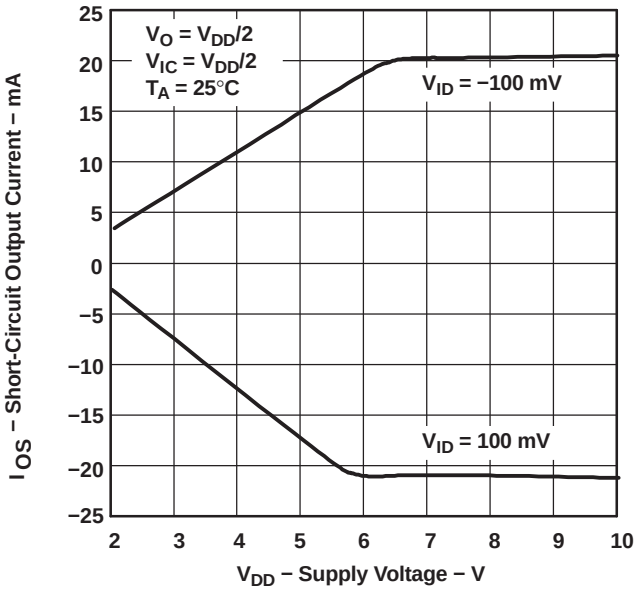



Figure 14.

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

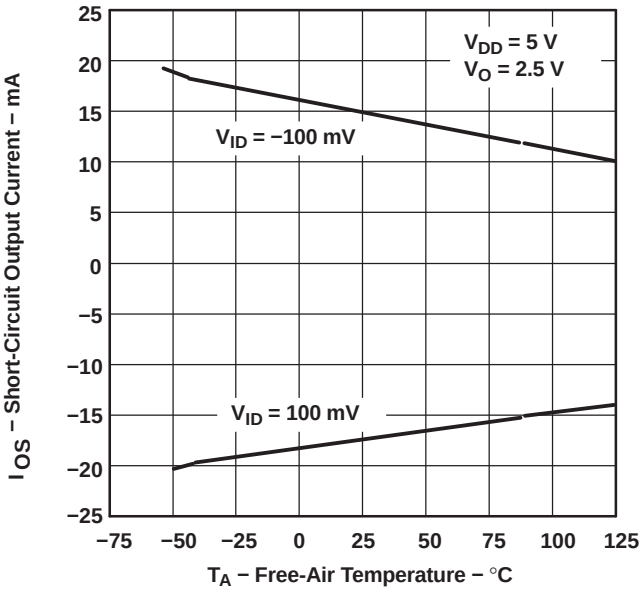



Figure 15.

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

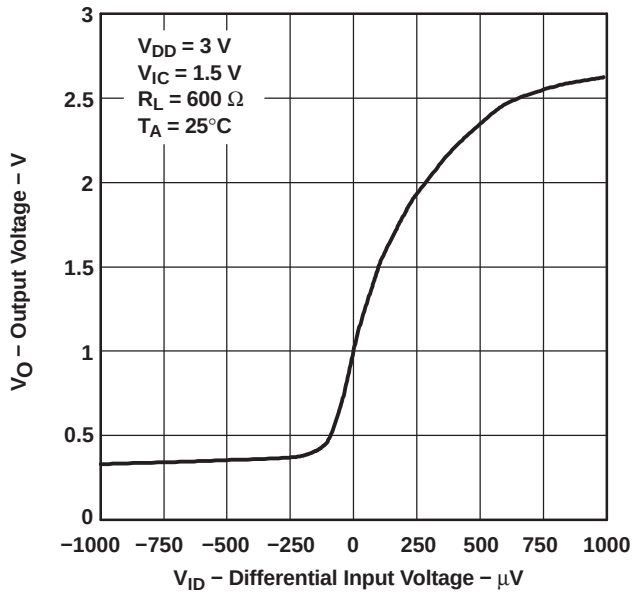



Figure 16.

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

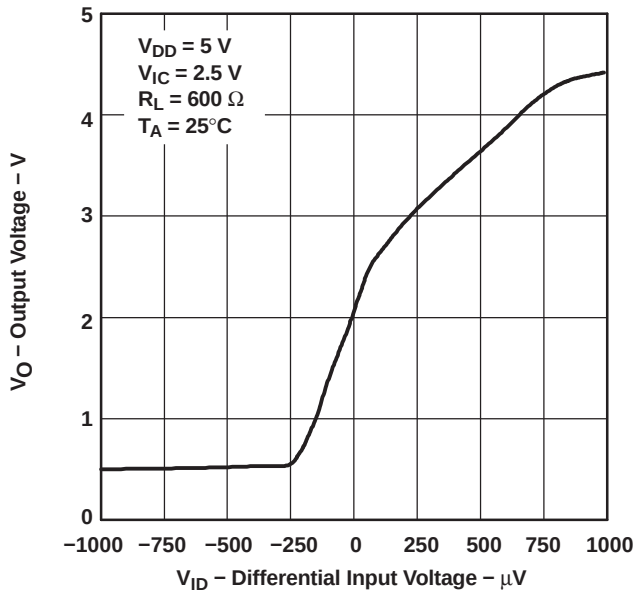



Figure 17.

**DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE**

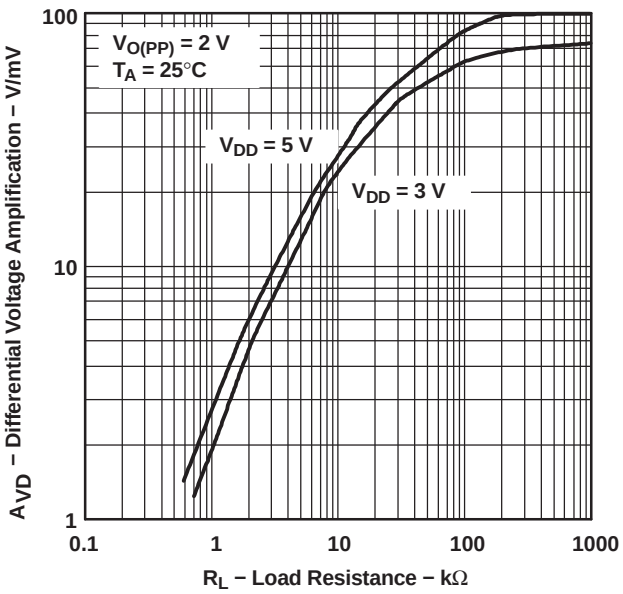



**Figure 18.**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY**

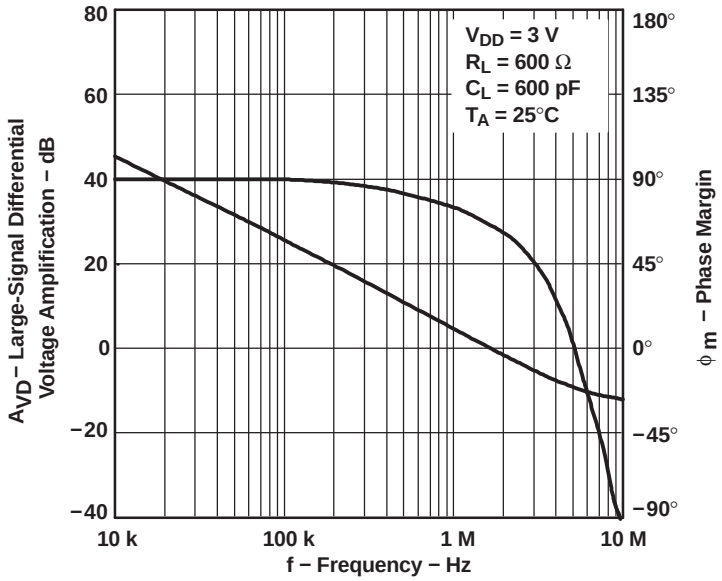



**Figure 19.**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY**

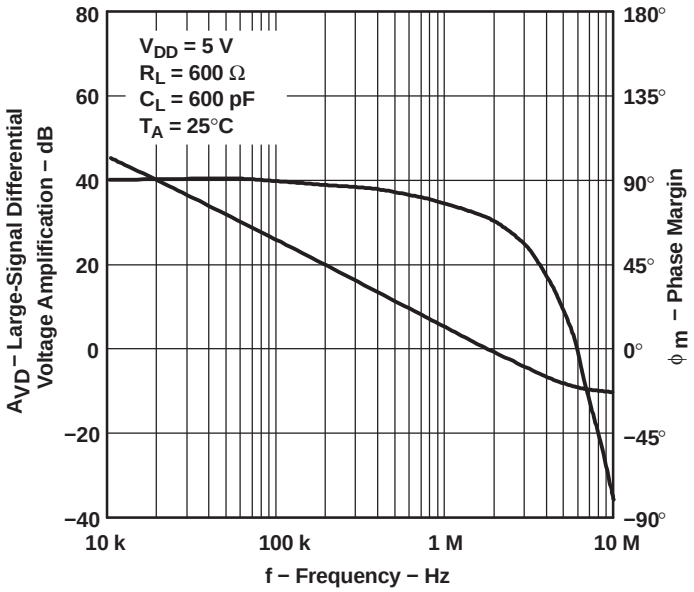



**Figure 20.**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE**

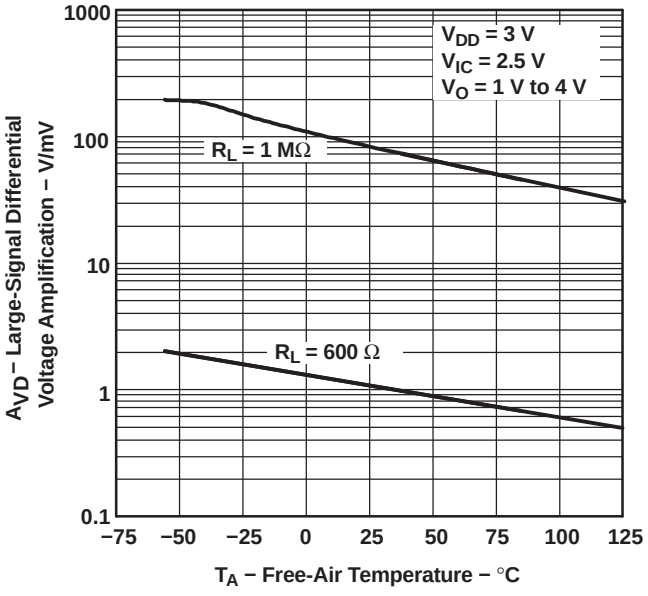



**Figure 21.**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE**

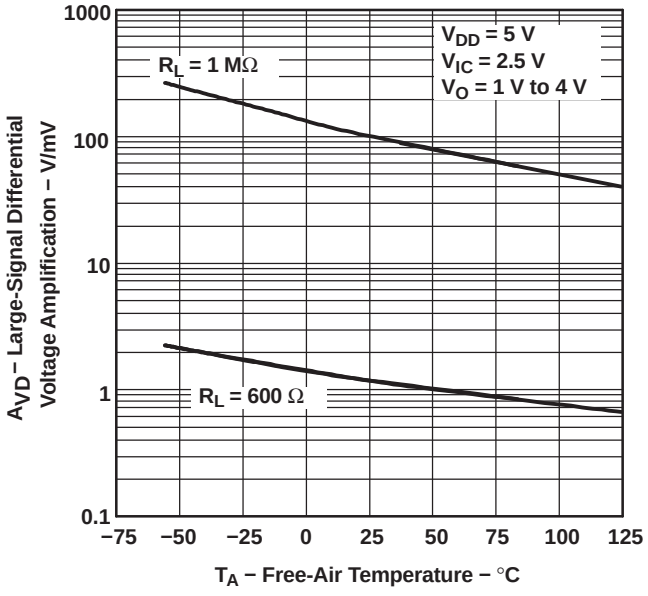



**Figure 22.**

OUTPUT IMPEDANCE
vs
FREQUENCY

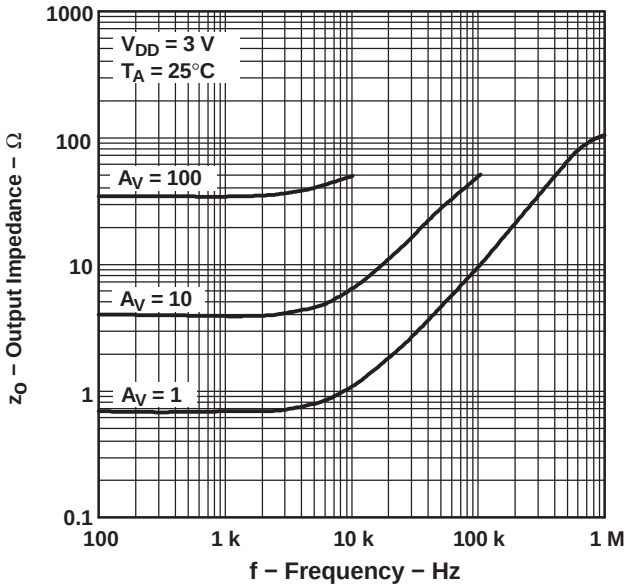



**Figure 23.**

OUTPUT IMPEDANCE
vs
FREQUENCY

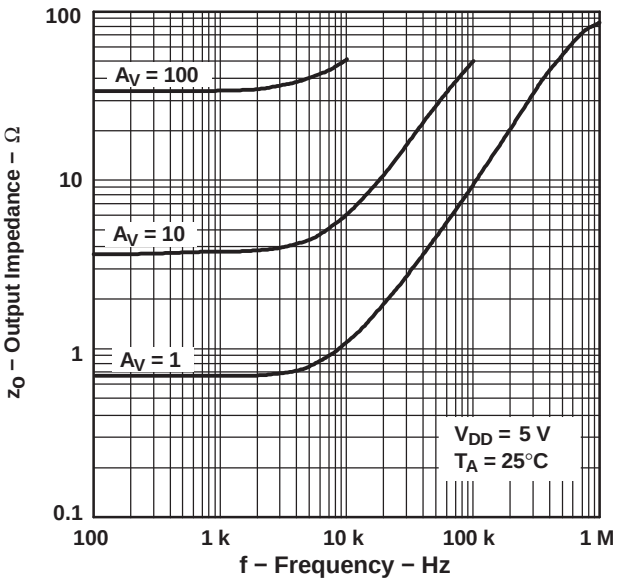



**Figure 24.**

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

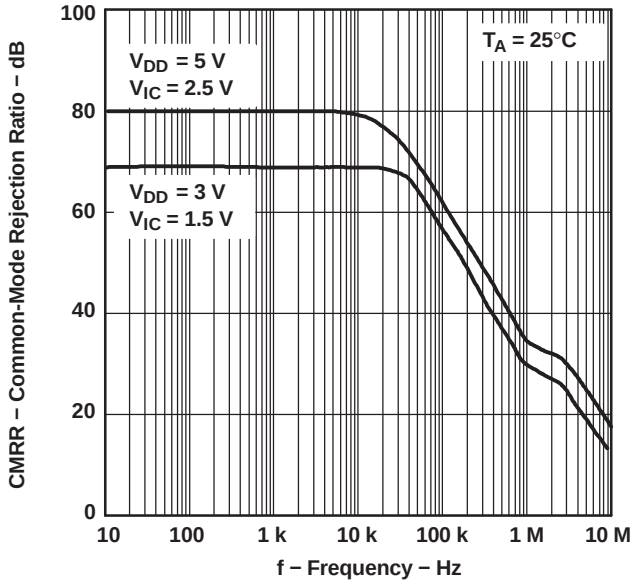



**Figure 25.**

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

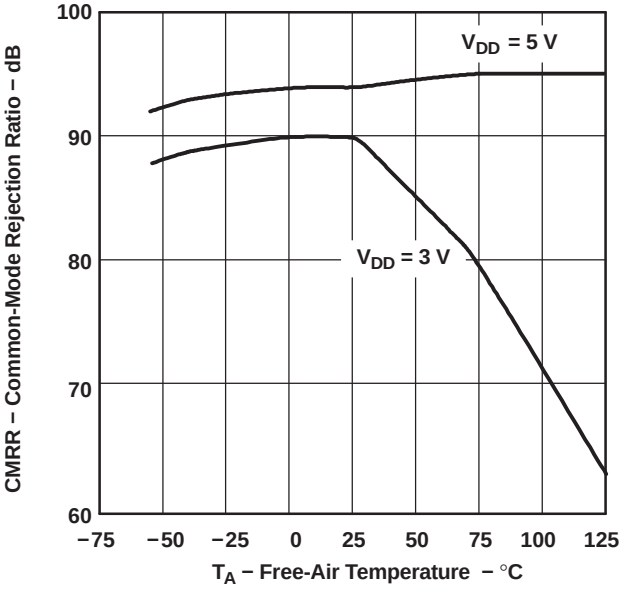



**Figure 26.**

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

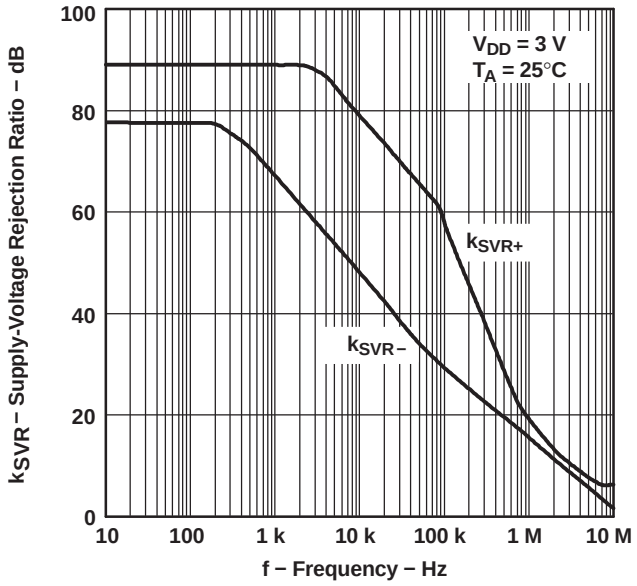



**Figure 27.**

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

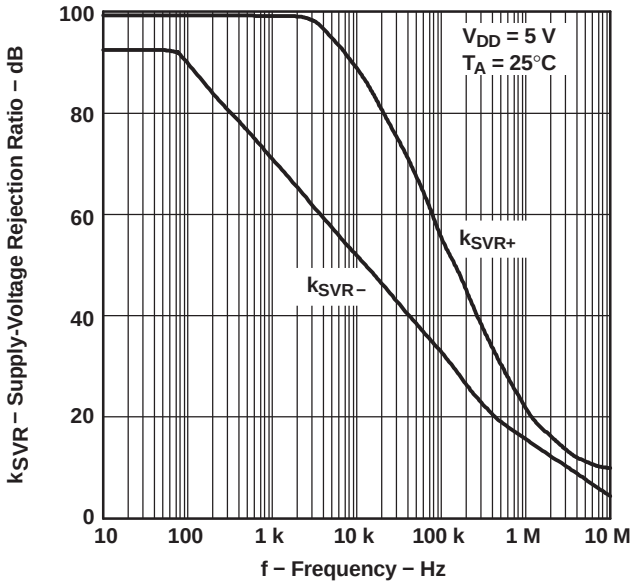



**Figure 28.**

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

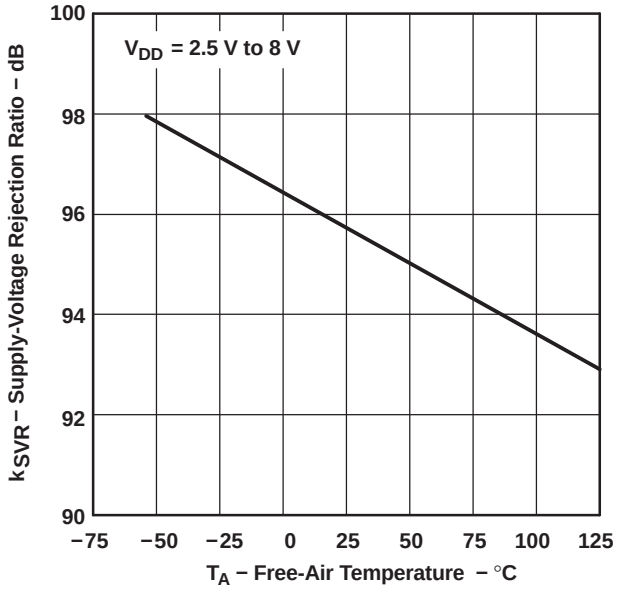



**Figure 29.**

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

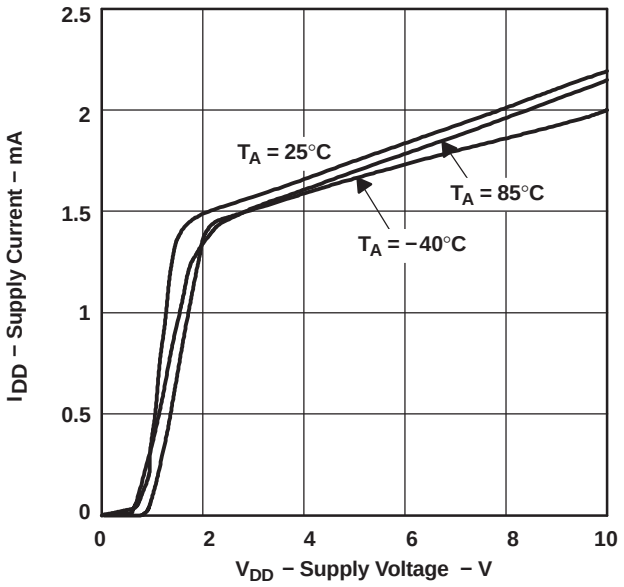



**Figure 30.**

SLEW RATE
vs
LOAD CAPACITANCE

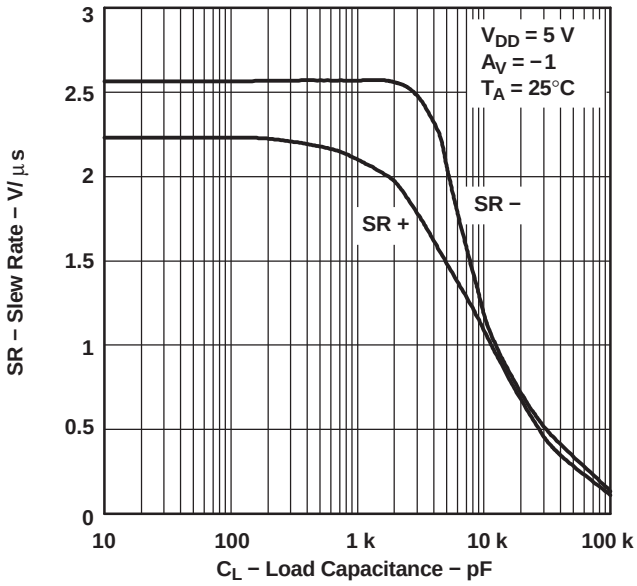



Figure 31.

SLEW RATE
vs
FREE-AIR TEMPERATURE

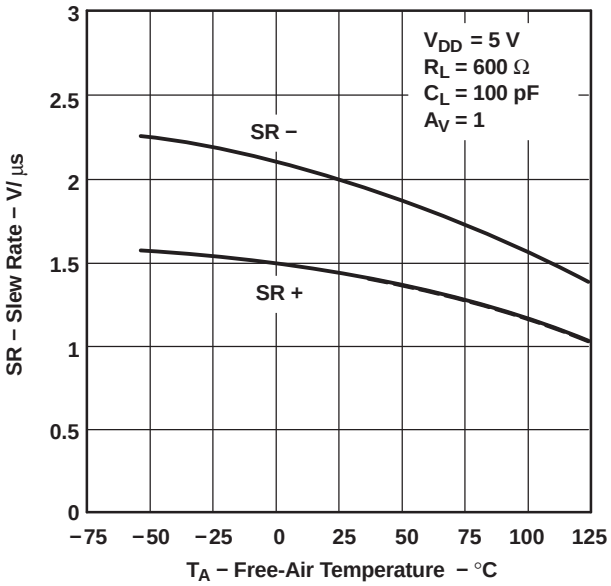



Figure 32.

INVERTING LARGE-SIGNAL PULSE RESPONSE

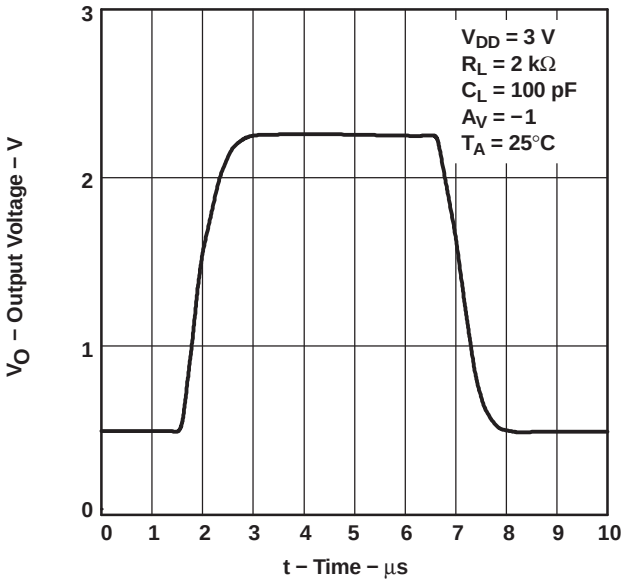



Figure 33.

INVERTING LARGE-SIGNAL PULSE RESPONSE

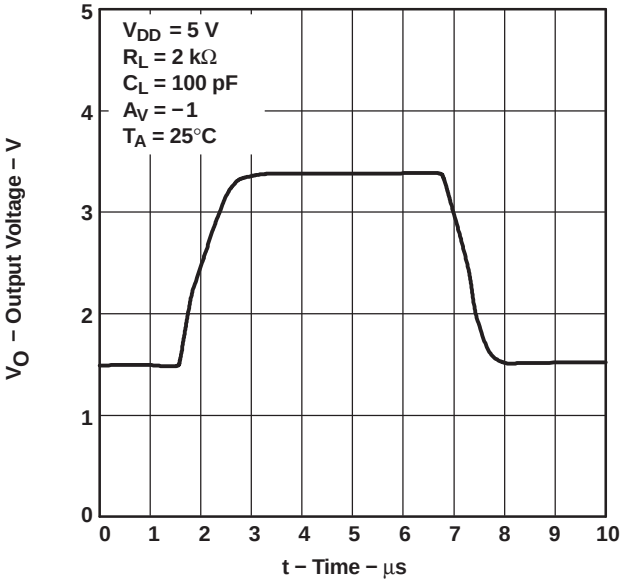



Figure 34.

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

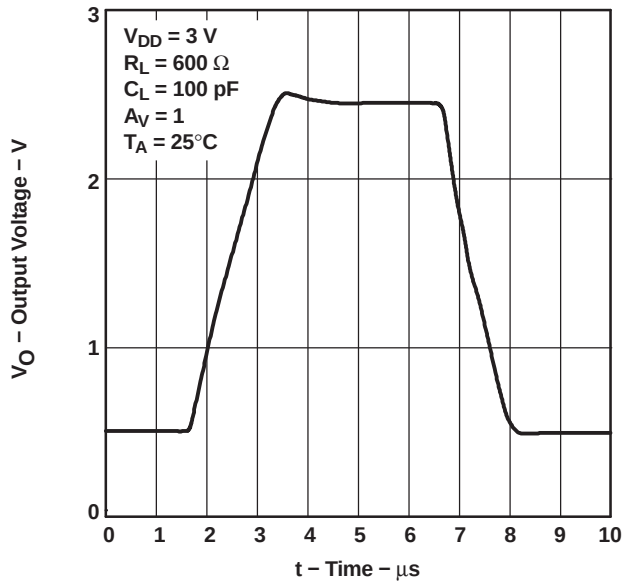



Figure 35.

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

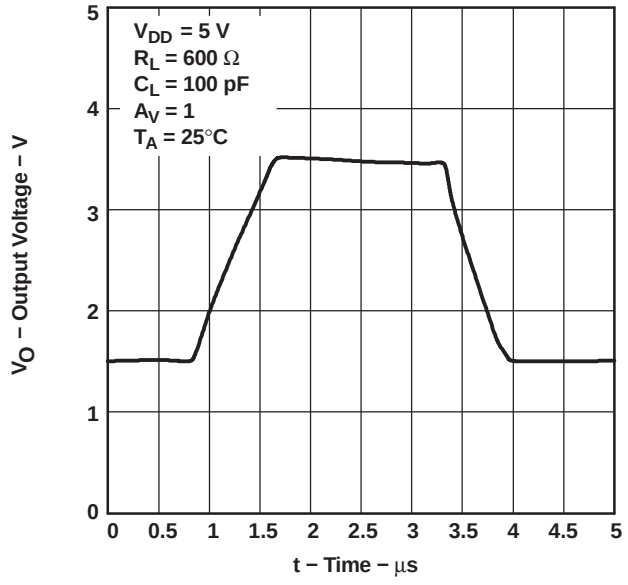



Figure 36.

INVERTING SMALL-SIGNAL PULSE RESPONSE

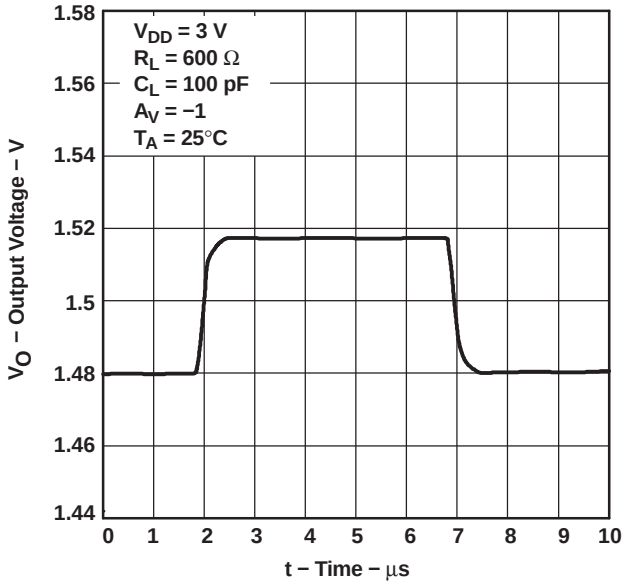



Figure 37.

INVERTING SMALL-SIGNAL PULSE RESPONSE

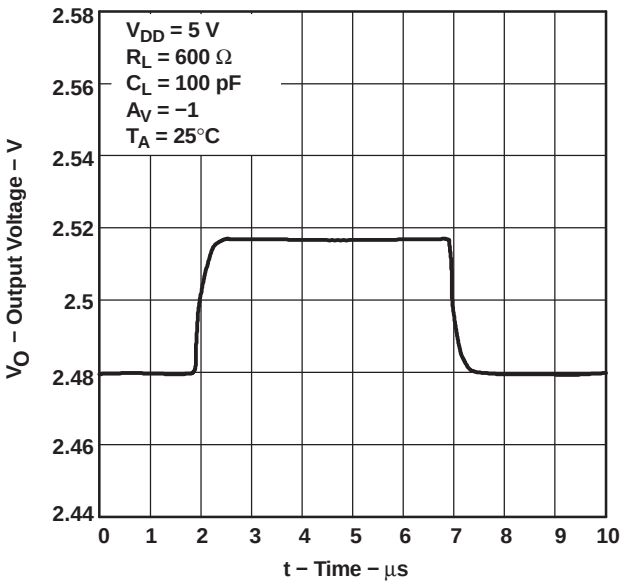



Figure 38.

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

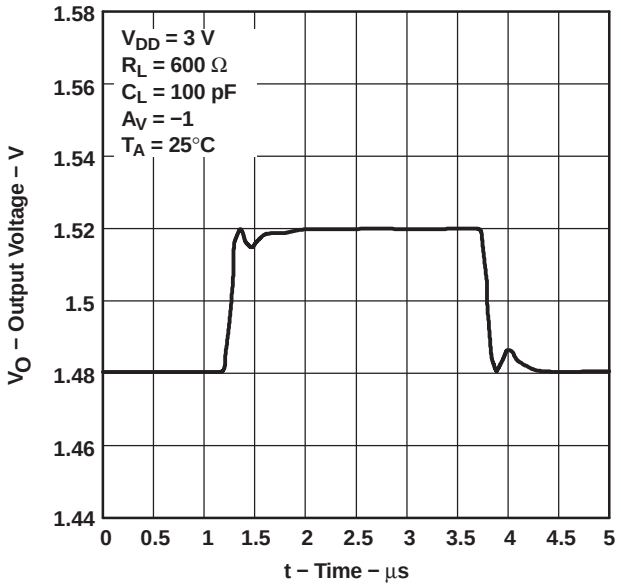



**Figure 39.**

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

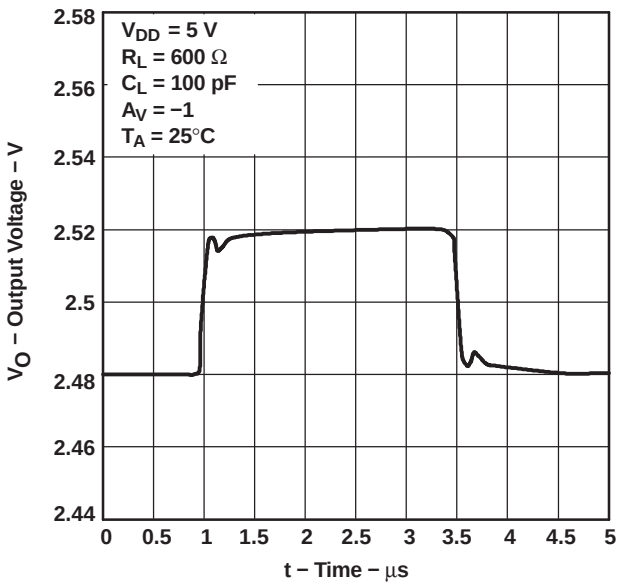



**Figure 40.**

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

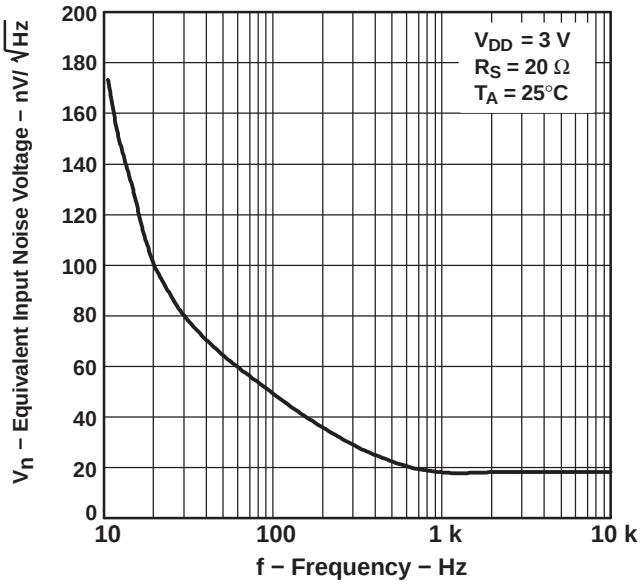



**Figure 41.**

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

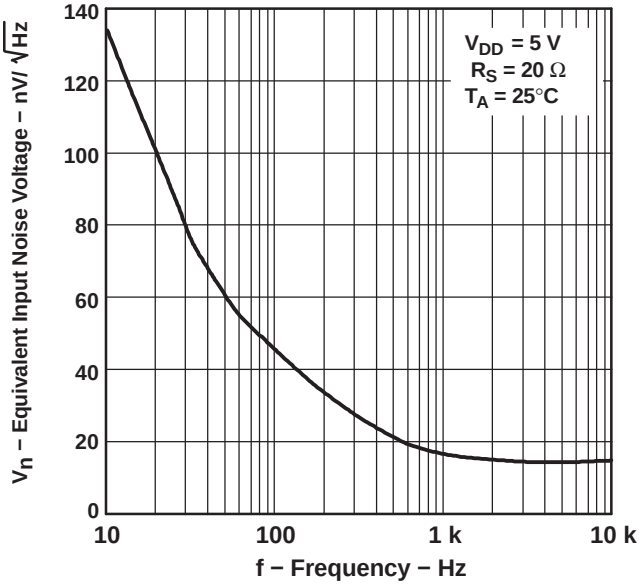



**Figure 42.**

NOISE VOLTAGE
OVER A 10-SECOND PERIOD

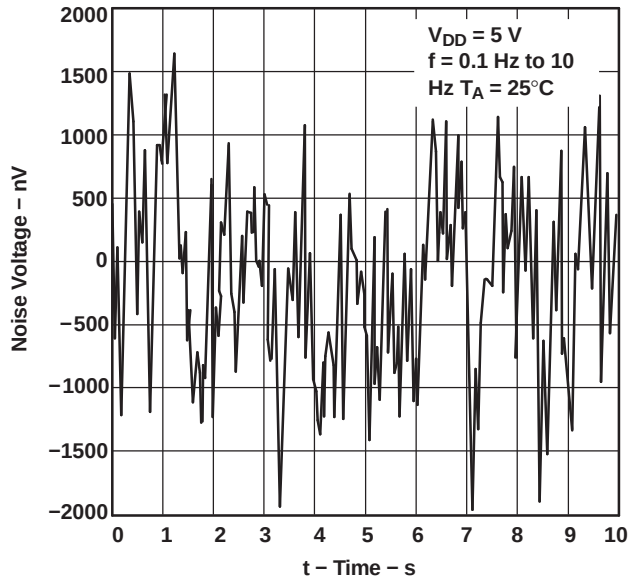



Figure 43.

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

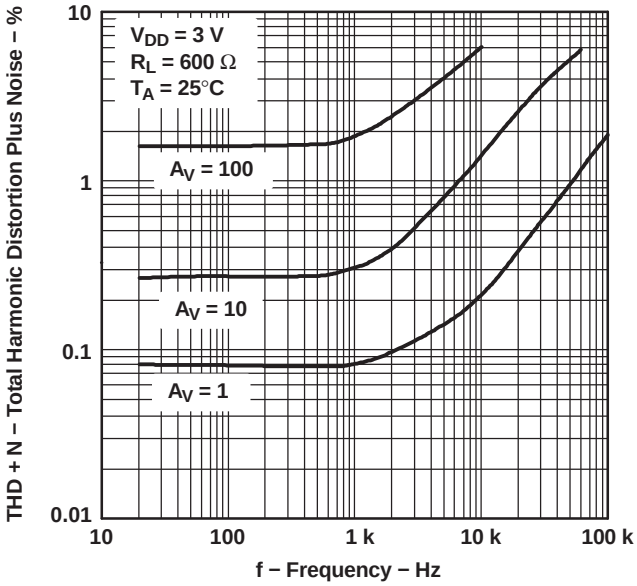



Figure 44.

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

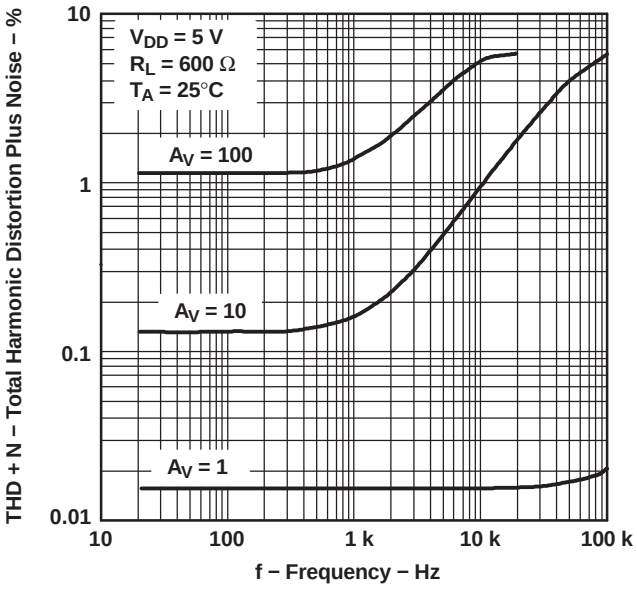



Figure 45.

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

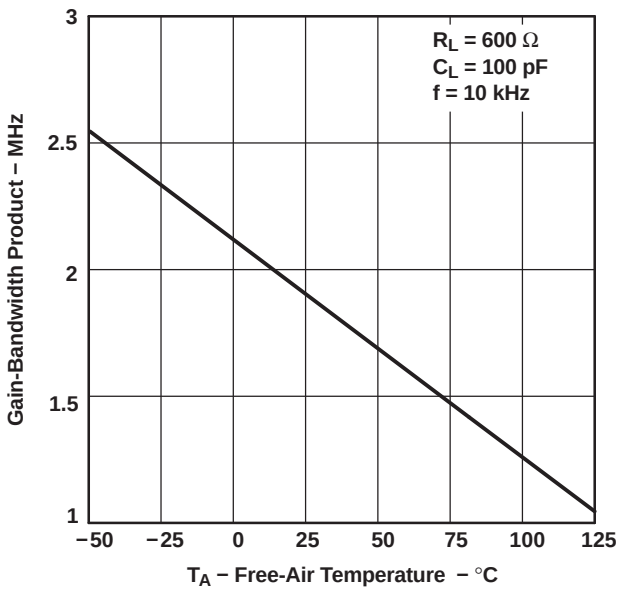



Figure 46.

**GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE**

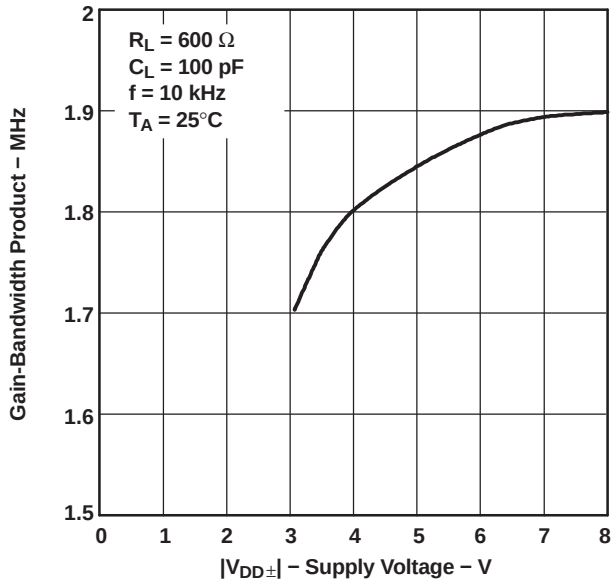



**Figure 47.**

**PHASE MARGIN vs LOAD CAPACITANCE**

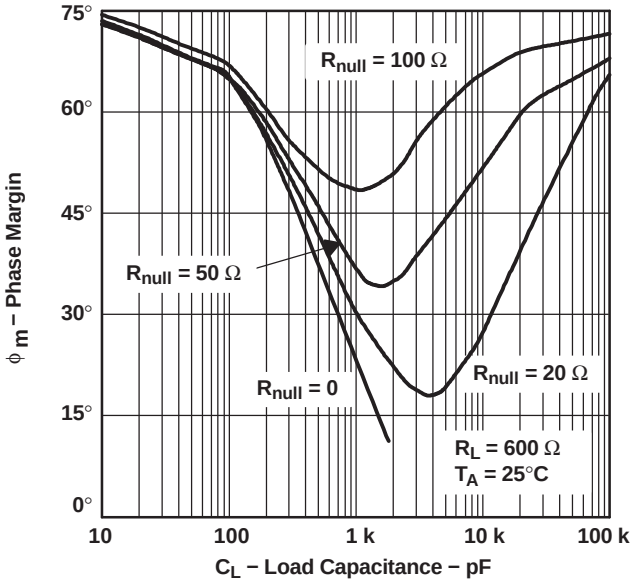



**Figure 48.**

**GAIN MARGIN vs LOAD CAPACITANCE**

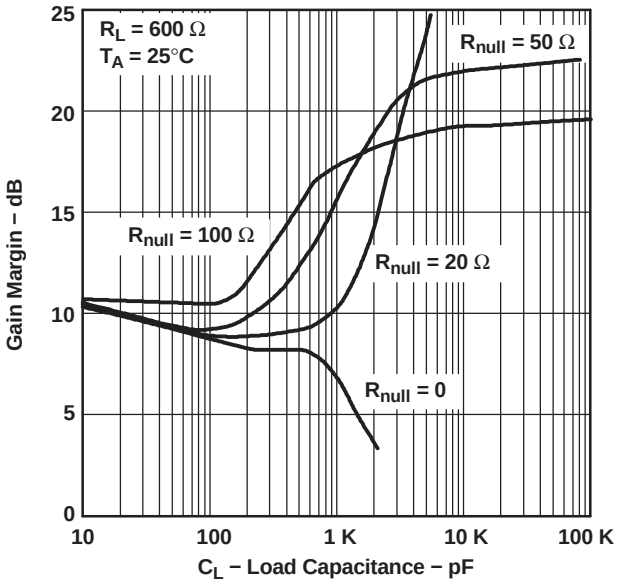



**Figure 49.**

**UNITY-GAIN BANDWIDTH vs LOAD CAPACITANCE**

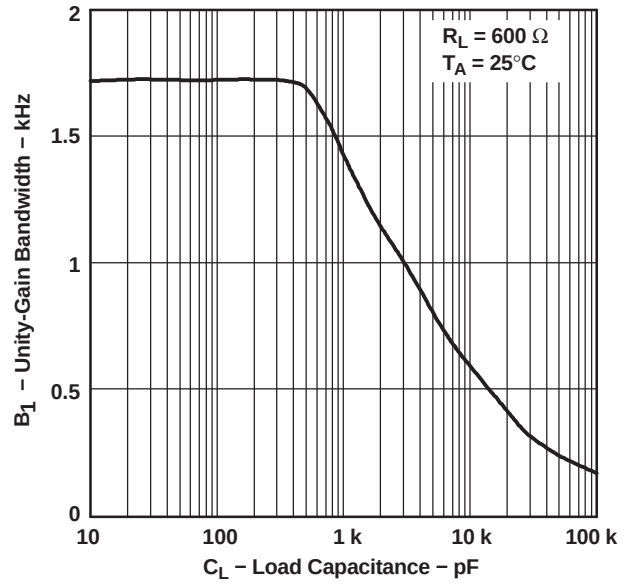



**Figure 50.**

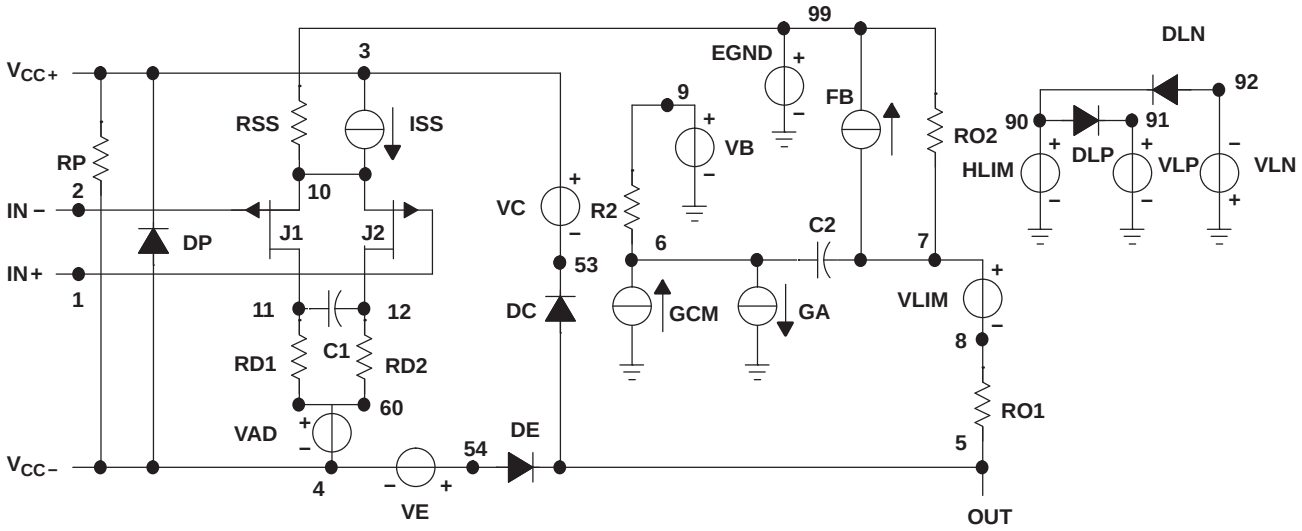
## APPLICATION INFORMATION

### macromodel information

Macromodel information provided was derived using PSpice™ Parts™ model generation software. The Boyle macromodel(2) and subcircuit in Figure 51 were generated using the TLV244x typical electrical and operating characteristics at $T_A$ = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

(2) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit




```
.SUBCKT TLV2442 1 2 3 4 5
C1      11      12      14E−12
C2      6       7       60.00E−12
DC      5       53      DX
DE      54      5       DX
DLP     90      91      DX
DLN     92      90      DX
DP      4       3       DX
EGND    99      0       POLY (2) (3,0) (4,) 0 .5 .5
FB      7       99      POLY (5) VB VC VE VLP VLN 0
+ 984.9E3 −1E6 1E6 1E6 −1E6
GA      6       0       11      12 377.0E−6
GCM     0       6       10      99 134E−9
ISS     3       10      DC 216.0E−6
HLIM    90      0       VLIM 1K
J1      11      2       10 JX
J2      12      1       10 JX
R2      6       9       100.OE3
RD1     60      11      2.653E3
RD2     60      12      2.653E3
R01     8       5       50
R02     7       99      50
RP      3       4       4.310E3
RSS     10      99      925.9E3
VAD     60      4       −.5
VB      9       0       DC 0
VC      3       53      DC .78
VE      54      4       DC .78
VLIM    7       8       DC 0
VLP     91      0       DC 1.9
VLN     0       92      DC 9.4
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=1.500E−12BETA=1.316E-3
+ VTO=−.270)
.ENDS
```

**Figure 51. Boyle Macromodel and Subcircuit**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV2442AQDRQ1 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2442AQ |
| TLV2442AQDRQ1.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2442AQ |
| TLV2442QDGKRQ1 | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | Call TI \| Nipdauag \| Nipdau | Level-2-260C-1 YEAR | -40 to 125 | OBR |
| TLV2442QDGKRQ1.A | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | Call TI | Level-2-260C-1 YEAR | -40 to 125 | OBR |
| TLV2442QPWRG4Q1 | Active | Production | TSSOP (PW) \| 8 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2442Q1 |
| TLV2442QPWRG4Q1.A | Active | Production | TSSOP (PW) \| 8 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2442Q1 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**OTHER QUALIFIED VERSIONS OF TLV2442-Q1, TLV2442A-Q1 :**

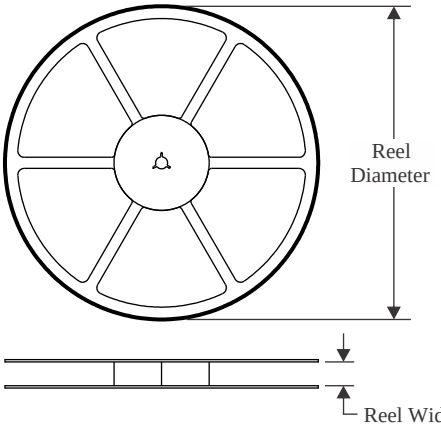
- Catalog : TLV2442, TLV2442A

NOTE: Qualified Version Definitions:

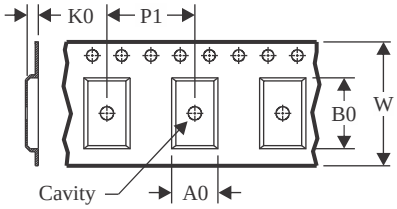
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

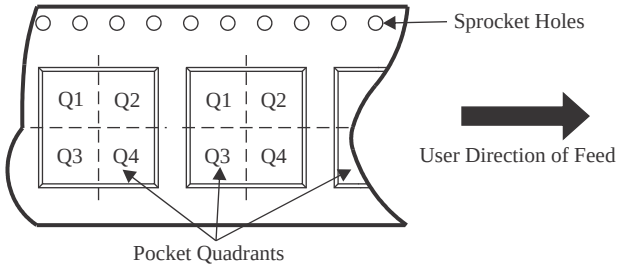



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

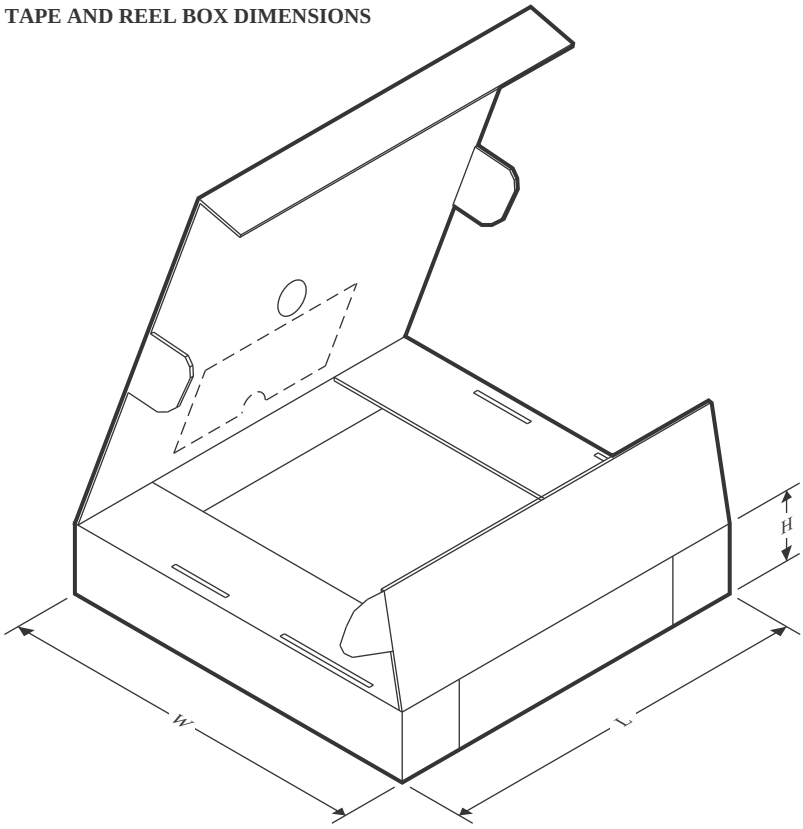
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

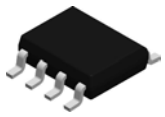
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2442QPWRG4Q1 | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV2442QPWRG4Q1 | TSSOP | PW | 8 | 2000 | 353.0 | 353.0 | 32.0 |

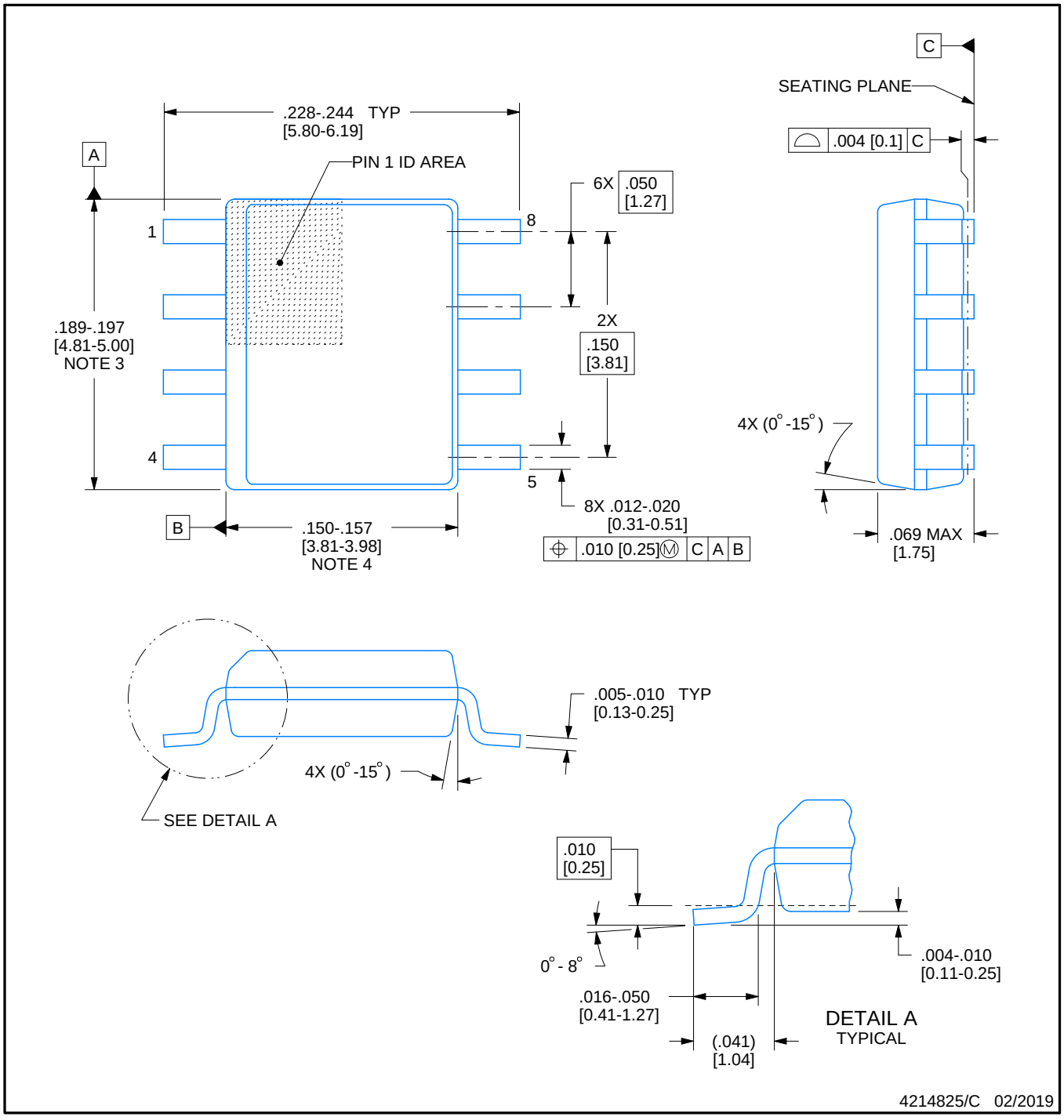


# PACKAGE OUTLINE

## D0008A

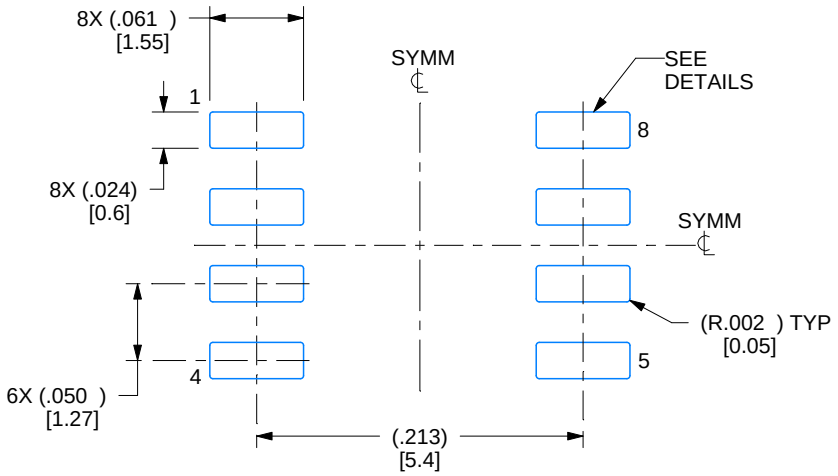
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

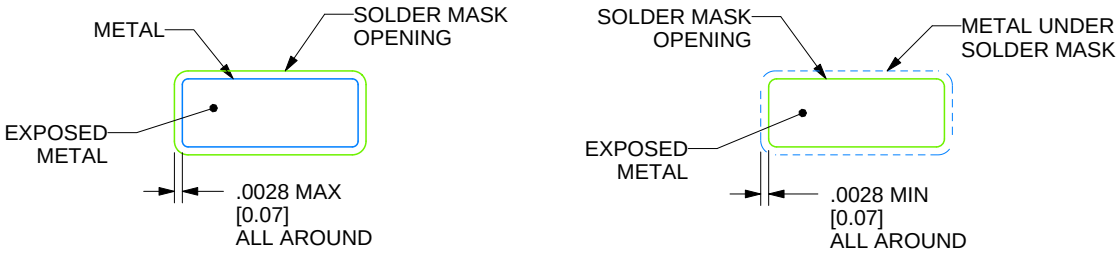



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

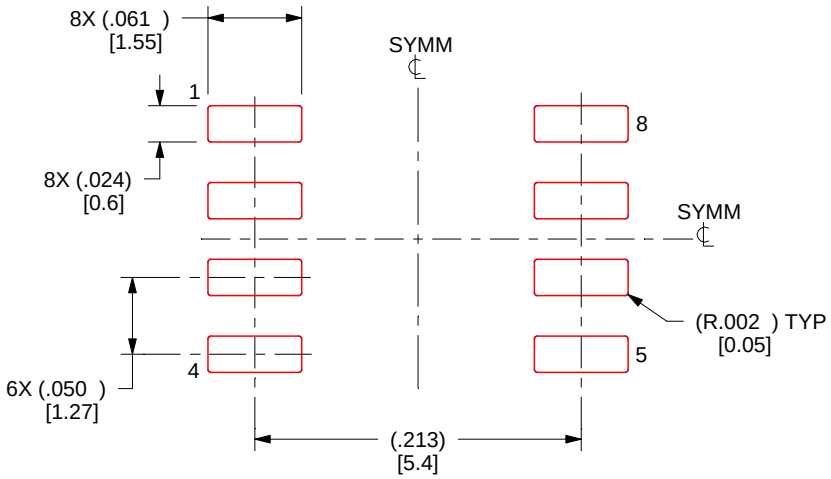
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

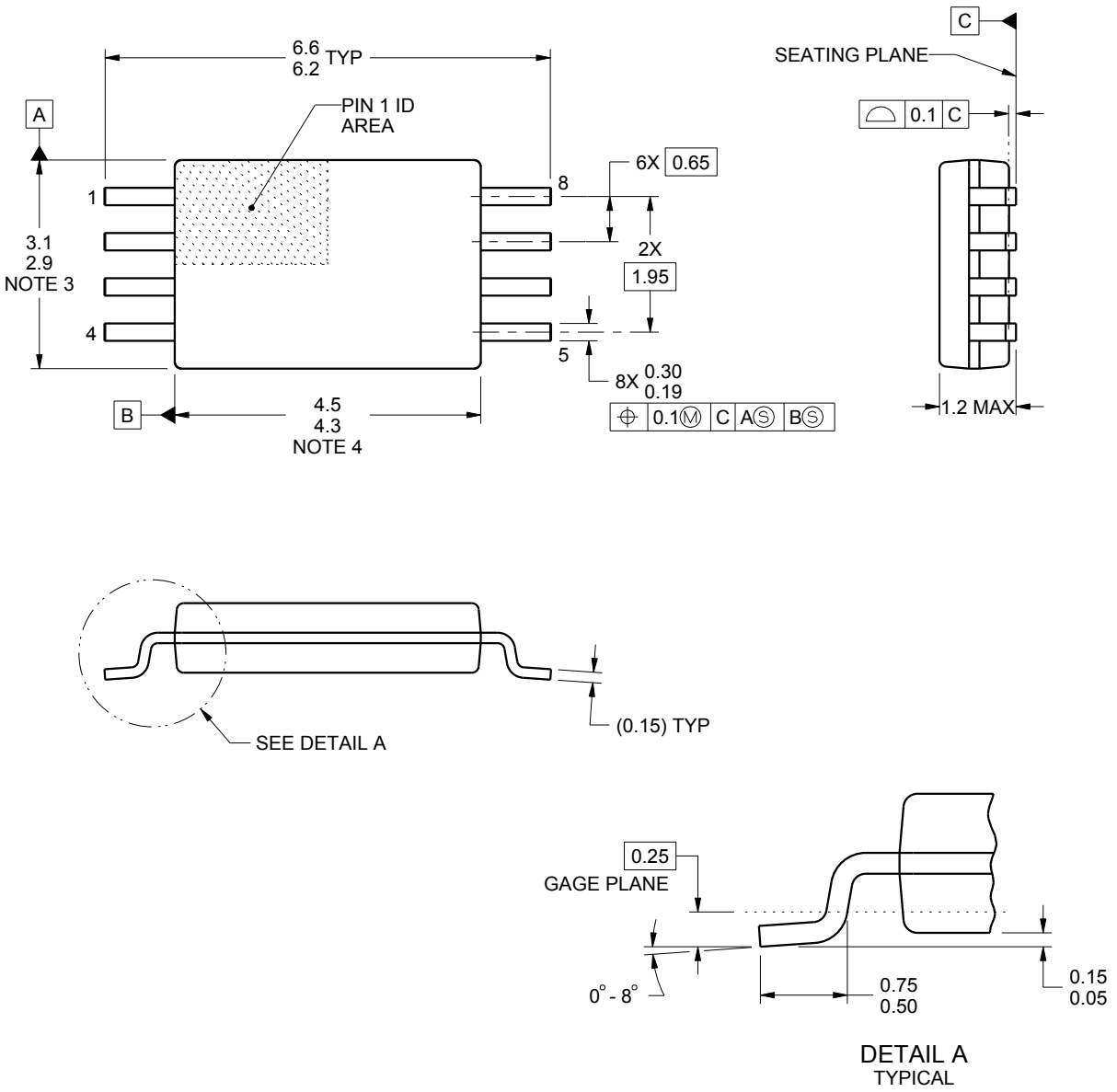
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PW0008A

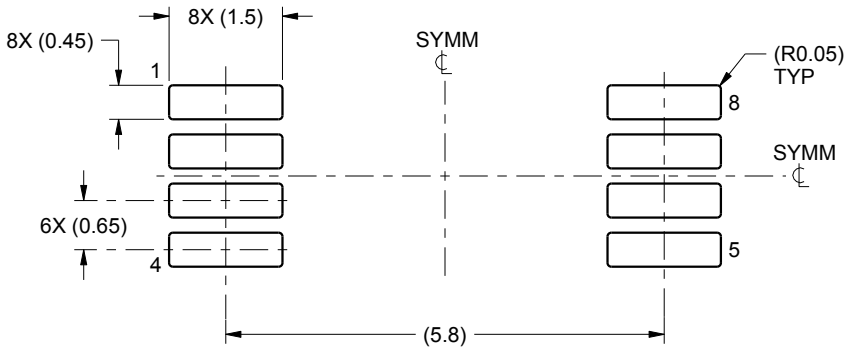
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

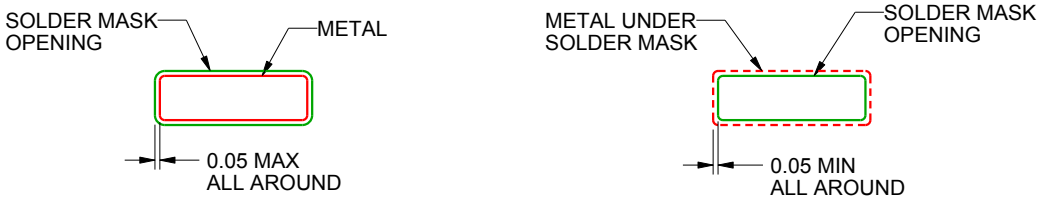



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.




LAND PATTERN EXAMPLE
SCALE:10X

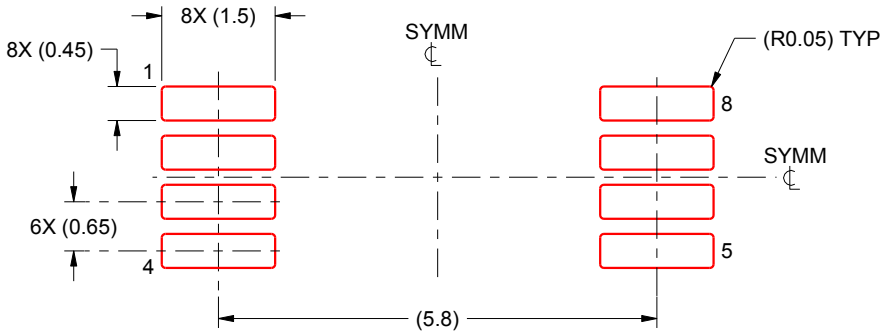



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

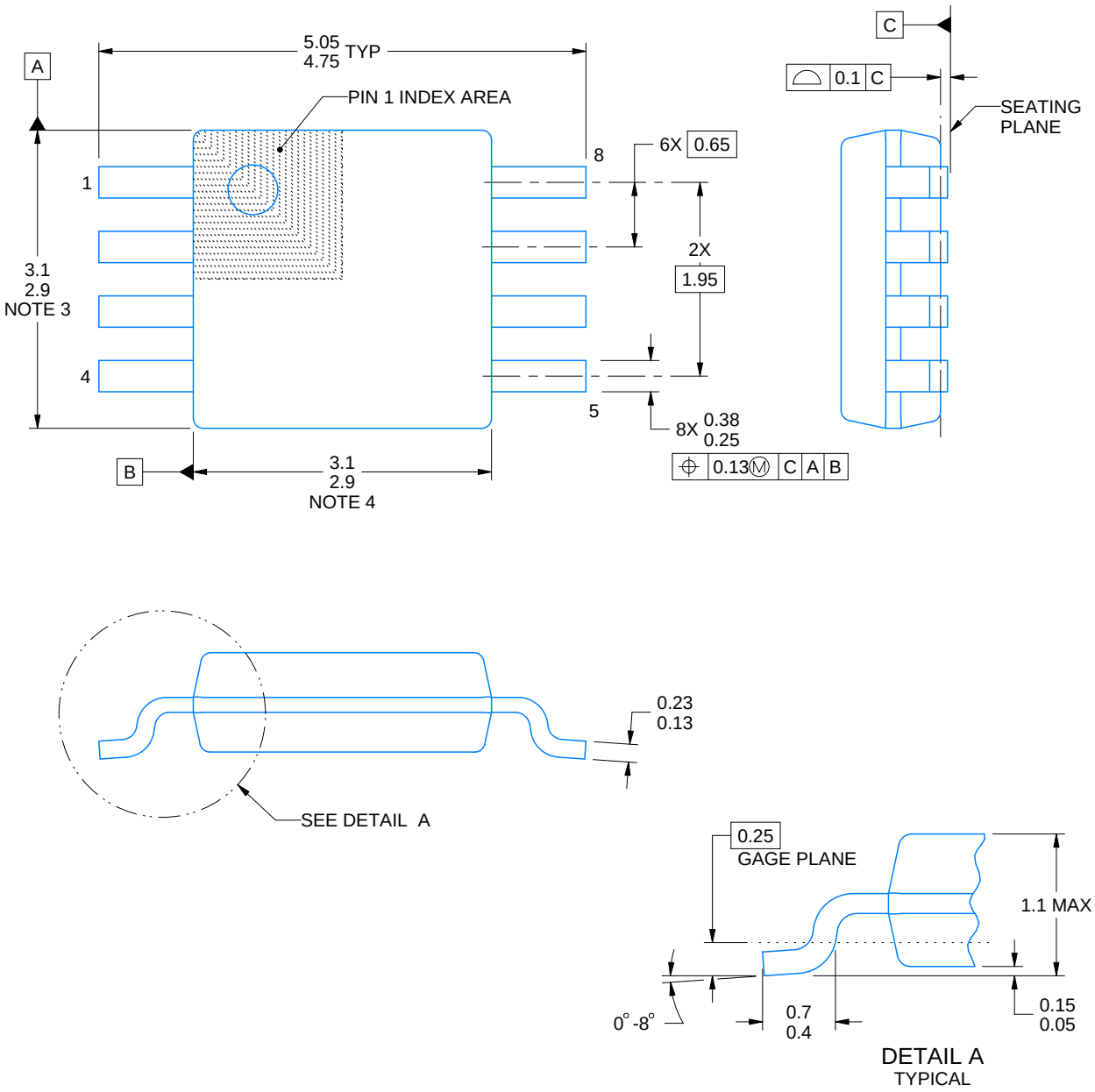
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

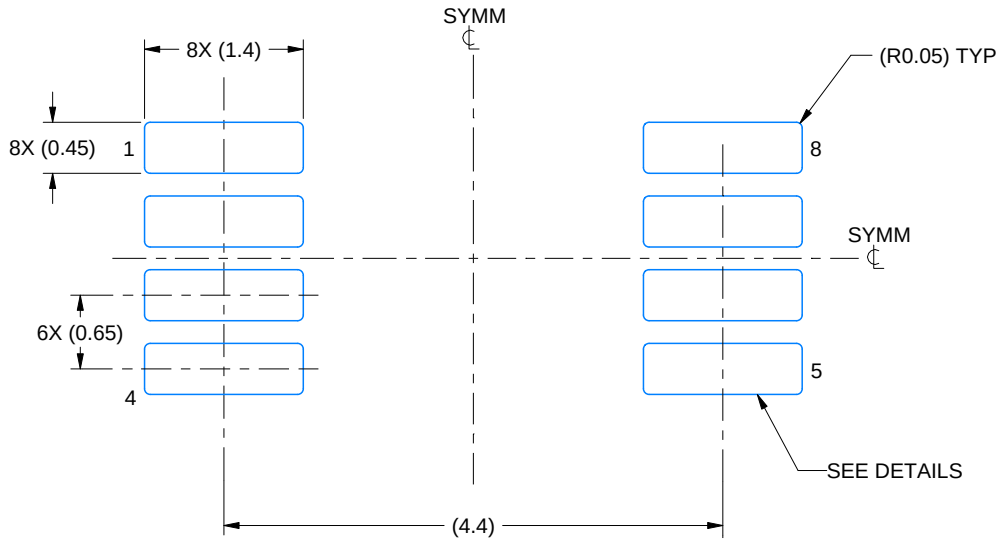
SMALL OUTLINE PACKAGE



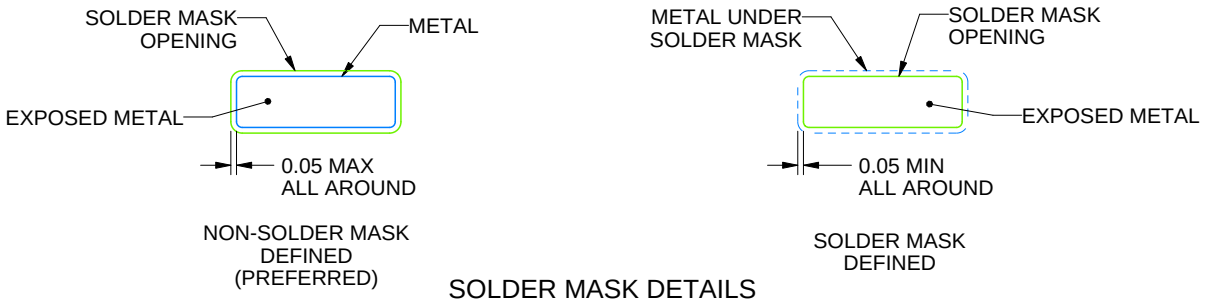

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

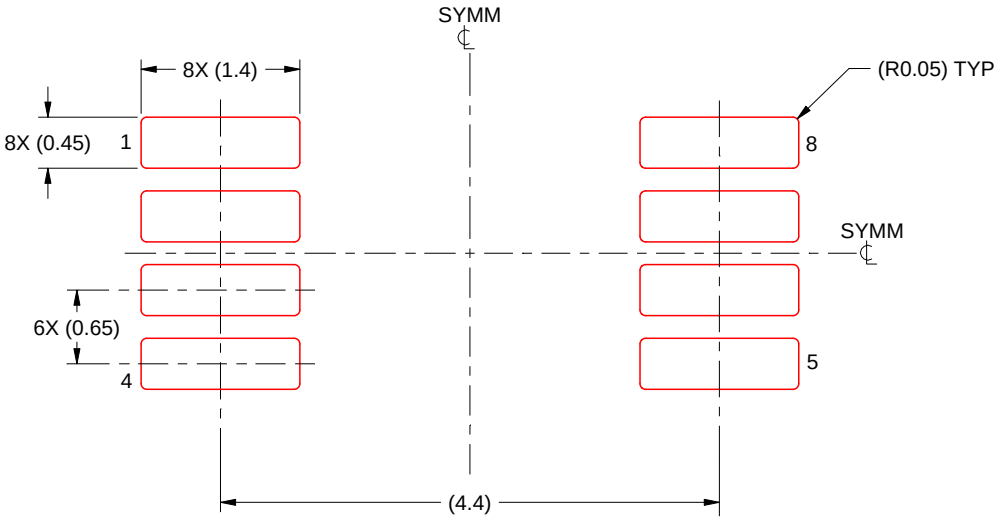



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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