TLV2721 Advanced CMOS, Rail-to-Rail, Very Low-Power, Single Operational Amplifier

1 Features

- Output swing includes both supply rails
- Low noise: 38nV/√Hz (typical) at f = 1kHz
- Low input bias current: 1pA (typical)
- Fully specified for single-supply 3V and 5V operation
- Very low power: 110µA (typical)
- Common-mode input voltage range includes negative rail
- Wide supply voltage range: 2.7V to 10V

2 Applications

- PC PSU and game console unit
- Merchant DC/DC
- Flow transmitter
- Pressure transmitter
- Merchant battery charger
- Electricity meter

3 Description

The TLV2721 is a single low-voltage operational amplifier available in the SOT-23 package. The TLV2721 offers a compromise between the ac performance and output drive of the TLV2731 and the micropower TLV2711. The device consumes only 150µA (max) of supply current and is an excellent choice for battery-powered applications. The device exhibits rail-to-rail output performance for increased dynamic range in single or split-supply applications.

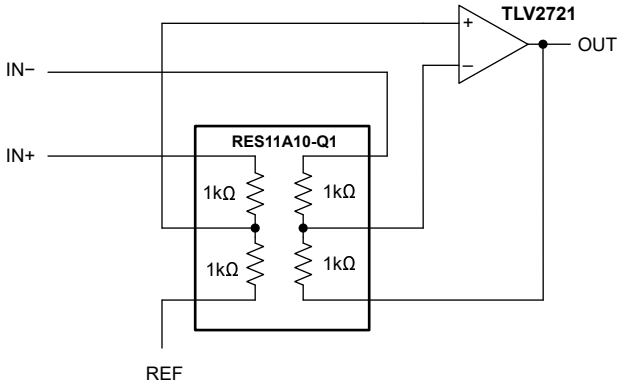
The TLV2721 is fully characterized at 3V and 5V and is optimized for low-voltage applications. The TLV2721, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3V operation, these devices work well in battery operated monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs).

With a total area of 5.6mm^2, the SOT-23 package only requires one third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pick-up from long PCB traces.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLV2721	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) For all available packages, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Difference Amplifier With RES11A-Q1

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4 Pin Configuration and Functions

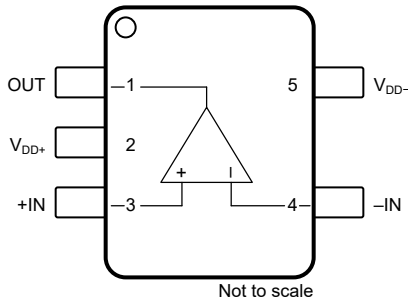


Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
−IN	4	Input	Inverting input
+IN	3	Input	Noninverting input
OUT	1	Output	Output
V−	5	Power	Negative supply
V+	2	Power	Positive supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage, $(V_{DD+}) - (V_{DD-})$(2)			12	V
V_{ID}	Differential input voltage(3)			$\pm V_{DD}$	V
V_I	Input voltage(2)		–0.3	V_{DD}	V
I_I	Input current (each input)			±5	mA
I_O	Output current			±50	mA
	Total current into supply pins	Into V_{DD+}		±50	mA
		Into V_{DD-}		±50	
	Duration of short-circuit current (at or less than 25°C)(4)		Unlimited		
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C
	Lead temperature, 1.6mm (1/16 inch) from case for 10 seconds (DBV package)			260	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) All voltage values, except differential voltages, are with respect to V_{DD-}.
(3) Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below (V_{DD}) − 0.3V.
(4) Temperature and/or supply voltages must be limited so that the maximum dissipation rating is not exceeded.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage, $(V_{DD+}) - (V_{DD-})$		2.7		10	V
V_I	Input voltage		V_{DD-}		$(V_{DD+}) - 1.3$	V
V_{IC}	Common-mode input voltage		V_{DD-}		$(V_{DD+}) - 1.3$	V
T_A	Operating free-air temperature	TLV2721C	0		70	°C
		TLV2721I	–40		85	

5.3 Thermal Information

THERMAL METRIC(1)		TLV2721 DBV (SOT5-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	113.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	37.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Electrical Characteristics V_S = 3V

at T_A = 25°C, V_{DD} = 3V, R_L = 2kΩ connected to mid-supply, and V_{IC} = V_{OUT} = V_{DD} / 2 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{IO}	Input offset voltage	TLV2721C, T_A = 0°C to 70°C			±0.5	±3	mV
		TLV2721I, T_A = –40°C to +85°C			±0.5	±3	
dV_{IO}/dT	Input offset voltage drift	TLV2721C, T_A = 0°C to 70°C			±1		µV/°C
		TLV2721I, T_A = –40°C to +85°C			±1		
PSRR	Power supply rejection ratio	V+ = 2.7V to 8V, no load		70	95		dB
			TLV2721C T_A = 0°C to 70°C	66			
			TLV2721I T_A = –40°C to +85°C	66			
INPUT BIAS CURRENT							
I_{IB}	Input bias current(1)				±1	±60	pA
		TLV2721C, T_A = 0°C to 70°C				±150	
		TLV2721I, T_A = –40°C to +85°C				±150	
I_{IO}	Input offset current(1)				±0.5	±60	pA
		TLV2721C, T_A = 0°C to 70°C				±150	
		TLV2721I, T_A = –40°C to +85°C				±150	
NOISE							
V_n	Input voltage noise	f = 10Hz			120		nV/√Hz
		f = 1kHz			38		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1Hz to 1Hz			3		µV
		f = 0.1Hz to 10Hz			6		
I_n	Input current noise				2		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 1V to 2V, f = 20kHz, R_L = 2kΩ to 1.5V	G = 1		2.52		%
			G = 10		7.01		
		V_O = 1V to 2V, f = 20kHz, R_L = 2kΩ to 0V	G = 1		0.076		
			G = 10		0.147		
INPUT VOLTAGE RANGE							
V_{IC}	Common-mode input voltage	V_{IO} ≤ 5mV		0 to 2	–0.3 to +2.2		V
			TLV2721C T_A = 0°C to 70°C	0 to 1.7			
			TLV2721I T_A = –40°C to +85°C	0 to 1.7			
CMRR	Common-mode rejection ratio	V_{IC} = 0V to 1.7V		58	77		dB
			TLV2721C T_A = 0°C to 70°C	55			
			TLV2721I T_A = –40°C to +85°C	55			
INPUT CAPACITANCE							
	Input resistance	Differential			540^9		Ω
		Common-mode			10^{12}		
c_{ic}	Common-mode input capacitance	f = 10kHz			6		pF

5.4 Electrical Characteristics V_S = 3V (continued)

at T_A = 25°C, V_{DD} = 3V, R_L = 2kΩ connected to mid-supply, and V_{IC} = V_{OUT} = V_{DD} / 2 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{VD}	Large-signal differential voltage amplification	V_O = 1V to 2V, R_L = 2kΩ		2	3		V/mV
			TLV2721C T_A = 0°C to 70°C	1			
			TLV2721I T_A = –40°C to +85°C	1			
		V_O = 1V to 2V, R_L = 10kΩ			250		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product	f = 1kHz, C_L = 100pF, R_L = 2kΩ			480		kHz
B_{OM}	Maximum output-swing bandwidth	V_O = 1V_{PP}, G = 1, C_L = 100pF, R_L = 2kΩ			30		kHz
SR	Slew rate	G = 1, C_L = 100pF, R_L = 2kΩ			0.25		V/ms
t_S	Settling time	G = –1, 1V to 2V step, R_L = 2kΩ, C_L = 100pF	0.1%		4.5		µs
			0.01%		6.8		
$Θ_M$	Phase margin at unity gain	R_L = 2kΩ, C_L = 100pF			53		°
G_M	Gain margin	R_L = 2kΩ, C_L = 100pF			12		dB
OUTPUT							
V_O	Voltage output swing	To positive rail, I_L = –100µA			2.97		V
		To positive rail, I_L = –400µA			2.88		
			TLV2721C T_A = 0°C to 70°C	2.6			
			TLV2721I T_A = –40°C to +85°C	2.6			
		To negative rail, I_L = 50µA			15		mV
		To negative rail, I_L = 500µA			150		
			TLV2721C T_A = 0°C to 70°C			500	
			TLV2721I T_A = –40°C to +85°C			500	
Z_O	Closed-loop output impedance	f = 10kHz, G = 10			90		Ω
POWER SUPPLY							
I_{DD}	Supply current	No load			100	150	µA
			TLV2721C T_A = 0°C to 70°C			200	
			TLV2721I T_A = –40°C to +85°C			200	

(1) Specification established from device population bench system measurements across multiple lots.

5.5 Electrical Characteristics V_S = 5V

at T_A = 25°C, V_{DD} = 5V, R_L = 2kΩ connected to mid-supply, and V_{IC} = V_{OUT} = V_{DD} / 2 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{IO}	Input offset voltage	TLV2721C, T_A = 0°C to 70°C			±0.5	±3	mV
		TLV2721I, T_A = –40°C to +85°C			±0.5	±3	
dV_{OS}/dT	Input offset voltage drift	TLV2721C, T_A = 0°C to 70°C			±1		µV/°C
		TLV2721I, T_A = –40°C to +85°C			±1		
PSRR	Power supply rejection ratio	V_{DD} = 4.4V to 8V, no load		80	95		dB
			TLV2721C T_A = 0°C to 70°C	80			
			TLV2721I T_A = –40°C to +85°C	80			
INPUT BIAS CURRENT							
I_{IB}	Input bias current(1)				±1	±60	pA
		TLV2721C, T_A = 0°C to 70°C				±150	
		TLV2721I, T_A = –40°C to +85°C				±150	
I_{IO}	Input offset current(1)				±0.5	±60	pA
		TLV2721C, T_A = 0°C to 70°C				±150	
		TLV2721I, T_A = –40°C to +85°C				±150	
NOISE							
V_n	Input voltage noise	f = 10Hz			120		nV/√Hz
		f = 1kHz			38		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1Hz to 1Hz			3		µV
		f = 0.1Hz to 10Hz			6		
I_n	Input current noise				2		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 1V to 3.5V, f = 20kHz, R_L = 2kΩ to 2.5V	G = 1		2.45		%
			G = 10		5.54		
		V_O = 1V to 3.5V, f = 20kHz, R_L = 2kΩ to 0V	G = 1		0.142		
			G = 10		0.257		
INPUT VOLTAGE RANGE							
V_{IC}	Common-mode input voltage	V_{IO} ≤ 5mV		0 to 4	–0.3 to 4.2		V
			TLV2721C T_A = 0°C to 70°C	0 to 3.5			
			TLV2721I T_A = –40°C to +85°C	0 to 3.5			
CMRR	Common-mode rejection ratio	V_{IC} = 0V to 2.7V, V_O = 1.5V		70	85		dB
			TLV2721C T_A = 0°C to 70°C	65			
			TLV2721I T_A = –40°C to +85°C	65			
INPUT CAPACITANCE							
	Input resistance	Differential			540^9		Ω
		Common-mode			10^{12}		
c_{ic}	Common-mode input capacitance	f = 10kHz			6		pF

5.5 Electrical Characteristics V_S = 5V (continued)

at T_A = 25°C, V_{DD} = 5V, R_L = 2kΩ connected to mid-supply, and V_{IC} = V_{OUT} = V_{DD} / 2 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{VD}	Large-signal differential voltage amplification	V_O = 1V to 4V, R_L = 2kΩ		3	5		V/mV
			TLV2721C T_A = 0°C to 70°C	1			
			TLV2721I T_A = –40°C to +85°C	1			
		V_O = 1V to 4V, R_L = 1MΩ			800		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product	f = 1kHz, C_L = 100pF, R_L = 2kΩ			510		kHz
B_{OM}	Maximum output-swing bandwidth	V_O = 1V_{PP}, G = 1, C_L = 100pF, R_L = 2kΩ			40		kHz
SR	Slew rate	G = 1, V_O = 1.5V to 3.5V, C_L = 100pF, R_L = 2kΩ			0.25		V/ms
t_S	Settling time	G = –1, 1.5V to 3.5V step, R_L = 2kΩ, C_L = 100pF	0.1%		6.8		µs
			0.01%		9.2		
Θ_M	Phase margin at unity gain	R_L = 2kΩ, C_L = 100pF			53		°
G_M	Gain margin	R_L = 2kΩ, C_L = 100pF			12		dB
OUTPUT							
V_O	Voltage output swing	To positive rail, I_L = –500µA		4.75	4.88		V
		To positive rail, I_L = –1mA		4.6	4.76		
		To negative rail, I_L = 50µA			12		mV
		To negative rail, I_L = 500µA			120		
			TLV2721C T_A = 0°C to 70°C			500	
			TLV2721I T_A = –40°C to +85°C			500	
Z_O	Closed-loop output impedance	f = 10kHz, G = 10			70		Ω
POWER SUPPLY							
I_{DD}	Supply current	No load			100	150	µA
			TLV2721C T_A = 0°C to 70°C			200	
			TLV2721I T_A = –40°C to +85°C			200	

(1) Specification established from device population bench system measurements across multiple lots.

5.6 Typical Characteristics

for all curves where V_{DD} = 5V, all loads are referenced to 2.5V, for all curves where V_{DD} = 3V, all loads are referenced to 1.5V, data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

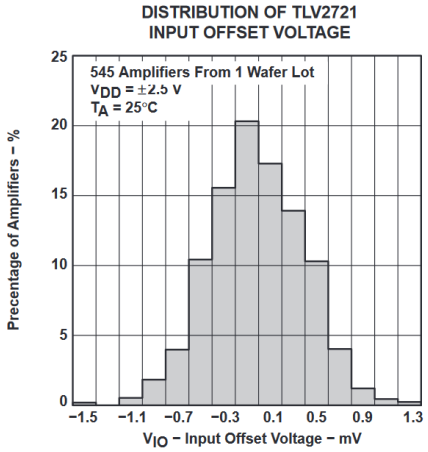


Figure 5-1.

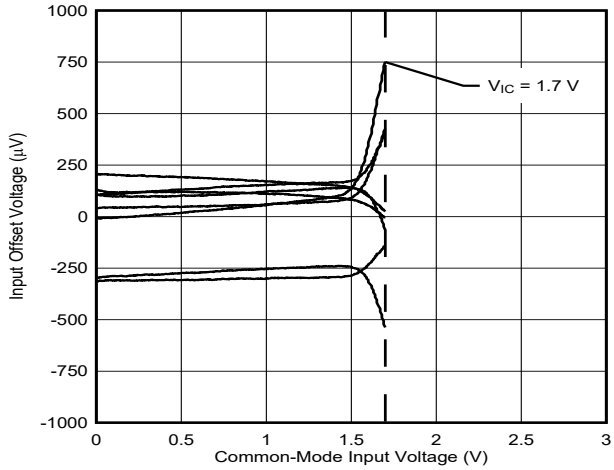


Figure 5-2. Input Offset Voltage vs Common-Mode Input Voltage (V_{DD} = 3V)

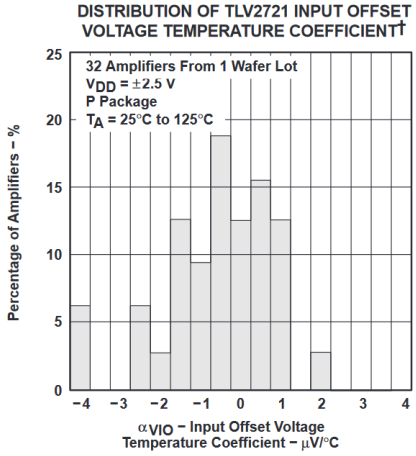


Figure 5-3.

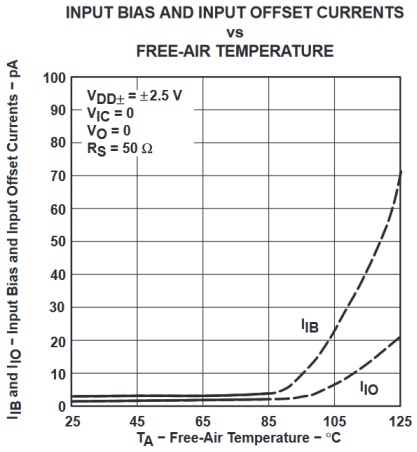


Figure 5-4.

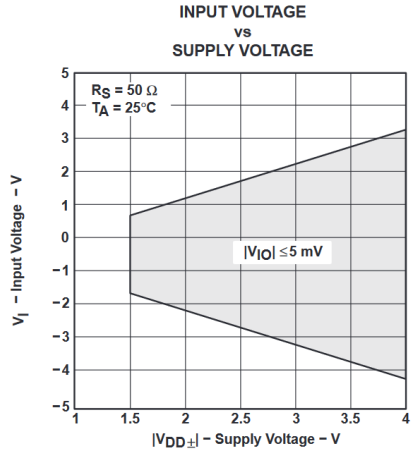


Figure 5-5.

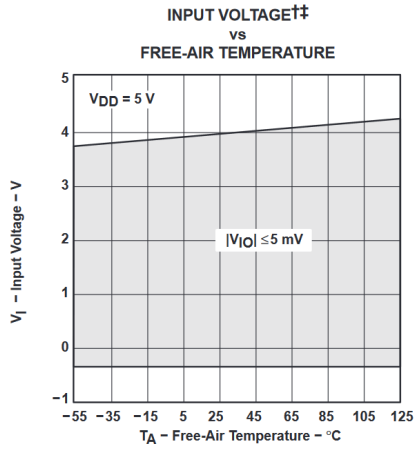


Figure 5-6.

5.6 Typical Characteristics (continued)

for all curves where V_{DD} = 5V, all loads are referenced to 2.5V, for all curves where V_{DD} = 3V, all loads are referenced to 1.5V, data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

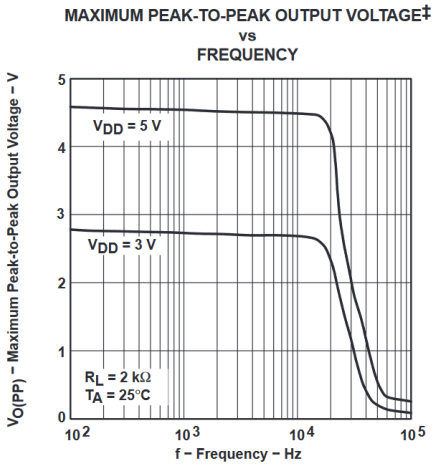


Figure 5-7.

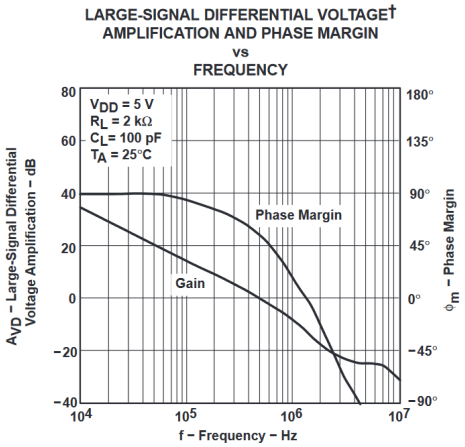


Figure 5-8.

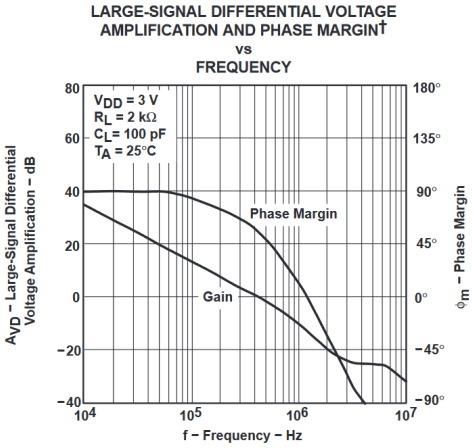


Figure 5-9.

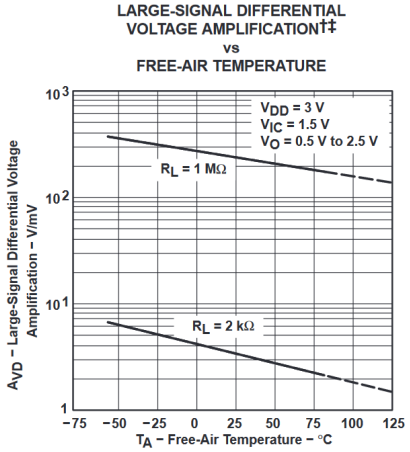


Figure 5-10.

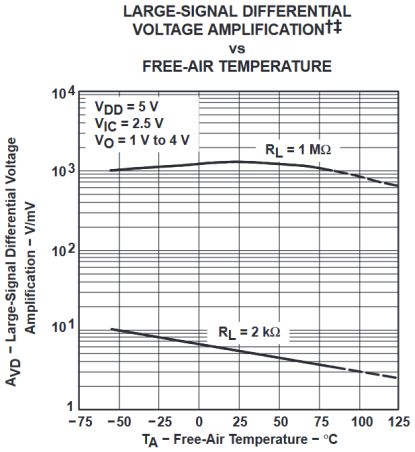


Figure 5-11.

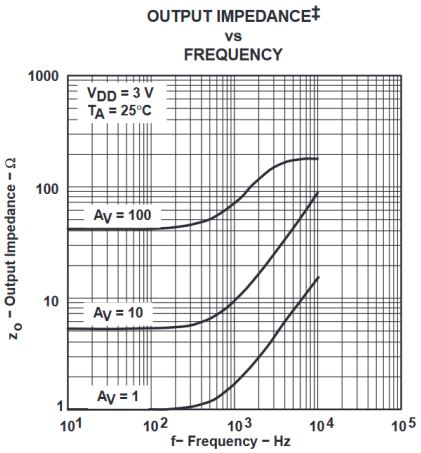


Figure 5-12.

5.6 Typical Characteristics (continued)

for all curves where V_{DD} = 5V, all loads are referenced to 2.5V, for all curves where V_{DD} = 3V, all loads are referenced to 1.5V, data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

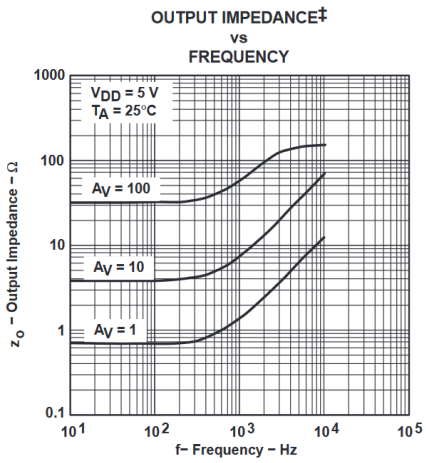


Figure 5-13.

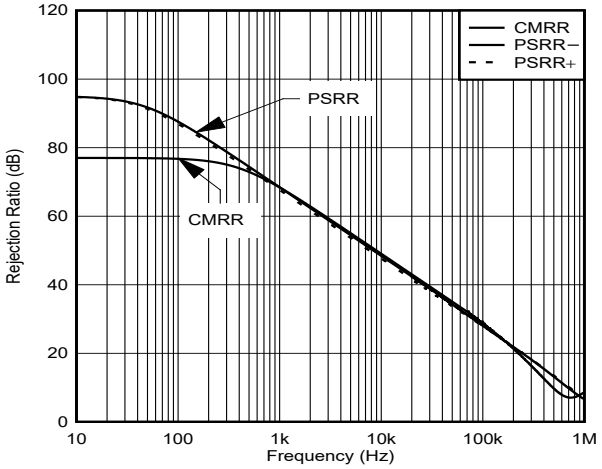


Figure 5-14. Common-Mode and Power Supply Rejection Ratio (V_{DD} = 3V)

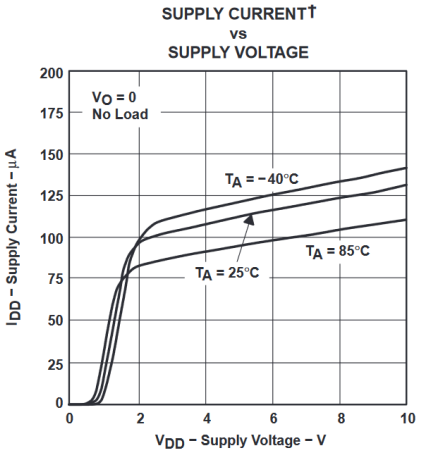


Figure 5-15.

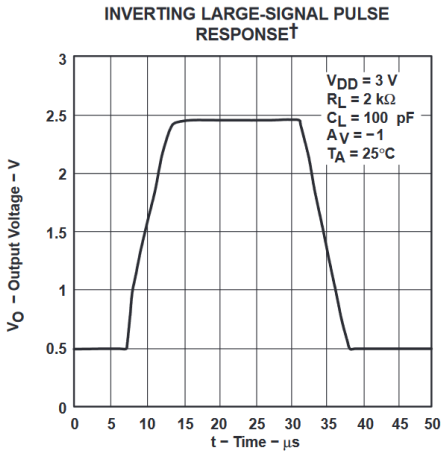
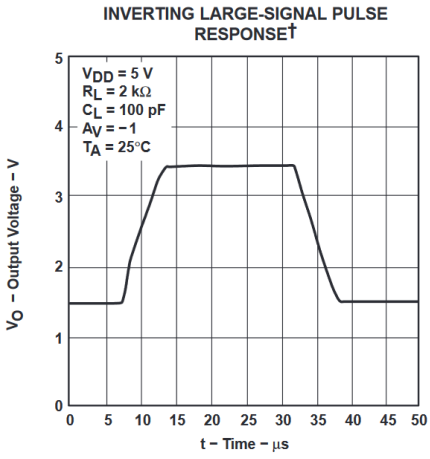


Figure 5-16.



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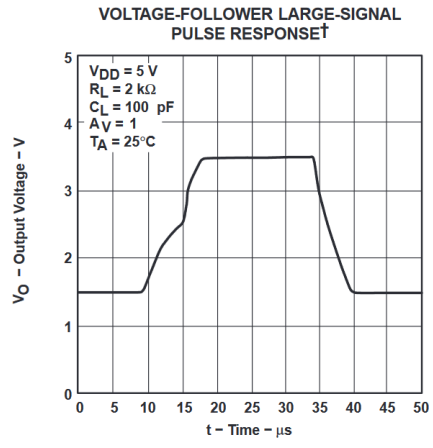


Figure 5-18.

5.6 Typical Characteristics (continued)

for all curves where V_{DD} = 5V, all loads are referenced to 2.5V, for all curves where V_{DD} = 3V, all loads are referenced to 1.5V, data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

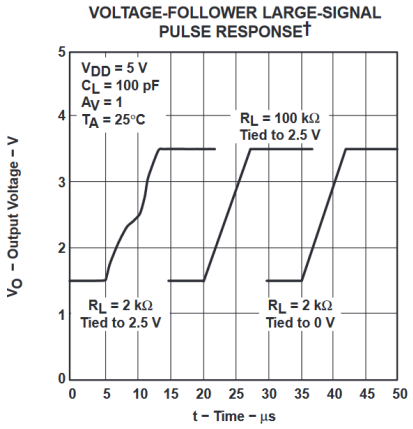


Figure 5-19.

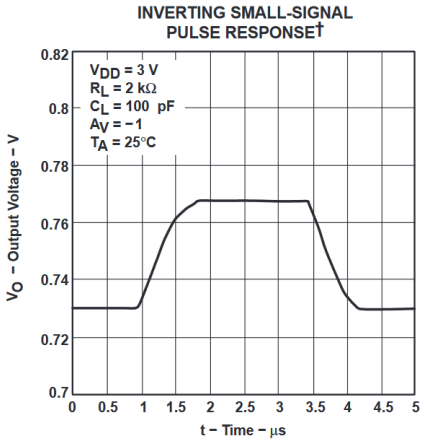


Figure 5-20.

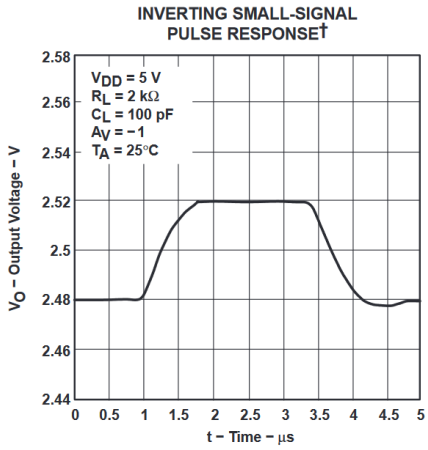


Figure 5-21.

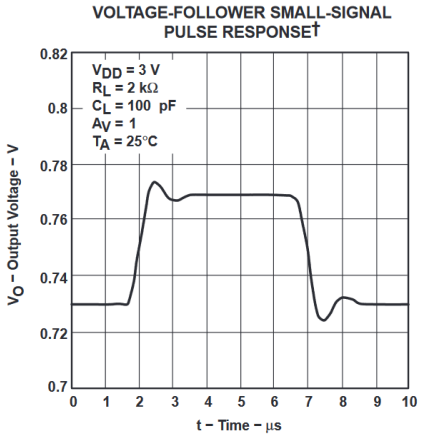


Figure 5-22.

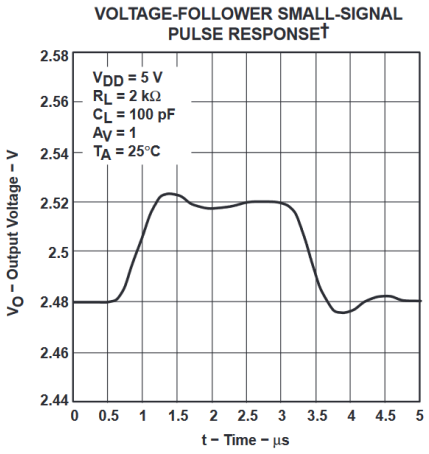


Figure 5-23.

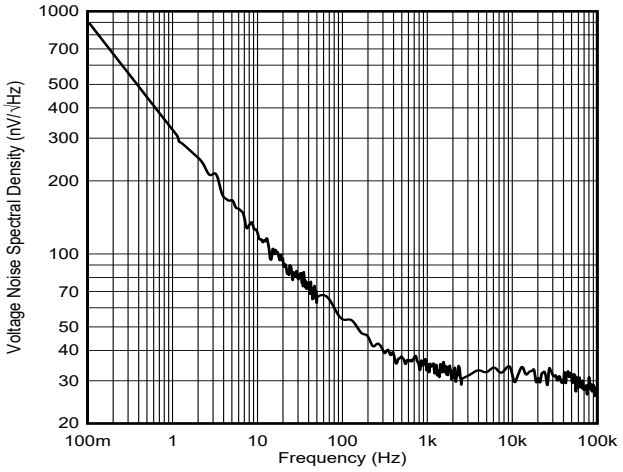


Figure 5-24. Input Voltage Noise Density (V_{DD} = 3V)

5.6 Typical Characteristics (continued)

for all curves where V_{DD} = 5V, all loads are referenced to 2.5V, for all curves where V_{DD} = 3V, all loads are referenced to 1.5V, data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

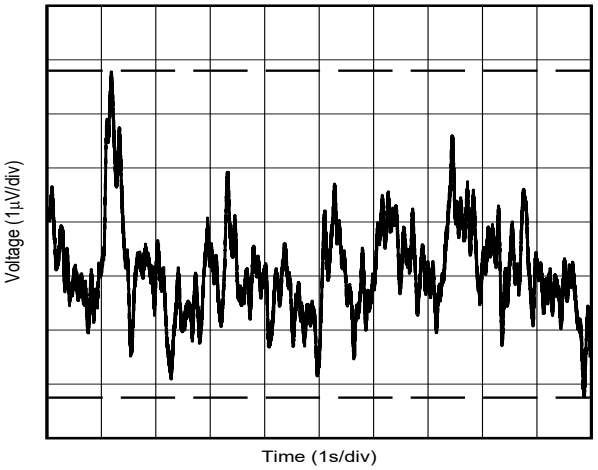


Figure 5-25. 0.1Hz to 10Hz Noise

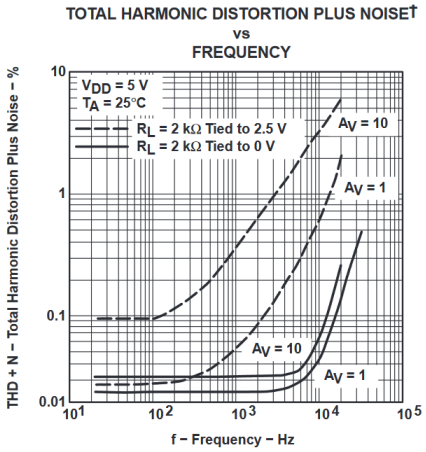


Figure 5-26.

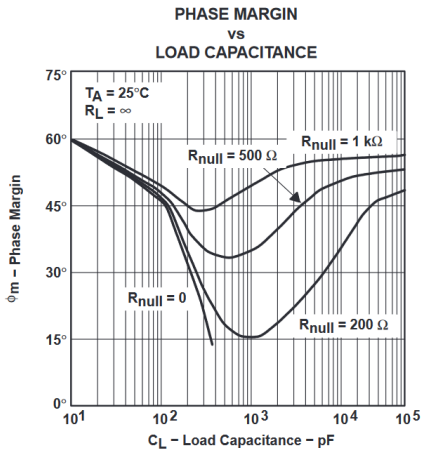


Figure 5-27.

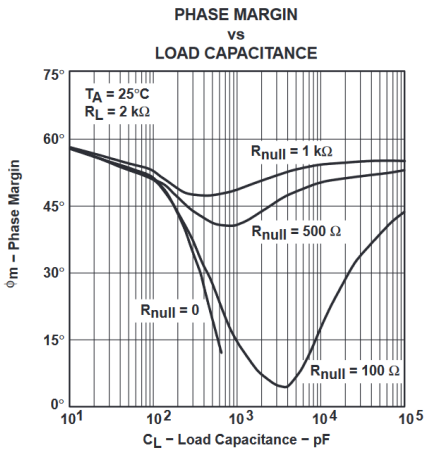


Figure 5-28.

6 Detailed Description

6.1 Overview

The TLV2721 is a single operational amplifier available in the small SOT-23 package. The TLV2721 offers low supply-current consumption and low noise. An advanced CMOS process enables the device to achieve excellent rail-to-rail output swing performance along with high input impedance. The combination of features make this device an excellent choice for a wide range of applications, including many battery-operated systems.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Driving Large Capacitive Loads

The TLV2721 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 5-27 and Figure 5-28 illustrate an ability to drive loads greater than 100pF while maintaining good gain and phase margins (R_{null} = 0Ω).

A small series resistor (R_{null}) at the output of the device (Figure 7-1) improves the gain and phase margins when driving large capacitive loads. Figure 5-27 and Figure 5-28 show the effects of adding series resistances of 100Ω, 200Ω, 500Ω, and 1kΩ. The addition of this series resistor has two effects: the first effect is that the resistor adds a zero to the transfer function and the second effect is that the resistor reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the approximate improvement in phase margin, use the following equation:

$$\Delta \phi_{m1} = \tan^{-1}(2\pi \times \text{UGBW} \times R_{null} \times C_L) \quad (1)$$

Where:

$\Delta\varphi_{m1}$ = Improvement in phase margin

UGBW = Unity-gain bandwidth frequency

R_{null} = Output series resistance

C_L = Load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases. To use Equation 1, approximate UGBW for the given capacitive load in Figure 7-1.

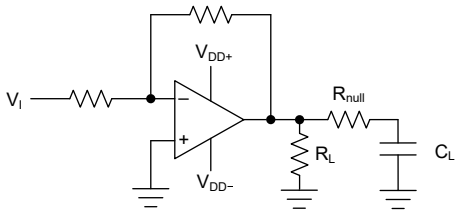


Figure 7-1. Series Resistance Circuit

The TLV2721 is designed to provide better sinking and sourcing output currents than earlier CMOS rail-to-rail output devices. This device is specified to sink 500µA and source 1mA at V_{DD} = 5V at a maximum quiescent I_{DD} of 200µA. This provides a greater than 80% power efficiency.

When driving heavy dc loads, such as 2kΩ, the positive edge under slewing conditions can experience some distortion; see also Figure 5-22. This condition is affected by three factors:

- Where the load is referenced. When the load is referenced to either rail, this condition does not occur. The distortion occurs only when the output signal swings through the point where the load is referenced. Figure 5-23 illustrates two 2kΩ load conditions. The first load condition shows the distortion seen for a 2kΩ load tied to 2.5V. The third load condition in Figure 5-23 shows no distortion for a 2kΩ load tied to 0V.
- Load resistance. As the load resistance increases, the distortion seen on the output decreases. Figure 5-23 illustrates the difference seen on the output for a 2kΩ load and a 100kΩ load with both tied to 2.5V.
- Input signal edge rate. Faster input edge rates for a step input result in more distortion than with slower input edge rates.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2001) to Revision B (July 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *Applications*, *Pin Configuration and Functions*, *Specifications*, *Thermal Information*, *Detailed Description*, *Overview*, *Application and Implementation*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Deleted TLV2721Y device and associated content from data sheet	1
• Deleted references to LinCMOS™ throughout data sheet	1
• Deleted "Macromodel included" from *Features*	1
• Changed low noise from 19nV/√Hz to 38nV/√Hz in *Features*	1
• Updated note 4 in *Absolute Maximum Ratings*	3
• Added *Thermal Information*	3
• Deleted *Dissipation Ratings Table*	3
• Added ± to input offset voltage, input offset voltage drift, input bias current, and input offset current in 3V and 5V *Electrical Characteristics*	4
• Deleted input offset voltage long-term drift from 3V and 5V *Electrical Characteristics*	4
• Changed power supply rejection ratio MIN from 80dB to 70dB in 3V *Electrical Characteristics*	4
• Changed power supply rejection ratio (–40°C to +85°C and 0°C to 70°C) from 80dB to 66dB in 3V *Electrical Characteristics*	4
• Deleted all notes from 3V and 5V *Electrical Characteristics*	4
• Added note 1 to 3V and 5V *Electrical Characteristics*	4

- Changed input voltage noise (1kHz) from 20nV/√Hz to 38nV/√Hz in 3V *Electrical Characteristics* 4
- Changed peak to peak equivalent noise voltage units from mV to nV (typo) in all *Electrical Characteristics* ... 4
- Changed peak-to-peak equivalent noise voltage (0.1Hz to 1Hz) from 680nV to 3µV in 3V *Electrical Characteristics* 4
- Changed peak-to-peak equivalent noise voltage (0.1Hz to 10Hz) from 860nV to 6µV in 3V *Electrical Characteristics* 4
- Changed input current noise from 0.6fA/√Hz to 2fA/√Hz in 3V and 5V *Electrical Characteristics* 4
- Changed common-mode rejection ratio MIN from 70dB to 58dB and TYP from 82dB to 77dB in 3V *Electrical Characteristics* 4
- Changed common-mode rejection ratio (0°C to 70°C and –40°C and +85°C) MIN from 65dB to 55dB in 3V *Electrical Characteristics* 4
- Changed input resistance (differential) from 10^{12}Ω to 540^{9}Ω in 3V and 5V *Electrical Characteristics* 4
- Deleted slew rate at unity gain MIN for 25°C and full range on 3V and 5V *Electrical Characteristics* tables..... 4
- Changed input voltage noise (10Hz) from 90nV/√Hz to 120nV/√Hz in 5V *Electrical Characteritics* 6
- Changed input voltage noise (1kHz) from 19nV/√Hz to 38nV/√Hz in 5V *Electrical Characteristics* 6
- Changed peak-to-peak equivalent noise voltage (0.1Hz to 1Hz) from 800nV to 3µV in 5V *Electrical Characteristics* 6
- Changed peak-to-peak equivalent noise voltage (0.1Hz to 10Hz) from 960nV to 6µV in 5V *Electrical Characteristics* 6
- Deleted Figures 1, 4–5, 10–14, 16–20, 27–31, 33–34, 45, 47–50, and 53–54..... 8
- Updated Figures 5-2, 5-23, and 5-24..... 8
- Added Figure 5-14..... 8
- Deleted *Macromodel Information* 13

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2721CDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	VAKC
TLV2721CDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	VAKC
TLV2721CDBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-	VAKC
TLV2721IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	No	SN	Level-1-260C-UNLIM	-40 to 85	VAKI
TLV2721IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	VAKI
TLV2721IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	No	SN	Level-1-260C-UNLIM	-40 to 85	VAKI
TLV2721IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	VAKI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

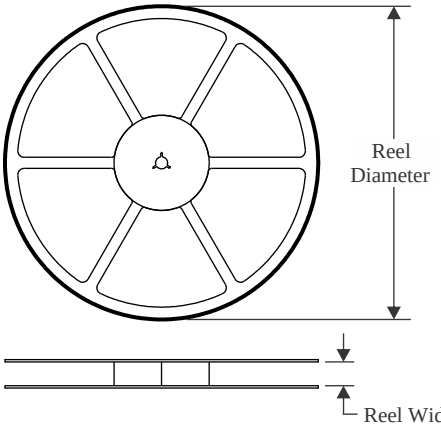
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

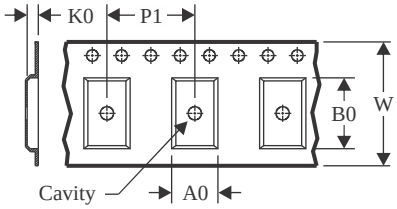
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

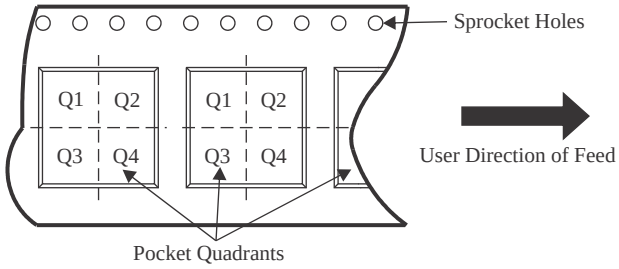


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

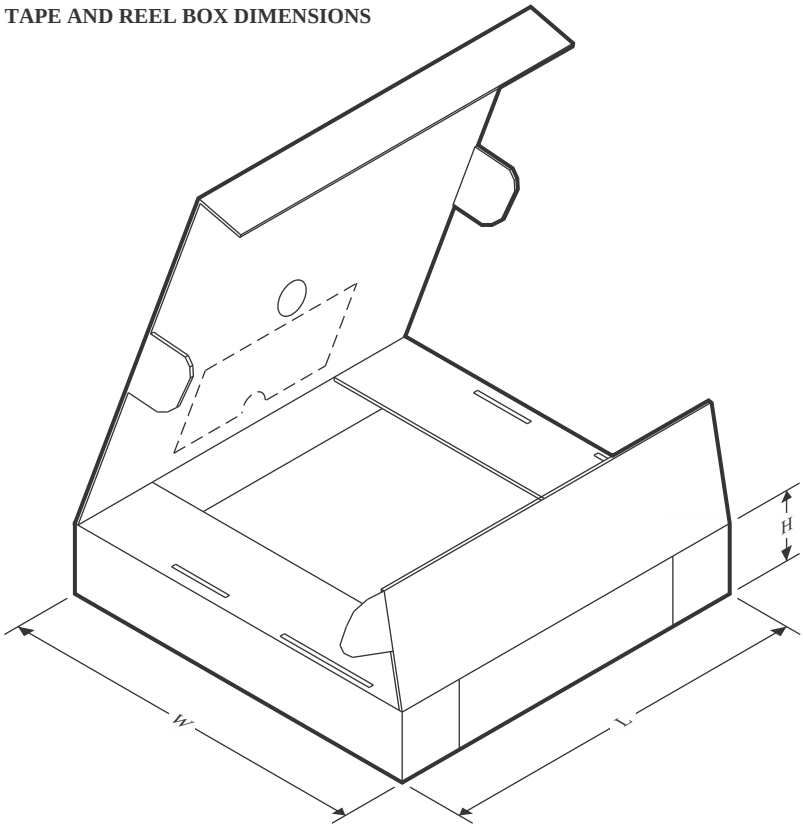
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2721CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2721IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

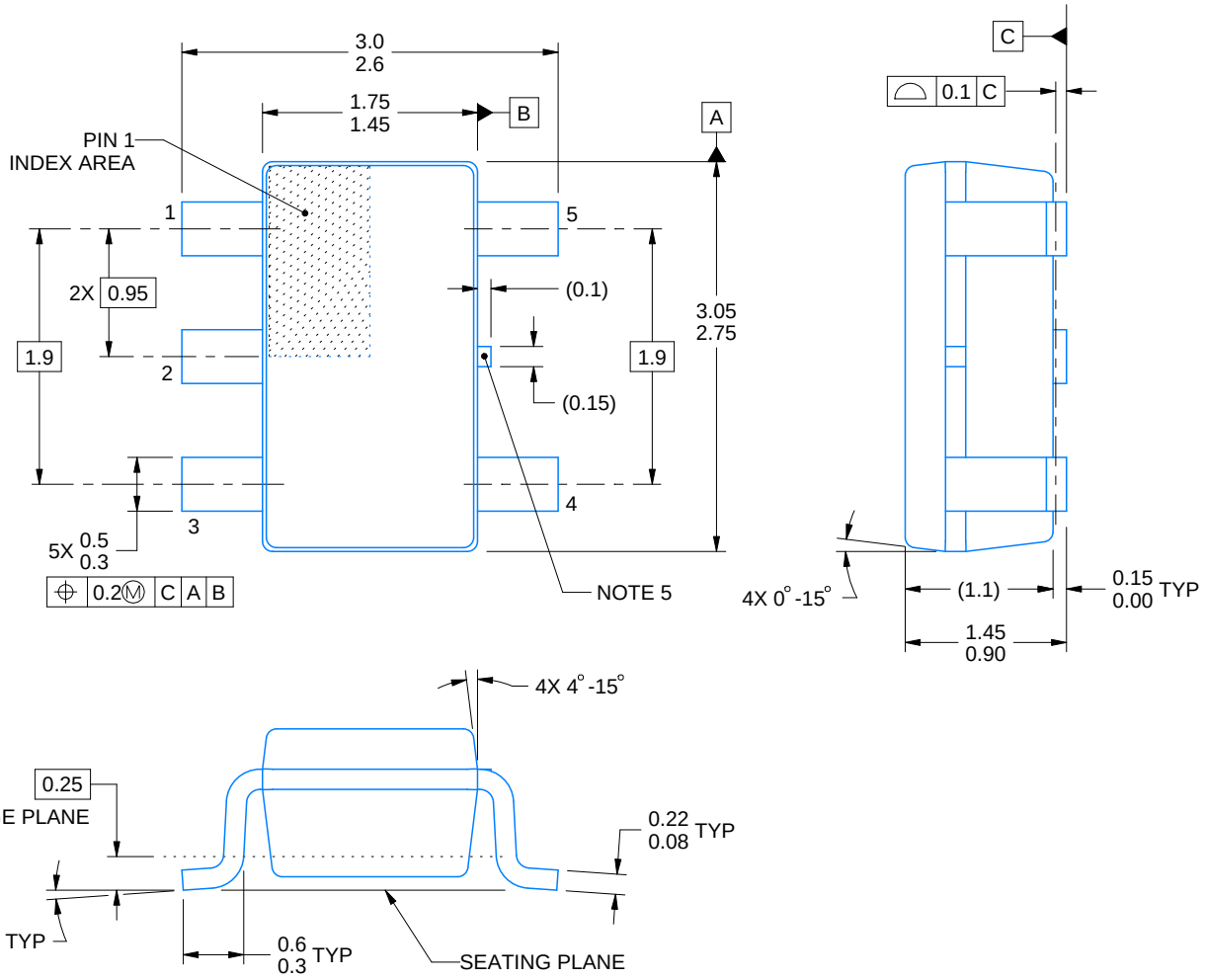
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2721CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV2721IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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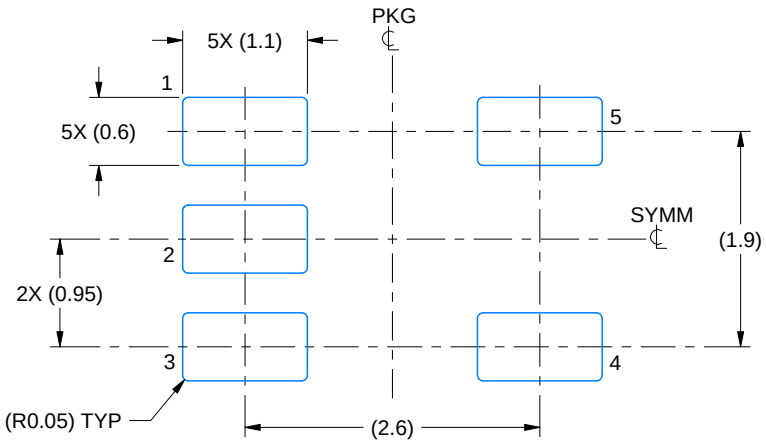
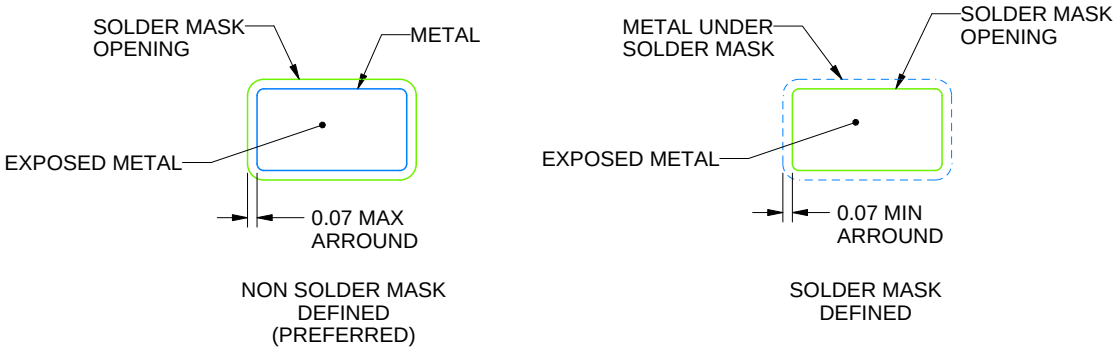
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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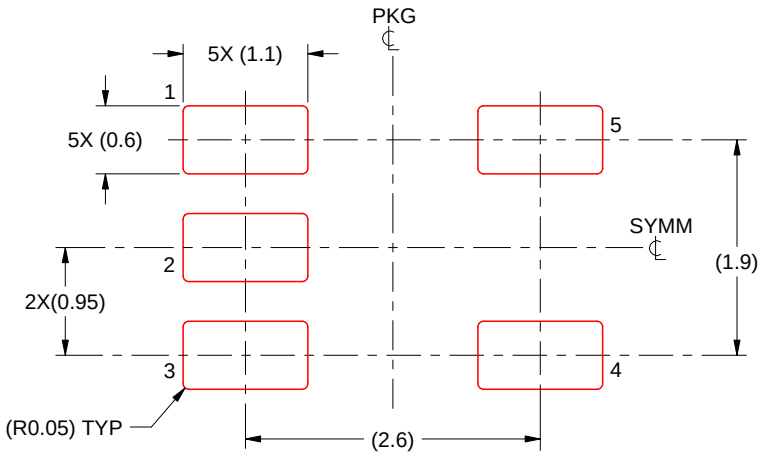
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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