TLV700xx-Q1 Automotive, 200mA, Low-I_Q, Low-Dropout Regulator (LDO) for Portable Devices

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to 125°C, T_A
  - Device HBM ESD classification level H2
  - Device CDM ESD classification level C4B
- 2% accuracy
- Low I_Q: 31µA
- Fixed output voltage combination possible from 1.9V to 4.8V
- High PSRR: 68dB at 1kHz
- Stable with effective capacitance of 0.1µF
- Thermal shutdown and overcurrent protection
- Latch-up performance meets 100mA per AEC-Q100, level I
- Available in SOT-23-5 and SC70 packages

2 Applications

- Automotive camera modules
- Image sensor power
- Microprocessor rails
- Automotive infotainment head units
- Automotive body electronics

3 Description

The TLV700xx-Q1 family of low-dropout (LDO) linear regulators are low-quiescent-current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision band-gap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage make this series of devices designed for for most battery-operated handheld equipment. All device versions have thermal shutdown and current limit for safety.

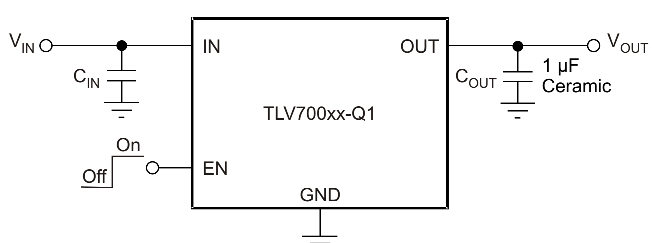
Furthermore, these devices are stable with an effective output capacitance of only 0.1µF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

The TLV700xx-Q1 LDOs are available in SOT-23-5 and SC70 packages.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLV700xx-Q1	DCK (SC70, 5)	2mm × 2.1mm
	DDC (SOT, 5)	2.9mm × 2.8mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit (Fixed-Voltage Versions)

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4 Pin Configuration and Functions

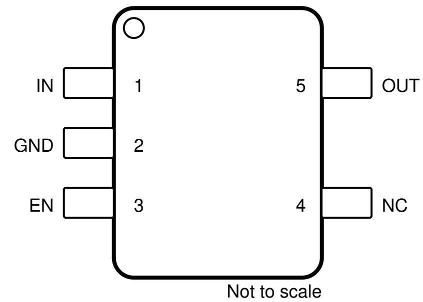


Figure 4-1. DDC and DCK Packages, 5-Pin SOT (Top View)

Table 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	SC70	SOT		
EN	3	3	I	Enable pin. Driving EN over 0.9V turns on the regulator. Driving EN below 0.4V puts the regulator into shutdown mode and reduces operating current to 1µA, nominal.
GND	2	2	—	Ground pin
IN	1	1	I	Input pin. A small 1µF ceramic capacitor is recommended from this pin to ground to provide stability and good transient performance. See the *Input and Output Capacitor Requirements* section for more details.
NC	4	4	—	No connection. This pin can be tied to ground to improve thermal dissipation.
OUT	5	5	O	Regulated output voltage pin. A small 1µF ceramic capacitor is needed from this pin to ground to provide stability. See the *Input and Output Capacitor Requirements* section for more details.

5 Specifications

5.1 Absolute Maximum Ratings

at T_A = –40°C to +125°C (unless otherwise noted); all voltages are with respect to GND[(1)]

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{EN}	Enable voltage	–0.3	V_{IN} + 0.3	V
V_{OUT}	Output voltage	–0.3	6	V
I_{OUT}	Maximum output current	Internally limited		
	Output short-circuit duration	Indefinite		
T_A	Operating ambient temperature	–40	150	°C
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2		5.5	V
V_{EN}	Enable voltage	0		5.5	V
I_{OUT}	Output current		200		mA
C_{IN}	Input capacitor	0	1		µF
C_{OUT}	Output capacitor	0.22	1		µF
T_A	Operating ambient temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		TLV700xx-Q1 DDC (SOT) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	262.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

at T_A = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.3V or 2V (whichever is greater), I_{OUT} = 10mA, V_{EN} = V_{IN}, and C_{OUT} = 1µF (unless otherwise noted); typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2		5.5	V
V_{OUT}	DC output accuracy	–40°C ≤ T_A ≤ +125°C, V_{OUT} ≥ 1V	–2%		2%	
$ΔV_O/ΔV_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 10mA		1	5	mV
$ΔV_O/ΔI_{OUT}$	Load regulation	0mA ≤ I_{OUT} ≤ 200mA			15	mV
V_{DO}	Dropout voltage(1)	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 200mA		175	250	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$	220	350	860	mA
I_{GND}	Ground pin current	I_{OUT} = 0mA		31	55	µA
		I_{OUT} = 200mA, V_{IN} = V_{OUT} + 0.5V		270		
I_{SHDN}	Ground pin current (shutdown)	V_{EN} ≤ 0.4V, 2.0V ≤ V_{IN} ≤ 4.5V		1	2.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3V, V_{OUT} = 1.8V, I_{OUT} = 10mA, f = 1kHz		68		dB
V_N	Output noise voltage	BW = 100Hz to 100kHz, V_{IN} = 2.3V, V_{OUT} = 1.8V, I_{OUT} = 10mA		48		$µV_{RMS}$
t_{STR}	Startup time(2)	C_{OUT} = 1µF, I_{OUT} = 200mA		100		µs
$V_{EN(HI)}$	Enable pin high (enabled)		0.9		V_{IN}	V
$V_{EN(LO)}$	Enable pin low (disabled)		0		0.4	V
I_{EN}	Enable pin current	V_{EN} = 5.5V , I_{OUT} = 10µA		0.04	0.5	µA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		
T_A	Operating ambient temperature		–40		125	°C

(1) V_{DO} is measured for devices with $V_{OUT(NOM)}$ ≥ 2.35V.
(2) Startup time = time from EN assertion to 0.98 × $V_{OUT(NOM)}$.

5.6 Typical Characteristics

at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2V (whichever is greater), I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted); typical values are at T_J = 25°C

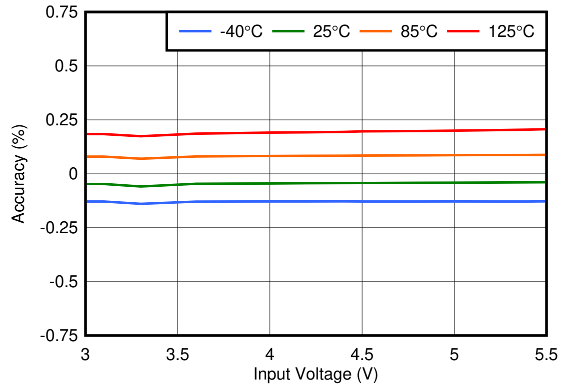


Figure 5-1. TLV70028-Q1 Line Regulation

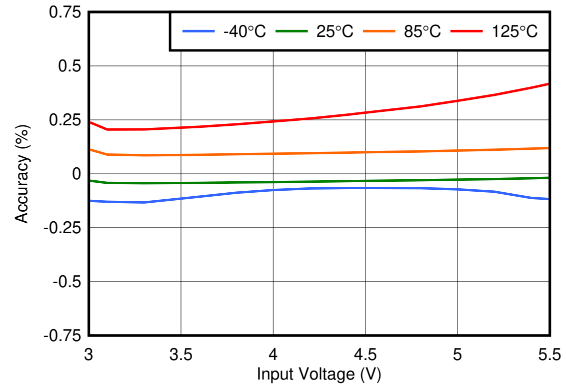


Figure 5-2. TLV70028-Q1 Line Regulation

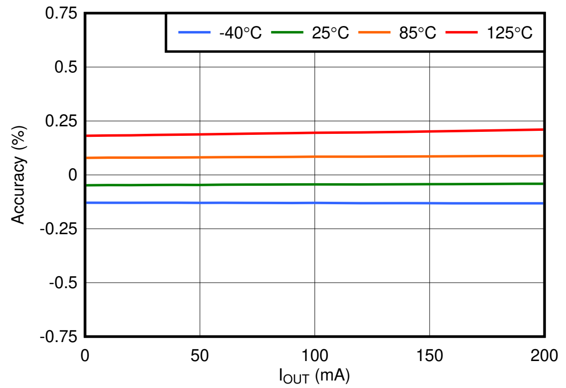


Figure 5-3. TLV70028-Q1 Load Regulation

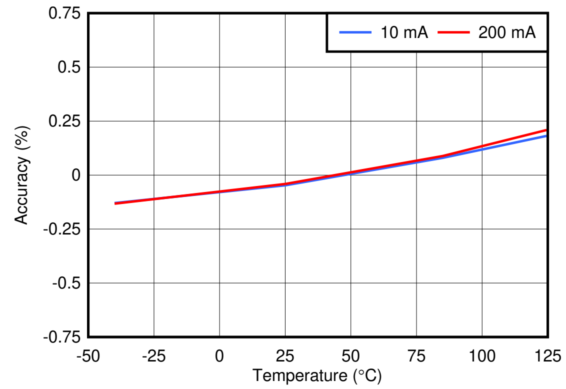


Figure 5-4. TLV70028-Q1 Accuracy vs Temperature

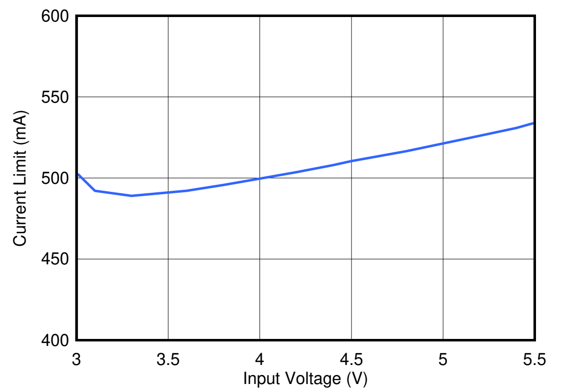


Figure 5-5. TLV70028-Q1 Current Limit vs Input Voltage

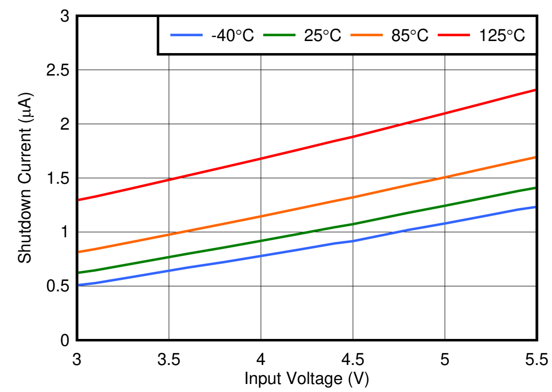


Figure 5-6. TLV70028-Q1 Shutdown Current vs Input Voltage

5.6 Typical Characteristics (continued)

at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2V (whichever is greater), I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted); typical values are at T_J = 25°C

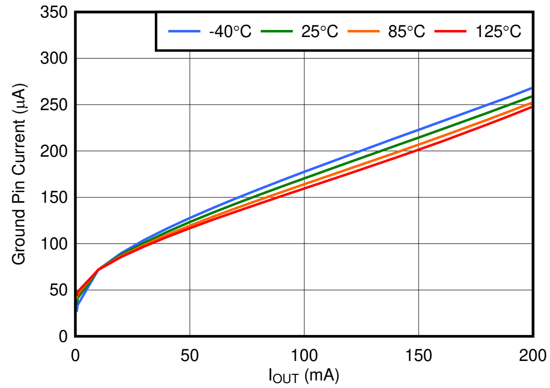


Figure 5-7. TLV70028-Q1 Ground Pin Current vs Output Current

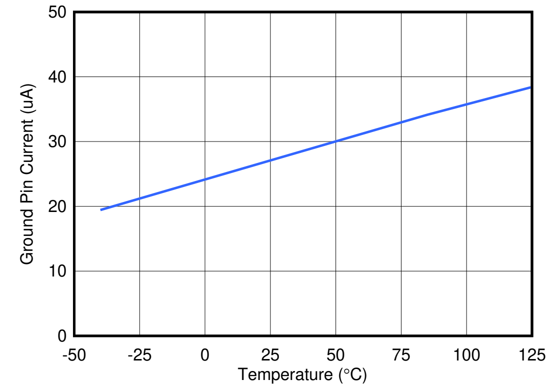
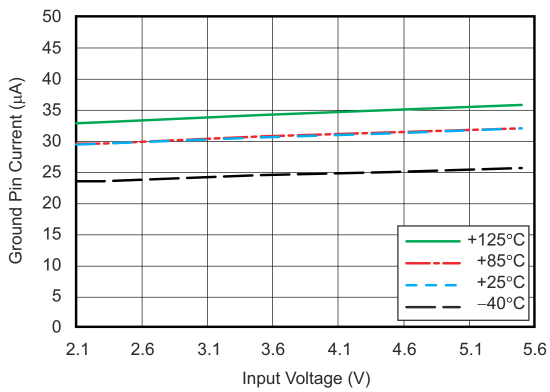
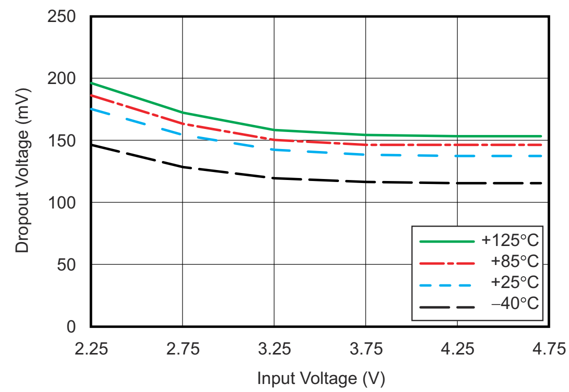


Figure 5-8. TLV70028-Q1 Ground Pin Current vs Temperature



I_{OUT} = 0mA

Figure 5-9. TLV70048-Q1 Ground Pin Current vs Input Voltage



I_{OUT} = 200mA

Figure 5-10. TLV70048-Q1 Dropout Voltage vs Input Voltage

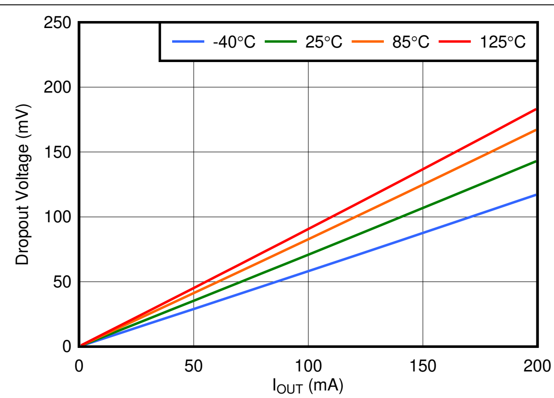


Figure 5-11. TLV70028-Q1 Dropout Voltage vs Output Current

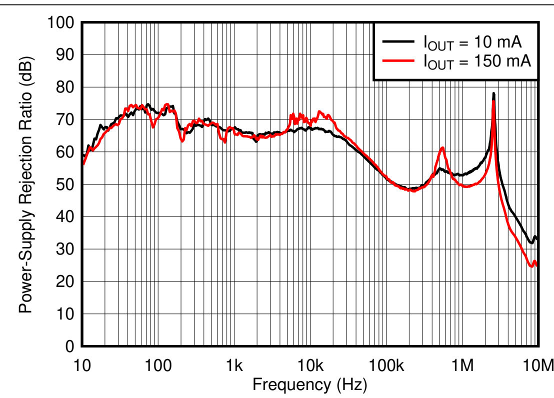


Figure 5-12. TLV70028-Q1 Power-Supply Rejection Ratio vs Frequency

5.6 Typical Characteristics (continued)

at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2V (whichever is greater), I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted); typical values are at T_J = 25°C

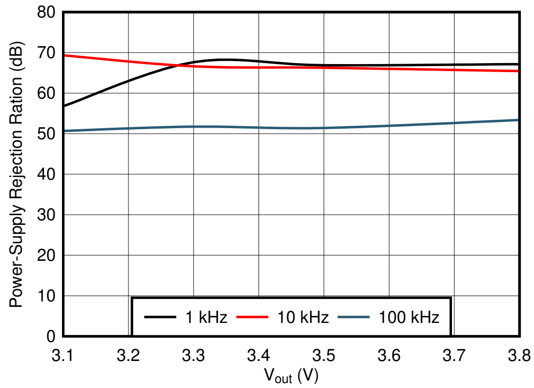


Figure 5-13. TLV70028-Q1 Power-Supply Rejection Ratio vs Output Voltage

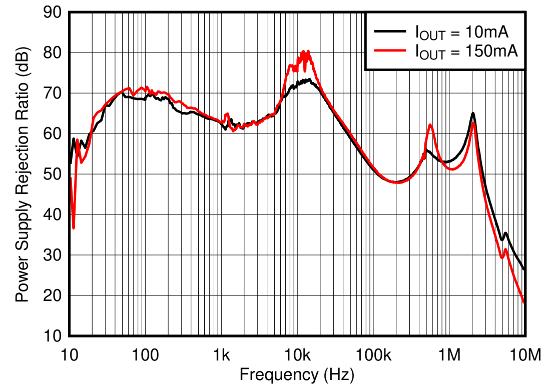


Figure 5-14. TLV70033-Q1 PSRR Ratio

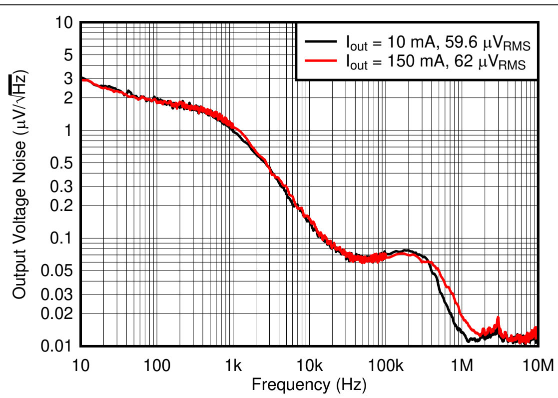
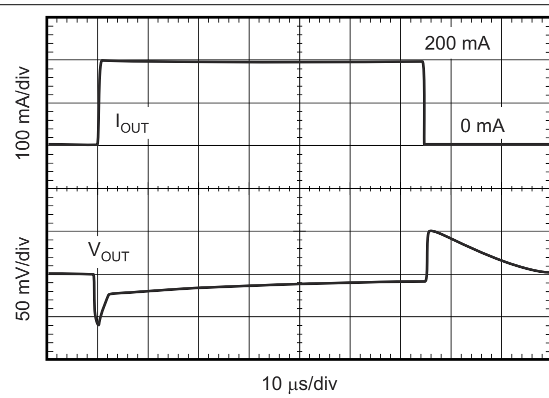
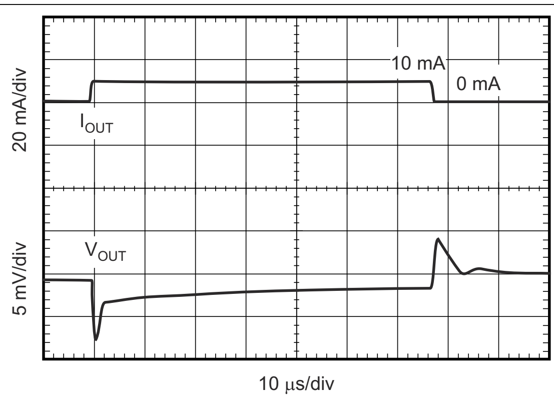


Figure 5-15. TLV70028-Q1 Output Spectral Noise Density vs Frequency



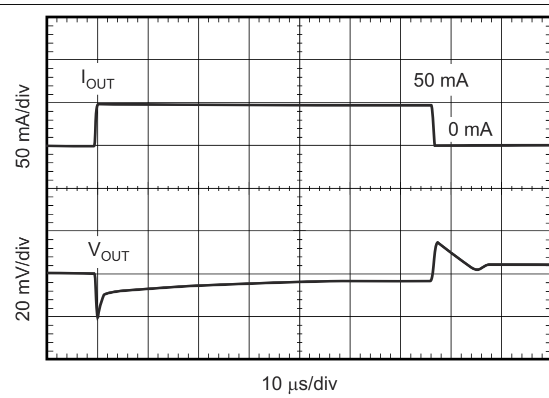
t_R = t_F = 1µs, V_{IN} = 2.1V

Figure 5-16. Load Transient Response



t_R = t_F = 1µs, V_{IN} = 2.3V

Figure 5-17. Load Transient Response

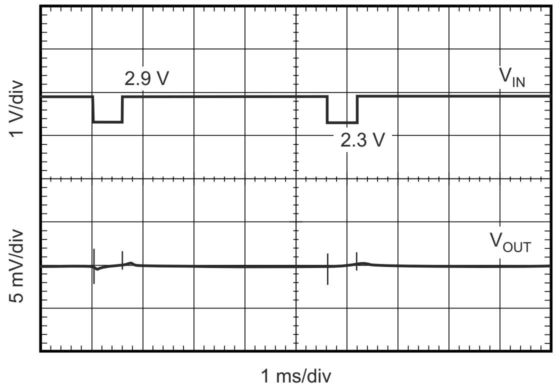


t_R = t_F = 1µs, V_{IN} = 2.3V

Figure 5-18. Load Transient Response

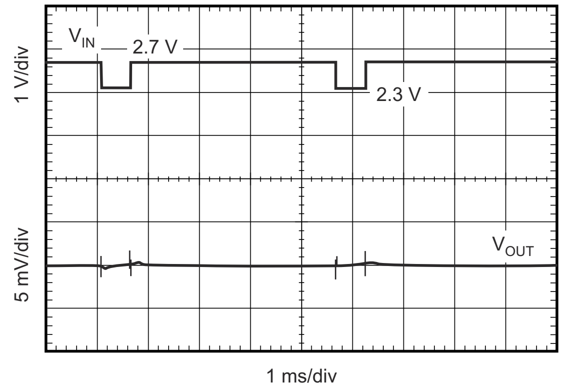
5.6 Typical Characteristics (continued)

at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2V (whichever is greater), I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted); typical values are at T_J = 25°C



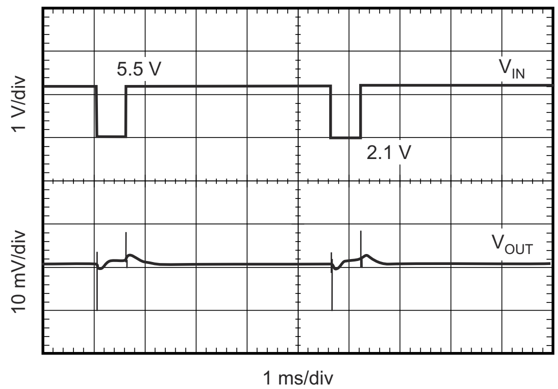
Slew rate = 1V/µs, I_{OUT} = 200mA

Figure 5-19. Line Transient Response



Slew rate = 1V/µs, I_{OUT} = 200mA

Figure 5-20. Line Transient Response



Slew rate = 1V/µs, I_{OUT} = 200mA

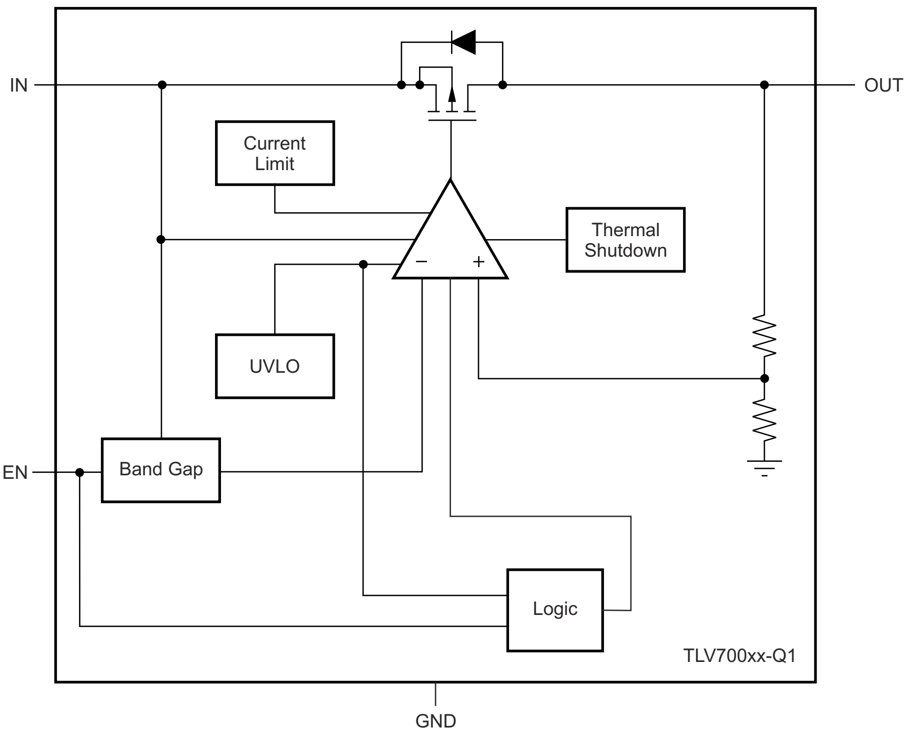
Figure 5-21. Line Transient Response

6 Detailed Description

6.1 Overview

The TLV700xx-Q1 low-dropout (LDO) linear regulators are low-quiescent-current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision band-gap and error amplifier provides overall 2% accuracy together with low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Internal Current Limit

The TLV700xx-Q1 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device turns off. When the TLV700xx-Q1 cools down, the device is turned on by the internal thermal-shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the *Thermal Protection* section for more details.

The PMOS pass transistor in the TLV700xx-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

6.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage transistor-transistor logic, complementary metal oxide semiconductor (TTL-CMOS) levels. When shutdown capability is not required, EN can be connected to the IN pin.

6.3.3 Dropout Voltage

The TLV700xx-Q1 uses a PMOS pass transistor to achieve low dropout. When $(V_{IN} – V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $r_{DS(on)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded when (V_{IN} – V_{OUT}) approaches dropout. This effect is illustrated in Figure 5-13 in the *Typical Characteristics* section.

6.3.4 Undervoltage Lockout (UVLO)

The TLV700xx-Q1 uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

6.4 Device Functional Modes

6.4.1 Operation with V_{IN} Less Than 2V

The TLV700xx-Q1 family of devices operates with input voltages above 2V. The typical UVLO voltage is 1.9V and the device operates at an input voltage above 2V. When the input voltage falls below the UVLO voltage, the device is shutdown.

6.4.2 Operation with V_{IN} Greater Than 2V

When V_{IN} is greater than 2V, if the input voltage is higher than the desired output voltage plus dropout voltage, the output voltage is equal to the desired value. Otherwise, the output voltage is V_{IN} minus the dropout voltage.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV700xx-Q1 devices belong to a family of next-generation-value LDO regulators. The devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise snd very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this device family designed for for RF portable applications. This family of regulators offers sub-band-gap output voltages down to 0.7V, current limit, and thermal protection, and is specified from –40°C to +125°C.

7.1.1 Input and Output Capacitor Requirements

Ceramic, 1.0µF, X5R- and X7R-type capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV700xx-Q1 devices are designed to be stable with an effective capacitance of 0.1µF or larger at the output. Thus, these devices are stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1µF. This effective capacitance refers to the capacitance under the operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 0.1µF effective capacitances also enables the use of smaller-footprint capacitors that have higher derating in size- and space-constrained applications.

Note that using a 0.1µF rated capacitor at the output of the LDO does not provide stability because the effective capacitance under the specified operating conditions is less than 0.1µF. Maximum ESR must be less than 200mΩ.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1µF to 1µF, low-ESR capacitor across the IN pin and the GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2Ω, a 0.1µF input capacitor may be necessary to provide stability.

7.1.2 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

7.1.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C (maximum). To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest-expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV700xx-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TLV700xx-Q1 into thermal shutdown degrades device reliability.

7.2 Typical Application

The TLV700xx-Q1 devices are 200mA, low quiescent current, low-noise, high-PSRR, fast start-up LDO linear regulators with excellent line and load transient response. The *TLV700xxEVM-503* user's guideevaluation module (EVM) helps designers evaluate the operation and performance of the TLV700xx-Q1 family.

Figure 7-1 shows a typical application for the TLV700xx-Q1 device.

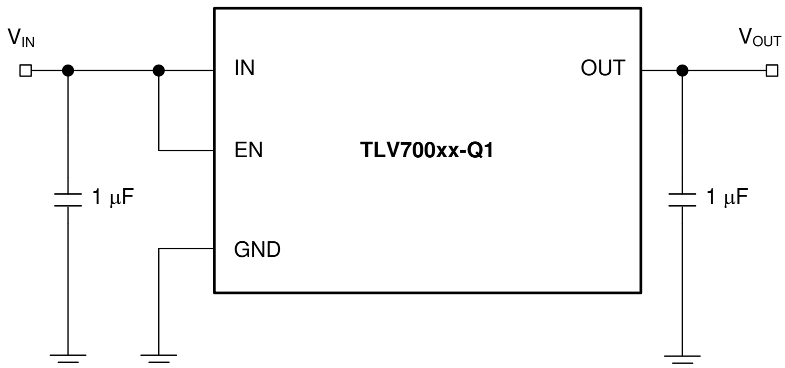


Figure 7-1. TLV700xx-Q1 Typical Application

7.2.1 Design Requirements

Table 7-1 shows example design parameters and values for this typical application.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input voltage range	2V to 5.5V
Output voltage	2.2V, 2.8V, 3.2V
Output current rating	200mA
Effective output capacitor range	> 0.1µF
Maximum output capacitor ESR range	< 200mΩ

7.2.2 Detailed Design Procedure

7.2.2.1 Input Capacitance

Although not required for stability, connecting a 0.1µF to 1µF low-ESR capacitor across the IN pin and GND pin the regulator is good analog design practice.

7.2.2.2 Output Capacitance

Effect capacitance of 0.1µF or larger is required to provide stable operation. The maximum ESR must be less than 200mΩ.

7.2.2.3 Thermal Calculation

Equation 1 shows the thermal calculation.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_Q \times V_{IN} \quad (1)$$

where:

- P_D = Continuous power dissipation
- I_{OUT} = Output current
- V_{IN} = Input voltage
- V_{OUT} = Output voltage
- Because I_Q << I_{OUT}, the term $I_Q \times V_{IN}$ is always ignored

For a device under operation at a given ambient air temperature (T_A), use Equation 2 to calculate the junction temperature (T_J).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (2)$$

where:

- $Z_{\theta JA}$ = Junction-to-ambient air thermal impedance

Use Equation 3 to calculate the rise in junction temperature because of power dissipation.

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (3)$$

For a given maximum junction temperature (T_{Jmax}), use Equation 4 to calculate the maximum ambient air temperature (T_{Amax}) at which the device can operate.

$$T_{Amax} = T_{Jmax} - (R_{\theta JA} \times P_D) \quad (4)$$

7.2.3 Application Curve

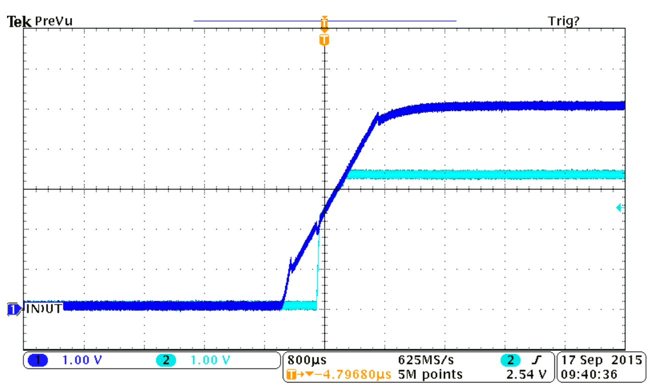


Figure 7-2. Power-Up

7.3 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 2V and 5.5V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B69xx-Q1 device, a capacitor with a value of 0.1µF and a ceramic bypass capacitor are recommended to be added at the input.

7.4 Layout

7.4.1 Layout Guidelines

When laying out the board for the TLV700xx-Q1, the board is recommended to be designed with separate ground planes for V_{IN} and V_{OUT} that are only connected at the GND pin of the device, as shown in Figure 7-3. Also, the ground connection for the bypass capacitor must be connected directly to the GND pin of the device. Improve the PSRR performance of the TLV700xx-Q1 by following these layout guidelines.

7.4.2 Board Layout Recommendations to Improve PSRR and Noise Performance

Place input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), the board is recommended to be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, connect the ground connection for the output capacitor directly to the GND pin of the device. High-ESR capacitors can degrade PSRR performance.

7.4.3 Layout Example

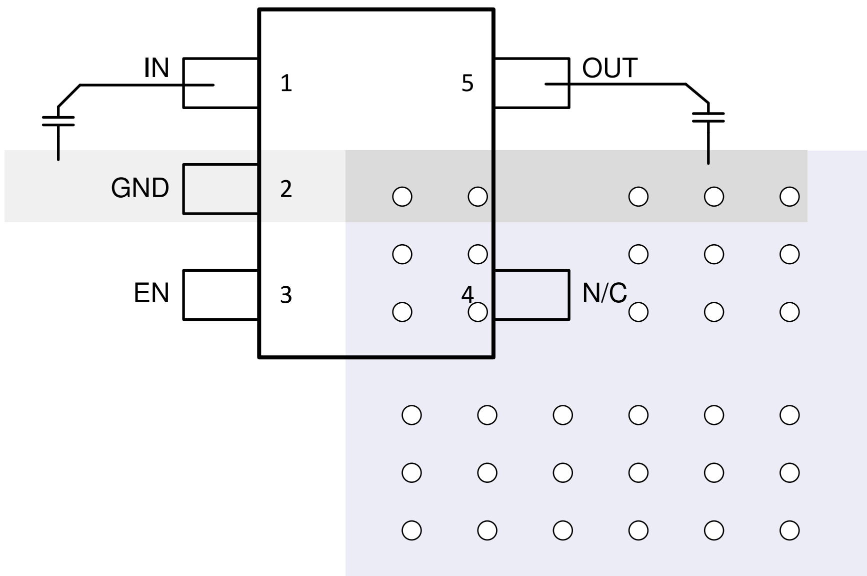


Figure 7-3. TLV700xx-Q1 Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT(1)	DESCRIPTION
TLV700**xxQyyyzQ1**	**xx** is the nominal output voltage (for example, 28 = 2.8V). **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **yyy** is the package designator. **z** is the tape and reel quantity (R = 3000, T = 250). **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TLV700xxEVM-503* user's guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision C (June 2018) to Revision D (January 2025) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Added *Device Nomenclature* table.. 16

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70025QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVC	Samples
TLV70028QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJU	Samples
TLV70032QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKA	Samples
TLV70033QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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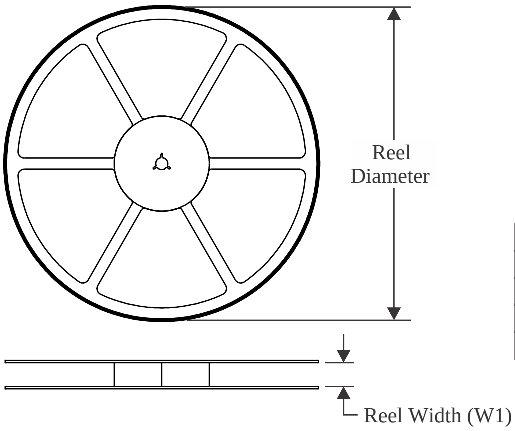
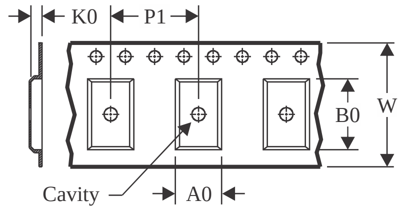
TAPE AND REEL INFORMATION

REEL DIMENSIONS

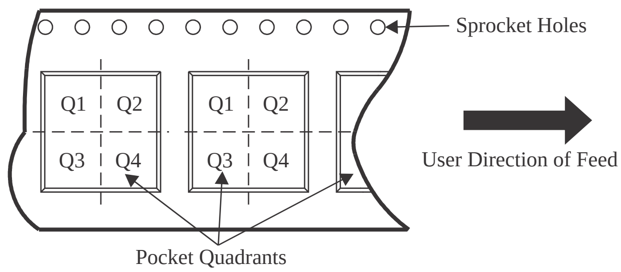


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

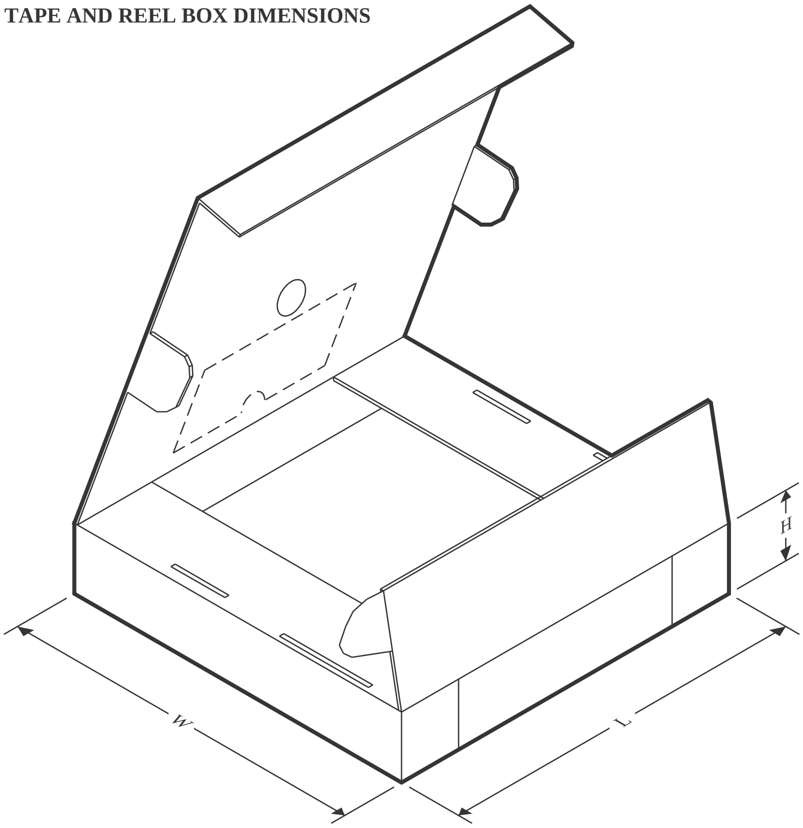
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

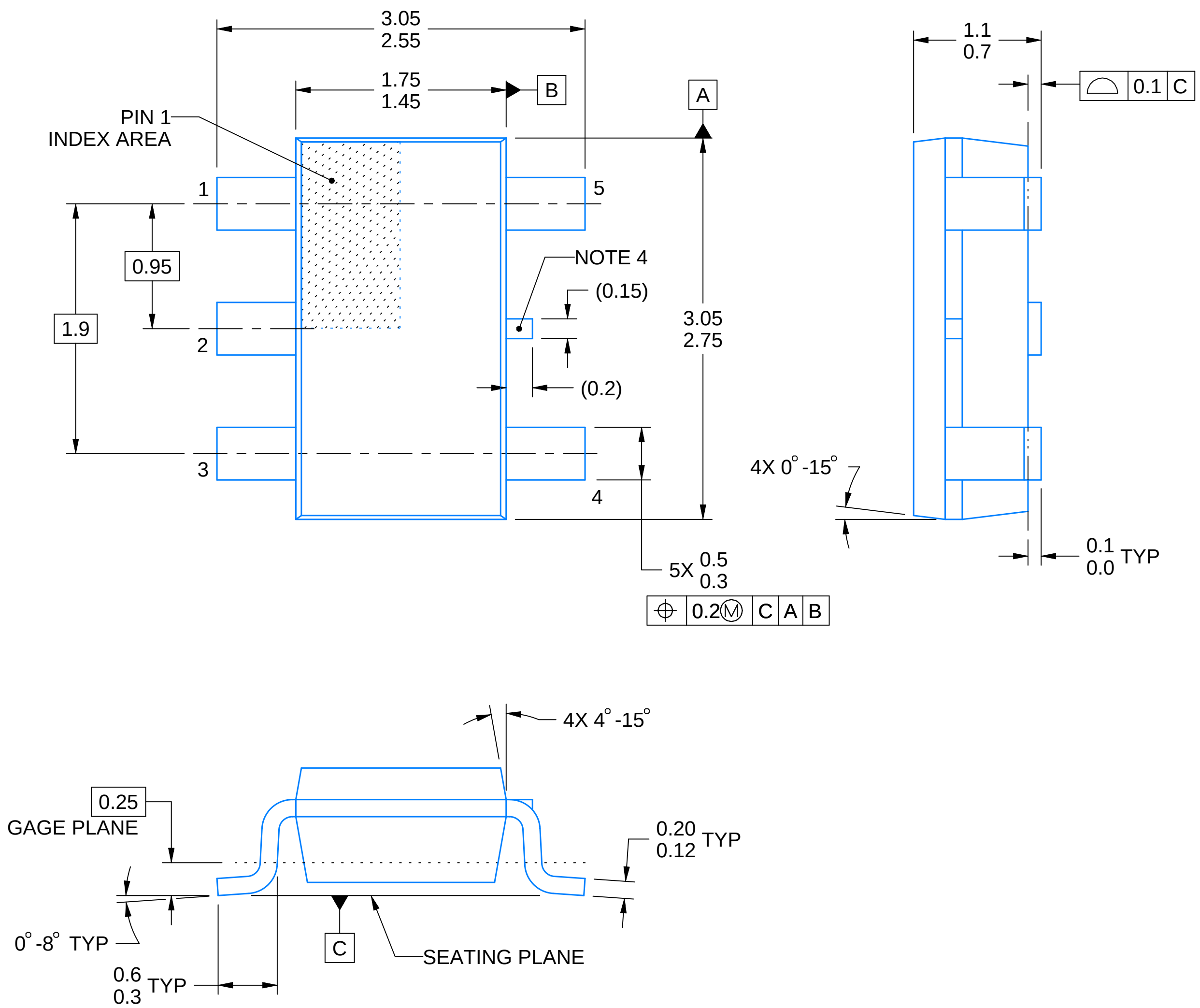
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70025QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70028QDDCRQ1	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70032QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70033QDDCRQ1	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70025QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TLV70028QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TLV70032QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TLV70033QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0



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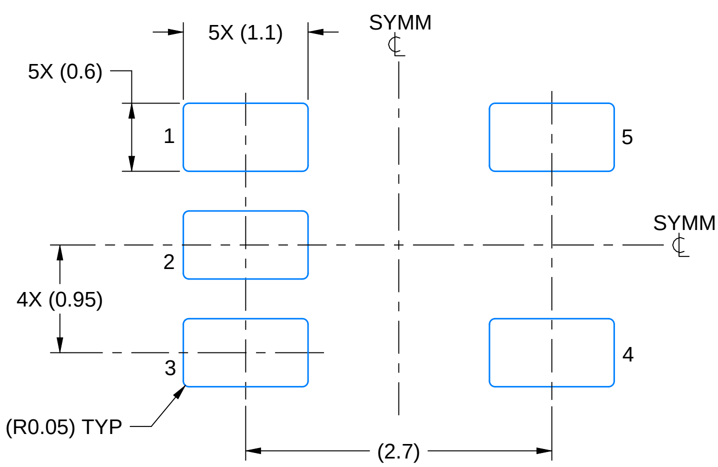
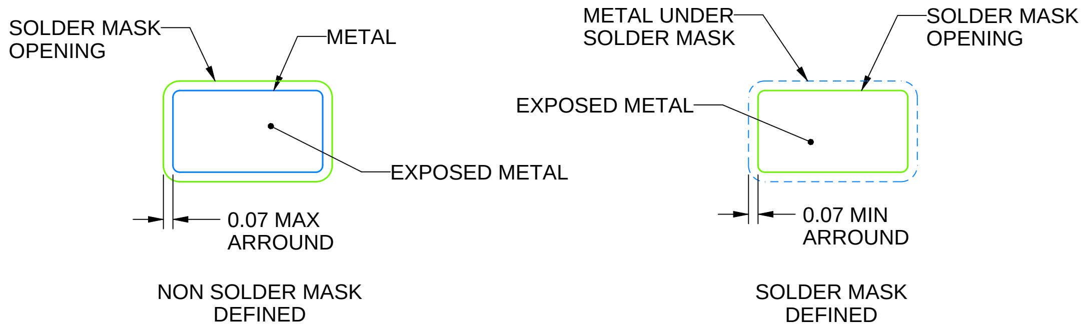
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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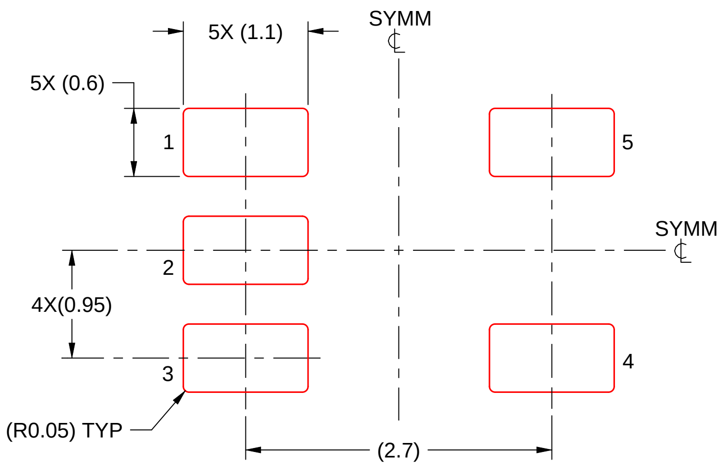
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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