TLV703 300-mA, Low-I_Q, Low-Dropout Regulator

1 Features

- Very Low Dropout:
  - 37 mV at I_{OUT} = 50 mA, V_{OUT} = 2.8 V
  - 75 mV at I_{OUT} = 100 mA, V_{OUT} = 2.8 V
  - 220 mV at I_{OUT} = 300 mA, V_{OUT} = 2.8 V
- 2% Accuracy
- Low I_Q: 35 µA
- Fixed-Output Voltage Combinations Possible From 1.2 V to 4.8 V
- High PSRR: 68 dB at 1 kHz
- Stable With Effective Capacitance of 0.1 µF
- Thermal Shutdown and Overcurrent Protection
- Packages: 5-Pin SOT-23

2 Applications

- Wireless Handsets
- Smart Phones
- ZigBee® Networks
- *Bluetooth*® Devices
- Li-Ion Battery-Operated Handheld Products
- WLAN and Other PC Add-on Cards

3 Description

The TLV703 series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision band-gap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low-dropout voltage make this series of devices ideal for a wide selection of battery-operated handheld equipment. All device versions have thermal shutdown and current limit for safety.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 µF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

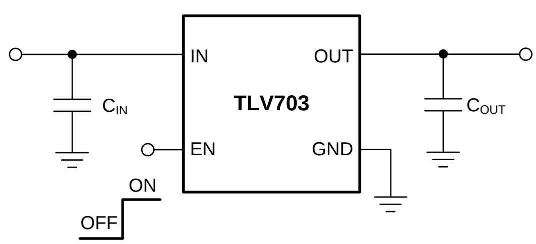
The TLV703 series of LDO linear regulators are available in a 5-pin SOT-23 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV703	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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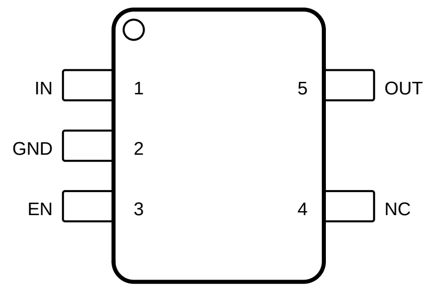
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2017	*	Initial release.

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Input pin. A small, 1-µF ceramic capacitor is recommended from this pin to ground to assure stability and good transient performance. See the *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
2	GND	—	Ground pin
3	EN	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode and reduces operating current to 1 µA, nominal.
4	NC	—	No connection. This pin can be tied to ground to improve thermal dissipation.
5	OUT	O	Regulated output voltage pin. A small, 1-µF ceramic capacitor is needed from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	IN, EN, OUT	–0.3	6	V
Current (source)	OUT	Internally limited		
Output short-circuit duration		Indefinite		
Total continuous power dissipation		See *Thermal Information*		
Temperature	Operating virtual junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2		5.5	V
V_{OUT}	Output voltage range	1.2		4.8	V
I_{OUT}	Output current	0		300	mA

6.4 Thermal Information

THERMAL METRIC(1)		TLV703 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	254.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	143.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

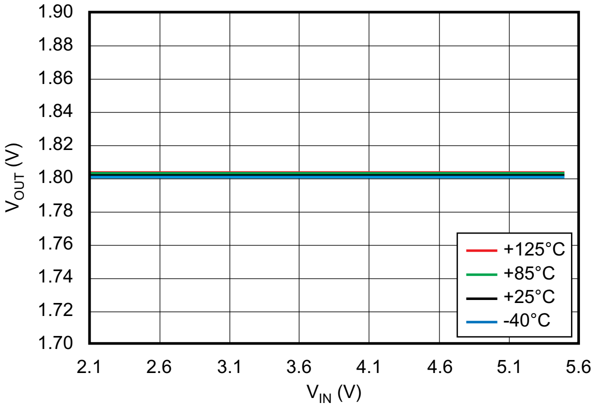
at V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1 µF, and T_J = –40°C to +125°C (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2		5.5	V
V_{OUT}	DC output accuracy	–40°C ≤ T_J ≤ 125°C	–2%	0.5%	2%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		1	5	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 300 mA		1	15	mV
V_{DO}	Dropout voltage (1)	V_{IN} = 0.98 × $V_{OUT(nom)}$, I_{OUT} = 300 mA		260	375	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$	320	500	860	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA		35	55	µA
		I_{OUT} = 300 mA, V_{IN} = V_{OUT} + 0.5 V		370		
I_{SHDN}	Ground pin current (shutdown)	V_{EN} ≤ 0.4 V, V_{IN} = 2 V		400		nA
		V_{EN} ≤ 0.4 V, 2 V ≤ V_{IN} ≤ 4.5 V, T_J = –40°C to +85°C		1	2	µA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, f = 1 kHz		68		dB
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA		48		μV_{RMS}
t_{STR}	Start-up time (2)	C_{OUT} = 1 µF, I_{OUT} = 300 mA		100		µs
$V_{EN(high)}$	Enable pin high (enabled)		0.9		V_{IN}	V
$V_{EN(low)}$	Enable pin low (disabled)		0		0.4	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 5.5 V		0.04		µA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		145		
T_J	Operating junction temperature		–40		125	°C

(1) V_{DO} is measured for devices with $V_{OUT(nom)}$ ≥ 2.35 V.
(2) Start-up time = time from EN assertion to 0.98 × $V_{OUT(nom)}$.

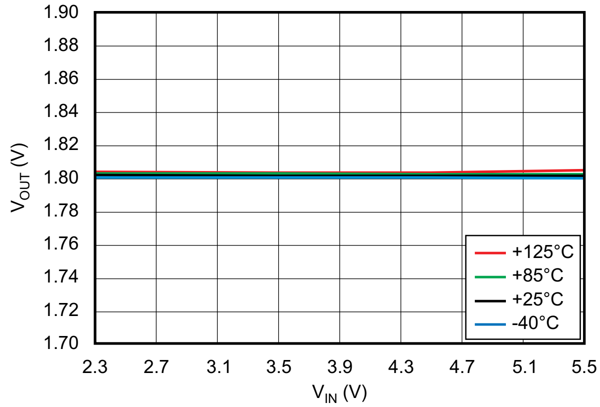
6.6 Typical Characteristics

over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater, I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



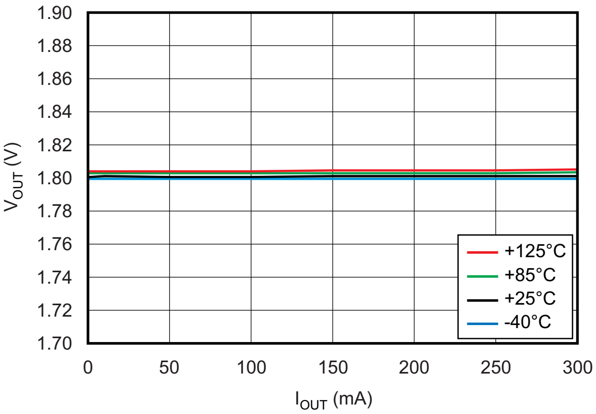
V_{OUT} = 1.8 V, I_{OUT} = 10 mA

Figure 1. Line Regulation



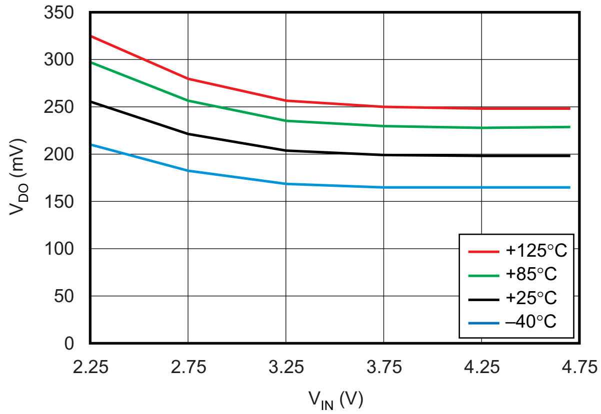
V_{OUT} = 1.8 V, I_{OUT} = 300 mA

Figure 2. Line Regulation



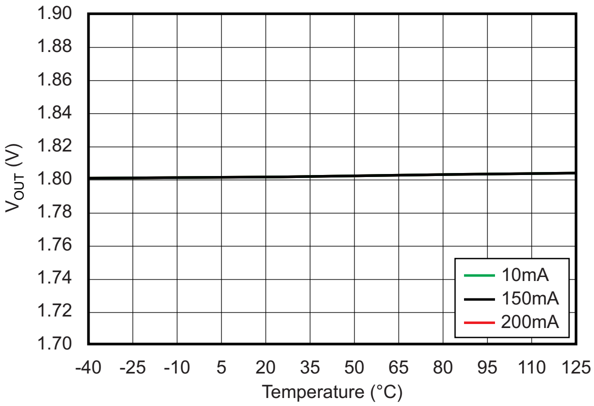
V_{OUT} = 1.8 V

Figure 3. Load Regulation



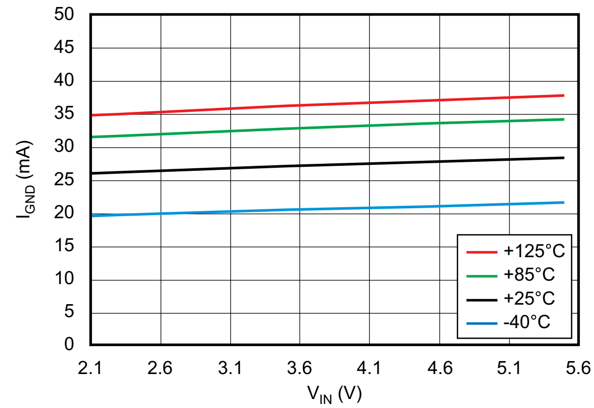
I_{OUT} = 300 mA

Figure 4. Dropout Voltage vs Input Voltage



V_{OUT} = 1.8 V

Figure 5. Output Voltage vs Temperature

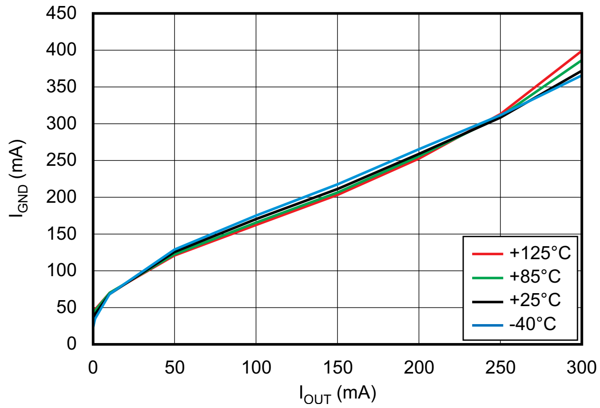


V_{OUT} = 1.8 V

Figure 6. Ground Pin Current vs Input Voltage

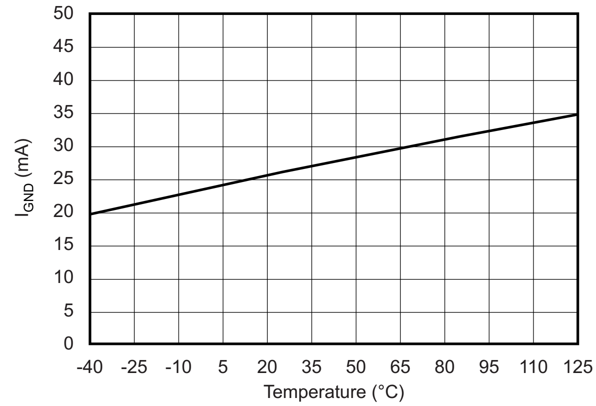
Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater, I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



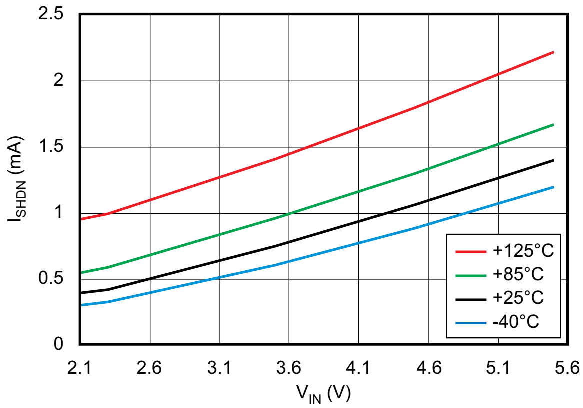
V_{OUT} = 1.8 V

Figure 7. Ground Pin Current vs Load



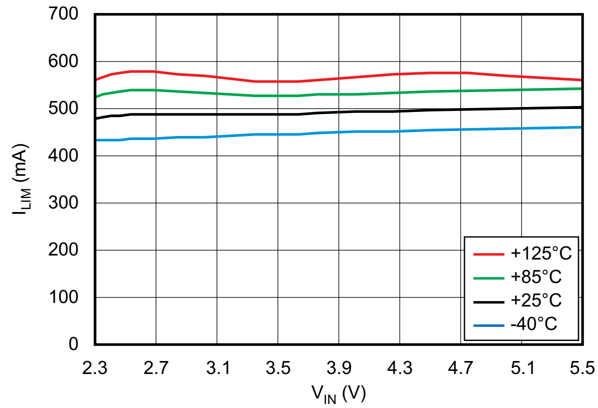
V_{OUT} = 1.8 V

Figure 8. Ground Pin Current vs Temperature



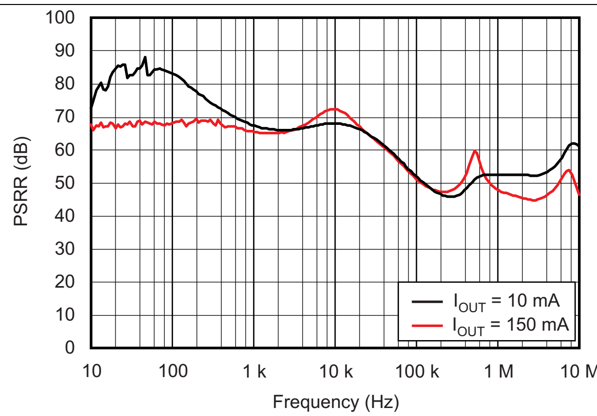
V_{OUT} = 1.8 V

Figure 9. Shutdown Current vs Input Voltage



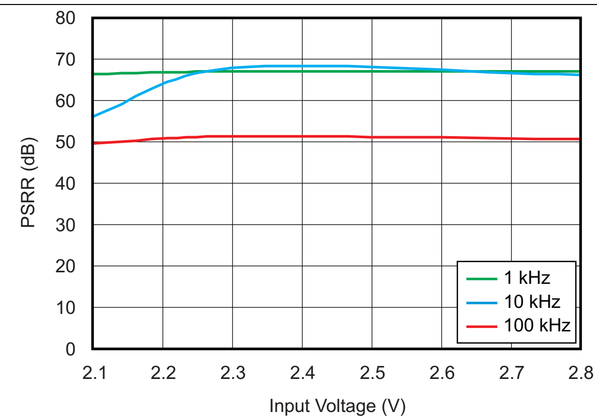
V_{OUT} = 1.8 V

Figure 10. Current Limit vs Input Voltage



V_{IN} – V_{OUT} = 0.5 V

Figure 11. Power-Supply Ripple Rejection vs Frequency

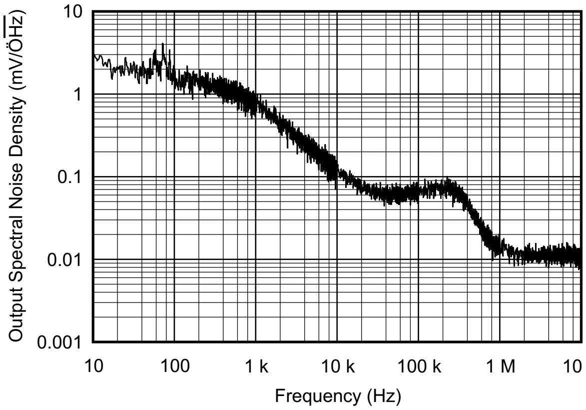


V_{OUT} = 1.8 V

Figure 12. Power-Supply Ripple Rejection vs Input Voltage

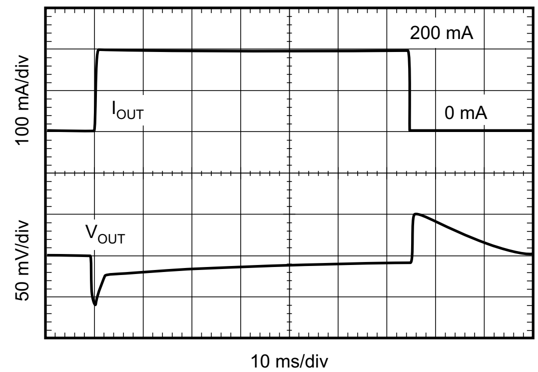
Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater, I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



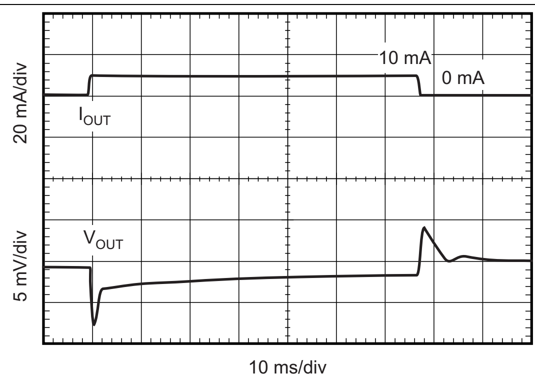
V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF

Figure 13. Output Spectral Noise Density vs Frequency



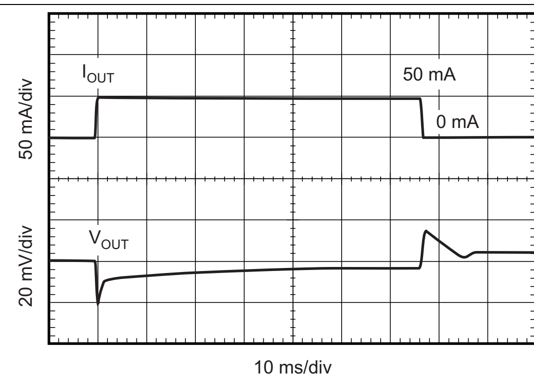
V_{OUT} = 1.8 V

Figure 14. Load Transient Response



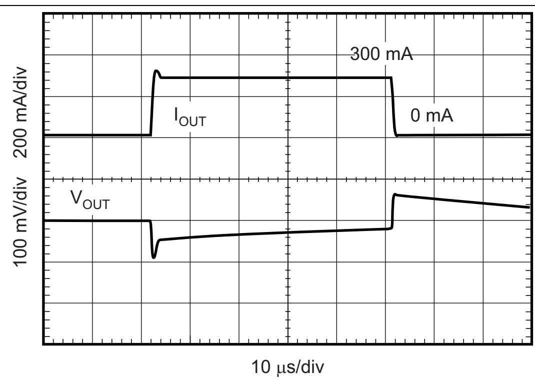
V_{OUT} = 1.8 V, t_R = t_F = 1 µs

Figure 15. Load Transient Response



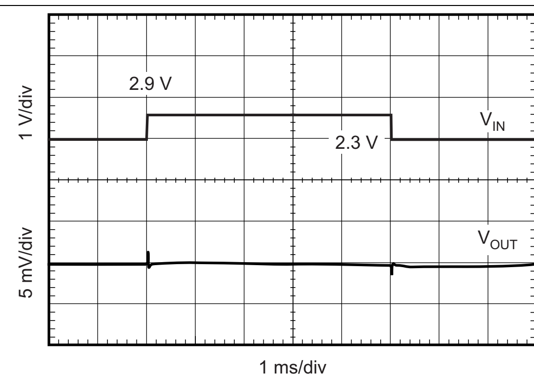
V_{OUT} = 1.8 V, t_R = t_F = 1 µs

Figure 16. Load Transient Response



V_{OUT} = 1.8 V, t_R = t_F = 1 µs

Figure 17. Load Transient Response

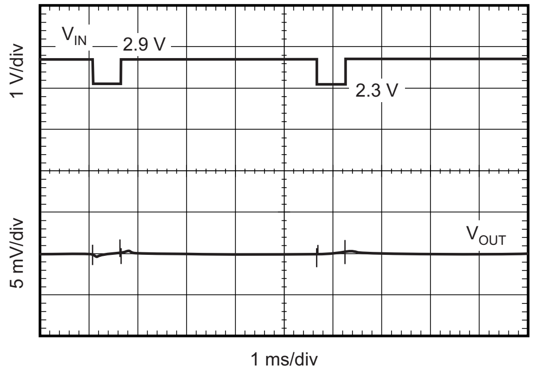


V_{OUT} = 1.8 V, I_{OUT} = 300 mA, slew rate = 1 V/µs

Figure 18. Line Transient Response

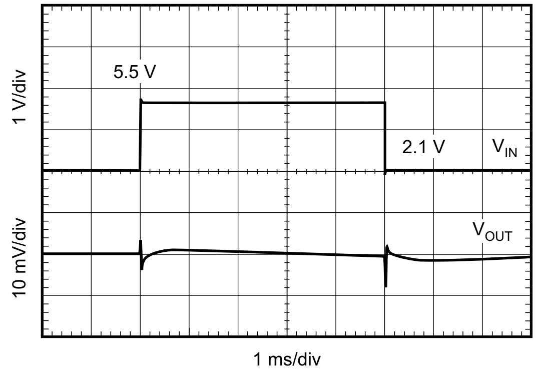
Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater, I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



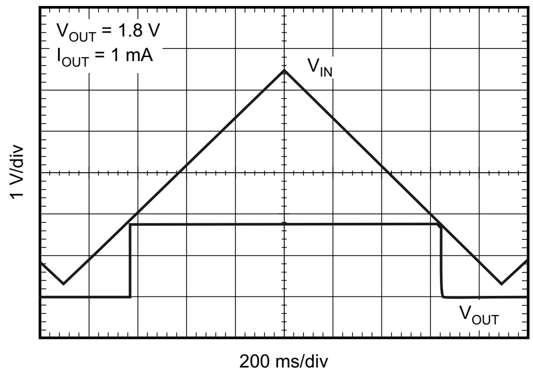
V_{OUT} = 1.8 V, I_{OUT} = 1 mA, slew rate = 1 V/µs

Figure 19. Line Transient Response



V_{OUT} = 1.8 V, I_{OUT} = 300 mA, slew rate = 1 V/µs

Figure 20. Line Transient Response



V_{OUT} = 1.8 V, I_{OUT} = 1 mA

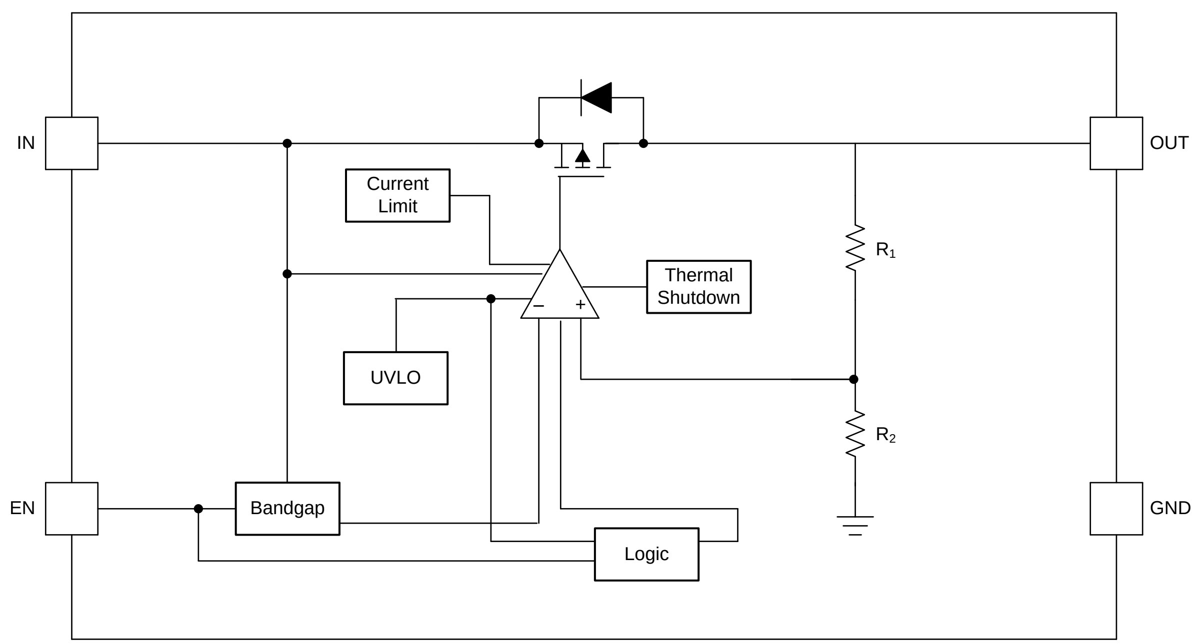
Figure 21. V_{IN} Ramp Up, Ramp Down Response

7 Detailed Description

7.1 Overview

The TLV703 series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage make this series of devices ideal for most battery-operated handheld equipment. All device versions have integrated thermal shutdown, current limit, and undervoltage lockout (UVLO).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The TLV703 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{CL} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{CL}$ until thermal shutdown is triggered and the device turns off. As the device cools, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the *Thermal Consideration* section for more details.

The PMOS pass element in the TLV703 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at the EN pin goes above 0.9 V. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

Feature Description (continued)

7.3.3 Dropout Voltage

The TLV703 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear (triode) region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device functions as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded when (V_{IN} – V_{OUT}) approaches dropout. Figure 12 illustrates this effect.

7.3.4 Undervoltage Lockout (UVLO)

The TLV703 uses a UVLO circuit to keep the output shut off until internal circuitry is operating properly.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage added to the dropout voltage
- The output current is less than the current limit
- The input voltage is greater than the UVLO voltage

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer regulates the output voltage of the LDO. Line or load transients in dropout can result in large output voltage deviations.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal mode	$V_{IN} > V_{OUT\ (nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout mode	$V_{IN} < V_{OUT\ (nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Current limit	V_{IN} > UVLO	$I_{OUT} > I_{CL}$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV703 belongs to a family of next-generation value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for portable RF applications. This family of regulators offers current limit and thermal protection, and is specified from –40°C to +125°C.

8.2 Typical Application

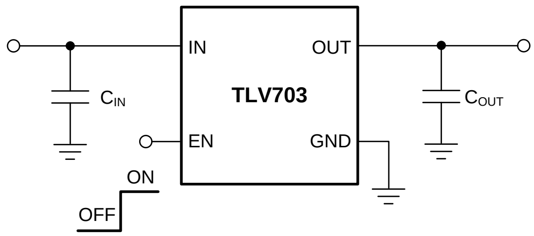


Figure 22. Typical Application Circuit

8.2.1 Design Requirements

Table 2 lists the design parameters.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	2.5 V to 3.3 V
Output voltage	1.8 V
Output current	100 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

1-µF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV703 is designed to be stable with an *effective capacitance* of 0.1 µF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. In addition to allowing the use of lower-cost dielectrics, this capability of being stable with 0.1-µF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

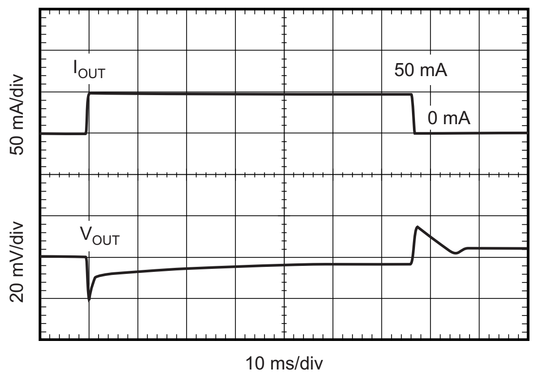
Using a 0.1-µF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions must not be less than 0.1 µF. Maximum ESR must be less than 200 mΩ.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1-µF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-µF input capacitor may be necessary to ensure stability.

8.2.2.2 Transient Response

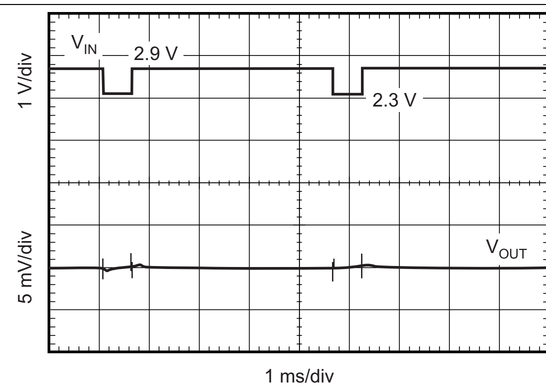
As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the duration of the transient response.

8.2.3 Application Curves



V_{OUT} = 1.8 V, t_R = t_F = 1 µs

Figure 23. Load Transient Response



V_{OUT} = 1.8 V, I_{OUT} = 1 mA, slew rate = 1 V/µs

Figure 24. Line Transient Response

9 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV703. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during start-up or load transient events.

9.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air; see the *Thermal Information* section for thermal performance on the TLV703 evaluation module (EVM). The EVM is a two-layer board with two ounces of copper per side.

Power dissipation depends on input voltage and load conditions. Equation 1 shows that power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

10 Layout

10.1 Layout Guidelines

Place input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT} with the ground plane connected only at the GND pin of the device. In addition, connect the ground connection for the output capacitor directly to the GND pin of the device. High ESR capacitors can degrade PSRR performance.

10.2 Layout Example

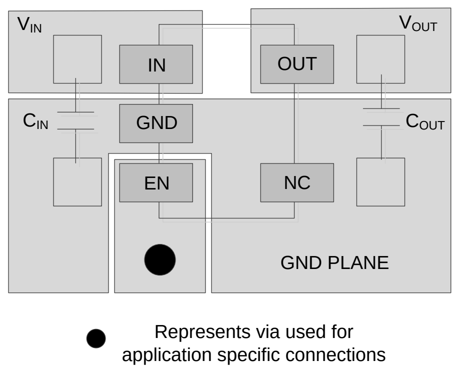


Figure 25. Example Layout

10.3 Thermal Consideration

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, thus protecting the regulator from damage resulting from overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum.

To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TLV703 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TLV703 into thermal shutdown degrades device reliability.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.2 Device Nomenclature

Table 3. Ordering Information(1)

PRODUCT	V_{OUT} (2)
TLV703**xx** ***yyyz***	**XX** is nominal output voltage (for example, 28 = 2.8 V). **YYY** is the package designator. **Z** is tape and reel quantity (R = 3000).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 1.2 V to 4.8 V in 50-mV increments are available. Contact factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Using the TLV700xxEVM-503 Evaluation Module

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG.
ZigBee is a registered trademark of the ZigBee Alliance.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70310DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1F4Q	Samples
TLV70311DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1F1Q	Samples
TLV70312DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1ECQ	Samples
TLV70313DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1G5Q	Samples
TLV70315DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1EDQ	Samples
TLV70318DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1AZE	Samples
TLV70325DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1EEQ	Samples
TLV70327DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1EXQ	Samples
TLV70328DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1B3E	Samples
TLV70329DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1EZQ	Samples
TLV70330DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1I9Q	Samples
TLV70333DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1AHQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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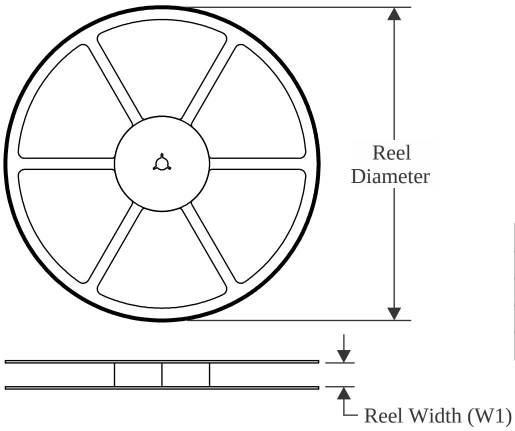
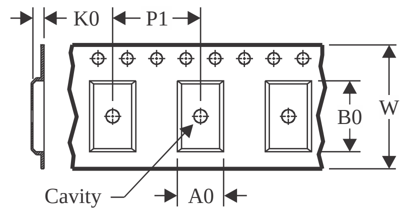
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

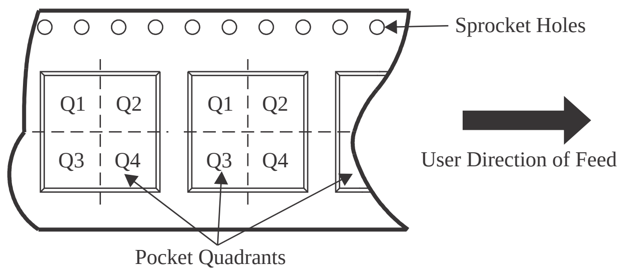


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

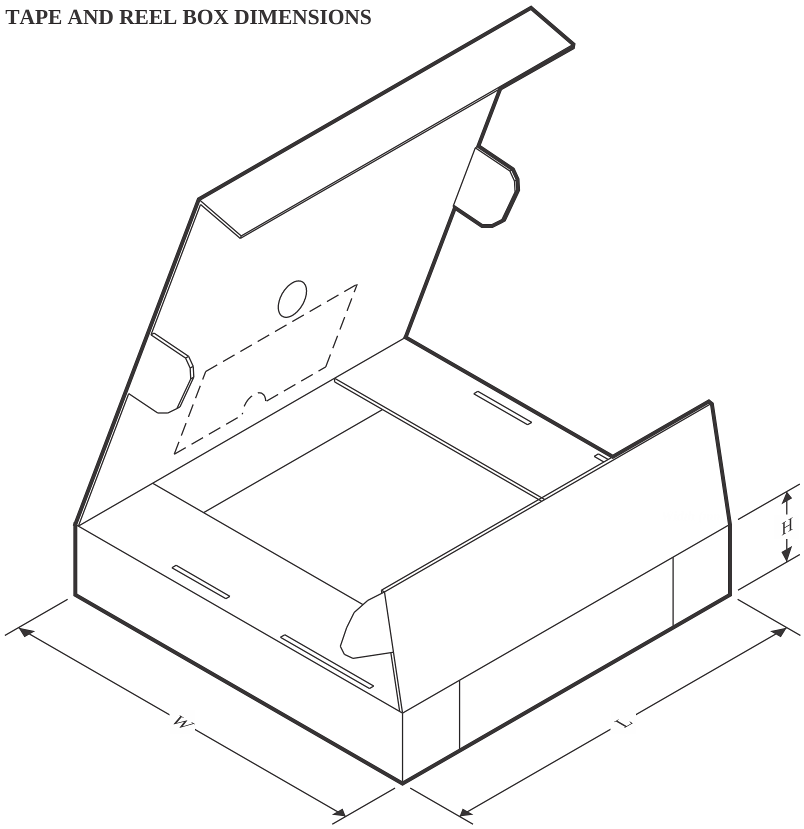
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

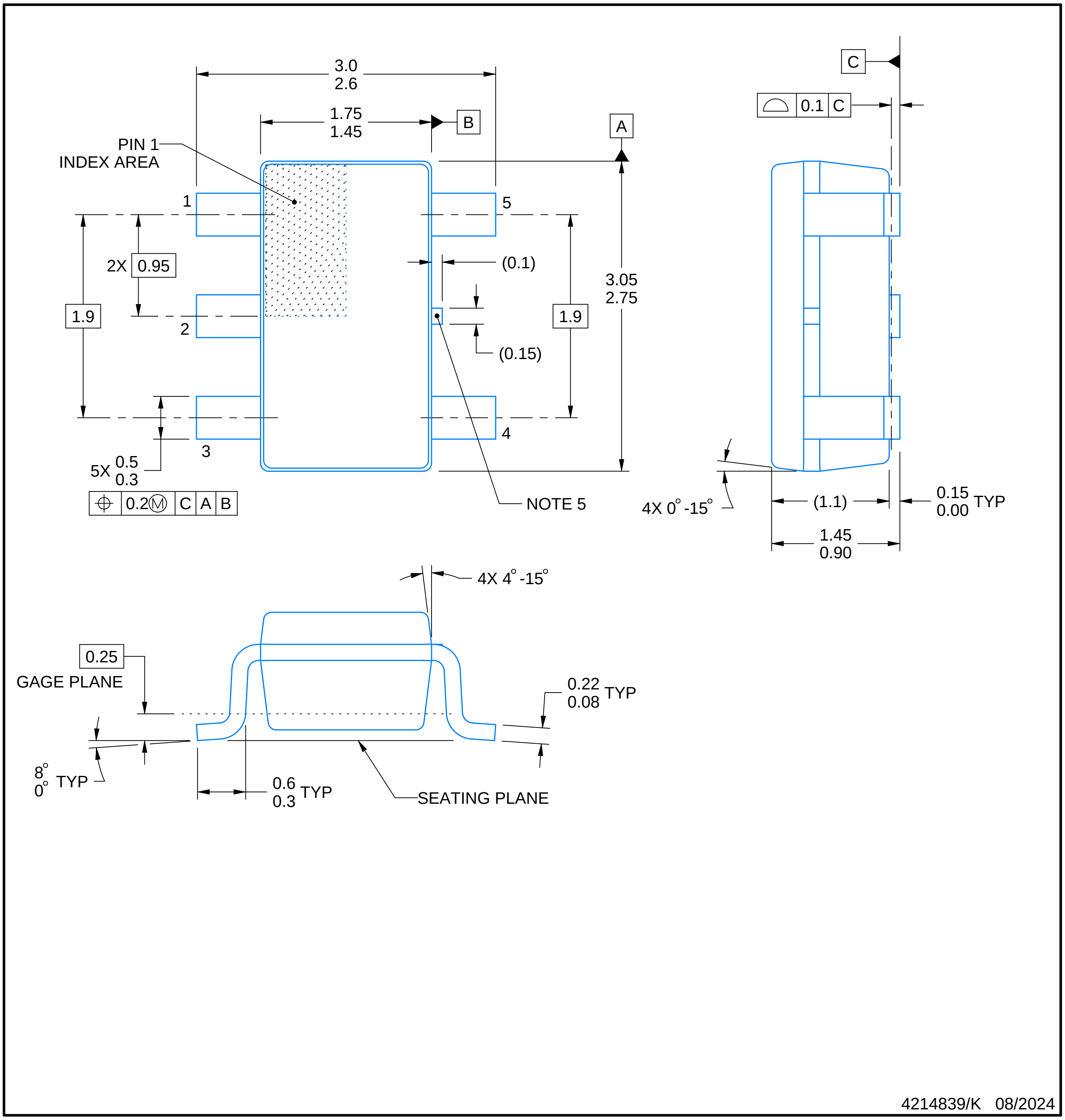
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70310DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70311DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70312DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70313DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70315DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70318DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70325DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70327DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70328DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70329DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70330DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70333DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70310DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70311DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70312DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70313DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70315DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70318DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70325DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70327DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70328DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70329DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70330DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70333DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0



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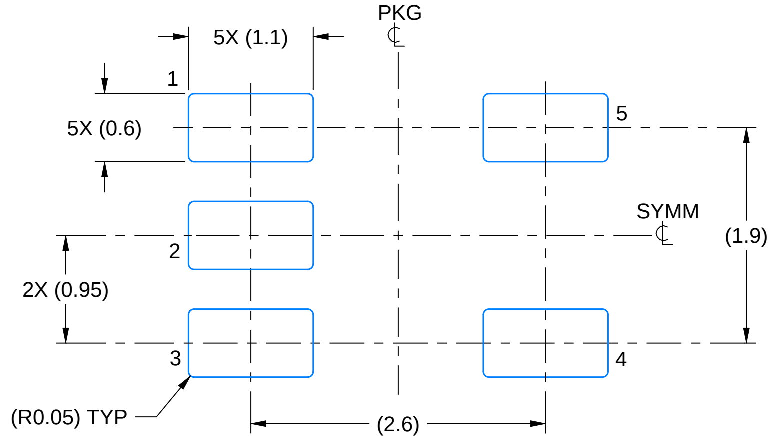
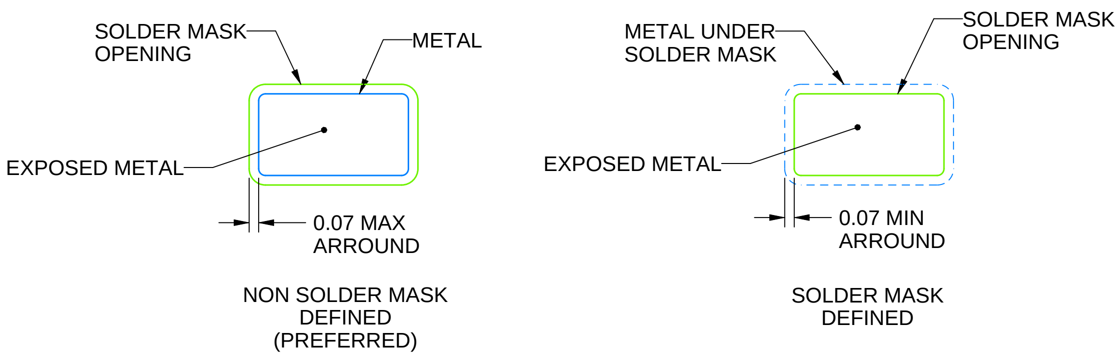
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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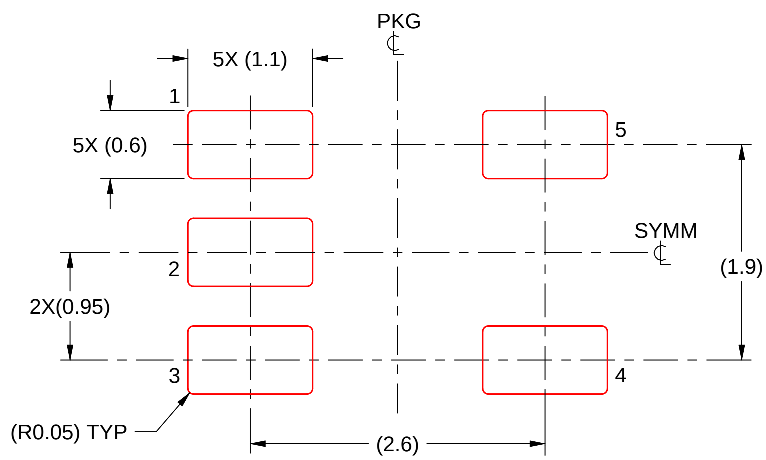
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.