

TMS320VC5402A

Fixed-Point Digital Signal Processor

Data Manual



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Literature Number: SPRS015F
September 2001 – Revised October 2008

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data sheet revision history highlights the technical changes made to the SPRS015E device-specific data sheet to make it an SPRS015F revision.

Scope: This document has been reviewed for technical accuracy; the technical content is up-to-date as of the specified release date with the following corrections.

| ADDITIONS/CHANGES/DELETIONS |
|--|
| <p>Table 2-2, Signal Descriptions:</p> <ul style="list-style-type: none">• Updated DESCRIPTION of $\overline{\text{TRST}}$• Added footnote about $\overline{\text{TRST}}$ |

Contents

| | |
|--|---------------------------|
| Revision History | 2 |
| 1 TMS320VC5402A DSP | 9 |
| 1.1 Features | 9 |
| 2 Introduction | 10 |
| 2.1 Description | 10 |
| 2.2 Pin Assignments | 10 |
| 2.2.1 Terminal Assignments for the GGU Package | 11 |
| 2.2.2 Pin Assignments for the PGE Package | 12 |
| 2.3 Signal Descriptions | 13 |
| 3 Functional Overview | 17 |
| 3.1 Memory | 17 |
| 3.1.1 Data Memory | 17 |
| 3.1.2 Program Memory | 18 |
| 3.1.3 Extended Program Memory | 18 |
| 3.2 On-Chip ROM With Bootloader | 18 |
| 3.3 On-Chip RAM | 19 |
| 3.4 On-Chip Memory Security | 19 |
| 3.5 Memory Map | 20 |
| 3.5.1 Relocatable Interrupt Vector Table | 21 |
| 3.6 On-Chip Peripherals | 23 |
| 3.6.1 Software-Programmable Wait-State Generator | 23 |
| 3.6.2 Programmable Bank-Switching | 25 |
| 3.6.3 Bus Holders | 26 |
| 3.7 Parallel I/O Ports | 27 |
| 3.7.1 Enhanced 8-/16-Bit Host-Port Interface (HPI8/16) | 27 |
| 3.7.2 HPI Nonmultiplexed Mode | 28 |
| 3.8 Multichannel Buffered Serial Ports (McBSPs) | 29 |
| 3.9 Hardware Timer | 32 |
| 3.10 Clock Generator | 32 |
| 3.11 Enhanced External Parallel Interface (XIO2) | 33 |
| 3.12 DMA Controller | 37 |
| 3.12.1 Features | 37 |
| 3.12.2 DMA External Access | 37 |
| 3.12.3 DMPREC Issue | 39 |
| 3.12.4 DMA Memory Map | 40 |
| 3.12.5 DMA Priority Level | 41 |
| 3.12.6 DMA Source/Destination Address Modification | 41 |
| 3.12.7 DMA in Autoinitialization Mode | 42 |
| 3.12.8 DMA Transfer Counting | 42 |
| 3.12.9 DMA Transfer in Doubleword Mode | 42 |
| 3.12.10 DMA Channel Index Registers | 43 |
| 3.12.11 DMA Interrupts | 43 |
| 3.12.12 DMA Controller Synchronization Events | 44 |
| 3.13 General-Purpose I/O Pins | 45 |
| 3.13.1 McBSP Pins as General-Purpose I/O | 45 |
| 3.13.2 HPI Data Pins as General-Purpose I/O | 45 |
| 3.14 Memory-Mapped Registers | 46 |
| 3.15 McBSP Control Registers and Subaddresses | 48 |
| 3.16 DMA Subbank Addressed Registers | 49 |

| | | |
|----------|--|-----------|
| 3.17 | Interrupts | 51 |
| 4 | Support | 52 |
| 4.1 | Documentation Support | 52 |
| 4.2 | Device and Development-Support Tool Nomenclature..... | 53 |
| 5 | Specification | 54 |
| 5.1 | Absolute Maximum Ratings | 54 |
| 5.2 | Recommended Operating Conditions | 54 |
| 5.3 | Electrical Characteristics Over Recommended Operating Case Temperature Range (Unless Otherwise Noted) | 55 |
| 5.3.1 | Test Load Circuit | 55 |
| 5.3.2 | Timing Parameter Symbology | 56 |
| 5.3.3 | Internal Oscillator With External Crystal..... | 57 |
| 5.3.4 | Clock Options | 58 |
| 5.3.4.1 | Divide-By-Two and Divide-By-Four Clock Options | 58 |
| 5.3.4.2 | Multiply-By-N Clock Option (PLL Enabled)..... | 60 |
| 5.3.5 | Memory and Parallel I/O Interface Timing | 61 |
| 5.3.5.1 | Memory Read | 61 |
| 5.3.5.2 | Memory Write | 64 |
| 5.3.5.3 | I/O Read | 65 |
| 5.3.5.4 | I/O Write | 67 |
| 5.3.6 | Ready Timing for Externally Generated Wait States | 68 |
| 5.3.7 | HOLD and HOLDA Timings..... | 71 |
| 5.3.8 | Reset, $\overline{\text{BIO}}$, Interrupt, and $\overline{\text{MP/MC}}$ Timings..... | 72 |
| 5.3.9 | Instruction Acquisition ($\overline{\text{IAQ}}$) and Interrupt Acknowledge ($\overline{\text{IACK}}$) Timings | 74 |
| 5.3.10 | External Flag (XF) and TOUT Timings | 75 |
| 5.3.11 | Multichannel Buffered Serial Port (McBSP) Timing..... | 76 |
| 5.3.11.1 | McBSP Transmit and Receive Timings | 76 |
| 5.3.11.2 | McBSP General-Purpose I/O Timing | 79 |
| 5.3.11.3 | McBSP as SPI Master or Slave Timing | 80 |
| 5.3.12 | Host-Port Interface Timing | 84 |
| 5.3.12.1 | HPI8 Mode | 84 |
| 5.3.12.2 | HPI16 Mode..... | 88 |
| 6 | Mechanical Data | 91 |
| 6.1 | Package Thermal Resistance Characteristics..... | 91 |

List of Figures

| | | |
|------|---|--------------------|
| 2-1 | 144-Ball GGU MicroStar BGA™ (Bottom View) | 10 |
| 2-2 | 144-Pin PGE Low-Profile Quad Flatpack (Top View) | 12 |
| 3-1 | TMS320VC5402A Functional Block Diagram | 17 |
| 3-2 | Program and Data Memory Map | 20 |
| 3-3 | Extended Program Memory Map | 21 |
| 3-4 | Processor Mode Status Register (PMST) | 21 |
| 3-5 | Software Wait-State Register (SWWSR) [Memory-Mapped Register (MMR) Address 0028h]..... | 23 |
| 3-6 | Software Wait-State Control Register (SWCR) [MMR Address 002Bh] | 24 |
| 3-7 | Bank-Switching Control Register (BSCR) [MMR Address 0029h]..... | 25 |
| 3-8 | Host-Port Interface — Nonmultiplexed Mode | 28 |
| 3-9 | HPI Memory Map | 29 |
| 3-10 | Pin Control Register (PCR) | 30 |
| 3-11 | Multichannel Control Register 1x (MCR1x) | 31 |
| 3-12 | Multichannel Control Register 2x (MCR2x) | 31 |
| 3-13 | Receive Channel Enable Registers Bit Layout for Partitions A to H | 31 |
| 3-14 | Transmit Channel Enable Registers Bit Layout for Partitions A to H..... | 32 |
| 3-15 | Nonconsecutive Memory Read and I/O Read Bus Sequence | 34 |
| 3-16 | Consecutive Memory Read Bus Sequence (n = 3 reads) | 35 |
| 3-17 | Memory Write and I/O Write Bus Sequence..... | 36 |
| 3-18 | Transfer Mode Control Register (DMMCRn) | 38 |
| 3-19 | DMA Channel Enable Control Register (DMCECTL)..... | 39 |
| 3-20 | On-Chip DMA Memory Map for Program Space (DLAXS = 0 and SLAXS = 0) | 40 |
| 3-21 | On-Chip DMA Memory Map for Data and IO Space (DLAXS = 0 and SLAXS = 0)..... | 41 |
| 3-22 | DMPREC Register | 42 |
| 3-23 | General-Purpose I/O Control Register (GPIOCR) [MMR Address 003Ch]..... | 45 |
| 3-24 | General-Purpose I/O Status Register (GPIOSR) [MMR Address 003Dh] | 45 |
| 3-25 | IFR and IMR | 51 |
| 5-1 | Tester Pin Electronics | 55 |
| 5-2 | Internal Divide-By-Two Clock Option With External Crystal..... | 57 |
| 5-3 | External Divide-By-Two Clock Timing | 59 |
| 5-4 | Multiply-By-One Clock Timing | 60 |
| 5-5 | Nonconsecutive Mode Memory Reads..... | 62 |
| 5-6 | Consecutive Mode Memory Reads | 63 |
| 5-7 | Memory Write ($\overline{MSTRB} = 0$) | 64 |
| 5-8 | Parallel I/O Port Read ($\overline{IOSTRB} = 0$) | 66 |
| 5-9 | Parallel I/O Port Write ($\overline{IOSTRB} = 0$) | 67 |
| 5-10 | Memory Read With Externally Generated Wait States..... | 68 |
| 5-11 | Memory Write With Externally Generated Wait States..... | 69 |
| 5-12 | I/O Read With Externally Generated Wait States..... | 69 |

TMS320VC5402A

Fixed-Point Digital Signal Processor

| | | |
|------|--|--------------------|
| 5-13 | I/O Write With Externally Generated Wait States | 70 |
| 5-14 | $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timings (HM = 1) | 71 |
| 5-15 | Reset and $\overline{\text{BIO}}$ Timings | 72 |
| 5-16 | Interrupt Timing | 73 |
| 5-17 | MP/ $\overline{\text{MC}}$ Timing | 73 |
| 5-18 | Instruction Acquisition ($\overline{\text{IAQ}}$) and Interrupt Acknowledge ($\overline{\text{IACK}}$) Timings | 74 |
| 5-19 | External Flag (XF) Timing | 75 |
| 5-20 | TOUT Timing | 75 |
| 5-21 | McBSP Receive Timings | 77 |
| 5-22 | McBSP Transmit Timings | 78 |
| 5-23 | McBSP General-Purpose I/O Timings | 79 |
| 5-24 | McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0 | 80 |
| 5-25 | McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0 | 81 |
| 5-26 | McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1 | 82 |
| 5-27 | McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1 | 83 |
| 5-28 | HPI-8 Mode Timing, Using $\overline{\text{HDS}}$ to Control Accesses ($\overline{\text{HCS}}$ Always Low) | 86 |
| 5-29 | HPI-8 Mode Timing, Using $\overline{\text{HCS}}$ to Control Accesses | 87 |
| 5-30 | HPI-8 Mode, $\overline{\text{HINT}}$ Timing | 87 |
| 5-31 | GPIOx Timings | 87 |
| 5-32 | HPI-16 Mode, Nonmultiplexed Read Timings | 89 |
| 5-33 | HPI-16 Mode, Nonmultiplexed Write Timings | 90 |
| 5-34 | HPI-16 Mode, HRDY Relative to CLKOUT | 90 |

List of Tables

| | | |
|------|---|--------------------|
| 2-1 | Terminal Assignments | 11 |
| 2-2 | Signal Descriptions | 13 |
| 3-1 | Standard On-Chip ROM Layout | 19 |
| 3-2 | Processor Mode Status Register (PMST) Field Descriptions | 22 |
| 3-3 | Software Wait-State Register (SWWSR) Field Descriptions | 24 |
| 3-4 | Software Wait-State Control Register (SWCR) Field Descriptions | 24 |
| 3-5 | Bank-Switching Control Register (BSCR) Field Descriptions | 25 |
| 3-6 | Bus Holder Control Bits | 26 |
| 3-7 | Sample Rate Generator Clock Source Selection | 30 |
| 3-8 | Receive Channel Enable Registers for Partitions A to H Field Descriptions | 31 |
| 3-9 | Transmit Channel Enable Registers for Partitions A to H Field Descriptions | 32 |
| 3-10 | Clock Mode Settings at Reset | 33 |
| 3-11 | DMD Section of the DMMCRn Register..... | 38 |
| 3-12 | DMA Channel Enable Control Register (DMCECTL) Descriptions | 39 |
| 3-13 | DMA Reload Register Selection | 42 |
| 3-14 | DMA Interrupts | 43 |
| 3-15 | DMA Synchronization Events..... | 44 |
| 3-16 | DMA Channel Interrupt Selection | 44 |
| 3-17 | CPU Memory-Mapped Registers..... | 46 |
| 3-18 | Peripheral Memory-Mapped Registers for Each DSP Subsystem | 47 |
| 3-19 | McBSP Control Registers and Subaddresses..... | 48 |
| 3-20 | DMA Subbank Addressed Registers | 49 |
| 3-21 | Interrupt Locations and Priorities..... | 51 |
| 5-1 | Input Clock Frequency Characteristics | 57 |
| 5-2 | Clock Mode Pin Settings for the Divide-By-2 and Divide-By-4 Clock Options | 58 |
| 5-3 | Divide-By-2 and Divide-By-4 Clock Options Timing Requirements | 58 |
| 5-4 | Divide-By-2 and Divide-By-4 Clock Options Switching Characteristics | 58 |
| 5-5 | Multiply-By-N Clock Option Timing Requirements..... | 60 |
| 5-6 | Multiply-By-N Clock Option Switching Characteristics | 60 |
| 5-7 | Memory Read Timing Requirements | 61 |
| 5-8 | Memory Read Switching Characteristics..... | 61 |
| 5-9 | Memory Write Switching Characteristics..... | 64 |
| 5-10 | I/O Read Timing Requirements | 65 |
| 5-11 | I/O Read Switching Characteristics..... | 65 |
| 5-12 | I/O Write Switching Characteristics | 67 |
| 5-13 | Ready Timing Requirements for Externally Generated Wait States | 68 |
| 5-14 | Ready Switching Characteristics for Externally Generated Wait States | 68 |
| 5-15 | $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timing Requirements | 71 |
| 5-16 | $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Switching Characteristics..... | 71 |

TMS320VC5402A

Fixed-Point Digital Signal Processor



SPRS015F – SEPTEMBER 2001 – REVISED OCTOBER 2008

www.ti.com

| | | |
|------|--|--------------------|
| 5-17 | Reset, $\overline{\text{BIO}}$, Interrupt, and $\text{MP}/\overline{\text{MC}}$ Timing Requirements | 72 |
| 5-18 | Instruction Acquisition ($\overline{\text{IAQ}}$) and Interrupt Acknowledge ($\overline{\text{IACK}}$) Switching Characteristics | 74 |
| 5-19 | External Flag (XF) and TOUT Switching Characteristics | 75 |
| 5-20 | McBSP Transmit and Receive Timing Requirements | 76 |
| 5-21 | McBSP Transmit and Receive Switching Characteristics | 77 |
| 5-22 | McBSP General-Purpose I/O Timing Requirements | 79 |
| 5-23 | McBSP General-Purpose I/O Switching Characteristics | 79 |
| 5-24 | McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0) | 80 |
| 5-25 | McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0) | 80 |
| 5-26 | McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0) | 81 |
| 5-27 | McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0) | 81 |
| 5-28 | McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1) | 82 |
| 5-29 | McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1) | 82 |
| 5-30 | McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1) | 83 |
| 5-31 | McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1) | 83 |
| 5-32 | HPI8 Mode Timing Requirements..... | 84 |
| 5-33 | HPI8 Mode Switching Characteristics | 85 |
| 5-34 | HPI16 Mode Timing Requirements | 88 |
| 5-35 | HPI16 Mode Switching Characteristics..... | 89 |
| 6-1 | Thermal Resistance Characteristics | 91 |

1 TMS320VC5402A DSP

1.1 Features

- **Advanced Multibus Architecture With Three Separate 16-Bit Data Memory Buses and One Program Memory Bus**
- **40-Bit Arithmetic Logic Unit (ALU) Including a 40-Bit Barrel Shifter and Two Independent 40-Bit Accumulators**
- **17- × 17-Bit Parallel Multiplier Coupled to a 40-Bit Dedicated Adder for Non-Pipelined Single-Cycle Multiply/Accumulate (MAC) Operation**
- **Compare, Select, and Store Unit (CSSU) for the Add/Compare Selection of the Viterbi Operator**
- **Exponent Encoder to Compute an Exponent Value of a 40-Bit Accumulator Value in a Single Cycle**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Data Bus With a Bus Holder Feature**
- **Extended Addressing Mode for 8M × 16-Bit Maximum Addressable External Program Space**
- **16K × 16-Bit On-Chip RAM Composed of:**
 - **Two Blocks of 8K × 16-Bit On-Chip Dual-Access Program/Data RAM**
- **16K × 16-Bit On-Chip ROM Configured for Program Memory**
- **Enhanced External Parallel Interface (XIO2)**
- **Single-Instruction-Repeat and Block-Repeat Operations for Program Code**
- **Block-Memory-Move Instructions for Better Program and Data Management**
- **Instructions With a 32-Bit Long Word Operand**
- **Instructions With Two- or Three-Operand Reads**
- **Arithmetic Instructions With Parallel Store and Parallel Load**
- **Conditional Store Instructions**
- **Fast Return From Interrupt**
- **On-Chip Peripherals**
 - **Software-Programmable Wait-State Generator and Programmable Bank-Switching**
 - **On-Chip Programmable Phase-Locked Loop (PLL) Clock Generator With Internal Oscillator or External Clock Source⁽¹⁾**
 - **Two 16-Bit Timers**
 - **Six-Channel Direct Memory Access (DMA) Controller**
 - **Three Multichannel Buffered Serial Ports (McBSPs)**
 - **8/16-Bit Enhanced Parallel Host-Port Interface (HPI8/16)**
- **Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions With Power-Down Modes**
- **CLKOUT Off Control to Disable CLKOUT**
- **On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1 (JTAG) Boundary Scan Logic⁽²⁾**
- **144-Pin Ball Grid Array (BGA) [GGU Suffix]**
- **144-Pin Low-Profile Quad Flatpack (LQFP)(PGE Suffix)**
- **6.25-ns Single-Cycle Fixed-Point Instruction Execution Time (160 MIPS)**
- **3.3-V I/O Supply Voltage**
- **1.6-V Core Supply Voltage**

- (1) The on-chip oscillator is not available on all 5402A devices. For applicable devices, see the TMS320VC5402A Digital Signal Processor Silicon Errata (literature number SPRZ018).
- (2) IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this document.

TMS320C54x, BGA, C54x, TMS320C5000, C5000, TMS320 are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

2 Introduction

This data manual also provides a detailed description, functional overview, electrical specifications, parameter measurement information, and mechanical data about the available packaging. This section describes the main features of the TMS320VC5402A, lists the pin assignments, and describes the function of each pin.

NOTE

This data manual is designed to be used in conjunction with the *TMS320C54x™ DSP Functional Overview* (literature number SPRU307).

2.1 Description

The TMS320VC5402A fixed-point, digital signal processor (DSP) (hereafter referred to as the device unless otherwise specified) is based on an advanced modified Harvard architecture that has one program memory bus and three data memory buses. This processor provides an arithmetic logic unit (ALU) with a high degree of parallelism, application-specific hardware logic, on-chip memory, and additional on-chip peripherals. The basis of the operational flexibility and speed of this DSP is a highly specialized instruction set.

Separate program and data spaces allow simultaneous access to program instructions and data, providing a high degree of parallelism. Two read operations and one write operation can be performed in a single cycle. Instructions with parallel store and application-specific instructions can fully utilize this architecture. In addition, data can be transferred between data and program spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that can all be performed in a single machine cycle. The device also includes the control mechanisms to manage interrupts, repeated operations, and function calls.

2.2 Pin Assignments

Figure 2-1 illustrates the ball locations for the 144-pin ball grid array (BGA) package and is used in conjunction with Table 2-1 to locate signal names and ball grid numbers. Figure 2-2 provides the pin assignments for the 144-pin low-profile flatpack (LQFP) package.

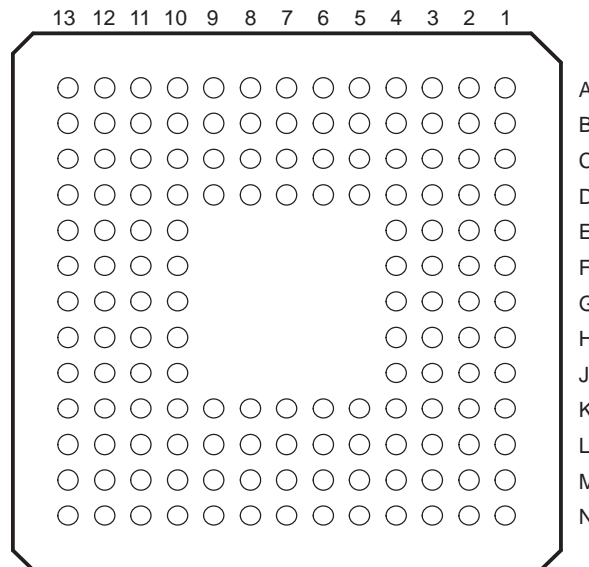


Figure 2-1. 144-Ball GGU MicroStar BGA™ (Bottom View)

2.2.1 Terminal Assignments for the GGU Package

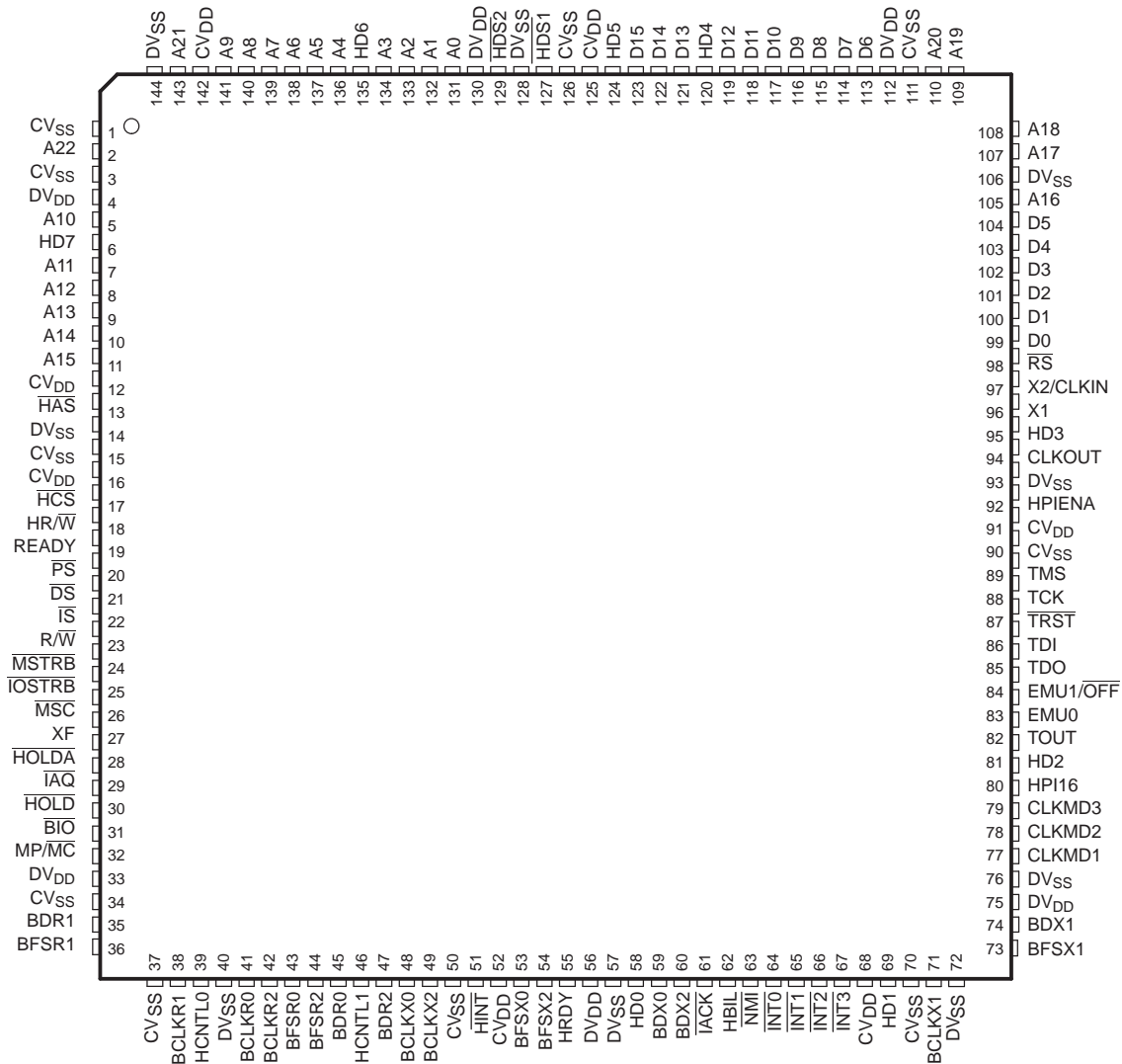
Table 2-1 lists each signal name and BGA ball number for the 144-pin TMS320VC5402AGGU package.

Table 2-1. Terminal Assignments

| SIGNAL QUADRANT 1 | BGA BALL # | SIGNAL QUADRANT 2 | BGA BALL # | SIGNAL QUADRANT 3 | BGA BALL # | SIGNAL QUADRANT 4 | BGA BALL # |
|----------------------------|------------|-------------------------------|------------|--------------------------|------------|-------------------|------------|
| CV _{SS} | A1 | BFSX1 | N13 | CV _{SS} | N1 | A19 | A13 |
| A22 | B1 | BDX1 | M13 | BCLKR1 | N2 | A20 | A12 |
| CV _{SS} | C2 | DV _{DD} | L12 | HCNTL0 | M3 | CV _{SS} | B11 |
| DV _{DD} | C1 | DV _{SS} | L13 | DV _{SS} | N3 | DV _{DD} | A11 |
| A10 | D4 | CLKMD1 | K10 | BCLKR0 | K4 | D6 | D10 |
| HD7 | D3 | CLKMD2 | K11 | BCLKR2 | L4 | D7 | C10 |
| A11 | D2 | CLKMD3 | K12 | BFSR0 | M4 | D8 | B10 |
| A12 | D1 | HPI16 | K13 | BFSR2 | N4 | D9 | A10 |
| A13 | E4 | HD2 | J10 | BDR0 | K5 | D10 | D9 |
| A14 | E3 | TOUT | J11 | HCNTL1 | L5 | D11 | C9 |
| A15 | E2 | EMU0 | J12 | BDR2 | M5 | D12 | B9 |
| CV _{DD} | E1 | EMU1/ $\overline{\text{OFF}}$ | J13 | BCLKX0 | N5 | HD4 | A9 |
| $\overline{\text{HAS}}$ | F4 | TDO | H10 | BCLKX2 | K6 | D13 | D8 |
| DV _{SS} | F3 | TDI | H11 | CV _{SS} | L6 | D14 | C8 |
| CV _{SS} | F2 | $\overline{\text{TRST}}$ | H12 | HINT | M6 | D15 | B8 |
| CV _{DD} | F1 | TCK | H13 | CV _{DD} | N6 | HD5 | A8 |
| $\overline{\text{HCS}}$ | G2 | TMS | G12 | BFSX0 | M7 | CV _{DD} | B7 |
| HR/ $\overline{\text{W}}$ | G1 | CV _{SS} | G13 | BFSX2 | N7 | CV _{SS} | A7 |
| READY | G3 | CV _{DD} | G11 | HRDY | L7 | HDS1 | C7 |
| $\overline{\text{PS}}$ | G4 | HPIENA | G10 | DV _{DD} | K7 | DV _{SS} | D7 |
| $\overline{\text{DS}}$ | H1 | DV _{SS} | F13 | DV _{SS} | N8 | HDS2 | A6 |
| $\overline{\text{IS}}$ | H2 | CLKOUT | F12 | HD0 | M8 | DV _{DD} | B6 |
| R/ $\overline{\text{W}}$ | H3 | HD3 | F11 | BDX0 | L8 | A0 | C6 |
| $\overline{\text{MSTRB}}$ | H4 | X1 | F10 | BDX2 | K8 | A1 | D6 |
| $\overline{\text{IOSTRB}}$ | J1 | X2/CLKIN | E13 | $\overline{\text{IACK}}$ | N9 | A2 | A5 |
| $\overline{\text{MSC}}$ | J2 | $\overline{\text{RS}}$ | E12 | HBIL | M9 | A3 | B5 |
| XF | J3 | D0 | E11 | $\overline{\text{NMI}}$ | L9 | HD6 | C5 |
| $\overline{\text{HOLDA}}$ | J4 | D1 | E10 | $\overline{\text{INT0}}$ | K9 | A4 | D5 |
| IAQ | K1 | D2 | D13 | $\overline{\text{INT1}}$ | N10 | A5 | A4 |
| $\overline{\text{HOLD}}$ | K2 | D3 | D12 | $\overline{\text{INT2}}$ | M10 | A6 | B4 |
| $\overline{\text{BIO}}$ | K3 | D4 | D11 | $\overline{\text{INT3}}$ | L10 | A7 | C4 |
| MP/ $\overline{\text{MC}}$ | L1 | D5 | C13 | CV _{DD} | N11 | A8 | A3 |
| DV _{DD} | L2 | A16 | C12 | HD1 | M11 | A9 | B3 |
| CV _{SS} | L3 | DV _{SS} | C11 | CV _{SS} | L11 | CV _{DD} | C3 |
| BDR1 | M1 | A17 | B13 | BCLKX1 | N12 | A21 | A2 |
| BFSR1 | M2 | A18 | B12 | DV _{SS} | M12 | DV _{SS} | B2 |

2.2.2 Pin Assignments for the PGE Package

The TMS320VC5402APGE 144-pin low-profile quad flatpack (LQFP) pin assignments are shown in Figure 2-2.



- A. DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. DV_{SS} is the ground for the I/O pins while CV_{SS} is the ground for the core CPU. The DV_{SS} and CV_{SS} pins can be connected to a common ground plane in a system.

Figure 2-2. 144-Pin PGE Low-Profile Quad Flatpack (Top View)

2.3 Signal Descriptions

Table 2-2 lists each signal, function, and operating mode(s) grouped by function. See Section 2.2 for exact pin locations based on package type.

Table 2-2. Signal Descriptions

| TERMINAL NAME | I/O ⁽¹⁾ | DESCRIPTION |
|--|-------------------------|---|
| DATA SIGNALS | | |
| A22 (MSB) A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 (LSB) | I/O/Z ⁽¹⁾⁽²⁾ | Parallel address bus A22 [most significant bit (MSB)] through A0 [least significant bit (LSB)]. The sixteen LSB lines, A0 to A15, are multiplexed to address external memory (program, data) or I/O. The seven MSB lines, A16 to A22, address external program space memory. A22-A0 is placed in the high-impedance state in the hold mode. A22-A0 also goes into the high-impedance state when $\overline{\text{OFF}}$ is low. A15-A0 are inputs in HPI16 mode. These pins can be used to address internal memory via the host-port interface (HPI) when the HPI16 pin is high. These pins also have Schmitt trigger inputs. The address bus has a bus holder feature that eliminates passive components and the power dissipation associated with them. The bus holder keeps the address bus at the previous logic level when the bus goes into a high-impedance state. |
| D15 (MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 (LSB) | I/O/Z ⁽¹⁾⁽²⁾ | Parallel data bus D15 (MSB) through D0 (LSB). D15-D0 is multiplexed to transfer data between the core CPU and external data/program memory or I/O devices or HPI in HPI16 mode (when HPI16 pin is high). D15-D0 is placed in the high-impedance state when not outputting data or when $\overline{\text{RS}}$ or $\overline{\text{HOLD}}$ is asserted. D15-D0 also goes into the high-impedance state when $\overline{\text{OFF}}$ is low. These pins also have Schmitt trigger inputs. The data bus has a bus holder feature that eliminates passive components and the power dissipation associated with them. The bus holder keeps the data bus at the previous logic level when the bus goes into the high-impedance state. The bus holders on the data bus can be enabled/disabled under software control. |
| INITIALIZATION, INTERRUPT AND RESET OPERATIONS | | |
| $\overline{\text{IACK}}$ | O/Z | Interrupt acknowledge signal. $\overline{\text{IACK}}$ indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15-A0. $\overline{\text{IACK}}$ also goes into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| $\overline{\text{INT0}}$ ⁽¹⁾ $\overline{\text{INT1}}$ ⁽¹⁾ $\overline{\text{INT2}}$ ⁽¹⁾ $\overline{\text{INT3}}$ ⁽¹⁾ | I | External user interrupt inputs. $\overline{\text{INT0}}-\overline{\text{INT3}}$ are maskable and are prioritized by the interrupt mask register (IMR) and the interrupt mode bit. $\overline{\text{INT0}}-\overline{\text{INT3}}$ can be polled and reset by way of the interrupt flag register (IFR). |
| $\overline{\text{NMI}}$ ⁽¹⁾ | I | Nonmaskable interrupt. $\overline{\text{NMI}}$ is an external interrupt that cannot be masked by way of the INTM or the IMR. When NMI is activated, the processor traps to the appropriate vector location. |
| $\overline{\text{RS}}$ ⁽¹⁾ | I | Reset. $\overline{\text{RS}}$ causes the digital signal processor (DSP) to terminate execution and forces the program counter to 0FF80h. When $\overline{\text{RS}}$ is brought to a high level, execution begins at location 0FF80h of program memory. $\overline{\text{RS}}$ affects various registers and status bits. |

(1) I = Input, O = Output, Z = High-impedance, S = Supply

(2) This pin has an internal bus holder controlled by way of the BSCR register.

Table 2-2. Signal Descriptions (continued)

| TERMINAL NAME | I/O ⁽¹⁾ | DESCRIPTION |
|---|--------------------|--|
| MP/̄MC | I | Microprocessor/microcomputer mode select. If active low at reset, microcomputer mode is selected, and the internal program ROM is mapped into the upper 16K words of program memory space. If the pin is driven high during reset, microprocessor mode is selected, and the on-chip ROM is removed from program space. This pin is only sampled at reset, and the MP/̄MC bit of the processor mode status (PMST) register can override the mode that is selected at reset. |
| MULTIPROCESSING SIGNALS | | |
| ̄BIO ⁽¹⁾ | I | Branch control. A branch can be conditionally executed when ̄BIO is active. If low, the processor executes the conditional instruction. The ̄BIO condition is sampled during the decode phase of the pipeline for the XC instruction, and all other instructions sample BIO during the read phase of the pipeline. |
| XF | O/Z | External flag output (latched software-programmable signal). XF is set high by the SSBX XF instruction, set low by RSBX XF instruction or by loading ST1. XF is used for signaling other processors in multiprocessor configurations or used as a general-purpose output pin. XF goes into the high-impedance state when ̄OFF is low, and is set high at reset. |
| MEMORY CONTROL SIGNALS | | |
| ̄DS ̄PS ̄IS | O/Z | Data, program, and I/O space select signals. ̄DS, ̄PS, and ̄IS are always high unless driven low for communicating to a particular external space. Active period corresponds to valid address information. ̄DS, ̄PS, and ̄IS are placed into the high-impedance state in the hold mode; these signals also go into the high-impedance state when ̄OFF is low. |
| ̄MSTRB | O/Z | Memory strobe signal. ̄MSTRB is always high unless low-level asserted to indicate an external bus access to data or program memory. MSTRB is placed in the high-impedance state in the hold mode; it also goes into the high-impedance state when ̄OFF is low. |
| READY | I | Data ready. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. Note that the processor performs ready detection if at least two software wait states are programmed. The READY signal is not sampled until the completion of the software wait states. |
| R/̄W | O/Z | Read/write signal. R/̄W indicates transfer direction during communication to an external device. R/̄W is normally in the read mode (high), unless it is asserted low when the DSP performs a write operation. R/̄W is placed in the high-impedance state in the hold mode; and it also goes into the high-impedance state when ̄OFF is low. |
| ̄IOSTRB | O/Z | I/O strobe signal. ̄IOSTRB is always high unless low-level asserted to indicate an external bus access to an I/O device. IOSTRB is placed in the high-impedance state in the hold mode; it also goes into the high-impedance state when ̄OFF is low. |
| ̄HOLD | I | Hold input. ̄HOLD is asserted to request control of the address, data, and control lines. When acknowledged by the 5402A, these lines go into the high-impedance state. |
| ̄HOLDA | O/Z | Hold acknowledge. ̄HOLDA indicates to the external circuitry that the processor is in a hold state and that the address, data, and control lines are in the high-impedance state, allowing them to be available to the external circuitry. HOLDA also goes into the high-impedance state when ̄OFF is low. This pin is driven high during reset. |
| ̄MSC | O/Z | Microstate complete. ̄MSC indicates completion of all software wait states. When two or more software wait states are enabled, the ̄MSC pin goes active at the beginning of the first software wait state and goes inactive high at the beginning of the last software wait state. If connected to the READY input, MSC forces one external wait state after the last internal wait state is completed. ̄MSC also goes into the high-impedance state when ̄OFF is low. |
| ̄IAQ | O/Z | Instruction acquisition signal. ̄IAQ is asserted (active low) when there is an instruction address on the address bus and goes into the high-impedance state when ̄OFF is low. |
| OSCILLATOR/TIMER SIGNALS | | |
| CLKOUT | O/Z | Clock output signal. CLKOUT can represent the machine-cycle rate of the CPU divided by 1, 2, 3, or 4 as configured in the bank-switching control register (BSCR). Following reset, CLKOUT represents the machine-cycle rate divided by 4. |
| CLKMD1 ⁽¹⁾ CLKMD2 ⁽¹⁾ CLKMD3 ⁽¹⁾ | I | Clock mode select signals. CLKMD1-CLKMD3 allow the selection and configuration of different clock modes such as crystal, external clock, and PLL mode. The external CLKMD1-CLKMD3 pins are sampled to determine the desired clock generation mode while RS is low. Following reset, the clock generation mode can be reconfigured by writing to the internal clock mode register in software. |
| X2/CLKIN ⁽¹⁾ | I | Clock/oscillator input. If the internal oscillator is not being used, X2/CLKIN functions as the clock input. (This is revision-dependent, see Section 3.10 for additional information.) |
| X1 | O | Output pin from the internal oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. X1 does not go into the high-impedance state when ̄OFF is low. (This is revision-dependent, see Section 3.10 for additional information.) |

Table 2-2. Signal Descriptions (continued)

| TERMINAL NAME | I/O ⁽¹⁾ | DESCRIPTION |
|---|--------------------|--|
| TOUT | O/Z | Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is one CLKOUT cycle wide. TOUT also goes into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| MULTICHANNEL BUFFERED SERIAL PORT 0 (McBSP #0), MULTICHANNEL BUFFERED SERIAL PORT 1 (McBSP #1), AND MULTICHANNEL BUFFERED SERIAL PORT 2 (McBSP #2) SIGNALS | | |
| BCLKR0 ⁽¹⁾ BCLKR1 ⁽¹⁾ BCLKR2 ⁽¹⁾ | I/O/Z | Receive clock input. BCLKR can be configured as an input or an output; it is configured as an input following reset. BCLKR serves as the serial shift clock for the buffered serial port receiver. |
| BDR0 BDR1 BDR2 | I | Serial data receive input |
| BFSR0 BFSR1 BFSR2 | I/O/Z | Frame synchronization pulse for receive input. BFSR can be configured as an input or an output; it is configured as an input following reset. The BFSR pulse initiates the receive data process over BDR. |
| BCLKX0 ⁽¹⁾ BCLKX1 ⁽¹⁾ BCLKX2 ⁽¹⁾ | I/O/Z | Transmit clock. BCLKX serves as the serial shift clock for the McBSP transmitter. BCLKX can be configured as an input or an output, and is configured as an input following reset. BCLKX enters the high-impedance state when $\overline{\text{OFF}}$ goes low. |
| BDX0 BDX1 BDX2 | O/Z | Serial data transmit output. BDX is placed in the high-impedance state when not transmitting, when $\overline{\text{RS}}$ is asserted, or when $\overline{\text{OFF}}$ is low. |
| BFSX0 BFSX1 BFSX2 | I/O/Z | Frame synchronization pulse for transmit input/output. The BFSX pulse initiates the data transmit process over BDX. BFSX can be configured as an input or an output, and is configured as an input following reset. BFSX goes into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| HOST-PORT INTERFACE SIGNALS | | |
| HD0-HD7 ⁽¹⁾⁽²⁾ | I/O/Z | Parallel bidirectional data bus. The HPI data bus is used by a host device bus to exchange information with the HPI registers. These pins can also be used as general-purpose I/O pins. HD0-HD7 is placed in the high-impedance state when not outputting data or when $\overline{\text{OFF}}$ is low. The HPI data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. When the HPI data bus is not being driven by the 5402A, the bus holders keep the pins at the previous logic level. The HPI data bus holders are disabled at reset and can be enabled/disabled via the HBH bit of the BSCR. These pins also have Schmitt trigger inputs. |
| HCNTL0 ⁽³⁾ HCNTL1 ⁽³⁾ | I | Control inputs. HCNTL0 and HCNTL1 select a host access to one of the three HPI registers. The control inputs have internal pullups that are only enabled when HPIENA = 0. These pins are not used when HPI16 = 1. |
| HBIL ⁽³⁾ | I | Byte identification. HBIL identifies the first or second byte of transfer. The HPIIL input has an internal pullup resistor that is only enabled when HPIENA = 0. This pin is not used when HPI16 = 1. |
| $\overline{\text{HCS}}$ ⁽¹⁾⁽³⁾ | I | Chip select. $\overline{\text{HCS}}$ is the select input for the HPI and must be driven low during accesses. The chip select input has an internal pullup resistor that is only enabled when HPIENA = 0. |
| $\overline{\text{HDS1}}$ ⁽¹⁾⁽³⁾ $\overline{\text{HDS2}}$ ⁽¹⁾⁽³⁾ | I | Data strobe. $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$ are driven by the host read and write strobes to control the transfer. The strobe inputs have internal pullup resistors that are only enabled when HPIENA = 0. |
| $\overline{\text{HAS}}$ ⁽¹⁾⁽³⁾ | I | Address strobe. Host with multiplexed address and data pins requires $\overline{\text{HAS}}$ to latch the address in the HPIA register. $\overline{\text{HAS}}$ input has an internal pullup resistor that is only enabled when HPIENA = 0. |
| $\text{HR}/\overline{\text{W}}$ ⁽³⁾ | I | Read/write. $\text{HR}/\overline{\text{W}}$ controls the direction of the HPI transfer. $\text{HR}/\overline{\text{W}}$ has an internal pullup resistor that is only enabled when HPIENA = 0. |
| HRDY | O/Z | Ready output. HRDY goes into the high-impedance state when $\overline{\text{OFF}}$ is low. The ready output informs the host when the HPI is ready for the next transfer. |
| $\overline{\text{HINT}}$ | O/Z | Interrupt output. This output is used to interrupt the host. When the DSP is in reset, $\overline{\text{HINT}}$ is driven high. $\overline{\text{HINT}}$ goes into the high-impedance state when $\overline{\text{OFF}}$ is low. This pin is not used when HPI16 = 1. |
| HPIENA ⁽⁴⁾ | I | HPI module select. HPIENA must be tied to DV _{DD} to have HPI selected. If HPIENA is left open or connected to ground, the HPI module is not selected, internal pullup for the HPI input pins are enabled, and the HPI data bus has holders set. HPIENA is provided with an internal pulldown resistor that is active only when RS is low. HPIENA is sampled when RS goes high and is ignored until RS goes low again. |
| HPI16 ⁽⁴⁾ | I | HPI16 mode selection. This pin must be tied to DV _{DD} to enable HPI16 mode. The pin has an internal pulldown resistor which is always active. If HPI16 is left open or driven low, the HPI16 mode is disabled. |
| SUPPLY PINS | | |
| CV _{SS} | S | Ground. Dedicated ground for the core CPU |

(3) This pin has an internal pullup resistor.

(4) This pin has an internal pulldown resistor.

Table 2-2. Signal Descriptions (continued)

| TERMINAL NAME | I/O ⁽¹⁾ | DESCRIPTION |
|--|--------------------|--|
| CV _{DD} | S | +V _{DD} . Dedicated power supply for the core CPU |
| DV _{SS} | S | Ground. Dedicated ground for I/O pins |
| DV _{DD} | S | +V _{DD} . Dedicated power supply for I/O pins |
| TEST PINS | | |
| TCK ⁽¹⁾⁽³⁾ | I | IEEE standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on test access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK. |
| TDI ⁽³⁾ | I | IEEE standard 1149.1 test data input. Pin with internal pullup device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. |
| TDO | O/Z | IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state <u>except</u> when the scanning of data is in progress. TDO also goes into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| TMS ⁽³⁾ | I | IEEE standard 1149.1 test mode select. Pin with internal pullup device. This serial control input is clocked into the TAP controller on the rising edge of TCK. |
| $\overline{\text{TRST}}$ ^{(4) (5)} | I | IEEE standard 1149.1 test reset. $\overline{\text{TRST}}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{\text{TRST}}$ is driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. Pin with internal pulldown device. |
| EMU0 ⁽⁶⁾ | I/O/Z | Emulator 0 pin. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for activation of the $\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of the IEEE standard 1149.1 scan system. |
| EMU1/ $\overline{\text{OFF}}$ ⁽⁶⁾ | I/O/Z | Emulator 1 pin/disable all outputs. When $\overline{\text{TRST}}$ is driven high, EMU1/ $\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as input/output by way of IEEE standard 1149.1 scan system. When $\overline{\text{TRST}}$ is driven low, EMU1/ $\overline{\text{OFF}}$ is configured as $\overline{\text{OFF}}$. The EMU1/ $\overline{\text{OFF}}$ signal, when active low, puts all output drivers into the high-impedance state. Note that $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). Therefore, for the $\overline{\text{OFF}}$ condition, the following apply: <ul style="list-style-type: none"> • $\overline{\text{TRST}}$ = low, • EMU0 = high • EMU1/$\overline{\text{OFF}}$ = low |

(5) Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{\text{TRST}}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.

(6) This pin must be pulled up with a 4.7-kΩ resistor to ensure the device is operable in functional mode or emulation mode.

3 Functional Overview

The following functional overview is based on the block diagram in [Figure 3-1](#).

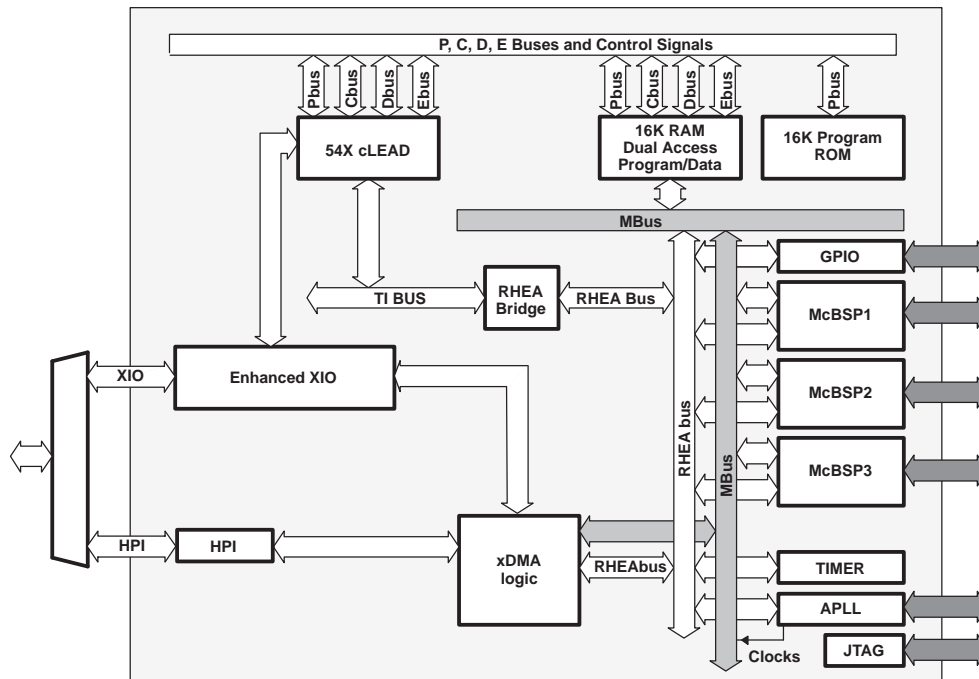


Figure 3-1. TMS320VC5402A Functional Block Diagram

3.1 Memory

The 5402A device provides both on-chip ROM and RAM memories to aid in system performance and integration.

3.1.1 Data Memory

The data memory space addresses up to 64K of 16-bit words. The device automatically accesses the on-chip RAM when addressing is within its bounds. When an address is generated outside the RAM bounds, the device automatically generates an external access.

The advantages of operating from on-chip memory are as follows:

- Higher performance because no wait states are required
- Higher performance because of better flow within the pipeline of the central arithmetic logic unit (CALU)
- Lower cost than external memory
- Lower power than external memory

The advantage of operating from off-chip memory is the ability to access a larger address space.

3.1.2 Program Memory

Software can configure the memory cells to reside inside or outside of the program address map. When the cells are mapped into program space, the device automatically accesses them when their addresses are within bounds. When the program-address generation (PAGEN) logic generates an address outside its bounds, the device automatically generates an external access. The advantages of operating from on-chip memory are as follows:

- Higher performance because no wait states are required
- Lower cost than external memory
- Lower power than external memory

The advantage of operating from off-chip memory is the ability to access a larger address space.

3.1.3 Extended Program Memory

This device uses a paged extended memory scheme in program space to allow access of up to 8192K of program memory. In order to implement this scheme, the device includes several features which are also present on C548/549/5410/5409A:

- Twenty-three address lines, instead of sixteen
- An extra memory-mapped register, the XPC
- Six extra instructions for addressing extended program space

Program memory is organized into 128 pages that are each 64K in length.

The value of the XPC register defines the page selection. This register is memory-mapped into data space to address 001Eh. At a hardware reset, the XPC is initialized to 0.

3.2 On-Chip ROM With Bootloader

This device features a 16K-word \times 16-bit on-chip maskable ROM that can only be mapped into program memory space.

Customers can arrange to have the ROM of the 5402A programmed with contents unique to any particular application.

A bootloader is available in the standard 5402A on-chip ROM. This bootloader can be used to automatically transfer user code from an external source to anywhere in the program memory at power up. If $\overline{\text{MP/MC}}$ of the device is sampled low during a hardware reset, execution begins at location FF80h of the on-chip ROM. This location contains a branch instruction to the start of the bootloader program.

The standard device provides different ways to download the code to accommodate various system requirements:

- Parallel from 8-bit or 16-bit-wide EPROM
- Parallel from I/O space, 8-bit or 16-bit mode
- Serial boot from serial ports, 8-bit or 16-bit mode
- Host-port interface boot
- Serial EEPROM mode
- Warm boot

The standard on-chip ROM layout is shown in [Table 3-1](#).

Table 3-1. Standard On-Chip ROM Layout

| ADDRESS RANGE | DESCRIPTION |
|---------------|---|
| C000h–D4FFh | ROM tables for the GSM EFR speech codec |
| D500h–F7FFh | Reserved |
| F800h–FBFFh | Bootloader |
| FC00h–FCFFh | μ-Law expansion table |
| FD00h–FDFFh | A-Law expansion table |
| FE00h–FEFFh | Sine look-up table |
| FF00h–FF7Fh | Reserved ⁽¹⁾ |
| FF80h–FFFFh | Interrupt vector table |

(1) In the 5402A ROM, 128 words are reserved for factory device-testing purposes. Application code to be implemented in on-chip ROM must reserve these 128 words at addresses FF00h–FF7Fh in program space.

3.3 On-Chip RAM

The 5402A device contains 16K-word × 16-bit of on-chip dual-access RAM (DARAM).

The DARAM is composed of two blocks of 8K words each. Each block in the DARAM can support two reads in one cycle, or a read and a write in one cycle. Two blocks of DARAM are located in the address range 0080h–3FFFh in data space, and can be mapped into program/data space by setting the OVLY bit to one.

3.4 On-Chip Memory Security

The TMS320VC5402A device has a maskable option to protect the contents of on-chip memories.

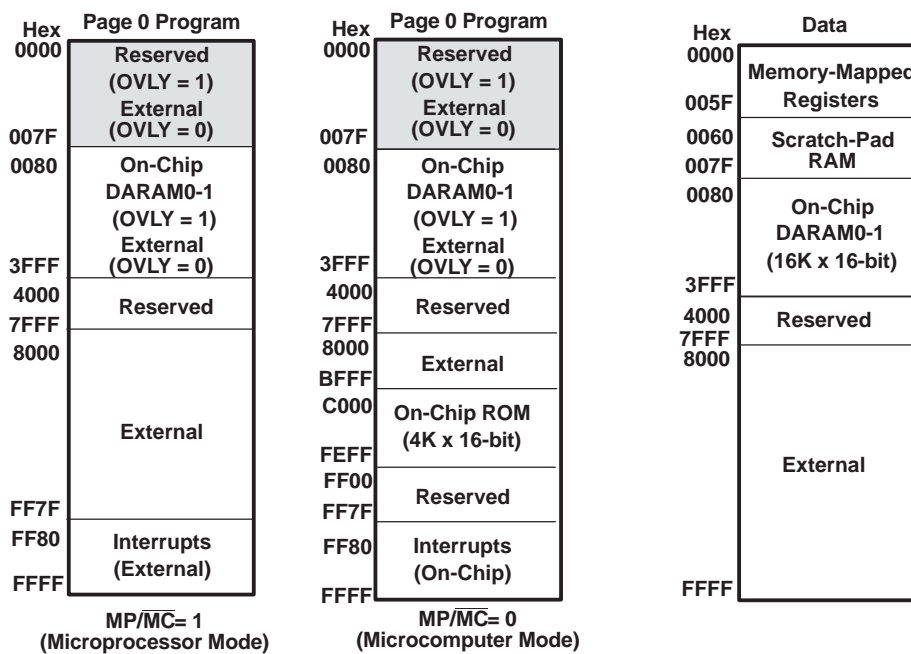
When the *RAM/ROM* security option is selected, the following restrictions apply:

- Only the on-chip ROM-originating instructions can read the contents of the on-chip ROM. On-chip RAM and external RAM-originating instructions cannot read data from ROM; instead, 0FFFFh is read. Code can still branch to ROM from on-chip RAM or external program memory.
- The contents of on-chip RAM can be read by all instructions, even by instructions fetched from external memory. To protect the internal RAM, the user must never branch to external memory.
- The security feature completely disables the scan-based emulation capability of the 54x to prevent the use of a debugger utility. This only affects emulation and does not prevent the use of the JTAG boundary scan test capability.
- The device is internally forced into microcomputer mode at reset ($\overline{MP/\overline{MC}}$ bit forced to zero), preventing the ROM from being disabled by the external $\overline{MP/\overline{MC}}$ pin. The status of the $\overline{MP/\overline{MC}}$ bit in the PMST register can be changed after reset by the user application.
- HPI writes have no restriction, but HPI reads are restricted to the 4000h - 5FFFh address range.

If the ROM-only security option is selected the following restrictions apply:

- Only the on-chip ROM-originating instructions can read the contents of the on-chip ROM. On-chip RAM and external RAM-originating instructions cannot read data from ROM; instead, 0FFFFh is read. Code can still branch to ROM from on-chip RAM or external program memory.
- The contents of on-chip RAM can be read by all instructions, even by instructions fetched from external memory. To protect the internal RAM the user must never branch to external memory.
- The security feature completely disables the scan-based emulation capability of the 54x to prevent the use of a debugger utility. This only affects emulation and does not prevent the use of the JTAG boundary scan test capability.
- The device can be started in either microcomputer mode or microprocessor mode at reset (depends on the MP/ \overline{MC} pin).
- HPI reads and writes have no restriction.

3.5 Memory Map



A. Address ranges for on-chip DARAM in data memory are: DARAM0: 0080h–1FFFh; DARAM1: 2000h–3FFFh

Figure 3-2. Program and Data Memory Map

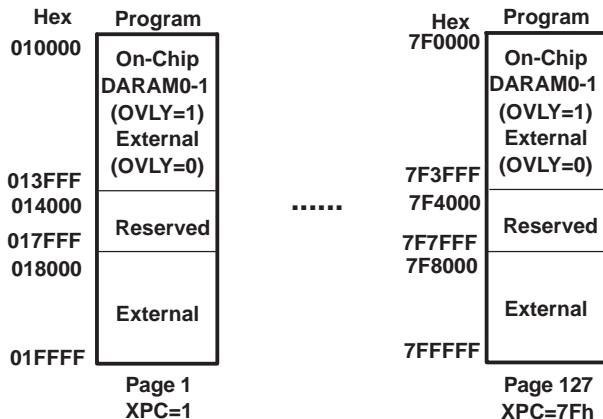


Figure 3-3. Extended Program Memory Map

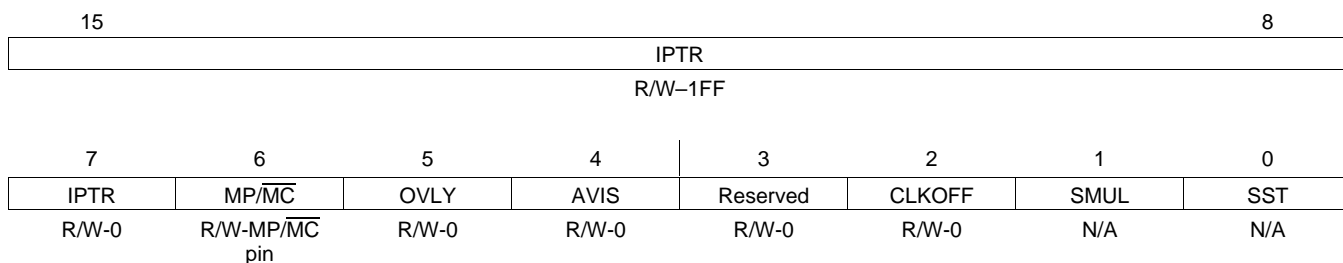
3.5.1 Relocatable Interrupt Vector Table

The reset, interrupt, and trap vectors are addressed in program space. These vectors are soft — meaning that the processor, when taking the trap, loads the program counter (PC) with the trap address and executes the code at the vector location. Four words, either two 1-word instructions or one 2-word instruction, are reserved at each vector location to accommodate a delayed branch instruction which allows branching to the appropriate interrupt service routine without the overhead.

At device reset, the reset, interrupt, and trap vectors are mapped to address FF80h in program space. However, these vectors can be remapped to the beginning of any 128-word page in program space after device reset. This is done by loading the interrupt vector pointer (IPTR) bits in the PMST register with the appropriate 128-word page boundary address. After loading IPTR, any user interrupt or trap vector is mapped to the new 128-word page.

NOTE

The hardware reset (\overline{RS}) vector cannot be remapped because the hardware reset loads the IPTR with 1s. Therefore, the reset vector is always fetched at location FF80h in program space.



LEGEND: R = Read, W = Write, n = value at reset

Figure 3-4. Processor Mode Status Register (PMST)

Table 3-2. Processor Mode Status Register (PMST) Field Descriptions

| BIT | FIELD | VALUE | DESCRIPTION |
|------|---------------------|-------|--|
| 15–7 | IPTR | 1FFh | Interrupt vector pointer. The 9-bit IPTR field points to the 128-word program page where the interrupt vectors reside. The interrupt vectors can be remapped to RAM for boot-loaded operations. At reset, these bits are all set to 1; the reset vector always resides at address FF80h in program memory space. The RESET instruction does not affect this field. |
| 6 | MP/ \overline{MC} | | Microprocessor/microcomputer mode. MP/ \overline{MC} enables/disables the on-chip ROM to be addressable in program memory space. |
| | | 0 | The on-chip ROM is enabled and addressable. |
| | | 1 | The on-chip ROM is not available. |
| | | | MP/ \overline{MC} is set to the value corresponding to the logic level on the MP/ \overline{MC} pin when sampled at reset. This pin is not sampled again until the next reset. The RESET instruction does not affect this bit. This bit can also be set or cleared by software. |
| 5 | OVLY | | RAM overlay. OVLY enables on-chip dual-access data RAM blocks to be mapped into program space. The values for the OVLY bit are: |
| | | 0 | The on-chip RAM is addressable in data space but not in program space. |
| | | 1 | The on-chip RAM is mapped into program space and data space. Data page 0 (addresses 0h to 7Fh), however, is not mapped into program space. |
| 4 | AVIS | | Address visibility mode. AVIS enables/disables the internal program address to be visible at the address pins. |
| | | 0 | The external address lines do not change with the internal program address. Control and data lines are not affected and the address bus is driven with the last address on the bus. |
| | | 1 | This mode allows the internal program address to appear at the pins of the 5402A so that the internal program address can be traced. Also, it allows the interrupt vector to be decoded in conjunction with IACK when the interrupt vectors reside on on-chip memory. |
| 3 | Reserved | 0 | Reserved |
| 2 | CLKOFF | 0 | CLOCKOUT off. When the CLKOFF bit is 1, the output of CLKOUT is disabled and remains at a high level. |
| 1 | SMUL | N/A | Saturation on multiplication. When SMUL = 1, saturation of a multiplication result occurs before performing the accumulation in a MAC of MAS instruction. The SMUL bit applies only when OVM = 1 and FRCT = 1. |
| 0 | SST | N/A | Saturation on store. When SST = 1, saturation of the data from the accumulator is enabled before storing in memory. The saturation is performed after the shift operation. |

3.6 On-Chip Peripherals

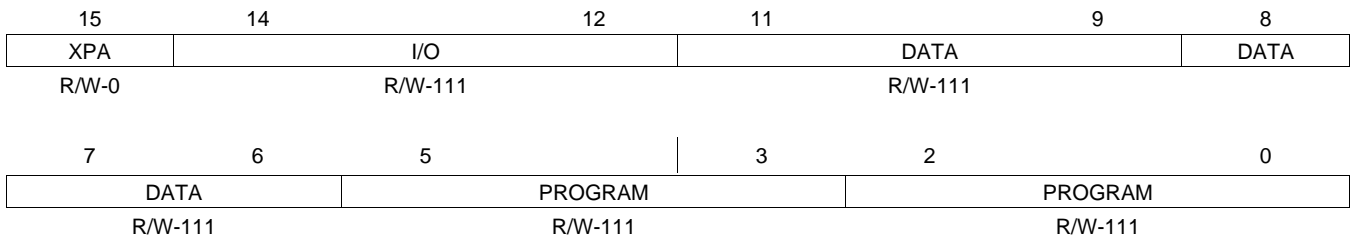
The 5402A device has the following peripherals:

- Software-programmable wait-state generator
- Programmable bank-switching
- A host-port interface (HPI8/16)
- Three multichannel buffered serial ports (McBSPs)
- Two hardware timers
- A clock generator with a multiple phase-locked loop (PLL)
- Enhanced external parallel interface (XIO2)
- A DMA controller (DMA)

3.6.1 Software-Programmable Wait-State Generator

The software wait-state generator of the 5402A can extend external bus cycles by up to fourteen machine cycles. Devices that require more than fourteen wait states can be interfaced using the hardware READY line. When all external accesses are configured for zero wait states, the internal clocks to the wait-state generator are automatically disabled. Disabling the wait-state generator clocks reduces the power consumption of the 5402A.

The software wait-state register (SWWSR) controls the operation of the wait-state generator. The 14 LSBs of the SWWSR specify the number of wait states (0 to 7) to be inserted for external memory accesses to five separate address ranges. This allows a different number of wait states for each of the five address ranges. Additionally, the software wait-state multiplier (SWSM) bit of the software wait-state control register (SWCR) defines a multiplication factor of 1 or 2 for the number of wait states. At reset, the wait-state generator is initialized to provide seven wait states on all external memory accesses. The SWWSR bit fields are shown in [Figure 3-5](#) and described in [Table 3-3](#).



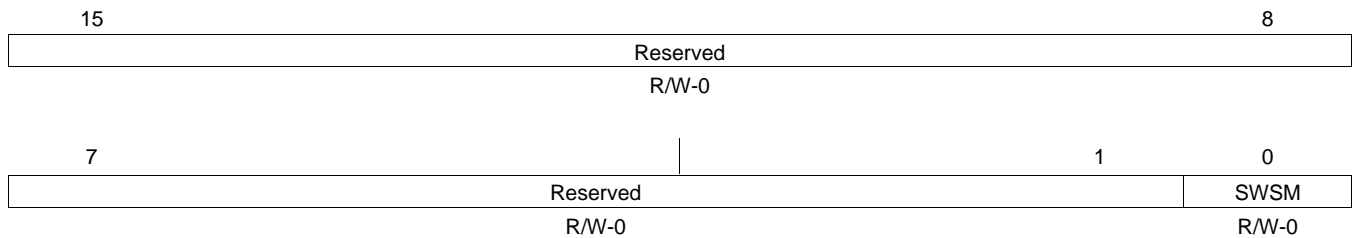
LEGEND: R = Read, W = Write, n = value at reset

Figure 3-5. Software Wait-State Register (SWWSR) [Memory-Mapped Register (MMR) Address 0028h]

Table 3-3. Software Wait-State Register (SWWSR) Field Descriptions

| BIT | FIELD | VALUE | DESCRIPTION |
|-------|---------|-------|---|
| 15 | XPA | 0 | Extended program address control bit. XPA is used in conjunction with the program space fields (bits 0 through 5) to select the address range for program space wait states. |
| 14–12 | I/O | 111 | I/O space. The field value (0–7) corresponds to the base number of wait states for I/O space accesses within addresses 0000–FFFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states. |
| 11–9 | Data | 111 | Upper data space. The field value (0–7) corresponds to the base number of wait states for external data space accesses within addresses 8000–FFFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states. |
| 8–6 | Data | 111 | Lower data space. The field value (0–7) corresponds to the base number of wait states for external data space accesses within addresses 0000–7FFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states. |
| 5–3 | Program | 111 | Upper program space. The field value (0–7) corresponds to the base number of wait states for external program space accesses within the following addresses: <ul style="list-style-type: none"> • XPA = 0: xx8000 – xxFFFFh • XPA = 1: 400000h – 7FFFFFFh The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states. |
| 2–0 | Program | 111 | Program space. The field value (0–7) corresponds to the base number of wait states for external program space accesses within the following addresses: <ul style="list-style-type: none"> • XPA = 0: xx0000 – xx7FFFh • XPA = 1: 000000 – 3FFFFFFh The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states. |

The software wait-state multiplier bit of the software wait-state control register (SWCR) is used to extend the base number of wait states selected by the SWWSR. The SWCR bit fields are shown in [Figure 3-6](#) and described in [Table 3-4](#).



LEGEND: R = Read, W = Write, n = value at reset

Figure 3-6. Software Wait-State Control Register (SWCR) [MMR Address 002Bh]

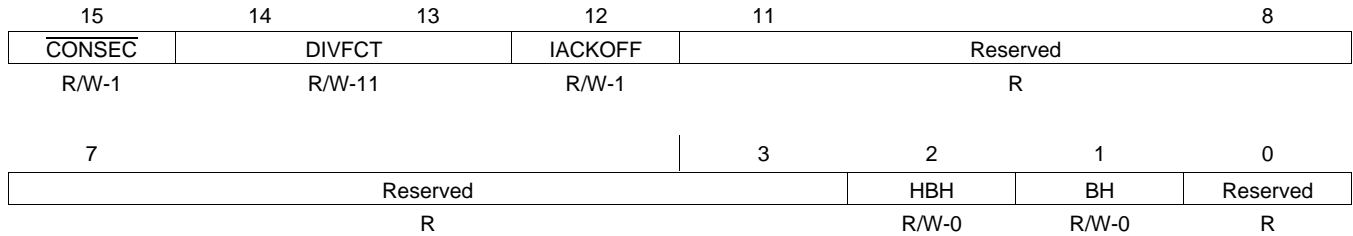
Table 3-4. Software Wait-State Control Register (SWCR) Field Descriptions

| BIT | FIELD | VALUE | DESCRIPTION |
|------|----------|-------|--|
| 15–1 | Reserved | | These bits are reserved and are unaffected by writes. |
| 0 | SWSM | | Software wait-state multiplier. Used to multiply the number of wait states defined in the SWWSR by a factor of 1 or 2. |
| | | 0 | Wait-state base values are unchanged (multiplied by 1). |
| | | 1 | Wait-state base values are multiplied by 2 for a maximum of 14 wait states. |

3.6.2 Programmable Bank-Switching

Programmable bank-switching logic allows the 5402A to switch between external memory banks without requiring external wait states for memories that need additional time to turn off. The bank-switching logic automatically inserts one cycle when accesses cross a 32K-word memory-bank boundary inside program or data space.

Bank-switching is defined by the bank-switching control register (BSCR), which is memory-mapped at address 0029h. The bit fields of the BSCR are shown in Figure 3-7 and are described in Table 3-5.



LEGEND: R = Read, W = Write, n = value at reset

Figure 3-7. Bank-Switching Control Register (BSCR) [MMR Address 0029h]

Table 3-5. Bank-Switching Control Register (BSCR) Field Descriptions

| BIT | FIELD | VALUE | DESCRIPTION |
|-------|-----------------------|-------|--|
| 15 | CONSEC ⁽¹⁾ | | Consecutive bank-switching. Specifies the bank-switching mode. |
| | | 0 | Bank-switching on 32K bank boundaries only. This bit is cleared if fast access is desired for continuous memory reads (i.e., no starting and trailing cycles between read cycles). |
| | | 1 | Consecutive bank switches on external memory reads. Each read cycle consists of 3 cycles: starting cycle, read cycle, and trailing cycle. |
| 14–13 | DIVFCT | | CLKOUT output divide factor. The CLKOUT output is driven by an on-chip source having a frequency equal to 1/(DIVFCT+1) of the DSP clock. |
| | | 00 | CLKOUT is not divided. |
| | | 01 | CLKOUT is divided by 2 from the DSP clock. |
| | | 10 | CLKOUT is divided by 3 from the DSP clock. |
| | | 11 | CLKOUT is divided by 4 from the DSP clock (default value following reset). |
| 12 | IACKOFF | | IACK signal output off. Controls the output of the IACK signal. IACKOFF is set to 1 at reset. |
| | | 0 | The IACK signal output off function is disabled. |
| | | 1 | The IACK signal output off function is enabled. |
| 11–3 | Reserved | | Reserved |
| 2 | HBH | | HPI bus holder. Controls the HPI bus holder. HBH is cleared to 0 at reset. |
| | | 0 | The bus holder is disabled except when HPI16=1. |
| | | 1 | The bus holder is enabled. When not driven, the HPI data bus, HD[7:0] is held in the previous logic level. |
| 1 | BH | | Bus holder. Controls the bus holder. BH is cleared to 0 at reset. |
| | | 0 | The bus holder is disabled. |
| | | 1 | The bus holder is enabled. When not driven, the data bus, D[15:0] is held in the previous logic level. |
| 0 | Reserved | | Reserved |

(1) For additional information, see Section 3.11 of this document.

The DSP has an internal register that holds the MSB of the last address used for a read or write operation in program or data space. In the non-consecutive bank switches ($\overline{\text{CONSEC}} = 0$), if the MSB of the address used for the current read does not match that contained in this internal register, the memory strobe ($\overline{\text{MSTRB}}$) signal is not asserted for one CLKOUT cycle. During this extra cycle, the address bus switches to the new address. The contents of the internal register are replaced with the MSB for the read of the current address. If the MSB of the address used for the current read matches the bits in the register, a normal read cycle occurs.

In non-consecutive bank switches ($\overline{\text{CONSEC}} = 0$), if repeated reads are performed from the same memory bank, no extra cycles are inserted. When a read is performed from a different memory bank, memory conflicts are avoided by inserting an extra cycle. For more information, see [Section 3.11](#) of this document.

The bank-switching mechanism automatically inserts one extra cycle in the following cases:

- A memory read followed by another memory read from a different memory bank.
- A program-memory read followed by a data-memory read.
- A data-memory read followed by a program-memory read.
- A program-memory read followed by another program-memory read from a different page.

3.6.3 Bus Holders

The device has two bus holder control bits, BH (BSCR[1]) and HBH (BSCR[2]), to control the bus keepers of the address bus (A[15–0]), data bus (D[15–0]), and the HPI data bus (HD[7–0]). Bus keeper enabling/disabling is described in [Table 3-6](#).

Table 3-6. Bus Holder Control Bits

| HPI16 PIN | BH | HBH | D[15–0] | A[15–0] | HD[7–0] |
|-----------|----|-----|---------|---------|---------|
| 0 | 0 | 0 | OFF | OFF | OFF |
| 0 | 0 | 1 | OFF | OFF | ON |
| 0 | 1 | 0 | ON | OFF | OFF |
| 0 | 1 | 1 | ON | OFF | ON |
| 1 | 0 | 0 | OFF | OFF | ON |
| 1 | 0 | 1 | OFF | ON | ON |
| 1 | 1 | 0 | ON | OFF | ON |
| 1 | 1 | 1 | ON | ON | ON |

3.7 Parallel I/O Ports

The 5402A has a total of 64K I/O ports. These ports can be addressed by the PORTR instruction or the PORTW instruction. The \overline{IS} signal indicates a read/write operation through an I/O port. The 5402A can interface easily with external devices through the I/O ports while requiring minimal off-chip address-decoding circuits.

3.7.1 Enhanced 8-/16-Bit Host-Port Interface (HPI8/16)

The 5402A host-port interface, also referred to as the HPI8/16, is an enhanced version of the standard 8-bit HPI found on earlier TMS320C54x™ DSPs (542, 545, 548, and 549). The 5402A HPI can be used to interface to an 8-bit or 16-bit host. When the address and data buses for external I/O is not used (to interface to external devices in program/data/IO spaces), the 5402A HPI can be configured as an HPI16 to interface to a 16-bit host. This configuration can be accomplished by connecting the HPI16 pin to logic "1".

When the HPI16 pin is connected to a logic "0", the 5402A HPI is configured as an HPI8. The HPI8 is an 8-bit parallel port for interprocessor communication. The features of the HPI8 include:

Standard features:

- Sequential transfers (with autoincrement) or random-access transfers
- Host interrupt and C54x™ interrupt capability
- Multiple data strobes and control pins for interface flexibility

The HPI8 interface consists of an 8-bit bidirectional data bus and various control signals. Sixteen-bit transfers are accomplished in two parts with the HBIL input designating high or low byte. The host communicates with the HPI8 through three dedicated registers — the HPI address register (HPIA), the HPI data register (HPID), and the HPI control register (HPIC). The HPIA and HPID registers are only accessible by the host, and the HPIC register is accessible by both the host and the 5402A.

Enhanced features:

- Access to entire on-chip RAM through DMA bus
- Capability to continue transferring during emulation stop

The HPI16 is an enhanced 16-bit version of the TMS320C54x™ DSP 8-bit host-port interface (HPI8). The HPI16 is designed to allow a 16-bit host to access the DSP on-chip memory, with the host acting as the master of the interface. Some of the features of the HPI16 include:

- 16-bit bidirectional data bus
- Multiple data strobes and control signals to allow glueless interfacing to a variety of hosts
- Only nonmultiplexed address/data modes are supported
- 15-bit address bus used in nonmultiplexed mode to allow access to all internal memory (including internal extended address pages)
- HRDY signal to hold off host accesses due to DMA latency
- The HPI16 acts as a slave to a 16-bit host processor and allows access to the on-chip memory of the DSP.

NOTE

Only the nonmultiplexed mode is supported when the 5402A HPI is configured as a HPI16 (see [Figure 3-8](#)).

The 5402A HPI functions as a slave and enables the host processor to access the on-chip memory. A major enhancement to the 5402A HPI over previous versions is that it allows host access to the entire on-chip memory range of the DSP. The host and the DSP both have access to the on-chip RAM at all times and host accesses are always synchronized to the DSP clock. If the host and the DSP contend for access to the same location, the host has priority, and the DSP waits for one cycle. Since host accesses are always synchronized to the 5402A clock, an active input clock (CLKIN) is required for HPI accesses during IDLE states, and host accesses are not allowed while the 5402A reset pin is asserted.

3.7.2 HPI Nonmultiplexed Mode

In *nonmultiplexed* mode, a host with separate address/data buses can access the HPI16 data register (HPID) via the HD 16-bit bidirectional data bus, and the address register (HPIA) via the 16-bit HA address bus. The host initiates the access with the strobe signals ($\overline{\text{HDS1}}$, $\overline{\text{HDS2}}$, $\overline{\text{HCS}}$) and controls the direction of the access with the $\overline{\text{HR/W}}$ signal. The HPI16 can stall host accesses via the $\overline{\text{HRDY}}$ signal. The HPIC register is not available in *nonmultiplexed* mode since there are no $\overline{\text{HCNTL}}$ signals available. All host accesses initiate a DMA read or write access. Figure 3-8 shows a block diagram of the HPI16 in *nonmultiplexed* mode.

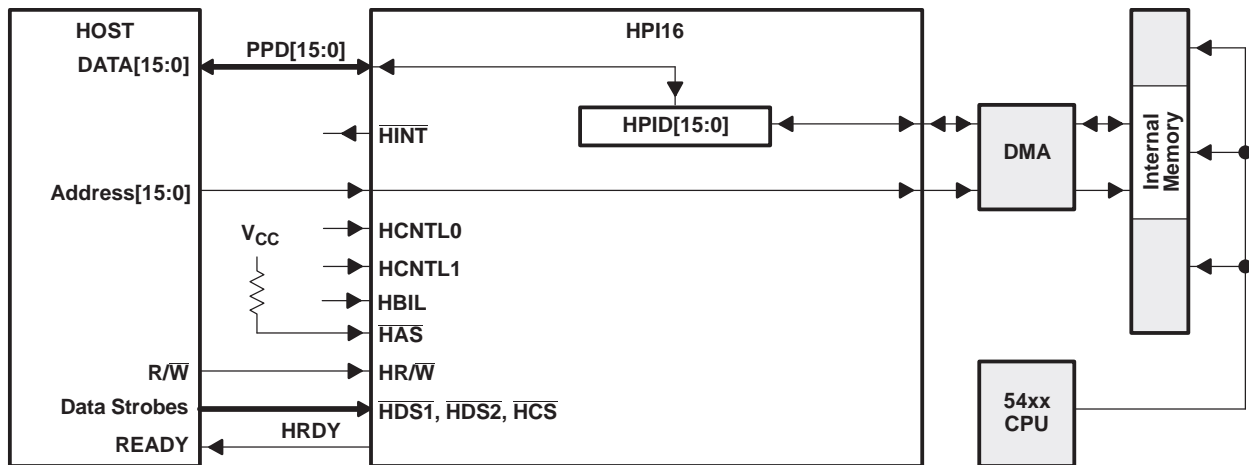


Figure 3-8. Host-Port Interface — Nonmultiplexed Mode

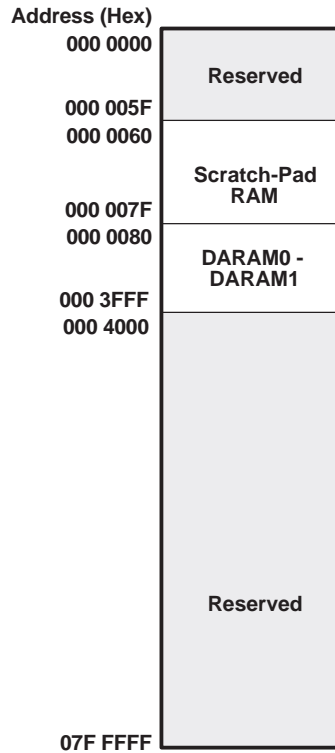


Figure 3-9. HPI Memory Map

3.8 Multichannel Buffered Serial Ports (McBSPs)

The 5402A device provides high-speed, full-duplex serial ports that allow direct interface to other C54x/LC54x devices, codecs, and other devices in a system. There are three multichannel buffered serial ports (McBSPs) on board (three per subsystem).

The McBSP provides:

- Full-duplex communication
- Double-buffer data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit

In addition, the McBSP has the following capabilities:

- Direct interface to:
 - T1/E1 framers
 - MVIP switching-compatible and ST-BUS compliant devices
 - IOM-2 compliant device
 - AC97-compliant device
 - Serial peripheral interface (SPI)
- Multichannel transmit and receive of up to 128 channels
- A wide selection of data sizes, including: 8, 12, 16, 20, 24, or 32 bits
- μ -law and A-law companding
- Programmable polarity for both frame synchronization and data clocks
- Programmable internal clock and frame generation

The 5402A McBSPs have been enhanced to provide more flexibility in the choice of the sample rate generator input clock source. On previous TMS320C5000™ DSP platform devices, the McBSP sample rate input clock can be driven from one of two possible choices: the internal CPU clock, or the external CLKS pin. However, most C5000™ DSP devices have only the internal CPU clock as a possible source because the CLKS pin is not implemented.

To accommodate applications that require an external reference clock for the sample rate generator, the 5402A McBSPs allow either the receive clock pin (BCLKR) or the transmit clock pin (BCLKX) to be configured as the input clock to the sample rate generator. This enhancement is enabled through two register bits: pin control register (PCR) bit 7 — enhanced sample clock mode (SCLKME), and sample rate generator register 2 (SRGR2) bit 13 — McBSP sample rate generator clock mode (CLKSM). SCLKME is an addition to the PCR contained in the McBSPs on previous C5000 devices. The new bit layout of the PCR is shown in [Figure 3-10](#). For a description of the remaining bits, see *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302).

| | | | | | | | |
|----------|-----------|---------|---------|--------|--------|--------|--------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | XIOEN | RIOEN | FSXM | FSRM | CLKXM | CLKRM |
| R, +0 | | R/W,+0 | R/W,+0 | R/W,+0 | R/W,+0 | R/W,+0 | R/W,+0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SCLKME | CLKS_STAT | DX_STAT | DR_STAT | FSXP | FSRP | CLKXP | CLKRP |
| R/W, +0 | R, +0 | R, +0 | R, +0 | R/W,+0 | R/W,+0 | R/W,+0 | R/W,+0 |

LEGEND: R = Read, W = Write, n = value at reset

Figure 3-10. Pin Control Register (PCR)

The selection of the sample rate generator (SRG) clock input source is made by the combination of the CLKSM and SCLKME bit values as shown in [Table 3-7](#).

Table 3-7. Sample Rate Generator Clock Source Selection

| SCLKME | CLKSM | SRG Clock Source |
|--------|-------|--|
| 0 | 0 | CLKS (not available as a pin on 5402A) |
| 0 | 1 | CPU clock |
| 1 | 0 | BCLKR pin |
| 1 | 1 | BCLKX pin |

When either of the bidirectional pins, BCLKR or BCLKX, is configured as the clock input, its output buffer is automatically disabled. For example, with SCLKME = 1 and CLKSM = 0, the BCLKR pin is configured as the SRG input. In this case, both the transmitter and receiver circuits can be synchronized to the SRG output by setting the PCR bits (9:8) for CLKXM = 1 and CLKRM = 1. However, the SRG output is only driven onto the BCLKX pin because the BCLKR output is automatically disabled.

The McBSP supports independent selection of multiple channels for the transmitter and receiver. When multiple channels are selected, each frame represents a time-division multiplexed (TDM) data stream. In using time-division multiplexed data streams, the CPU may only need to process a few of them. Thus, to save memory and bus bandwidth, multichannel selection allows independent enabling of particular channels for transmission and reception. Up to a maximum of 128 channels in a bit stream can be enabled or disabled.

The 5402A McBSPs have two working modes that are selected by setting the RMCME and XMCME bits in the multichannel control registers (MCR1x and MCR2x, respectively). See [Figure 3-11](#) and [Figure 3-12](#). For a description of the remaining bits, see *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302).

- In the first mode, when RMCME = 0 and XMCME = 0, there are two partitions (A and B), with each containing 16 channels as shown in Figure 3-11 and Figure 3-12. This is compatible with the McBSPs used in earlier TMS320C54x devices, where only 32-channel selection is enabled (default).

| | | | | | | | | |
|----------|---------|---|-------|----|---|---------|---------|---|
| 15 | | | | 10 | | 9 | 8 | |
| Reserved | | | | | | RMCME | RPBBLK | |
| R, +0 | | | | | | R/W, +0 | R/W, +0 | |
| 7 | | 6 | 5 | 4 | 2 | | 1 | 0 |
| RPBBLK | RPABLK | | RCBLK | | | RMCM | | |
| R/W, +0 | R/W, +0 | | R, +0 | | | R/W, +0 | | |

LEGEND: R = Read, W = Write, n = value at reset

Figure 3-11. Multichannel Control Register 1x (MCR1x)

| | | | | | | | | |
|----------|---------|---|-------|----|---|---------|---------|---|
| 15 | | | | 10 | | 9 | 8 | |
| Reserved | | | | | | XMCME | XPBBLK | |
| R, +0 | | | | | | R/W, +0 | R/W, +0 | |
| 7 | | 6 | 5 | 4 | 2 | | 1 | 0 |
| XPBBLK | XPABLK | | XCBLK | | | XMCM | | |
| R/W, +0 | R/W, +0 | | R, +0 | | | R, +0 | | |

LEGEND: R = Read, W = Write, n = value at reset

Figure 3-12. Multichannel Control Register 2x (MCR2x)

- In the second mode, with RMCME = 1 and XMCME = 1, the McBSPs have 128 channel selection capability. Twelve new registers (RCERCx–RCERHx and XCERCx–XCERHx) are used to enable the 128 channel selection. The subaddresses of the new registers are shown in Table 3-19. These new registers, functionally equivalent to the RCERA0–RCERB1 and XCERA0–XCERB1 registers in the 5420, are used to enable/disable the transmit and receive of additional channel partitions (C,D,E,F,G, and H) in the 128 channel stream. For example, XCERH1 is the transmit enable for channel partition H (channels 112 to 127) of McBSP1 for each DSP subsystem. See Figure 3-13, Table 3-8, Figure 3-14, and Table 3-9 for bit layout and function of the receive and transmit registers .

| | | | | | | | | |
|----------|----------|----------|----------|----------|----------|---------|---------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
| RCERYz15 | RCERYz14 | RCERYz13 | RCERYz12 | RCERYz11 | RCERYz10 | RCERYz9 | RCERYz8 | |
| RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | |
| 7 | | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RCERYz7 | RCERYz6 | RCERYz5 | RCERYz4 | RCERYz3 | RCERYz2 | RCERYz1 | RCERYz0 | |
| RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | |

LEGEND: R = Read, W = Write, n = value at reset

Figure 3-13. Receive Channel Enable Registers Bit Layout for Partitions A to H

Table 3-8. Receive Channel Enable Registers for Partitions A to H Field Descriptions

| BIT | FIELD | VALUE | DESCRIPTION |
|------|--------------|-------|---|
| 15–0 | RCERYz(15:0) | | Receive Channel Enable Register |
| | | 0 | Disables reception of <i>n</i> th channel in partition <i>y</i> . |
| | | 1 | Enables reception of <i>n</i> th channel in partition <i>y</i> . |

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|---------|---------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| XCERyz15 | XCERyz14 | XCERyz13 | XCERyz12 | XCERyz11 | XCERyz10 | XCERyz9 | XCERyz8 |
| RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XCERyz7 | XCERyz6 | XCERyz5 | XCERyz4 | XCERyz3 | XCERyz2 | XCERyz1 | XCERyz0 |
| RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 |

LEGEND: R = Read, W = Write, n = value at reset

Figure 3-14. Transmit Channel Enable Registers Bit Layout for Partitions A to H

Table 3-9. Transmit Channel Enable Registers for Partitions A to H Field Descriptions

| BIT | FIELD | VALUE | Description |
|------|--------------|-------|--|
| 15–0 | XCERyz(15:0) | | Transmit Channel Enable Register |
| | | 0 | Disables transmit of <i>n</i> th channel in partition <i>y</i> . |
| | | 1 | Enables transmit of <i>n</i> th channel in partition <i>y</i> . |

The clock stop mode (CLKSTP) in the McBSP provides compatibility with the serial port interface (SPI) protocol. Clock stop mode works with only single-phase frames and one word per frame. The word sizes supported by the McBSP are programmable for 8-, 12-, 16-, 20-, 24-, or 32-bit operation. When the McBSP is configured to operate in SPI mode, both the transmitter and the receiver operate together as a master or as a slave.

The McBSP is fully static and operates at arbitrarily low clock frequencies. The maximum McBSP multichannel operating frequency on the 5402A is 9 MBps. Nonmultichannel operation is limited to 38 MBps.

3.9 Hardware Timer

The device features two 16-bit timing circuits with 4-bit prescalers. The timer counters are decremented by one every CPU clock cycle. Each time the counter decrements to 0, a timer interrupt is generated. The timers can be stopped, restarted, reset, or disabled by specific status bits.

3.10 Clock Generator

The clock generator provides clocks to the device, and consists of a phase-locked loop (PLL) circuit. The clock generator requires a reference clock input, which can be provided from an external clock source. The reference clock input is then divided by two (DIV mode) to generate clocks, or the PLL circuit can be used (PLL mode) to generate the device clock by multiplying the reference clock frequency by a scale factor, allowing use of a clock source with a lower frequency than that of the CPU. The PLL is an adaptive circuit that, once synchronized, locks onto and tracks an input clock signal.

When the PLL is initially started, it enters a transitional mode during which the PLL acquires lock with the input signal. Once the PLL is locked, it continues to track and maintain synchronization with the input signal. Then, other internal clock circuitry allows the synthesis of new clock frequencies for use as master clock.

This clock generator allows system designers to select the clock source. The sources that drive the clock generator are:

- A crystal resonator circuit. The crystal resonator circuit is connected across the X1 and X2/CLKIN pins to enable the internal oscillator.
- An external clock. The external clock source is directly connected to the X2/CLKIN pin, and X1 is left unconnected.

NOTE

The crystal oscillator function is not supported by all die revisions of the 5402A device. See the *TMS320VC5402A Digital Signal Processor Silicon Errata* (literature number SPRZ018) to verify which die revisions support this functionality.

The software-programmable PLL features a high level of flexibility, and includes a clock scaler that provides various clock multiplier ratios, capability to directly enable and disable the PLL, and a PLL lock timer that can be used to delay switching to PLL clocking mode of the device until lock is achieved. Devices that have a built-in software-programmable PLL can be configured in one of two clock modes:

- PLL mode. The input clock (X2/CLKIN) is multiplied by 1 of 31 possible ratios.
- DIV (divider) mode. The input clock is divided by 2 or 4. Note that when DIV mode is used, the PLL can be completely disabled in order to minimize power dissipation.

The software-programmable PLL is controlled using the 16-bit memory-mapped (address 0058h) clock mode register (CLKMD). The CLKMD register is used to define the clock configuration of the PLL clock module. Upon reset, the CLKMD register is initialized with a predetermined value dependent only upon the state of the CLKMD1 – CLKMD3 pins. For more programming information, see the *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals* (literature number SPRU131). The CLKMD pin configured clock options are shown in [Table 3-10](#).

Table 3-10. Clock Mode Settings at Reset

| CLKMD1 | CLKMD2 | CLKMD3 | CLKMD RESET VALUE | CLOCK MODE ⁽¹⁾ |
|--------|--------|--------|-------------------|--|
| 0 | 0 | 0 | 0000h | 1/2 (PLL and Oscillator disabled) |
| 0 | 0 | 1 | 9007h | PLL x 10 (Oscillator enabled) |
| 0 | 1 | 0 | 4007h | PLL x 5 (Oscillator enabled) |
| 1 | 0 | 0 | 1007h | PLL x 2 (Oscillator enabled) |
| 1 | 1 | 0 | F007h | PLL x 1 (Oscillator enabled) |
| 1 | 1 | 1 | 0000h | 1/2 (PLL disabled, Oscillator enabled) |
| 1 | 0 | 1 | F000h | 1/4 (PLL disabled, Oscillator enabled) |
| 0 | 1 | 1 | — | Reserved (Bypass mode) |

- (1) The external CLKMD1–CLKMD3 pins are sampled to determine the desired clock generation mode while \overline{RS} is low. Following reset, the clock generation mode can be reconfigured by writing to the internal clock mode register in software. However, the oscillator enable/disable selection is performed independently of the state of \overline{RS} ; therefore, if CLKMD1–CLKMD3 are changed following reset, the oscillator enable/disable selection may change, but other aspects of the clock generation mode will not.

3.11 Enhanced External Parallel Interface (XIO2)

The 5402A external interface has been redesigned to include several improvements, including: simplification of the bus sequence, more immunity to bus contention when transitioning between read and write operations, the ability for external memory access to the DMA controller, and optimization of the power-down modes.

The bus sequence on the 5402A still maintains all of the same interface signals as on previous 54x devices, but the signal sequence has been simplified. Most external accesses now require 3 cycles composed of a leading cycle, an active (read or write) cycle, and a trailing cycle. The leading and trailing cycles provide additional immunity against bus contention when switching between read operations and write operations. To maintain high-speed read access, a consecutive read mode that performs single-cycle reads as on previous 54x devices is available.

Figure 3-15 shows the bus sequence for three cases: all I/O reads, memory reads in nonconsecutive mode, or single memory reads in consecutive mode. The accesses shown in Figure 3-15 always require 3 CLKOUT cycles to complete.

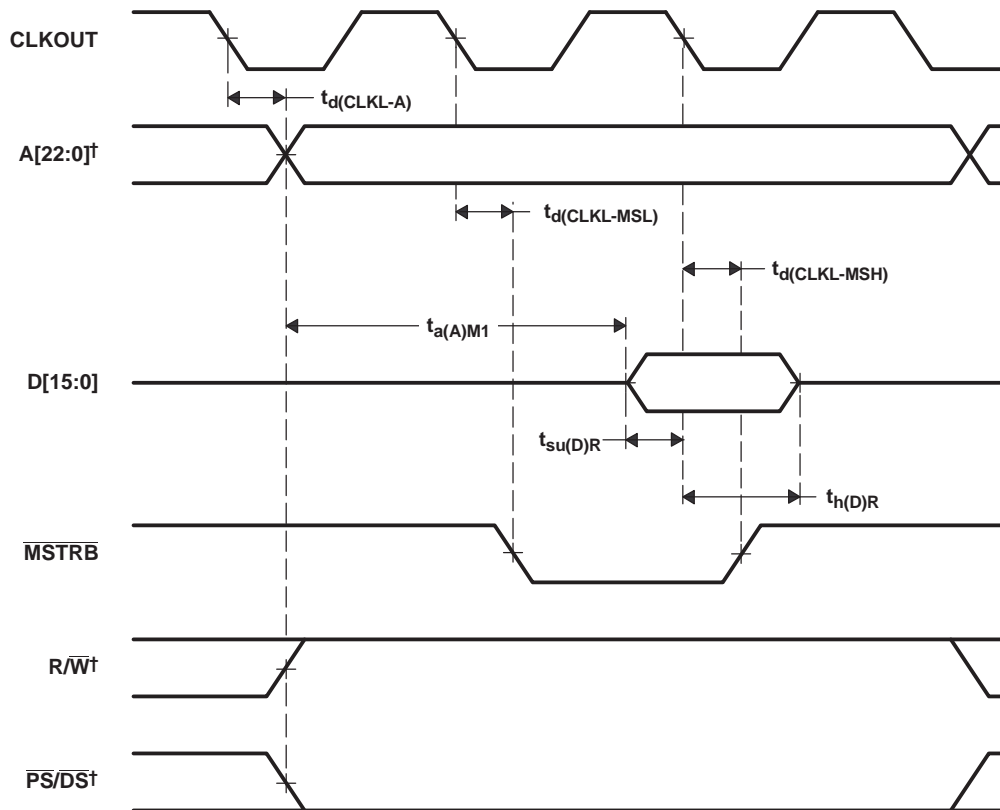


Figure 3-15. Nonconsecutive Memory Read and I/O Read Bus Sequence

Figure 3-16 shows the bus sequence for repeated memory reads in consecutive mode. The accesses shown in Figure 3-16 require $(2+n)$ CLKOUT cycles to complete, where n is the number of consecutive reads performed.

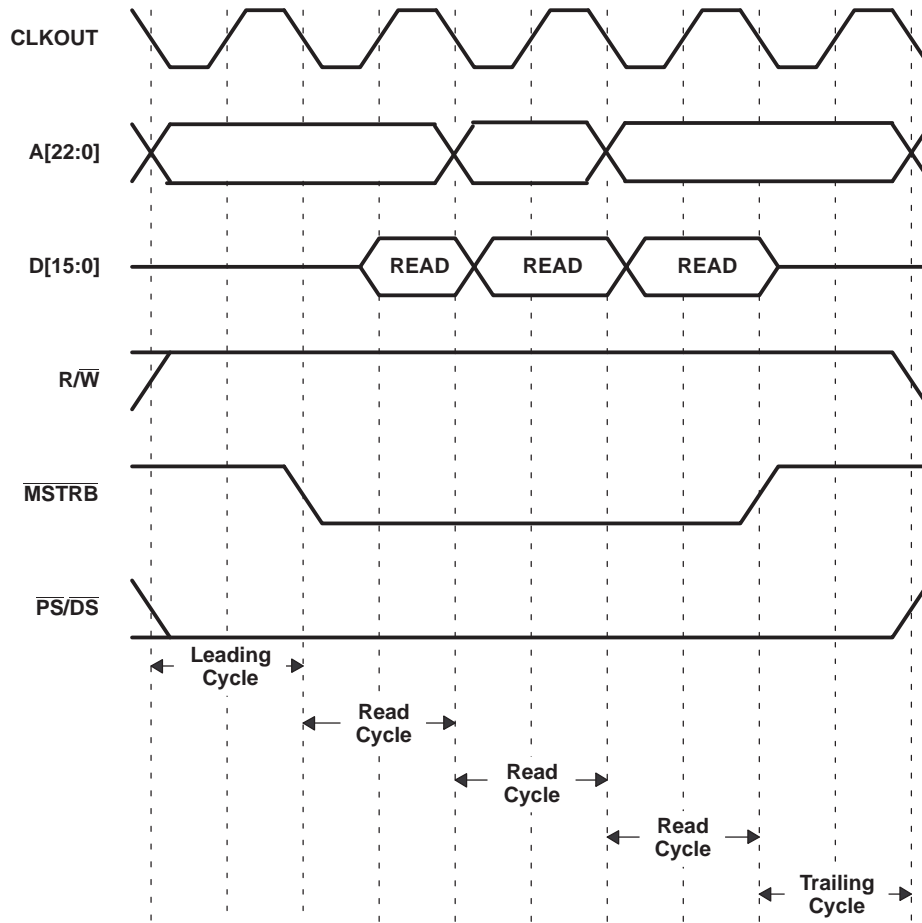


Figure 3-16. Consecutive Memory Read Bus Sequence ($n = 3$ reads)

Figure 3-17 shows the bus sequence for all memory writes and I/O writes. The accesses shown in Figure 3-17 always require 3 CLKOUT cycles to complete.

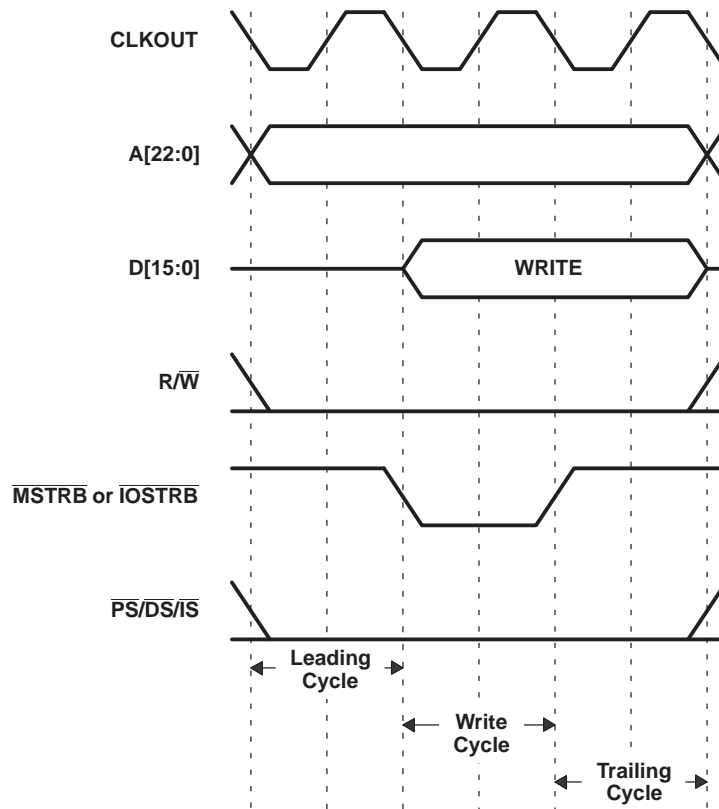


Figure 3-17. Memory Write and I/O Write Bus Sequence

The enhanced interface also provides the ability for DMA transfers to extend to external memory. For more information on DMA capability, see the DMA [Section 3.12](#).

The enhanced interface improves the low-power performance already present on the TMS320C5000™ DSP platform by switching off the internal clocks to the interface when it is not being used. This power-saving feature is automatic, requires no software setup, and causes no latency in the operation of the interface.

Additional features integrated in the enhanced interface are the ability to automatically insert bank-switching cycles when crossing 32K memory boundaries (see [Section 3.6.2](#)), the ability to program up to 14 wait states through software (see [Section 3.6.1](#)), and the ability to divide down CLKOUT by a factor of 1, 2, 3, or 4. Dividing down CLKOUT provides an alternative to wait states when interfacing to slower external memory or peripheral devices. While inserting wait states extends the bus sequence during read or write accesses, it does not slow down the bus signal sequences at the beginning and the end of the access. Dividing down CLKOUT provides a method of slowing the entire bus sequence when necessary. The CLKOUT divide-down factor is controlled through the DIVFCT field in the bank-switching control register (BSCR) (see [Figure 3-7](#)).

3.12 DMA Controller

The direct memory access (DMA) controller transfers data between points in the memory map without intervention by the CPU. The DMA allows movements of data to and from internal program/data memory, internal peripherals (such as the McBSPs), or external memory devices to occur in the background of CPU operation. The DMA has six independent programmable channels, allowing six different contexts for DMA operation.

3.12.1 Features

The DMA has the following features:

- The DMA operates independently of the CPU.
- The DMA has six channels. The DMA can keep track of the contexts of six independent block transfers.
- The DMA has higher priority than the CPU for both internal and external accesses.
- Each channel has independently programmable priorities.
- Each channel's source and destination address registers can have configurable indexes through memory on each read and write transfer, respectively. The address may remain constant, be post-incremented, be post-decremented, or be adjusted by a programmable value.
- Each read or write internal transfer may be initialized by selected events.
- On completion of a half- or entire-block transfer, each DMA channel may send an interrupt to the CPU.
- The DMA can perform double-word internal transfers (a 32-bit transfer of two 16-bit words).

3.12.2 DMA External Access

The DMA supports external accesses to extended program, extended data, and extended I/O memory. These overlay pages are only visible to the DMA controller. A maximum of two DMA channels can be used for external memory accesses. The DMA external accesses require a minimum of eight cycles for external writes and a minimum of nine cycles for external reads assuming the XIO02 is in consecutive mode ($\overline{\text{CONSEC}} = 1$), wait state is set to two, and CLKOUT is not divided ($\text{DIVFCT} = 00$).

The control of the bus is arbitrated between the CPU and the DMA. While the DMA or CPU is in control of the external bus, the other will be held-off via wait states until the current transfer is complete. The DMA takes precedence over XIO requests.

- Only two channels are available for external accesses. (One for external reads and one for external writes.)
- Single-word (16-bit) transfers are supported for external accesses.
- The DMA does not support transfers from the peripherals to external memory.
- The DMA does not support transfers from external memory to the peripherals.
- The DMA does not support external-to-external transfers.
- The DMA does not support synchronized external transfers.

3.12.3 DMPREC Issue

When updating the DE bits of the DMPREC register while one or more DMA channel transfers are in progress, it is possible for the write to the DMPREC to cause an additional transfer on one of the active channels.

The problem occurs when an active channel completes a transfer at the same time that the user updates the DMPREC register. When the transfer completes, the DMA logic attempts to clear the DE bit corresponding to the complete channel transfer, but the register is instead updated with the CPU write (usually an ORM instruction) which can set the bit and cause an additional transfer on the channel.

A hardware workaround has been implemented on this device. This solution consists of an additional memory mapped register, DMCECTL (DMA Channel Enable Control), at address 0x003E, with the following characteristics:

| | | | | | | | |
|-----------|----|----------|-----|-----|-----|-----|-----|
| 15 | 14 | | | | | | 8 |
| SET/RESET | | Reserved | | | | | |
| W-0 | | W-0 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
| W-0 | | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |

LEGEND: R = Read, W = Write, n = value at reset

Figure 3-19. DMA Channel Enable Control Register (DMCECTL)

Table 3-12. DMA Channel Enable Control Register (DMCECTL) Descriptions

| Bit | Field | Value | Description |
|------|-----------|-------|--|
| 15 | SET/RESET | | Sets or clears individual DE bits of the DMPREC register according to the values of CH0–CH5. |
| | | 0 | Clears the DE bits of the DMPREC register as specified by CH0–CH5. |
| | | 1 | Sets the DE bits of the DMPREC register as specified by CH0–CH5. |
| 14–6 | Reserved | | Reserved. |
| 5–0 | CH0–CH5 | | These bits are used in conjunction with the set/reset bit to write to the individual DE bits of the DMPREC register. |
| | | 0 | Corresponding DE bit in the DMPREC register is unaffected by the Set/Reset bit. |
| | | 1 | Corresponding bit in the DMPREC register is set or cleared depending on the state of Set/Reset. |

Use this register to enable or disable DMA channels instead of writing to the DMPREC register. For example, to enable channels zero and five, write a value of 0x8021 to address 0x03E. In this case only DE0 and DE5 of the DMPREC are set to 1. Or for another example, to disable channel one, write a value of 0x02 to address 0x03E. In this case only DE1 is cleared. This is a write-only register

3.12.4 DMA Memory Map

The DMA memory map, shown in Figure 3-20, allows the DMA transfer to be unaffected by the status of the MP/MC, DROM, and OVLY bits.

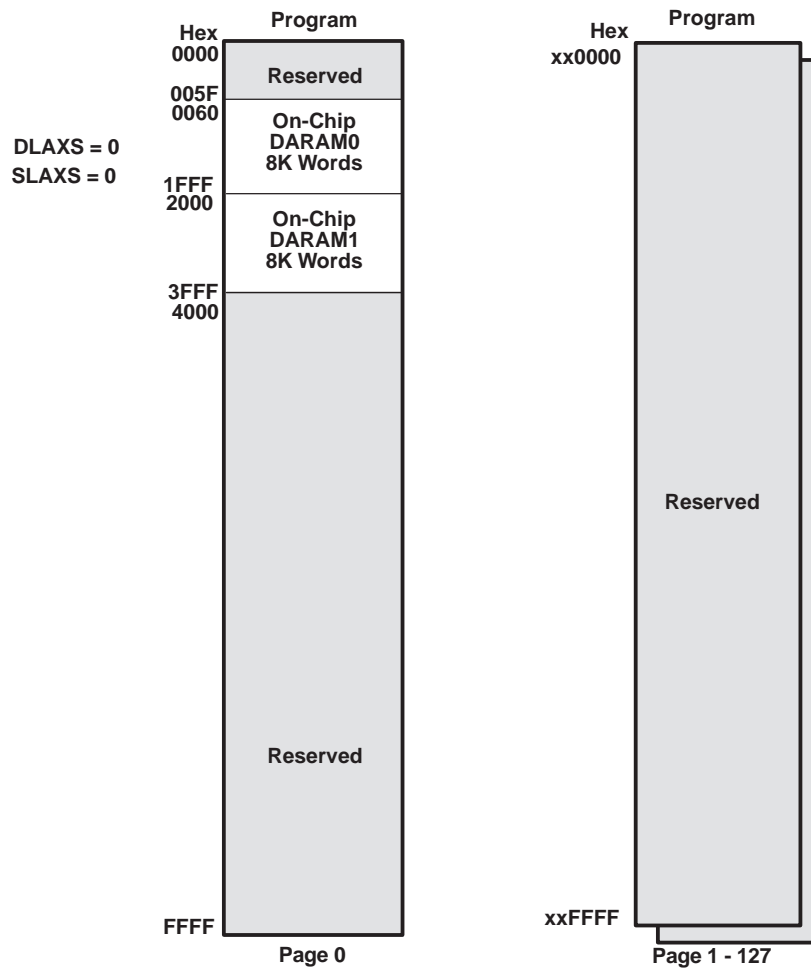


Figure 3-20. On-Chip DMA Memory Map for Program Space (DLAXS = 0 and SLAXS = 0)

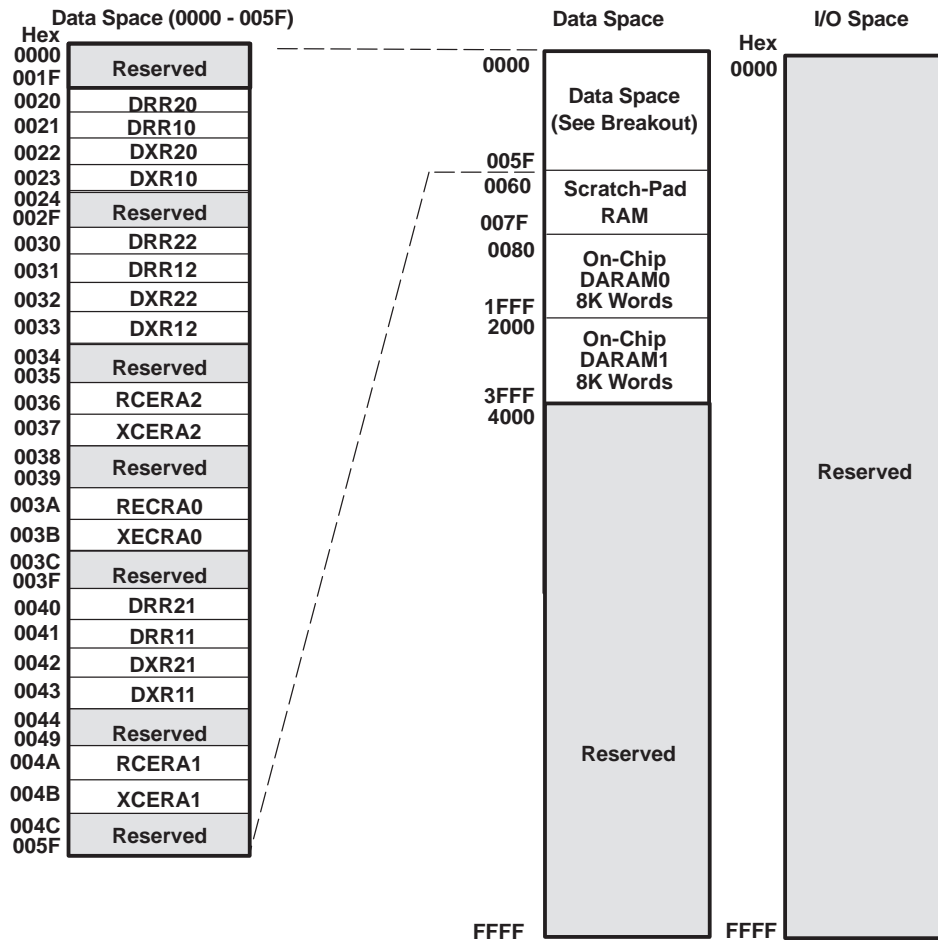


Figure 3-21. On-Chip DMA Memory Map for Data and IO Space (DLAXS = 0 and SLAXS = 0)

3.12.5 DMA Priority Level

Each DMA channel can be independently assigned high- or low-priority relative to each other. Multiple DMA channels that are assigned to the same priority level are handled in a round-robin manner.

3.12.6 DMA Source/Destination Address Modification

The DMA provides flexible address-indexing modes for easy implementation of data management schemes such as autobuffering and circular buffers. Source and destination addresses can be indexed separately and can be post-incremented, post-decremented, or post-incremented with a specified index offset.

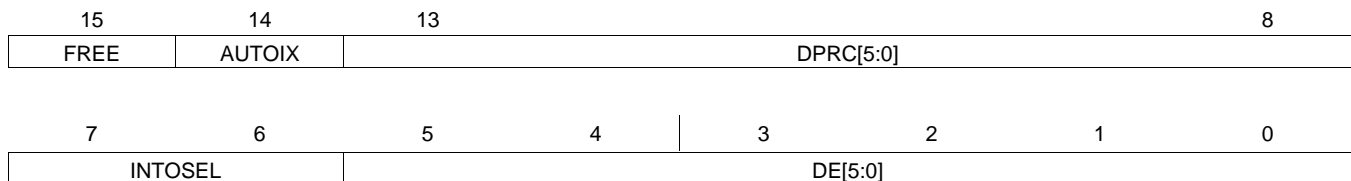
3.12.7 DMA in Autoinitialization Mode

The DMA can automatically reinitialize itself after completion of a block transfer. Some of the DMA registers can be preloaded for the next block transfer through the DMA reload registers (DMGSA, DMGDA, DMGCR, and DMGFR). Autoinitialization allows:

- Continuous operation: Normally, the CPU would have to reinitialize the DMA immediately after the completion of the current block transfers, but with the reload registers, it can reinitialize these values for the next block transfer any time after the current block transfer begins.
- Repetitive operation: The CPU does not preload the reload register with new values for each block transfer but only loads them on the first block transfer.

The 5402A DMA has been enhanced to expand the DMA reload register sets. Each DMA channel now has its own DMA reload register set. For example, the DMA reload register set for channel 0 has DMGSA0, DMGDA0, DMGCR0, and DMGFR0 while DMA channel 1 has DMGSA1, DMGDA1, DMGCR1, and DMGFR1, etc.

To utilize the additional DMA reload registers, the AUTOIX bit is added to the DMPREC register as shown in [Figure 3-22](#).



LEGEND: R = Read, W = Write, n = value at reset

Figure 3-22. DMPREC Register

Table 3-13. DMA Reload Register Selection

| AUTOIX | DMA RELOAD REGISTER USAGE IN AUTO INIT MODE |
|-------------|--|
| 0 (default) | All DMA channels use DMGSA0, DMGDA0, DMGCR0 and DMGFR0 |
| 1 | Each DMA channel uses its own set of reload registers |

3.12.8 DMA Transfer Counting

The DMA channel element count register (DMCTR_x) and the frame count register (DMFRC_x) contain bit fields that represent the number of frames and the number of elements per frame to be transferred.

- Frame count. This 8-bit value defines the total number of frames in the block transfer. The maximum number of frames per block transfer is 128 (FRAME COUNT= 0FFh). The counter is decremented upon the last read transfer in a frame transfer. Once the last frame is transferred, the selected 8-bit counter is reloaded with the DMA global frame reload register (DMGFR) if the AUTOINIT bit is set to 1. A frame count of 0 (default value) means the block transfer contains a single frame.
- Element count. This 16-bit value defines the number of elements per frame. This counter is decremented after the read transfer of each element. The maximum number of elements per frame is 65536 (DMCTR_n = 0FFFFh). In autoinitialization mode, once the last frame is transferred, the counter is reloaded with the DMA global count reload register (DMGCR).

3.12.9 DMA Transfer in Doubleword Mode

Doubleword mode allows the DMA to transfer 32-bit words in any index mode. In doubleword mode, two consecutive 16-bit transfers are initiated and the source and destination addresses are automatically updated following each transfer. In this mode, each 32-bit word is considered to be one element.

3.12.10 DMA Channel Index Registers

The particular DMA channel index register is selected by way of the SIND and DIND fields in the DMA transfer mode control register (DMMCRn). Unlike basic address adjustment, in conjunction with the frame index DMFRI0 and DMFRI1, the DMA allows different adjustment amounts depending on whether or not the element transfer is the last in the current frame. The normal adjustment value (element index) is contained in the element index registers DMIDX0 and DMIDX1. The adjustment value (frame index) for the end of the frame, is determined by the selected DMA frame index register, either DMFRI0 or DMFRI1.

The element index and the frame index affect address adjustment as follows:

- Element index: For all except the last transfer in the frame, the element index determines the amount to be added to the DMA channel for the source/destination address register (DMSRCx/DMDSTx) as selected by the SIND/DIND bits.
- Frame index: If the transfer is the last in a frame, frame index is used for address adjustment as selected by the SIND/DIND bits. This occurs in both single-frame and multiframe transfers.

3.12.11 DMA Interrupts

The ability of the DMA to interrupt the CPU based on the status of the data transfer is configurable and is determined by the IMOD and DINM bits in the DMA transfer mode control register (DMMCRn). The available modes are shown in [Table 3-14](#).

Table 3-14. DMA Interrupts

| MODE | DINM | IMOD | INTERRUPT |
|---------------------|------|------|--|
| ABU (non-decrement) | 1 | 0 | At full buffer only |
| ABU (non-decrement) | 1 | 1 | At half buffer and full buffer |
| Multiframe | 1 | 0 | At block transfer complete (DMCTRn = DMSEFCn[7:0] = 0) |
| Multiframe | 1 | 1 | At end of frame and end of block (DMCTRn = 0) |
| Either | 0 | X | No interrupt generated |
| Either | 0 | X | No interrupt generated |

3.12.12 DMA Controller Synchronization Events

The transfers associated with each DMA channel can be synchronized to one of several events. The DSYN bit field of the DMSEFCn register selects the synchronization event for a channel. The list of possible events and the DSYN values are shown in [Table 3-15](#).

Table 3-15. DMA Synchronization Events

| DSYN VALUE | DMA SYNCHRONIZATION EVENT |
|------------|-----------------------------------|
| 0000b | No synchronization used |
| 0001b | McBSP0 receive event |
| 0010b | McBSP0 transmit event |
| 0011b | McBSP2 receive event |
| 0100b | McBSP2 transmit event |
| 0101b | McBSP1 receive event |
| 0110b | McBSP1 transmit event |
| 0111b | McBSP0 receive event – ABIS mode |
| 1000b | McBSP0 transmit event – ABIS mode |
| 1001b | McBSP2 receive event – ABIS mode |
| 1010b | McBSP2 transmit event – ABIS mode |
| 1011b | McBSP1 receive event – ABIS mode |
| 1100b | McBSP1 transmit event – ABIS mode |
| 1101b | Timer interrupt event |
| 1110b | External interrupt 3 |
| 1111b | Reserved |

The DMA controller can generate a CPU interrupt for each of the six channels. However, due to a limit on the number of internal CPU interrupt inputs, channels 0, 1, 2, and 3 are multiplexed with other interrupt sources. DMA channels 0, 1, 2, and 3 share an interrupt line with the receive and transmit portions of the McBSP. When reset, the interrupts from these three DMA channels are deselected. The INTOSEL bit field in the DMPREC register can be used to select these interrupts, as shown in [Table 3-16](#).

Table 3-16. DMA Channel Interrupt Selection

| INTOSEL Value | IMR/IFR[6] | IMR/IFR[7] | IMR/IFR[10] | IMR/IFR[11] |
|---------------|------------|------------|-------------|-------------|
| 00b (reset) | BRINT2 | BXINT2 | BRINT1 | BXINT1 |
| 01b | BRINT2 | BXINT2 | DMAC2 | DMAC3 |
| 10b | DMAC0 | DMAC1 | DMAC2 | DMAC3 |
| 11b | Reserved | | | |

3.13 General-Purpose I/O Pins

In addition to the standard $\overline{\text{BIO}}$ and XF pins, the device has pins that can be configured for general-purpose I/O. These pins are:

- 18 McBSP pins — BCLKX0/1/2, BCLKR0/1/2, BDR0/1/2, BFSX0/1/2, BFSR0/1/2, BD0/1/2
- 8 HPI data pins — HD0–HD7

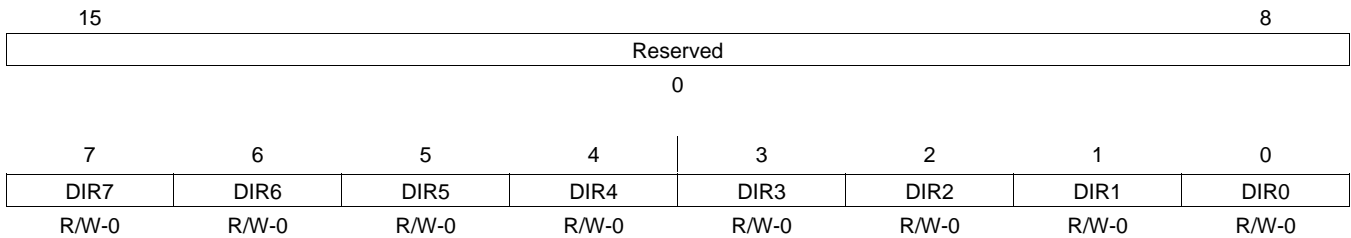
The general-purpose I/O function of these pins is only available when the primary pin function is not required.

3.13.1 McBSP Pins as General-Purpose I/O

When the receive or transmit portion of a McBSP is in reset, its pins can be configured as general-purpose inputs or outputs. For more details on this feature, see [Section 3.8](#).

3.13.2 HPI Data Pins as General-Purpose I/O

The 8-bit bidirectional data bus of the HPI can be used as general-purpose input/output (GPIO) pins when the HPI is disabled (HPIENA = 0) or when the HPI is used in HPI16 mode (HPI16 = 1). Two memory-mapped registers are used to control the GPIO function of the HPI data pins — the general-purpose I/O control register (GPIOCR) and the general-purpose I/O status register (GPIOSR). The GPIOCR is shown in [Figure 3-23](#).

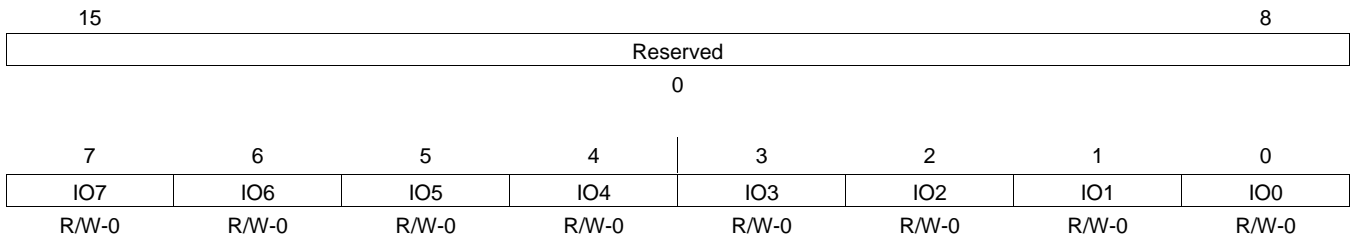


LEGEND: R = Read, W = Write, n = value at reset

Figure 3-23. General-Purpose I/O Control Register (GPIOCR) [MMR Address 003Ch]

The direction bits (DIRx) are used to configure HD0–HD7 as inputs or outputs.

The status of the GPIO pins can be monitored using the bits of the GPIOSR. The GPIOSR is shown in [Figure 3-24](#).



LEGEND: R = Read, W = Write, n = value at reset

Figure 3-24. General-Purpose I/O Status Register (GPIOSR) [MMR Address 003Dh]

3.14 Memory-Mapped Registers

The device provides 27 memory-mapped CPU registers, which are mapped in data memory space address 0h to 1Fh. Each device also has a set of memory-mapped registers associated with peripherals. [Table 3-17](#) gives a list of CPU memory-mapped registers (MMRs) available. [Table 3-18](#) shows additional peripheral MMRs associated with the device.

Table 3-17. CPU Memory-Mapped Registers

| NAME | ADDRESS | | DESCRIPTION |
|------|---------|-----|---------------------------------------|
| | DEC | HEX | |
| IMR | 0 | 0 | Interrupt mask register |
| IFR | 1 | 1 | Interrupt flag register |
| — | 2–5 | 2–5 | Reserved for testing |
| ST0 | 6 | 6 | Status register 0 |
| ST1 | 7 | 7 | Status register 1 |
| AL | 8 | 8 | Accumulator A low word (15–0) |
| AH | 9 | 9 | Accumulator A high word (31–16) |
| AG | 10 | A | Accumulator A guard bits (39–32) |
| BL | 11 | B | Accumulator B low word (15–0) |
| BH | 12 | C | Accumulator B high word (31–16) |
| BG | 13 | D | Accumulator B guard bits (39–32) |
| TREG | 14 | E | Temporary register |
| TRN | 15 | F | Transition register |
| AR0 | 16 | 10 | Auxiliary register 0 |
| AR1 | 17 | 11 | Auxiliary register 1 |
| AR2 | 18 | 12 | Auxiliary register 2 |
| AR3 | 19 | 13 | Auxiliary register 3 |
| AR4 | 20 | 14 | Auxiliary register 4 |
| AR5 | 21 | 15 | Auxiliary register 5 |
| AR6 | 22 | 16 | Auxiliary register 6 |
| AR7 | 23 | 17 | Auxiliary register 7 |
| SP | 24 | 18 | Stack pointer register |
| BK | 25 | 19 | Circular buffer size register |
| BRC | 26 | 1A | Block repeat counter |
| RSA | 27 | 1B | Block repeat start address |
| REA | 28 | 1C | Block repeat end address |
| PMST | 29 | 1D | Processor mode status (PMST) register |
| XPC | 30 | 1E | Extended program page register |
| — | 31 | 1F | Reserved |

Table 3-18. Peripheral Memory-Mapped Registers for Each DSP Subsystem

| NAME | ADDRESS | | DESCRIPTION |
|--------|---------|-------|---|
| | DEC | HEX | |
| DRR20 | 32 | 20 | McBSP 0 Data Receive Register 2 |
| DRR10 | 33 | 21 | McBSP 0 Data Receive Register 1 |
| DXR20 | 34 | 22 | McBSP 0 Data Transmit Register 2 |
| DXR10 | 35 | 23 | McBSP 0 Data Transmit Register 1 |
| TIM | 36 | 24 | Timer Register |
| PRD | 37 | 25 | Timer Period Register |
| TCR | 38 | 26 | Timer Control Register |
| — | 39 | 27 | Reserved |
| SWWSR | 40 | 28 | Software Wait-State Register |
| BSCR | 41 | 29 | Bank-Switching Control Register |
| — | 42 | 2A | Reserved |
| SWCR | 43 | 2B | Software Wait-State Control Register |
| HPIC | 44 | 2C | HPI Control Register (HMODE = 0 only) |
| — | 45–47 | 2D–2F | Reserved |
| DRR22 | 48 | 30 | McBSP 2 Data Receive Register 2 |
| DRR12 | 49 | 31 | McBSP 2 Data Receive Register 1 |
| DXR22 | 50 | 32 | McBSP 2 Data Transmit Register 2 |
| DXR12 | 51 | 33 | McBSP 2 Data Transmit Register 1 |
| SPSA2 | 52 | 34 | McBSP 2 Subbank Address Register ⁽¹⁾ |
| SPSD2 | 53 | 35 | McBSP 2 Subbank Data Register ⁽¹⁾ |
| — | 54–55 | 36–37 | Reserved |
| SPSA0 | 56 | 38 | McBSP 0 Subbank Address Register ⁽¹⁾ |
| SPSD0 | 57 | 39 | McBSP 0 Subbank Data Register ⁽¹⁾ |
| — | 58–59 | 3A–3B | Reserved |
| GPIOCR | 60 | 3C | General-Purpose I/O Control Register |
| GPIOSR | 61 | 3D | General-Purpose I/O Status Register |
| — | 62–63 | 3E–3F | Reserved |
| DRR21 | 64 | 40 | McBSP 1 Data Receive Register 2 |
| DRR11 | 65 | 41 | McBSP 1 Data Receive Register 1 |
| DXR21 | 66 | 42 | McBSP 1 Data Transmit Register 2 |
| DXR11 | 67 | 43 | McBSP 1 Data Transmit Register 1 |
| — | 68–71 | 44–47 | Reserved |
| SPSA1 | 72 | 48 | McBSP 1 Subbank Address Register ⁽¹⁾ |
| SPSD1 | 73 | 49 | McBSP 1 Subbank Data Register ⁽¹⁾ |
| — | 74–83 | 4A–53 | Reserved |
| DMPREC | 84 | 54 | DMA Priority and Enable Control Register |
| DMSA | 85 | 55 | DMA Subbank Address Register ⁽²⁾ |
| DMSDI | 86 | 56 | DMA Subbank Data Register with Autoincrement ⁽²⁾ |
| DMSDN | 87 | 57 | DMA Subbank Data Register ⁽²⁾ |
| CLKMD | 88 | 58 | Clock Mode Register (CLKMD) |
| — | 89–95 | 59–5F | Reserved |

(1) See [Table 3-19](#) for a detailed description of the McBSP control registers and their subaddresses.

(2) See [Table 3-20](#) for a detailed description of the DMA subbank addressed registers.

3.15 McBSP Control Registers and Subaddresses

The control registers for the multichannel buffered serial port (McBSP) are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The McBSP subbank address register (SPSA) is used as a pointer to select a particular register within the subbank. The McBSP data register (SPSDx) is used to access (read or write) the selected register. [Table 3-19](#) shows the McBSP control registers and their corresponding subaddresses.

Table 3-19. McBSP Control Registers and Subaddresses

| McBSP0 | | McBSP1 | | McBSP2 | | SUB-ADDRESS | DESCRIPTION |
|--------|---------|--------|---------|--------|---------|-------------|--|
| NAME | ADDRESS | NAME | ADDRESS | NAME | ADDRESS | | |
| SPCR10 | 39h | SPCR11 | 49h | SPCR12 | 35h | 00h | Serial port control register 1 |
| SPCR20 | 39h | SPCR21 | 49h | SPCR22 | 35h | 01h | Serial port control register 2 |
| RCR10 | 39h | RCR11 | 49h | RCR12 | 35h | 02h | Receive control register 1 |
| RCR20 | 39h | RCR21 | 49h | RCR22 | 35h | 03h | Receive control register 2 |
| XCR10 | 39h | XCR11 | 49h | XCR12 | 35h | 04h | Transmit control register 1 |
| XCR20 | 39h | XCR21 | 49h | XCR22 | 35h | 05h | Transmit control register 2 |
| SRGR10 | 39h | SRGR11 | 49h | SRGR12 | 35h | 06h | Sample rate generator register 1 |
| SRGR20 | 39h | SRGR21 | 49h | SRGR22 | 35h | 07h | Sample rate generator register 2 |
| MCR10 | 39h | MCR11 | 49h | MCR12 | 35h | 08h | Multichannel control register 1 |
| MCR20 | 39h | MCR21 | 49h | MCR22 | 35h | 09h | Multichannel control register 2 |
| RCERA0 | 39h | RCERA1 | 49h | RCERA2 | 35h | 0Ah | Receive channel enable register partition A |
| RCERB0 | 39h | RCERB1 | 49h | RCERA2 | 35h | 0Bh | Receive channel enable register partition B |
| XCERA0 | 39h | XCERA1 | 49h | XCERA2 | 35h | 0Ch | Transmit channel enable register partition A |
| XCERB0 | 39h | XCERB1 | 49h | XCERA2 | 35h | 0Dh | Transmit channel enable register partition B |
| PCR0 | 39h | PCR1 | 49h | PCR2 | 35h | 0Eh | Pin control register |
| RCERC0 | 39h | RCERC1 | 49h | RCERC2 | 35h | 010h | Additional channel enable register for 128-channel selection |
| RCERD0 | 39h | RCERD1 | 49h | RCERD2 | 35h | 011h | Additional channel enable register for 128-channel selection |
| XCERC0 | 39h | XCERC1 | 49h | XCERC2 | 35h | 012h | Additional channel enable register for 128-channel selection |
| XCERD0 | 39h | XCERD1 | 49h | XCERD2 | 35h | 013h | Additional channel enable register for 128-channel selection |
| RCERE0 | 39h | RCERE1 | 49h | RCERE2 | 35h | 014h | Additional channel enable register for 128-channel selection |
| RCERF0 | 39h | RCERF1 | 49h | RCERF2 | 35h | 015h | Additional channel enable register for 128-channel selection |
| XCERE0 | 39h | XCERE1 | 49h | XCERE2 | 35h | 016h | Additional channel enable register for 128-channel selection |
| XCERF0 | 39h | XCERF1 | 49h | XCERF2 | 35h | 017h | Additional channel enable register for 128-channel selection |
| RCERG0 | 39h | RCERG1 | 49h | RCERG2 | 35h | 018h | Additional channel enable register for 128-channel selection |
| RCERH0 | 39h | RCERH1 | 49h | RCERH2 | 35h | 019h | Additional channel enable register for 128-channel selection |
| XCERG0 | 39h | XCERG1 | 49h | XCERG2 | 35h | 01Ah | Additional channel enable register for 128-channel selection |
| XCERH0 | 39h | XCERH1 | 49h | XCERH2 | 35h | 01Bh | Additional channel enable register for 128-channel selection |

3.16 DMA Subbank Addressed Registers

The direct memory access (DMA) controller has several control registers associated with it. The main control register (DMPREC) is a standard memory-mapped register. However, the other registers are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The DMA subbank address (DMSA) register is used as a pointer to select a particular register within the subbank, while the DMA subbank data (DMSD) register or the DMA subbank data register with autoincrement (DMSDI) is used to access (read or write) the selected register.

When the DMSDI register is used to access the subbank, the subbank address is automatically postincremented so that a subsequent access affects the next register within the subbank. This autoincrement feature is intended for efficient, successive accesses to several control registers. If the autoincrement feature is not required, the DMSDN register should be used to access the subbank.

[Table 3-20](#) shows the DMA controller subbank addressed registers and their corresponding subaddresses.

Table 3-20. DMA Subbank Addressed Registers

| NAME | ADDRESS | SUB-ADDRESS | DESCRIPTION |
|--------|---------|-------------|---|
| DMSRC0 | 56h/57h | 00h | DMA channel 0 source address register |
| DMDST0 | 56h/57h | 01h | DMA channel 0 destination address register |
| DMCTR0 | 56h/57h | 02h | DMA channel 0 element count register |
| DMSFC0 | 56h/57h | 03h | DMA channel 0 sync select and frame count register |
| DMMCR0 | 56h/57h | 04h | DMA channel 0 transfer mode control register |
| DMSRC1 | 56h/57h | 05h | DMA channel 1 source address register |
| DMDST1 | 56h/57h | 06h | DMA channel 1 destination address register |
| DMCTR1 | 56h/57h | 07h | DMA channel 1 element count register |
| DMSFC1 | 56h/57h | 08h | DMA channel 1 sync select and frame count register |
| DMMCR1 | 56h/57h | 09h | DMA channel 1 transfer mode control register |
| DMSRC2 | 56h/57h | 0Ah | DMA channel 2 source address register |
| DMDST2 | 56h/57h | 0Bh | DMA channel 2 destination address register |
| DMCTR2 | 56h/57h | 0Ch | DMA channel 2 element count register |
| DMSFC2 | 56h/57h | 0Dh | DMA channel 2 sync select and frame count register |
| DMMCR2 | 56h/57h | 0Eh | DMA channel 2 transfer mode control register |
| DMSRC3 | 56h/57h | 0Fh | DMA channel 3 source address register |
| DMDST3 | 56h/57h | 10h | DMA channel 3 destination address register |
| DMCTR3 | 56h/57h | 11h | DMA channel 3 element count register |
| DMSFC3 | 56h/57h | 12h | DMA channel 3 sync select and frame count register |
| DMMCR3 | 56h/57h | 13h | DMA channel 3 transfer mode control register |
| DMSRC4 | 56h/57h | 14h | DMA channel 4 source address register |
| DMDST4 | 56h/57h | 15h | DMA channel 4 destination address register |
| DMCTR4 | 56h/57h | 16h | DMA channel 4 element count register |
| DMSFC4 | 56h/57h | 17h | DMA channel 4 sync select and frame count register |
| DMMCR4 | 56h/57h | 18h | DMA channel 4 transfer mode control register |
| DMSRC5 | 56h/57h | 19h | DMA channel 5 source address register |
| DMDST5 | 56h/57h | 1Ah | DMA channel 5 destination address register |
| DMCTR5 | 56h/57h | 1Bh | DMA channel 5 element count register |
| DMSFC5 | 56h/57h | 1Ch | DMA channel 5 sync select and frame count register |
| DMMCR5 | 56h/57h | 1Dh | DMA channel 5 transfer mode control register |
| DMSRCP | 56h/57h | 1Eh | DMA source program page address (common channel) |
| DMDSTP | 56h/57h | 1Fh | DMA destination program page address (common channel) |
| DMIDX0 | 56h/57h | 20h | DMA element index address register 0 |
| DMIDX1 | 56h/57h | 21h | DMA element index address register 1 |

Table 3-20. DMA Subbank Addressed Registers (continued)

| NAME | ADDRESS | SUB-ADDRESS | DESCRIPTION |
|---------|---------|-------------|---|
| DMFRI0 | 56h/57h | 22h | DMA frame index register 0 |
| DMFRI1 | 56h/57h | 23h | DMA frame index register 1 |
| DMGSA0 | 56h/57h | 24h | DMA global source address reload register, channel 0 |
| DMGDA0 | 56h/57h | 25h | DMA global destination address reload register, channel 0 |
| DMGCR0 | 56h/57h | 26h | DMA global count reload register, channel 0 |
| DMGFR0 | 56h/57h | 27h | DMA global frame count reload register, channel 0 |
| – | 56h/57h | 28h | Reserved |
| – | 56h/57h | 29h | Reserved |
| DMGSA1 | 56h/57h | 2Ah | DMA global source address reload register, channel 1 |
| DMGDA1 | 56h/57h | 2Bh | DMA global destination address reload register, channel 1 |
| DMGCR1 | 56h/57h | 2Ch | DMA global count reload register, channel 1 |
| DMGFR1 | 56h/57h | 2Dh | DMA global frame count reload register, channel 1 |
| DMGSA2 | 56h/57h | 2Eh | DMA global source address reload register, channel 2 |
| DMGDA2 | 56h/57h | 2Fh | DMA global destination address reload register, channel 2 |
| DMGCR2 | 56h/57h | 30h | DMA global count reload register, channel 2 |
| DMGFR2 | 56h/57h | 31h | DMA global frame count reload register, channel 2 |
| DMGSA3 | 56h/57h | 32h | DMA global source address reload register, channel 3 |
| DMGDA3 | 56h/57h | 33h | DMA global destination address reload register, channel 3 |
| DMGCR3 | 56h/57h | 34h | DMA global count reload register, channel 3 |
| DMGFR3 | 56h/57h | 35h | DMA global frame count reload register, channel 3 |
| DMGSA4 | 56h/57h | 36h | DMA global source address reload register, channel 4 |
| DMGDA4 | 56h/57h | 37h | DMA global destination address reload register, channel 4 |
| DMGCR4 | 56h/57h | 38h | DMA global count reload register, channel 4 |
| DMGFR4 | 56h/57h | 39h | DMA global frame count reload register, channel 4 |
| DMGSA5 | 56h/57h | 3Ah | DMA global source address reload register, channel 5 |
| DMGDA5 | 56h/57h | 3Bh | DMA global destination address reload register, channel 5 |
| DMGCR5 | 56h/57h | 3Ch | DMA global count reload register, channel 5 |
| DMGFR5 | 56h/57h | 3Dh | DMA global frame count reload register, channel 5 |
| DMCECTL | 56h/57h | 3Eh | DMA channel enable control register |

3.17 Interrupts

Vector-relative locations and priorities for all internal and external interrupts are shown in [Table 3-21](#).

Table 3-21. Interrupt Locations and Priorities

| NAME | TRAP/INTR NUMBER (K) | LOCATION DECIMAL HEX | | PRIORITY | FUNCTION |
|---------------------------|----------------------|----------------------|-------|----------|---------------------------------------|
| \overline{RS} , SINTR | 0 | 0 | 00 | 1 | Reset (hardware and software reset) |
| \overline{NMI} , SINT16 | 1 | 4 | 04 | 2 | Nonmaskable interrupt |
| SINT17 | 2 | 8 | 08 | — | Software interrupt #17 |
| SINT18 | 3 | 12 | 0C | — | Software interrupt #18 |
| SINT19 | 4 | 16 | 10 | — | Software interrupt #19 |
| SINT20 | 5 | 20 | 14 | — | Software interrupt #20 |
| SINT21 | 6 | 24 | 18 | — | Software interrupt #21 |
| SINT22 | 7 | 28 | 1C | — | Software interrupt #22 |
| SINT23 | 8 | 32 | 20 | — | Software interrupt #23 |
| SINT24 | 9 | 36 | 24 | — | Software interrupt #24 |
| SINT25 | 10 | 40 | 28 | — | Software interrupt #25 |
| SINT26 | 11 | 44 | 2C | — | Software interrupt #26 |
| SINT27 | 12 | 48 | 30 | — | Software interrupt #27 |
| SINT28 | 13 | 52 | 34 | — | Software interrupt #28 |
| SINT29 | 14 | 56 | 38 | — | Software interrupt #29 |
| SINT30 | 15 | 60 | 3C | — | Software interrupt #30 |
| $\overline{INT0}$, SINT0 | 16 | 64 | 40 | 3 | External user interrupt #0 |
| $\overline{INT1}$, SINT1 | 17 | 68 | 44 | 4 | External user interrupt #1 |
| $\overline{INT2}$, SINT2 | 18 | 72 | 48 | 5 | External user interrupt #2 |
| TINT, SINT3 | 19 | 76 | 4C | 6 | Timer interrupt |
| RINT0, SINT4 | 20 | 80 | 50 | 7 | McBSP #0 receive interrupt (default) |
| XINT0, SINT5 | 21 | 84 | 54 | 8 | McBSP #0 transmit interrupt (default) |
| RINT2, SINT6 | 22 | 88 | 58 | 9 | McBSP #2 receive interrupt (default) |
| XINT2, SINT7 | 23 | 92 | 5C | 10 | McBSP #2 transmit interrupt (default) |
| $\overline{INT3}$, SINT8 | 24 | 96 | 60 | 11 | External user interrupt #3 |
| \overline{HINT} , SINT9 | 25 | 100 | 64 | 12 | HPI interrupt |
| RINT1, SINT10 | 26 | 104 | 68 | 13 | McBSP #1 receive interrupt (default) |
| XINT1, SINT11 | 27 | 108 | 6C | 14 | McBSP #1 transmit interrupt (default) |
| DMAC4,SINT12 | 28 | 112 | 70 | 15 | DMA channel 4 (default) |
| DMAC5,SINT13 | 29 | 116 | 74 | 16 | DMA channel 5 (default) |
| Reserved | 30–31 | 120–127 | 78–7F | — | Reserved |

The bit layout of the interrupt flag register (IFR) and the interrupt mask register (IMR) is shown in [Figure 3-25](#).

| | | | | | | | |
|----------|-------|-------|-------|-------|-------------------|-------------------|-------------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | DMAC5 | DMAC4 | XINT1 | RINT1 | \overline{HINT} | $\overline{INT3}$ |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XINT2 | RINT2 | XINT0 | RINT0 | TINT | $\overline{INT2}$ | $\overline{INT1}$ | $\overline{INT0}$ |

LEGEND: R = Read, W = Write, n = value at reset

Figure 3-25. IFR and IMR

4 Support

4.1 Documentation Support

Extensive documentation supports all TMS320™ DSP family of devices from product announcement through applications development. The following types of documentation are available to support the design and use of the C5000™ platform of DSPs:

SPRU307: [TMS320C54x DSP Family Functional Overview](#)

Provides a functional overview of the devices included in the TMS320C54x™ DSP generation of digital signal processors. Included are descriptions of the CPU architecture, bus structure, memory structure, on-chip peripherals, and instruction set.

SPRA164: [Calculation of TMS320LC54x Power Dissipation](#)

Describes the power-saving features of the TMS320LC54x and presents techniques for analyzing systems and device conditions to determine operating current levels and power dissipation. From this information, informed decisions can be made regarding power supply requirements and thermal management considerations.

The five-volume *TMS320C54x DSP Reference Set* consists of:

SPRU131: [TMS320C54x DSP Reference Set, Volume 1: CPU](#)

Describes the TMS320C54x 16-bit fixed-point general-purpose digital signal processors. Covered are its architecture, internal register structure, data and program addressing, and the instruction pipeline. Also includes development support information, parts lists, and design considerations for using the XDS510 emulator.

SPRU172: [TMS320C54x DSP Reference Set, Volume 2: Mnemonic Instruction Set](#)

Describes the TMS320C54x digital signal processor mnemonic instructions individually. Also includes a summary of instruction set classes and cycles.

SPRU179: [TMS320C54x DSP Reference Set, Volume 3: Algebraic Instruction Set](#)

Describes the TMS320C54x digital signal processor algebraic instructions individually. Also includes a summary of instruction set classes and cycles.

SPRU173: [TMS320C54x DSP Reference Set, Volume 4: Applications Guide](#)

Describes software and hardware applications for the TMS320C54x digital signal processor. Also includes development support information, parts lists, and design considerations for using the XDS510 emulator.

SPRU302: [TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals](#)

Describes the enhanced peripherals available on the TMS320C54x digital signal processors. Includes the multichannel buffered serial ports (McBSPs), direct memory access (DMA) controller, interprocessor communications, and the HPI-8 and HPI-16 host port interfaces.

The reference set describes in detail the TMS320C54x™ DSP products currently available and the hardware and software applications, including algorithms, for fixed-point TMS320™ DSP family of devices.

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320 DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320 DSP customers on product information.

Information regarding TI DSP products is also available on the web at www.ti.com.

4.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320 DSP devices and support tools. Each TMS320 DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., TMS320C6412GDK600). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

- TMX** Experimental device that is not necessarily representative of the final device's electrical specifications
- TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
- TMS** Fully qualified production device

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped with appropriate disclaimers describing their limitations and intended uses.

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

5 Specification

This section provides the absolute maximum ratings and the recommended operating conditions for the TMS320VC5402A DSP.

5.1 Absolute Maximum Ratings

The list of absolute maximum ratings are specified over operating case temperature. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3.1](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

| | | |
|-----------|----------------------------------|------------------|
| DV_{DD} | Supply voltage I/O range | – 0.3 V to 4.0 V |
| CV_{DD} | Supply voltage core range | – 0.3 V to 2.0 V |
| V_I | Input voltage range | – 0.3 V to 4.5 V |
| V_O | Output voltage range | – 0.3 V to 4.5 V |
| T_C | Operating case temperature range | – 40°C to 100°C |
| T_{stg} | Storage temperature range | – 55°C to 150°C |

5.2 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT | |
|--------------------------|---|---|-----|------|-----------------|---|
| DV_{DD} | Device supply voltage, I/O | 2.7 | 3.3 | 3.6 | V | |
| CV_{DD} | Device supply voltage, core | 1.55 | 1.6 | 1.65 | V | |
| DV_{SS} , CV_{SS} | Supply voltage, GND | | 0 | | V | |
| V_{IH} | High-level input voltage, I/O | RS, INTn, NMI, X2/CLKIN, CLKMDn, BCLKRn, BCLKXn, HCS, HDS1, HDS2, HAS, TRST, TCK, BIO, Dn, An, HDn(DV_{DD} = 2.7 V to 3.6 V) | | 2.4 | $DV_{DD} + 0.3$ | V |
| | | All other inputs | | 2 | $DV_{DD} + 0.3$ | |
| V_{IL} | Low-level input voltage | -0.3 | | 0.8 | V | |
| I_{OH} | High-level output current ⁽¹⁾⁽²⁾ | | | -8 | mA | |
| I_{OL} | Low-level output current ⁽¹⁾⁽²⁾ | | | 8 | mA | |
| T_C | Operating case temperature | -40 | | 100 | °C | |

(1) The maximum output currents are DC values only. Transient currents may exceed these values.

(2) These output current limits are used for the test conditions on V_{OL} and V_{OH} , except where noted otherwise..

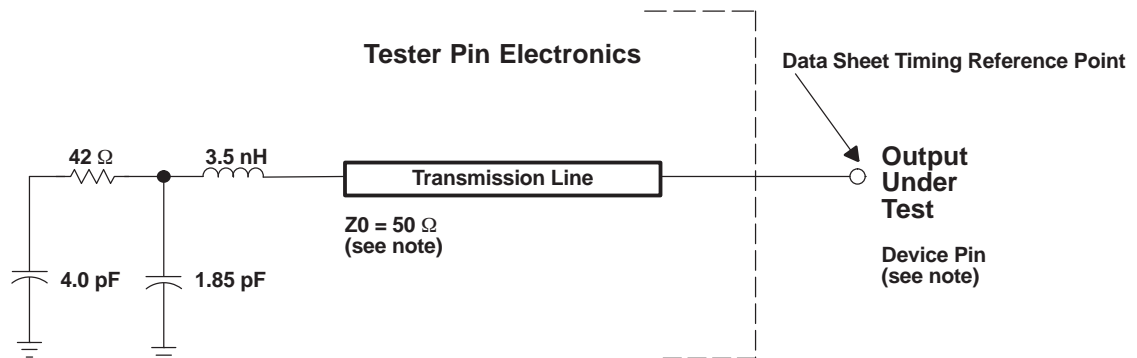
5.3 Electrical Characteristics Over Recommended Operating Case Temperature Range (Unless Otherwise Noted)

| PARAMETER | | TEST CONDITIONS | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX | UNIT |
|------------------|--|--|---|--------------------|------------------|-------------------|
| V _{OH} | High-level output voltage | (DV _{DD} = 2.7 V to 3.0 V), I _{OH} = -2 mA | 2.2 | | | V |
| | | (DV _{DD} = 3.0 V to 3.6 V), I _{OH} = MAX | 2.4 | | | |
| V _{OL} | Low-level output voltage ⁽¹⁾ | I _{OL} = MAX | | | 0.4 | V |
| I _{Iz} | Input current in high impedance | A[15:0] | DV _{DD} = MAX, V _O = DV _{SS} to DV _{DD} | - 275 | 275 | μA |
| I _I | Input current (V _I = DV _{SS} to DV _{DD}) | X2/CLKIN | | - 40 | 40 | μA |
| | | TRST, HPI16 | With internal pulldown | - 10 | 800 | |
| | | HPIENA | With internal pulldown, RS = 0 | - 10 | 400 | |
| | | TMS, TCK, TDI, HPI ⁽³⁾ | With internal pullups | - 400 | 10 | |
| | | D[15:0], HD[7:0] | Bus holders enabled, DV _{DD} = MAX ⁽⁴⁾ | - 275 | 275 | |
| | | All other input-only pins | | - 5 | 5 | |
| I _{DCC} | Supply current, core CPU | CV _{DD} = 1.6 V, f _x = 160, ⁽⁵⁾ T _C = 25°C | | 60 ⁽⁶⁾ | | mA |
| I _{DDP} | Supply current, pins | DV _{DD} = 3.0 V, f _x = 160 MHz, ⁽⁵⁾ T _C = 25°C | | 40 ⁽⁷⁾ | | mA ⁽⁴⁾ |
| I _{DD} | Supply current, standby | IDLE2 | PLL × 1 mode, 20 MHz input | | 2 | mA |
| | | IDLE3 divide-by-two mode, CLKIN stopped | T _C = 25°C | | 1 ⁽⁸⁾ | |
| | | | T _C = 100°C | | 30 | |
| C _i | Input capacitance | | | 5 | | pF |
| C _o | Output capacitance | | | 5 | | pF |

- (1) All input and output voltage levels except RS, INT0–INT3, NMI, X2/CLKIN, CLKMD1–CLKMD3, BCLKRn, BCLKXn, HCS, HAS, HDS1, HDS2, BIO, TCK, TRST, Dn, An, HDn are LVTTTL-compatible.
- (2) All values are typical unless otherwise specified.
- (3) HPI input signals except for HPIENA and HPI16, when HPIENA = 0.
- (4) V_{IL(MIN)} ≤ V_I ≤ V_{IL(MAX)} or V_{IH(MIN)} ≤ V_I ≤ V_{IH(MAX)}
- (5) Clock mode: PLL × 1 with external source
- (6) This value was obtained with 50% usage of MAC and 50% usage of NOP instructions. Actual operating current varies with program being executed.
- (7) This value was obtained with single-cycle external writes, CLKOFF = 0 and load = 15 pF. For more details on how this calculation is performed, refer to the *Calculation of TMS320LC54x Power Dissipation* application report (literature number SPRA164).
- (8) Material with high I_{DD} has been observed with a typical I_{DD} value of 5 to 10 mA during high temperature testing.

5.3.1 Test Load Circuit

The test load circuit shown in Figure 5-1 is used to measure all switching characteristics.



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 5-1. Tester Pin Electronics

5.3.2 Timing Parameter Symbology

Timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:

| | |
|-----|--|
| a | access time |
| c | cycle time (period) |
| d | delay time |
| dis | disable time |
| en | enable time |
| f | fall time |
| h | hold time |
| r | rise time |
| su | setup time |
| t | transition time |
| v | valid time |
| w | pulse duration (width) |
| X | Unknown, changing, or don't care level |

Letters and symbols and their meanings:

| | |
|---|----------------|
| H | High |
| L | Low |
| V | Valid |
| Z | High impedance |

5.3.3 Internal Oscillator With External Crystal

The internal oscillator is enabled by selecting the appropriate clock mode at reset (this is device-dependent; see [Section 3.10](#)) and connecting a crystal or ceramic resonator across X1 and X2/CLKIN. The CPU clock frequency is one-half, one-fourth, or a multiple of the oscillator frequency. The multiply ratio is determined by the bit settings in the CLKMD register.

The crystal should be in fundamental-mode operation, and parallel resonant, with an effective series resistance of 30Ω maximum and power dissipation of 1 mW. The connection of the required circuit, consisting of the crystal and two load capacitors, is shown in [Figure 5-2](#). The load capacitors, C₁ and C₂, should be chosen such that the equation below is satisfied. C_L (recommended value: 10 pF) in the equation is the load specified for the crystal.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

Table 5-1. Input Clock Frequency Characteristics

| | MIN | MAX | UNIT |
|--------------------------------------|-------------------|-------------------|------|
| f _x Input clock frequency | 10 ⁽¹⁾ | 20 ⁽²⁾ | MHz |

- (1) This device utilizes a fully static design and therefore can operate with t_{c(CI)} approaching ∞. The device is characterized at frequencies approaching 0 Hz
- (2) It is recommended that the PLL multiply-by-N clocking option be used for maximum frequency operation.

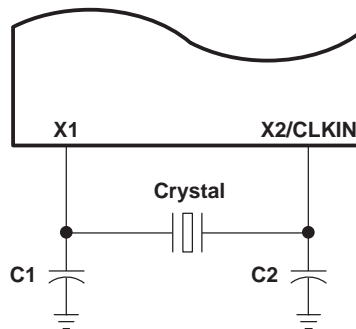


Figure 5-2. Internal Divide-By-Two Clock Option With External Crystal

5.3.4 Clock Options

The frequency of the reference clock provided at the CLKIN pin can be divided by a factor of two or four or multiplied by one of several values to generate the internal machine cycle.

5.3.4.1 Divide-By-Two and Divide-By-Four Clock Options

The frequency of the reference clock provided at the X2/CLKIN pin can be divided by a factor of two or four to generate the internal machine cycle. The selection of the clock mode is described in [Section 3.10](#).

When an external clock source is used, the frequency injected must conform to specifications listed in [Table 5-3](#).

An external frequency source can be used by applying an input clock to X2/CLKIN with X1 left unconnected.

[Table 5-2](#) shows the configuration options for the CLKMD pins that generate the external divide-by-2 or divide-by-4 clock option.

Table 5-2. Clock Mode Pin Settings for the Divide-By-2 and Divide-By-4 Clock Options

| CLKMD1 | CLKMD2 | CLKMD3 | Clock Mode |
|--------|--------|--------|-------------------|
| 0 | 0 | 0 | 1/2, PLL disabled |
| 1 | 0 | 1 | 1/4, PLL disabled |
| 1 | 1 | 1 | 1/2, PLL disabled |

[Table 5-3](#) and [Table 5-4](#) assume testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see [Figure 5-3](#)).

Table 5-3. Divide-By-2 and Divide-By-4 Clock Options Timing Requirements

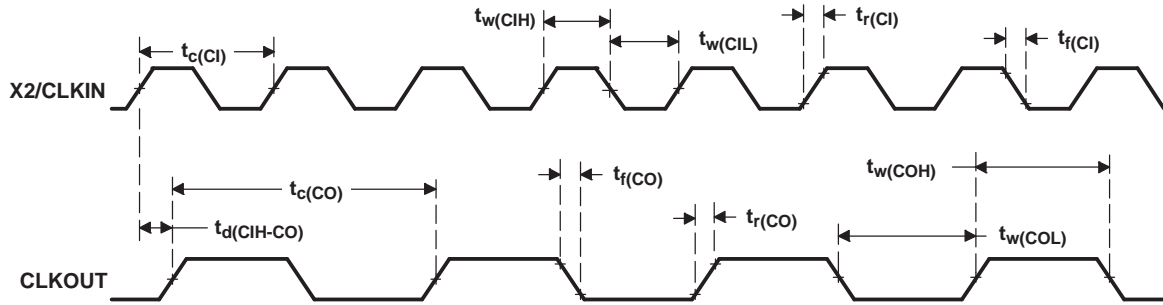
| | | MIN | MAX | UNIT |
|--------------|-------------------------------|-----|-----|------|
| $t_{c(CI)}$ | Cycle time, X2/CLKIN | 20 | | ns |
| $t_{f(CI)}$ | Fall time, X2/CLKIN | | 4 | ns |
| $t_{r(CI)}$ | Rise time, X2/CLKIN | | 4 | ns |
| $t_{w(CIL)}$ | Pulse duration, X2/CLKIN low | 4 | | ns |
| $t_{w(CIH)}$ | Pulse duration, X2/CLKIN high | 4 | | ns |

Table 5-4. Divide-By-2 and Divide-By-4 Clock Options Switching Characteristics

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-----------------|--|---------------------|-----|----------------|------|
| $t_{c(CO)}$ | Cycle time, CLKOUT | 6.25 ⁽¹⁾ | | ⁽²⁾ | ns |
| $t_{d(CIH-CO)}$ | Delay time, X2/CLKIN high to CLKOUT high/low | 4 | 7 | 11 | ns |
| $t_{f(CO)}$ | Fall time, CLKOUT | | 1 | | ns |
| $t_{r(CO)}$ | Rise time, CLKOUT | | 1 | | ns |
| $t_{w(COL)}$ | Pulse duration, CLKOUT low | H - 3 | H | H + 3 | ns |
| $t_{w(COH)}$ | Pulse duration, CLKOUT high | H - 3 | H | H + 3 | ns |

(1) It is recommended that the PLL clocking option be used for maximum frequency operation.

(2) This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞ . The device is characterized at frequencies approaching 0 Hz.



- A. The CLKOUT timing in this diagram assumes the CLKOUT divide factor (DIVFCT field in the BSCR) is configured as 00 (CLKOUT not divided). DIVFCT is configured as CLKOUT divided-by-4 mode following reset.

Figure 5-3. External Divide-By-Two Clock Timing

5.3.4.2 Multiply-By-N Clock Option (PLL Enabled)

The frequency of the reference clock provided at the X2/CLKIN pin can be multiplied by a factor of N to generate the internal machine cycle. The selection of the clock mode and the value of N is described in Section 3.10. Following reset, the software PLL can be programmed for the desired multiplication factor. Refer to the *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals* (literature number SPRU131) for detailed information on programming the PLL.

When an external clock source is used, the external frequency injected must conform to specifications listed in Table 5-5.

Table 5-5 and Table 5-6 assume testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 5-4).

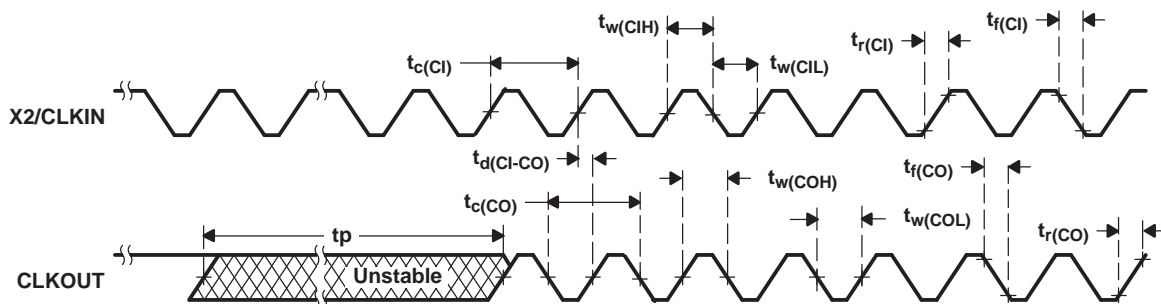
Table 5-5. Multiply-By-N Clock Option Timing Requirements

| | | MIN | MAX | UNIT |
|--------------|-------------------------------|--|-----|------|
| $t_{c(CI)}$ | Cycle time, X2/CLKIN | Integer PLL multiplier N (N = 1–15) ⁽¹⁾ | | ns |
| | | PLL multiplier N = x.5 ⁽¹⁾ | | |
| | | PLL multiplier N = x.25, x.75 ⁽¹⁾ | | |
| $t_{f(CI)}$ | Fall time, X2/CLKIN | | 4 | ns |
| $t_{r(CI)}$ | Rise time, X2/CLKIN | | 4 | ns |
| $t_{w(CIL)}$ | Pulse duration, X2/CLKIN low | 4 | | ns |
| $t_{w(CIH)}$ | Pulse duration, X2/CLKIN high | 4 | | ns |

(1) N is the multiplication factor.

Table 5-6. Multiply-By-N Clock Option Switching Characteristics

| PARAMETER | MIN | TYP | MAX | UNIT |
|----------------|------|-----|-----|------|
| $t_{c(CO)}$ | 6.25 | | | ns |
| $t_{d(CI-CO)}$ | 4 | 7 | 11 | ns |
| $t_{f(CO)}$ | | 2 | | ns |
| $t_{r(CO)}$ | | 2 | | ns |
| $t_{w(COL)}$ | | H | | ns |
| $t_{w(COH)}$ | | H | | ns |
| t_p | | | 30 | ms |



A. The CLKOUT timing in this diagram assumes the CLKOUT divide factor (DIVFCT field in the BSCR) is configured as 00 (CLKOUT not divided). DIVFCT is configured as CLKOUT divided-by-4 mode following reset.

Figure 5-4. Multiply-By-One Clock Timing

5.3.5 Memory and Parallel I/O Interface Timing

Address delay times are longer for cycles immediately following a HOLD operation. All timings related to the address bus have been separated into two cases; one showing normal operation and the other showing the delays related to the HOLD operation.

5.3.5.1 Memory Read

External memory reads can be performed in consecutive or nonconsecutive mode under control of the **CONSEC** bit in the BSCR. Table 5-7 and Table 5-8 assume testing over recommended operating conditions with $\overline{\text{MSTRB}} = 0$ and $H = 0.5t_{c(\text{CO})}$ (see Figure 5-5 and Figure 5-6).

Table 5-7. Memory Read Timing Requirements

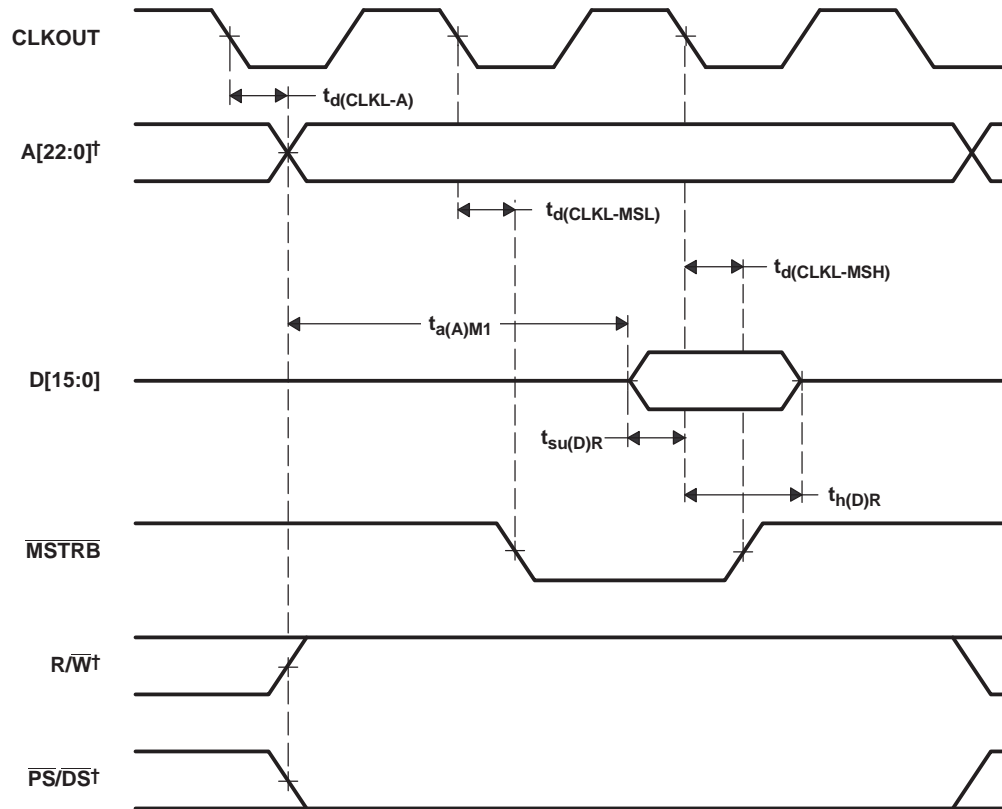
| | | MIN | MAX | UNIT | |
|-----------------------------------|--|--|-----|-------|----|
| $t_{a(\text{A})\text{M1}}$ | Access time, read data access from address valid, first read access ⁽¹⁾ | For accesses not immediately following a HOLD operation | | 4H–9 | ns |
| | | For a read accesses immediately following a HOLD operation | | 4H–11 | ns |
| $t_{a(\text{A})\text{M2}}$ | Access time, read data access from address valid, consecutive read accesses ⁽¹⁾ | 2H–9 | | ns | |
| $t_{\text{su}(\text{D})\text{R}}$ | Setup time, read data valid before CLKOUT low | 7 | | ns | |
| $t_{\text{h}(\text{D})\text{R}}$ | Hold time, read data valid after CLKOUT low | 0 | | ns | |

(1) Address, $\overline{\text{R/W}}$, $\overline{\text{P\S}}$, $\overline{\text{D\S}}$, and $\overline{\text{I\S}}$ timings are all included in timings referenced as address.

Table 5-8. Memory Read Switching Characteristics

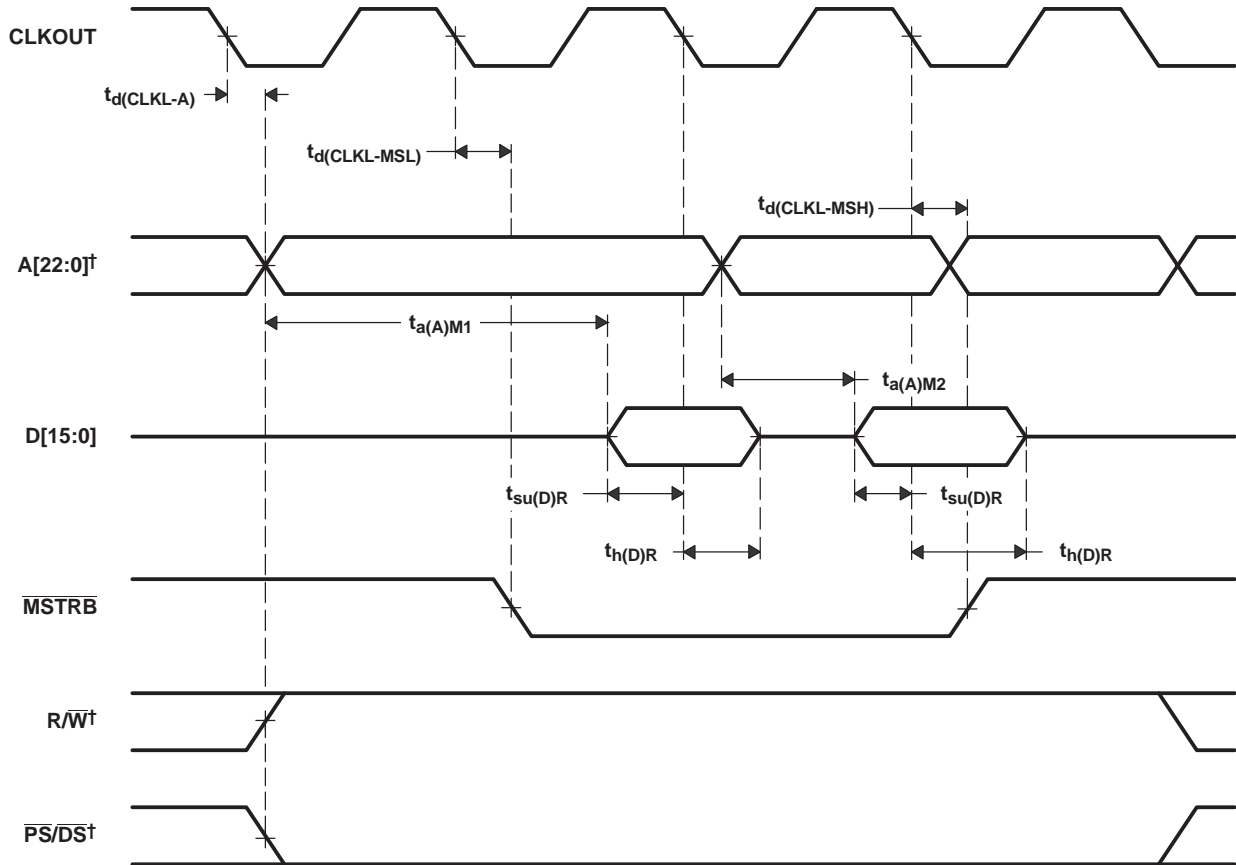
| PARAMETER | | MIN | MAX | UNIT | | |
|---------------------------------|--|--|-----|------|---|----|
| $t_{\text{d}(\text{CLKL-A})}$ | Delay time, CLKOUT low to address valid ⁽¹⁾ | For accesses not immediately following a HOLD operation | | – 1 | 4 | ns |
| | | For a read accesses immediately following a HOLD operation | | – 1 | 6 | ns |
| $t_{\text{d}(\text{CLKL-MSL})}$ | Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ low | – 1 | 4 | ns | | |
| $t_{\text{d}(\text{CLKL-MSH})}$ | Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ high | – 1 | 4 | ns | | |

(1) Address, $\overline{\text{R/W}}$, $\overline{\text{P\S}}$, $\overline{\text{D\S}}$, and $\overline{\text{I\S}}$ timings are all included in timings referenced as address.



A. Address, $\overline{\text{R/W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.

Figure 5-5. Nonconsecutive Mode Memory Reads



A. Address, $\overline{\text{R}}/\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.

Figure 5-6. Consecutive Mode Memory Reads

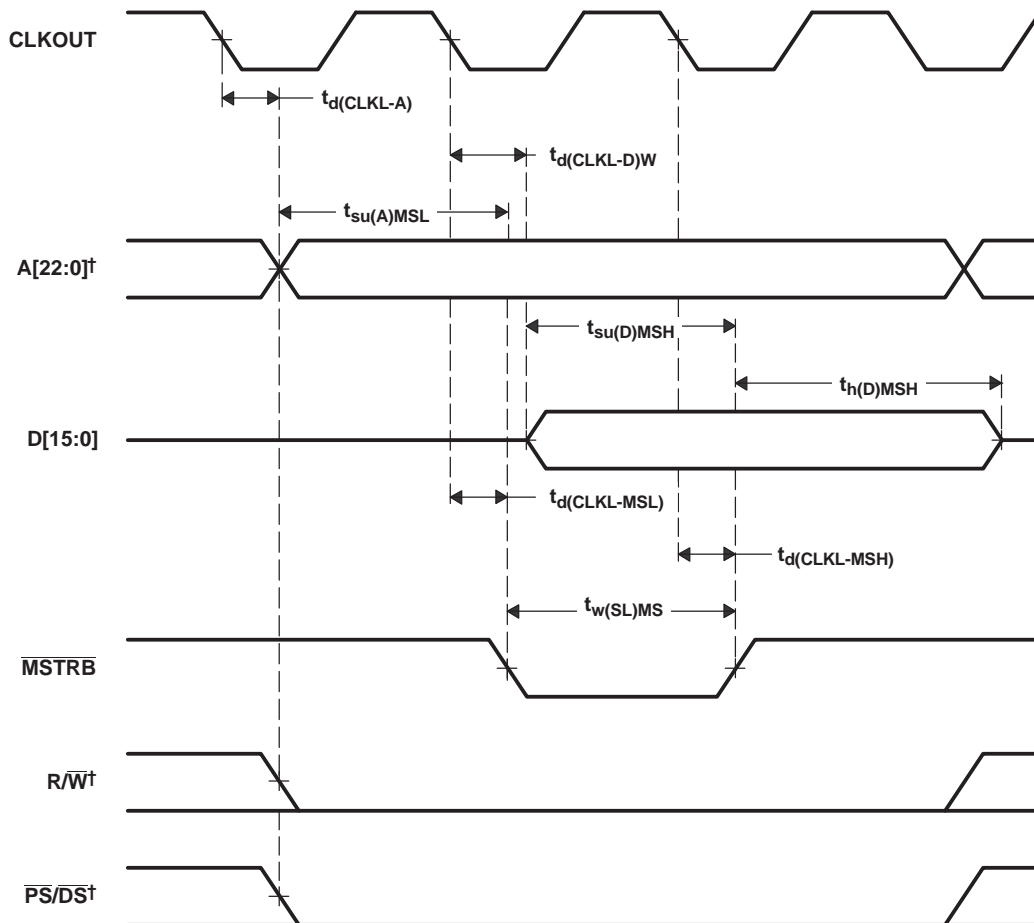
5.3.5.2 Memory Write

Table 5-9 assumes testing over recommended operating conditions with $\overline{\text{MSTRB}} = 0$ and $H = 0.5t_{c(\text{CO})}$ (see Figure 5-7).

Table 5-9. Memory Write Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT | |
|--------------------------|---|--|--------|------|----|
| $t_{d(\text{CLKL-A})}$ | Delay time, CLKOUT low to address valid ⁽¹⁾ | For accesses not immediately following a HOLD operation | - 1 | 4 | ns |
| | | For a read accesses immediately following a HOLD operation | - 1 | 6 | ns |
| $t_{\text{su(A)MSL}}$ | Setup time, address valid before $\overline{\text{MSTRB}}$ low ⁽¹⁾ | For accesses not immediately following a HOLD operation | 2H - 3 | | ns |
| | | For a read accesses immediately following a HOLD operation | 2H - 5 | | ns |
| $t_{d(\text{CLKL-D})W}$ | Delay time, CLKOUT low to data valid | - 1 | 4 | ns | |
| $t_{\text{su(D)MSH}}$ | Setup time, data valid before $\overline{\text{MSTRB}}$ high | 2H - 5 | 2H + 6 | ns | |
| $t_{h(\text{D)MSH}}$ | Hold time, data valid after $\overline{\text{MSTRB}}$ high | 2H - 5 | 2H + 6 | ns | |
| $t_{d(\text{CLKL-MSL})}$ | Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ low | - 1 | 4 | ns | |
| $t_{w(\text{SL})MS}$ | Pulse duration, $\overline{\text{MSTRB}}$ low | 2H - 2 | | ns | |
| $t_{d(\text{CLKL-MSH})}$ | Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ high | - 1 | 4 | ns | |

(1) Address, R/W, PS, DS, and IS timings are all included in timings referenced as address.



A. Address, R/W, PS, DS, and IS timings are all included in timings referenced as address.

Figure 5-7. Memory Write ($\overline{\text{MSTRB}} = 0$)

5.3.5.3 I/O Read

Table 5-10 and Table 5-11 assume testing over recommended operating conditions, $\overline{\text{IOSTRB}} = 0$, and $H = 0.5t_{c(\text{CO})}$ (see Figure 5-8).

Table 5-10. I/O Read Timing Requirements

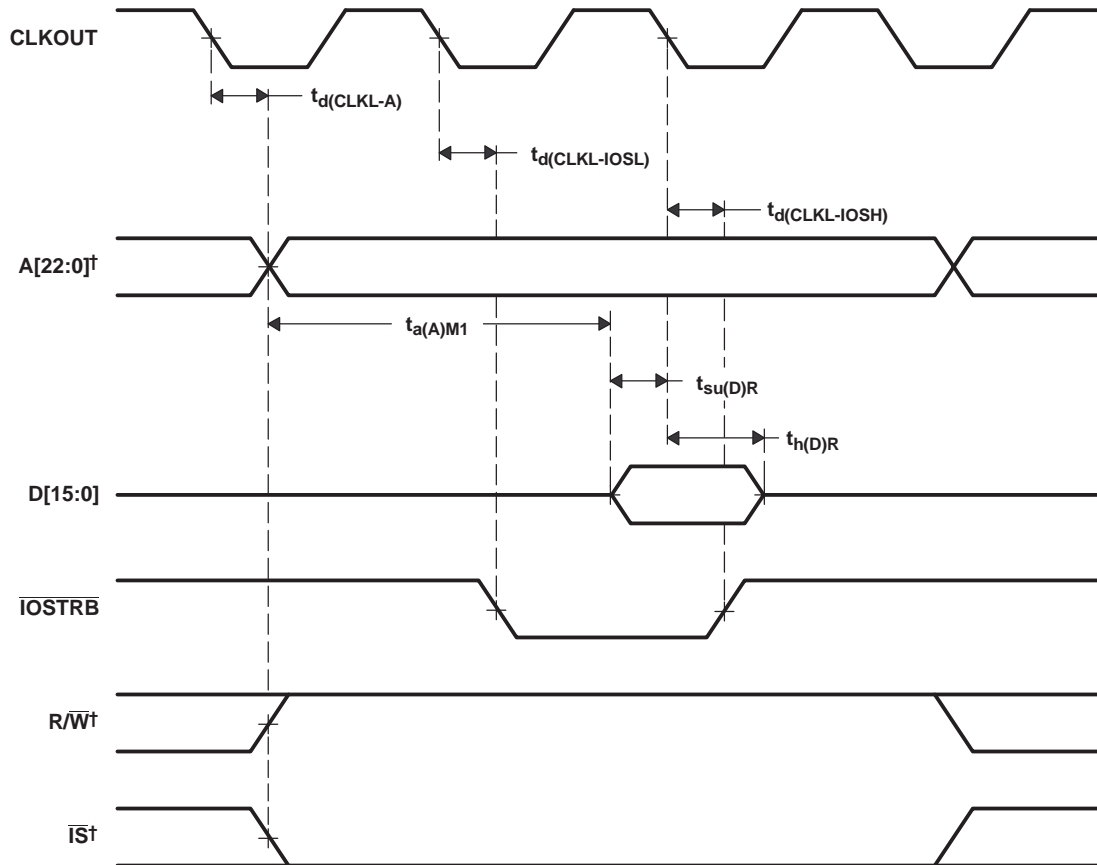
| | | MIN | MAX | UNIT | |
|-----------------------------------|--|--|-----|---------|----|
| $t_{a(\text{A})\text{M1}}$ | Access time, read data access from address valid, first read access ⁽¹⁾ | For accesses not immediately following a HOLD operation | | 4H – 9 | ns |
| | | For a read accesses immediately following a HOLD operation | | 4H – 11 | ns |
| $t_{\text{su}(\text{D})\text{R}}$ | Setup time, read data valid before CLKOUT low | 7 | | ns | |
| $t_{\text{h}(\text{D})\text{R}}$ | Hold time, read data valid after CLKOUT low | 0 | | ns | |

(1) Address, $\overline{\text{R/W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.

Table 5-11. I/O Read Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT | | |
|---|---|--|-----|------|---|----|
| $t_{\text{d}(\text{CLKL}-\text{A})}$ | Delay time, CLKOUT low to address valid ⁽¹⁾ | For accesses not immediately following a HOLD operation | | – 1 | 4 | ns |
| | | For a read accesses immediately following a HOLD operation | | – 1 | 6 | ns |
| $t_{\text{d}(\text{CLKL}-\text{IOSL})}$ | Delay time, CLKOUT low to $\overline{\text{IOSTRB}}$ low | – 1 | 4 | ns | | |
| $t_{\text{d}(\text{CLKL}-\text{OSH})}$ | Delay time, CLKOUT low to $\overline{\text{IOSTRB}}$ high | – 1 | 4 | ns | | |

(1) Address, $\overline{\text{R/W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.



A. Address, $\overline{\text{R/W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.

Figure 5-8. Parallel I/O Port Read ($\overline{\text{IOSTRB}} = 0$)

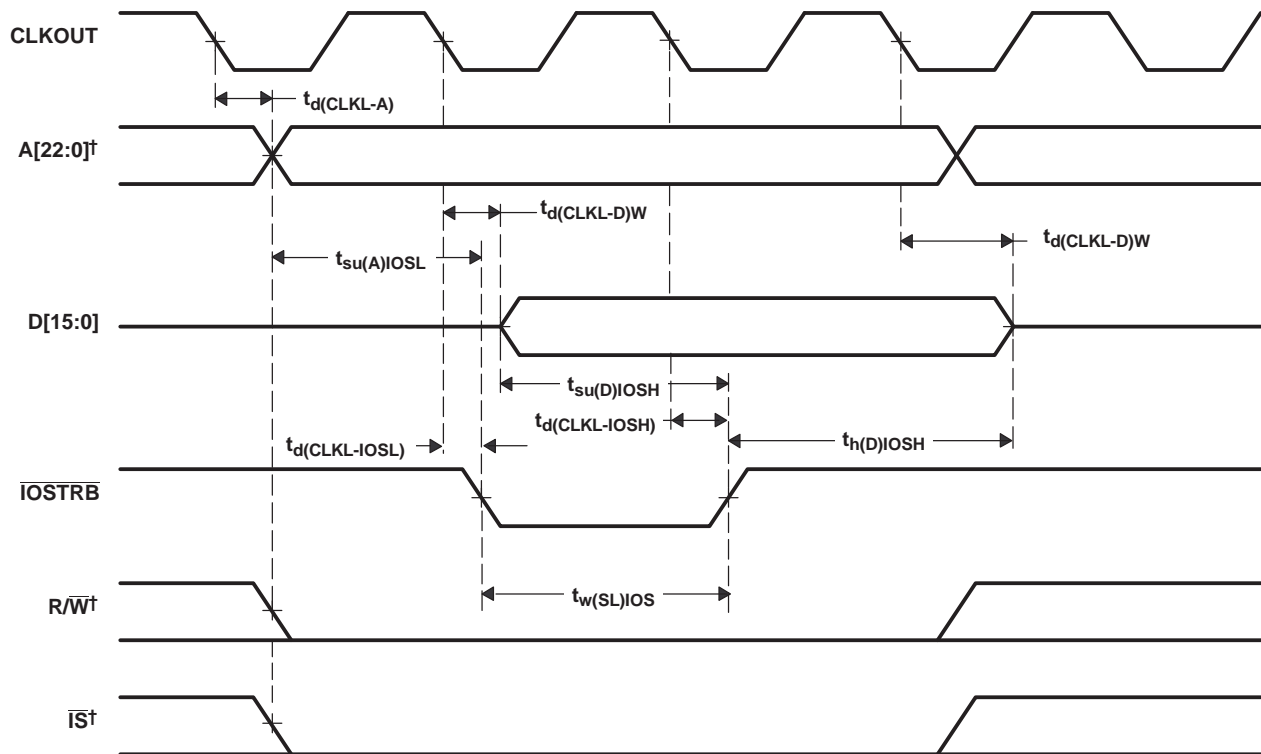
5.3.5.4 I/O Write

Table 5-12 assumes testing over recommended operating conditions, $\overline{\text{IOSTRB}} = 0$, and $H = 0.5t_{c(\text{CO})}$ (see Figure 5-9).

Table 5-12. I/O Write Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT | |
|--------------------------------|--|--|--------|------|----|
| $t_{d(\text{CLKL-A})}$ | Delay time, CLKOUT low to address valid ⁽¹⁾ | For accesses not immediately following a HOLD operation | - 1 | 4 | ns |
| | | For a read accesses immediately following a HOLD operation | - 1 | 6 | ns |
| $t_{su(\text{A})\text{IOSL}}$ | Setup time, address valid before $\overline{\text{IOSTRB}}$ low ⁽¹⁾ | For accesses not immediately following a HOLD operation | 2H - 3 | | ns |
| | | For a read accesses immediately following a HOLD operation | 2H - 5 | | ns |
| $t_{d(\text{CLKL-D})\text{W}}$ | Delay time, CLKOUT low to write data valid | - 1 | 4 | ns | |
| $t_{su(\text{D})\text{IOSH}}$ | Setup time, data valid before $\overline{\text{IOSTRB}}$ high | 2H - 5 | 2H + 6 | ns | |
| $t_{h(\text{D})\text{IOSH}}$ | Hold time, data valid after $\overline{\text{IOSTRB}}$ high | 2H - 5 | 2H + 6 | ns | |
| $t_{d(\text{CLKL-IOSL})}$ | Delay time, CLKOUT low to $\overline{\text{IOSTRB}}$ low | - 1 | 4 | ns | |
| $t_{w(\text{SL})\text{IOS}}$ | Pulse duration, $\overline{\text{IOSTRB}}$ low | 2H - 2 | | ns | |
| $t_{d(\text{CLKL-IOSH})}$ | Delay time, CLKOUT low to $\overline{\text{IOSTRB}}$ high | - 1 | 4 | ns | |

(1) Address, $\overline{\text{R/W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.



A. Address, $\overline{\text{R/W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.

Figure 5-9. Parallel I/O Port Write ($\overline{\text{IOSTRB}} = 0$)

5.3.6 Ready Timing for Externally Generated Wait States

Table 5-13 and Table 5-14 assume testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 5-10, Figure 5-11, Figure 5-12, and Figure 5-13).

Table 5-13. Ready Timing Requirements for Externally Generated Wait States

| | | MIN | MAX | UNIT |
|--------------------|--|-----|--------|------|
| $t_{su(RDY)}$ | Setup time, READY before CLKOUT low ⁽¹⁾ | 7 | | ns |
| $t_{h(RDY)}$ | Hold time, READY after CLKOUT low ⁽¹⁾ | 0 | | ns |
| $t_{v(RDY)MSTRB}$ | Valid time, READY after \overline{MSTRB} low ⁽²⁾ | | 4H – 4 | ns |
| $t_{h(RDY)MSTRB}$ | Hold time, READY after \overline{MSTRB} low ⁽²⁾ | | 4H | ns |
| $t_{v(RDY)IOSTRB}$ | Valid time, READY after \overline{IOSTRB} low ⁽²⁾ | | 4H – 4 | ns |
| $t_{h(RDY)IOSTRB}$ | Hold time, READY after \overline{IOSTRB} low ⁽²⁾ | | 4H | ns |

- (1) The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the internal software wait states.
- (2) These timings are included for reference only. The critical timings for READY are those referenced to CLKOUT.

Table 5-14. Ready Switching Characteristics for Externally Generated Wait States

| | PARAMETER | MIN | MAX | UNIT |
|---------------|---|-----|-----|------|
| $t_{d(MCSL)}$ | Delay time, CLKOUT low to \overline{MSC} low | – 1 | 4 | ns |
| $t_{d(MSCH)}$ | Delay time, CLKOUT low to \overline{MSC} high | – 1 | 4 | ns |

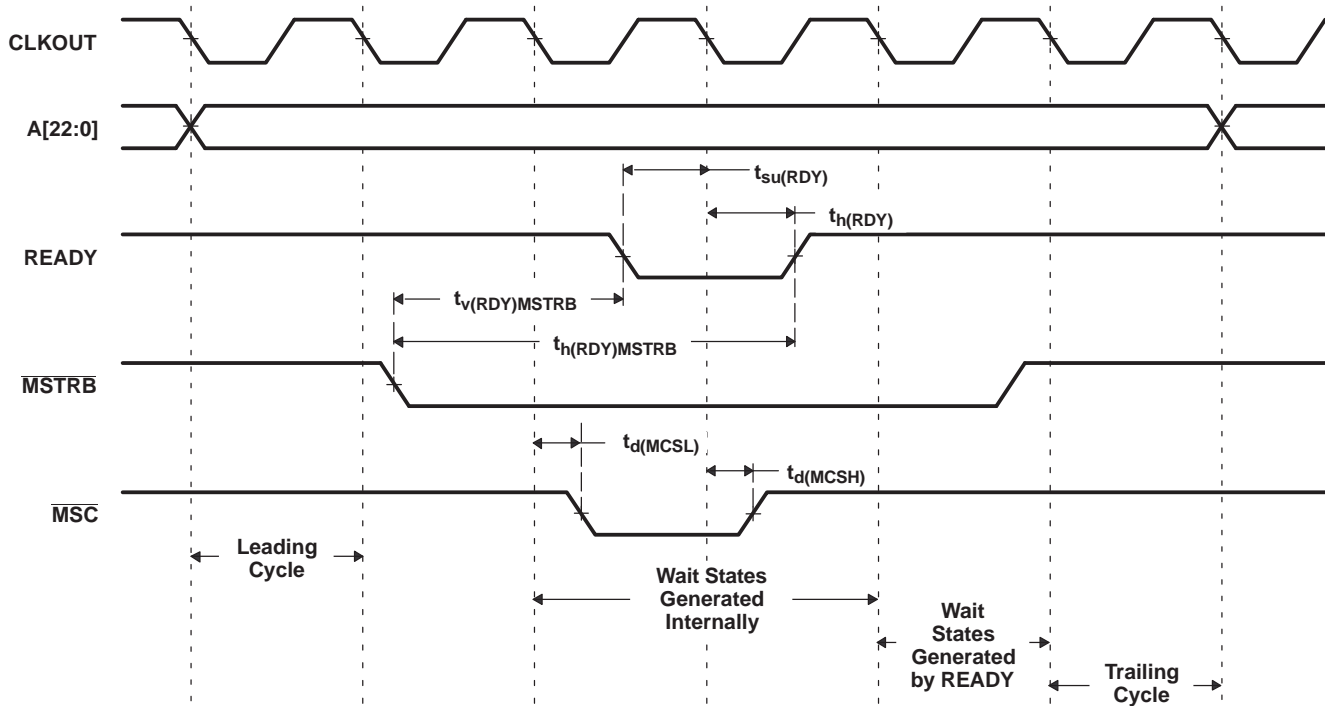


Figure 5-10. Memory Read With Externally Generated Wait States

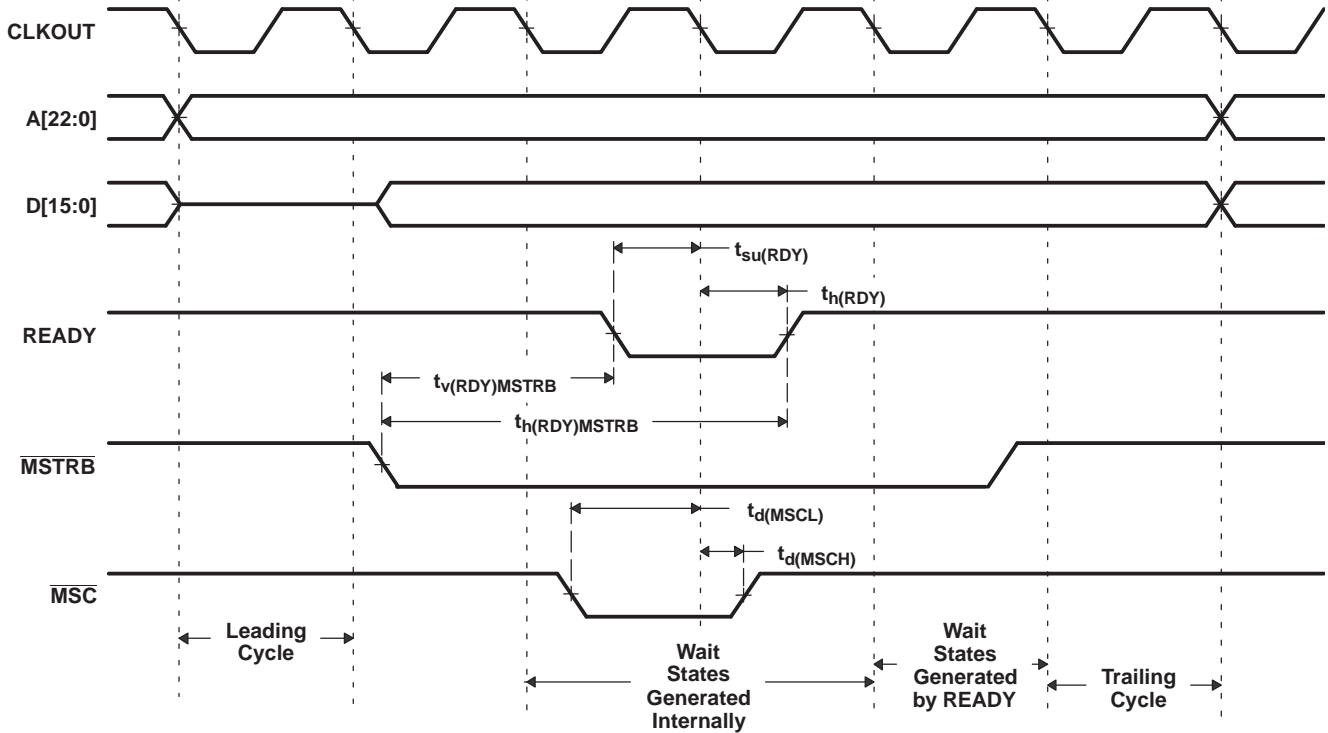


Figure 5-11. Memory Write With Externally Generated Wait States

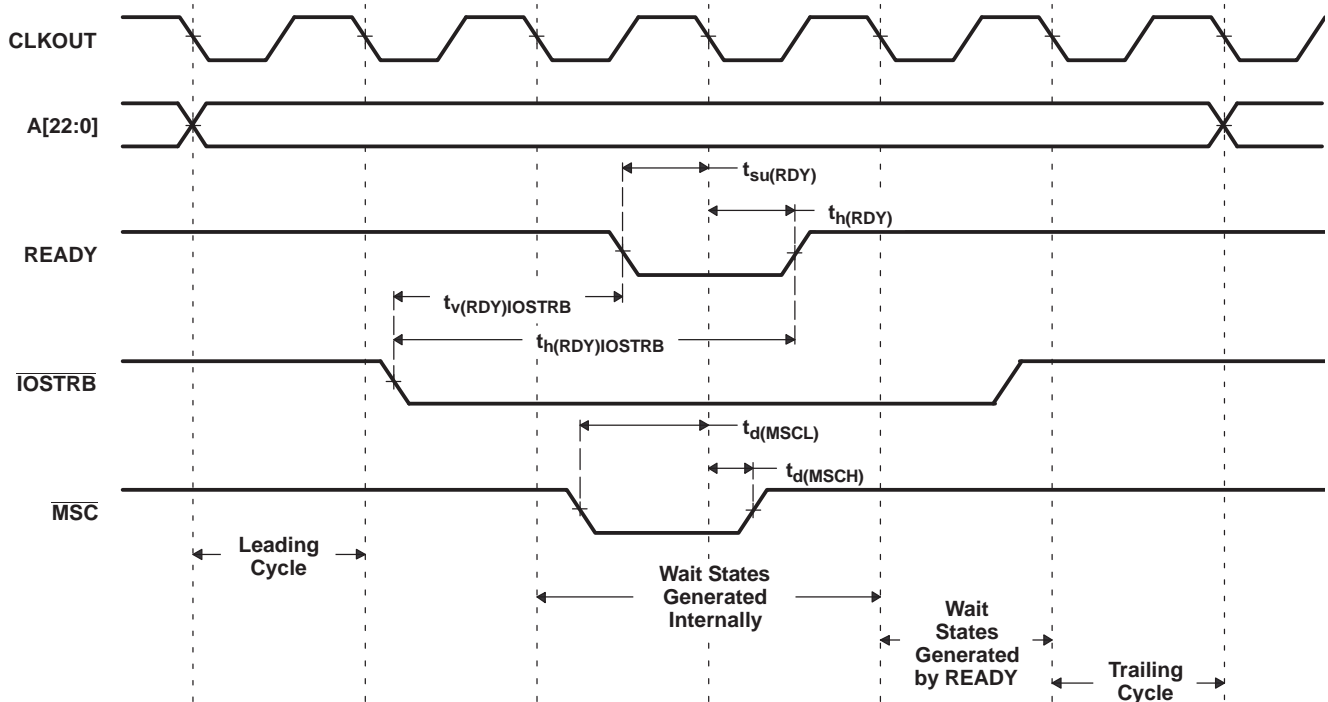


Figure 5-12. I/O Read With Externally Generated Wait States

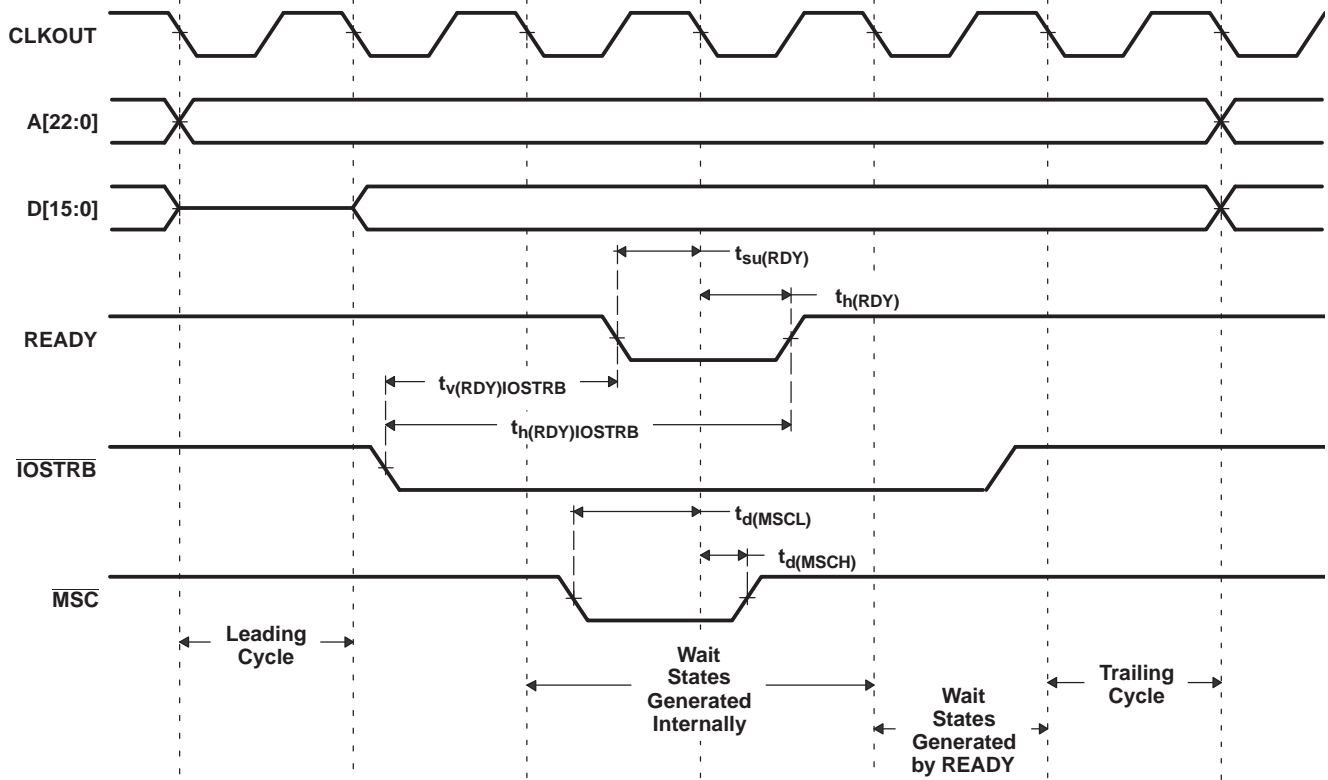


Figure 5-13. I/O Write With Externally Generated Wait States

5.3.7 HOLD and HOLDA Timings

Table 5-15 and Table 5-16 assume testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 5-14).

Table 5-15. HOLD and HOLDA Timing Requirements

| | | MIN | MAX | UNIT |
|----------------|--|------|-----|------|
| $t_{w(HOLD)}$ | Pulse duration, \overline{HOLD} low duration | 4H+8 | | ns |
| $t_{su(HOLD)}$ | Setup time, \overline{HOLD} before CLKOUT low ⁽¹⁾ | 7 | | ns |

(1) This input can be driven from an asynchronous source, therefore, there are no specific timing requirements with respect to CLKOUT, however, if this timing is met, the input will be recognized on the CLKOUT edge referenced.

Table 5-16. HOLD and HOLDA Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT |
|--------------------|---|--------|------|------|
| $t_{dis(CLKL-A)}$ | Disable time, Address, \overline{PS} , \overline{DS} , \overline{IS} high impedance from CLKOUT low | | 3 | ns |
| $t_{dis(CLKL-RW)}$ | Disable time, R/\overline{W} high impedance from CLKOUT low | | 3 | ns |
| $t_{dis(CLKL-S)}$ | Disable time, \overline{MSTRB} , \overline{IOSTRB} high impedance from CLKOUT low | | 3 | ns |
| $t_{en(CLKL-A)}$ | Enable time, Address, \overline{PS} , \overline{DS} , \overline{IS} valid from CLKOUT low | | 2H+6 | ns |
| $t_{en(CLKL-RW)}$ | Enable time, R/\overline{W} enabled from CLKOUT low | | 2H+3 | ns |
| $t_{en(CLKL-S)}$ | Enable time, \overline{MSTRB} , \overline{IOSTRB} enabled from CLKOUT low | 2 | 2H+3 | ns |
| $t_v(HOLDA)$ | Valid time, \overline{HOLDA} low after CLKOUT low | -1 | 4 | ns |
| | Valid time, \overline{HOLDA} high after CLKOUT low | -1 | 4 | ns |
| $t_w(HOLDA)$ | Pulse duration, \overline{HOLDA} low duration | 2H - 3 | | ns |

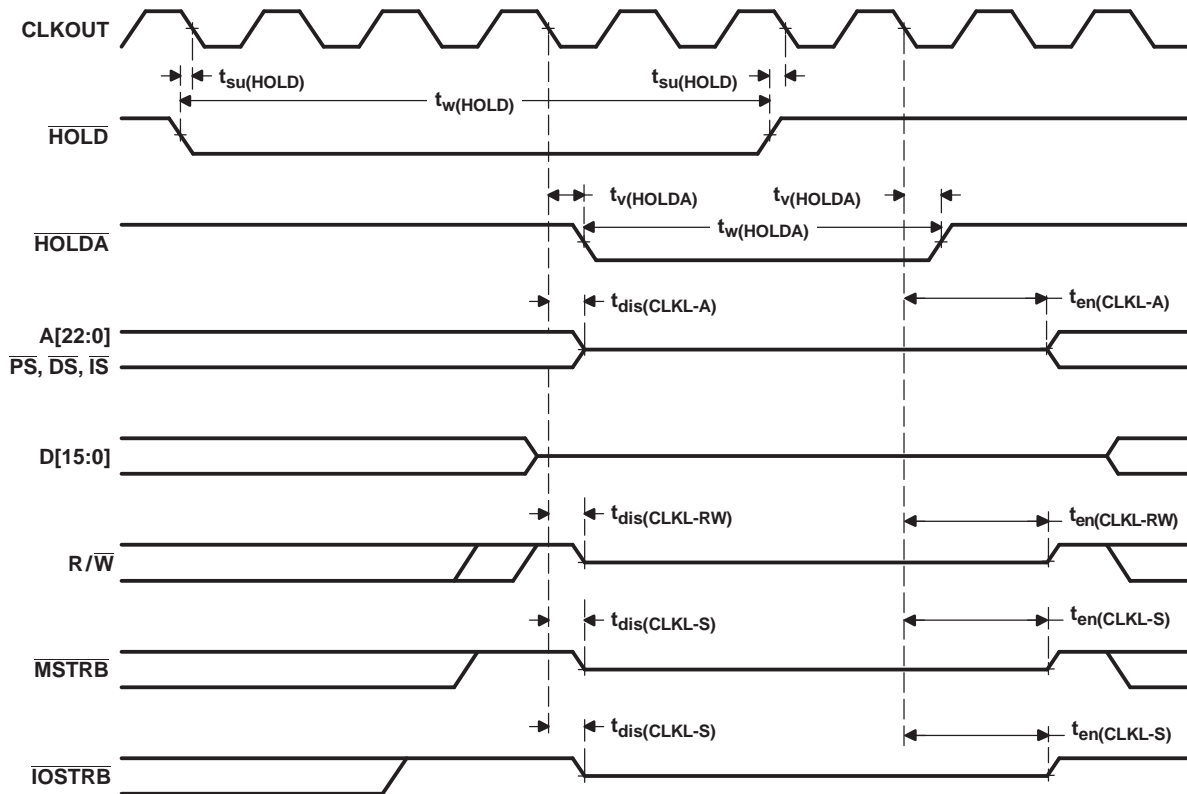


Figure 5-14. HOLD and HOLDA Timings (HM = 1)

5.3.8 Reset, $\overline{\text{BIO}}$, Interrupt, and $\overline{\text{MP/MC}}$ Timings

Table 5-17 assumes testing over recommended operating conditions and $H = 0.5t_{c(\text{CO})}$ (see Figure 5-15, Figure 5-16, and Figure 5-17).

Table 5-17. Reset, $\overline{\text{BIO}}$, Interrupt, and $\overline{\text{MP/MC}}$ Timing Requirements

| | | MIN | MAX | UNIT |
|--------------------------------|--|------|-----|------|
| $t_{h(\text{RS})}$ | Hold time, $\overline{\text{RS}}$ after CLKOUT low ⁽¹⁾ | 2 | | ns |
| $t_{h(\text{BIO})}$ | Hold time, $\overline{\text{BIO}}$ after CLKOUT low ⁽¹⁾ | 4 | | ns |
| $t_{h(\text{INT})}$ | Hold time, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$, after CLKOUT low ⁽¹⁾⁽²⁾ | 1 | | ns |
| $t_{h(\text{MPMC})}$ | Hold time, $\overline{\text{MP/MC}}$ after CLKOUT low ⁽¹⁾ | 4 | | ns |
| $t_{w(\text{RSL})}$ | Pulse duration, $\overline{\text{RS}}$ low ⁽³⁾⁽⁴⁾ | 4H+3 | | ns |
| $t_{w(\text{BIO})\text{S}}$ | Pulse duration, $\overline{\text{BIO}}$ low, synchronous | 2H+3 | | ns |
| $t_{w(\text{BIO})\text{A}}$ | Pulse duration, $\overline{\text{BIO}}$ low, asynchronous | 4H | | ns |
| $t_{w(\text{INTH})\text{S}}$ | Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ high (synchronous) | 2H+2 | | ns |
| $t_{w(\text{INTH})\text{A}}$ | Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ high (asynchronous) | 4H | | ns |
| $t_{w(\text{INTL})\text{S}}$ | Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low (synchronous) | 2H+2 | | ns |
| $t_{w(\text{INTL})\text{A}}$ | Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low (asynchronous) | 4H | | ns |
| $t_{w(\text{INTL})\text{WKP}}$ | Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low for IDLE2/IDLE3 wakeup | 7 | | ns |
| $t_{\text{su}(\text{RS})}$ | Setup time, $\overline{\text{RS}}$ before X2/CLKIN low ⁽¹⁾⁽²⁾ | 3 | | ns |
| $t_{\text{su}(\text{BIO})}$ | Setup time, $\overline{\text{BIO}}$ before CLKOUT low ⁽¹⁾ | 7 | | ns |
| $t_{\text{su}(\text{INT})}$ | Setup time, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$, $\overline{\text{RS}}$ before CLKOUT low ⁽¹⁾ | 7 | | ns |
| $t_{\text{su}(\text{MPMC})}$ | Setup time, $\overline{\text{MP/MC}}$ before CLKOUT low ⁽¹⁾ | 5 | | ns |

- (1) These inputs can be driven from an asynchronous source, therefore, there are no specific timing requirements with respect to CLKOUT, however, if setup and hold timings are met, the input will be recognized on the CLKOUT edge referenced.
- (2) The external interrupts ($\overline{\text{INT0}}\text{--}\overline{\text{INT3}}$, $\overline{\text{NMI}}$) are synchronized to the core CPU by way of a two-flip-flop synchronizer that samples these inputs with consecutive falling edges of CLKOUT. The input to the interrupt pins is required to represent a 1-0-0 sequence at the timing that is corresponding to three CLKOUTs sampling sequence.
- (3) If the PLL mode is selected, then at power-on sequence, or at wakeup from IDLE3, $\overline{\text{RS}}$ must be held low for at least 50 μs to ensure synchronization and lock-in of the PLL.
- (4) $\overline{\text{RS}}$ may cause a change in clock frequency, therefore changing the value of H.

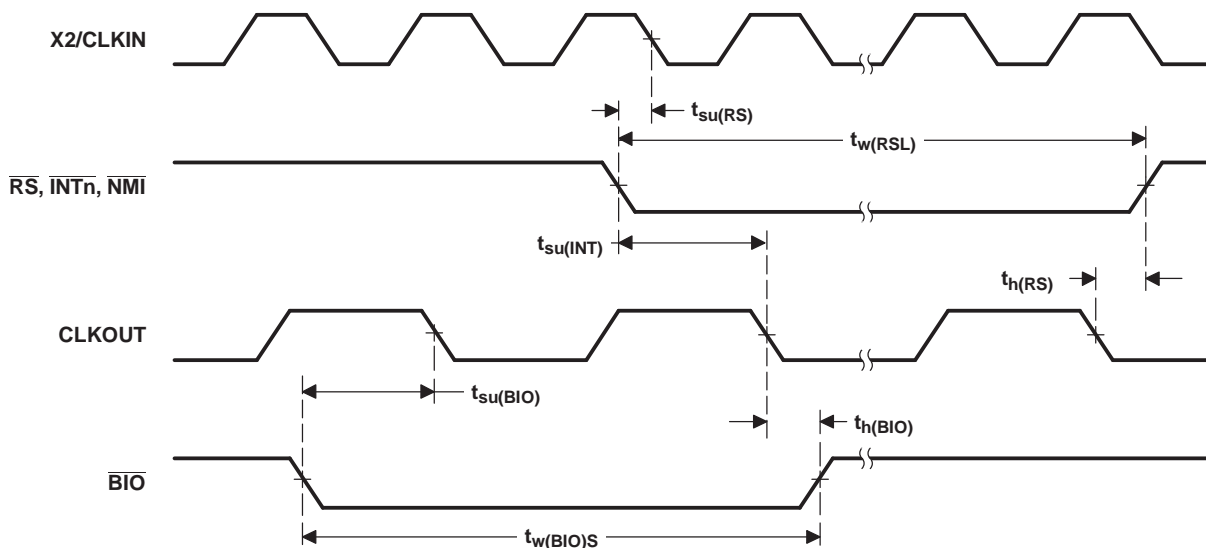


Figure 5-15. Reset and $\overline{\text{BIO}}$ Timings

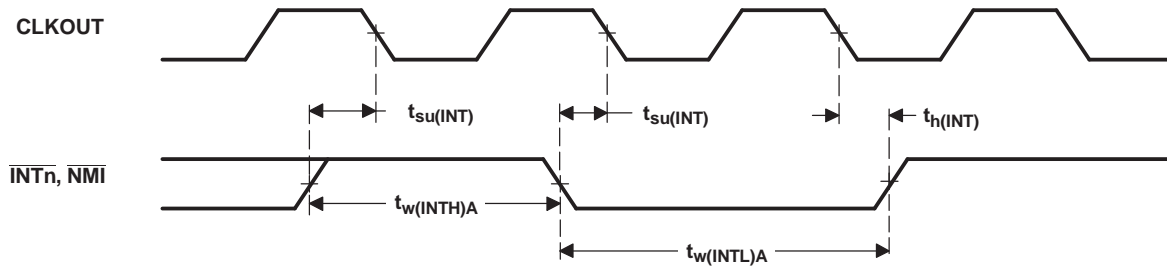


Figure 5-16. Interrupt Timing

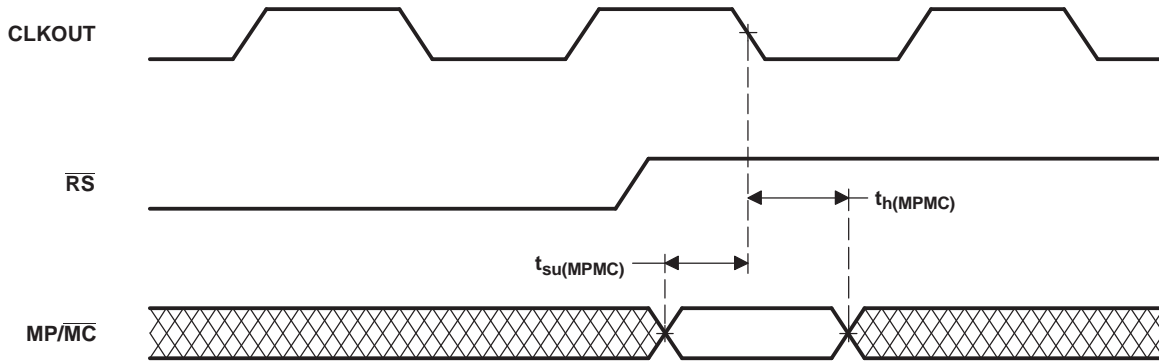


Figure 5-17. MP/MC Timing

5.3.9 Instruction Acquisition ($\overline{\text{IAQ}}$) and Interrupt Acknowledge ($\overline{\text{IACK}}$) Timings

Table 5-18 assumes testing over recommended operating conditions and $H = 0.5t_{c(\text{CO})}$ (see Figure 5-18).

Table 5-18. Instruction Acquisition ($\overline{\text{IAQ}}$) and Interrupt Acknowledge ($\overline{\text{IACK}}$) Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT |
|------------------------------|--|--------|-----|------|
| $t_{d(\text{CLKL-IAQL})}$ | Delay time, CLKOUT low to $\overline{\text{IAQ}}$ low | -1 | 4 | ns |
| $t_{d(\text{CLKL-IAQH})}$ | Delay time, CLKOUT low to $\overline{\text{IAQ}}$ high | -1 | 4 | ns |
| $t_{d(\text{A})\text{IAQ}}$ | Delay time, $\overline{\text{IAQ}}$ low to address valid | | 2 | ns |
| $t_{d(\text{CLKL-IACKL})}$ | Delay time, CLKOUT low to $\overline{\text{IACK}}$ low | -1 | 4 | ns |
| $t_{d(\text{CLKL-IACKH})}$ | Delay time, CLKOUT low to $\overline{\text{IACK}}$ high | -1 | 4 | ns |
| $t_{d(\text{A})\text{IACK}}$ | Delay time, $\overline{\text{IACK}}$ low to address valid | | 2 | ns |
| $t_{h(\text{A})\text{IAQ}}$ | Hold time, address valid after $\overline{\text{IAQ}}$ high | -2 | | ns |
| $t_{h(\text{A})\text{IACK}}$ | Hold time, address valid after $\overline{\text{IACK}}$ high | -2 | | ns |
| $t_w(\text{IAQL})$ | Pulse duration, $\overline{\text{IAQ}}$ low | 2H - 2 | | ns |
| $t_w(\text{IACKL})$ | Pulse duration, $\overline{\text{IACK}}$ low | 2H - 2 | | ns |

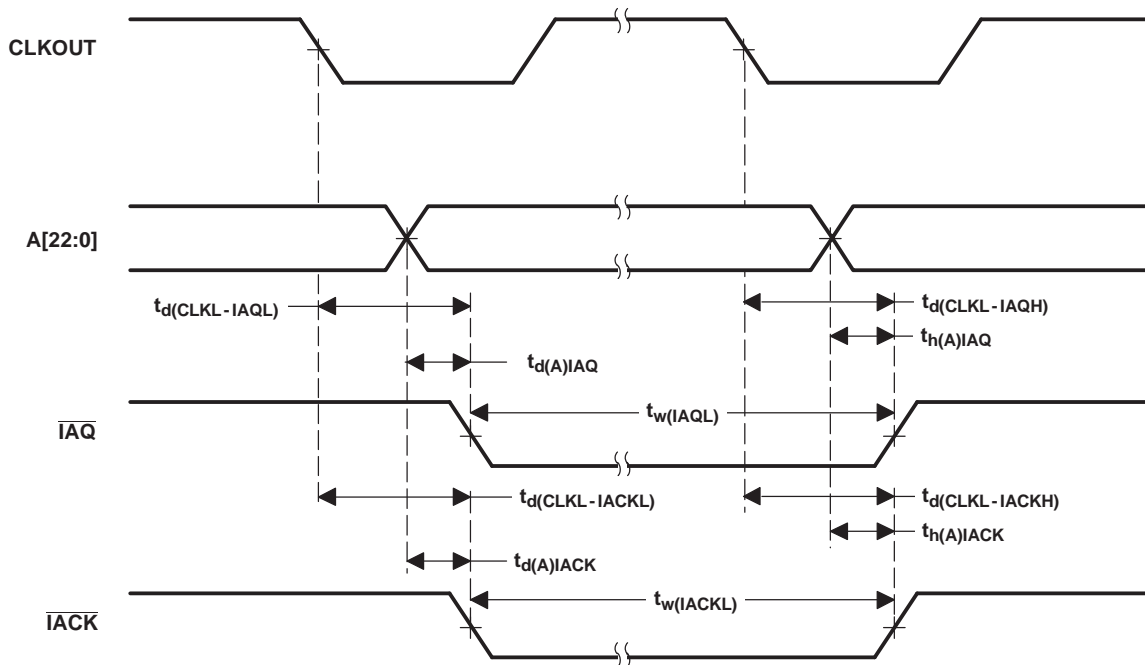


Figure 5-18. Instruction Acquisition ($\overline{\text{IAQ}}$) and Interrupt Acknowledge ($\overline{\text{IACK}}$) Timings

5.3.10 External Flag (XF) and TOUT Timings

Table 5-19 assumes testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 5-19 and Figure 5-20).

Table 5-19. External Flag (XF) and TOUT Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT |
|----------------|-------------------------------------|--------|-----|------|
| $t_{d(XF)}$ | Delay time, CLKOUT low to XF high | -1 | 4 | ns |
| | Delay time, CLKOUT low to XF low | -1 | 4 | |
| $t_{d(TOUTH)}$ | Delay time, CLKOUT low to TOUT high | -1 | 4 | ns |
| $t_{d(TOURL)}$ | Delay time, CLKOUT low to TOUT low | -1 | 4 | ns |
| $t_w(TOUT)$ | Pulse duration, TOUT | 2H - 4 | | ns |

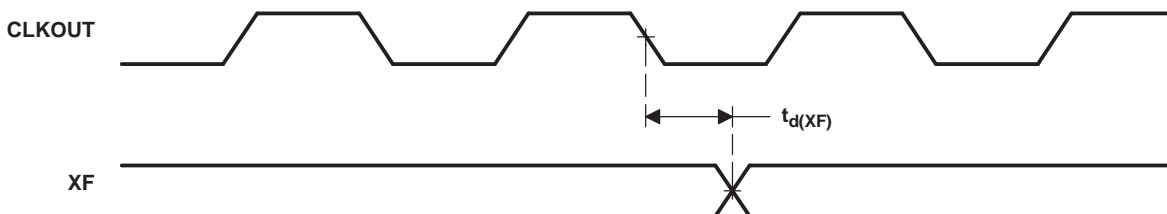


Figure 5-19. External Flag (XF) Timing

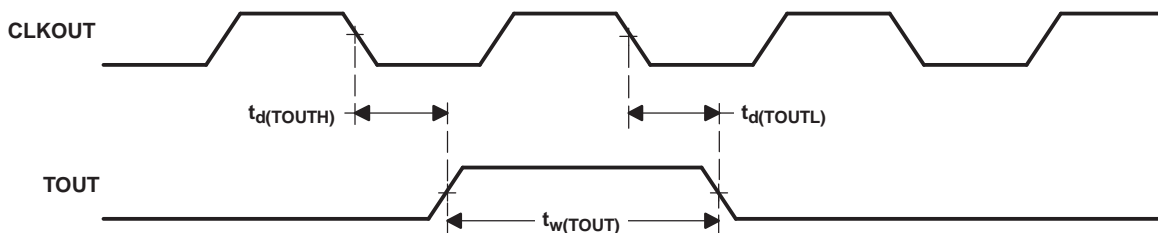


Figure 5-20. TOUT Timing

5.3.11 Multichannel Buffered Serial Port (McBSP) Timing

5.3.11.1 McBSP Transmit and Receive Timings

Table 5-20 and Table 5-21 assume testing over recommended operating conditions (see Figure 5-21 and Figure 5-22).

Table 5-20. McBSP Transmit and Receive Timing Requirements

| | | | MIN ⁽¹⁾ | MAX | UNIT |
|-----------------------------|--|-------------|-----------------------|-----|------|
| $t_c(\text{BCKRX})$ | Cycle time, BCLKR/X ⁽²⁾ | BCLKR/X ext | 4P ⁽¹⁾ | | ns |
| $t_w(\text{BCKRX})$ | Pulse duration, BCLKR/X high or BCLKR/X low ⁽²⁾ | BCLKR/X ext | 2P – 1 ⁽¹⁾ | | ns |
| $t_{su}(\text{BFRH-BCKRL})$ | Setup time, external BFSR high before BCLKR low | BCLKR int | 8 | | ns |
| | | BCLKR ext | 1 | | |
| $t_h(\text{BCKRL-BFRH})$ | Hold time, external BFSR high after BCLKR low | BCLKR int | 1 | | ns |
| | | BCLKR ext | 2 | | |
| $t_{su}(\text{BDRV-BCKRL})$ | Setup time, BDR valid before BCLKR low | BCLKR int | 7 | | ns |
| | | BCLKR ext | 1 | | |
| $t_h(\text{BCKRL-BDRV})$ | Hold time, BDR valid after BCLKR low | BCLKR int | 2 | | ns |
| | | BCLKR ext | 3 | | |
| $t_{su}(\text{BFXH-BCKXL})$ | Setup time, external BFSX high before BCLKX low | BCLKX int | 8 | | ns |
| | | BCLKX ext | 1 | | |
| $t_h(\text{BCKXL-BFXH})$ | Hold time, external BFSX high after BCLKX low | BCLKX int | 0 | | ns |
| | | BCLKX ext | 2 | | |
| $t_r(\text{BCKRX})$ | Rise time, BCKR/X | BCLKR/X ext | | 6 | ns |
| $t_f(\text{BCKRX})$ | Fall time, BCKR/X | BCLKR/X ext | | 6 | ns |

(1) P = 0.5 * processor clock

(2) Note that in some cases, for example when driving another 54x device McBSP, maximum serial port clocking rates may not be achievable at maximum CPU clock frequency due to transmitted data timings and corresponding receive timing requirements. A separate detailed timing analysis should be performed for each specific McBSP interface.

Table 5-21. McBSP Transmit and Receive Switching Characteristics

| PARAMETER | | | MIN ⁽¹⁾ | MAX | UNIT |
|-------------------------------|--|-------------|----------------------|----------------------|------|
| $t_c(\text{BCKRX})$ | Cycle time, BCLKR/X ⁽²⁾ | BCLKR/X int | 4P ⁽³⁾ | | ns |
| $t_w(\text{BCKRXH})$ | Pulse duration, BCLKR/X high ⁽²⁾ | BCLKR/X int | D - 1 ⁽⁴⁾ | D + 1 ⁽⁴⁾ | ns |
| $t_w(\text{BCKRXL})$ | Pulse duration, BCLKR/X low | BCLKR/X int | C - 1 ⁽⁴⁾ | C + 1 ⁽⁴⁾ | ns |
| $t_d(\text{BCKRH-BFRV})$ | Delay time, BCLKR high to internal BFSR valid | BCLKR int | - 3 | 3 | ns |
| | | BCLKR ext | 0 | 11 | ns |
| $t_d(\text{BCKXH-BFXV})$ | Delay time, BCLKX high to internal BFSX valid | BCLKX int | - 1 | 5 | ns |
| | | BCLKX ext | 2 | 10 | ns |
| $t_{dis}(\text{BCKXH-BDXHZ})$ | Disable time, BCLKX high to BDX high impedance following last data bit of transfer | BCLKX int | | 6 | ns |
| | | BCLKX ext | | 10 | ns |
| $t_d(\text{BCKXH-BDXV})$ | Delay time, BCLKX high to BDX valid | DXENA = 0 | | | |
| | | BCLKX int | - 1 ⁽⁵⁾ | 10 | ns |
| $t_d(\text{BCKXH-BDXV})$ | Delay time, BCLKX high to BDX valid | BCLKX ext | 2 | 20 | ns |
| | | BFSX int | -1 ⁽⁵⁾ | 7 | ns |
| $t_d(\text{BFXH-BDXV})$ | Delay time, BFSX high to BDX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode | BFSX ext | 2 | 11 | ns |

- (1) CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
- (2) Note that in some cases, for example when driving another 54x device McBSP, maximum serial port clocking rates may not be achievable at maximum CPU clock frequency due to transmitted data timings and corresponding receive timing requirements. A separate detailed timing analysis should be performed for each specific McBSP interface.
- (3) P = 0.5 * processor clock
- (4) T = BCLKRX period = (1 + CLKGDV) * 2P
C = BCLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2P when CLKGDV is even
D = BCLKRX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2P when CLKGDV is even
- (5) Minimum delay times also represent minimum output hold times.

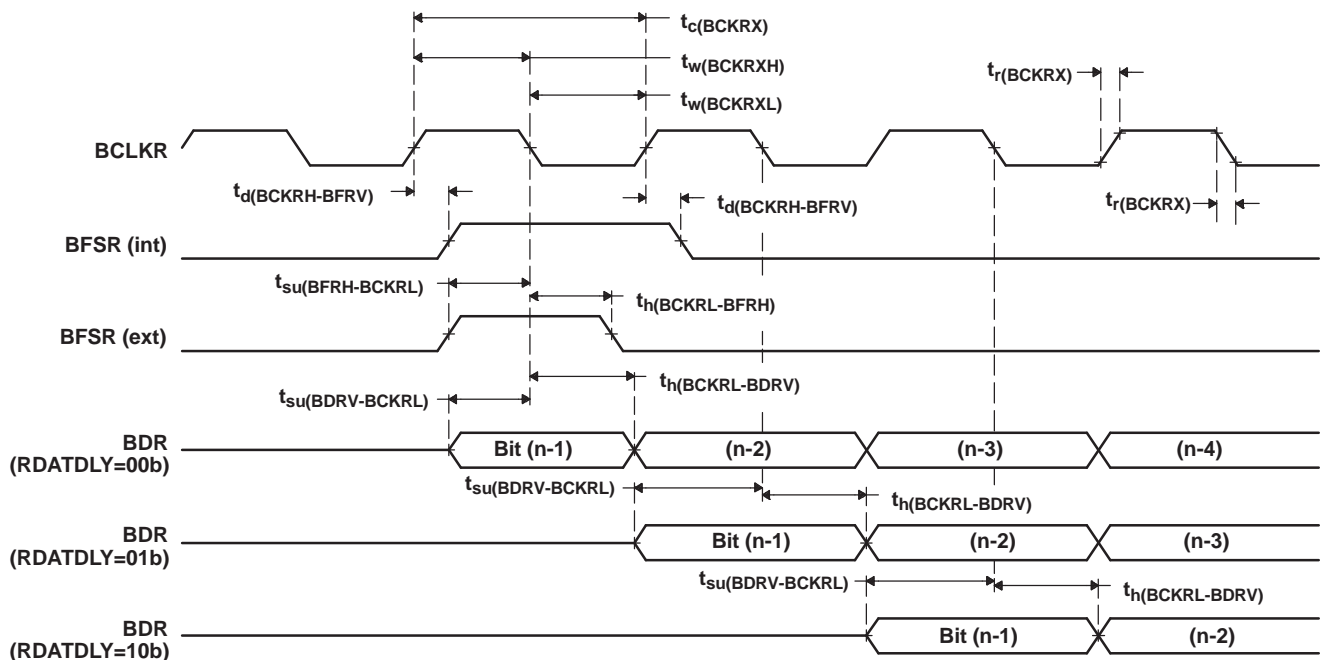


Figure 5-21. McBSP Receive Timings

5.3.11.2 McBSP General-Purpose I/O Timing

Table 5-22 and Table 5-23 assume testing over recommended operating conditions (see Figure 5-23).

Table 5-22. McBSP General-Purpose I/O Timing Requirements

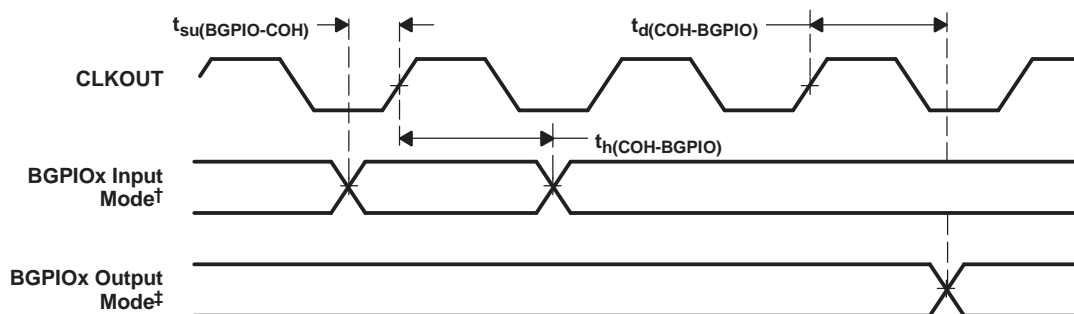
| | | MIN | MAX | UNIT |
|---------------------|---|-----|-----|------|
| $t_{su}(BGPIO-COH)$ | Setup time, BGPIOx input mode before CLKOUT high ⁽¹⁾ | 7 | | ns |
| $t_h(COH-BGPIO)$ | Hold time, BGPIOx input mode after CLKOUT high ⁽¹⁾ | 0 | | ns |

(1) BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general-purpose input.

Table 5-23. McBSP General-Purpose I/O Switching Characteristics

| PARAMETER | MIN | MAX | UNIT | |
|------------------|--|-----|------|----|
| $t_d(COH-BGPIO)$ | Delay time, CLKOUT high to BGPIOx output mode ⁽¹⁾ | -2 | 4 | ns |

(1) BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general-purpose input.



- A. BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general-purpose input.
- B. BGPIOx refers to BCLKRx, BFSRx, BCLKXx, BFSXx, or BDXx when configured as a general-purpose output.

Figure 5-23. McBSP General-Purpose I/O Timings

5.3.11.3 McBSP as SPI Master or Slave Timing

Table 5-24 to Table 5-31 assume testing over recommended operating conditions (see Figure 5-24, Figure 5-25, Figure 5-26, and Figure 5-27).

Table 5-24. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)

| | | MASTER | | SLAVE ⁽¹⁾ | | UNIT |
|----------------------|--|--------|-----|------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{su}(BDRV-BCKXL)$ | Setup time, BDR valid before BCLKX low | 12 | | 2 – 6P ⁽²⁾ | | ns |
| $t_h(BCKXL-BDRV)$ | Hold time, BDR valid after BCLKX low | 4 | | 5 + 12P ⁽²⁾ | | ns |

- (1) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
 (2) P = 0.5 * processor clock

Table 5-25. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)

| PARAMETER | | MASTER ⁽¹⁾ | | SLAVE ⁽¹⁾ | | UNIT |
|------------------------|---|-----------------------|-------|-----------------------|-------------------------|------|
| | | MIN | MAX | MIN | MAX | |
| $t_h(BCKXL-BFXL)$ | Hold time, BFSX low after BCLKX low ⁽²⁾ | T – 3 | T + 4 | | | ns |
| $t_d(BFXL-BCKXH)$ | Delay time, BFSX low to BCLKX high ⁽³⁾ | C – 4 | C + 3 | | | ns |
| $t_d(BCKXH-BDXV)$ | Delay time, BCLKX high to BDX valid | – 4 | 5 | 6P + 2 ⁽⁴⁾ | 10P + 17 ⁽⁴⁾ | ns |
| $t_{dis}(BCKXL-BDXHZ)$ | Disable time, BDX high impedance following last data bit from BCLKX low | C – 2 | C + 3 | | | ns |
| $t_{dis}(BFXH-BDXHZ)$ | Disable time, BDX high impedance following last data bit from BFSX high | | | 2P – 4 ⁽⁴⁾ | 6P + 17 ⁽⁴⁾ | ns |
| $t_d(BFXL-BDXV)$ | Delay time, BFSX low to BDX valid | | | 4P + 2 ⁽⁴⁾ | 8P + 17 ⁽⁴⁾ | ns |

- (1) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
 (2) FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally. CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
 (3) BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).
 (4) P = 0.5 * processor clock

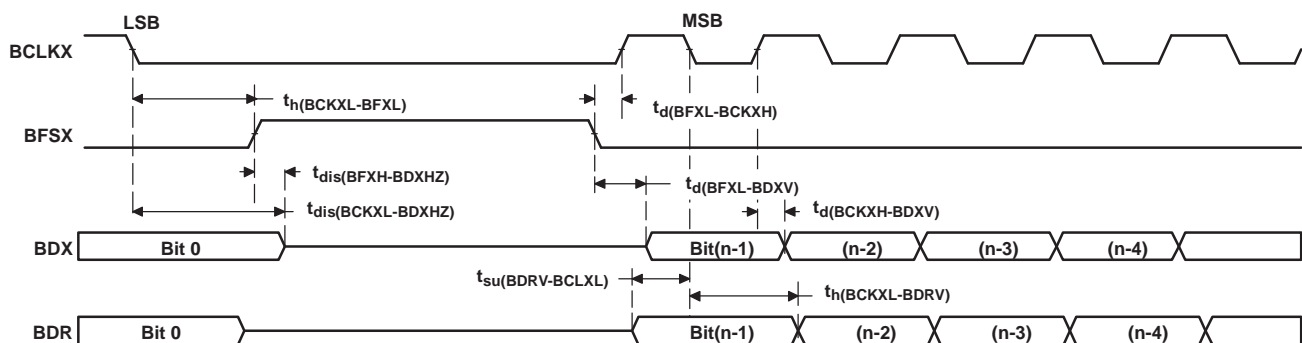


Figure 5-24. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

Table 5-26. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)

| | | MASTER | | SLAVE ⁽¹⁾ | | UNIT |
|----------------------|------------------------------------|--------|-----|------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{su}(BDRV-BCKXL)$ | Setup time, BDR valid before BCKXL | 12 | | 2 – 6P ⁽²⁾ | | ns |
| $t_h(BCKXH-BDRV)$ | Hold time, BDR valid after BCKXH | 4 | | 5 + 12P ⁽²⁾ | | ns |

- (1) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
 (2) P = 0.5 * processor clock

Table 5-27. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)

| PARAMETER | | MASTER ⁽¹⁾ | | SLAVE ⁽²⁾ | | UNIT |
|------------------------|---|-----------------------|-------|-----------------------|-------------------------|------|
| | | MIN | MAX | MIN | MAX | |
| $t_h(BCKXL-BFXL)$ | Hold time, BFSX low after BCKXL low ⁽³⁾ | C – 3 | C + 4 | | | ns |
| $t_d(BFXL-BCKXH)$ | Delay time, BFSX low to BCKXH high ⁽⁴⁾ | T – 4 | T + 3 | | | ns |
| $t_d(BCKXL-BDXV)$ | Delay time, BCKXL low to BDX valid | – 4 | 5 | 6P + 2 ⁽⁵⁾ | 10P + 17 ⁽⁵⁾ | ns |
| $t_{dis}(BCKXL-BDXHZ)$ | Disable time, BDX high impedance following last data bit from BCKXL low | – 2 | 4 | 6P – 4 ⁽⁵⁾ | 10P + 17 ⁽⁵⁾ | ns |
| $t_d(BFXL-BDXV)$ | Delay time, BFSX low to BDX valid | D – 2 | D + 4 | 4P + 2 ⁽⁵⁾ | 8P + 17 ⁽⁵⁾ | ns |

- (1) T = BCKLX period = (1 + CLKGDV) * 2P
 C = BCKLX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2P when CLKGDV is even
 D = BCKLX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2P when CLKGDV is even
 (2) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
 (3) FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally. CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
 (4) BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCKLX).
 (5) P = 0.5 * processor clock

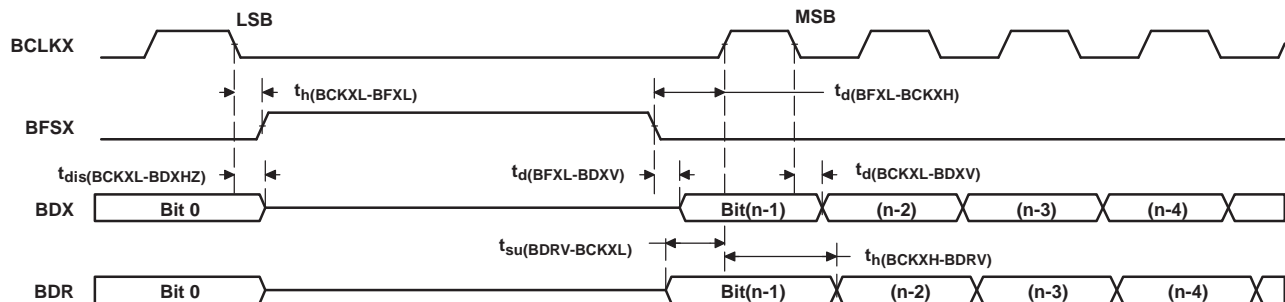


Figure 5-25. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

Table 5-28. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)

| | | MASTER | | SLAVE ⁽¹⁾ | | UNIT |
|----------------------|---|--------|-----|----------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{su}(BDRV-BCKXH)$ | Setup time, BDR valid before BCLKX high | 12 | | $2 - 6P^{(2)}$ | | ns |
| $t_h(BCKXH-BDRV)$ | Hold time, BDR valid after BCLKX high | 4 | | $5 + 12P^{(2)}$ | | ns |

- (1) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
 (2) $P = 0.5 * \text{processor clock}$

Table 5-29. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)

| PARAMETER | | MASTER ⁽¹⁾ | | SLAVE ⁽²⁾ | | UNIT |
|------------------------|--|-----------------------|---------|----------------------|------------------|------|
| | | MIN | MAX | MIN | MAX | |
| $t_h(BCKXH-BFXL)$ | Hold time, BFSX low after BCLKX high ⁽³⁾ | $T - 3$ | $T + 4$ | | | ns |
| $t_d(BFXL-BCKXL)$ | Delay time, BFSX low to BCLKX low ⁽⁴⁾ | $D - 4$ | $D + 3$ | | | ns |
| $t_d(BCKXL-BDXV)$ | Delay time, BCLKX low to BDX valid | $- 4$ | 5 | $6P + 2^{(5)}$ | $10P + 17^{(5)}$ | ns |
| $t_{dis}(BCKXH-BDXHZ)$ | Disable time, BDX high impedance following last data bit from BCLKX high | $D - 2$ | $D + 3$ | | | ns |
| $t_{dis}(BFXH-BDXHZ)$ | Disable time, BDX high impedance following last data bit from BFSX high | | | $2P - 4^{(5)}$ | $6P + 17^{(5)}$ | ns |
| $t_d(BFXL-BDXV)$ | Delay time, BFSX low to BDX valid | | | $4P + 2^{(5)}$ | $8P + 17^{(5)}$ | ns |

- (1) FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally. CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
 (2) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
 (3) BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).
 (4) $T = \text{BCLKX period} = (1 + \text{CLKGDV}) * 2P$
 $D = \text{BCLKX high pulse width} = T/2$ when CLKGDV is odd or zero and $= (\text{CLKGDV}/2 + 1) * 2P$ when CLKGDV is even
 (5) $P = 0.5 * \text{processor clock}$

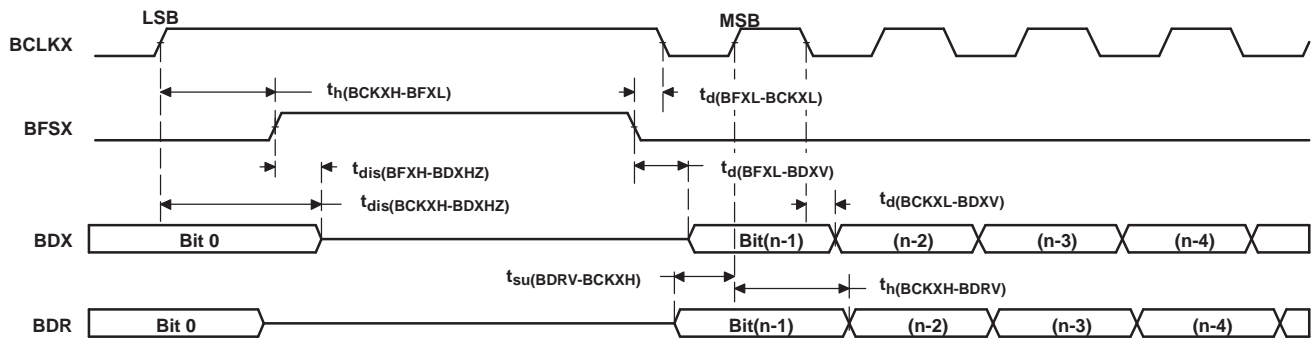


Figure 5-26. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

Table 5-30. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)

| | | MASTER | | SLAVE ⁽¹⁾ | | UNIT |
|----------------------|--|--------|-----|------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{su}(BDRV-BCKXL)$ | Setup time, BDR valid before BCLKX low | 12 | | 2 – 6P ⁽²⁾ | | ns |
| $t_h(BCKXL-BDRV)$ | Hold time, BDR valid after BCLKX low | 4 | | 5 + 12P ⁽²⁾ | | ns |

- (1) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
 (2) P = 0.5 * processor clock

Table 5-31. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)

| PARAMETER | | MASTER ⁽¹⁾ | | SLAVE ⁽²⁾ | | UNIT |
|------------------------|--|-----------------------|-------|-----------------------|-------------------------|------|
| | | MIN | MAX | MIN | MAX | |
| $t_h(BCKXH-BFXL)$ | Hold time, BFSX low after BCLKX high ⁽³⁾ | D – 3 | D + 4 | | | ns |
| $t_d(BFXL-BCKXL)$ | Delay time, BFSX low to BCLKX low ⁽⁴⁾ | T – 4 | T + 3 | | | ns |
| $t_d(BCKXH-BDXV)$ | Delay time, BCLKX high to BDX valid | – 4 | 5 | 6P + 2 ⁽⁵⁾ | 10P + 17 ⁽⁵⁾ | ns |
| $t_{dis}(BCKXH-BDXHZ)$ | Disable time, BDX high impedance following last data bit from BCLKX high | – 2 | 4 | 6P – 4 ⁽⁵⁾ | 10P + 17 ⁽⁵⁾ | ns |
| $t_d(BFXL-BDXV)$ | Delay time, BFSX low to BDX valid | C – 2 | C + 4 | 4P + 2 ⁽⁵⁾ | 8P + 17 ⁽⁵⁾ | ns |

- (1) T = BCLKX period = (1 + CLKGDV) * 2P
 C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2P when CLKGDV is even
 D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2P when CLKGDV is even
 (2) For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
 (3) FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally. CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
 (4) BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).
 (5) P = 0.5 * processor clock

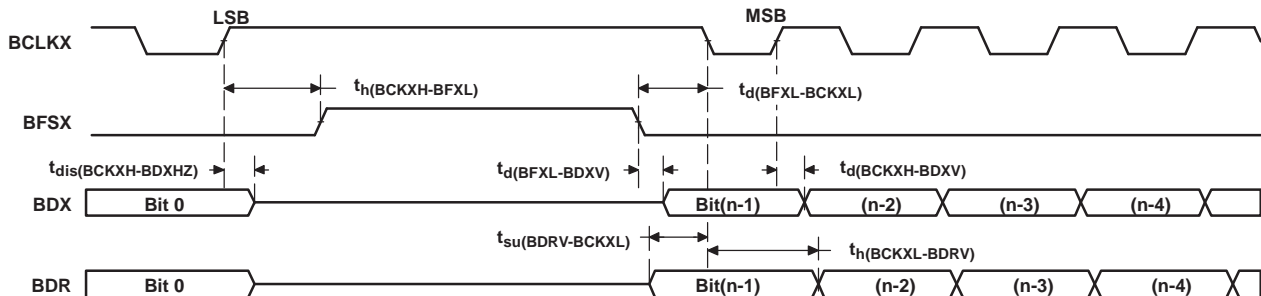


Figure 5-27. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

5.3.12 Host-Port Interface Timing

5.3.12.1 HPI8 Mode

Table 5-32 and Table 5-33 assume testing over recommended operating conditions and $P = 0.5$ * processor clock (see Figure 5-28 through Figure 5-31). In the following tables, DS refers to the logical OR of HCS, HDS1, and HDS2. HD refers to any of the HPI data bus pins (HD0, HD1, HD2, etc.). HAD stands for HCNTL0, HCNTL1, and HR/W.

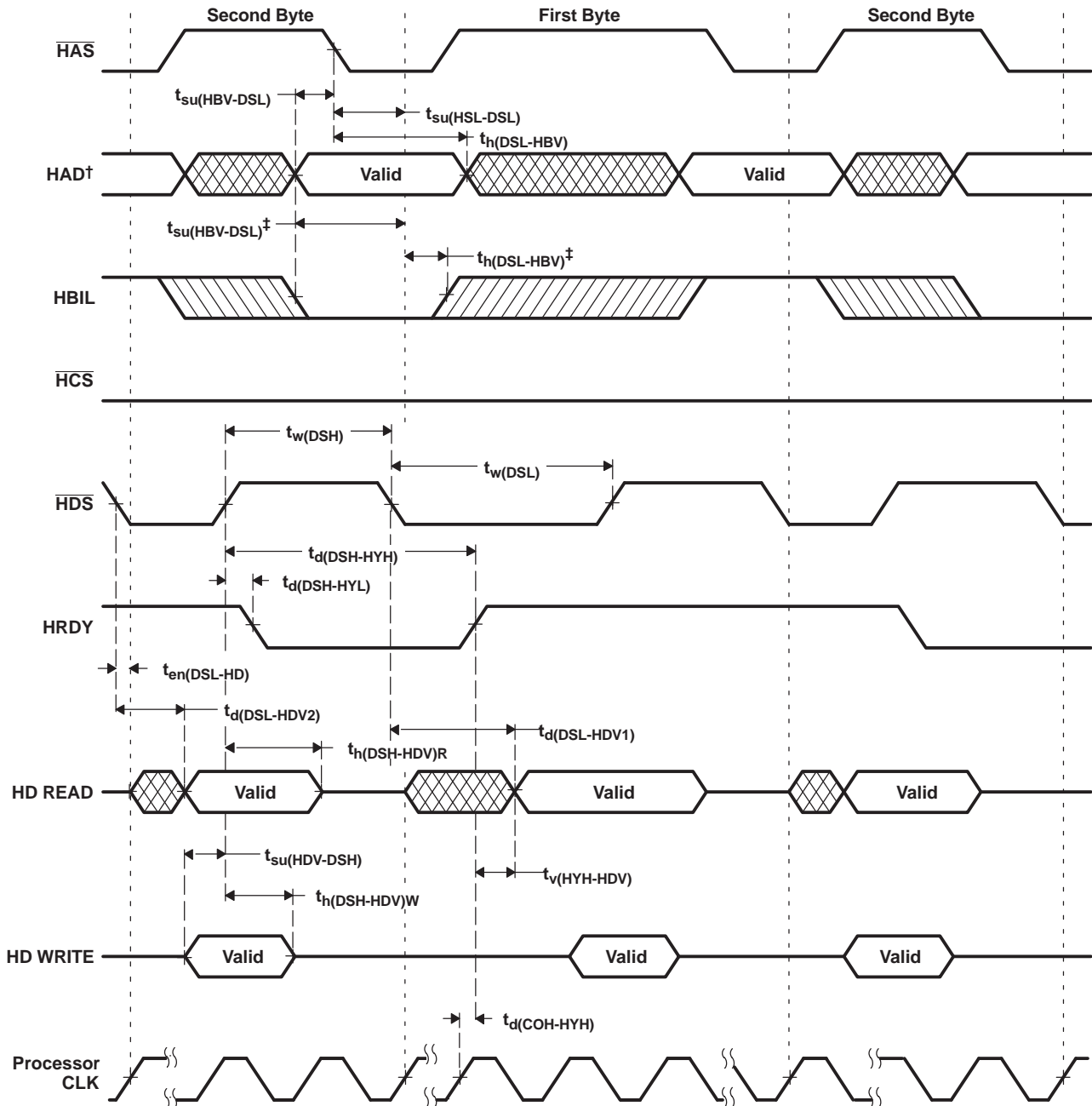
Table 5-32. HPI8 Mode Timing Requirements

| | | MIN | MAX | UNIT |
|--------------------|---|-----|-----|------|
| $t_{su}(HBV-DSL)$ | Setup time, HBIL and HAD valid before DS low (when \overline{HAS} is not used), or HBIL valid before \overline{HAS} low | 6 | | ns |
| $t_h(DSL-HBV)$ | Hold time, HBIL and HAD valid after DS low (when \overline{HAS} is not used), or HBIL valid after \overline{HAS} low | 3 | | ns |
| $t_{su}(HSL-DSL)$ | Setup time, \overline{HAS} low before DS low | 8 | | ns |
| $t_w(DSL)$ | Pulse duration, DS low | 13 | | ns |
| $t_w(DSH)$ | Pulse duration, DS high | 7 | | ns |
| $t_{su}(HDV-DSH)$ | Setup time, HD valid before DS high, HPI write | 3 | | ns |
| $t_h(DSH-HDV)W$ | Hold time, HD valid after DS high, HPI write | 2 | | ns |
| $t_{su}(GPIO-COH)$ | Setup time, HDx input valid before CLKOUT high, HDx configured as general-purpose input | 3 | | ns |
| $t_h(GPIO-COH)$ | Hold time, HDx input valid before CLKOUT high, HDx configured as general-purpose input | 0 | | ns |

Table 5-33. HPI8 Mode Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT |
|-------------------|---|--|---------------------|------|
| $t_{en(DSL-HD)}$ | Enable time, HD driven from DS low | 0 | 10 | ns |
| $t_{d(DSL-HDV1)}$ | Delay time, DS low to HD valid for first byte of an HPI read | Case 1a: Memory accesses when DMAC is active and $t_{w(DSH)} < 18H^{(1)}$ | $18P+10-t_{w(DSH)}$ | ns |
| | | Case 1b: Memory accesses when DMAC is active and $t_{w(DSH)} \geq 18H^{(1)}$ | 10 | |
| | | Case 2a: Memory accesses when DMAC is inactive and $t_{w(DSH)} < 10H^{(1)}$ | $10P+10-t_{w(DSH)}$ | |
| | | Case 2b: Memory accesses when DMAC is inactive and $t_{w(DSH)} \geq 10H^{(1)}$ | 10 | |
| | | Case 3: Register accesses | 10 | |
| $t_{d(DSL-HDV2)}$ | Delay time, DS low to HD valid for second byte of an HPI read | | 10 | ns |
| $t_{h(DSH-HDV)R}$ | Hold time, HD valid after DS high, for a HPI read | 0 | | ns |
| $t_{v(HYH-HDV)}$ | Valid time, HD valid after HRDY high | | 2 | ns |
| $t_{d(DSH-HYL)}$ | Delay time, DS high to HRDY low ⁽²⁾ | | 8 | ns |
| $t_{d(DSH-HYH)}$ | Delay time, DS high to HRDY high ⁽²⁾ | Case 1: Memory accesses when DMAC is active ⁽¹⁾ | $18P+6$ | ns |
| | | Case 2: Memory accesses when DMAC is inactive ⁽¹⁾ | $10P+6$ | |
| | | Case 3: Write accesses to HPIC register ⁽³⁾ | $6P+6$ | |
| $t_{d(HCS-HRDY)}$ | Delay time, \overline{HCS} low/high to HRDY low/high | | 6 | ns |
| $t_{d(COH-HYH)}$ | Delay time, CLKOUT high to HRDY high | | 9 | ns |
| $t_{d(COH-HTX)}$ | Delay time, CLKOUT high to \overline{HINT} change | | 6 | ns |
| $t_{d(COH-GPIO)}$ | Delay time, CLKOUT high to HDx output change. HDx is configured as a general-purpose output | | 5 | ns |

- (1) DMAC stands for direct memory access controller (DMAC). The HPI8 shares the internal DMA bus with the DMAC, thus HPI8 access times are affected by DMAC activity.
- (2) The HRDY output is always high when the \overline{HCS} input is high, regardless of DS timings.
- (3) This timing applies when writing a one to the DSPINT bit or \overline{HINT} bit of the HPIC register. All other writes to the HPIC occur asynchronously, and do not cause HRDY to be deasserted.



- A. HAD refers to HCNTL0 , HCNTL1 , and $\text{HR}/\overline{\text{W}}$.
- B. When $\overline{\text{HAS}}$ is not used ($\overline{\text{HAS}}$ always high)

Figure 5-28. HPI-8 Mode Timing, Using $\overline{\text{HDS}}$ to Control Accesses ($\overline{\text{HCS}}$ Always Low)

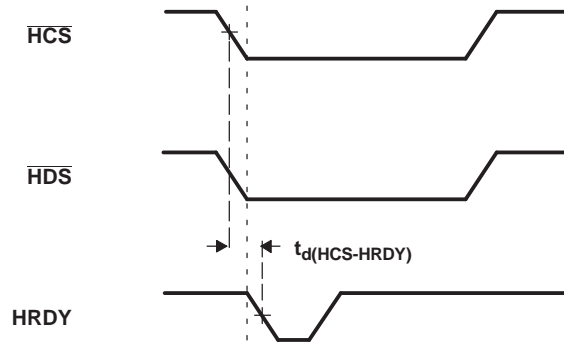


Figure 5-29. HPI-8 Mode Timing, Using $\overline{\text{HCS}}$ to Control Accesses

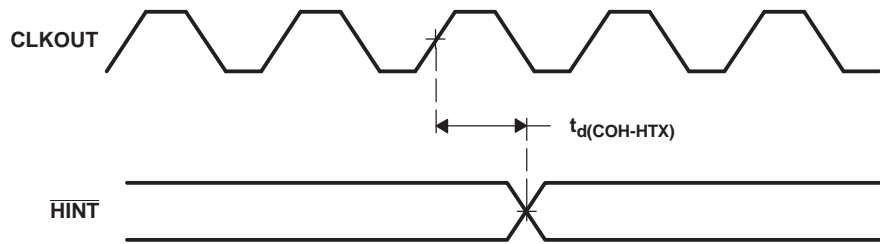
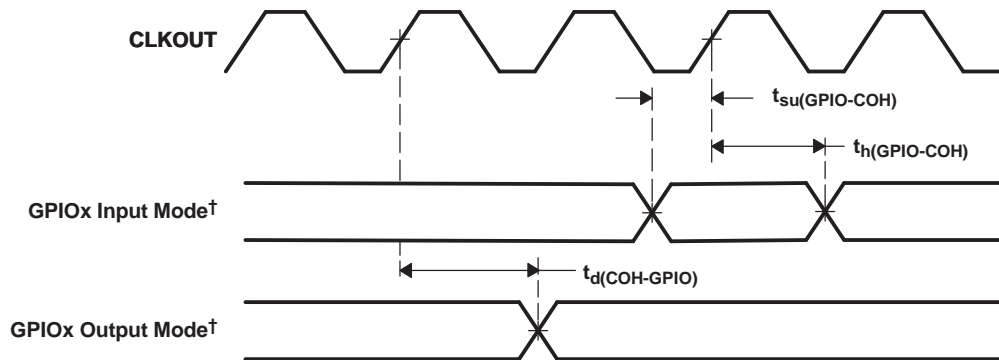


Figure 5-30. HPI-8 Mode, $\overline{\text{HINT}}$ Timing



A. GPIOx refers to HD0, HD1, HD2, ...HD7, when the HD bus is configured for general-purpose input/output (I/O).

Figure 5-31. GPIOx Timings

5.3.12.2 HPI16 Mode

Table 5-34 and Table 5-35 assume testing over recommended operating conditions and $P = 0.5 * \text{processor clock}$ (see Figure 5-32 through Figure 5-34). In the following tables, DS refers to the logical OR of HCS, HDS1, and HDS2, and HD refers to any of the HPI data bus pins (HD0, HD1, HD2, etc.). These timings are shown assuming that HDS is the signal controlling the transfer. See the *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302) for addition information.

Table 5-34. HPI16 Mode Timing Requirements

| | | | MIN | MAX | UNIT |
|--------------------|---|---|-------------|------------------|------|
| $t_{su(HBV-DSL)}$ | Setup time, $\overline{HR/\overline{W}}$ valid before DS falling edge | | 6 | | ns |
| $t_h(DSL-HBV)$ | Hold time, $\overline{HR/\overline{W}}$ valid after DS falling edge | | 5 | | ns |
| $t_{su(HAV-DSH)}$ | Setup time, address valid before DS rising edge (write) | | 5 | | ns |
| $t_{su(HAV-DSL)}$ | Setup time, address valid before DS falling edge (read) | | $-(4P - 6)$ | | ns |
| $t_h(DSH-HAV)$ | Hold time, address valid after DS rising edge | | 1 | | ns |
| $t_w(DSL)$ | Pulse duration, DS low | | 30 | | ns |
| $t_w(DSH)$ | Pulse duration, DS high | | 10 | | ns |
| $t_c(DSH-DSH)$ | Cycle time, DS rising edge to next DS rising edge | Memory accesses with no DMA activity. | Reads | $10P + 30^{(1)}$ | ns |
| | | | Writes | $10P + 10^{(1)}$ | |
| | | Memory accesses with 16-bit DMA activity. | Reads | $16P + 30^{(1)}$ | |
| | | | Writes | $16P + 10^{(1)}$ | |
| | | Memory accesses with 32-bit DMA activity. | Reads | $24P + 30^{(1)}$ | |
| | | | Writes | $24P + 10^{(1)}$ | |
| $t_{su(HDV-DSH)W}$ | Setup time, HD valid before DS rising edge | | 8 | | ns |
| $t_h(DSH-HDV)W$ | Hold time, HD valid after DS rising edge, write | | 2 | | ns |

(1) $P = 0.5 * \text{processor clock}$

Table 5-35. HPI16 Mode Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT |
|-------------------|--|--|-------------------------|------|
| $t_{d(DSL-HDD)}$ | Delay time, DS low to HD driven | 0 | 10 | ns |
| $t_{d(DSL-HDV1)}$ | Delay time, DS low to HD valid for first word of an HPI read | Case 1a: Memory accesses initiated immediately following a write when DMAC is active in 16-bit mode and $t_{w(DSH)}$ was < 18H | $32P + 20 - t_{w(DSH)}$ | ns |
| | | Case 1b: Memory accesses not immediately following a write when DMAC is active in 16-bit mode | $16P + 20$ | |
| | | Case 1c: Memory accesses initiated immediately following a write when DMAC is active in 32-bit mode and $t_{w(DSH)}$ was < 26H | $48P + 20 - t_{w(DSH)}$ | |
| | | Case 1d: Memory access not immediately following a write when DMAC is active in 32-bit mode | $24P + 20$ | |
| | | Case 2a: Memory accesses initiated immediately following a write when DMAC is inactive and $t_{w(DSH)}$ was < 10H | $20P + 20 - t_{w(DSH)}$ | |
| | | Case 2b: Memory accesses not immediately following a write when DMAC is inactive | $10P + 20$ | |
| $t_{d(DSH-HYH)}$ | Delay time, DS high to HRDY high | Memory writes when no DMA is active | $10P + 5$ | ns |
| | | Memory writes with one or more 16-bit DMA channels active | $16P + 5$ | |
| | | Memory writes with one or more 32-bit DMA channels active | $24P + 5$ | |
| $t_{v(HYH-HDV)}$ | Valid time, HD valid after HRDY high | | 7 | ns |
| $t_{h(DSH-HDV)R}$ | Hold time, HD valid after DS rising edge, read | 1 | 6 | ns |
| $t_{d(COH-HYH)}$ | Delay time, CLKOUT rising edge to HRDY high | | 5 | ns |
| $t_{d(DSL-HYL)}$ | Delay time, DS low to HRDY low | | 12 | ns |
| $t_{d(DSH-HYL)}$ | Delay time, DS high to HRDY low | | 12 | ns |

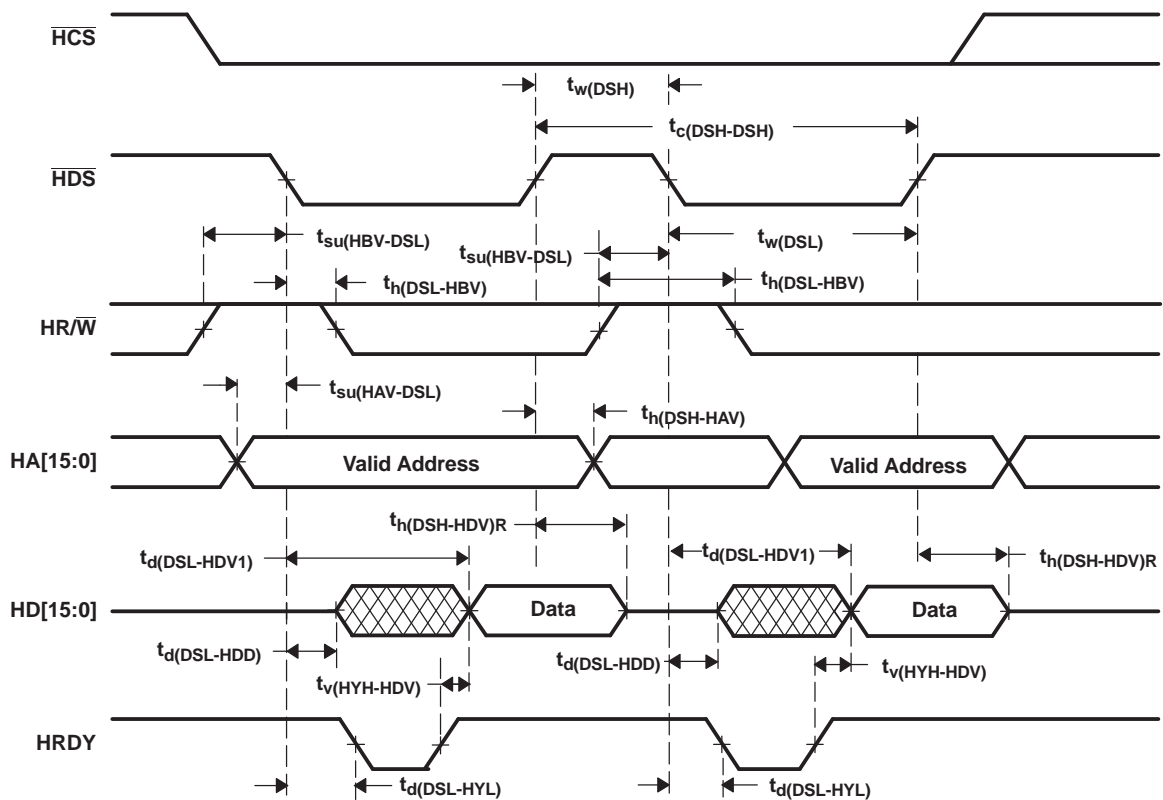


Figure 5-32. HPI-16 Mode, Nonmultiplexed Read Timings

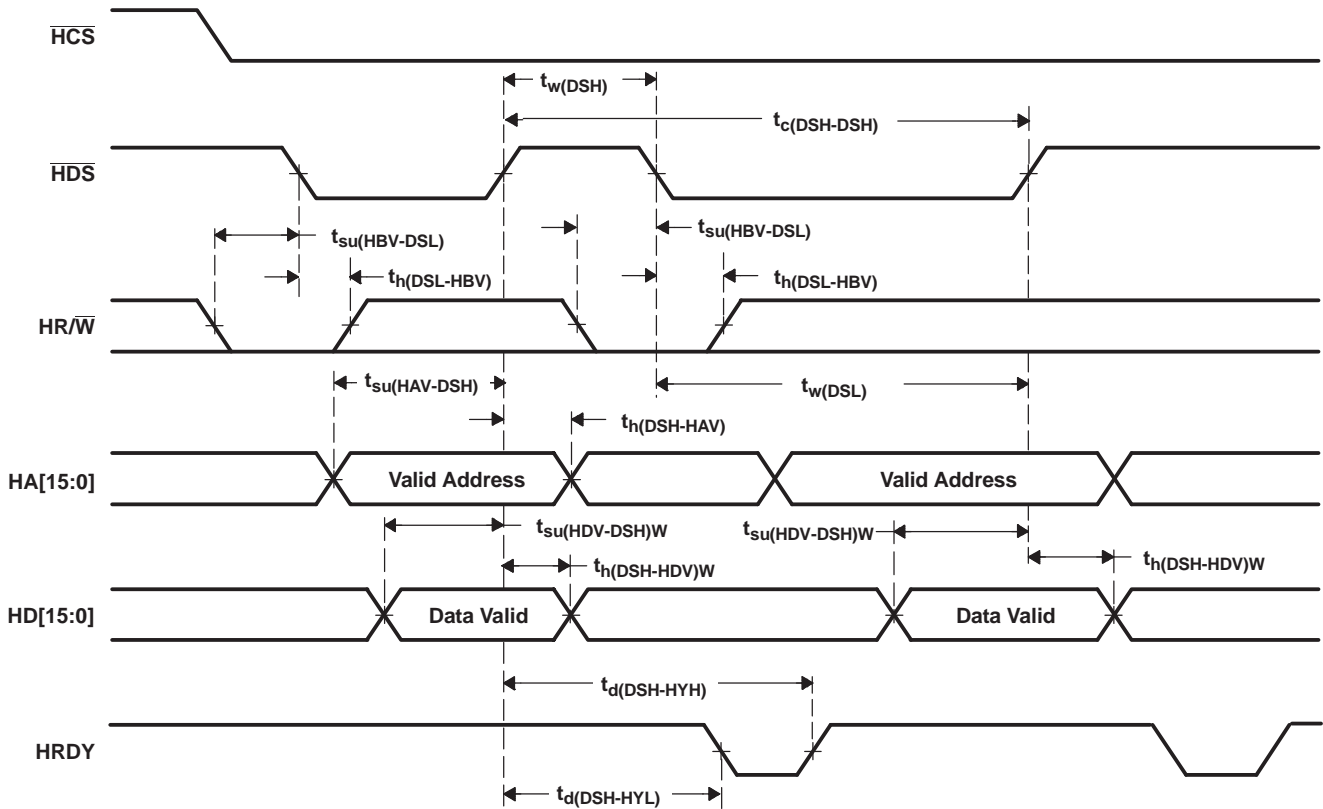


Figure 5-33. HPI-16 Mode, Nonmultiplexed Write Timings

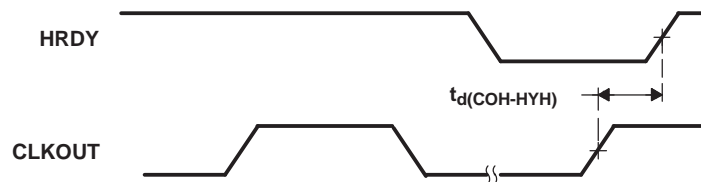


Figure 5-34. HPI-16 Mode, HRDY Relative to CLKOUT

6 Mechanical Data

The following mechanical package diagram(s) reflect the most current released mechanical data available for the designated device(s).

6.1 Package Thermal Resistance Characteristics

[Table 6-1](#) provides the estimated thermal resistance characteristics for the recommended package types used on the device.

Table 6-1. Thermal Resistance Characteristics

| PARAMETER | GGU PACKAGE | PGE PACKAGE | UNIT |
|-----------------|-------------|-------------|------|
| $R_{\theta JA}$ | 38 | 56 | °C/W |
| $R_{\theta JC}$ | 5 | 5 | °C/W |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|---------------------------------|---------|
| TMS320VC5402AGWS16 | OBSOLETE | NFBGA | GWS | 144 | | TBD | Call TI | Call TI | -40 to 100 | DVC5402AGWS 160 | |
| TMS320VC5402APGE16 | OBSOLETE | LQFP | PGE | 144 | | TBD | Call TI | Call TI | 0 to 0 | 320VC5402 APGE 160 TMS | |
| TMS320VC5402AZWS16 | OBSOLETE | NFBGA | ZWS | 144 | | TBD | Call TI | Call TI | -40 to 100 | DVC5402AZWS 160 | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

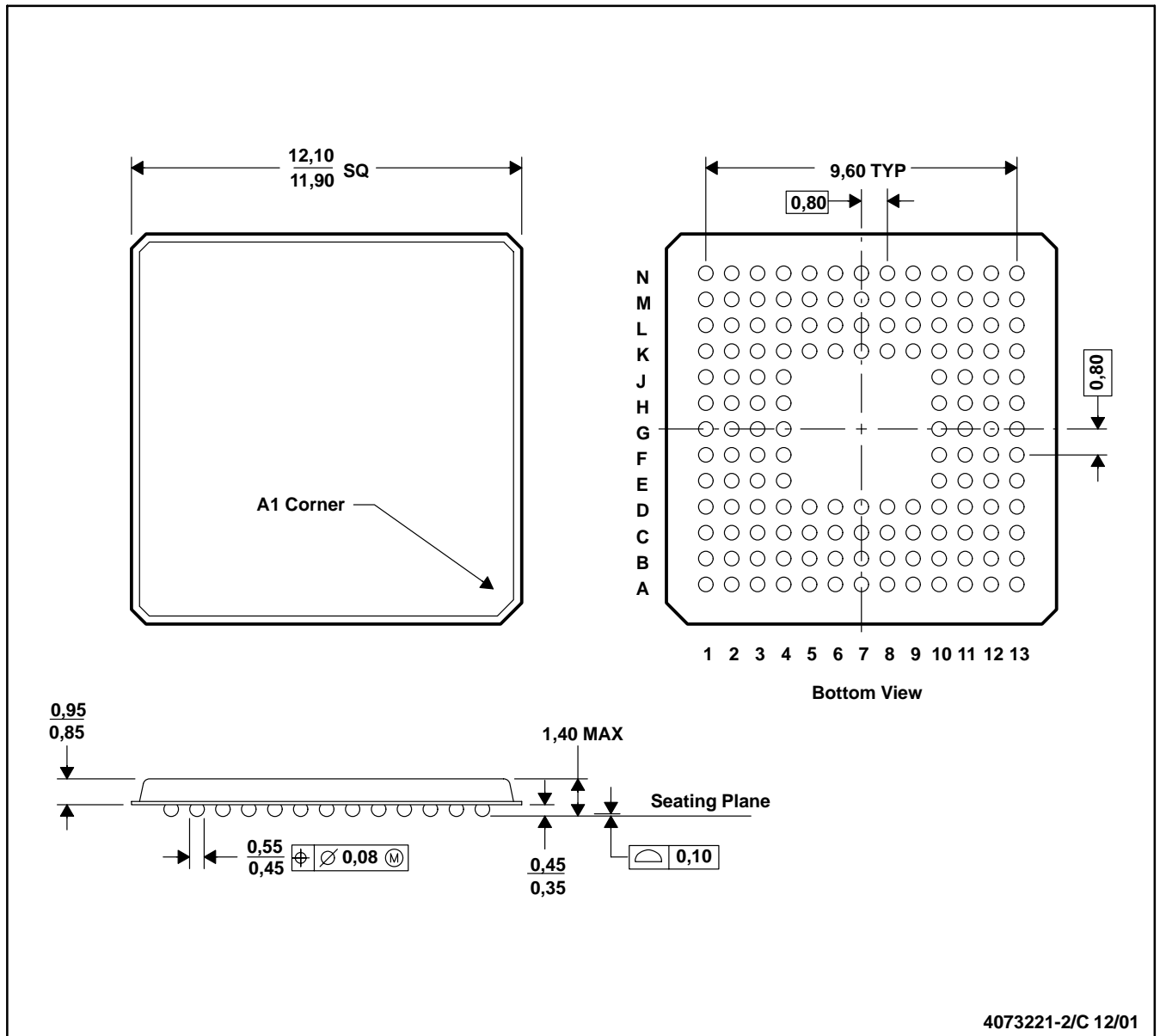
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GGU (S-PBGA-N144)

PLASTIC BALL GRID ARRAY

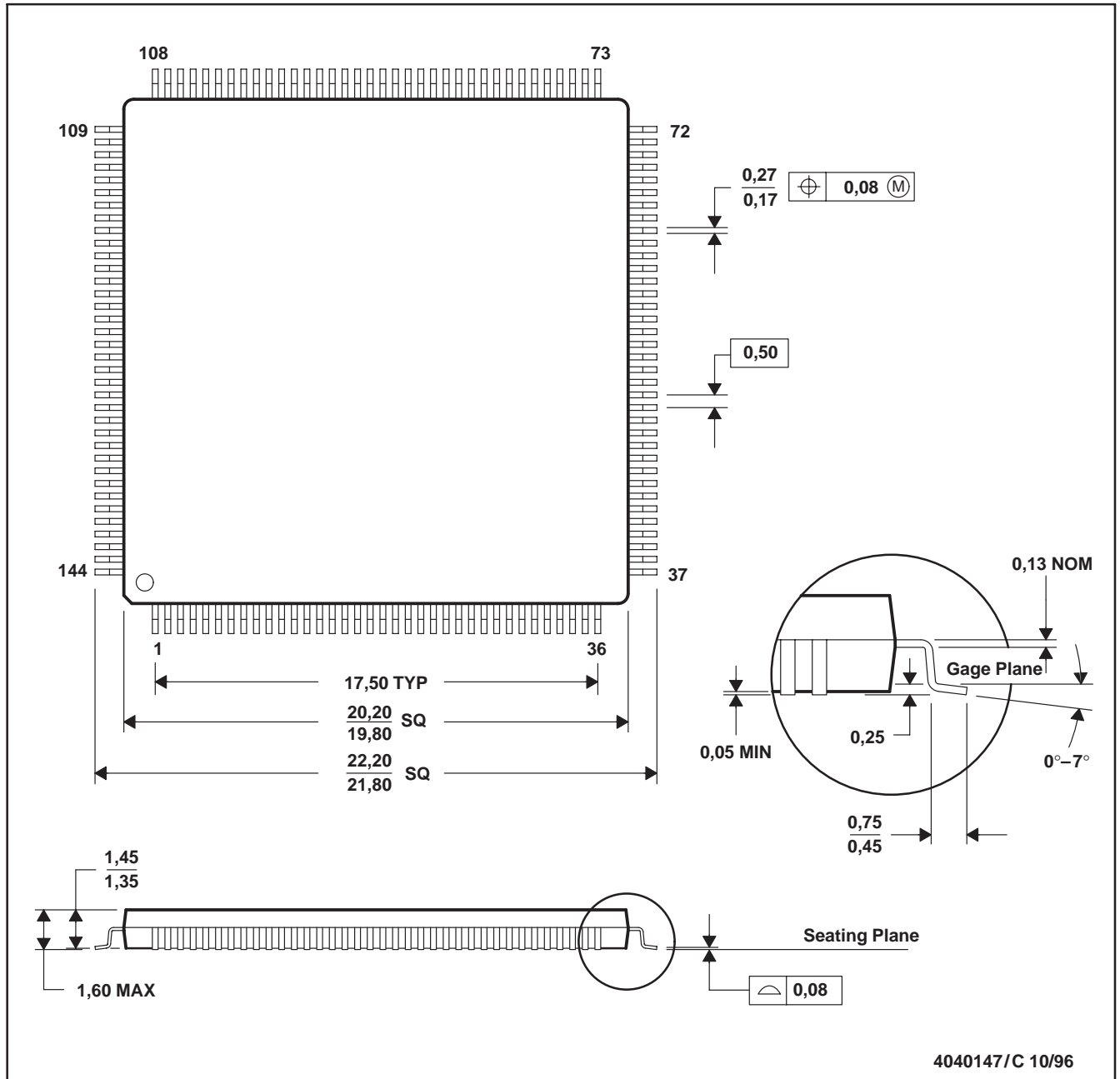


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice
 C. MicroStar BGA™ configuration

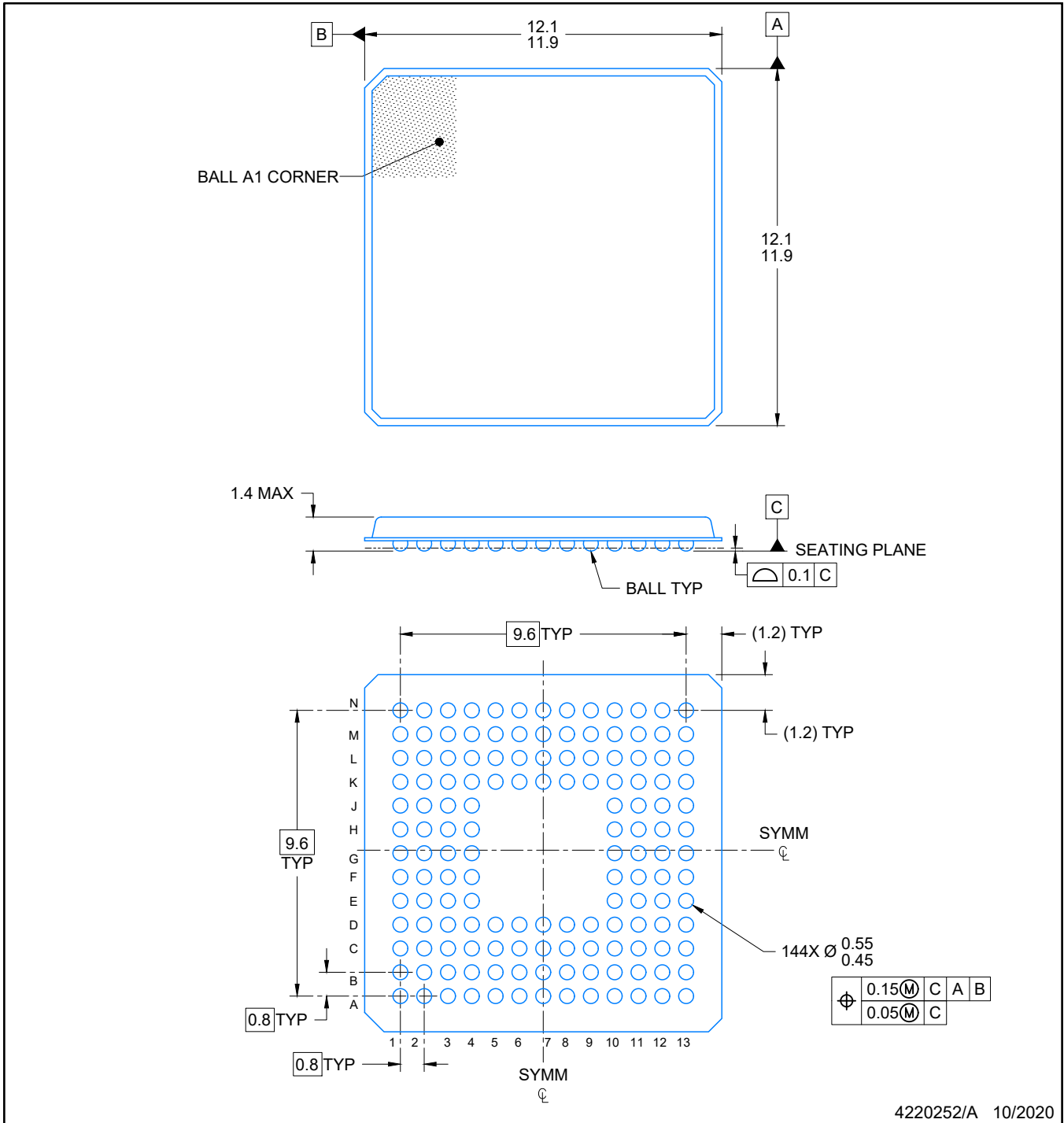
MicroStar BGA is a trademark of Texas Instruments Incorporated.

PGE (S-PQFP-G144)

PLASTIC QUAD FLATPACK

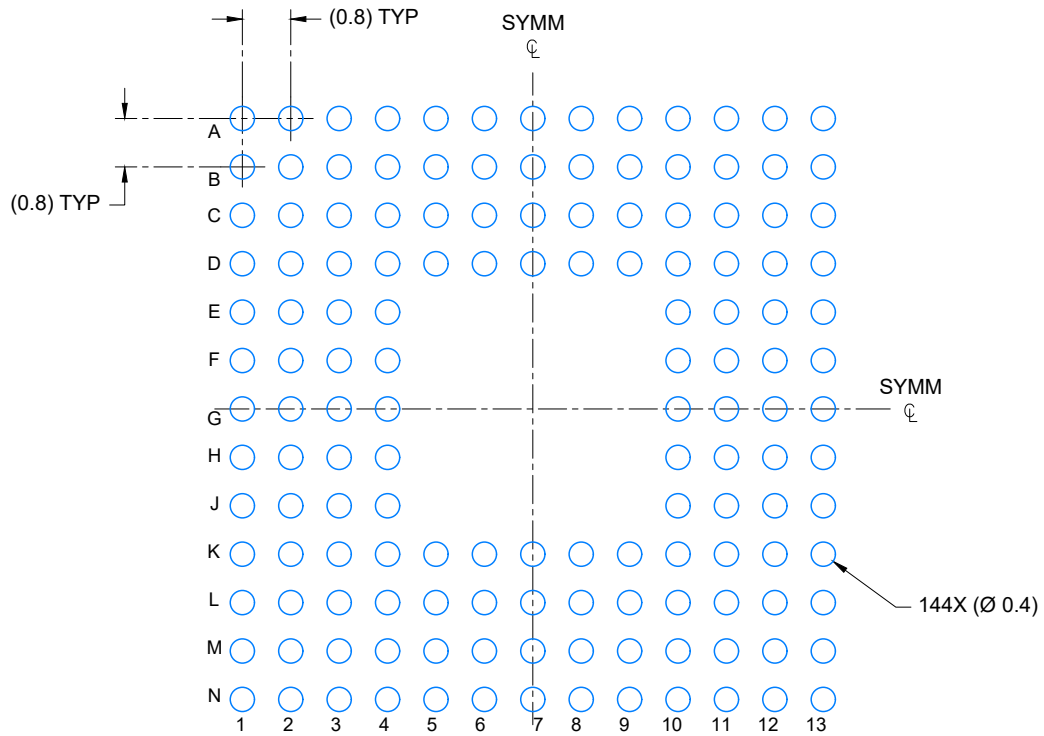


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

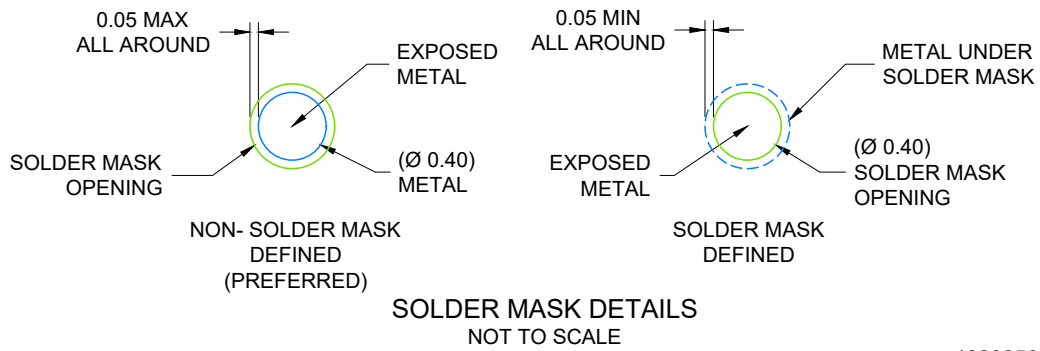


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-Free ball design.



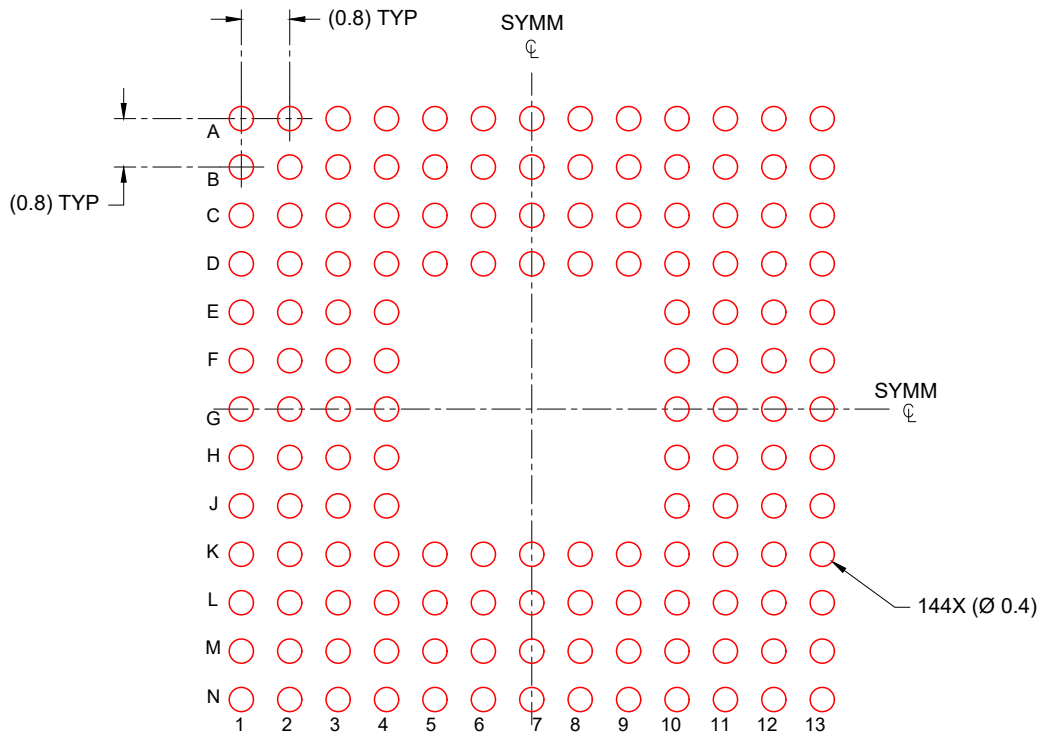
LAND PATTERN EXAMPLE
SCALE: 8X



4220252/A 10/2020

NOTES: (continued)

- 4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.



SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 8X

NOTES: (continued)

- 5. For alternate stencil design recommendations see IPC-7525 or board assembly site preference.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated