TMUX121 Low-Capacitance, 2-Channel, 2:1 Switch with Power-Off Isolation and 1.8-V Logic

1 Features

- Compatible with high-speed I^3C signals
- High performance switch characteristics:
  - Bandwidth (–3 dB): 3.0 GHz
  - R_{ON} (typical): 3 Ω
  - C_{ON} (typical): 1.7 pF
  - T_{PD} (typical): 60 ps
  - T_{SWEK} (typical): 2 ps
- Low current consumption: 12 µA (typical)
- Special features:
  - I_{POFF} protection prevents current leakage in Powered-Down state
  - 1.8 V and 3.3 V compatible control inputs (SEL, $\overline{EN}$)
- 3.3 V supply voltage
- Industrial temperature range: –40 to 125°C
- Compact 10-pin 1.4 mm × 1.8 mm, UQFN package

2 Applications

- I^3C (SenseWire)
- I^3C and I^2C peripheral switching
- Servers
- Handset: smart phone
- Notebook PC
- Tablet: multimedia
- Electronic point-of-sale
- Field instrumentation
- Portable monitor

3 Description

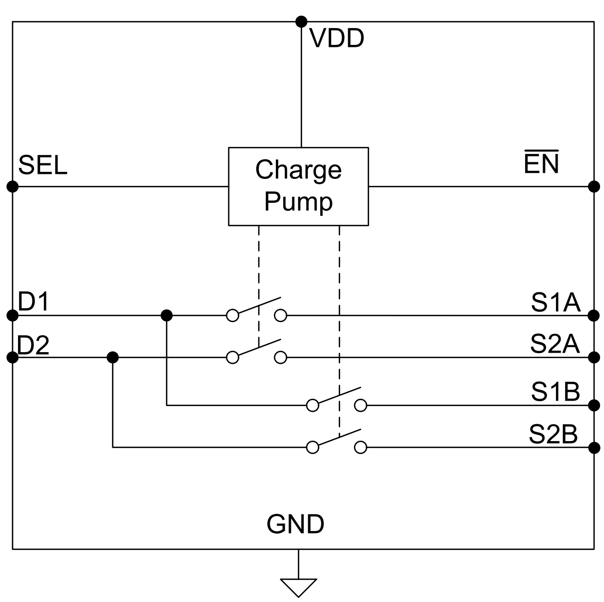
The TMUX121 is a high performance bidirectional 2-channel, 2:1 (SPDT) switch that supports both differential and single ended signals. The TMUX121 is an analog passive switch which features power-off protection forcing all I/O pins to be in high-impedance mode when power is not present on the V_{DD} pin. The select and enable pins of the TMUX121 compatible with 1.8 V and 3.3 V control voltage, allowing them to be directly interfaced with the General purpose I/O (GPIO) from low voltage processors. This, along with the low on-resistance and low on capacitance of the device, make the TMUX121 an excellent choice for supporting switching a wide range of analog signals and digital communication protocol standards, including high-speed standards such as I^3C.

The TMUX121 comes in a small 10-pin UQFN package with only 1.8 mm × 1.4 mm in size, which makes it useful when PCB area is limited.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUX121	NKG (UQFN, 10)	1.8 mm × 1.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Use Case

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4 Revision History

DATE	REVISION	NOTES
August 2023	*	Initial Release

5 Pin Configuration and Functions

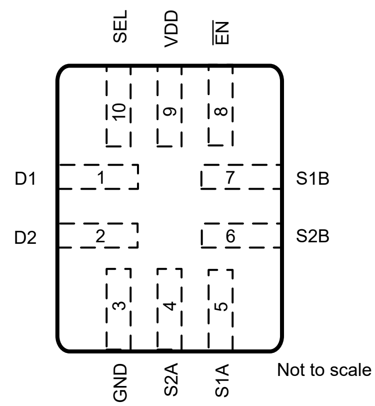


Figure 5-1. TMUX121 NKG Package, 10-Pin UQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
D1	1	I/O	Drain pin 1. Can be an input or output.
D2	2	I/O	Drain pin 2. Can be an input or output.
S1A	5	I/O	Source pin 1A. Can be an input or output.
S2A	4	I/O	Source pin 2A. Can be an input or output.
S1B	7	I/O	Source pin 1B. Can be an input or output.
S2B	6	I/O	Source pin 2B. Can be an input or output.
SEL	10	IN	Switch logic control input. Controls the switch connection as provided in Table 7-1.
$\overline{EN}$	8	IN	Active low enable input. Controls the switch connection as provided in Table 7-1.
VDD	9	P	3.3 V power supply
GND	3	G	Ground

(1) IN = input, I/O = input or output, P = power, G = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.5	4.0	V
V_{EN} or V_{SEL}	Logic control input pin current (SEL, EN)	–0.5	4.0	V
V_D or V_S	Source or drain voltage (Sx, Dx)	–0.5	5.5	V
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature	–40	125	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±5000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
VDD	Power Supply voltage	3.0	3.3	3.6	V
VDD_{RAMP}	Power Supply voltage ramp time	0.1		100	ms
V_D or V_S	Source or drain voltage (Sx, Dx)	0		3.6	V
V_{EN} or V_{SEL}	Logic control input pin current (SEL, EN)	0		3.6	V
I_S or I_D (cont)	Source or drain continuous current (Sx, Dx)			90	mA
T_A	Operating free-air/ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TMUX121 NKG (UQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance - High K	225.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	147.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	147.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Over operating free-air temperature and supply voltage range (unless otherwise noted)
Typical at V_{DD} = 3.3 V T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DDQ}	V_{DD} quiescent supply current	EN = V_{DD}		1.3	4	µA
I_{DD}	V_{DD} supply current	EN = 0 V		11	30	µA
R_{ON}	On-resistance	V_S = 0 V , I_S = –8 mA		3	5.4	Ω
		V_S = 2.4 V , I_S = –8 mA		3.9	8	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V , I_S = –8 mA			0.5	Ω
		V_S = 2.4 V , I_S = –8 mA			0.5	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V and V_S = 2.4 V; I_S = –8 mA		1		Ω
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current (Sx, Dx)	Switch state is on V_D = V_S = 3.6 V			2	µA
		Switch state is on V_D = V_S = 0 V			0.2	µA
$I_{S(OFF)}$	Source off leakage current (Sx)	Switch state is off V_S = 3.6 V			2	µA
$I_{D(OFF)}$	Drain off leakage current (Dx)	Switch state is off V_D = 3.6 V			2	µA
$I_{(POFF)}$	Powered-off leakage current (Sx, Dx)	V_{CC} = 0 V, V_D or V_S = 3.6 V			10	µA
V_{IH}	Logic voltage high (EN, SEL)		1.4		3.6	V
V_{IL}	Logic voltage low (EN, SEL)		0		0.4	
I_{IL}	Input leakage current (EN, SEL)				0.2	µA
I_{IH}	Input leakage current (EN, SEL)				1	µA
I_{IH}	Failsafe Input leakage current (EN, SEL)	V_{CC} = 0 V, V_{EN} or V_{SEL} = 3.6 V			10	µA

6.6 Switching Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input (SEL)	R_L = 50 Ω, C_L = 10 pF			1	µs
t_{ON}	Turn-on time from control input (EN)	R_L = 50 Ω, C_L = 10 pF			16	µs
t_{OFF}	Turn-off time from control input (EN)	R_L = 50 Ω, C_L = 10 pF			0.5	µs
t_{PD}	Switch propagation delay (Sx to Dx or Dx to Sx)			60	80	ps
t_{SKEW_INTRA}	Intra-pair propagation delay skew for same channel			2	10	ps
t_{SKEW_INTER}	Inter-pair propagation delay skew between channels			2	10	ps
BW	–3-dB bandwidth			3		GHz
I_L	Differential insertion loss	f = 10 MHz		-0.3		dB
O_{ISO}	Differential OFF isolation (D to SA/SB)	f = 10 MHz		-56		dB
X_{TALK}	Differential cross-talk (SA to SB or SB to SA)	f = 10 MHz		-64		dB
$C_{S(ON)}$ $C_{D(ON)}$	On capacitance	f = 10 MHz		1.7		pF

6.7 Typical Characteristics

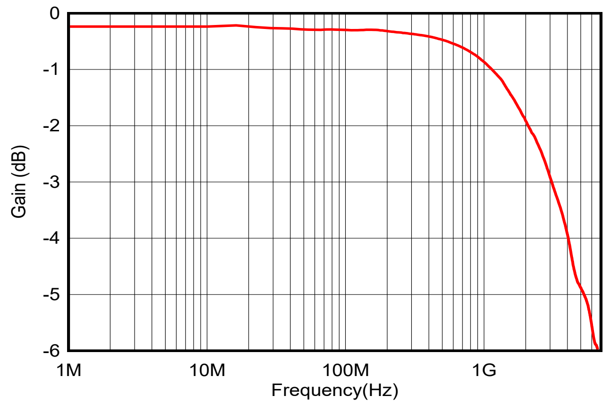


Figure 6-1. Typical Differential Bandwidth vs Frequency

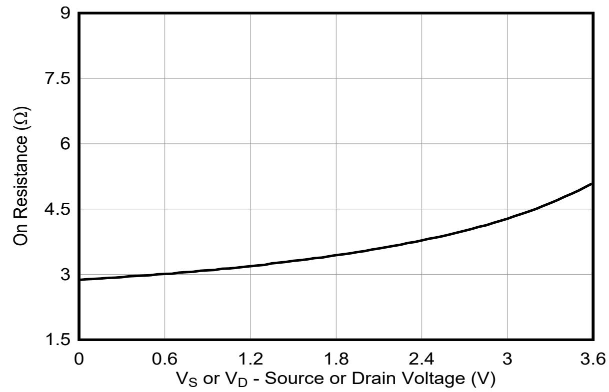


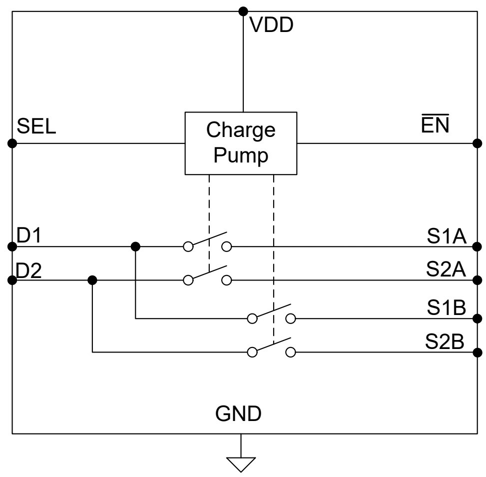
Figure 6-2. R_{ON} vs Common Mode Voltage VCM

7 Detailed Description

7.1 Overview

The TMUX121 is an analog passive 2 channel 2:1 (SPDT) that can work for any low-speed, high-speed, differential or single ended signals. Excellent low capacitance characteristics of the device allow signal switching with minimal attenuation and very little added jitter. The signals must be within the allowable voltage range of 0 to 3.6 V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Low Power Mode

The TMUX121 can be placed in a power saving mode by pulling $\overline{EN}$ high. This reduces the supply power consumption from 12 µA to 1.5 µA. which is extremely beneficial for systems where saving power is critical.

7.4 Device Functional Modes

Table 7-1. Mux Configuration Control Logic for TMUX121 (1)

SEL	$\overline{EN}$	Mux Configuration
L	L	D to SA
H	L	D to SB
X	H	All channels are disabled and Hi-Z

(1) The TMUX121 can tolerate polarity inversions for differential signals. Keep the polarity consistent for all differential pairs.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMUX121 is an analog high-speed mux or demux that can be used for routing differential as well as single ended signals through it. The device can be used for many interfaces including I^2C and I^3C.

An available GPIO pin of a controller or hard tie to voltage level H or L can easily control the mux or demux selection pin (SEL) of the device as an application requires. The switch path is passive and therefore bidirectional.

8.2 Typical Applications

8.2.1 Signal Expansion (I^3C and I^2C)

There are many applications in which microprocessors or controllers have a limited number of I/Os. The TMUX121 solution can effectively expand the limited I/Os by switching between multiple buses to interface them to a single microprocessor or controller. A common application where the TMUX121 is as a I^3C 1:2 multiplexer. In this application, the TMUX121 is used to route communicating between different peripherals from a single controller or driver within a server, as shown in Figure 8-1. The high bandwidth of the TMUX121 will preserve signal integrity at even the fastest communication protocols that may be used in server applications, such as I^3C. Also, because I^3C is backwards compatible, any of the peripherals can also be I^2C, and the TMUX121 will still support it.

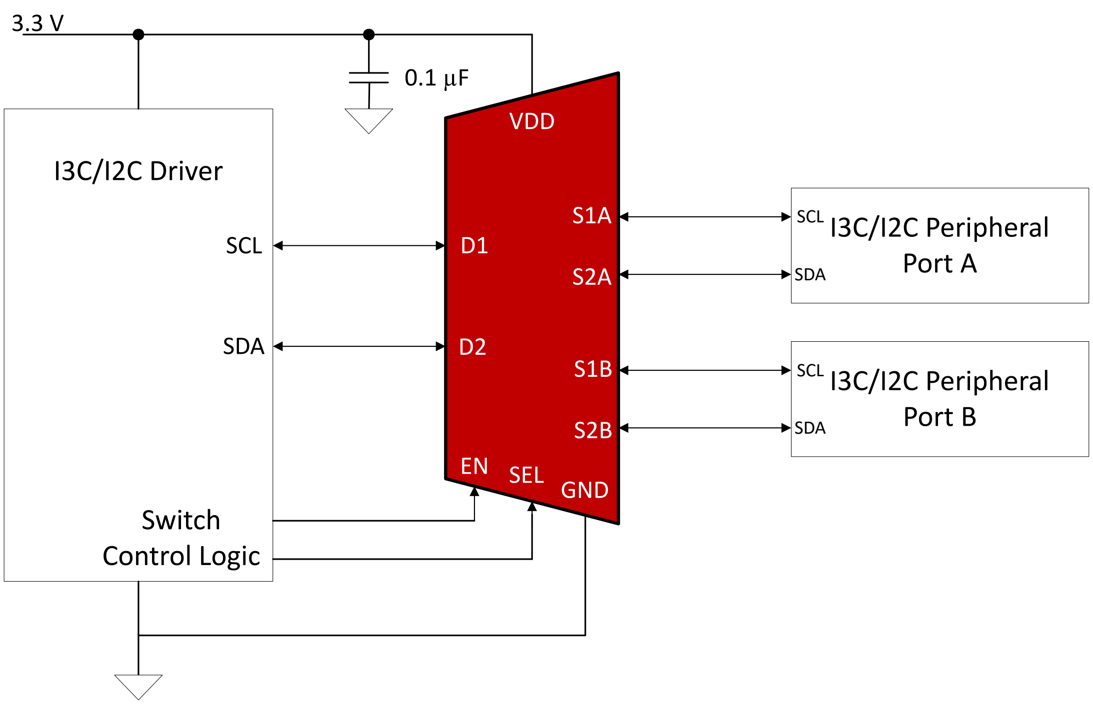


Figure 8-1. Typical Application

8.2.1.1 Design Requirements

Table 8-1. TMUX121 I3C Compatibility

	I3C Requirements	TMUX121 Specification
Voltage	1.0 V, 1.2 V, 1.8 V, 3.3 V	0-3.6 V
Frequency	Up to 12.5 MHz	3 GHz Bandwidth
Capacitance	50 pF maximum bus capacitance	< 2 pF On or Off Capacitance

8.2.1.2 Detailed Design Procedure

The TMUX121 supports I3C standard by maintaining signal integrity through the switch. Table 8-1 details how the TMUX121 specifications make this device optimal for switching I3C signals. Choosing a multiplexer with very low capacitance helps reduces the impact to your total capacitance budget. This can enable more design flexibility keeping the total bus capacitance under 50 pF such as: longer traces, more ICs, multiple buses, and so forth.

8.2.1.3 Application Curves

Figure 8-2 shows bandwidth of the TMUX121. This can easily support the max data rate of the I3C standard. A combination of low on-resistance, low capacitance, and low added jitter from the device allows it to be used for I3C.

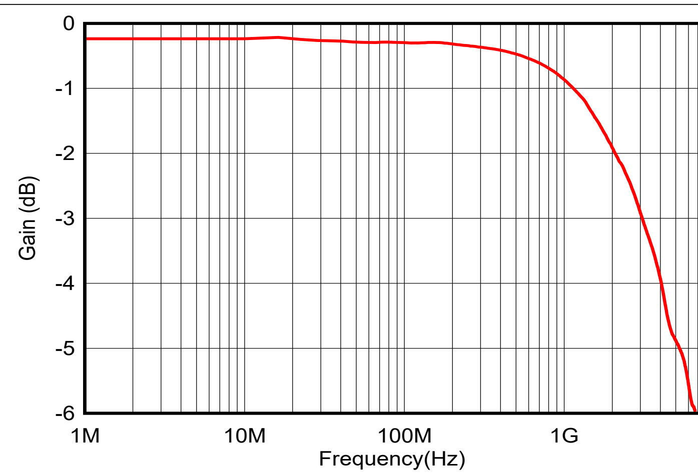


Figure 8-2. Typical Differential Bandwidth vs Frequency

8.3 Power Supply Recommendations

The TMUX121 does not require a power supply sequence. However, TI recommends to enable the device after VDD is stable and in specification. TI also recommends placing a bypass capacitor as close to the supply pin VDD as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

8.4 Layout

8.4.1 Layout Guidelines

Place supply bypass capacitors as close to VDD pin as possible and avoid placing the bypass capacitors near the high speed traces.

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. Doing this reduces reflections on the signal traces by minimizing impedance discontinuities. Avoid stubs on the high-speed signals because they cause signal reflections. Route all high-speed signal traces over continuous planes (VDD or GND) with no interruptions.

Due to high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 8-3.

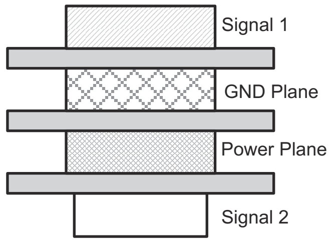


Figure 8-3. Four-Layer Board Stack-Up

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

For high speed layout guidelines, refer to *High-Speed Layout Guidelines* application note.

8.4.2 Layout Example

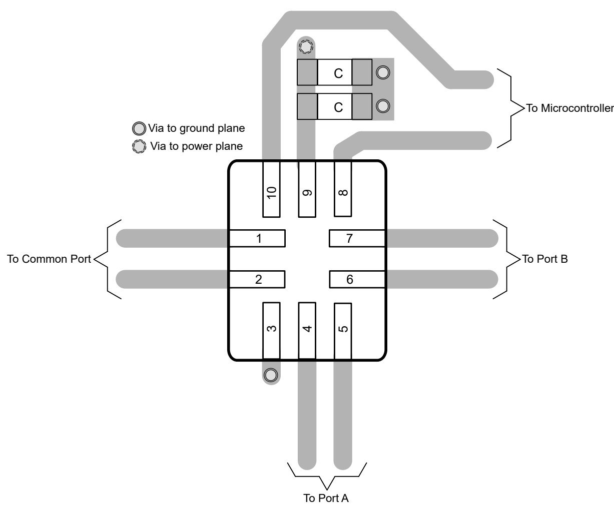


Figure 8-4. TMUX121 Layout Example

9 Device and Documentation Support

9.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *High-Speed Layout Guidelines* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX121NKGR	Active	Production	UQFN (NKG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OJ
TMUX121NKGR.A	Active	Production	UQFN (NKG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OJ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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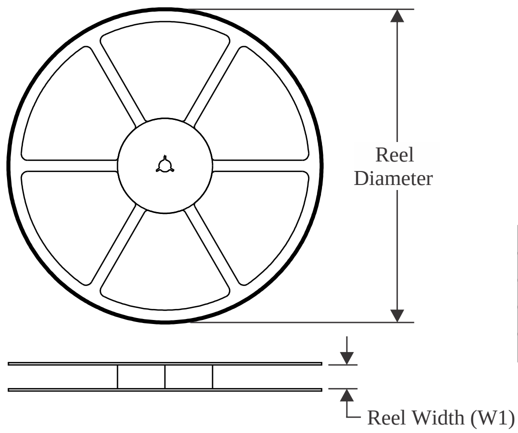
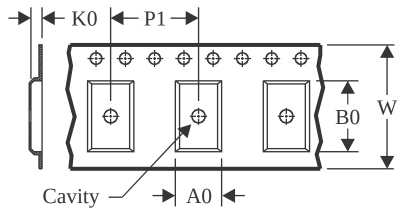
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

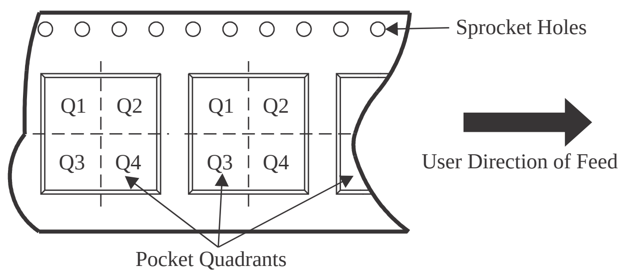


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

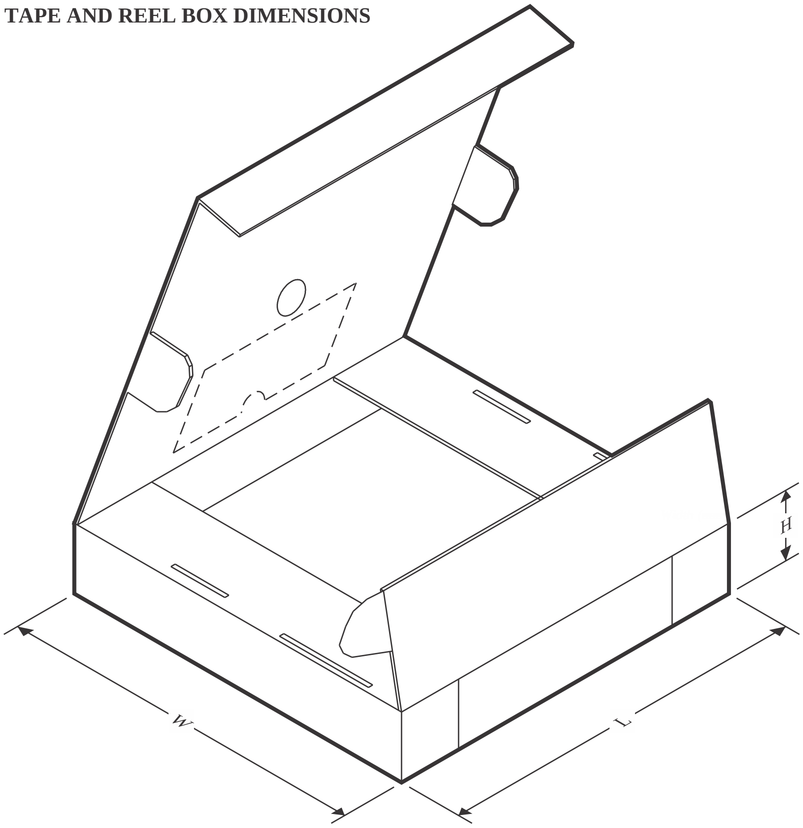
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

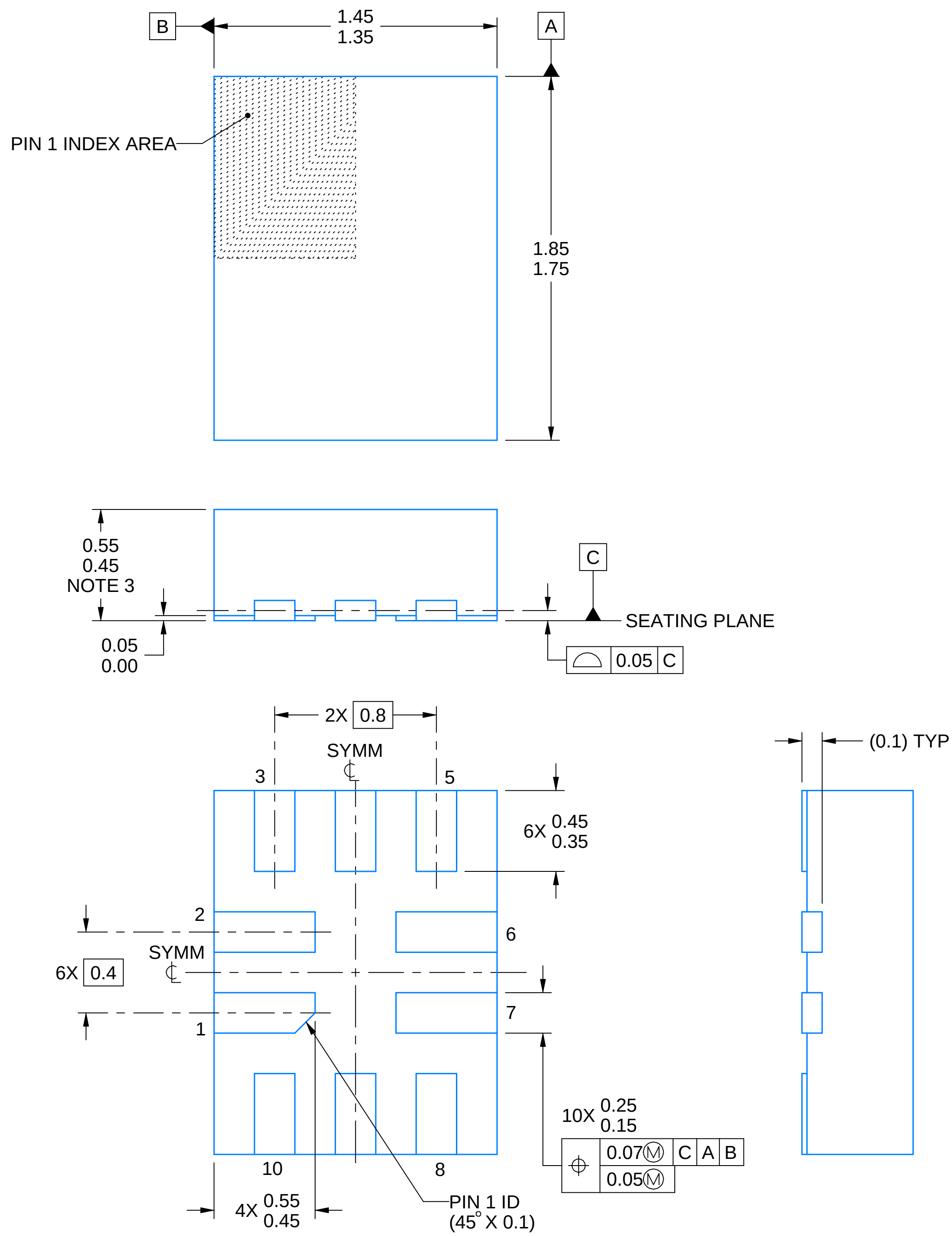
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX121NKGR	UQFN	NKG	10	3000	180.0	8.4	1.6	2.0	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX121NKGR	UQFN	NKG	10	3000	210.0	185.0	35.0



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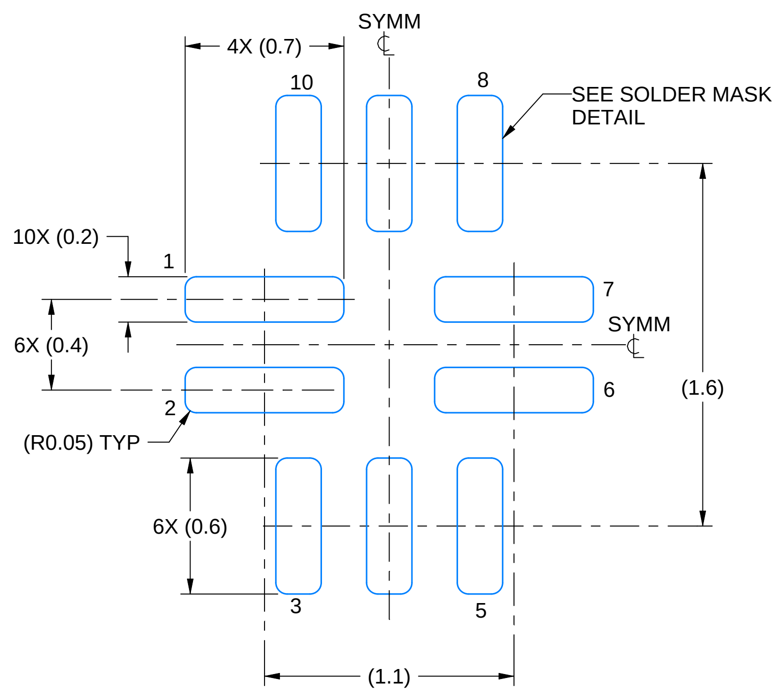
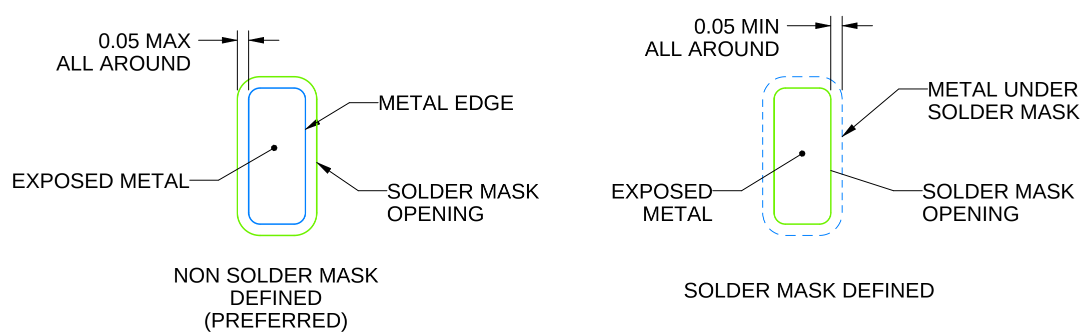
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

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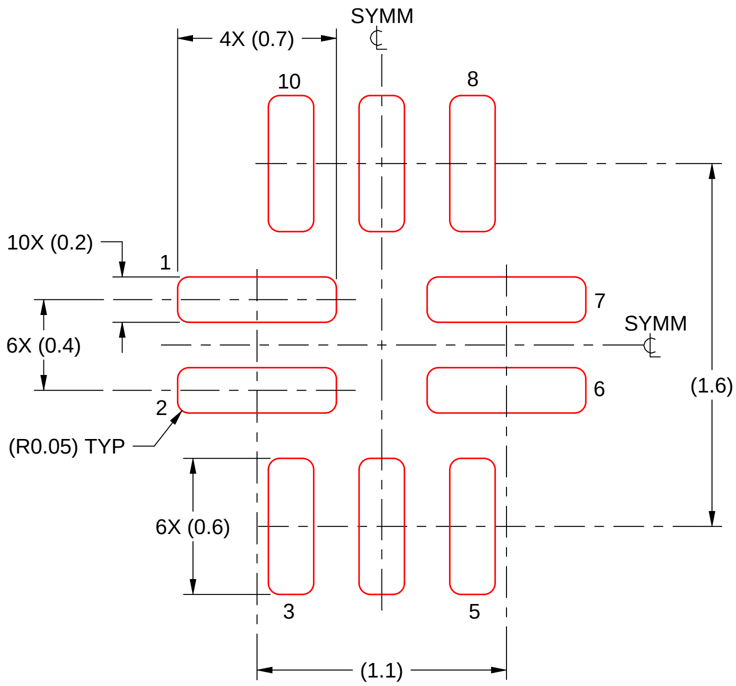
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.