TEXAS INSTRUMENTS
TMUX7221, TMUX7222
SCDS444B – FEBRUARY 2023 – REVISED MAY 2024

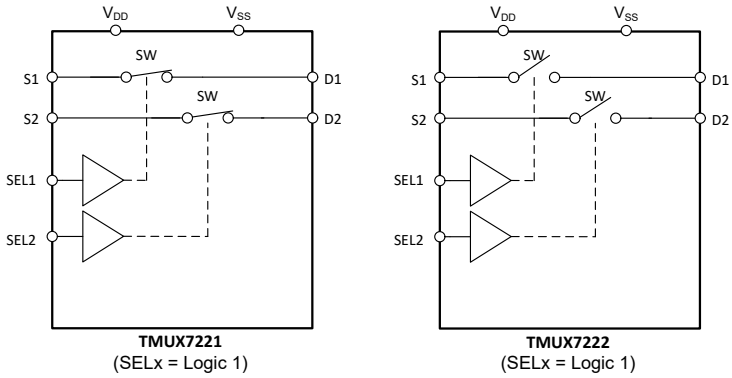
TMUX722x 44 V, Low-RON, 1:1 (SPST), 2-Channel Precision Switches with Latch-Up Immunity and 1.8-V Logic

1 Features

- Latch-up immune
- Dual supply range: ±4.5 V to ±22 V
- Single supply range: 4.5 V to 44 V
- Low on-resistance: 2.1 Ω
- –40°C to +125°C operating temperature
- 1.8 V logic compatible
- Integrated pull-down resistor on logic pins
- Fail-safe logic
- Rail-to-rail operation
- Bidirectional operation

2 Applications

- Optical networking
- Optical test equipment
- HVAC controller
- Ultrasound scanners
- Active oscilloscope probes
- Factory automation and industrial controls
- Programmable logic controllers (PLC)
- Analog input modules
- Semiconductor test
- Patient monitoring and diagnostics
- Wired networking
- Data acquisition systems



Block Diagram

3 Description

The TMUX722x are complementary metal-oxide semiconductor (CMOS) switches with latch-up immunity in a dual channel, 1:1 (SPST) configuration. These devices work with a single supply (4.5 V to 44 V), dual supplies (±4.5 V to ±22 V), or asymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5 V). The TMUX722x supports bidirectional analog and digital signals on the source (Sx) and drain (D) pins ranging from V_{SS} to V_{DD}.

The TMUX722x can be enabled or disabled by controlling the SEL pins, turning on signal path 1 (S1 to D1) or signal path 2 (S2 to D2). All logic control inputs support logic levels from 1.8 V to V_{DD}, allowing for both TTL and CMOS logic compatibility when operating in the valid supply voltage range. Fail-safe logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. For more information, see Section 7.3.5.

The TMUX72xx family provides latch-up immunity, preventing undesirable high current events between parasitic structures within the device typically caused by overvoltage events. A latch-up condition typically continues until the power supply rails are turned off and can lead to device failure. The latch-up immunity feature allows the TMUX72xx family of switches and multiplexers to be used in harsh environments.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUX7221 TMUX7222	DGS (VSSOP, 10)	3 mm × 4.9 mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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4 Pin Configuration and Functions

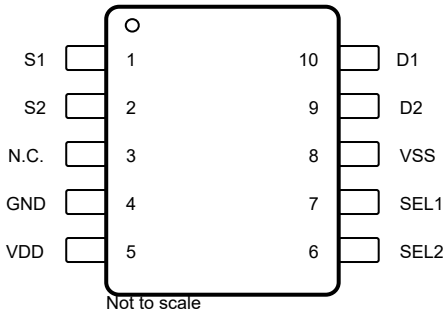


Figure 4-1. DGS Package, 10-Pin VSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION[2]
NAME	NO.		
S1	1	I/O	Source pin 1. Can be an input or output.
S2	2	I/O	Source pin 2. Can be an input or output.
N.C.	3	—	No internal connection. Can be shorted to GND or left floating.
GND	4	P	Ground (0 V) reference
V_{DD}	5	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
SEL2	6	I	Logic control input, has internal pull-down resistor. Controls the switch connection. For more information, see Section 7.5.
SEL1	7	I	Logic control input, has internal pull-down resistor. Controls the switch connection. For more information, see Section 7.5
V_{SS}	8	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
D2	9	I/O	Drain pin 2. Can be an input or output.
D1	10	I/O	Drain pin 1. Can be an input or output.

(1) I = input, O = output, I/O = input and output, P = power.
(2) For what to do with unused pins, refer to Section 7.4.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{DD} – V_{SS}$	Supply voltage		48	V
V_{DD}		–0.5	48	V
V_{SS}		–48	0.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SELx)	–0.5	48	V
I_{SEL} or I_{EN}	Logic control input pin current (SELx)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(3)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)		I_{DC} + 10 %(4)	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation (VSSOP)(5)		450	mW

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.
(5) For VSSOP package: P_{tot} derates linearly above T_A = 70°C by 6.7mW/°C.

5.2 ESD Ratings

			VALUE	UNIT
TMUX722x				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC[1]		TMUX722x DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	154.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	73.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ [1]	Power supply voltage differential	4.5		44	V
V_{DD}	Positive power supply voltage	4.5		44	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Address or enable pin voltage	0		44	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} [2]	mA
T_A	Ambient temperature	–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ (V_{DD} – V_{SS}) ≤ 44 V, and the minimum V_{DD} is met.
(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

5.5 Source or Drain Continuous Current

at supply voltage of V_{DD} ± 10%, V_{SS} ± 10 % (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC}) [2]		T_A = 25°C	T_A = 85°C	T_A = 125°C	UNIT
PACKAGE	TEST CONDITIONS				
DGS (VSSOP)	+44 V Single Supply[1]	380	260	130	mA
	±15 V Dual Supply	380	260	130	mA
	+12 V Single Supply	280	190	100	mA
	±5 V Dual Supply	240	160	90	mA

(1) Specified for nominal supply voltage only.
(2) Refer to Total power dissipation (P_{tot}) limits in *Absolute Maximum Ratings* table that must be followed with max continuous current specification.

5.6 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA	25°C		2.1	2.9	Ω
			–40°C to +85°C			3.8	Ω
			–40°C to +125°C			4.5	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA	25°C		0.05	0.25	Ω
			–40°C to +85°C			0.3	Ω
			–40°C to +125°C			0.35	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_S = –10 mA	25°C		0.5	0.6	Ω
			–40°C to +85°C			0.7	Ω
			–40°C to +125°C			0.85	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.01		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–0.15	0.05	0.15	nA
			–40°C to +85°C	–1.6		1.6	nA
			–40°C to +125°C	–15		15	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–0.15	0.05	0.15	nA
			–40°C to +85°C	–1.6		1.6	nA
			–40°C to +125°C	–15		15	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V	25°C	–0.15	0.05	0.15	nA
			–40°C to +85°C	–1.6		1.6	nA
			–40°C to +125°C	–15		15	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		1	2.5	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		30	47	µA
			–40°C to +85°C			55	µA
			–40°C to +125°C			72	µA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		7	15	µA
			–40°C to +85°C			20	µA
			–40°C to +125°C			30	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.7 ±15 V Dual Supply: Switching Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		145	180	ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			200	ns
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		100	180	ns
			–40°C to +85°C			195	ns
			–40°C to +125°C			210	ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF	25°C		0.19		ms
			–40°C to +85°C		0.2		ms
			–40°C to +125°C		0.2		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF	25°C		500		ps
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF	25°C		-15		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz	25°C		–114		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1MHz	25°C		–93		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V	25°C		45		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.18		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–71		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0005		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		25		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		33		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		120		pF

5.8 ±20 V Dual Supply: Electrical Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V I_D = –10 mA	25°C		1.9	2.7	Ω
			–40°C to +85°C			3.5	Ω
			–40°C to +125°C			4.2	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15 V to +15 V I_D = –10 mA	25°C		0.04	0.22	Ω
			–40°C to +85°C			0.28	Ω
			–40°C to +125°C			0.3	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –15 V to +15 V I_S = –10 mA	25°C		0.3	0.75	Ω
			–40°C to +85°C			0.9	Ω
			–40°C to +125°C			1.2	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.009		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–1.5	0.05	1.5	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–24		24	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–1.5	0.05	1.5	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–24		24	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is on V_S = V_D = ±15 V	25°C	–1.5	0.05	1.5	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–24		24	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.5	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 22 V, V_{SS} = –22 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		38	55	µA
			–40°C to +85°C			61	µA
			–40°C to +125°C			81	µA
I_{SS}	V_{SS} supply current	V_{DD} = 22 V, V_{SS} = –22 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		8	15	µA
			–40°C to +85°C			19	µA
			–40°C to +125°C			37	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.9 ±20 V Dual Supply: Switching Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		110	170	ns
			–40°C to +85°C			185	ns
			–40°C to +125°C			200	ns
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		90	180	ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			200	ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF	25°C		0.18		ms
			–40°C to +85°C		0.2		ms
			–40°C to +125°C		0.2		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF	25°C		500		ps
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF	25°C		-20		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz	25°C		–112		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1MHz	25°C		–93		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V	25°C		45		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.16		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–69		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 20 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0005		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		25		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		32		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		120		pF

5.10 44 V Single Supply: Electrical Characteristics

V_{DD} = +44 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +44 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 40 V I_D = –10 mA	25°C		2.2	2.8	Ω
			–40°C to +85°C			3.6	Ω
			–40°C to +125°C			4.2	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 40 V I_D = –10 mA	25°C		0.1	0.23	Ω
			–40°C to +85°C			0.3	Ω
			–40°C to +125°C			0.35	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 40 V I_D = –10 mA	25°C		0.2	1	Ω
			–40°C to +85°C			1.3	Ω
			–40°C to +125°C			1.5	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 22 V, I_S = –10 mA	–40°C to +125°C		0.008		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 44 V, V_{SS} = 0 V Switch state is off V_S = 40 V / 1 V V_D = 1 V / 40 V	25°C	–5	0.05	5	nA
			–40°C to +85°C	–10		10	nA
			–40°C to +125°C	–35		35	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 44 V, V_{SS} = 0 V Switch state is off V_S = 40 V / 1 V V_D = 1 V / 40 V	25°C	–5	0.05	5	nA
			–40°C to +85°C	–10		10	nA
			–40°C to +125°C	–35		35	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 44 V, V_{SS} = 0 V Switch state is on V_S = V_D = 40 V or 1 V	25°C	–5	0.05	5	nA
			–40°C to +85°C	–10		10	nA
			–40°C to +125°C	–35		35	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.5	2.75	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 44 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		40	62	µA
			–40°C to +85°C			70	µA
			–40°C to +125°C			90	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.11 44 V Single Supply: Switching Characteristics

V_{DD} = +44 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +44 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF	25°C		120	168	ns
			–40°C to +85°C			185	ns
			–40°C to +125°C			195	ns
t_{OFF}	Turn-off time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF	25°C		120	180	ns
			–40°C to +85°C			200	ns
			–40°C to +125°C			205	ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF	25°C		0.15		ms
			–40°C to +85°C		0.17		ms
			–40°C to +125°C		0.17		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF	25°C		500		ps
Q_{INJ}	Charge injection	V_S = 22 V, C_L = 100 pF	25°C		–16		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		–112		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz	25°C		–93		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V	25°C		45		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.18		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–70		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 22 V, V_{BIAS} = 22 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0004		%
$C_{S(OFF)}$	Source off capacitance	V_S = 22 V, f = 1 MHz	25°C		25		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 22 V, f = 1 MHz	25°C		34		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 22 V, f = 1 MHz	25°C		120		pF

5.12 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 10 V I_D = –10 mA	25°C		4.6	6	Ω
			–40°C to +85°C			7.5	Ω
			–40°C to +125°C			8.4	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 10 V I_D = –10 mA	25°C		0.08	0.2	Ω
			–40°C to +85°C			0.32	Ω
			–40°C to +125°C			0.35	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 10 V I_S = –10 mA	25°C		1.2	2	Ω
			–40°C to +85°C			2.2	Ω
			–40°C to +125°C			2.4	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6 V, I_S = –10 mA	–40°C to +125°C		0.017		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C	–0.5	0.05	0.5	nA
			–40°C to +85°C	–2		2	nA
			–40°C to +125°C	–12		12	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C	–0.5	0.05	0.5	nA
			–40°C to +85°C	–2		2	nA
			–40°C to +125°C	–12		12	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V	25°C	–0.5	0.05	0.5	nA
			–40°C to +85°C	–2		2	nA
			–40°C to +125°C	–12		12	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.5	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		30	40	µA
			–40°C to +85°C			50	µA
			–40°C to +125°C			62	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.13 12 V Single Supply: Switching Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	25°C		120	180	ns
			–40°C to +85°C			210	ns
			–40°C to +125°C			230	ns
t_{OFF}	Turn-off time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	25°C		130	210	ns
			–40°C to +85°C			235	ns
			–40°C to +125°C			250	ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF	25°C		0.19		ms
			–40°C to +85°C		0.2		ms
			–40°C to +125°C		0.2		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF	25°C		500		ps
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 100 pF	25°C		–6		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		–112		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz	25°C		–93		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V	25°C		60		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.3		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–76		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0009		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6 V, f = 1 MHz	25°C		30		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 6 V, f = 1 MHz	25°C		38		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 6 V, f = 1 MHz	25°C		110		pF

5.14 Typical Characteristics

at T_A = 25°C

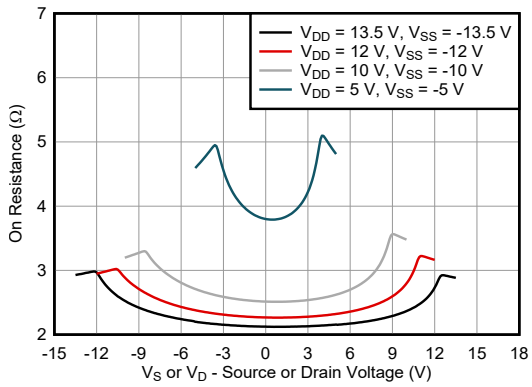


Figure 5-1. On-Resistance vs Source or Drain Voltage – Dual Supply

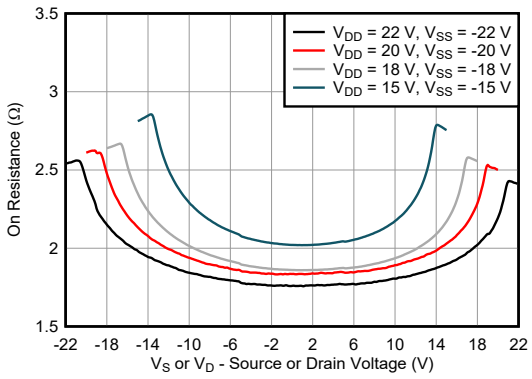


Figure 5-2. On-Resistance vs Source or Drain Voltage – Dual Supply

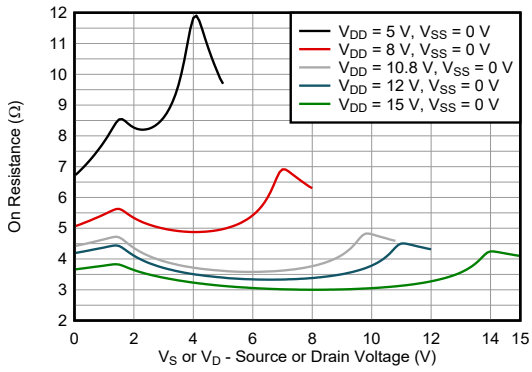


Figure 5-3. On-Resistance vs Source or Drain Voltage – Single Supply

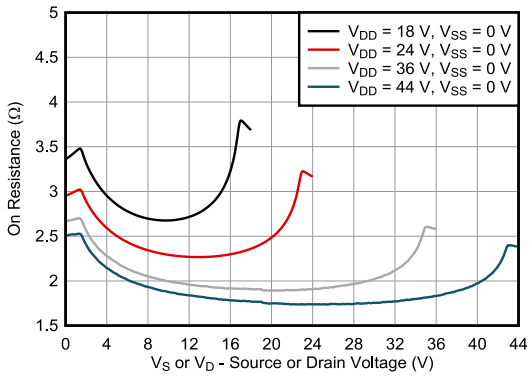
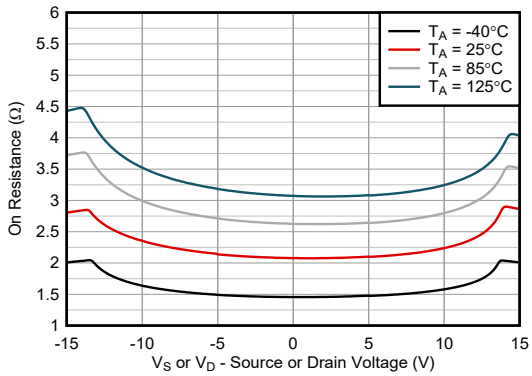
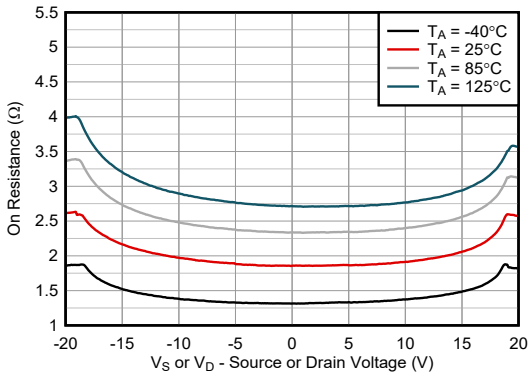


Figure 5-4. On-Resistance vs Source or Drain Voltage – Single Supply



V_{DD} = 15 V, V_{SS} = -15 V

Figure 5-5. On-Resistance vs Temperature

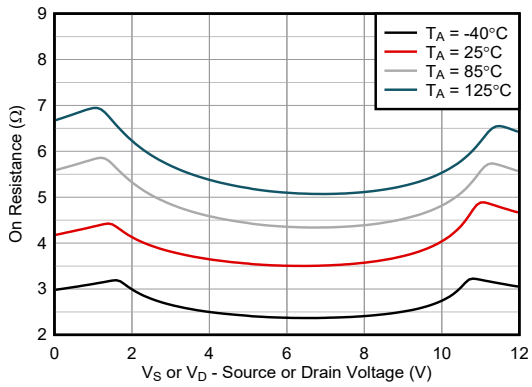


V_{DD} = 20 V, V_{SS} = -20 V

Figure 5-6. On-Resistance vs Temperature

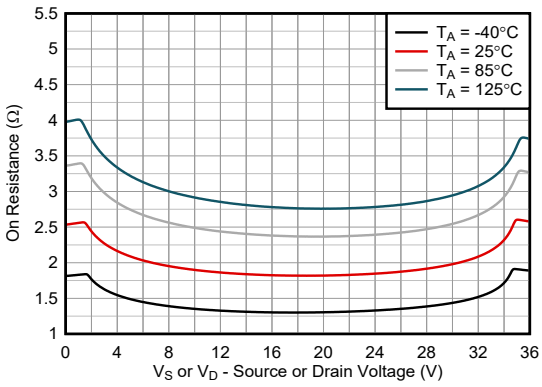
5.14 Typical Characteristics (continued)

at T_A = 25°C



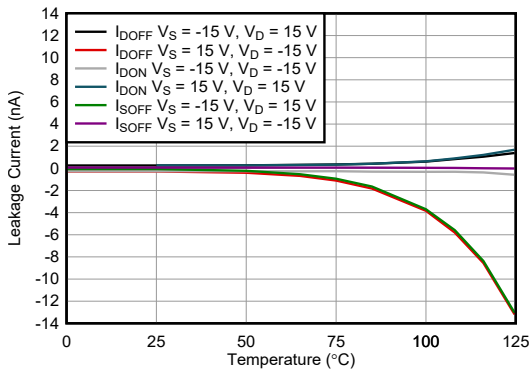
V_{DD} = 12 V, V_{SS} = 0 V

Figure 5-7. On-Resistance vs Temperature



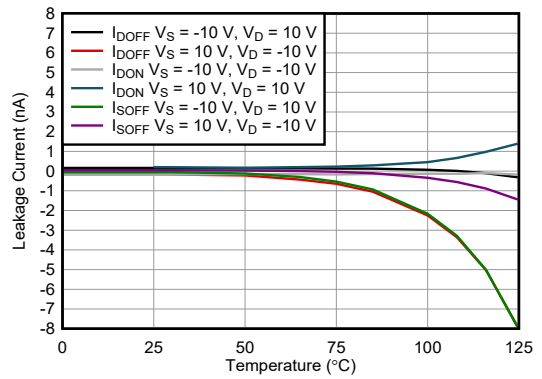
V_{DD} = 36 V, V_{SS} = 0 V

Figure 5-8. On-Resistance vs Temperature



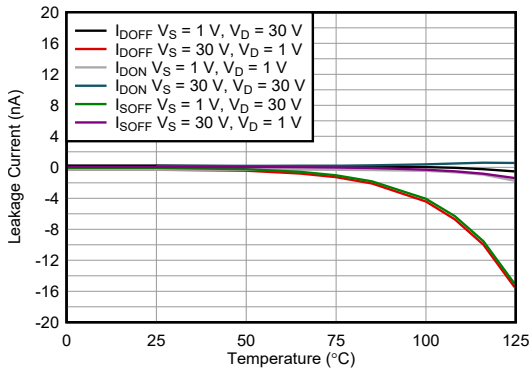
V_{DD} = 20 V, V_{SS} = -20 V

Figure 5-9. Leakage Current vs Temperature



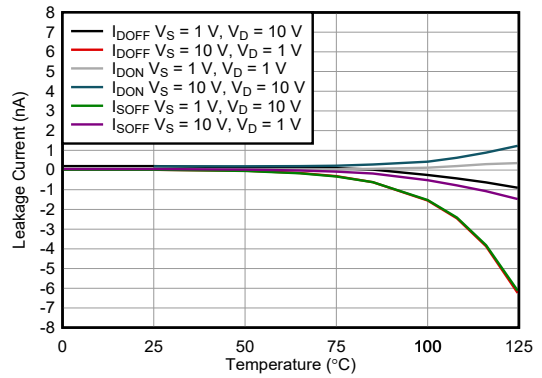
V_{DD} = 15 V, V_{SS} = -15 V

Figure 5-10. Leakage Current vs Temperature



V_{DD} = 36 V, V_{SS} = 0 V

Figure 5-11. Leakage Current vs Temperature



V_{DD} = 12 V, V_{SS} = 0 V

Figure 5-12. Leakage Current vs Temperature

5.14 Typical Characteristics (continued)

at T_A = 25°C

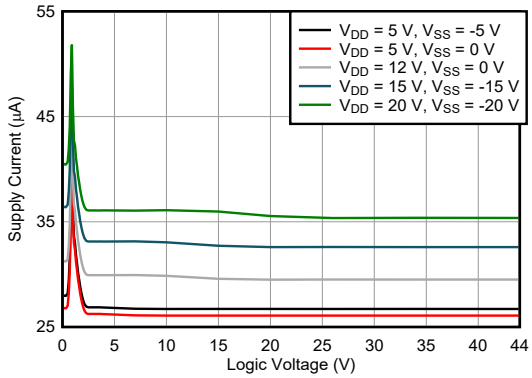


Figure 5-13. Supply Current vs Logic Voltage

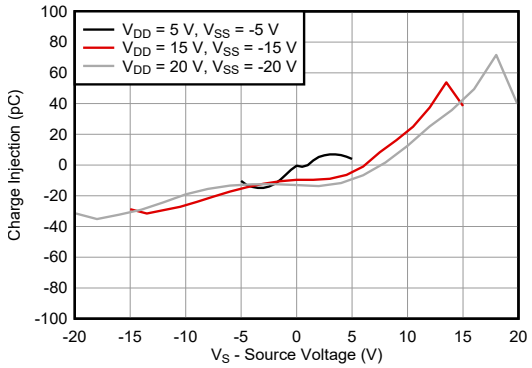


Figure 5-14. Charge Injection vs Source Voltage – Dual Supplies

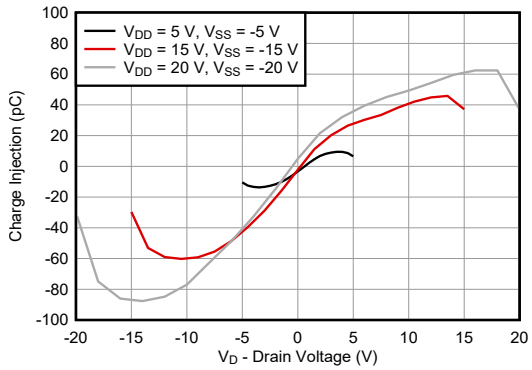


Figure 5-15. Charge Injection vs Drain Voltage – Dual Supplies

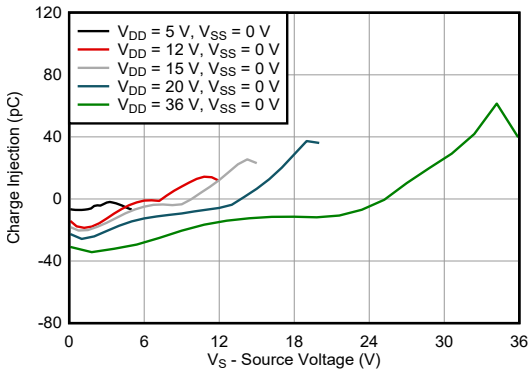
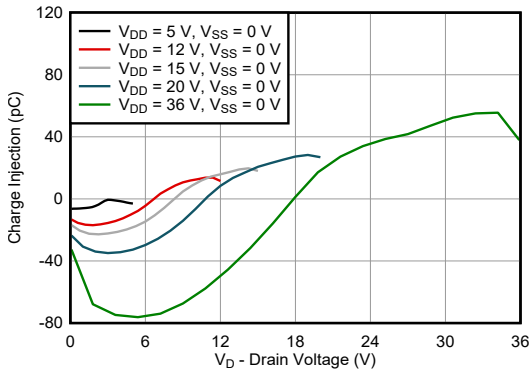
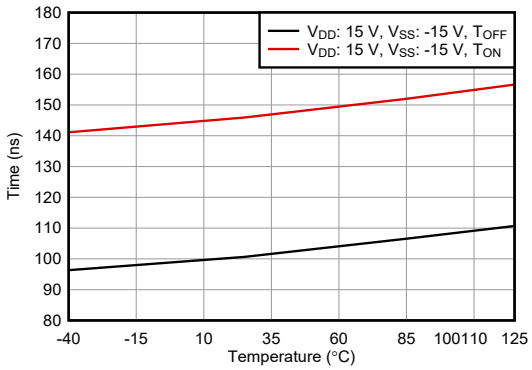


Figure 5-16. Charge Injection vs Source Voltage – Single Supplies



T_A = 25°C

Figure 5-17. Charge Injection vs Drain Voltage – Single Supplies

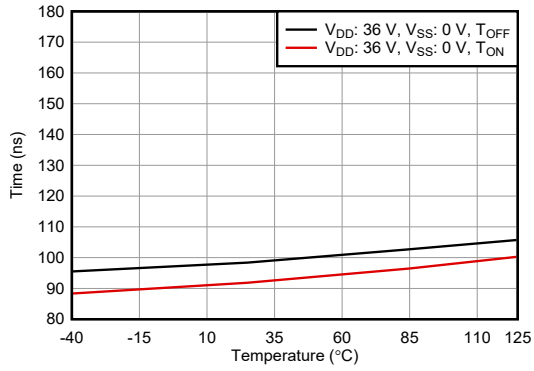


V_{DD} = 15 V, V_{SS} = -15 V

Figure 5-18. T_{ON} and T_{OFF} vs Temperature

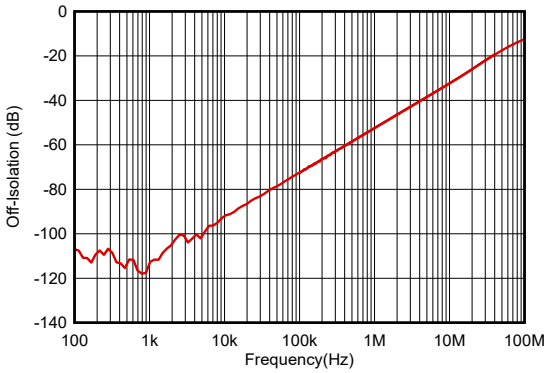
5.14 Typical Characteristics (continued)

at T_A = 25°C



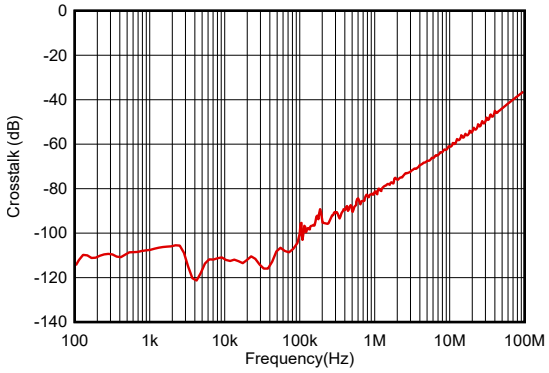
V_{DD} = 36 V, V_{SS} = 0 V

Figure 5-19. T_{ON} and T_{OFF} vs Temperature



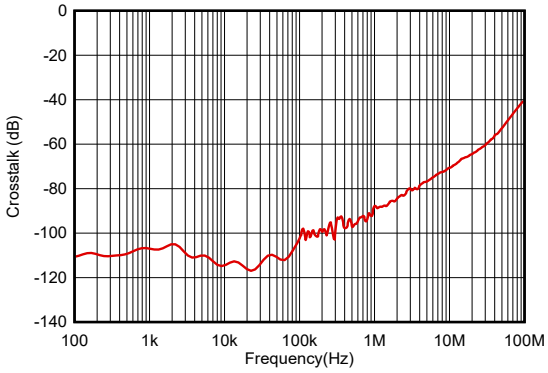
T_A = 25°C

Figure 5-20. Off-Isolation vs Frequency



Switch *ON* (EN = 1)

Figure 5-21. Crosstalk vs Frequency



Switch *OFF* (EN = 0)

Figure 5-22. Crosstalk vs Frequency

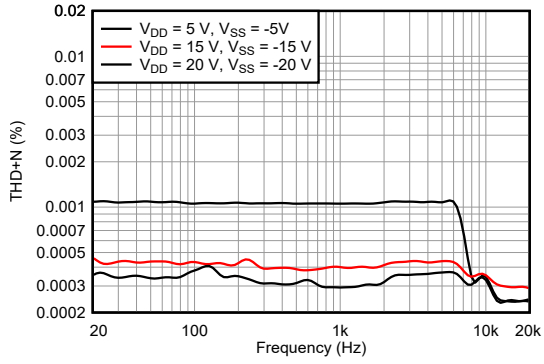


Figure 5-23. THD+N vs Frequency (Dual Supplies)

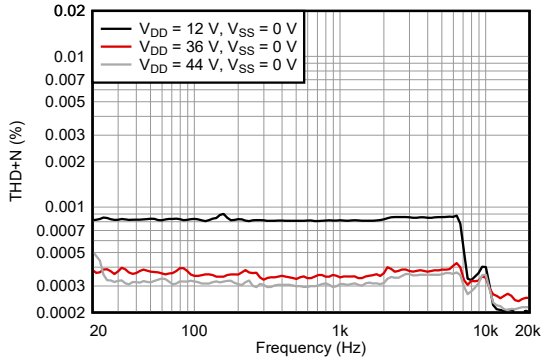
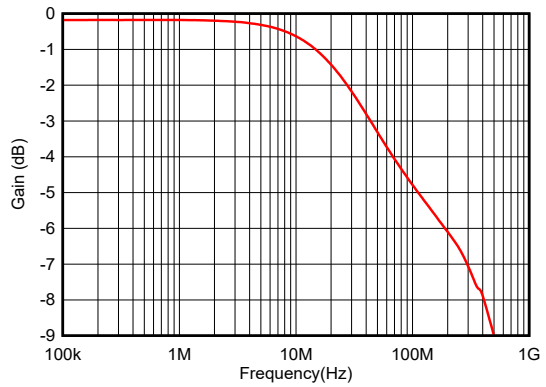


Figure 5-24. THD+N vs Frequency (Single Supplies)

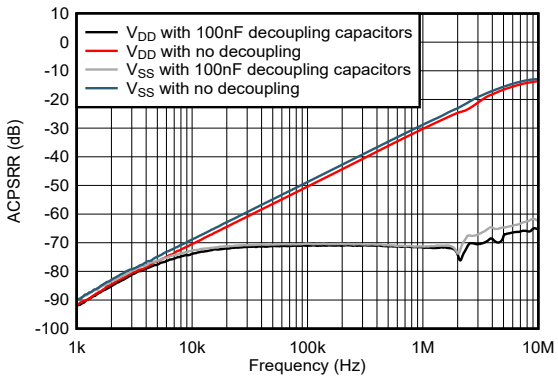
5.14 Typical Characteristics (continued)

at T_A = 25°C



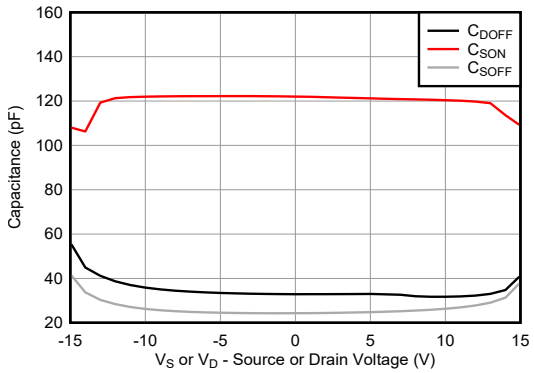
V_{DD} = 15 V, V_{SS} = -15 V

Figure 5-25. On Response vs Frequency



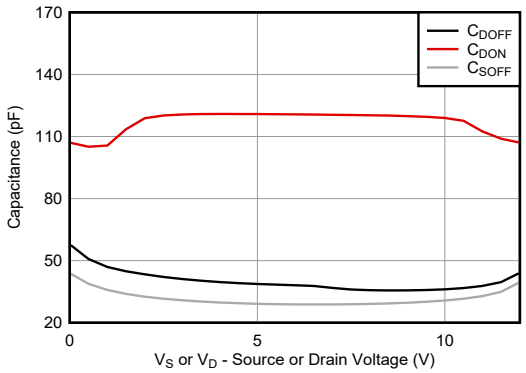
V_{DD} = +15 V, V_{SS} = -15 V

Figure 5-26. ACPSRR vs Frequency



V_{DD} = +15 V, V_{SS} = -15 V

Figure 5-27. Capacitance vs Source Voltage or Drain Voltage



V_{DD} = 12 V, V_{SS} = 0 V

Figure 5-28. Capacitance vs Source Voltage or Drain Voltage

6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 6-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using the following setup, where R_{ON} is computed as $R_{ON} = V / I_{SD}$:

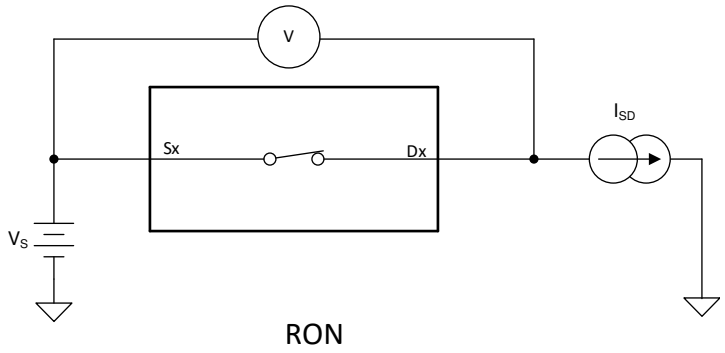


Figure 6-1. On-Resistance

6.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 6-2 shows the setup used to measure both off-leakage currents.

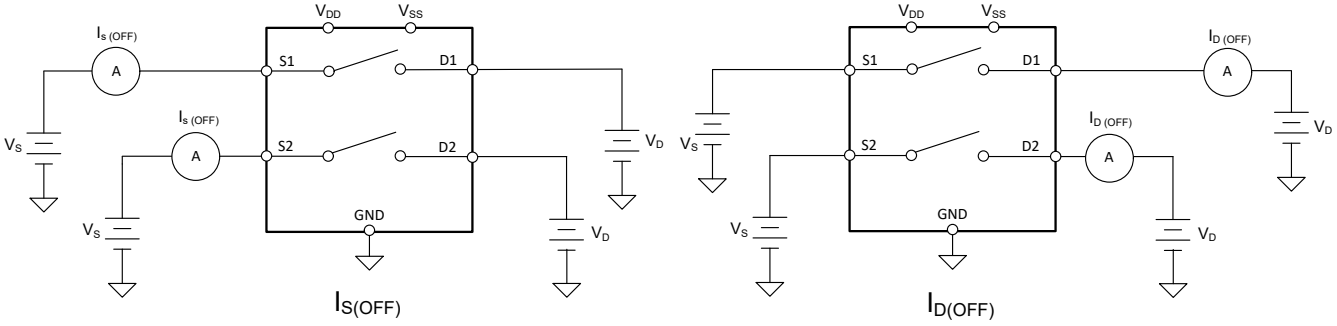


Figure 6-2. Off-Leakage Measurement Setup

6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

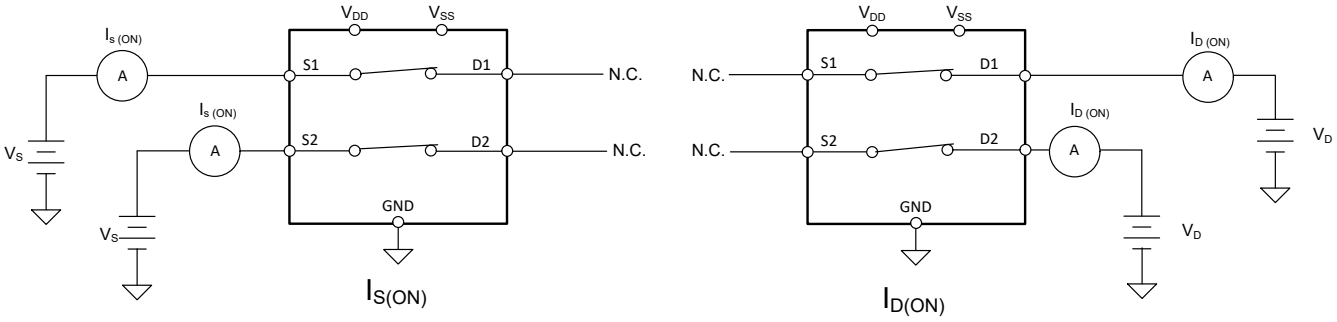


Figure 6-3. On-Leakage Measurement Setup

6.4 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

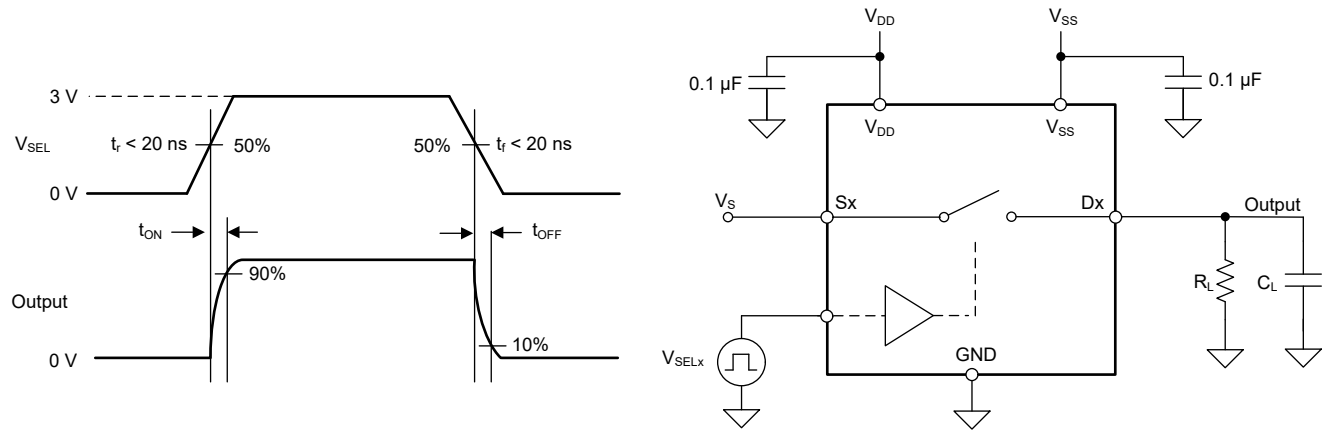


Figure 6-4. Turn-On and Turn-Off Time Measurement Setup

6.5 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 6-5 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

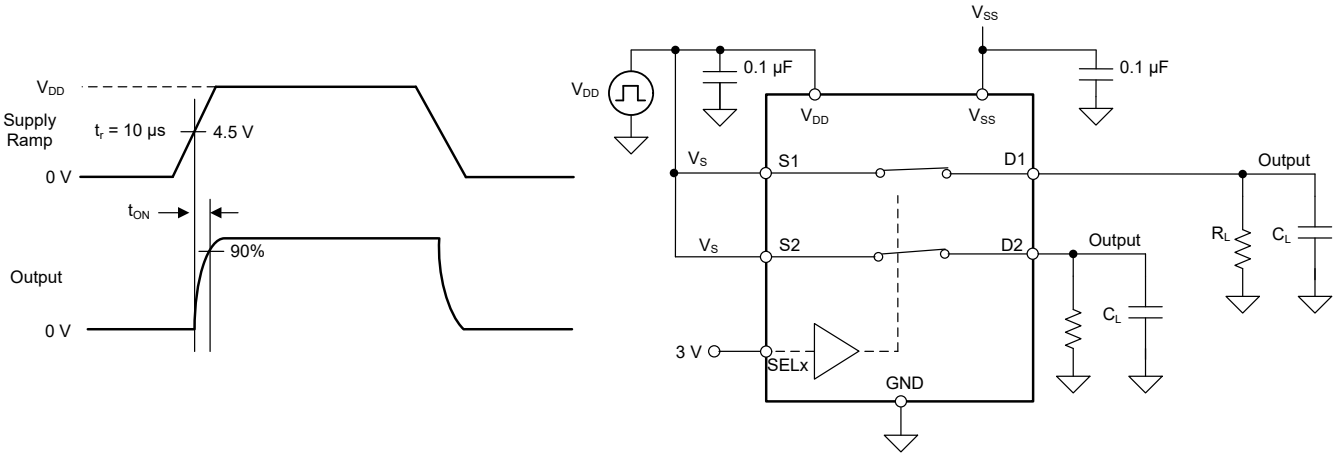


Figure 6-5. $t_{ON\ (VDD)}$ Time Measurement Setup

6.6 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 6-6 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

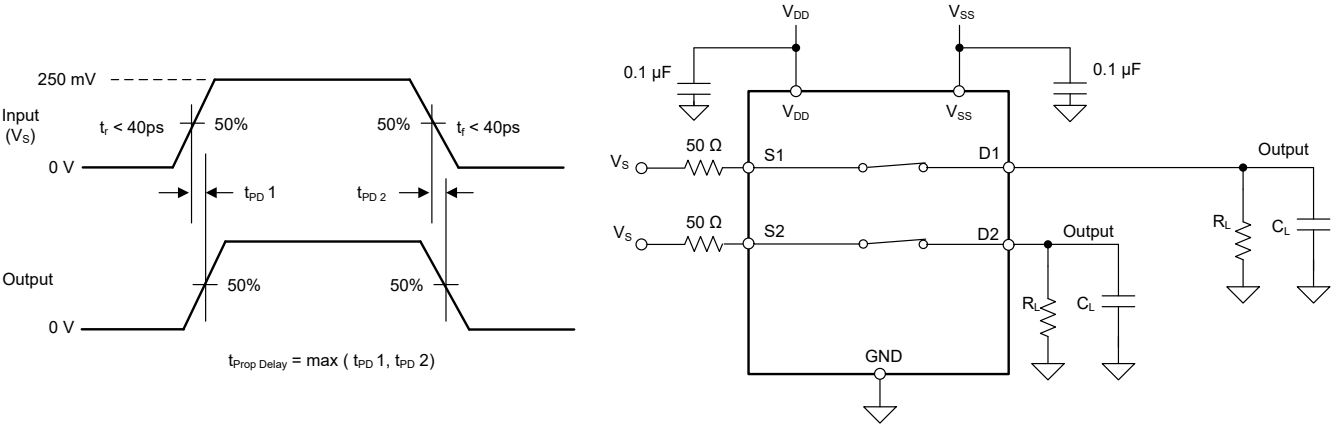


Figure 6-6. Propagation Delay Measurement Setup

6.7 Charge Injection

The TMUX722x has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 6-7 shows the setup used to measure charge injection from source (Sx) to drain (D).

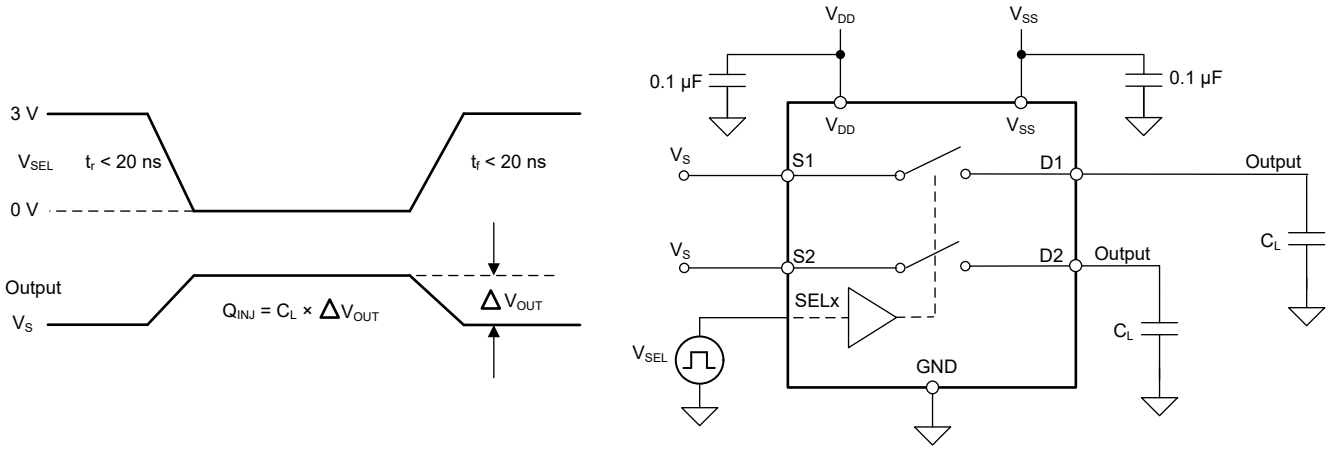
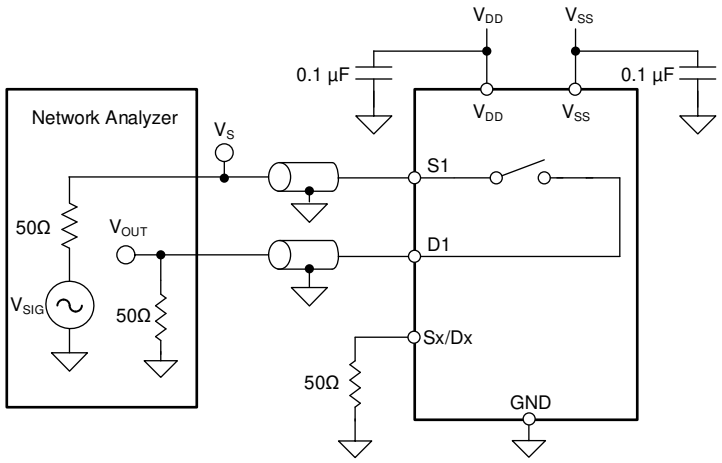


Figure 6-7. Charge-Injection Measurement Setup

6.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 6-8 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

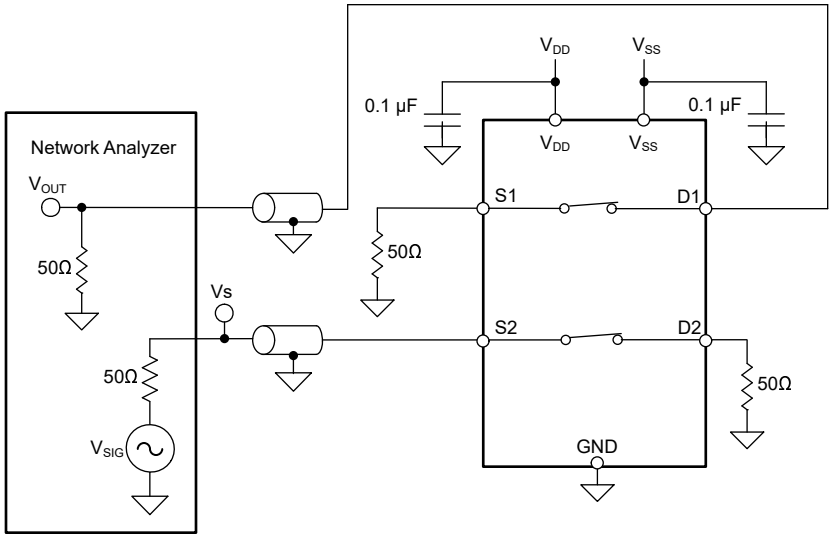


$$Off\ Isolation = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 6-8. Off Isolation Measurement Setup

6.9 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 6-9 shows the setup used to measure, and the equation used to calculate crosstalk.

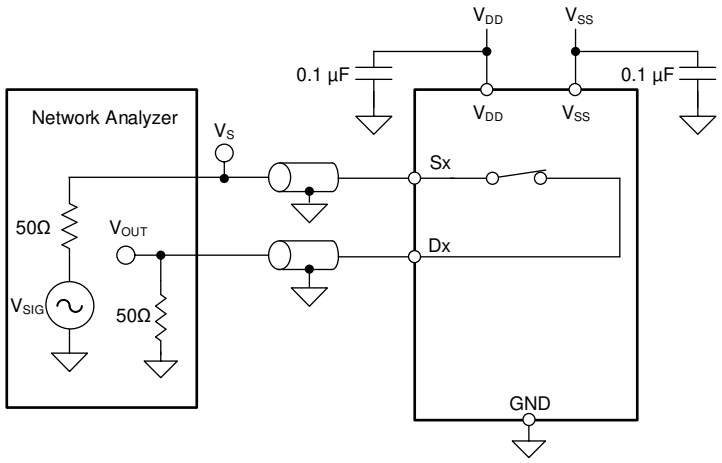


$$\text{Crosstalk} = 20 \times \text{Log}\ \frac{V_{OUT}}{V_S}$$

Figure 6-9. Crosstalk Measurement Setup

6.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 6-10 shows the setup used to measure bandwidth.



$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 6-10. Bandwidth Measurement Setup

6.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

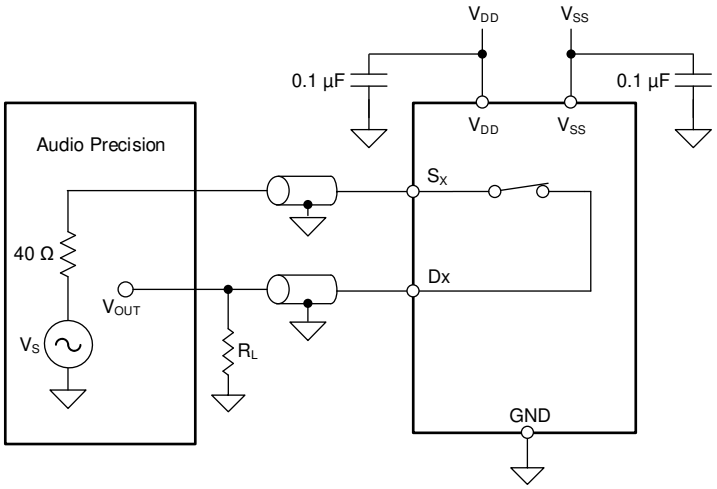
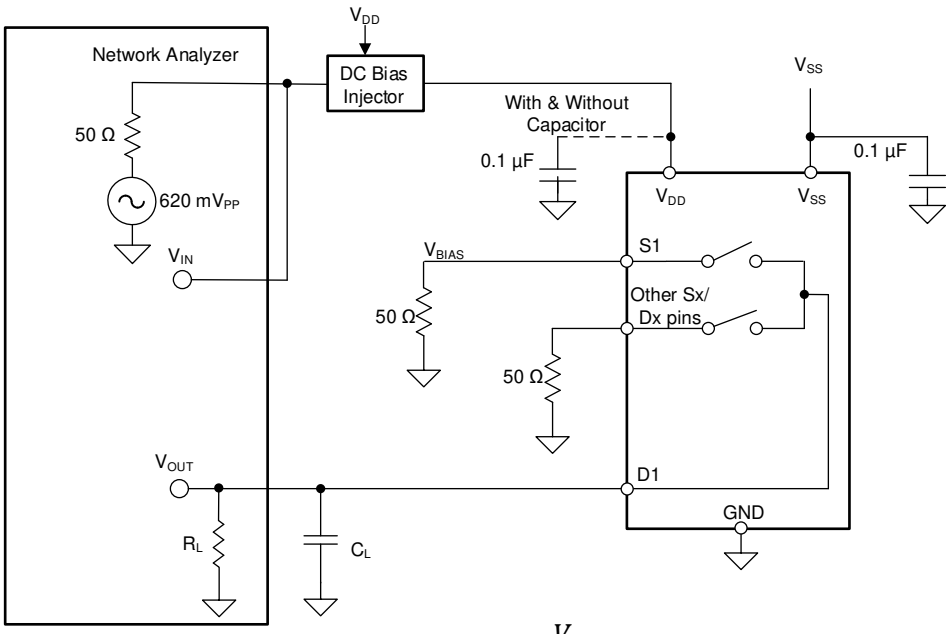


Figure 6-11. THD + N Measurement Setup

6.12 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 100 mV_{PP}. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.



$$PSRR = 20 \times Log \frac{V_{OUT}}{V_{IN}}$$

Figure 6-12. AC PSRR Measurement Setup

7 Detailed Description

7.1 Overview

The TMUX722x is a 1:1, 2-channel switch. Each input is turned on or turned off based on the state of the select line and enable pin.

7.2 Functional Block Diagram

Figure 7-1 shows the functional block diagram of the TMUX722x.

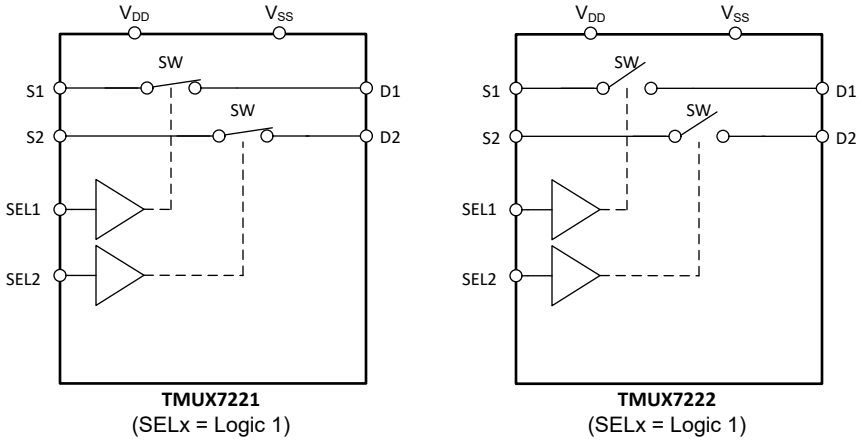


Figure 7-1. TMUX722x Functional Block Diagram

7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUX722x conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

7.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUX722x ranges from V_{SS} to V_{DD}.

7.3.3 1.8 V Logic Compatible Inputs

The TMUX722x has 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the device to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

7.3.4 Integrated Pull-Down Resistor on Logic Pins

The TMUX722x have internal weak pull-down resistors to GND so that the logic pins are not left floating. The value of this pull-down resistor is approximately 4 MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

7.3.5 Fail-Safe Logic

The TMUX722x supports Fail-Safe Logic on the control input pins (EN, SEL) allowing for operation up to 44 V above ground, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pins of the TMUX722x to be ramped to +44 V while V_{DD} and V_{SS} = 0 V. The logic control inputs are protected against positive faults of up to +44 V in powered-off condition, but do not offer protection against negative overvoltage conditions.

7.3.6 Latch-Up Immune

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX722x family of devices are constructed on Silicon on Insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX722x family of switches and multiplexers to be used in harsh environments.

7.3.7 Ultra-Low Charge Injection

The TMUX722x has a transmission gate topology, as shown in Figure 7-2. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

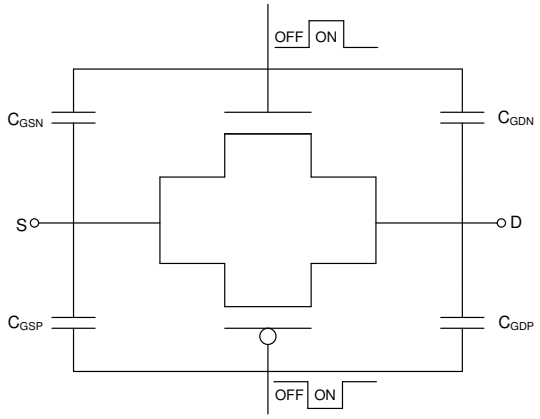


Figure 7-2. Transmission Gate Topology

The TMUX722x contains specialized architecture to reduce charge injection on the Drain (Dx). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the Source (Sx). Doing this will push excess charge from the switch transition into the compensation capacitor on the Source (Sx) instead of the Drain (Dx). As a general rule, Cp should be 20x larger than the equivalent load capacitance on the Drain (Dx). Figure 7-3 shows charge injection variation with different compensation capacitors on the Source side. This plot was captured on the TMUX7219 as part of the TMUX72xx family with a 100 pF load capacitance.

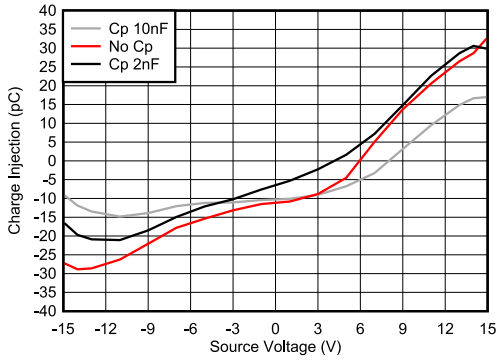


Figure 7-3. Charge Injection Compensation

7.4 Device Functional Modes

The TMUX722x devices have two independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. The control pins can be as high as 44 V.

The TMUX722x devices can be operated without any external components except for the supply decoupling capacitors. The SEL pins has internal pull-down resistor of 4 MΩ. If unused, tie the SEL pins to GND so that the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Connect unused signal path inputs (S1, S2, D1, or D2) to GND.

7.5 Truth Tables

Table 7-1 provides the truth tables for the TMUX722x.

Table 7-1. TMUX7221 Truth Table

SEL x	CHANNEL x
0	Channel x OFF
1	Channel x ON

Table 7-2. TMUX7222 Truth Table

SEL x	CHANNEL x
0	Channel x ON
1	Channel x OFF

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

TMUX722x is part of the precision switches and multiplexers family of devices. TMUX722x offers low RON, low on and off leakage currents and ultra-low charge injection performance. These properties make TMUX722x ideal for implementing high precision industrial systems requiring selection of one of two inputs or outputs.

8.2 Typical Applications

8.2.1 Switched Gain Amplifier - Discrete PGA

Switches and multiplexers are commonly used in the feedback path of amplifier circuits to provide configurable gain control. By using various resistor values on each switch path the TMUX722x allows the system to have multiple gain settings. An external resistor, ensures the amplifier isn't operating in an open loop configuration, and gives up to 4 gain settings. The leakage current, on-resistance, and charge injection performance of the TMUX722x are key specifications to evaluate when selecting a device for gain control.

Figure 8-1 shows the TMUX722x configured to select the gain of an op-amp, creating a discrete PGA.

For more information on how to use TI's analog switches in Discrete Programmable Gain Amplifier (PGA) such as the impact of On-Capacitance, see *Choosing the Right Multiplexer for a Discrete Programmable Gain Amplifier (PGA)*

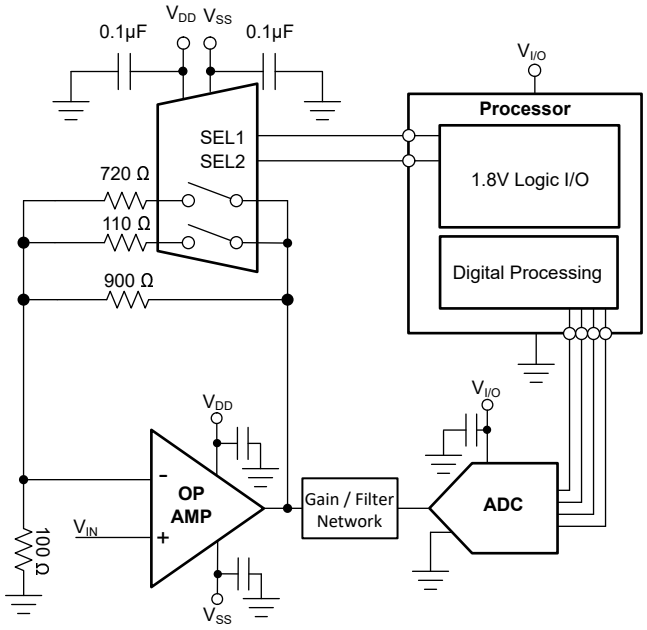


Figure 8-1. Gain Switching

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Section 8.2.1.1.

Table 8-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	15 V
Supply (V_{SS})	- 15 V
Input / Output signal range	-15 V to 15 V (Rail-to-Rail)
Control logic thresholds	1.8 V compatible

8.2.1.2 Detailed Design Procedure

The TMUX722x device can be operated without any external components except for the supply decoupling capacitors. All inputs signals passing through the switch must fall within the recommend operating conditions of the TMUX722x including signal range and continuous current. For this design example, with a supply of +15 V and -15 V, the signals can range from +15 V to -15 V when the device is powered.

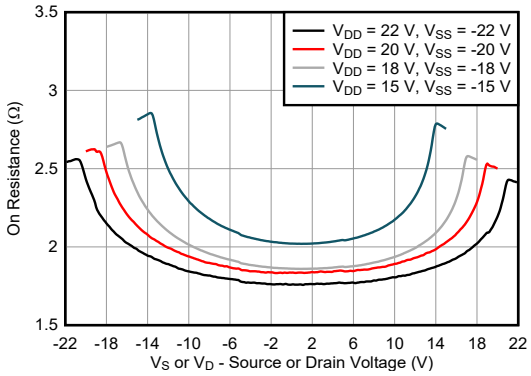
The application shown in *Switching Gain Settings* demonstrates how to use the TMUX722x to control the feedback gain of a precision op-amp. This feedback design can very sensitive to induced voltage and current offsets. The TMUX722x has a typical On-leakage current of 100 pA which would lead to an accuracy well within 1% of a full scale 1 µA signal, thus minimizing errors from current offsets. The low On-Resistance of the TMUX722x leads to a low error in the feedback resistance and resulting gain, and also minimizes any voltage offsets.

Table 8-2. Programmable Gain and Error

SEL1	SEL2	Gain	Gain Error
0	0	10x	0%
1	0	5x	0.13%
0	1	2x	0.16%

8.2.1.3 Application Curve

The TMUX722x is capable of switching signals with minimal distortion because of the ultra-low leakage currents and excellent on-resistance flatness. Figure 8-2 shows how the on-resistance for the TMUX722x varies with different supply voltages.



T_A = 25°C

Figure 8-2. On-Resistance vs Source or Drain Voltage

8.3 Power Supply Recommendations

The TMUX722x operates across a wide supply range of ±4.5 V to ±22 V (4.5 V to 44 V in single-supply mode). The device also performs well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS} = –5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always ensure the ground (GND) connection is established before supplies are ramped.

8.4 Layout

8.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

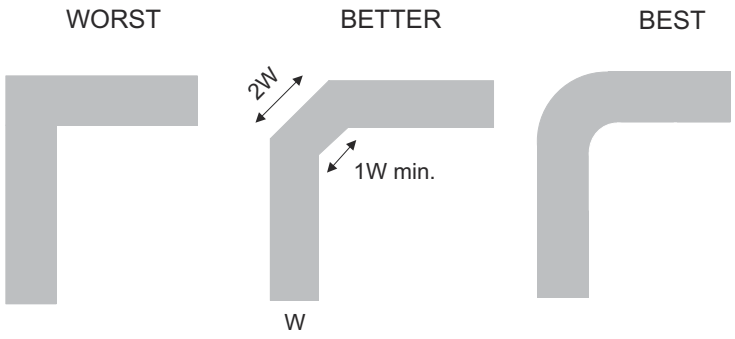


Figure 8-3. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Some key considerations are:

- For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD/VSS and GND. We recommend a 0.1 µF and 1 µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

8.4.2 Layout Example

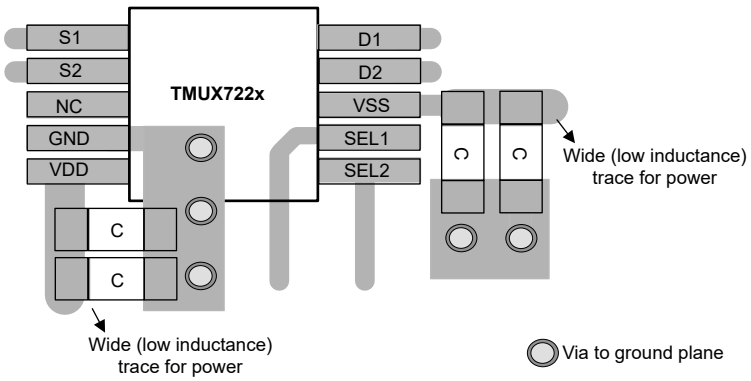


Figure 8-4. TMUX722x Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*.
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment*.
- Texas Instruments, *Multiplexers and Signal Switches Glossary*.
- Texas Instruments, *QFN/SON PCB Attachment*.
- Texas Instruments, *Quad Flat pack No-Lead Logic Packages*.
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches*.
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers*.
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit*.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2023) to Revision B (May 2024)	Page
• Updated the *Pin Configuration* section to accurately reflect the correct pin number for SEL1 and SEL2	3

Changes from Revision * (February 2023) to Revision A (April 2023)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX7221DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TM221	Samples
TMUX7222DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TM222	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

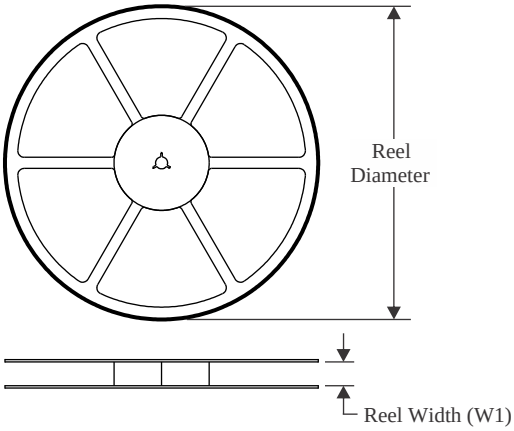
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

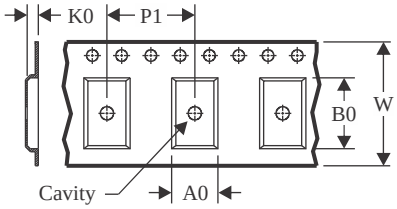
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

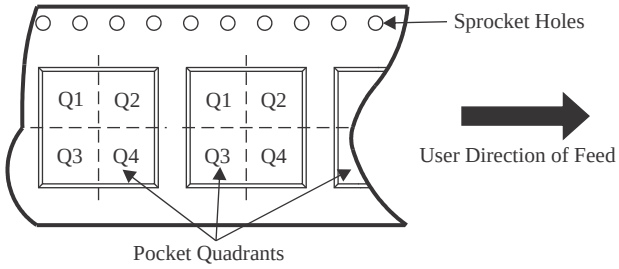


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

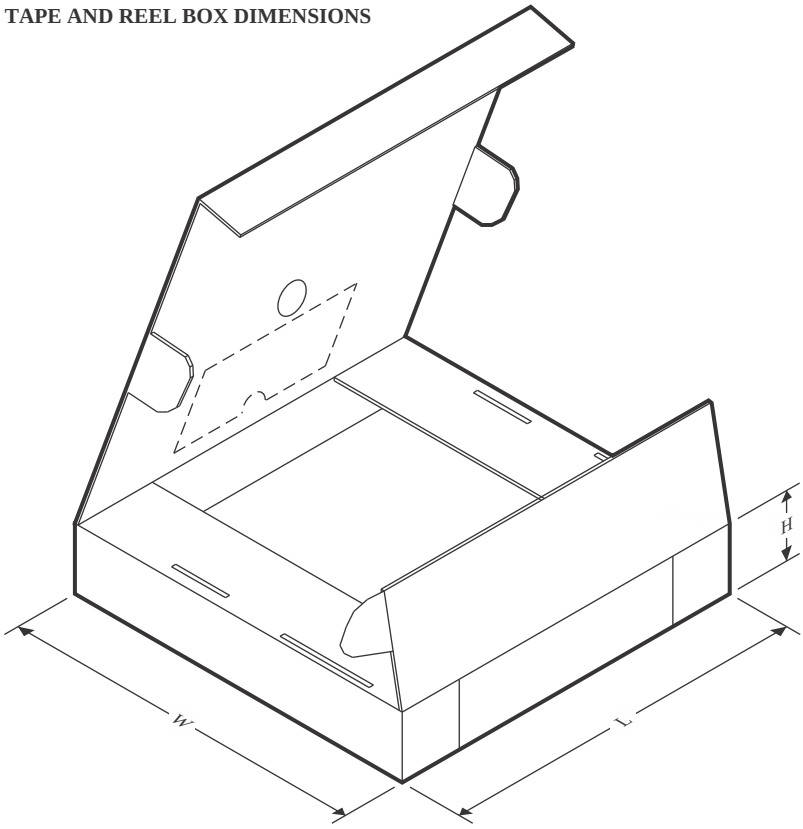
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX7221DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TMUX7222DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

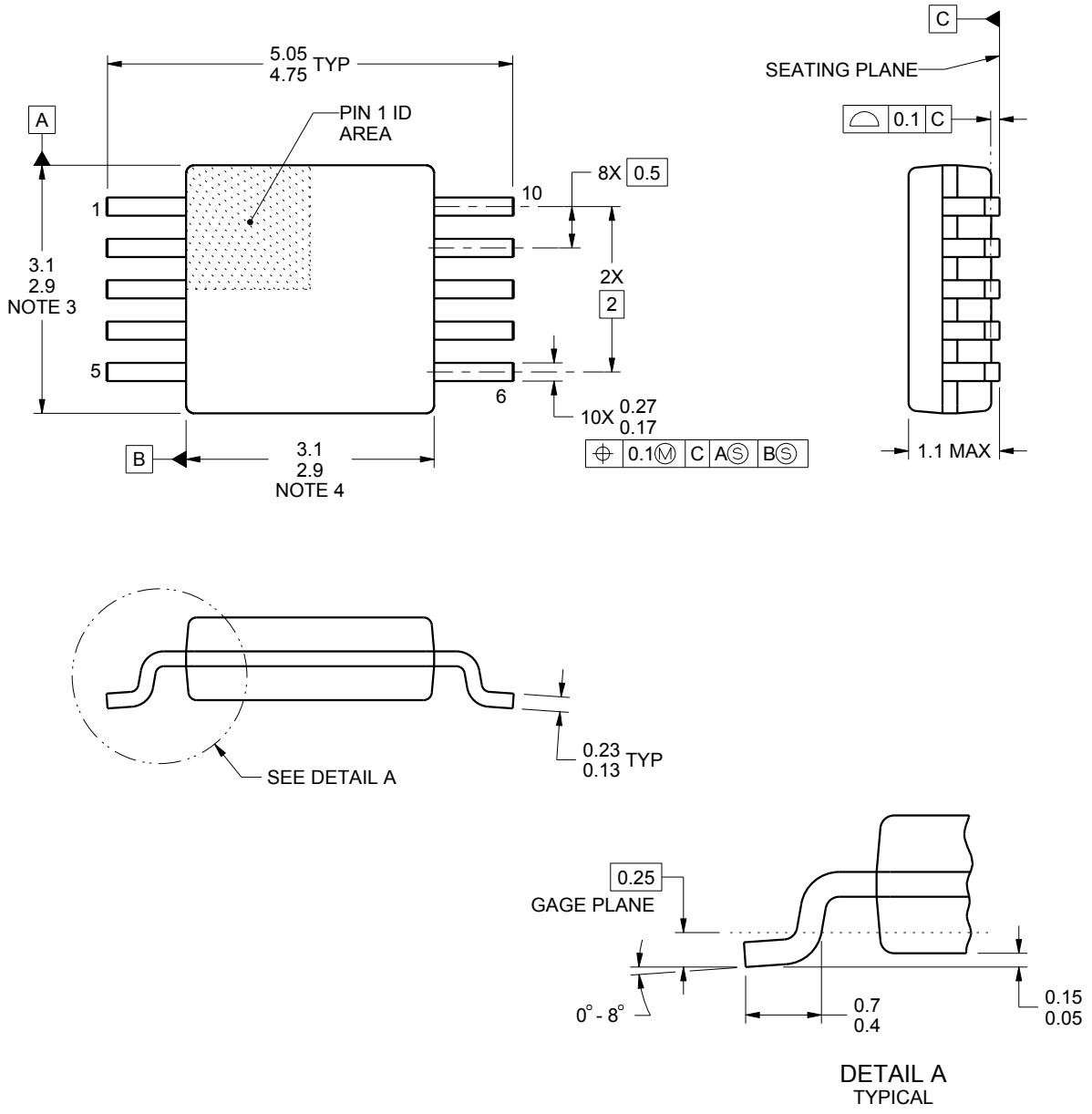
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX7221DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TMUX7222DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0

PACKAGE OUTLINE

DGS0010A

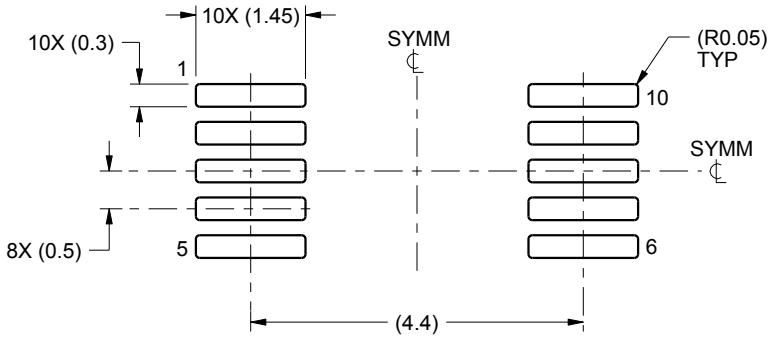
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

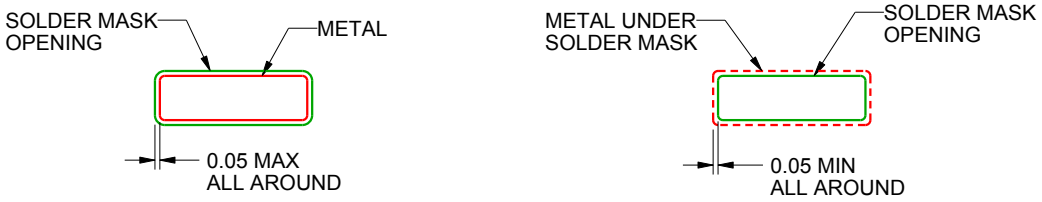


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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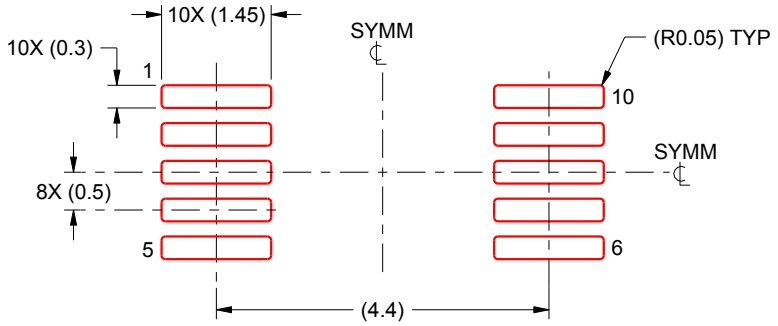
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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