TMUXHS4612 6-Channel 20Gbps Differential 2:1 Mux / 1:2 Demux

1 Features

- Supports HDMI 1.4b/2.0/2.1 up to 12Gbps, DisplayPort 1.4/2.1 up to UHBR20
- Data rate support up to 20Gbps
- High-speed path supports wide common-mode voltage range (0V to V_{CC})
- Low RON of 8.0Ω typical for high-speed data pins
- –3dB differential BW of 15GHz for high-speed data pins
- Excellent dynamic characteristics at 10GHz:
  - Insertion loss: –2.4dB
  - Return loss: –14dB
  - Cross talk: –35dB
- All sideband signals can pass-thru up to 5V levels and are 5.5V tolerant
- Support 1.8V and 3.3V control logic
- Single supply voltage of 3.3V
- Low active (750µA) and standby power (30µA)
- I_{OFF} protection that prevents current leakage when supply rail collapsed (V_{CC} = 0V)
- Temperature range: –40°C to 125°C
- 40-pin, 3mm × 6mm, 0.4mm pitch WQFN package

2 Applications

- PC and notebooks
- Gaming, Home theater & entertainment and TV
- Data center and enterprise computing
- Medical applications
- Test and measurements
- Factory automation and control
- Aerospace and defense
- Electronic point of sale (EPOS)
- Wireless infrastructure

3 Description

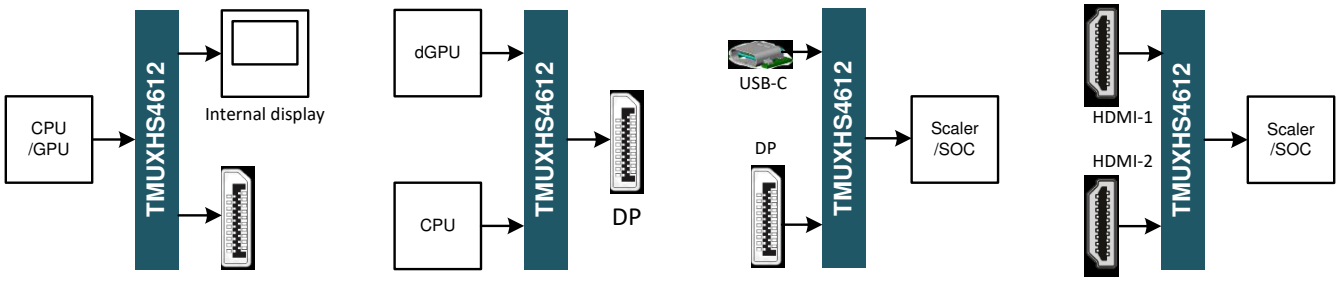
The TMUXHS4612 is a high-speed bidirectional passive switch in mux or demux configurations. The device is protocol agnostic supporting many applications including HDMI 1.4 / 2.0 / 2.1 and DisplayPort 1.4 / 2.1. The TMUXHS4612 is a generic analog differential passive mux or demux that works for many high-speed differential interfaces with data rates up to 20Gbps. The TMUXHS4612 high-speed channels support differential signaling and single-ended signaling as long as the single-ended signals do not violate V_{P-N_ABSMAX} parameter. The sideband channels are 5V tolerant and support single-ended and differential signaling such as I^2C, UART, DisplayPort AUX, and USB2, just to name few. The high-speed channel's dynamic characteristics allows high speed switching with minimal attenuation to the signal eye diagram and with very little added jitter. The silicon design of the device is optimized for excellent frequency response at higher frequency spectrum of the signals. The device supports differential signaling with common-mode voltage range (CMV) of 0V to 3.6V in the Dxx datapaths.

The TMUXHS4612 consumes very low active power of 750µA. The device also offers a power-down mode in which all channels become Hi-Z and the device operates with minimal power of just 30µA.

Package Information (1)

PART NUMBER	TEMPERATURE	PACKAGE	PACKAGE SIZE(2)
TMUXHS4612	T_A = 0°C to 105°C	RET (WQFN, 40)	6mm × 3mm
TMUXHS4612I	T_A = –40°C to 125°C		

(1) For all available packages, see Section 11.
(2) The package size (length x width) is a nominal value and includes pins, where applicable.



Internal vs external display | Switchable Graphics in PC | Choosing video in dock/monitor | Choosing HDMI Port in TV/STB

Simplified Use Cases

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4 Pin Configuration and Functions

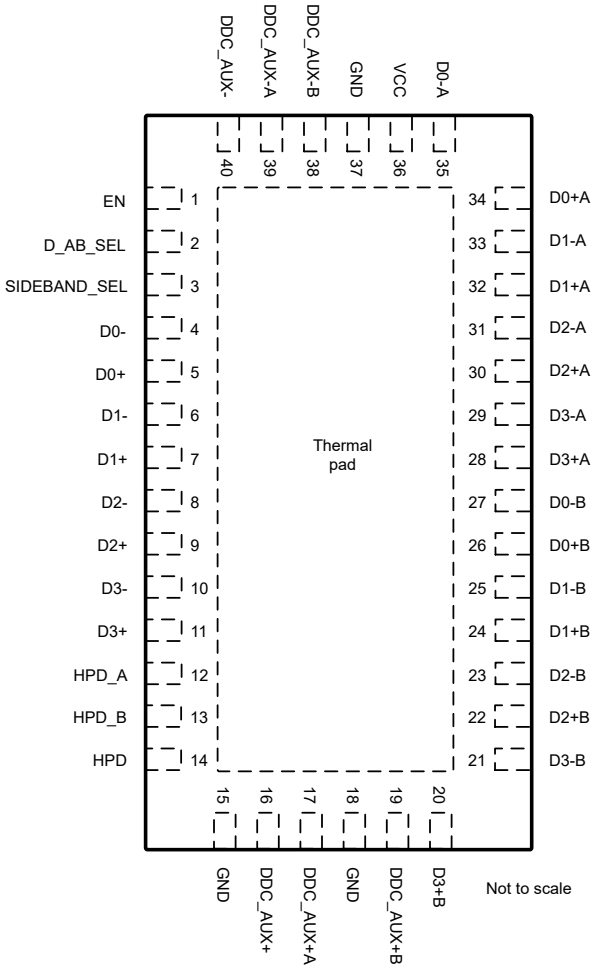

Figure 4-1. RET Package 40-Pin WQFN With Exposed Thermal Pad (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	1	I	Device Enable L: Device Disabled. All data and sideband signals in Hi-Z. H: Device Enabled. All data and sideband signals selected by D_AB_SEL and SIDEBAND_SEL are enabled.
D_AB_SEL	2	I	Selects between high-speed datapath A and B. L: High-speed datapath A H: High-speed datapath B
SIDEBAND_SEL	3	I	Selects between sideband path A and B L: Sideband path A H: Sideband path B
D0–	4	I/O	Common Port, Channel 0, –ve signal
D0+	5	I/O	Common Port, Channel 0, +ve signal
D1–	6	I/O	Common Port, Channel 1, –ve signal
D1+	7	I/O	Common Port, Channel 1, +ve signal
D2–	8	I/O	Common Port, Channel 2, –ve signal

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Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
D2+	9	I/O	Common Port, Channel 2, +ve signal
D3–	10	I/O	Common Port, Channel 3,–ve signal
D3+	11	I/O	Common Port, Channel 3, +ve signal
HPD_A	12	I/O	Port A, Hot Plug Detect sideband signal
HPD_B	13	I/O	Port B, Hot Plug Detect sideband signal
HPD	14	I/O	Common Port, Hot Plug Detect sideband signal
GND	15	GND	Ground
DDC_AUX+	16	I/O	Common Port, DDC or AUX sideband signal
DDC_AUX+A	17	I/O	Port A, DDC or AUX sideband signal
GND	18	GND	Ground
DDC_AUX+B	19	I/O	Port B, DDC or AUX sideband signal
D3+B	20	I/O	Port B, Channel 3, +ve signal
D3–B	21	I/O	Port B, Channel 3, –ve signal
D2+B	22	I/O	Port B, Channel 2, +ve signal
D2–B	23	I/O	Port B, Channel 2,–ve signal
D1+B	24	I/O	Port B, Channel 1, +ve signal
D1–B	25	I/O	Port B, Channel 1, –ve signal
D0+B	26	I/O	Port B, Channel 0, +ve signal
D0–B	27	I/O	Port B, Channel 0, –ve signal
D3+A	28	I/O	Port A, Channel 3, +ve signal
D3–A	29	I/O	Port A, Channel 3, –ve signal
D2+A	30	I/O	Port A, Channel 2, +ve signal
D2–A	31	I/O	Port A, Channel 2,–ve signal
D1+A	32	I/O	Port A, Channel 1, +ve signal
D1-A	33	I/O	Port A, Channel 1, –ve signal
D0+A	34	I/O	Port A, Channel 0, +ve signal
D0–A	35	I/O	Port A, Channel 0, –ve signal
VCC	36	Power	Supply Voltage
GND	37	GND	Ground
DDC_AUX-B	38	I/O	Port B, DDC or AUX sideband signal
DDC_AUX-A	39	I/O	Port A, DDC or AUX sideband signal
DDC_AUX-	40	I/O	Common Port, DDC or AUX sideband signal
GND	PowerPad	GND	Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VCC_{ABSMAX}	Supply voltage range		–0.5	4.0	V
$V_{I/O-ABSMAX}$	Analog voltage range(2) (3) (4)	All high-speed data I/O pins	–0.5	4.0	V
$V_{I/O-ABSMAX}$	Analog voltage range(2) (3) (4)	All sideband(5) pins	–0.5	6.0	V
$V_{IN-ABSMAX}$	Digital input voltage range(2) (3)	All control pins(6)	–0.5	5.0	V
V_{P-N_ABSMAX}	Absolute value of positive pin minus negative pin	All high-speed data I/O pins		0.8	V
T_{jmax}	Maximum junction temperature TMUXHS4612		0	105	°C
T_{jmax}	Maximum junction temperature TMUXHS4612I		–40	125	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) Sideband pins: DDC_AUX+A, DDC_AUX-A, HPD_A, DDC_AUX+B, DDC_AUX-B, HPD_B, DDC_AUX+, DDC_AUX-, HPD
(6) Control pins: D_AB_SEL, SIDEBAND_SEL, EN

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, (1)	±1500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, (2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	3.0	3.3	3.6	V
$V_{I/O,CM}$	Input/Output common mode voltage (data pins)	0		3.6	V
$V_{I/O}$	Input/Output voltage data pins	0		3.6	V
$V_{I/O}$	Input/Output voltage sideband(2) pins	0		5	V
V_{IN}	Digital input voltage (control(3) pins)	0		VCC	V
DR	Data rate for differential signals			20	Gbps
T_A	Operating ambient temperature TMUXHS4612	0		105	°C
T_A	Operating ambient temperature TMUXHS4612I	–40		125	°C
T_J	Operating junction temperature TMUXHS4612	0		110	°C
T_J	Operating junction temperature TMUXHS4612I	–40		125	°C

(1) All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the *TI application report, Implications of Slow or Floating CMOS Inputs,* literature number SCBA004.
(2) Sideband pins: DDC_AUX+A, DDC_AUX-A, HPD_A, DDC_AUX+B, DDC_AUX-B, HPD_B, DDC_AUX+, DDC_AUX-, HPD
(3) Control pins: D_AB_SEL, SIDEBAND_SEL, EN

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5.4 Thermal Information

THERMAL METRIC(1)		TMUXHS4612 RET 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER (3) (4)			TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
DC Characteristics (data and sideband)							
R_{ON-D}	ON-state resistance	All data pins;	$V_{I/O}$ = 0V to VCC; $I_{I/O}$ = –10mA; VCC = 3.3V ±10%; 0 to 85°C;		8.0	10	Ω
			$V_{I/O}$ = 0V to VCC; $I_{I/O}$ = –10mA; VCC = 3.3V ±10%; –40 to 125°C;		8.0	12	Ω
R_{ON-SB}	ON-state resistance	All sideband pins;	$V_{I/O}$ = 0V to VCC; $I_{I/O}$ = –10mA; VCC = 3.3V ±10%; 0 to 85°C;		8.5	15	Ω
			$V_{I/O}$ = 0V to VCC; $I_{I/O}$ = –10mA; VCC = 3.3V ±10%; –40 to 125°C;		8.5	15	Ω
$R_{ON-SB-5V}$	ON-state resistance	All sideband pins;	$V_{I/O}$ = 5V; $I_{I/O}$ = –10 mA; VCC = 3.3V ±10%; –40 to 125°C;		70	140	Ω
$C_{ON-SB-100K}$	Sideband ON capacitance to GND		f = 100kHz;			10	pF
$C_{OFF-SB-100K}$	Sideband Off capacitance to GND		f = 100kHz;			5	pF
$C_{ON-SB-1M}$	Sideband ON capacitance to GND		f = 1MHz;			9	pF
$C_{OFF-SB-1M}$	Sideband Off capacitance to GND		f = 1MHz;			4.5	pF
I_{IH-D}	Input current for high-speed data pair	All selected data pins.	EN = H; $V_{I/O}$ = 3.3V; VCC = 3.3V ±10%;			5	µA
		All non-selected data pins.	EN = H; $V_{I/O}$ = 3.3V; VCC = 3.3V ±10%;			130	µA
I_{IH-SB}	Input current for sideband	All selected sideband pins.	EN = H; $V_{I/O}$ = 3.3V; VCC = 3.3V ±10%;			5	µA
		All non-selected sideband pins.	EN = H; $V_{I/O}$ = 3.3V; VCC = 3.3V ±10%;			1	µA
$I_{OFF-DAB}$	Leakage under power off (failsafe current)	All data pins	VCC = 0V; $V_{I/O}$ = 0V to 3.3V;	–1		30	µA
I_{OFF-SB}	Leakage under power off (failsafe current)	All sideband pins	VCC = 0V; $V_{I/O}$ = 0V to 5.5V;	–1		20	µA
Control Inputs (SIDEBAND_SEL, D_AB_SEL, EN)							
$V_{IH-CTRL}$	High-level input voltage for control pins	Per pin for all control pins.	VCC = 3.3V ±10%;	1.4			V
$V_{IL-CTRL}$	Low-level input voltage for control pins	Per pin for all control pins.	VCC = 3.3V ±10%;			0.5	V
$I_{IH-CTRL}$	Input high leakage current for control pins	Per pin for all control pins.	VCC = 3.6V; V_{IN} = 3.6V;	–2		2	µA
$I_{IL-CTRL}$	Input low leakage current for control pins	Per pin for all control pins.	VCC = 3.6V; V_{IN} = 0V;	–1		1	µA
$I_{OFF-CTRL}$	Leakage under power off (failsafe current)	Per pin for all control pins.	VCC = 0V; VIN = 0V or 3.6V;	–10		10	µA
$C_{IN-CTRL}$	Input capacitance	Per pin for all control pins.	f = 1MHz;			12	pF
Power Supply							

over operating free-air temperature range (unless otherwise noted)

PARAMETER (3) (4)		TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
I_{CC}	VCC supply current in active mode	EN = H; $V_{I/O}$ = 0V or VCC;			750	µA
I_{CC-PD}	VCC supply current in power-down mode	EN = L; $V_{I/O}$ = 0V or VCC;			30	µA

(1) V_I, V_O, I_I, and I_O refer to data and sideband I/O pins.V_{IN} refers to the control inputs.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) Sideband pins: DDC_AUX+A, DDC_AUX-A, HPD_A, DDC_AUX+B, DDC_AUX-B, HPD_B, DDC_AUX+, DDC_AUX-, HPD
(4) Control pins: D_AB_SEL, SIDEBAND_SEL, EN

5.6 High-Speed Performance Parameters

Over recommended operation free-air temperature range, (unless otherwise noted). For all data pins. R_L = 50 Ω where applicable.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
BW_{SB}	Sideband pins differential bandwidth (–3dB from DC)			2.0		GHz
BW_{HS}	High-speed pins differential bandwidth (–3dB from DC)			15		GHz
IL_{DAB}	Differential insertion loss	At 10MHz; VCM = 0V;		–0.6		dB
		At 1.7GHz; VCM = 0V;		–0.9		dB
		At 2.7GHz; VCM = 0V;		–1.1		dB
		At 4.0GHz; VCM = 0V;		–1.3		dB
		At 6.0GHz; VCM = 0V;		–1.7		dB
		At 10.0 GHz; VCM = 0V;		–2.4		dB
RL_{DAB}	Differential return loss	At 10MHz; VCM = 0V;		–24		dB
		At 1.7GHz; VCM = 0V;		–20		dB
		At 2.7GHz; VCM = 0V;		–17		dB
		At 4.0GHz; VCM = 0V;		–15		dB
		At 6.0GHz; VCM = 0V;		–14		dB
		At 10.0GHz; VCM = 0V;		–14		dB
Xtalk	Differential crosstalk	At 10MHz; VCM = 0V;		–80		dB
		At 1.7GHz; VCM = 0V;		–38		dB
		At 2.7GHz; VCM = 0V;		–35		dB
		At 4.0GHz; VCM = 0V;		–35		dB
		At 6.0GHz; VCM = 0V;		–35		dB
		At 10.0GHz; VCM = 0V;		–35		dB
OISO	Differential off isolation	At 10MHz; VCM = 0V;		–80		dB
		At 1.7GHz; VCM = 0V;		–35		dB
		At 2.7GHz; VCM = 0V;		–32		dB
		At 4.0GHz; VCM = 0V;		–28		dB
		At 6.0GHz; VCM = 0V;		–25		dB
		At 10.0GHz; VCM = 0V;		–22		dB

(1) All Typical Values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.

5.7 Switching Characteristics

PARAMETER			MIN	TYP	MAX	UNIT
Device Switching Time						
$t_{SW\_POWER\_ON}$	Device power ON time	EN pin from L to H;			200	µs
$t_{SW\_POWER\_OFF}$	Device power OFF time	EN pin from H to L;			400	ns
High Speed Pins						
t_{PD}	Switch differential propagation delay	f = 1GHz		40		ps
t_{SW_AB}	Switching time from A to B	Measured from 50% of select to 50% of VOH/VOL			40	µs

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PARAMETER			MIN	TYP	MAX	UNIT
t_{SW_BA}	Switching time from B to A	Measured from 50% of select to 50% of VOH/VOL			40	µs
t_{SK_INTRA}	Intra-pair output skew between + and - pins for same channel	f = 1GHz		1.3	3	ps
t_{SK_INTER}	Inter-pair output skew between channels	f = 1GHz			6	ps
Sideband Pins						
$t_{PD\text{-}SB}$	Switch single-ended propagation delay	f = 1MHz			250	ps
$t_{SW\text{-}SB\_AB}$	Switching time from A to B	Measured from 50% of select to 50% of VOH/VOL			20	µs
$t_{SW\text{-}SB\_BA}$	Switching time from B to A	Measured from 50% of select to 50% of VOH/VOL			20	µs
$t_{SK\text{-}SB}$	Output skew between DDC_AUX+ and DDC_AUX- pins	f = 1MHz			8	ps

ADVANCE INFORMATION

5.8 Typical Characteristics

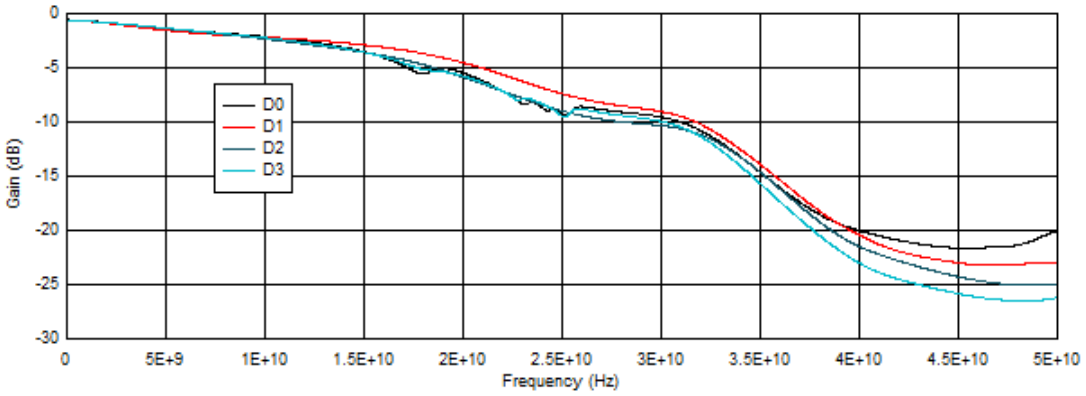

Figure 5-1. Differential Insertion Loss vs Frequency for Port A

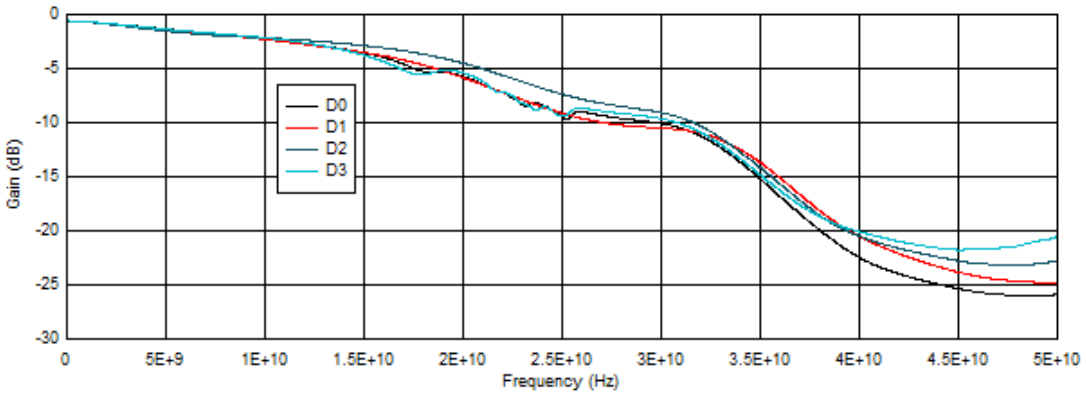

Figure 5-2. Differential Insertion Loss vs Frequency for Port B

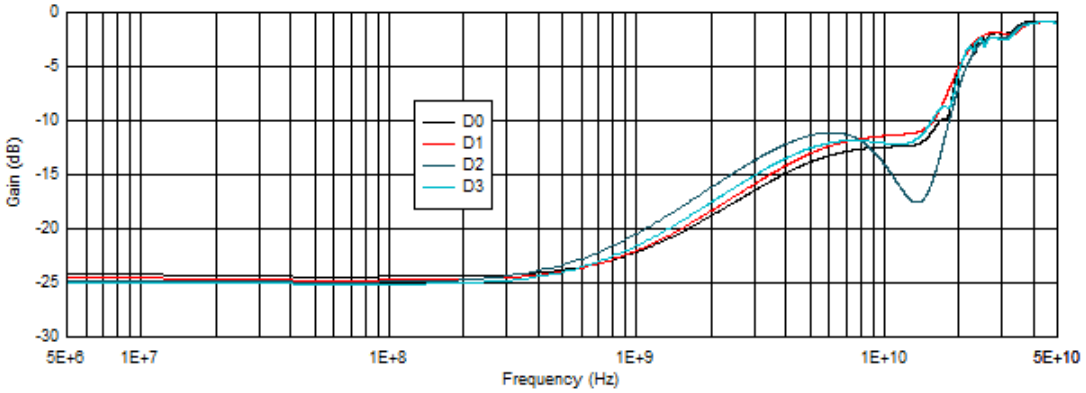

Figure 5-3. Input Differential Return Loss Characteristics when Port A is selected

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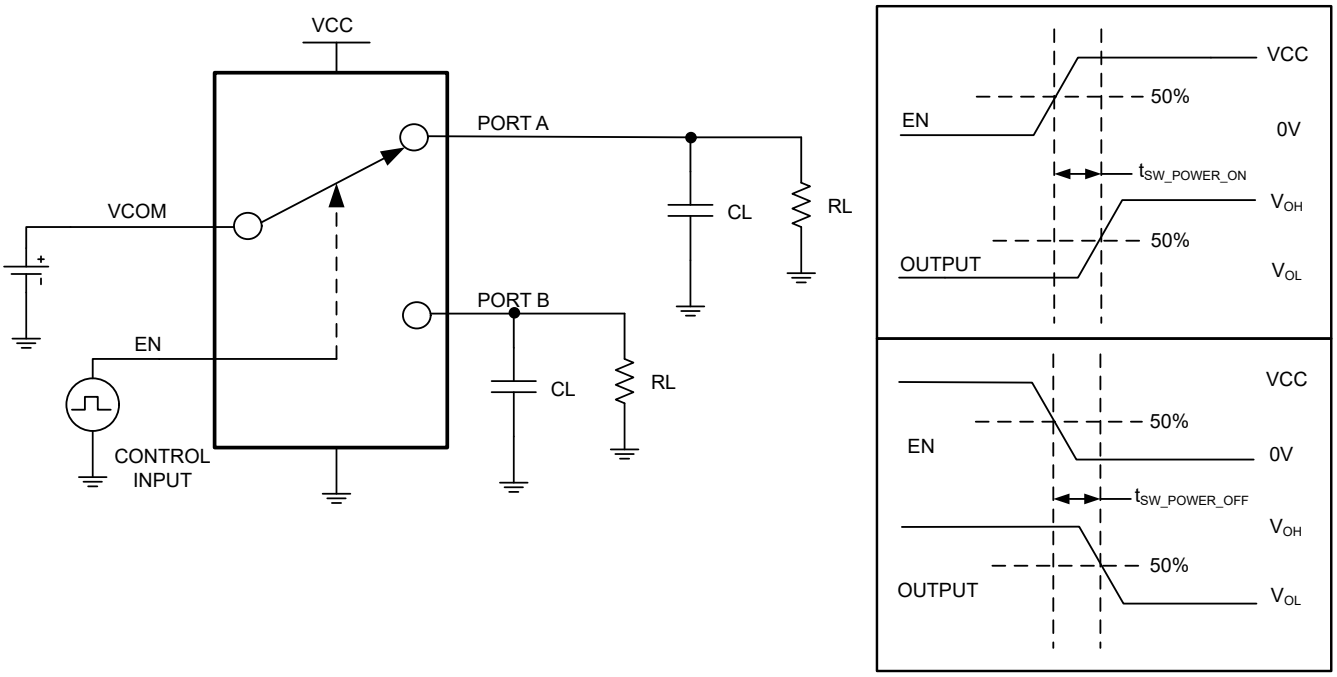
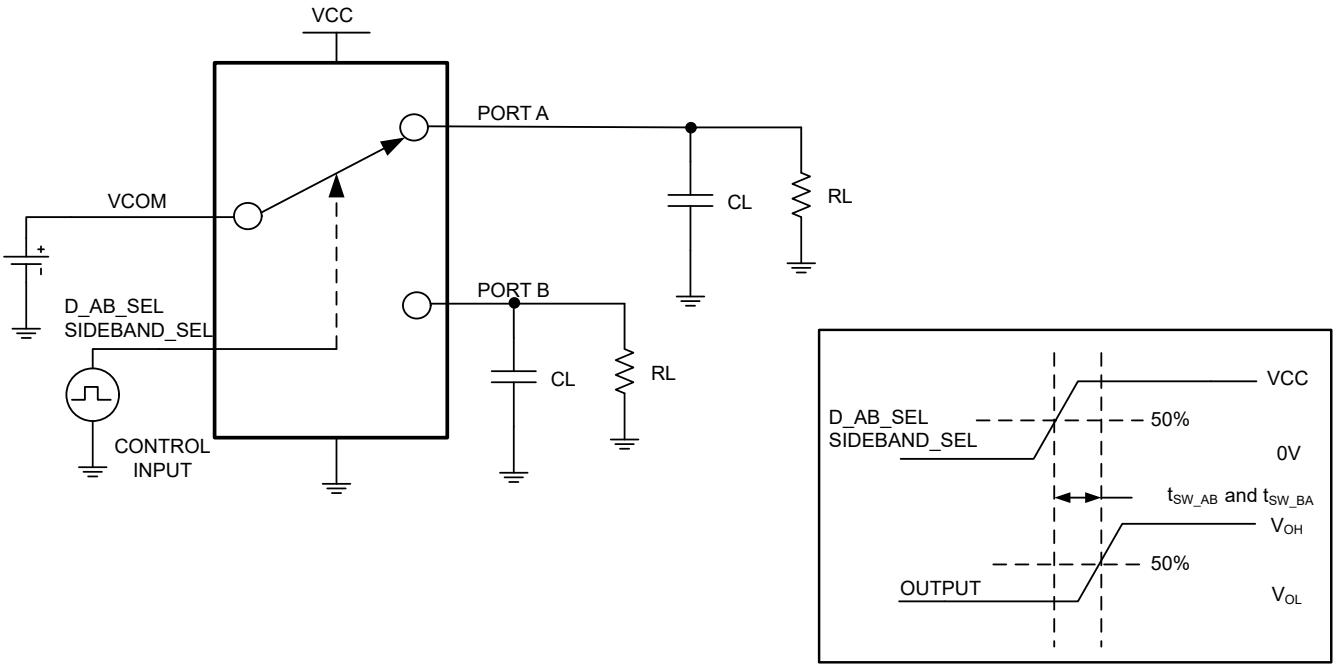
6 Parameter Measurement Information



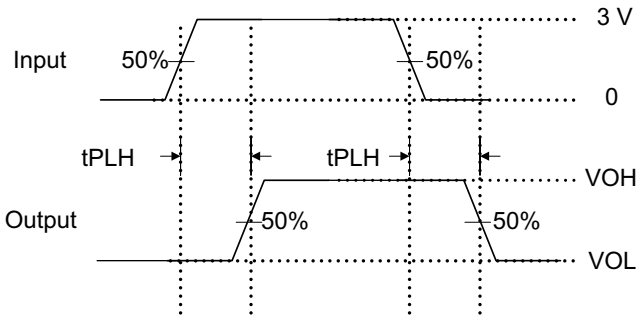
A. NOTE: RL = 10kΩ; VCOM = VCC; CL = 1pF

Figure 6-1. Switch Turn-On Time ($t_{SW\_POWER\_ON}$ and $t_{SW\_POWER\_OFF}$)



A. RL = 10kΩ; VCOM = VCC; CL = 1pF

Figure 6-2. Switching Time Between Channels (t_{SW_AB} and t_{SW_BA})



$$tpd = (tPLH + tPLH) / 2$$

Figure 6-3. Propagation Delay (t_{pd})

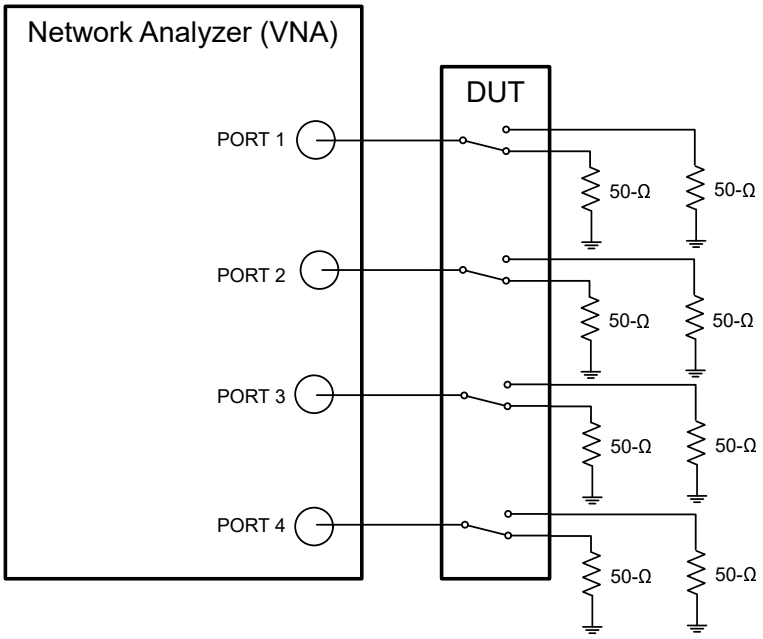


Figure 6-4. Crosstalk (Xtalk)

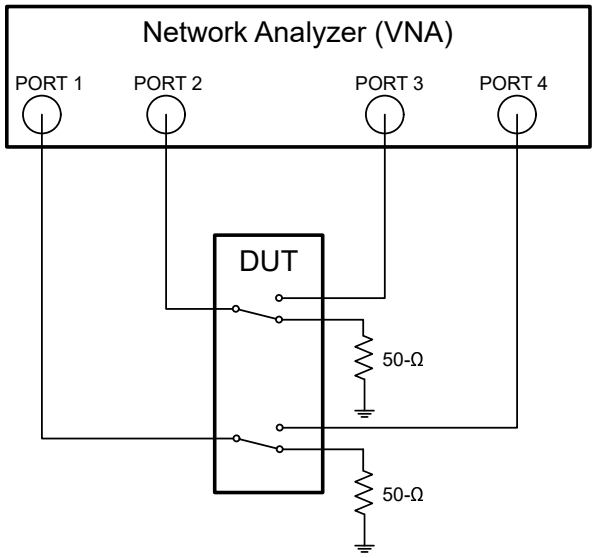


Figure 6-5. Differential Off-Isolation (OISO)

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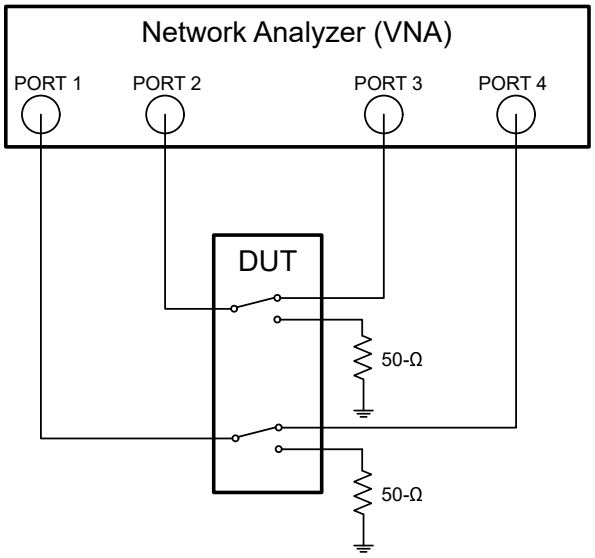


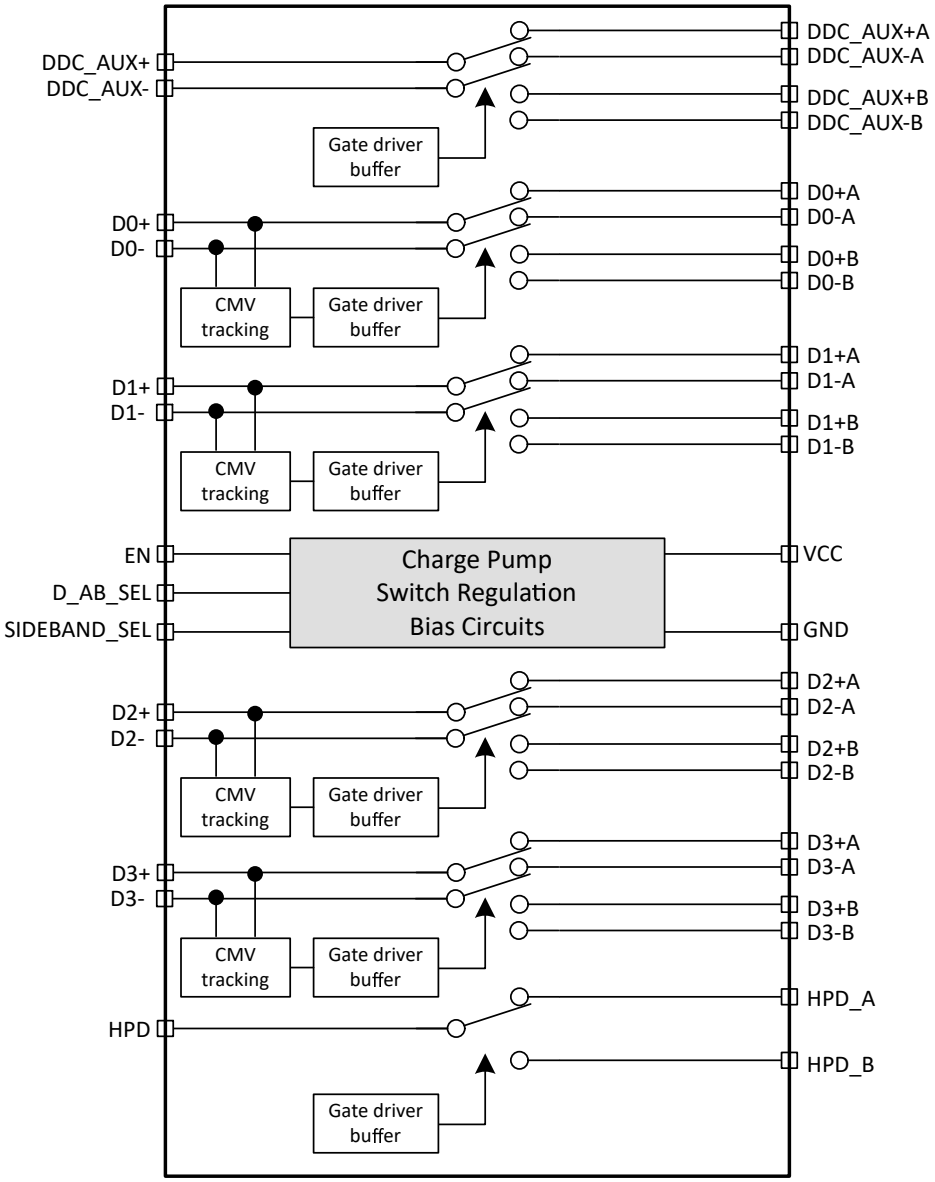
Figure 6-6. Differential Bandwidth (BW), Insertion Loss, and Return Loss

7 Detailed Description

7.1 Overview

The TMUXHS4612 is a protocol agnostic bidirectional multiplexer/demultiplexer that offers low on-state resistance as well as low I/O capacitance, which allows the device to achieve a high bandwidth of 15GHz typical for differential channels. The TMUXHS4612 is a passive mux that is recommended for data rates up to 20Gbps. However, the device can be used for interfaces with higher data rates if overall electrical link loss permits. The device's high-speed data channels provide the high bandwidth necessary for many interfaces to handle differential as well as single-ended signals as long as the single-ended signals do not violate V_{P-N_ABSMAX}. The device's high-speed channels support differential signaling with common-mode voltage range (CMV) of 0V to 3.6V making the device ideal for high common mode interfaces such as HDMI. The sideband channels are 5V tolerant. The sideband channels support 0V to 3.6V CMOS signals with a typical Ron of 8.5Ω and 5V CMOS signals with a typical Ron of 70Ω.

7.2 Functional Block Diagram



ADVANCE INFORMATION

7.3 Feature Description

The TMUXHS4612 is based on proprietary TI technology which uses FET switches driven by a high-voltage generated from an integrated charge-pump to achieve a low on-state resistance. The TMUXHS4612's low power technology uses only 750µA in active and just 30µA in powerdown (EN = L) mode. The device has integrated ESD that can support up to 1.5kV Human-Body Model (HBM) and 750V Charge Device Model (CDM). The TMUXHS4612 also has a special feature that prevents the device from back-powering when the V_{CC} supply is not available and an analog signal is applied on the I/O pin. In this situation this special feature prevents leakage current in the device. The TMUXHS4612 is not designed for passing signals with negative swings.

7.4 Device Functional Modes

Table 7-1 lists the device functions for the TMUXHS4612 device.

Table 7-1. Functional Table

EN	D_AB_SEL	SIDEBAND_SEL	FUNCTION
L	X	X	Switch disabled. All channels are Hi-Z.
H	L	L	All A channels are enabled. All B channels are Hi-Z.
H	L	H	All A data high-speed channels are enabled and B sideband channels are enabled. All other channels are Hi-Z.
H	H	L	All B data high-speed channels are enabled and A sideband channels are enabled. All other channels are Hi-Z.
H	H	H	All B channels are enabled. All A channels are Hi-Z.

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMUXHS4612 is a generic analog differential passive mux or demux that works for many high-speed differential interfaces with data rates up to 20Gbps. The TMUXHS4612 supports differential signaling with common-mode voltage range (CMV) of 0V to 3.6V and with differential amplitude up to 1600mVpp in Dxx channels. The device can be also used for single-ended CMOS signals with swing limited to 0V to 3.6V in sideband channels. The TMUXHS4612 can be used as mux or demux switch for:

- HDMI 1.4 up to 3.4Gbps, HDMI 2.0 up to 6Gbps and HDMI 2.1 up to 12Gbps
- DisplayPort (DP) for up to UHBR20 for data rates up to 20Gbps

8.2 Typical Application - HDMI

The TMUXHS4612 can be used to switch HDMI signals in both source and sink applications. In source applications HDMI port from a graphics processor can be demultiplexed into one of the two HDMI connectors. In a PC the TMUXHS4612 can be used to switch integrated graphics versus discrete graphics to a connector. In a sink application the device also can be used to select between two HDMI connectors to provide HDMI signals into a scaler (SOC) in HDMI sink application. This section provides detailed design implementation for a sink application where TMUXHS4612 provides 2:1 demultiplexing function.

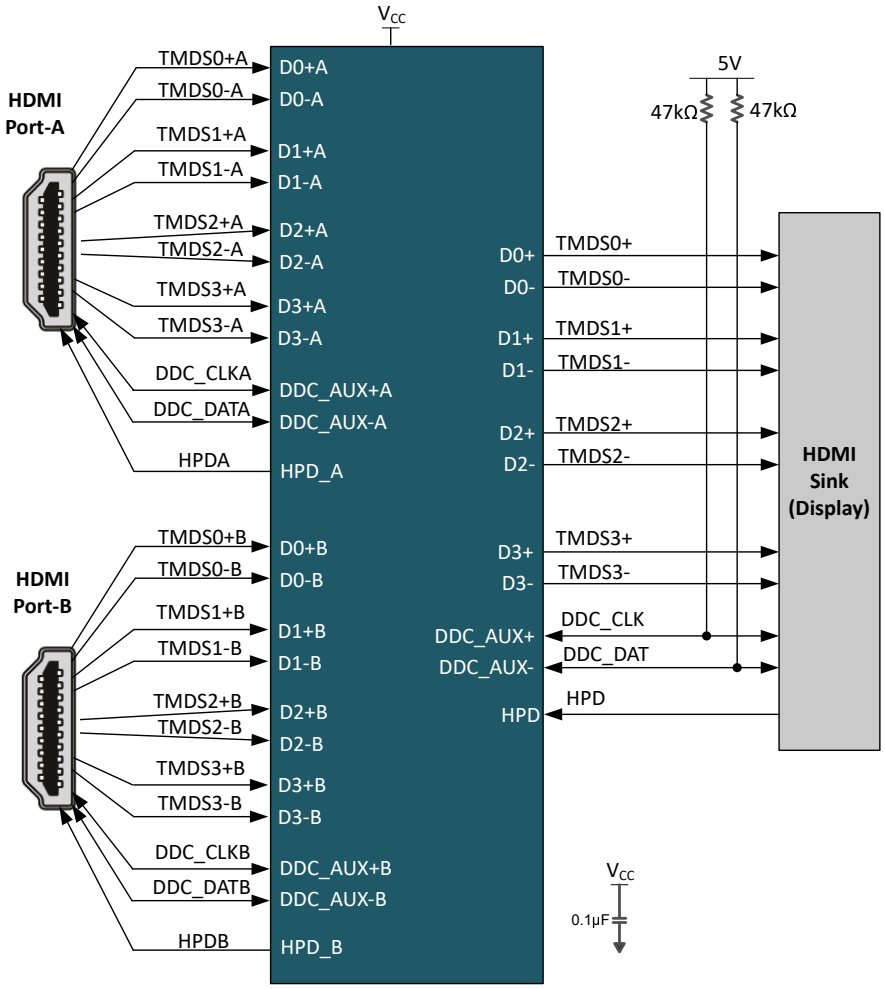


Figure 8-1. Choosing One of Two HDMI Port - Application Schematic

8.2.1 Design Requirements

Table 8-1 lists the design parameters for this HDMI example.

Table 8-1. Design Parameters for HDMI Application

Design parameter	Example value
V_{CC}	3V to 3.6V
VCC decoupling capacitor	0.1µF
DDC Pullup resistors	Sink Side: 47kΩ to 5V Source Side: 2kΩ to 5V

8.2.2 Detailed Design Procedure

The TMUXHS4612 is designed to operate with 3.0V to 3.6V power supply. Decoupling capacitors can be used to reduce noise and improve power supply integrity. Pullup resistors to 5V must be placed on the source side DDC clock and data lines according to the HDMI standard.

8.3 Power Supply Recommendations

Keep the V_{CC} in the range of 3.0V to 3.6V. Do not use voltage levels above those listed in the *Absolute Maximum Ratings* table. Use decoupling capacitors to reduce noise and improve power supply integrity. There are no power sequence requirements for the TMUXHS4612.

8.4 Layout

8.4.1 Layout Guidelines

To ensure reliability of the device, the following commonly used printed circuit board layout guidelines are recommended:

- Use decoupling capacitors between power supply pin and ground pin to ensure low impedance to reduce noise. To achieve a low impedance over a wide frequency range use capacitors with a high self-resonance frequency.
- Place ESD and EMI protection devices (if used) as close as possible to the connector.
- Use short trace lengths to avoid excessive loading.
- Keep traces at least two times the trace width apart to minimize the effects of crosstalk on adjacent traces.
- Separate high-speed signals from low-speed signals and digital from analog signals
- Avoid right-angle bends in a trace and try to route them at least with two 45° corners.
- Route the high-speed differential signal traces parallel to each other as much as possible. The traces are recommended to be symmetrical.
- Place a solid ground plane next to the high-speed signal layer. This also provides an excellent low-inductance path for the return current flow.

ADVANCE INFORMATION

8.4.2 Layout Example

The TMUXHS4612 application with a single controller interfacing between a common port and two separate ports.

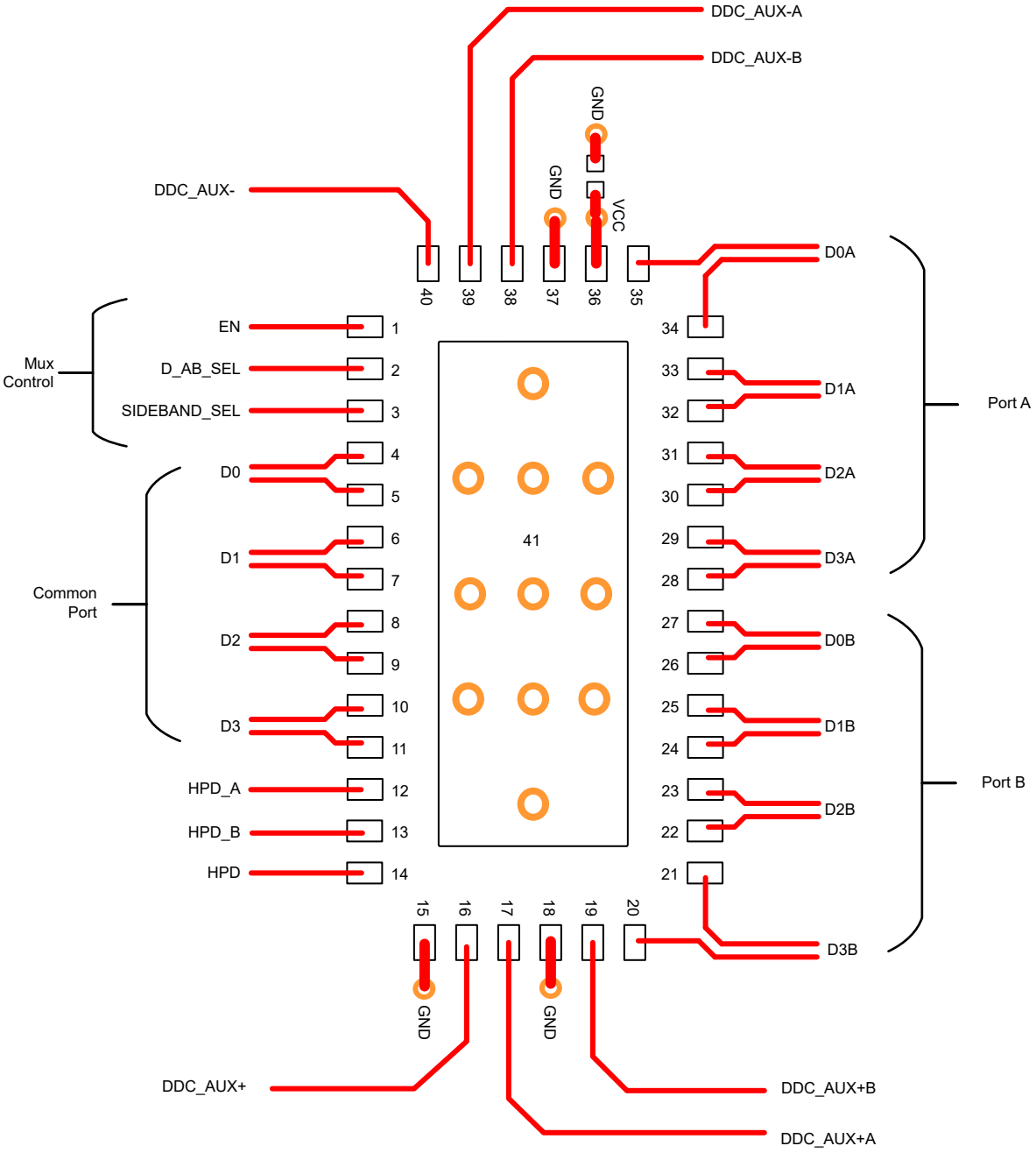


Figure 8-2. Layout Example

8.5 Systems Examples

8.5.1 DisplayPort 2:1 Mulitplexing

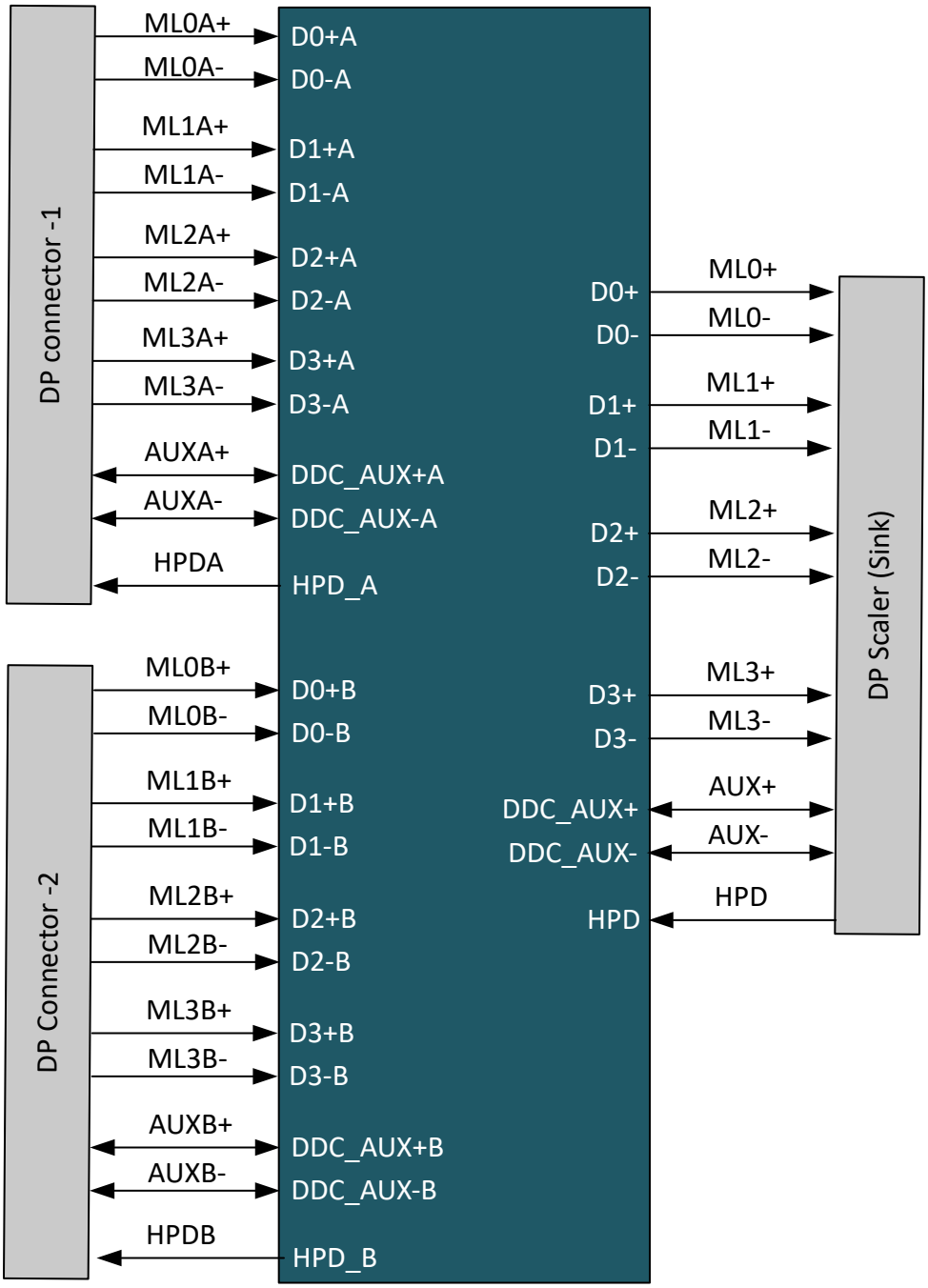


Figure 8-3. DisplayPort 2:1 Switching

ADVANCE INFORMATION

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

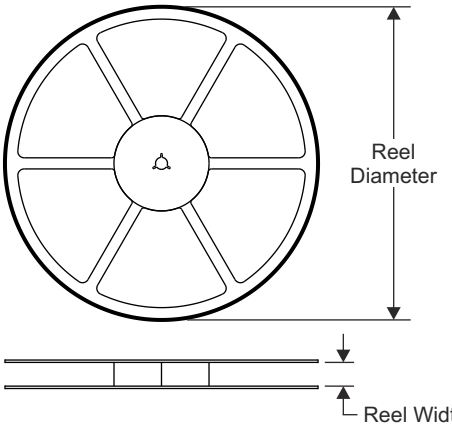
Date	Revision	Notes
June 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

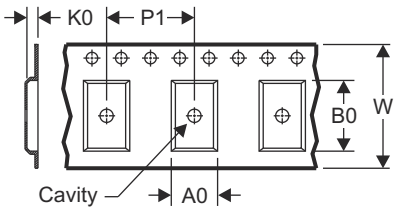
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

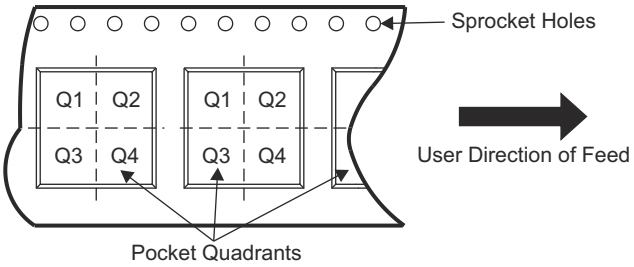


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

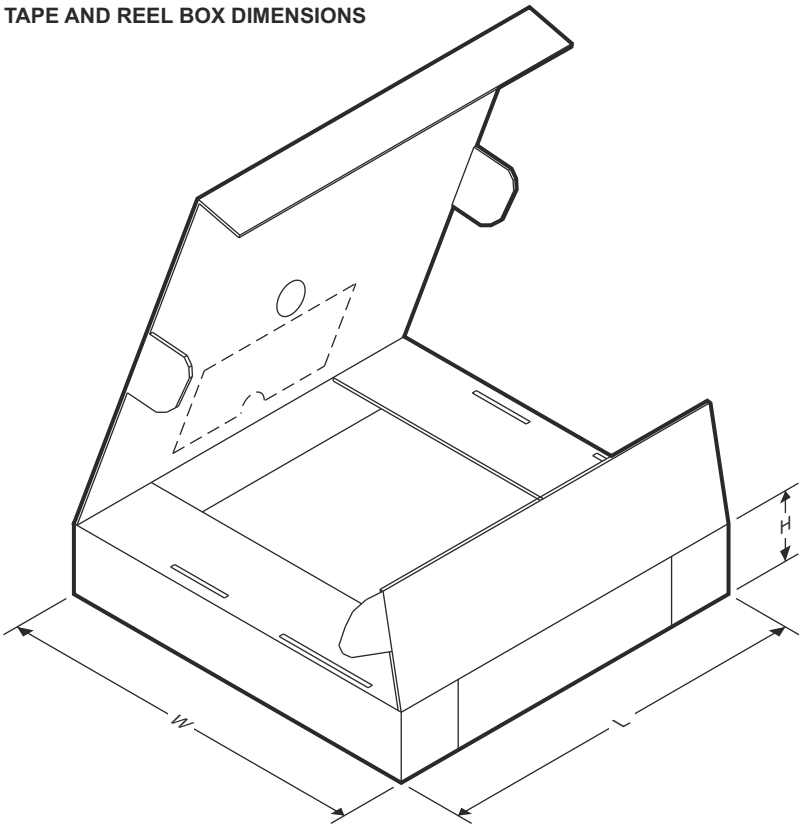


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTMUXHS4612RET	WQFN	RET	40	250	330	12.4	3.3	6.3	1.05	8.0	12.0	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTMUXHS4612RET	WQFN	RET	40	250	367.0	367.0	38.0

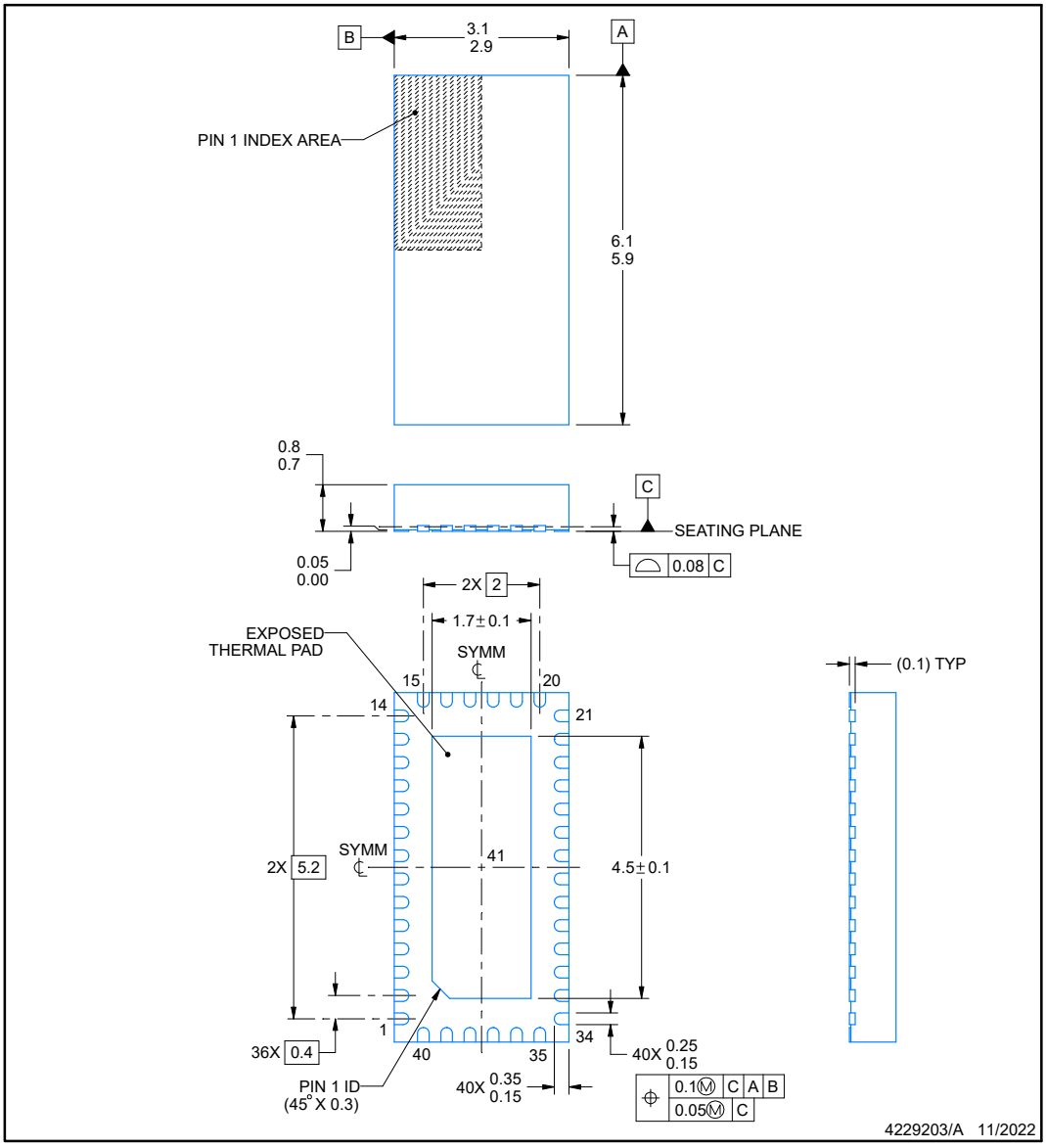
11.2 Mechanical Data

RET0040A

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

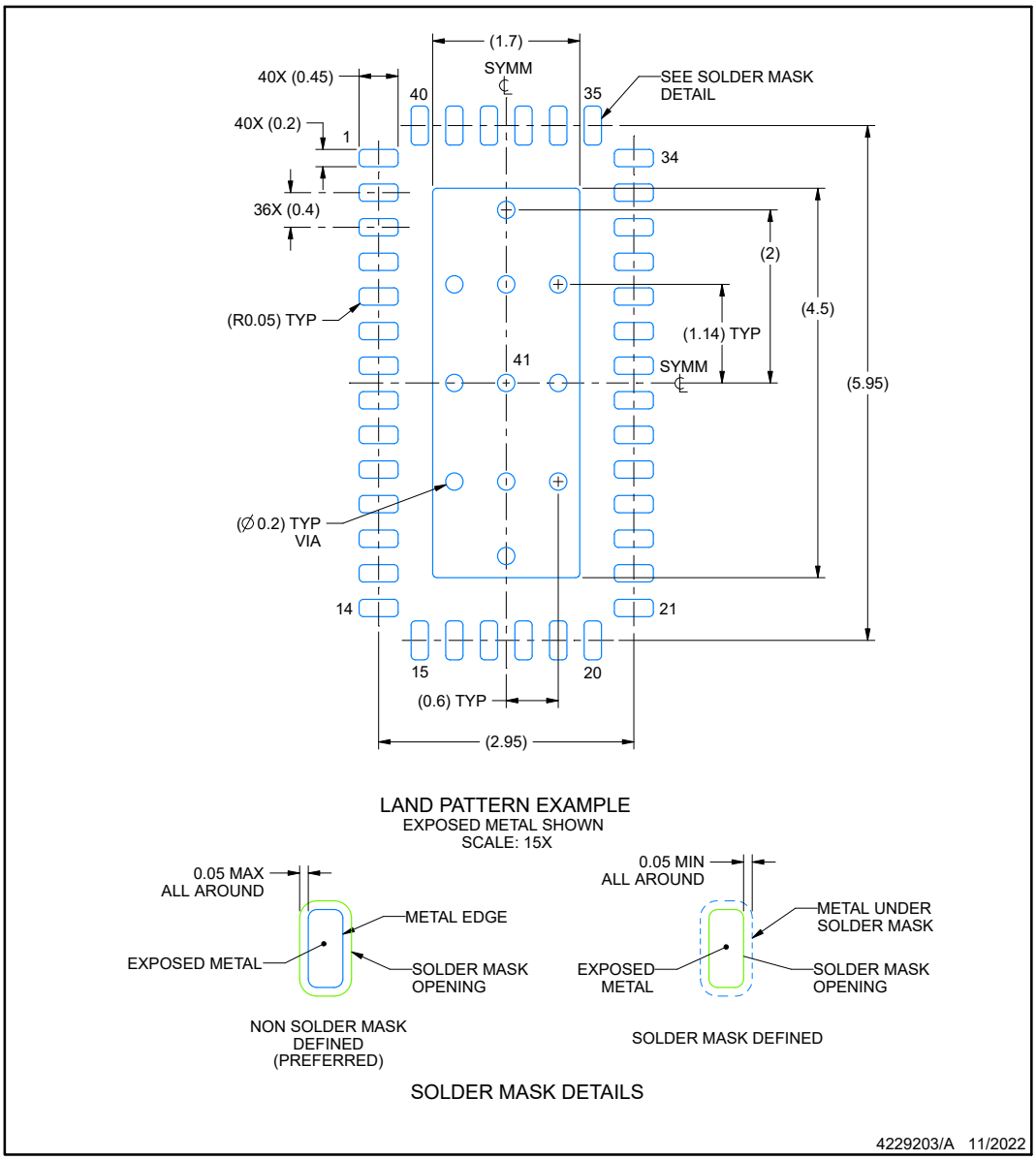
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RET0040A — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



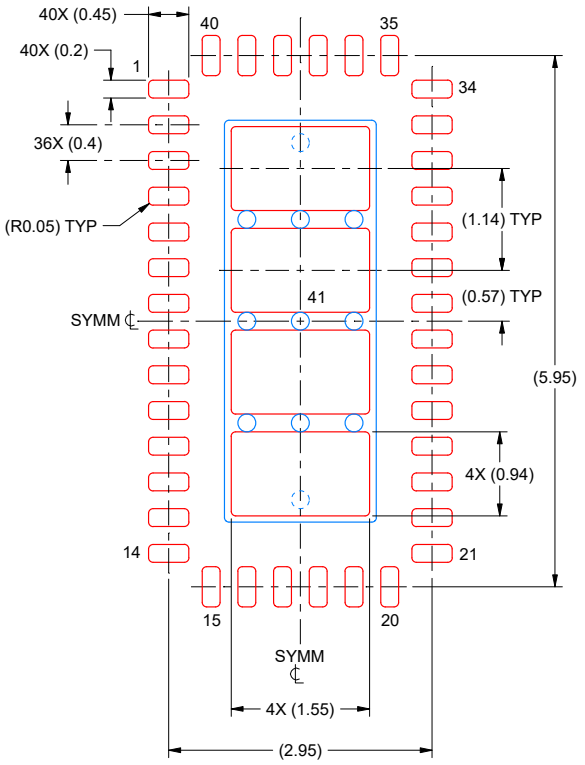
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RET0040A — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTMUXHS4612RET	ACTIVE	WQFN	RET	40	250	TBD	Call TI	Call TI	0 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

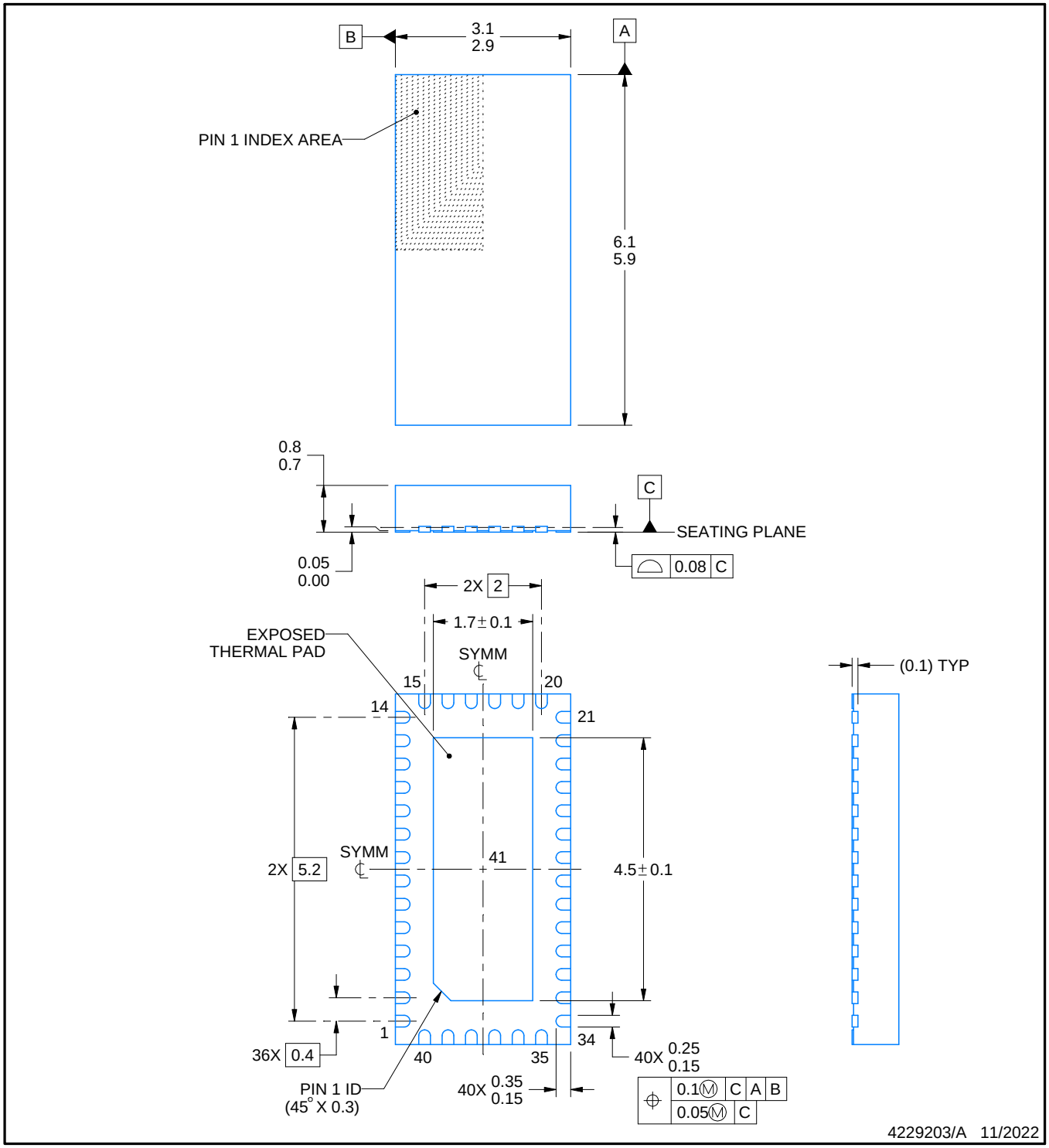
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

RET0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

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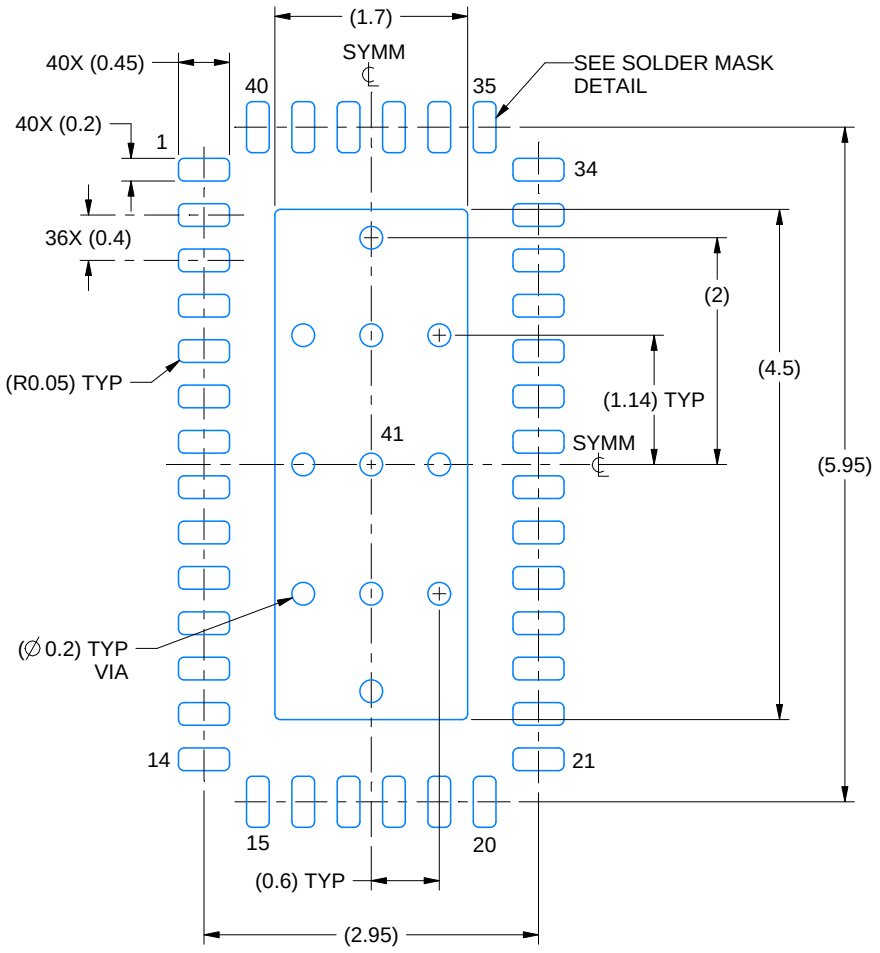
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

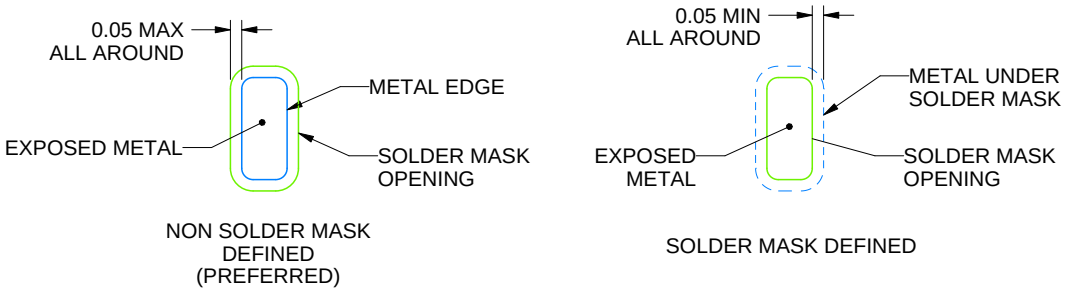
RET0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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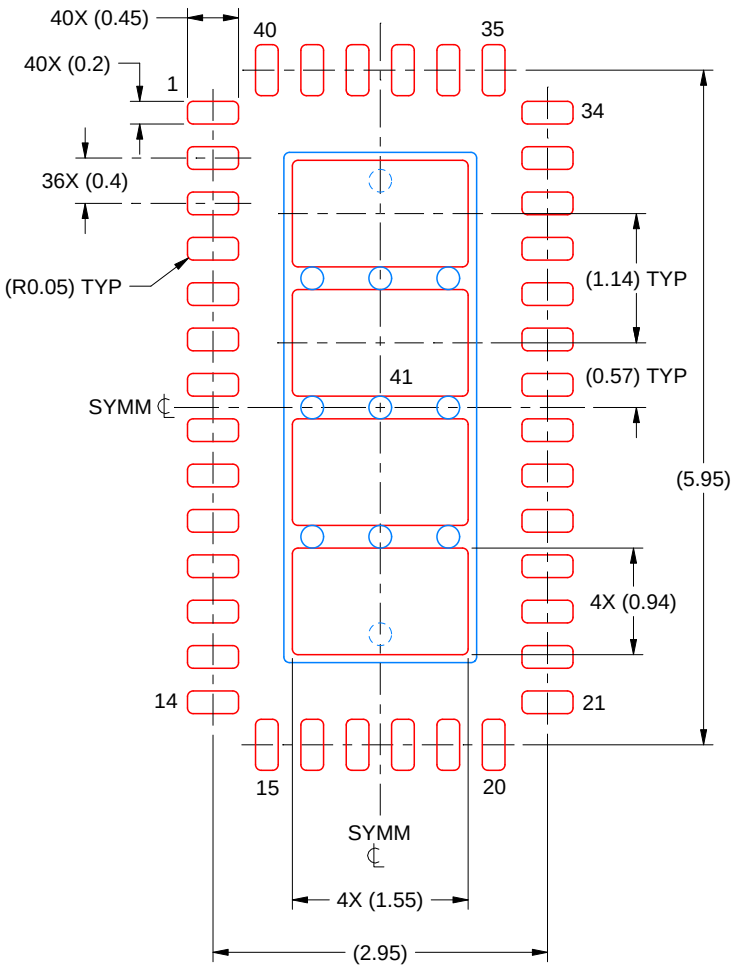
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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