TEXAS INSTRUMENTS
TPD4F202, TPD6F202
SLLS800B – JUNE 2010 – REVISED MAY 2021

TPDxF202 Four or Six-Channel EMI Filter With ESD Protection For LCD Display

1 Features

- Four or six-channel EMI filtering and ESD protection for data lines
- Excellent filter performance
  - > 40-dB attenuation at 1 GHz to 3G Hz
  - –3-dB bandwidth at 108 MHz
  - 70-dB crosstalk attenuation at 100 MHz
- Exceeds IEC 61000-4-2 (Level 4) ESD protection requirements
  - ±25-kV IEC 61000-4-2 contact discharge
  - ±25-kV IEC 61000-4-2 air-gap discharge
  - ±15-kV human body model (HBM)
- Pi-style C-R-C filter configuration offers symmetric filter performance
  (R = 100 Ω, C_{TOTAL} = 30 pF)
- Low 10-nA leakage current
- Space-saving DSBGA package and flow-through pin mapping provide optimum performance in portable applications

2 Applications

- End equipment:
  - LCD displays
  - Memory interface
  - Keypads
  - Portables
- Interfaces:
  - DVI
  - VGA, SVGA
  - SIM cards
  - Data lines

3 Description

The TPDxF202 devices are four or six-channel EMI filters, designed particularly to suppress EMI noise in the cell phone and other portable applications. These filters also provide a Transient Voltage Suppressor (TVS) diode circuit for Electrostatic Discharge (ESD) protection which prevents damage to the application when subjected to ESD stress far exceeding IEC 61000-4-2 (Level 4). The pi-style C-R-C filter provides symmetric filter performance in the data lines to and from either side of the filter.

Due to the tiny parasitics of the DSBGA package, the TPDxF202 filters provide excellent signal attenuation (–40 dB at 1 GHz) at the typical cell-phone carrier frequency ranges.

The ultra thin (0.3-mm package height, when mounted on board) space-saving YFU package enables the TPDxF202 devices to mount on the printed-circuit-boards where height is a key constraint.

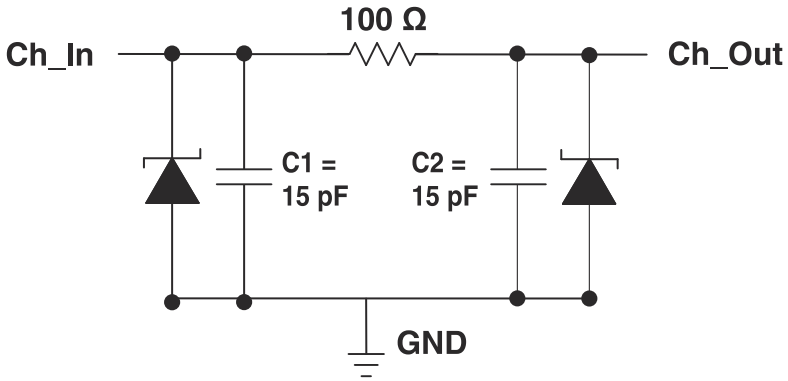
The TPDxF202 devices are specified for –40°C to 85°C operation.

A typical application for TPDxF202 devices are in portable equipment with DVI, VGA, SVGA, SIM Card, and other data interfaces.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4F202	DSBGA (10)	1.06 mm × 1.57 mm
TPD6F202	DSBGA (15)	1.06 mm × 2.36 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2015) to Revision B (May 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed the dimensions for the DSBGA (15) package from *1.06 mm × 2.63 mm* to *1.06 mm × 2.36 mm* in the *Device Information* table	1

Changes from Revision * (June 2010) to Revision A (November 2015)	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* section	1

5 Pin Configuration and Functions

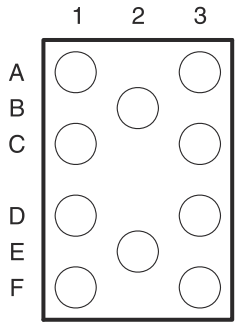


Figure 5-1. YFU Package 10-Pin DSBGA Top View

Table 5-1. Pin Functions — TPD4F202

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	Ch1_In	I/O	ESD-protected channel, route to connector. Corresponds with CH1_Out.
A3	Ch1_Out	I/O	ESD-protected channel, route to system. Corresponds with CH1_In.
B2	GND	G	Ground
C1	Ch2_In	I/O	ESD-protected channel, route to connector. Corresponds with CH2_Out.
C3	Ch2_Out	I/O	ESD-protected channel, route to system. Corresponds with CH2_In.
D1	Ch3_In	I/O	ESD-protected channel, route to connector. Corresponds with CH3_Out.
D3	Ch3_Out	I/O	ESD-protected channel, route to system. Corresponds with CH3_In.
E2	GND	G	Ground
F1	Ch4_In	I/O	ESD-protected channel, route to connector. Corresponds with CH4_Out.
F3	Ch4_Out	I/O	ESD-protected channel, route to system. Corresponds with CH4_In.

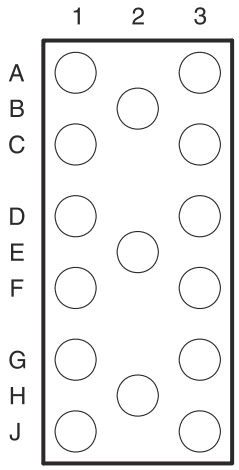


Figure 5-2. YFU Package 15-Pin DSBGA Top View

Table 5-2. Pin Functions — TPD6F202

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	Ch1_In	I/O	ESD-protected channel, route to connector. Corresponds with CH1_Out.
A3	Ch1_Out	I/O	ESD-protected channel, route to system. Corresponds with CH1_In.
B2	GND	G	Ground
C1	Ch2_In	I/O	ESD-protected channel, route to connector. Corresponds with CH2_Out.
C3	Ch2_Out	I/O	ESD-protected channel, route to system. Corresponds with CH2_In.
D1	Ch3_In	I/O	ESD-protected channel, route to connector. Corresponds with CH3_Out.
D3	Ch3_Out	I/O	ESD-protected channel, route to system. Corresponds with CH3_In.
E2	GND	G	Ground
F1	Ch4_In	I/O	ESD-protected channel, route to connector. Corresponds with CH4_Out.
F3	Ch4_Out	I/O	ESD-protected channel, route to system. Corresponds with CH4_In.
G1	Ch5_In	I/O	ESD-protected channel, route to connector. Corresponds with CH5_Out.
G3	Ch5_Out	I/O	ESD-protected channel, route to system. Corresponds with CH5_In.
H2	GND	G	Ground
J1	Ch6_In	I/O	ESD-protected channel, route to connector. Corresponds with CH6_Out.
J3	Ch6_Out	I/O	ESD-protected channel, route to system. Corresponds with CH6_In.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IO}	IO to GND	–0.3	6	V
	Continuous power dissipation (T_A = 70°C)		100	mW
T_J	Junction temperature		150	°C
	Lead temperature (soldering, 10 s)		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings — JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±15000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings — IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±25000	V
		IEC 61000-4-2 air-gap discharge	±25000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	I/O to GND	0	5.5	V
T_A	Ambient temperature	–40	85	°C

6.5 Thermal Information

THERMAL METRIC(1)		TPD4F202 YFU (DSBGA) 10 PINS	TPD6F202 YFU (DSBGA) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.8	72	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.7	14.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.7	14.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

T_A = –40°C to 85°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{BR}	DC breakdown voltage	I_{IO} = 10 µA	6			V
R	Resistance		85	100	115	Ω
C	Capacitance (C1 or C2)	V_{IO} = 3.3 V, f = 1 MHz		15		pF
I_{IO}	Channel leakage current	V_{IO} = 3.3 V		10		nA
f_C	Cut-off frequency	Z_{SOURCE} = 50 Ω, Z_{LOAD} = 50 Ω		108		MHz

(1) Typical values are at T_A = 25°C.

6.7 Typical Characteristics

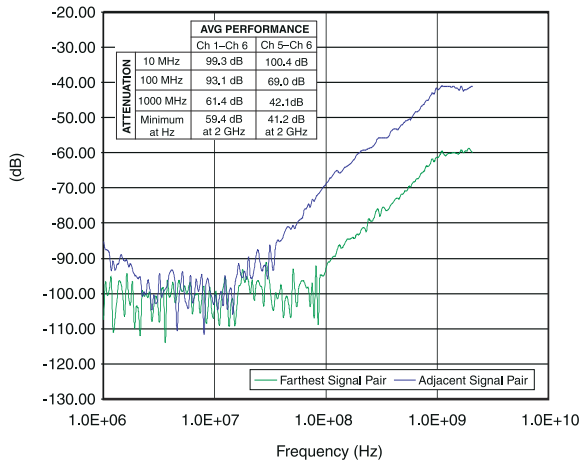


Figure 6-1. Channel-to-Channel Crosstalk

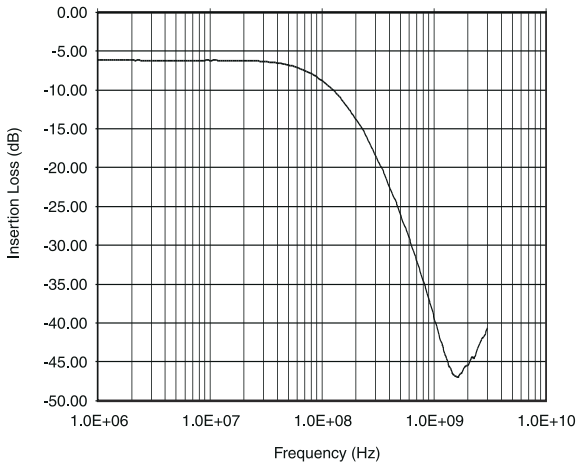


Figure 6-2. Frequency Response Data (0-V Bias)

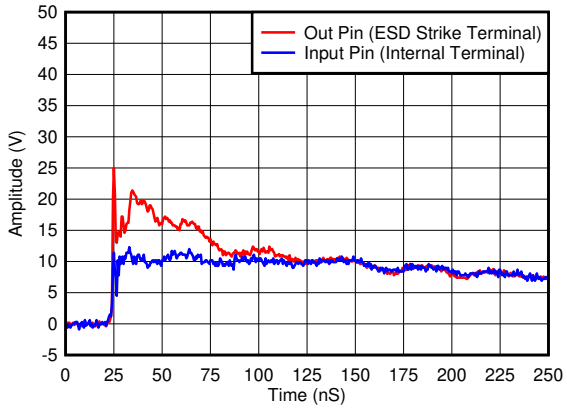


Figure 6-3. IEC Clamping Waveforms +8-kV Contact

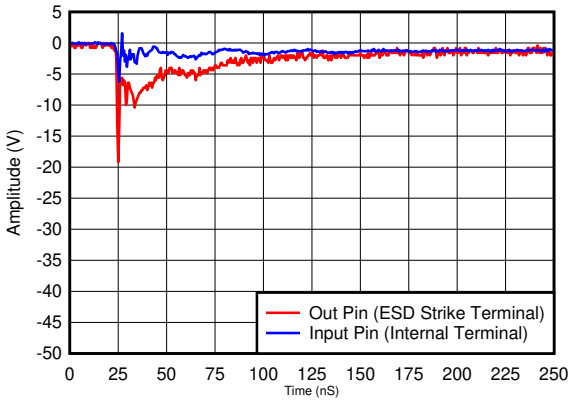


Figure 6-4. IEC Clamping Waveforms –8-kV Contact

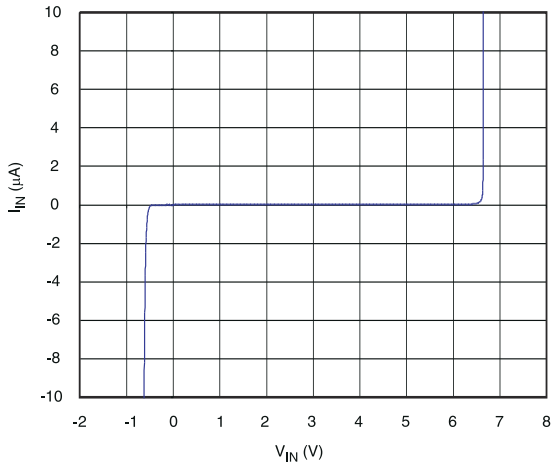


Figure 6-5. DC Characteristics (I_{IN} vs V_{IN}), T_A = 25°C

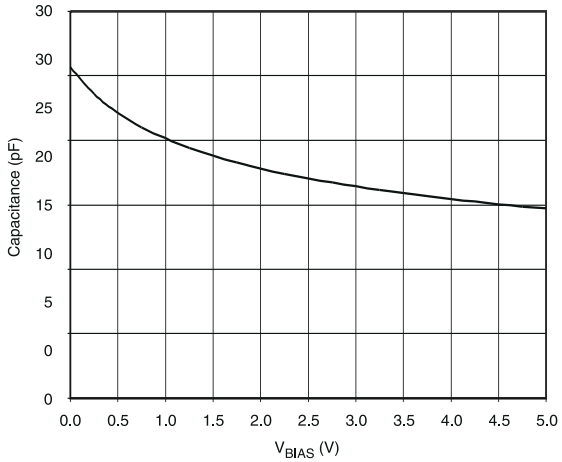


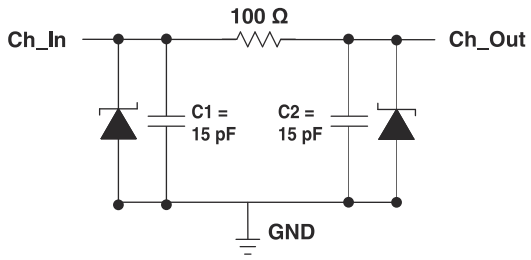
Figure 6-6. C1 or C2 Capacitance vs V_{BIAS}

7 Detailed Description

7.1 Overview

The TPDxF202 family is a series of highly integrated devices designed to provide EMI filtering in all systems subjected to electromagnetic interference. These filters also provide a Transient Voltage Suppressor (TVS) diode circuit for ESD protection which prevents damage to the application when subjected to ESD stress far exceeding IEC 61000-4-2 (Level 4).

7.2 Functional Block Diagram



7.3 Feature Description

The TPDxF202 family is a line of ESD and EMI filtering devices designed to reduce EMI emissions and provide system level ESD protection. Each device can dissipate ESD strikes above the maximum level specified by IEC 61000-4-2 international standard. Additionally, the EMI filtering structure reduces EMI emissions by providing high frequency roll-off.

7.3.1 Exceeds IEC61000-4-2 (Level 4) ESD Protection Requirements

The ESD protection on all pins exceeds the IEC 61000-4-2 level 4 standard. Contact and Air-Gap ESD are rated at ±25 kV.

7.3.2 Pi-Style C-R-C Filter Configuration

This family of devices has a pi-style filtering configuration composed of a series resistor and two capacitors in parallel with the I/O pins. The typical resistor value is 100 Ω and the typical capacitor values are 15 pF each. Signal attenuation is above 40 dB at 1 GHz to 3 GHz, which provides significant reduction in spurious emissions, with a bandwidth (3-dB loss) of 108 MHz. Crosstalk is attenuated 70 dB at 100 MHz.

7.3.3 Low 10-nA Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (typical) with a bias of 3.3 V.

7.3.4 Space-Saving DSBGA Package

The DSBGA package is characterized by a minimal footprint for savings in board space, fitting the design philosophy of portable devices.

7.3.4.1 Flow-Through Pin Mapping

The pinout of this device makes it easy to add protection to existing board layouts. The packages offer flow-through routing which requires minimal changes to existing board layout for addition of these devices.

7.4 Device Functional Modes

The TPDxF202 family of devices are passive-integrated circuits that passively filter EMI and trigger when voltages are above V_{BR} or below the lower diode voltage (–0.6 V). During IEC 61000-4-2 ESD events, transient voltages as high as ±25 kV can be directed to ground through the internal diode network. Once the voltages on the protected line falls below the trigger levels, the device reverts to passive.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPDxF202 family are diode-type TVSs integrated with series resistors and parallel capacitors for filtering emitted EMI. As a signal passes through the device, higher frequency components are filtered out. This device also provides a path to ground during ESD events and isolates the protected IC. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. In particular, these filters are ideal for EMI filtering and protecting data lines from ESD at display, keypad, and memory interfaces.

8.2 Typical Application

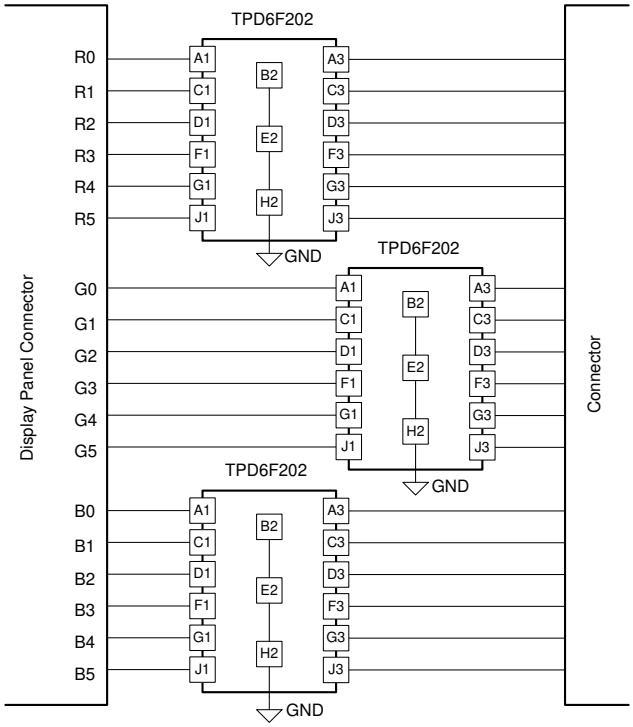


Figure 8-1. Display Panel Schematic

8.2.1 Design Requirements

For this design example, three TPD6F202 devices are used in an 18-bit display panel application. This application provides a complete ESD and EMI protection solution for the display connector. For the display panel application, the following parameters are in shown Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on all pins except GND	0 V to 5 V
Data Rate	200 Mbps
ESD Protection Level	IEC 61000-4-2 Level 4

8.2.2 Detailed Design Procedure

To begin the design process, some design parameters must be decided; the designer needs to know the operating frequency and the signal range on all the protected lines.

8.2.2.1 Signal Range on All Protected Lines

The TPD6F202 has 6 identical protection channels for signal lines. All I/O pins will support a signal range from 0 to 5.5 V.

8.2.2.2 Data Rate

The TPD6F202 has a 108-MHz, –3-dB bandwidth, which supports the data rate for this display.

8.2.2.3 ESD Protection Level

The contact and air-gap ratings of ± 25 kV for TPD6F202 exceeds the IEC 61000-4-2 Level 4 rating of ± 8-kV contact and ± 15-kV air-gap ratings.

8.2.3 Application Curve

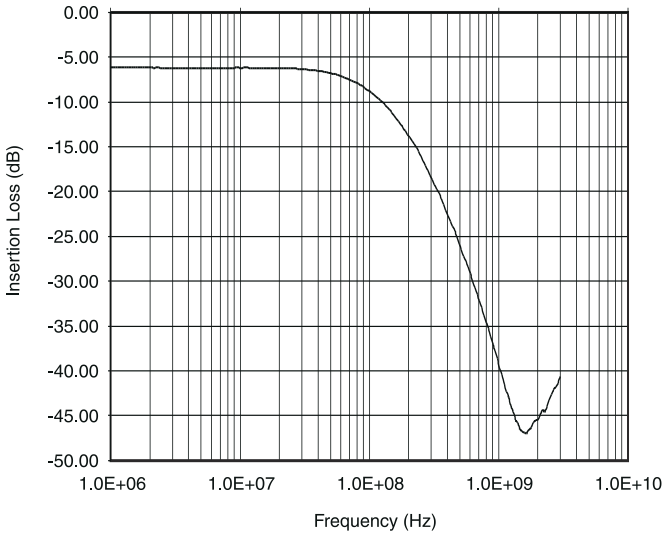


Figure 8-2. Frequency Response Data (0-V Bias)

9 Power Supply Recommendations

The TPDxF202 device is a passive ESD-protection device, and therefore, does not require a power supply. Take care to avoid violating the maximum-voltage specification to ensure that the device functions properly. The IO lines can tolerate up to 6-V DC.

10 Layout

10.1 Layout Guidelines

Typically, there are multiple EMI filters being used in portable applications to suppress the EMI interference. This means the total board area consumed by EMI filters are relatively large. One example of space-saving innovation is to place the EMI filters right under the connectors so that the main PCB space is not used. The YFU packages of the TPDxF202 series offer ultra low-profile package height which enables such innovative component placement in portable applications. Package under-fill is recommended while using the YFU packages in flex boards.

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

For maximum efficiency of filtering and ESD protection, while doing the board layout, take care to reduce board parasitic series inductances from package GND pins to board GND plane. The TPDxF202 devices must be connected to a ground plane with a micro via adjacent to the device GND pad. If this is not possible, the connection to the ground plane must be as direct as possible to minimize the inductance. Due to flow-through pin mapping, the signal pins routing is easily achieved in a single layer.

10.2 Layout Example

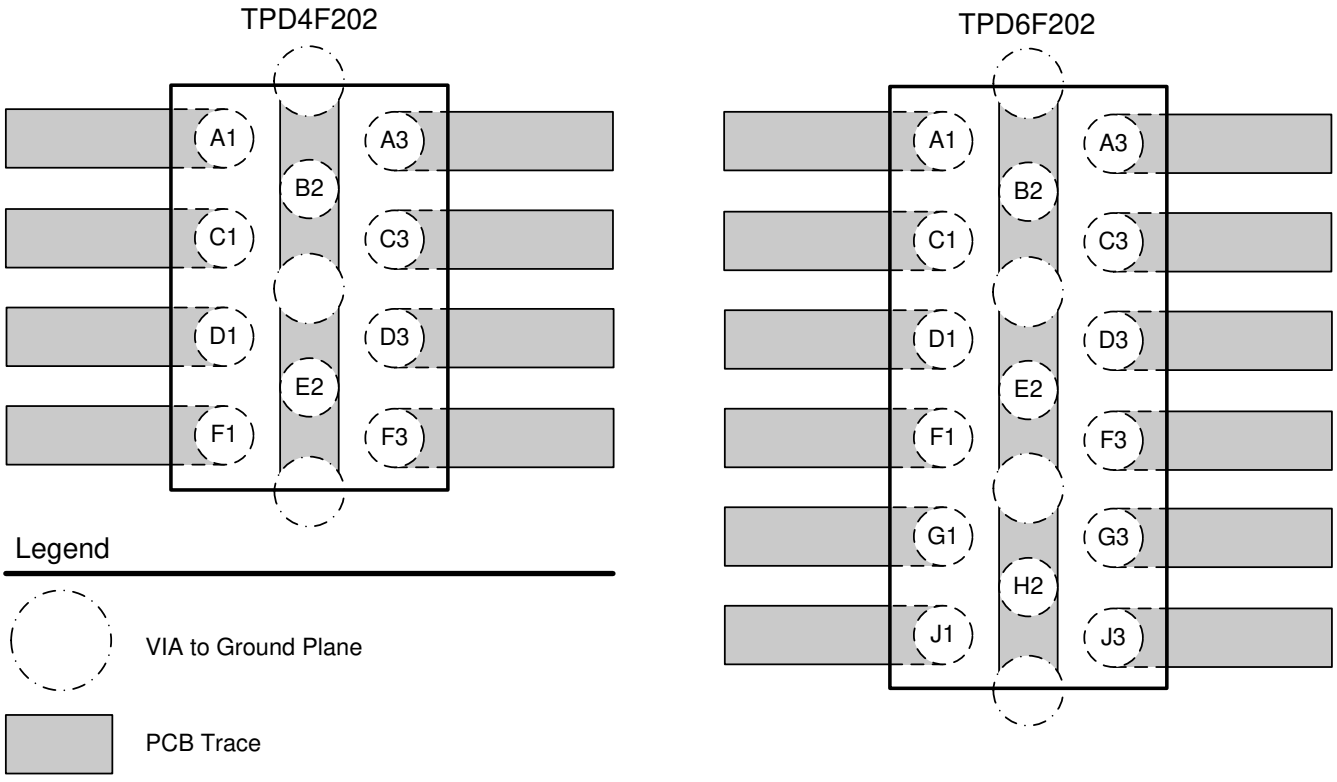


Figure 10-1. Board Layout With TPDxF202

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

The following documents contain additional information related to the use of the TPDxF202 device:

- Texas Instruments, *ESD Protection Layout Guide* application report
- Texas Intruments, *Reading and Understanding an ESD Protection Data Sheet* application report

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPD4F202	Click here	Click here	Click here	Click here	Click here
TPD6F202	Click here	Click here	Click here	Click here	Click here

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD6F202YFUR	OBSOLETE	DSBGA	YFU	15		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

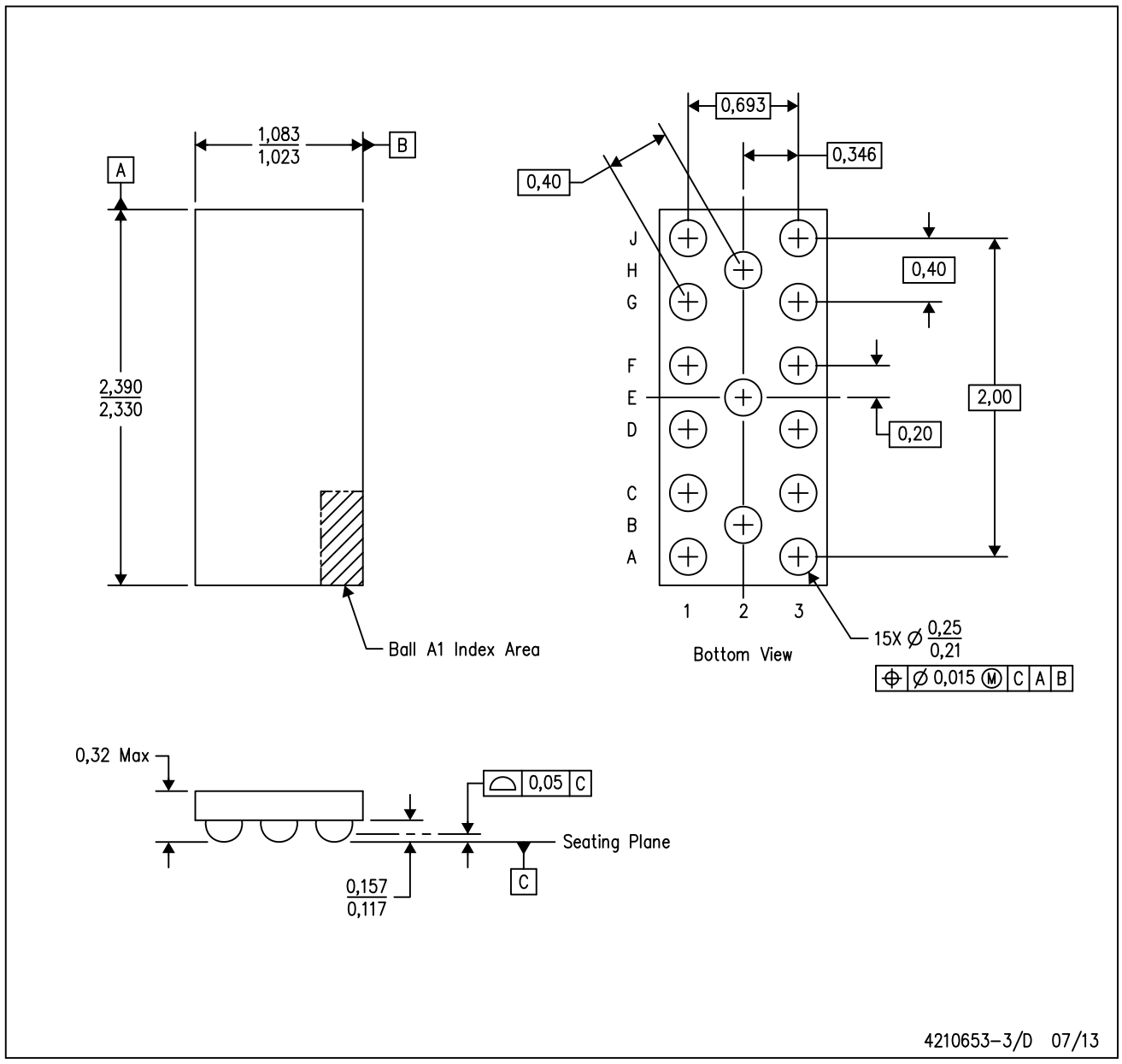
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

YFU (R–XBGA–N15) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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