

# TPS25751A USB Type-C® and USB PD Controller With Integrated Power Switches Optimized for DRP Power Applications

## 1 Features

- This device is certified by the USB-IF for PD3.2
  - TPS25751A TID#: 15341
  - Article on [PD2.0 vs. PD3.0](#)
- Optimized for USB Type-C PD Sink (UFP) and Dual Role Power (DRP) power applications
  - Built in I2C control for TI battery chargers
  - [Web-based GUI](#) and pre-configured firmware
  - For a more extensive selection guide and getting started information, please refer to [www.ti.com/usb-c](http://www.ti.com/usb-c)
- Programmable power supply (PPS) and adjustable voltage supply (AVS)
  - Supports PPS source and sink
  - Standalone PPS source control TI battery chargers
  - Programmable interface for PPS sink
  - Supports AVS source
- Liquid detection
  - Measures directly at the Type-C connector
  - Integrated error handling and protection
- Integrated fully managed power paths
  - Integrated 5V, 3A, and 36mΩ sourcing switch (TPS25751AD and TPS25751AS)
  - Integrated 20V, 5A, 15mΩ bi-directional load switch (TPS25751AD only)
- Integrated robust power path protection
  - 20V, 5A bi-directional switch: reverse current protection (RCP), undervoltage protection (UVP), overvoltage protection (OVP), and slew rate control
  - 5V, 3A sourcing switch: OVP, UVP, and current limiting (ILIM) for inrush current protection
  - 26V tolerant CC pins for robust protection when connected to non-compliant devices
- Additional features
  - 11 configurable GPIOs
  - BC1.2 charging support
  - 3.3V LDO output for dead battery support
  - Power supply from 3.3V or VBUS source
  - 1 I2C controller port
  - 1 I2C target port

## 2 Applications

- [Power tools](#), [power banks](#), [retail and payment](#)
- [Wireless speakers](#), [cordless vacuum cleaner](#)
- [personal electronics](#) and [industrial applications](#)
- [Home health care](#) and [personal care and fitness](#)

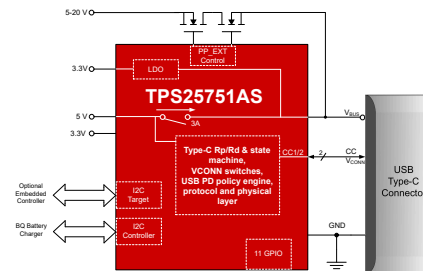
## 3 Description

The TPS25751A is a highly integrated stand-alone USB Type-C and Power Delivery (PD) controller optimized for applications supporting USB-C PD Power. The TPS25751A integrates fully managed power paths with robust protection for a complete USB-C PD application. The TPS25751A also integrates control for external battery charger ICs for added ease of use and reduced time to market. The intuitive web based GUI asks the user a few simple questions on the applications needs using clear block diagrams and simple multiple-choice questions. As a result, the GUI creates the configuration image for the user's application, reducing much of the complexity associated with USB PD applications.

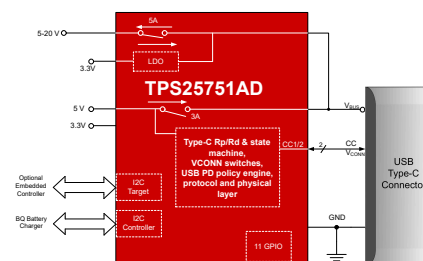
### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TPS25751AD	38-WQFN (REF)	4.00mm x 6.00mm
TPS25751AS	32-VQFN (RSM)	4.00mm x 4.00mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



**TPS25751AS Schematic**



**TPS25751AD Schematic**

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## 4 Device Comparison Table

DEVICE NUMBER	5V SOURCE LOAD SWITCH	INTEGRATED HIGH VOLTAGE BI-DIRECTIONAL LOAD SWITCH (PPHV)	HIGH VOLTAGE GATE DRIVER FOR BI-DIRECTIONAL EXTERNAL PATH (PP_EXT)
TPS25751AD	Yes	Yes	No
TPS25751AS	Yes	No	Yes

## 5 Pin Configuration and Functions

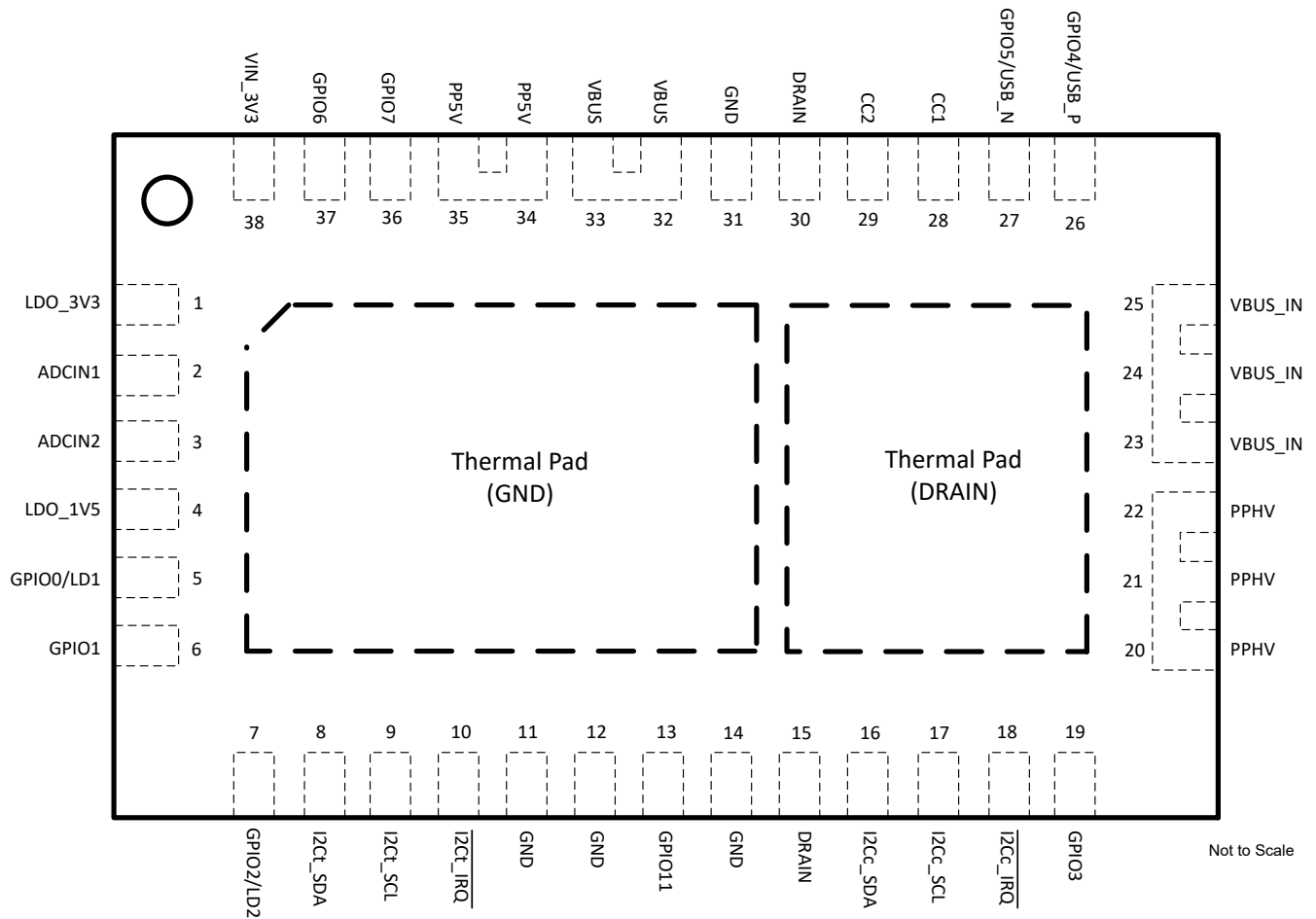


Figure 5-1. TPS25751AD QFN Package, 38-Pin (Top View)

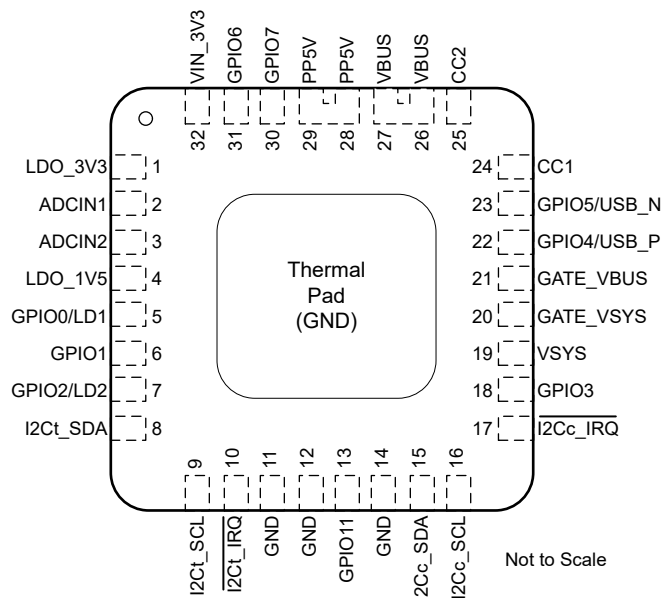


Figure 5-2. TPS25751AS QFN Package, 32-Pin (Top View)

**Table 5-1. TPS25751AD Pin Functions**

PIN		TYPE <sup>(1)</sup>	RESET	DESCRIPTION
NAME	NO.			
ADCIN1	2	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
ADCIN2	3	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CC1	28	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (C <sub>CC</sub> ).
CC2	29	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (C <sub>CC</sub> ).
GND	11, 12, 14, 31	—	—	Ground. Connect to ground plane.
GPIO0/LD1	5	GPIO	Hi-Z	General purpose digital I/O. Pin can be connected for liquid detection on the Type-C connector. Tie to ground when unused.
GPIO1	6	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO2/LD2	7	GPIO	Hi-Z	General purpose digital I/O. Pin can be connected for liquid detection on the Type-C connector. Tie to ground when unused.
GPIO3	19	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when pin is unused.
GPIO5/USB_N	27	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused. Pin can be connected to D- for BC1.2 support.
GPIO4/USB_P	26	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused. Pin can be connected to D+ for BC1.2 support.
GPIO6	37	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO7	36	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when pin is unused.
I2Ct_SCL	9	I	Hi-Z	I2C target serial clock input. Tie to pullup voltage through a resistor. Tie to ground when pin is unused.
I2Ct_SDA	8	I/O	Hi-Z	I2C target serial data. Open-drain input/output. Tie to pullup voltage through a resistor. Tie to ground when pin is unused.
I2Ct_IRQ	10	O	Hi-Z	I2C target interrupt. Active low. Connect to external voltage through a pull-up resistor. Pin can be re-configured to GPIO10. Tie to ground if unused.
I2Cc_SCL	17	O	Hi-Z	I2C controller serial clock. Open-drain output. Tie to pullup voltage through a resistor. Tie to ground when pin is unused.
GPIO11	13	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when pin is unused.
I2Cc_SDA	16	I/O	Hi-Z	I2C controller serial data. Open-drain input/output. Tie to pullup voltage through a resistor. Tie to ground when pin is unused.
I2Cc_IRQ	18	I	Hi-Z	I2C controller interrupt. Active low. Connect to external voltage through a pull-up resistor. Do not tie to GND when unused. Pin can be re-configured to GPIO12.
LDO_1V5	4	O	—	Output of the CORE LDO. Bypass with capacitance C <sub>LDO_1V5</sub> to GND. This pin cannot source current to external circuits.
LDO_3V3	1	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance C <sub>LDO_3V3</sub> to GND.
DRAIN	15, 30	N/A	—	Connects to drain of internal FET.
PP5V	34, 35	I	—	5V system supply to VBUS, supply for CC <sub>y</sub> pins as VCONN.
PPHV	20, 21, 22	I/O		High-voltage sinking node in the system.
VBUS_IN	23, 24, 25	I/O		5V to 20V input.
VBUS	32, 33	O		VBUS input to LDO. Bypass with capacitance C <sub>VBUS</sub> to GND.
VIN_3V3	38	I	—	Supply for core circuitry and I/O. Bypass with capacitance C <sub>VIN_3V3</sub> to GND. Tie to GND if device is VBUS powered only.

(1) I = input, O = output, I/O = input and output, GPIO = general purpose digital input and output

**Table 5-2. TPS25751A S Pin Functions**

PIN		TYPE <sup>(1)</sup>	RESET	DESCRIPTION
NAME	NO.			
ADCIN1	2	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
ADCIN2	3	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CC1	24	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (C <sub>CC</sub> ).
CC2	25	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (C <sub>CC</sub> ).
GATE_VSYS	20	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to VSYS
GATE_VBUS	21	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to VBUS
GND	11, 12, 14	—	—	Ground. Connect to ground plane.
GPIO0/LD1	5	GPIO	Hi-Z	General purpose digital I/O. Pin can be connected for liquid detection on Type-C connector. Tie to ground when pin is unused.
GPIO1	6	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when pin is unused.
GPIO2/LD2	7	GPIO	Hi-Z	General purpose digital I/O. Pin can be connected for liquid detection on Type-C connector. Tie to ground when pin is unused.
GPIO3	18	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when pin is unused.
GPIO4/USB_P	22	GPIO	Hi-Z	General purpose digital I/O. Pin can be connected to D+ for BC1.2 support. Tie to ground when pin is unused.
GPIO5/USB_N	23	GPIO	Hi-Z	General purpose digital I/O. Pin can be connected to D- for BC1.2 support. Tie to ground when pin is unused.
GPIO6	31	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when pin is unused.
GPIO7	30	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when pin is unused.
I2Ct_SCL	9	I	Hi-Z	I2C target serial clock input. Tie to pullup voltage through a resistor. Tie to ground if unused.
I2Ct_SDA	8	I/O	Hi-Z	I2C target serial data. Open-drain input/output. Tie to pullup voltage through a resistor. Tie to ground if unused.
I2Ct_IRQ	10	O	Hi-Z	I2C target interrupt. Active low. Connect to external voltage through a pull-up resistor. Pin can be re-configured to GPIO10. Tie to ground when unused.
I2Cc_SCL	16	O	Hi-Z	I2C controller serial clock. Open-drain output. Tie to pullup voltage through a resistor.
GPIO11	13	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when pin is unused.
I2Cc_SDA	15	I/O	Hi-Z	I2C controller serial data. Open-drain input/output. Tie to pullup voltage through a resistor.
I2Cc_IRQ	17	I	Hi-Z	I2C controller interrupt. Active low. Connect to external voltage through a pull-up resistor. Pin can be re-configured to GPIO12.
LDO_1V5	4	O	—	Output of the CORE LDO. Bypass with capacitance C <sub>LDO_1V5</sub> to GND. This pin cannot source current to external circuits.
LDO_3V3	1	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance C <sub>LDO_3V3</sub> to GND.
PP5V	28, 29	I	—	5V system supply to VBUS, supply for CC <sub>y</sub> pins as VCONN.
VSYS	19	I	—	System side high voltage sensing node. High-voltage sinking node in the system. Used to implement reverse current protection (RCP) for the external sink path controlled by GATE_VSYS.
VBUS	26, 27	I/O	—	5V to 20V input. Bypass with capacitance C <sub>VBUS</sub> to GND.
VIN_3V3	32	I	—	Supply for core circuitry and I/O. Bypass with capacitance C <sub>VIN_3V3</sub> to GND. Tie to GND if device is VBUS powered only.

(1) I = input, O = output, I/O = input and output, GPIO = general purpose digital input and output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

#### 6.1.1 TPS25751AD and TPS25751AS - Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>1</sup>

PARAMETER		MIN	MAX	UNIT
Input voltage range <sup>2</sup>	VIN_3V3	-0.3	4	V
	PP5V	-0.3	6	V
	ADCINx	-0.3	4	V
	VBUS_IN, VBUS <sup>4</sup>	-0.3	28	V
	CC1, CC2 <sup>4</sup>	-0.5	26	V
	GPIOx	-0.3	6	V
	I2Ct_SCL, I2Ct_SDA	-0.3	4	V
Output voltage range <sup>2</sup>	LDO_1V5 <sup>3</sup>	-0.3	2	V
	LDO_3V3 <sup>3</sup>	-0.3	4	
Source current	Source or Sink current VBUS	internally limited		A
	Positive source current for LDO_3V3, LDO_1V5	internally limited		
Source current	GPIOx	0.005		A
T <sub>J</sub> Operating junction temperature		-40	175	°C
T <sub>STG</sub> Storage temperature		-55	150	°C

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent damage to the device. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
- (3) Do not apply voltage to these pins.
- (4) A TVS with a break down voltage falling between the Recommended max and the Abs max value is recommended such as TVS2200.

#### 6.1.2 TPS25751AD - Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNIT
Input voltage range <sup>1</sup>	PPHV	-0.3	28	V
V <sub>PPHV_VBUS_IN</sub>	Source-to-source voltage	28		V
Sink current	Continuous current to/from VBUS_IN to PPHV	7		A
	Pulsed current to/from VBUS_IN to PPHV <sup>2</sup>	10		
T <sub>J_PPHV</sub> Operating junction temperature	PP_HV switch	-40	175	°C

- (1) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
- (2) Pulse duration ≤ 100 μs and duty-cycle ≤ 1%.

#### 6.1.3 TPS25751AS - Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNIT
Output voltage range <sup>1</sup>	GATE_VBUS, GATE_VSYS <sup>2</sup>	-0.3	40	V
V <sub>GS</sub>	V <sub>GATE_VBUS</sub> - V <sub>VBUS</sub> , V <sub>GATE_SYS</sub> - V <sub>VSYS</sub>	-0.5	12	V

- (1) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
- (2) Do not apply voltage to these pins.

## 6.2 ESD Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup>	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 6.3.1 TPS25751AD - Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER			MIN	MAX	UNIT
V <sub>I</sub>	Input voltage range <sup>(1)</sup>	VIN_3V3	3.0	3.6	V
		PP5V	4.9	5.5	V
		ADCIN1, ADCIN2, VBUS_IN, VBUS	4	22	V
		PPHV	0	22	V
V <sub>IO</sub>	I/O voltage range <sup>(1)</sup>	I2Cx_SDA, I2Cx_SCL, I2Cx_IRQ, ADCIN1, ADCIN2	0	3.6	V
		GPIOx	0	5.5	
		CC1, CC2	0	5.5	
I <sub>PP_HV</sub>	Current from VBUS_IN to PPHV			7	A
I <sub>O</sub>	Output current (from LDO_3V3)	GPIOx		1	mA
I <sub>O</sub>	Output current (from VBUS LDO)	Sum of current from LDO_3V3 and GPIOx		5	mA
T <sub>A</sub>	Ambient operating temperature	I <sub>PP_5V</sub> = 0, I <sub>PP_HV</sub> ≤ 7A, I <sub>PP_CABLE</sub> = 0	-40	45	°C
		I <sub>PP_5V</sub> = 0, I <sub>PP_HV</sub> ≤ 6A, I <sub>PP_CABLE</sub> = 0	-40	65	
T <sub>J_PPHV</sub>	Operating junction temperature	PP_HV switch	-40	150	°C
T <sub>J</sub>	Operating junction temperature		-40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

### 6.3.2 TPS25751AS - Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER			MIN	MAX	UNIT
V <sub>I</sub>	Input voltage range <sup>(1)</sup>	VIN_3V3	3.0	3.6	V
V <sub>I</sub>	Input voltage range <sup>(1)</sup>	PP5V	4.9	5.5	V
V <sub>I</sub>	Input voltage range <sup>(1)</sup>	VBUS <sup>2</sup>	4	22	V
V <sub>I</sub>	Input voltage range <sup>(1)</sup>	VSYS	0	22	V
V <sub>IO</sub>	I/O voltage range <sup>(1)</sup>	I2Cx_SDA, I2Cx_SCL, I2Cx_IRQ ADCINx	0	3.6	V
		GPIOx	0	5.5	
		CC1, CC2	0	5.5	
I <sub>O</sub>	Output current (from PP5V)	VBUS		3	A
		CC1, CC2		315	mA
I <sub>O</sub>	Output current (from LDO_3V3)	GPIOx		1	mA
I <sub>O</sub>	Output current (from VBUS LDO)	Sum of current from LDO_3V3 and GPIOx		5	mA
T <sub>J</sub>	Operating junction temperature		-40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

(2) Short all VBUS and VBUS\_IN pins together.

### 6.4 Recommended Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER <sup>(1)</sup>		VOLTAGE RATING	MIN	NOM	MAX	UNIT
C <sub>VIN_3V3</sub>	Capacitance on VIN_3V3	6.3V	5	10		μF
C <sub>LDO_3V3</sub>	Capacitance on LDO_3V3	6.3V	5	10	25	μF
C <sub>LDO_1V5</sub>	Capacitance on LDO_1V5	4V	4.5		12	μF
C <sub>VBUS</sub>	Capacitance on VBUS <sup>(4)</sup>	25V	1	4.7	10	μF
C <sub>PP5V</sub>	Capacitance on PP5V	10V	120 <sup>(2)</sup>			μF
C <sub>VSYS</sub> TPS25751A	Capacitance on VSYS Sink from VBUS <sup>(5)</sup>	25V		47	100	μF
C <sub>PPHV</sub> TPS25751AD	Capacitance on PPHV Sink from VBUS <sup>(5)</sup>	25V		47	100	μF
C <sub>CCy</sub>	Capacitance on CCy pins <sup>(3)</sup>	6.3V	200	400	480	pF

(1) Capacitance values do not include any derating factors. For example, if 5μF is required and the external capacitor value reduces by 50% at the required operating voltage, then the required external capacitor value is 10μF.

(2) Minimum capacitance is a requirement from USB PD (cSrcBulkShared). Keep at least 120μF tied directly to PP5V.

(3) Capacitance includes all external capacitance to the Type-C receptacle.

(4) The device can be configured to quickly disable the sinking power path upon certain events. When such a configuration is used, a capacitance on the higher side of this range is recommended.

(5) USB PD specification for cSnkBulkPd (100μF) is the maximum bulk capacitance allowed on a VBUS sink after a PD contract is in place. The capacitance is sufficient for all power conversion devices deriving power from the PD Controller sink path. For systems requiring greater than 100μF, VBUS surge current limiting is implemented as described in the USB3.2 specification.

### 6.5.1 TPS25751AD - Thermal Information

THERMAL METRIC <sup>1</sup>		TPS25751AD	UNIT
		QFN (REF)	
		38 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance (sinking through PP_HV)	57.4	°C/W

### 6.5.1 TPS25751AD - Thermal Information (continued)

THERMAL METRIC <sup>1</sup>		TPS25751AD		
		QFN (REF)		UNIT
		38 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance (sourcing through PP_5V)	46.5	°C/W	
R <sub>θJC</sub> (top)	Junction-to-case (top) thermal resistance (sinking through PP_HV)	30.5	°C/W	
R <sub>θJC</sub> (top)	Junction-to-case (top) thermal resistance (sourcing through PP_5V)	20.3	°C/W	
R <sub>θJB</sub>	Junction-to-board thermal resistance (sinking through PP_HV)	21.1	°C/W	
R <sub>θJB</sub>	Junction-to-board thermal resistance (sourcing through PP_5V)	11.1	°C/W	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter (sinking through PP_HV)	18.2	°C/W	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter (sourcing through PP_5V)	1.0	°C/W	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter (sinking through PP_HV)	21.1	°C/W	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter (sourcing through PP_5V)	11.1	°C/W	
R <sub>θJC</sub> (bot_GND)	Junction-to-board (bottom GND pad) thermal resistance	1.8	°C/W	
R <sub>θJC</sub> (bot_DRAIN)	Junction-to-board (bottom DRAIN pad) thermal resistance	4.6	°C/W	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 6.5.2 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS25751AS		
		QFN (RSM)		UNIT
		32 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	30.5	°C/W	
R <sub>θJC</sub> (top)	Junction-to-case (top) thermal resistance	24.5	°C/W	
R <sub>θJC</sub>	Junction-to-board (bottom) thermal resistance	2	°C/W	
R <sub>θJB</sub>	Junction-to-board thermal resistance	9.8	°C/W	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2	°C/W	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	9.7	°C/W	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Power Supply Characteristics

Operating under these conditions unless otherwise noted:  $3.0V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VIN_3V3, VBUS</b>						
V <sub>VBUS_UVLO</sub>	VBUS UVLO threshold	rising	3.6		3.9	V
		falling	3.5		3.8	
		hysteresis		0.1		

## 6.6 Power Supply Characteristics (continued)

Operating under these conditions unless otherwise noted:  $3.0V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VIN3V3\_UVLO}$	Voltage required on VIN_3V3 for power on	rising, $V_{VBUS} = 0$	2.56	2.66	2.76	V
		falling, $V_{VBUS} = 0$	2.44	2.54	2.64	
		hysteresis		0.12		
<b>LDO_3V3, LDO_1V5</b>						
$V_{LDO\_3V3}$	Voltage on LDO_3V3	$V_{VIN\_3V3} = 0V, 10\mu A \leq I_{LOAD} \leq 18mA, V_{VBUS} \geq 3.9V$	3.0	3.4	3.6	V
$R_{LDO\_3V3}$	Rdson of VIN_3V3 to LDO_3V3	$I_{LDO\_3V3} = 50mA$			1.4	$\Omega$
$V_{LDO\_1V5}$	Voltage on LDO_1V5	up to maximum internal loading condition	1.49	1.5	1.65	V

## 6.7 Power Consumption

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$ , no GPIO loading

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VIN\_3V3,ActSrc}$	Current into VIN_3V3	Active Source mode: $V_{VBUS} = 5V, V_{VIN\_3V3} = 3.3V$		3		mA
$I_{VIN\_3V3,ActSnk}$	Current into VIN_3V3	Active PPHV mode: $22V \geq V_{VBUS} \geq 4V, V_{VIN\_3V3} = 3.3V$		3	6	mA
$I_{VIN\_3V3,IdlSrc}$	Current into VIN_3V3	Idle Source mode: $V_{VBUS} = 5V, V_{VIN\_3V3} = 3.3V$		1.0		mA
$I_{VIN\_3V3,IdlSnk}$	Current into VIN_3V3	Idle PPHV mode: $22V \geq V_{VBUS} \geq 4V, V_{VIN\_3V3} = 3.3V$		1.0		mA
$I_{PP5V,Sleep}$	Current into PP5V	Sleep mode: $V_{PA\_VBUS} = 0V, V_{VIN\_3V3} = 3.3V$		2		$\mu A$
$I_{VIN\_3V3,Sleep}$	Current into VIN_3V3	Sleep DRP mode: $V_{VBUS} = 0V, V_{VIN\_3V3} = 3.3V$		56		$\mu A$

## 6.8 PP\_5V Power Switch Characteristics

Operating under these conditions unless otherwise noted:  $3.0V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{PP\_5V}$	Resistance from PP5V to VBUS	$I_{LOAD} = 3A, T_J = 25^\circ C$		36	38	m $\Omega$
$R_{PP\_5V}$	Resistance from PP5V to VBUS	$I_{LOAD} = 3A, T_J = 125^\circ C$		36	53	m $\Omega$
$I_{PP5V\_REV}$	VBUS to PP5V leakage current	$V_{PP5V} = 0V, V_{VBUS} = 5.5V, PP\_5V$ disabled, $T_J \leq 85^\circ C$ , measure $I_{PP5V}$			5	$\mu A$
$I_{PP5V\_FWD}$	PP5V to VBUS leakage current	$V_{PP5V} = 5.5V, V_{VBUS} = 0V, PP\_5V$ disabled, $T_J \leq 85^\circ C$ , measure $I_{VBUS}$			15	$\mu A$
$I_{LIM5V}$	Current limit setting	Configure to setting 0	1.15		1.36	A
$I_{LIM5V}$	Current limit setting	Configure to setting 1	1.61		1.90	A
$I_{LIM5V}$	Current limit setting	Configure to setting 2	2.3		2.70	A
$I_{LIM5V}$	Current limit setting	Configure to setting 3	3.04		3.58	A
$I_{LIM5V}$	Current limit setting	Configure to setting 4	3.22		3.78	A
$I_{VBUS}$	PP5V to VBUS current sense accuracy	$3.64A \geq I_{VBUS} \geq 1A$	3.05	3.5	3.75	A/V
$V_{PP\_5V\_RCP}$	RCP clears and PP_5V starts turning on when $V_{VBUS} - V_{PP5V} < V_{PP\_5V\_RCP}$ . Measure $V_{VBUS} - V_{PP5V}$		10		20	mV
$t_{IOS\_PP\_5V}$	Response time to VBUS short circuit	VBUS to GND through 10m $\Omega$ , $C_{VBUS} = 0$		1.15		$\mu s$

## 6.8 PP\_5V Power Switch Characteristics (continued)

Operating under these conditions unless otherwise noted:  $3.0V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PP\_5V\_ovp}$	Response time to $V_{VBUS} > V_{OVP4RCP}$	Enable PP_5V, $I_{RpDef}$ being drawn from PP5V, configure $V_{OVP4RCP}$ to setting 2, ramp $V_{VBUS}$ from 4V to 20V at 100V/ms, $C_{PP5V} = 2.5 \mu F$ , measure time from OVP detection until reverse current < 100mA		4.5		$\mu s$
$t_{PP\_5V\_uvlo}$	Response time to $V_{PP5V} < V_{PP5V\_UVLO}$ , PP_VBUS is deemed off when $V_{VBUS} < 0.8V$	$R_L = 100\Omega$ , no external capacitance on VBUS		4		$\mu s$
$t_{PP\_5V\_rcp}$	Response time to $V_{PP5V} < V_{VBUS} + V_{PP\_5V\_RCP}$	$V_{PP5V} = 5.5V$ , $I_{RpDef}$ being drawn from PP5V, enable PP_5V, configure $V_{OVP4RCP}$ to setting 2, ramp $V_{VBUS}$ from 4V to 21.5V at 10 V/ $\mu s$ , measure $V_{PP5V}$ . $C_{PP5V} = 104\mu F$ , $C_{VBUS} = 10\mu F$ , measure time from RCP detection until reverse current < 100mA		0.7		$\mu s$
$t_{LIM}$	Current clamping deglitch time			5.1		ms
$t_{ON}$	From enable signal to VBUS at 90% of final value	$R_L = 100\Omega$ , $V_{PP5V} = 5V$ , $C_L = 0$	2.3	3.3	4.3	ms
$t_{OFF}$	From disable signal to VBUS at 10% of final value	$R_L = 100\Omega$ , $V_{PP5V} = 5V$ , $C_L = 0$	0.30	0.45	0.6	ms
$t_{RISE}$	VBUS from 10% to 90% of final value	$R_L = 100\Omega$ , $V_{PP5V} = 5V$ , $C_L = 0$	1.2	1.7	2.2	ms
$t_{FALL}$	VBUS from 90% to 10% of initial value	$R_L = 100\Omega$ , $V_{PP5V} = 5V$ , $C_L = 0$	0.06	0.1	0.14	ms

## 6.9 PPHV Power Switch Characteristics - TPS25751AD

Operating under these conditions unless otherwise noted:  $3.0V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{PPHV}$	Resistance from VBUS_IN to PPHV power switch resistance	$T_J PPHV = 25^\circ C$ , $I_{PPHV} = 6.5A$		16	19	$m\Omega$
		$T_J PPHV = 125^\circ C$ , $I_{PPHV} = 6.5A$		24	29	
		$T_J PPHV = 150^\circ C$ , $I_{PPHV} = 6.5A$		27	32	$m\Omega$
$V_{RCP}$	Comparator mode RCP threshold, $V_{PPHV} - V_{VBUS}$	Setting 0, $4V \leq V_{VBUS} \leq 22V$ , $V_{VIN\_3V3} \leq 3.63V$	2	6	10	mV
$V_{RCP}$	Comparator mode RCP threshold, $V_{PPHV} - V_{VBUS}$	setting 1, $4V \leq V_{VBUS} \leq 22V$ , $V_{VIN\_3V3} \leq 3.63V$	4	8	12	mV
$V_{RCP}$	Comparator mode RCP threshold, $V_{PPHV} - V_{VBUS}$	Setting 2, $4V \leq V_{VBUS} \leq 22V$ , $V_{VIN\_3V3} \leq 3.63V$	6	10	14	mV
$V_{RCP}$	Comparator mode RCP threshold, $V_{PPHV} - V_{VBUS}$	Setting 3, $4V \leq V_{VBUS} \leq 22V$ , $V_{VIN\_3V3} \leq 3.63V$	8	12	16	mV
SS	Soft start slew rate for GATE_VSYS, setting 0	$4V \leq V_{VBUS} \leq 22V$ , $I_{LOAD} = 100mA$ , 500pF < $C_{GATE\_VSYS}$ < 16nF, measure slope from 10% to 90% of final VSYS value	0.35	0.41	0.47	V/ms

## 6.9 PPHV Power Switch Characteristics - TPS25751AD (continued)

Operating under these conditions unless otherwise noted:  $3.0V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SS	Soft start slew rate for GATE_VSYS, setting 1	$4V \leq V_{VBUS} \leq 22V$ , $I_{LOAD} = 100mA$ , $500pF < C_{GATE\_VSYS} < 16nF$ , measure slope from 10% to 90% of final VSYS value	0.67	0.81	0.95	V/ms
SS	Soft start slew rate for GATE_VSYS, setting 2	$4V \leq V_{VBUS} \leq 22V$ , $I_{LOAD} = 100mA$ , $500pF < C_{GATE\_VSYS} < 16nF$ , measure slope from 10% to 90% of final VSYS value	1.33	1.7	2.0	V/ms
SS	Soft start slew rate for GATE_VSYS, setting 3	$4V \leq V_{VBUS} \leq 22V$ , $I_{LOAD} = 100mA$ , $500pF < C_{GATE\_VSYS} < 16nF$ , measure slope from 10% to 90% of final VSYS value	2.8	3.3	3.80	V/ms
$t_{PPHV\_OFF}$	Time allowed to disable the internal PPHV switch in normal shutdown mode	$V_{VBUS} = 20V$ , $V_{PPHV} = 20V$ (initially), $C_{PPHV} < 1nF$ , $I_{PPHV} = 0.1A$ , switch is off when $V_{VBUS\_IN} - V_{PPHV} > 1V$		400	1000	$\mu s$
$t_{PPHV\_OVP}$	Time allowed to disable the internal PPHV switch in fast shutdown mode ( $V_{OVP4RCP}$ exceeded), this includes the response time of the comparator	OVP: $V_{OVP4RCP} =$ setting 57, $V_{VBUS} = 20V$ initially, then raised to 23V in 50ns, $V_{PPHV} = V_{VBUS\_IN}$ (initially), $C_{PPHV} < 1nF$ , $I_{PPHV} = 0.1A$ , switch is off when $V_{VBUS\_IN} - V_{PPHV} > 0.1V$		2	4	$\mu s$
$t_{PPHV\_RCP}$	Time allowed to disable the internal PPHV switch in fast shutdown mode ( $V_{RCP}$ exceeded), this includes the response time of the comparator	RCP: $V_{RCP} =$ setting 0, $V_{VBUS} = 5V$ , $V_{VSYS} = 5V$ initially, then raised to 6V with $dV/dt = 0.1V/\mu s$ , $C_{VBUS} = 10\mu F$ , measure time from $V_{VSYS} > V_{BUS} + V_{RCP}$ to the time of peak voltage on VBUS		1	2	$\mu s$
$t_{PPHV\_FSD}$	Time allowed to disable the internal PPHV switch in fast shutdown mode (OVP)	$V_{PPHV} = 20V$ (initially), $V_{VBUS} = 20V$ then raised to 23V in 50ns, $r_{OVP} = 1$ , $C_{PPHV} < 1nF$ , $I_{PPHV} = 0.1A$ , switch is off when $V_{VBUS\_IN} - V_{PPHV} > 0.5V$		0.25	20	$\mu s$
$t_{PPHV\_ON}$	Time to enable the internal PPHV switch	$V_{VBUS\_IN} = 5V$ , $C_{PPHV} = 0$ , $I_{PPHV} = 0$ , measure time from register write to enable PPHV until $V_{VBUS\_IN} - V_{PPHV} < 0.1V$ , soft start setting 3	1500	1800	2100	$\mu s$

## 6.10 PP\_EXT Characteristics - TPS25751AS

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{GATE\_ON}$	Gate driver sourcing current	$0V \leq V_{GATE\_VSYS} - V_{VSYS} \leq 6V$ , $V_{VSYS} \leq 22V$ , $V_{VBUS} > 4V$ , measure $I_{GATE\_VSYS}$	8.5		11.5	$\mu A$
		$0V \leq V_{GATE\_VBUS} - V_{VBUS} \leq 6V$ , $4V \leq V_{VBUS} \leq 22V$ , measure $I_{GATE\_VBUS}$	8.5		11.5	$\mu A$

## 6.10 PP\_EXT Characteristics - TPS25751AS (continued)

Operating under these conditions unless otherwise noted: ,  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>GATE_ON</sub>	Sourcing voltage (ON)	0V ≤ V <sub>VSYS</sub> ≤ 22V, I <sub>GATE_VSYS</sub> < 4μA, measure V <sub>GATE_VSYS</sub> – V <sub>VSYS</sub> , V <sub>VBUS</sub> > 4V	6		12	V
		4V ≤ V <sub>VBUS</sub> ≤ 22V, I <sub>GATE_VBUS</sub> < 4μA, measure V <sub>GATE_VBUS</sub> – V <sub>VBUS</sub>	6		12	V
V <sub>RCP</sub>	Comparator mode RCP threshold, V <sub>VSYS</sub> - V <sub>VBUS</sub>	4V ≤ V <sub>VBUS</sub> ≤ 22V, V <sub>VIN_3V3</sub> ≤ 3.63V	2	6	10	mV
I <sub>GATE_OFF</sub>	Sinking strength	Normal turnoff: V <sub>VSYS</sub> = 5V, V <sub>GATE_VSYS</sub> = 6V, measure I <sub>GATE_VSYS</sub>	13			μA
		Normal turnoff: V <sub>VBUS</sub> = V <sub>VSYS</sub> = 5V, V <sub>GATE_VBUS</sub> = 6V, measure I <sub>GATE_VBUS</sub>	13			μA
R <sub>GATE_FSD</sub>	Sinking strength	Fast turnoff: V <sub>VSYS</sub> = 5V, V <sub>GATE_VSYS</sub> = 6V, assert PPHV1_FAST_DISABLE, measure R <sub>GATE_VSYS</sub>			85	Ω
		Fast turnoff: V <sub>VBUS</sub> = V <sub>VSYS</sub> = 5V, V <sub>GATE_VBUS</sub> = 6V, assert PPHV1_FAST_DISABLE, measure R <sub>GATE_VBUS</sub>			85	Ω
R <sub>GATE_OFF_UVLO</sub>	Sinking strength in UVLO (safety)	V <sub>VIN_3V3</sub> = 0V, V <sub>VBUS</sub> = 3V, V <sub>GATE_VSYS</sub> = 0.1V, measure resistance from GATE_VSYS to GND			1.5	MΩ
SS	Soft start slew rate for GATE_VSYS	4V ≤ V <sub>VBUS</sub> ≤ 22V, I <sub>LOAD</sub> = 100mA, 500pF < C <sub>GATE_VSYS</sub> < 16nF, measure slope from 10% to 90% of final V <sub>VSYS</sub> value	2.8	3.3	3.80	V/ms
t <sub>GATE_VBUS_OFF</sub>	Time allowed to disable the external FET via GATE_VBUS in normal shutdown mode. <sup>(1)</sup>	V <sub>VBUS</sub> = 20V, Q <sub>G</sub> of external FET = 40nC or C <sub>GATE_VBUS</sub> < 3nF, gate is off when V <sub>GATE_VBUS</sub> – V <sub>VBUS</sub> < 1V		450	4000	μs
t <sub>GATE_VBUS_OVP</sub>	Time allowed to disable the external FET via GATE_VBUS in fast shutdown mode (V <sub>OVP4RCP</sub> exceeded), this includes the response time of the comparator <sup>(1)</sup>	OVP: V <sub>OVP4RCP</sub> = setting 57, V <sub>VBUS</sub> = 20V initially, then raised to 23V in 50ns, Q <sub>G</sub> of external FET = 40nC or C <sub>GATE_VBUS</sub> < 3nF, gate is off when V <sub>GATE_VBUS</sub> – V <sub>VBUS</sub> < 1V		3	5	μs
t <sub>GATE_VBUS_RCP</sub>	Time allowed to disable the external FET via GATE_VBUS in fast shutdown mode (V <sub>RCP</sub> exceeded), this includes the response time of the comparator <sup>(1)</sup>	RCP: V <sub>RCP</sub> = setting 0, V <sub>VBUS</sub> = 5V, V <sub>VSYS</sub> = 5V initially, then raised to 5.5V in 50ns, Q <sub>G</sub> of external FET = 40 nC or C <sub>GATE_VBUS</sub> < 3nF, gate is off when V <sub>GATE_VBUS</sub> – V <sub>VBUS</sub> < 1V		1	2	μs
t <sub>GATE_VSYS_OFF</sub>	Time allowed to disable the external FET via GATE_VSYS in normal shutdown mode <sup>(1)</sup>	V <sub>VSYS</sub> = 20V, Q <sub>G</sub> of external FET = 40nC or C <sub>GATE_VBUS</sub> < 3nF, gate is off when V <sub>GATE_VSYS</sub> – V <sub>VSYS</sub> < 1V		450	4000	μs

## 6.10 PP\_EXT Characteristics - TPS25751AS (continued)

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{GATE\_VSY\_FSD}$	Time allowed to disable the external FET via GATE_VSYS in fast shutdown mode (OVP) <sup>(1)</sup>	$V_{VBUS} = 20V$ initially, then raised to 23V in 50ns, $Q_G$ of external FET = 40 nC or $C_{GATE\_VBUS} < 3nF$ , gate is off when $V_{GATE\_VSY} - V_{VSY} < 1V$ , $r_{OVP} = 1$		0.25	20	$\mu s$
$t_{GATE\_VBUS\_ON}$	Time to enable GATE_VBUS <sup>(1)</sup>	Measure time from when $V_{GS} = 0V$ until $V_{GS} > 3V$ , where $V_{GS} = V_{GATE\_VBUS} - V_{VBUS}$		0.25	2	ms

(1) These values depend upon the characteristics of the external N-ch MOSFET. The typical values measured are when Px\_GATE\_VSYS and Px\_GATE\_VBUS are used to drive two CSD17571Q2 in common drain back-to-back configuration.

## 6.11 Power Path Supervisory

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PP5V\_UVLO}$	Voltage required on PP5V	rising	3.9	4.1	4.3	V
		falling	3.8	4.0	4.2	
		hysteresis		0.1		
$V_{OVP4RCP}$	VBUS overvoltage protection for RCP programmable range	OVP detected when $V_{VBUS} > V_{OVP4RCP}$	5.0		24	V
$V_{OVP4RCPH}$	Hysteresis		1.75	2	2.25	%
$r_{OVP}$	Ratio of OVP4RCP input used for OVP4VSY comparator. $r_{OVP} \times V_{OVP4VSY} = V_{OVP4RCP}$	Setting 0		1		V/V
		Setting 1		0.95		
		Setting 2		0.9		
		Setting 3		0.875		
$V_{OVP4VSY}$	VBUS overvoltage protection range for VSY protection	OVP detected when $r_{OVP} \times V_{VBUS} > V_{OVP4RCP}$	5		27.5	V
$V_{OVP4VSY}$	Hysteresis	VBUS falling, % of $V_{OVP4VSY}$ , $r_{OVP}$ setting 0	1.75	2	2.25	%
		VBUS falling, % of $V_{OVP4VSY}$ , $r_{OVP}$ setting 1	1.8	2.1	2.4	
		VBUS falling, % of $V_{OVP4VSY}$ , $r_{OVP}$ setting 2	1.9	2.2	2.5	
		VBUS falling, % of $V_{OVP4VSY}$ , $r_{OVP}$ setting 3	2	2.3	2.6	
$I_{DSCH}$	VBUS discharge current	$V_{VBUS} = 22V$ , measure $I_{VBUS}$	4		15	mA

## 6.12 CC Cable Detection Parameters

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Type-C Source (Rp pullup)</b>						
$V_{OC\_3.3}$	Unattached CCy open circuit voltage while Rp enabled, no load	$V_{LDO\_3V3} > 2.302V$ , $R_{CC} = 47k\Omega$	1.85			V
$V_{OC\_5}$	Attached CCy open circuit voltage while Rp enabled, no load	$V_{PP5V} > 3.802V$ , $R_{CC} = 47k\Omega$	2.95			V

## 6.12 CC Cable Detection Parameters (continued)

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Rev}$	Unattached reverse current on CCy	$V_{CCy} = 5.5V, V_{CCx} = 0V,$ $V_{LDO\_3V3\_UVLO} < V_{LDO\_3V3} < 3.6V,$ $V_{PP5V} = 3.8V,$ measure current into CCy			10	$\mu A$
		$V_{CCy} = 5.5V, V_{CCx} = 0V,$ $V_{LDO\_3V3\_UVLO} < V_{LDO\_3V3} < 3.6V,$ $V_{PP5V} = 0V, T_J \leq 85^\circ C,$ measure current into CCy			10	
$I_{RpDef}$	Current source - USB Default	$0 < V_{CCy} < 1V,$ measure $I_{CCy}$	64	80	96	$\mu A$
$I_{Rp1.5}$	Current source - 1.5A	$4.75V < V_{PP5V} < 5.5V, 0V < V_{CCy} < 1.5V,$ measure $I_{CCy}$	166	180	194	$\mu A$
$I_{Rp3.0}$	Current source - 3.0A	$4.75V < V_{PP5V} < 5.5V, 0 < V_{CCy} < 2.45V,$ measure $I_{CCy}$	304	330	356	$\mu A$
<b>Type-C Sink (Rd pulldown)</b>						
$V_{SNK1}$	Open/Default detection threshold when Rd applied to CCy	rising	0.2		0.24	V
	Open/Default detection threshold when Rd applied to CCy	falling	0.16		0.20	V
	Hysteresis			0.04		V
$V_{SNK2}$	Default/1.5A detection threshold	falling	0.62		0.68	V
	Default/1.5A detection threshold	rising	0.63	0.66	0.69	V
	Hysteresis			0.01		V
$V_{SNK3}$	1.5A/3.0A detection threshold when Rd applied to CCy	falling	1.17		1.25	V
	1.5A/3.0A detection threshold when Rd applied to CCy	rising	1.22		1.3	V
	Hysteresis			0.05		V
$R_{SNK}$	Rd pulldown resistance	$0.25V \leq V_{CCy} \leq 2.1V,$ measure resistance on CCy, after trimming using trim_cd_rd, $V_{LDO\_3V3\_UVLO} < V_{LDO\_3V3} < 3.6V,$	4.6		5.6	k $\Omega$
$R_{VCONN\_DIS}$	VCONN discharge resistance	$0V \leq V_{CCy} \leq 5.5V,$ measure resistance on CCy, after trimming using trim_cd_rd	4.0		6.12	k $\Omega$
$V_{CLAMP}$	Dead battery Rd clamp	$V_{VIN\_3V3} = 0V, 64\mu A < I_{CCy} < 96\mu A$	0.25		1.32	V
		$V_{VIN\_3V3} = 0V, 166\mu A < I_{CCy} < 194\mu A$	0.65		1.32	
		$V_{VIN\_3V3} = 0V, 304\mu A < I_{CCy} < 356\mu A$	1.20		2.18	
$R_{Open}$	Resistance from CCy to GND when configured as open	$V_{VBUS} = 0V, V_{VIN\_3V3} = 3.3V, V_{CCy} = 5V,$ measure resistance on CCy	500			k $\Omega$
		$V_{VBUS} = 5V, V_{VIN\_3V3} = 0V, V_{CCy} = 5V,$ measure resistance on CCy	500			k $\Omega$
<b>Common Comparator</b>						
$t_{CC}$	deglitch time for comparators on Px_CCy			3.2		ms

### 6.13 CC VCONN Parameters

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{PP\_CABLE}$	Rdson of the VCONN path	$V_{PP5V} = 5V, I_L = 250mA$ , measure resistance from PP5V to CCy			1.2	$\Omega$
$I_{LIMVC}$	Short circuit current limit	Setting 0, $V_{PP5V} = 5V$ , $R_L = 10m\Omega$ , measure $I_{CCy}$	350	410	470	mA
$I_{LIMVC}$	Short circuit current limit	Setting 1, $V_{PP5V} = 5V$ , $R_L = 10m\Omega$ , measure $I_{CCy}$	540	600	660	mA
$I_{CC2PP5V}$	Reverse leakage current through VCONN FET	VCONN disabled, $T_J \leq 85^\circ C$ , $V_{CCy} = 5.5V$ , $V_{PP5V} = 0V$ , $V_{VBUS} = 5V$ , LDO forced to draw from VBUS, measure $I_{CCy}$			10	$\mu A$
$V_{VC\_OVP}$	Overvoltage protection threshold for PP_CABLE	$V_{PP5V}$ rising	5.6	5.9	6.2	V
$V_{VC\_RCP}$	Reverse current protection threshold for PP_CABLE, sourcing VCONN through CCx	$V_{PP5V} \geq 4.9V$ , $V_{CCy} = V_{PP5V}$ , $V_{CCx}$ rising	60	200	340	mV
		$V_{PP5V} \geq 4.9V$ , $V_{CCy} \leq 4V$ , $V_{CCx}$ rising	210	340	470	mV
$t_{VCILIM}$	Current clamp deglitch time			1.3		ms
$t_{PP\_CABLE\_FSD}$	Time to disable PP_CABLE after $V_{PP5V} > V_{VC\_OVP}$ or $V_{CCx} - V_{PP5V} > V_{VC\_RCP}$	$C_L = 0$		0.5		$\mu s$
$t_{PP\_CABLE\_off}$	From disable signal to CCy at 10% of final value	$I_L = 250mA$ , $V_{PP5V} = 5V$ , $C_L = 0$	100	200	300	$\mu s$
$t_{IOS\_PP\_CABLE}$	Response time to short circuit	$V_{PP5V} = 5V$ , for short circuit $R_L = 10m\Omega$		2		$\mu s$

### 6.14 CC PHY Parameters

Operating under these conditions unless otherwise noted: and (  $3V \leq V_{VIN\_3V3} \leq 3.6V$  or  $V_{VBUS} \geq 3.9V$  )

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Transmitter</b>						
$V_{TXHI}$	Transmit high voltage on CCy	Standard External load	1.05	1.125	1.2	V
$V_{TXLO}$	Transmit low voltage on CCy	Standard External load	-75		75	mV
$Z_{DRIVER}$	Transmit output impedance while driving the CC line using CCy	measured at 750kHz	33	54	75	$\Omega$
$t_{Rise}$	Rise time. 10% to 90% amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	$C_{CCy} = 520pF$	300			ns
$t_{Fall}$	Fall time. 90% to 10% amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	$C_{CCy} = 520pF$	300			ns
$V_{PHY\_OVP}$	OVP detection threshold for USB PD PHY	$0V \leq V_{VIN\_3V3} \leq 3.6V$ , $0V \leq V_{PP5V} \leq 5.5V$ , $V_{VBUS} \geq 4V$ . Initially $V_{CC1} \leq 5.5V$ and $V_{CC2} \leq 5.5V$ , then $V_{CCx}$ rises	5.5		8.5	V
<b>Receiver</b>						
$Z_{BMC RX}$	Receiver input impedance on CCy	Does not include pullup or pulldown resistance from cable detect. Transmitter is Hi-Z	1			M $\Omega$

## 6.14 CC PHY Parameters (continued)

Operating under these conditions unless otherwise noted: and ( $3V \leq V_{IN\_3V3} \leq 3.6V$  or  $V_{VBUS} \geq 3.9V$ )

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{CC}$	Receiver capacitance on CCy <sup>1</sup>	Capacitance looking into the CC pin when in receiver mode			120	pF
$V_{RX\_SNK\_R}$	Rising threshold on CCy for receiver comparator	Sink mode (rising)	499	525	551	mV
$V_{RX\_SRC\_R}$	Rising threshold on CCy for receiver comparator	Source mode (rising)	784	825	866	mV
$V_{RX\_SNK\_F}$	Falling threshold on CCy for receiver comparator	Sink mode (falling)	230	250	270	mV
$V_{RX\_SRC\_F}$	Falling threshold on CCy for receiver comparator	Source mode (falling)	523	550	578	mV

- (1)  $C_{CC}$  includes only the internal capacitance on a CCy pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications (cReceiver). Therefore, TI recommends adding  $C_{CCy}$  externally.

## 6.15 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{SD\_MAIN}$	Temperature shutdown threshold	Temperature rising	145	160	175	°C
		Hysteresis		15		°C
$T_{SD\_PP5V}$	Temperature controlled shutdown threshold. The power paths for each port sourcing from PP5V and PP_CABLE power paths have local sensors that disables them when the temperature is exceeded	Temperature rising	135	150	165	°C
		Hysteresis		10		°C

## 6.16 ADC Characteristics

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LSB	Least significant bit	3.6V max scaling, voltage divider of 3		14		mV
		25.2V max scaling, voltage divider of 21		98		mV
		4.07A max scaling		16.5		mA
GAIN_ERR	Gain error	$0.05V \leq V_{ADCINx} \leq 3.6V$ , $V_{ADCINx} \leq V_{LDO\_3V3}$	-2.7		2.7	%
		$0.05V \leq V_{GPIOx} \leq 3.6V$ , $V_{GPIOx} \leq V_{LDO\_3V3}$				
		$2.7V \leq V_{LDO\_3V3} \leq 3.6V$	-2.4	2.4		
		$0.6V \leq V_{VBUS} \leq 22V$	-2.1	2.1		
		$1A \leq I_{VBUS} \leq 3A$	-2.1	2.1		

## 6.16 ADC Characteristics (continued)

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOS_ERR	Offset error <sup>1</sup>	$0.05V \leq V_{ADCINx} \leq 3.6V, V_{ADCINx} \leq V_{LDO\_3V3}$	-4.1		4.1	mV
		$0.05V \leq V_{GPIOx} \leq 3.6V, V_{GPIOx} \leq V_{LDO\_3V3}$				
		$2.7V \leq V_{LDO\_3V3} \leq 3.6V$	-4.5		4.5	
		$0.6V \leq V_{VBUS} \leq 22V$	-4.1		4.1	
		$1A \leq I_{VBUS} \leq 3A$	-4.5		4.5	mA

(1) The offset error is specified after the voltage divider.

## 6.17 Input/Output (I/O) Characteristics

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>GPIO0-7 (Inputs)</b>						
GPIO_VIH	GPIOx high-level input voltage	$V_{LDO\_3V3} = 3.3V$	1.3			V
GPIO_VIL	GPIOx low-level input voltage	$V_{LDO\_3V3} = 3.3V$			0.54	V
GPIO_HYS	GPIOx input hysteresis voltage	$V_{LDO\_3V3} = 3.3V$	0.09			V
GPIO_ILKG	GPIOx leakage current	$V_{GPIOx} = 3.45V$	-1		1	$\mu A$
GPIO_RPU	GPIOx internal pullup	Pullup enabled	50	100	150	k $\Omega$
GPIO_RPD	GPIOx internal pulldown	Pulldown enabled	50	100	150	k $\Omega$
GPIO_DG	GPIOx input deglitch			20	50	ns
<b>GPIO0-7 (Outputs)</b>						
GPIO_VOH	GPIOx output high voltage	$V_{LDO\_3V3} = 3.3V, I_{GPIOx} = -2mA$	2.9			V
GPIO_VOL	GPIOx output low voltage	$V_{LDO\_3V3} = 3.3V, I_{GPIOx} = 2mA$			0.4	V
<b>ADCIN1, ADCIN2</b>						
ADCIN_ILKG	ADCINx leakage current	$V_{ADCINx} \leq V_{LDO\_3V3}$	-1		1	$\mu A$
t <sub>BOOT</sub>	Time from LDO_3V3 going high until ADCINx is read for configuration			10		ms

## 6.18 BC1.2 Characteristics

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Data Contact Detect</b>						
I <sub>DP_SRC</sub>	DCD source current	$V_{LDO\_3V3} = 3.3V$	7	10	13	$\mu A$
R <sub>DM_DWN</sub>	DCD pulldown resistance	$V_{USB\_N} = 3.6V$	14.25	20	24.8	k $\Omega$
R <sub>DP_DWN</sub>	DCD pulldown resistance	$V_{USB\_P} = 3.6V$	14.25	20	24.8	k $\Omega$
V <sub>LGC_HI</sub>	Threshold for no connection	$V_{USB\_P} \geq V_{LGC\_HI}, V_{LDO\_3V3} = 3.3V, R_{USB\_P} = 300k\Omega$	2		3.6	V
V <sub>LGC_LO</sub>	Threshold for connection	$V_{USB\_N} \leq V_{LGC\_LO}, V_{LDO\_3V3} = 3.3V, R_{USB\_P} = 24.8k\Omega$	0		0.8	V
<b>Advertisement and Detection</b>						
V <sub>DX_SRC</sub>	Source voltage	$C_{GPIO4} \leq 600pF$	0.55	0.6	0.65	V
V <sub>DX_ILIM</sub>	V <sub>DX_SRC</sub> current limit		250		400	$\mu A$
I <sub>DX_SNK</sub>	Sink Current	$V_{USB\_P} \geq 250mV$	25	75	125	$\mu A$
I <sub>DX_SNK</sub>	Sink Current	$V_{USB\_N} \geq 250mV$	25	75	125	$\mu A$

## 6.18 BC1.2 Characteristics (continued)

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R <sub>DCP_DAT</sub>	Dedicated Charging Port Resistance	$0.5V \leq V_{USB\_P} \leq 0.7V$ , $25\mu A \leq I_{USB\_N} \leq 175\mu A$			200	$\Omega$

## 6.19 I2C Requirements and Characteristics

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>I2Ct_IRQ</b>						
OD_VOL_IRQ	Low level output voltage	$I_{OL} = 2mA$			0.4	V
OD_LKG_IRQ	Leakage Current	Output is Hi-Z, $V_{I2Cx\_IRQ} = 3.45V$	-1		1	$\mu A$
<b>I2Cc_IRQ</b>						
IRQ_VIH	High-Level input voltage	$V_{LDO\_3V3} = 3.3V$	1.3			V
IRQ_VIH_THRESH	High-Level input voltage threshold	$V_{LDO\_3V3} = 3.3V$	0.72		1.3	V
IRQ_VIL	low-level input voltage	$V_{LDO\_3V3} = 3.3V$			0.54	V
IRQ_VIL_THRESH	low-level input voltage threshold	$V_{LDO\_3V3} = 3.3V$	0.54		1.08	V
IRQ_HYS	input hysteresis voltage	$V_{LDO\_3V3} = 3.3V$	0.09			V
IRQ_DEG	input deglitch			20		ns
IRQ_ILKG	I2Cc_IRQ leakage current	$V_{I2Cc\_IRQ} = 3.45V$	-1		1	$\mu A$
<b>SDA and SCL Common Characteristics (Common Characteristics)</b>						
V <sub>IL</sub>	Input low signal	$V_{LDO\_3V3} = 3.3V$			0.54	V
V <sub>IH</sub>	Input high signal	$V_{LDO\_3V3} = 3.3V$	1.3			V
V <sub>HYS</sub>	Input hysteresis	$V_{LDO\_3V3} = 3.3V$	0.165			V
V <sub>OL</sub>	Output low voltage	$I_{OL} = 3mA$			0.36	V
I <sub>LEAK</sub>	Input leakage current	Voltage on pin = $V_{LDO\_3V3}$	-3		3	$\mu A$
I <sub>OL</sub>	Max output low current	$V_{OL} = 0.4V$	15			mA
I <sub>OL</sub>	Max output low current	$V_{OL} = 0.6V$	20			mA
t <sub>f</sub>	Fall time from $0.7 \times V_{DD}$ to $0.3 \times V_{DD}$	$V_{DD} = 1.8V$ , $10pF \leq C_b \leq 400pF$ $V_{DD} = 3.3V$ , $10pF \leq C_b \leq 400pF$	12		80	ns
t <sub>SP</sub>	I <sup>2</sup> C pulse width suppressed				50	ns
C <sub>I</sub>	Pin capacitance (internal)				10	pF
C <sub>b</sub>	Capacitive load for each bus line (external)				400	pF
<b>SDA and SCL Standard Mode Characteristics (Target)</b>						
f <sub>SCLS</sub>	Clock frequency for target	$V_{DD} = 1.8V$ or $3.3V$			100	kHz
t <sub>VD;DAT</sub>	Valid data time	Transmitting Data, $V_{DD} = 1.8V$ or $3.3V$ , SCL low to SDA output valid			3.45	$\mu s$
t <sub>VD;ACK</sub>	Valid data time of ACK condition	Transmitting Data, $V_{DD} = 1.8V$ or $3.3V$ , ACK signal from SCL low to SDA (out) low			3.45	$\mu s$
<b>SDA and SCL Fast Mode Characteristics (Target)</b>						
f <sub>SCLS</sub>	Clock frequency for target	$V_{DD} = 1.8V$ or $3.3V$	100		400	kHz
t <sub>VD;DAT</sub>	Valid data time	Transmitting data, $V_{DD} = 1.8V$ , SCL low to SDA output valid			0.9	$\mu s$

## 6.19 I2C Requirements and Characteristics (continued)

Operating under these conditions unless otherwise noted:  $3V \leq V_{LDO\_3V3} \leq 3.6V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, $V_{DD} = 1.8V$ or $3.3V$ , ACK signal from SCL low to SDA (out) low			0.9	$\mu s$
<b>SDA and SCL Fast Mode Plus Characteristics (Target)</b>						
$f_{SCLS}$	Clock frequency for Fast Mode Plus <sup>1</sup>	$V_{DD} = 1.8V$ or $3.3V$	400		800	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, $V_{DD} = 1.8V$ or $3.3V$ , SCL low to SDA output valid			0.55	$\mu s$
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, $V_{DD} = 1.8V$ or $3.3V$ , ACK signal from SCL low to SDA (out) low			0.55	$\mu s$

(1) Controller must control  $f_{SCLS}$  to make sure  $t_{LOW} > t_{VD; ACK}$ .

## 6.20 Typical Characteristics

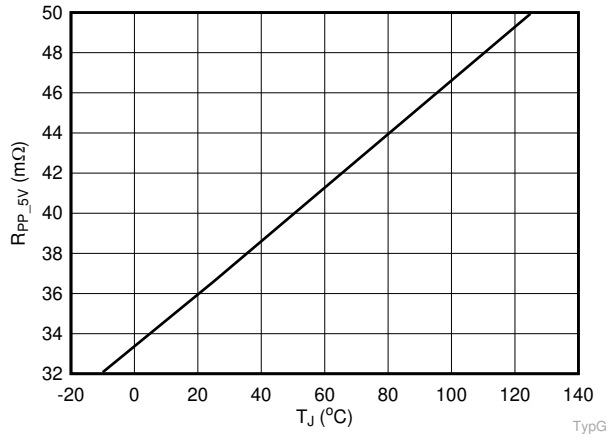


Figure 6-1. PP\_5V Rdson vs Temperature

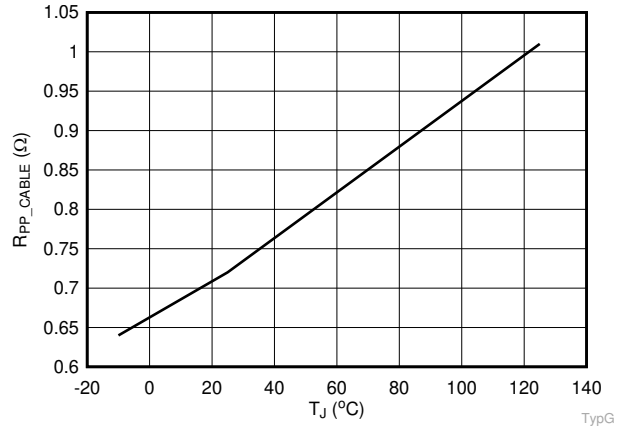


Figure 6-2. PP\_CABLE Rdson vs Temperature

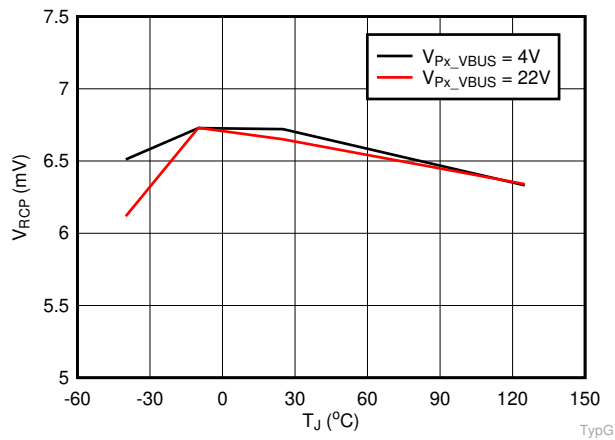


Figure 6-3. V<sub>RCP</sub> vs Temperature

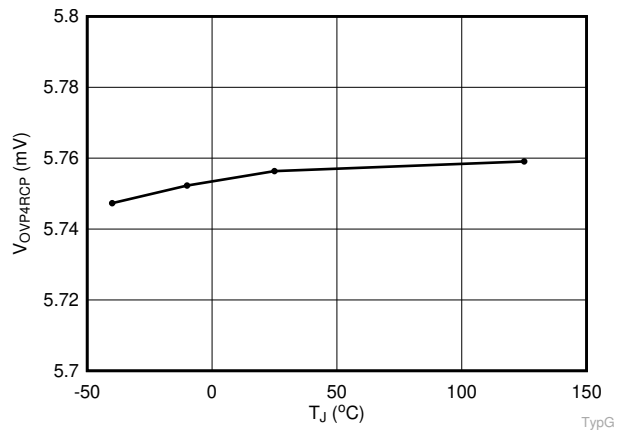


Figure 6-4. V<sub>OVP4RCP</sub> (Setting 2) vs Temperature

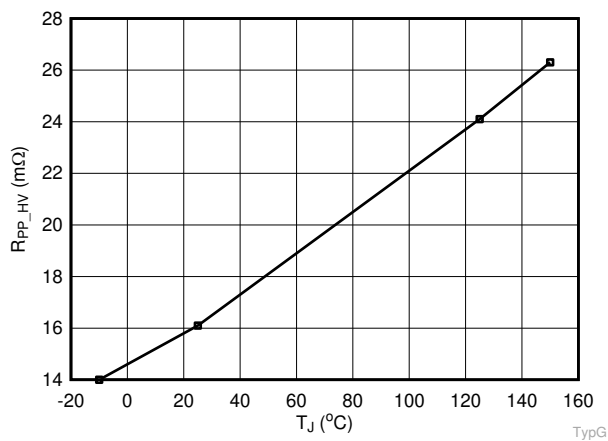


Figure 6-5. R<sub>PPHV</sub> vs. Temperature for TPS25751AD

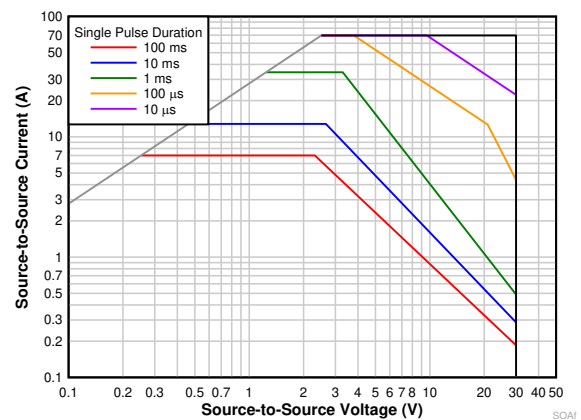


Figure 6-6. Safe-Operating-Area (SOA) of PPHV for TPS25751AD

## 6.20 Typical Characteristics (continued)

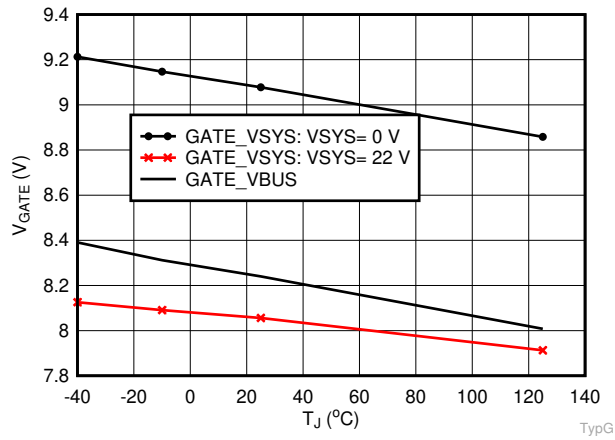


Figure 6-7. V<sub>GATE\_VBUS\_ON</sub> vs Temperature for TPS25751AS

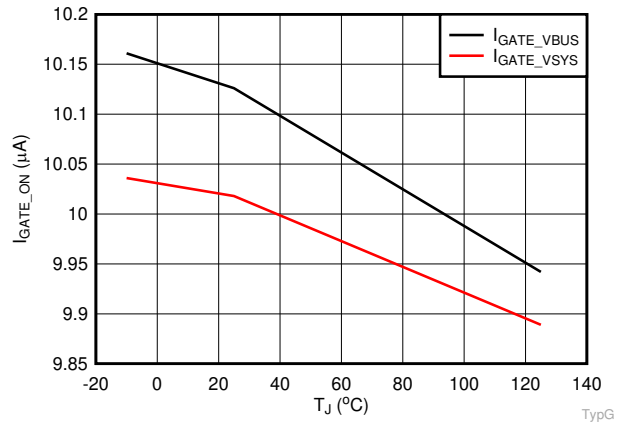


Figure 6-8. I<sub>GATE\_ON</sub> vs Temperature for TPS25751AS

## 7 Parameter Measurement Information

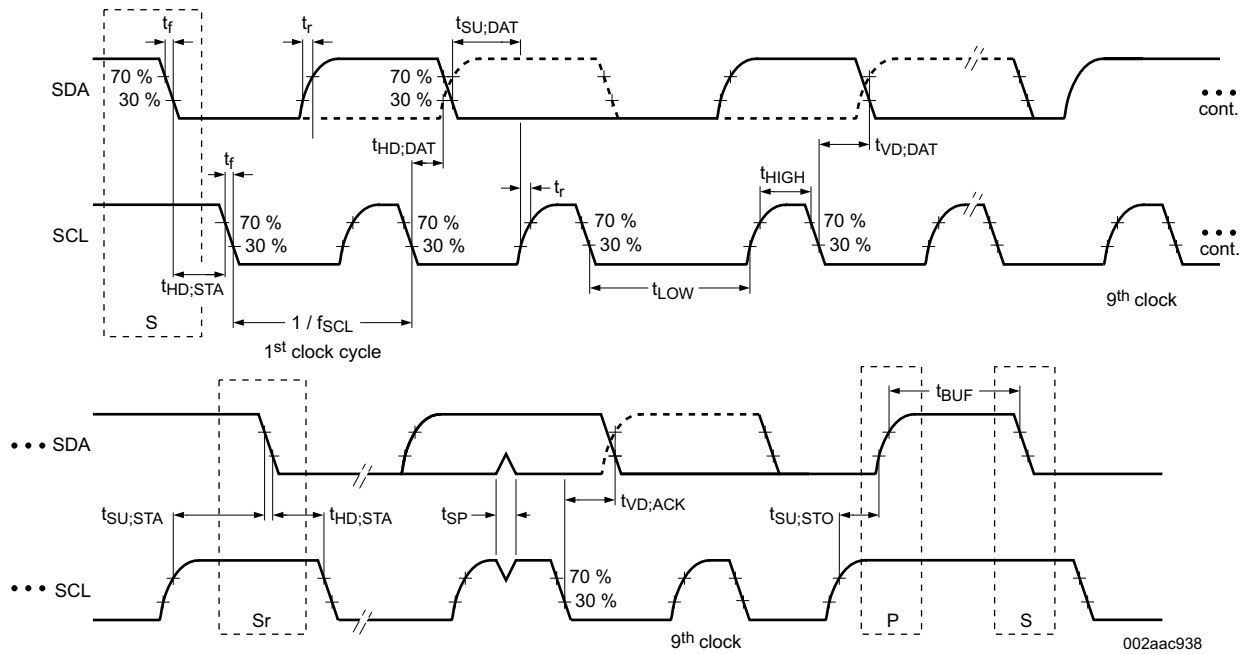


Figure 7-1. I<sup>2</sup>C Target Interface Timing

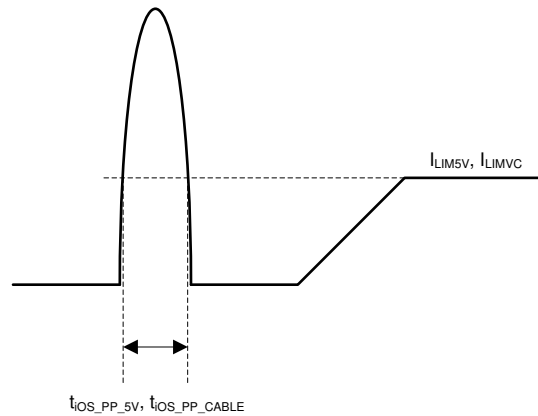


Figure 7-2. Short-circuit Response Time for Internal Power Paths PP\_5V and PP\_CABLE

## 8 Detailed Description

### 8.1 Overview

The TPS25751A is a fully-integrated USB Power Delivery (USB-PD) management device providing cable plug and orientation detection for USB Type-C and PD receptacles. The TPS25751A communicates with the other USB Type-C and PD port partner at the opposite end of the cable. The TPS25751AS also enables a high voltage port power switch for sourcing and sinking. The TPS25751AD also enables an integrated port power switch for sourcing and sinking.

The TPS25751A is divided into several main sections:

- USB-PD controller
- Cable plug and orientation detection circuitry
- Port power switches
- Power management circuitry
- Digital core

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the CC1 pin or the CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of features, and more detailed circuitry, see [USB-PD Physical Layer](#).

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion and the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of features, and more detailed circuitry, see [Cable Plug and Orientation Detection](#).

The port power switches provide power to the VBUS pin and CC1 or CC2 pins based on the detected plug orientation. For a high-level block diagram of the port power switches, a description of features, and more detailed circuitry, see [Power Paths](#).

The power management circuitry receives and provides power to the TPS25751A internal circuitry and LDO\_3V3 output. See [Power Management](#) for more information.

The digital core provides the engine for receiving, processing, and sending all USB-PD packets as well as handling control of all other TPS25751A functionality. A portion of the digital core contains ROM memory, which contains all the necessary firmware required to execute Type-C and PD applications. In addition, a section of the ROM, called boot code, is capable of initializing the TPS25751A, loading of the device configuration information, and loading any code patches into volatile memory in the digital core. For a high-level block diagram of the digital core, a description of features, and more detailed circuitry, see [Digital Core](#).

The TPS25751A has one I<sup>2</sup>C controller to write to and read from external target devices such as a battery charger or an optional external EEPROM memory (see [I2C Interface](#)).

The TPS25751A also integrates a thermal shutdown mechanism and runs off of accurate clocks provided by the integrated oscillator.

## 8.2 Functional Block Diagram

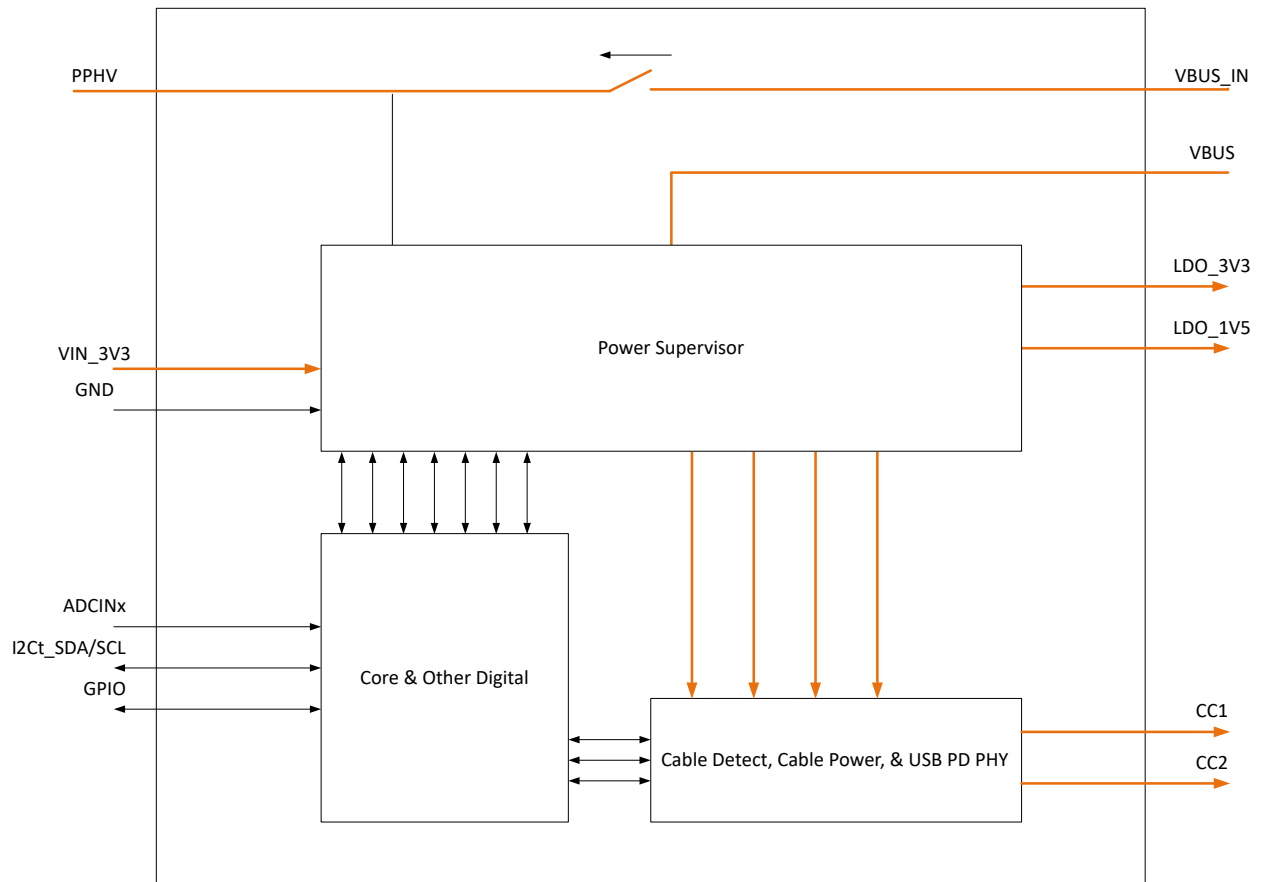
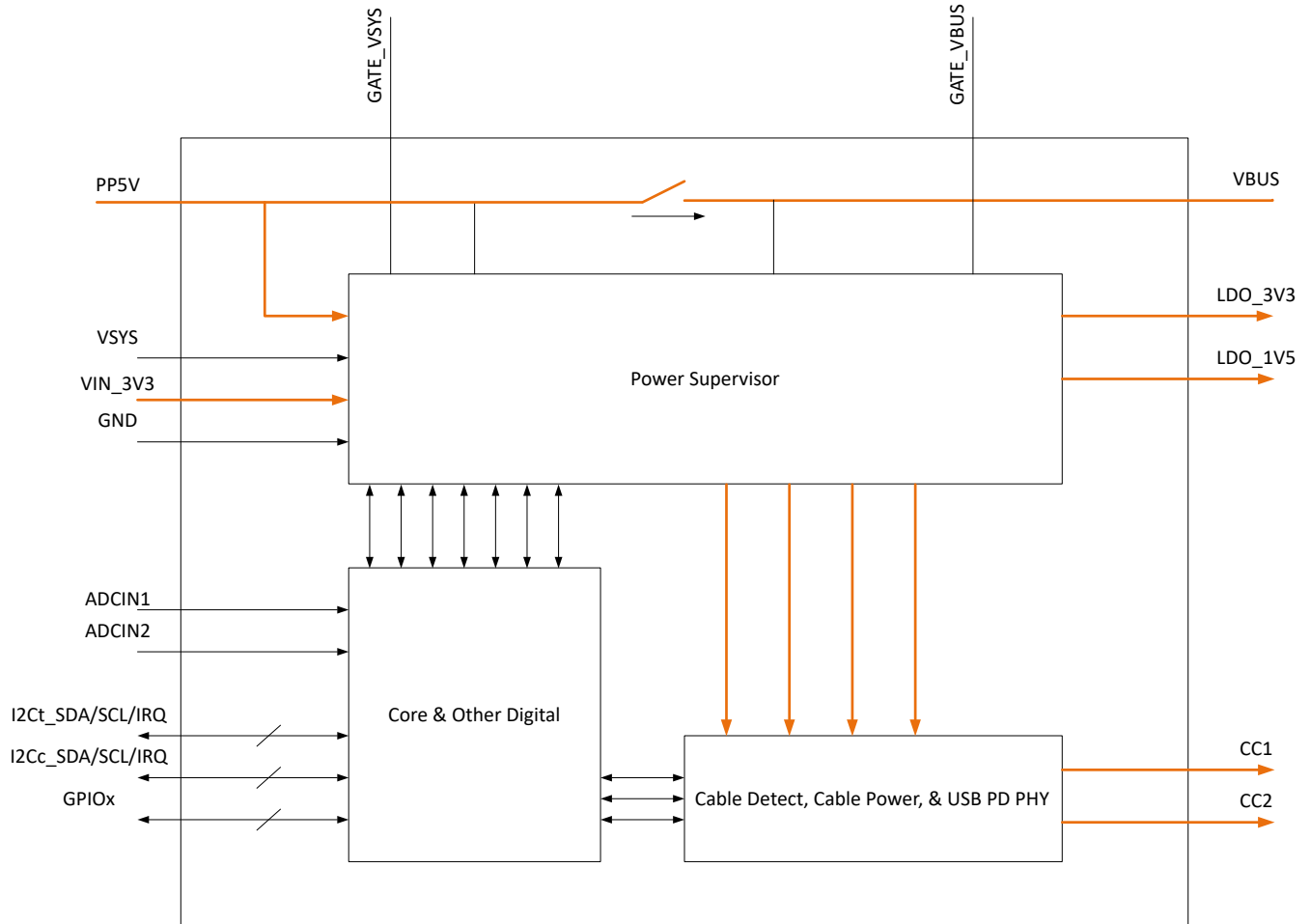


Figure 8-1. TPS25751AD



**Figure 8-2. TPS25751AS**

### 8.3 Feature Description

#### 8.3.1 USB-PD Physical Layer

Figure 8-3 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block.

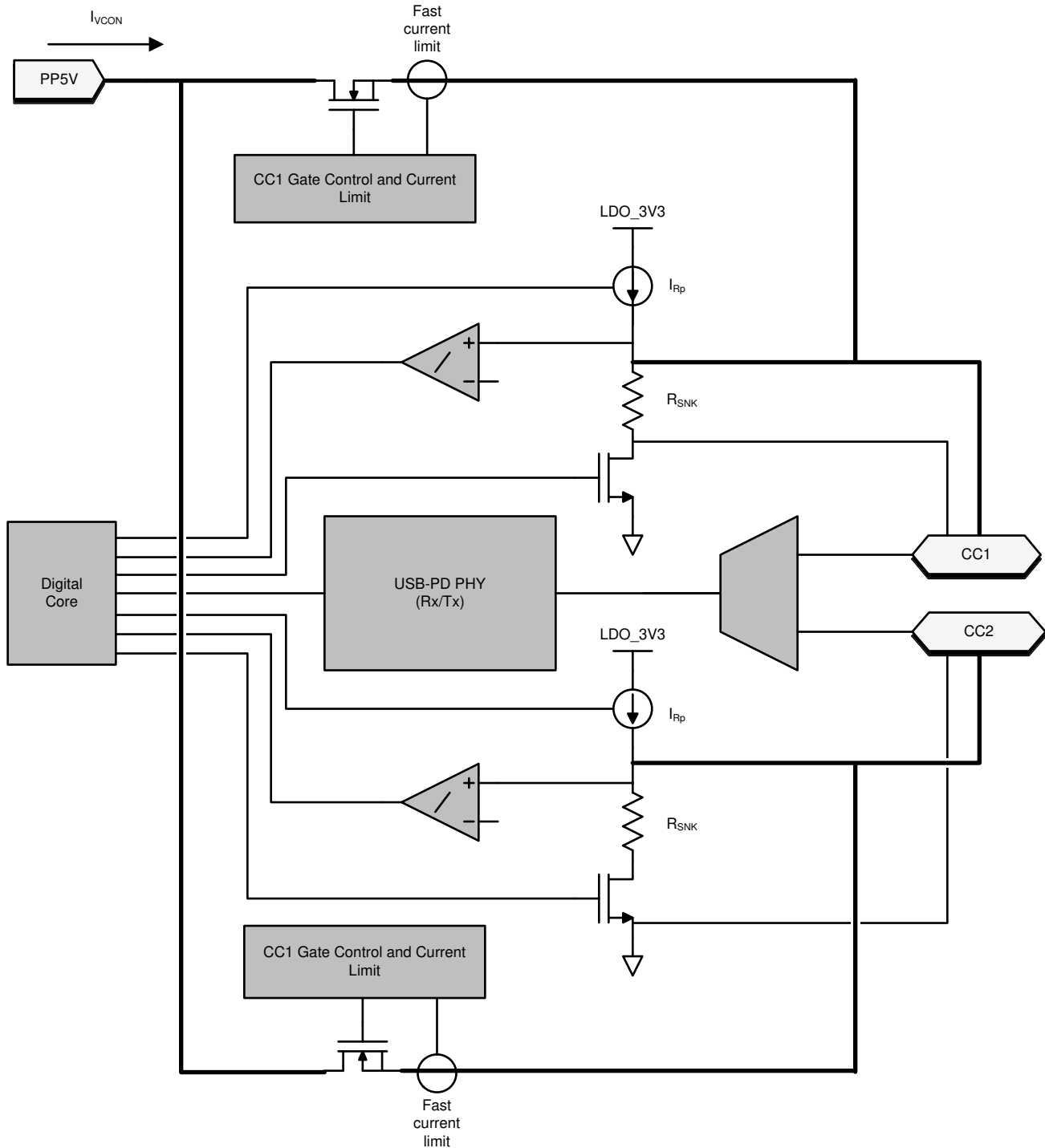


Figure 8-3. USB-PD Physical Layer and Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (CC1 or CC2) that is DC biased due to the Rp (or Rd) cable attach mechanism.

### 8.3.1.1 USB-PD Encoding and Signaling

Figure 8-4 illustrates the high-level block diagram of the baseband USB-PD transmitter. Figure 8-5 illustrates the high-level block diagram of the baseband USB-PD receiver.

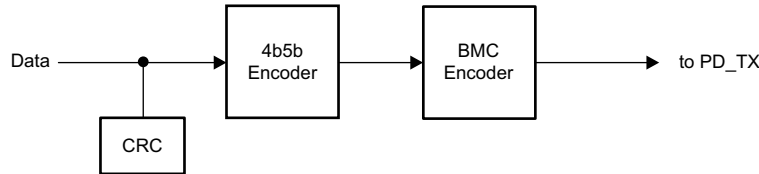


Figure 8-4. USB-PD Baseband Transmitter Block Diagram

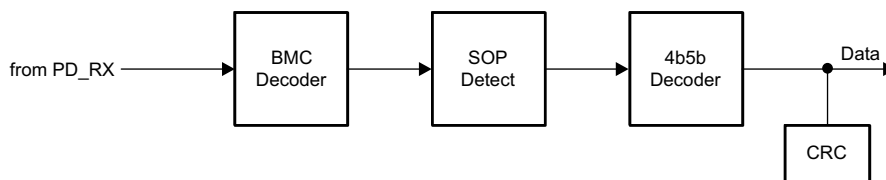


Figure 8-5. USB-PD Baseband Receiver Block Diagram

### 8.3.1.2 USB-PD Bi-Phase Marked Coding

The USB-PD physical layer implemented in the TPS25751A is compliant to the *USB-PD Specifications*. The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphasic Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). *Biphase Mark Coding Example* illustrates Biphasic Mark Coding.

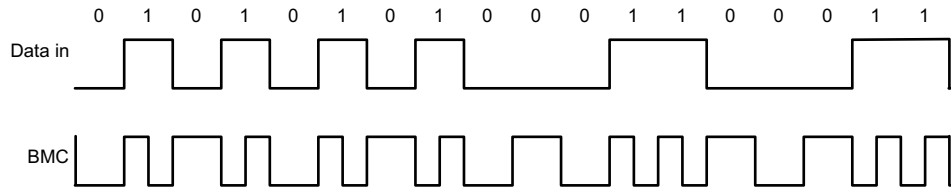


Figure 8-6. Biphasic Mark Coding Example

The USB PD baseband signal is driven onto the CC1 or CC2 pin with a tri-state driver. The tri-state driver is slew rate to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to make sure the receiver clocks the final bit of EOP.

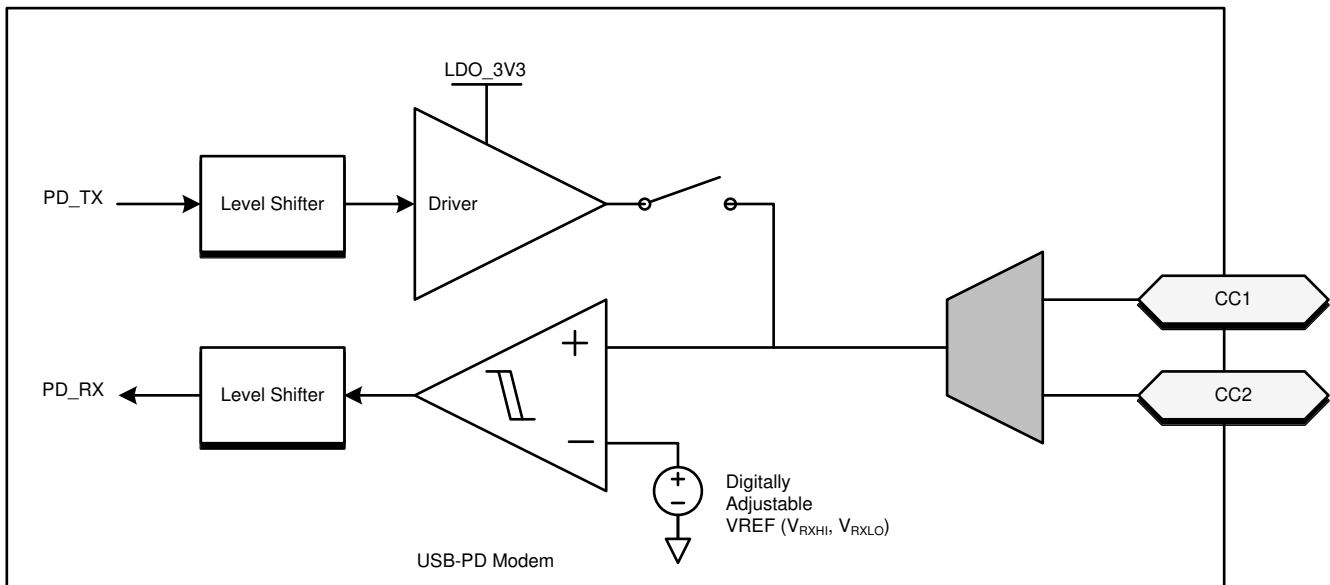
### 8.3.1.3 USB-PD Transmit (TX) and Receive (Rx) Masks

The USB-PD driver meets the defined USB-PD BMC TX masks. Because a BMC coded “1” contains a signal edge at the beginning and middle of the UI, and the BMC coded “0” contains only an edge at the beginning, the masks are different for each. The USB-PD receiver meets the defined USB-PD BMC Rx masks. The boundaries of the Rx outer mask are specified to accommodate a change in signal amplitude due to the ground offset through the cable. The Rx masks are therefore larger than the boundaries of the TX outer mask. Similarly, the boundaries of the Rx inner mask are smaller than the boundaries of the TX inner mask. Triangular time masks are superimposed on the TX outer masks and defined at the signal transitions to require a minimum edge rate

that has minimal impact on adjacent higher speed lanes. The TX inner mask enforces the maximum limits on the rise and fall times. Refer to the [USB-PD Specifications](#) for more details.

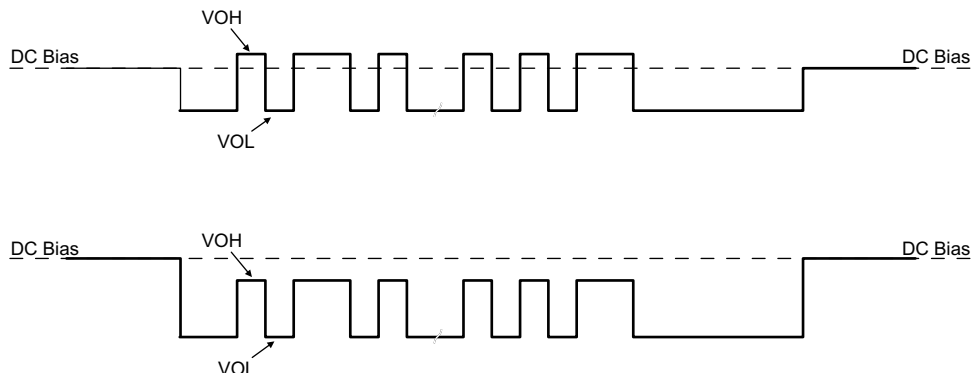
### 8.3.1.4 USB-PD BMC Transmitter

The TPS25751A transmits and receives USB-PD data over one of the CCy pins for a given CC pin pair (one pair per USB Type-C port). The CCy pins are also used to determine the cable orientation and maintain the cable/device attach detection. Thus, a DC bias exists on the CCy pins. The transmitter driver overdrives the CCy DC bias while transmitting, but returns to a Hi-Z state, allowing the DC voltage to return to the CCy pin when not transmitting. While either CC1 or CC2 can be used for transmitting and receiving, during a given connection only, the one that mates with the CC pin of the plug is used, so there is no dynamic switching between CC1 and CC2. [USB-PD BMC TX/RX Block Diagram](#) shows the USB-PD BMC TX and RX driver block diagram.



**Figure 8-7. USB-PD BMC TX/RX Block Diagram**

[Figure 8-8](#) shows the transmission of the BMC data on top of the DC bias. Note that the DC bias can be anywhere between the minimum and maximum threshold for detecting a Sink attach. This note means that the DC bias can be above or below the VOH of the transmitter driver.



**Figure 8-8. TX Driver Transmission with DC Bias**

The transmitter drives a digital signal onto the CCy lines. The signal peak,  $V_{TXHI}$ , is set to meet the TX masks defined in the [USB-PD Specifications](#). Note that the TX mask is measured at the far-end of the cable.

When driving the line, the transmitter driver has an output impedance of  $Z_{DRIVER}$ .  $Z_{DRIVER}$  is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent.  $Z_{DRIVER}$  impacts the noise ingress in the cable.

**ZDRIVER Circuit** shows the simplified circuit determining  $Z_{DRIVER}$ . The circuit is specified such that noise at the receiver is bounded.

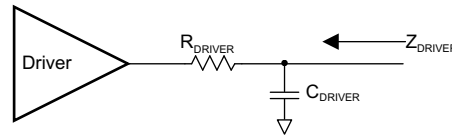


Figure 8-9. ZDRIVER Circuit

### 8.3.1.5 USB-PD BMC Receiver

The receiver block of the TPS25751A receives a signal that follows the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask.

**Example USB-PD Multi-Drop Configuration** shows an example of a multi-drop USB-PD connection (only the CC wire). This connection has the typical Sink (device) to Source (host) connection, but also includes cable USB-PD Tx/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z ( $Z_{BMCRX}$ ). The **USB-PD Specification** also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

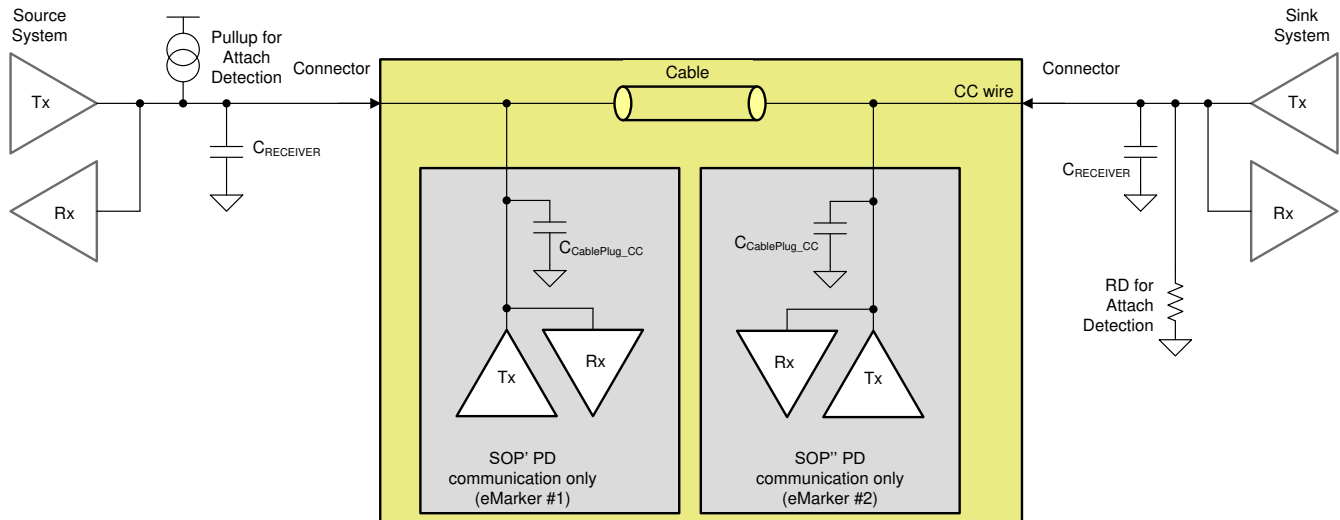


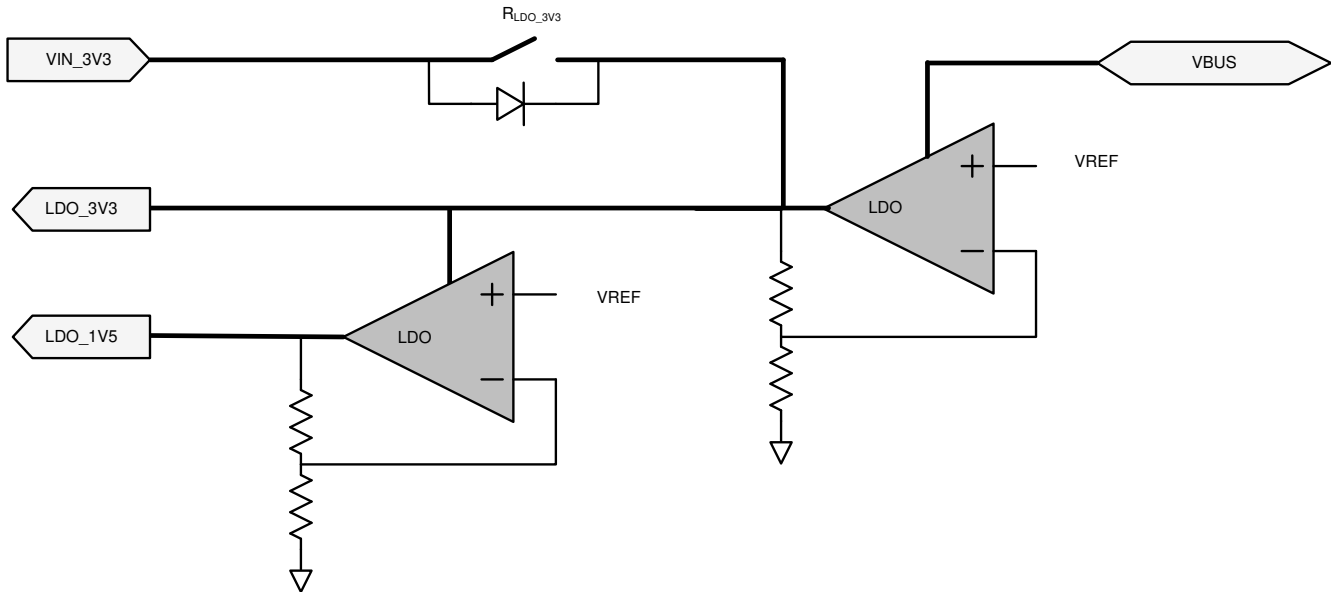
Figure 8-10. Example USB-PD Multi-Drop Configuration

### 8.3.1.6 Squelch Receiver

The TPS25751A has a squelch receiver to monitor for the bus idle condition as defined by the USB PD specification.

### 8.3.2 Power Management

The TPS25751A power management block receives power and generates voltages to provide power to the TPS25751A internal circuitry. These generated power rails are LDO\_3V3 and LDO\_1V5. LDO\_3V3 can also be used as a low power output for external EEPROM memory. The power supply path is shown in [Figure 8-11](#).



**Figure 8-11. Power Supplies**

The TPS25751A is powered from either VIN\_3V3 or VBUS. The normal power supply input is VIN\_3V3. When powering from VIN\_3V3, current flows from VIN\_3V3 to LDO\_3V3 to power the core 3.3V circuitry and I/Os. A second LDO steps the voltage down from LDO\_3V3 to LDO\_1V5 to power the 1.5V core digital circuitry. When VIN\_3V3 power is unavailable and power is available on VBUS, the device is considered to be in the dead-battery start-up condition. In a dead-battery start-up condition, the TPS25751A opens the VIN\_3V3 switch until the host clears the dead-battery flag through I<sup>2</sup>C. Therefore, the TPS25751A is powered from the VBUS input with the higher voltage during the dead-battery start-up condition and until the dead-battery flag is cleared. When powering from a VBUS input, the voltage on VBUS is stepped down through an LDO to LDO\_3V3.

### 8.3.2.1 Power-On And Supervisory Functions

A power-on reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present.

### 8.3.2.2 VBUS LDO

The TPS25751A contains an internal high-voltage LDO which is capable of converting VBUS to 3.3V for powering internal device circuitry. The VBUS LDO is used when in the dead-battery condition. (VIN\_3V3 is low and the dead-battery flag is active). The VBUS LDO is powered from VBUS.

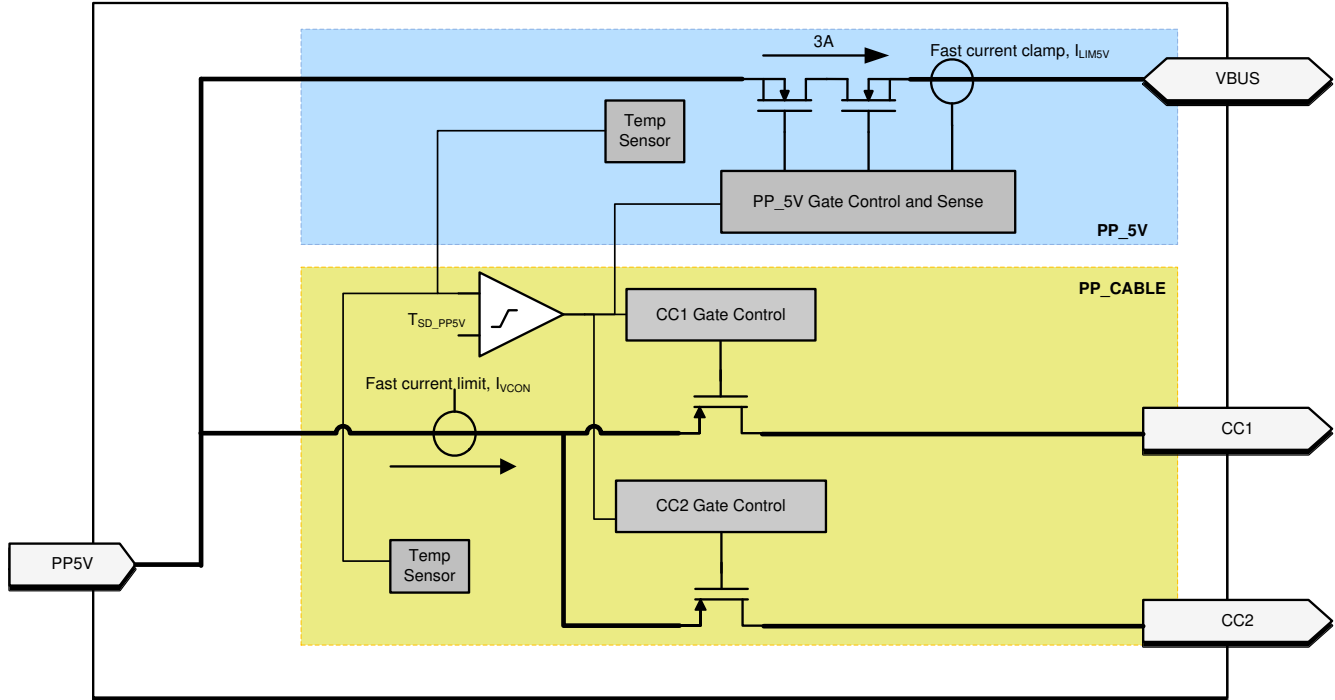
### 8.3.3 Power Paths

The TPS25751A has internal sourcing power paths: PP\_5V and PP\_CABLE. TPS25751AD has an integrated bidirectional high voltage load switch for sinking power path: PPHV.

TPS25751AS has a high voltage gate driver for power path control: PP\_EXT. Each power path is described in detail in this section.

#### 8.3.3.1 Internal Sourcing Power Paths

Figure 8-12 shows the TPS25751A internal sourcing power paths available in both TPS25751AD and TPS25751AS. The TPS25751A features two internal 5V sourcing power paths. The path from PP5V to VBUS is called PP\_5V. The path from PP5V to CCx is called PP\_CABLE. Each path contains two back-to-back common drain N-FETs, with current clamping protection, overvoltage protection, UVLO protection, and temperature sensing circuitry. PP\_5V can conduct up to 3A continuously, while PP\_CABLE can conduct up to 315mA continuously. When disabled, the blocking FET protects the PP5V rail from high-voltage that can appear on VBUS.



**Figure 8-12. Port Power Switches**

#### 8.3.3.1.1 PP\_5V Current Clamping

The current through the internal PP\_5V path are current limited to  $I_{LIM5V}$ . The  $I_{LIM5V}$  value is configured by application firmware. When the current through the switch exceeds  $I_{LIM5V}$ , the current limiting circuit activates within  $t_{OS\_PP\_5V}$  and the path behaves as a constant current source. If the duration of the overcurrent event exceeds  $t_{LIM}$ , the PP\_5V switch is disabled.

#### 8.3.3.1.2 PP\_5V Local Overtemperature Shut Down (OTSD)

When PP\_5V clamps the current, the temperature of the switch begin to increase. When the local temperature sensors of PP\_5V or PP\_CABLE detect that  $T_J > T_{SD\_PP5V}$ , the PP\_5V switch is disabled and the affected port enters the USB Type-C ErrorRecovery state.

#### 8.3.3.1.3 PP\_5V OVP

The overvoltage protection level is automatically configured based on the expected maximum  $V_{BUS}$  voltage, which depends upon the USB PD contract. When the voltage on the VBUS pin of a port exceeds the configured value ( $V_{OVP4RCP}$ ) while PP\_5V is enabled, then PP\_5V is disabled within  $t_{PP\_5V\_ovp}$  and the port enters into the Type-C ErrorRecovery state.

#### 8.3.3.1.4 PP\_5V UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold ( $V_{PP5V\_UVLO}$ ) while PP\_5V is enabled, then PP\_5V is disabled within  $t_{PP\_5V\_uvlo}$  and the port that had PP\_5V enabled enters into the Type-C ErrorRecovery state.

#### 8.3.3.1.5 PP\_5V Reverse Current Protection

If  $V_{VBUS} - V_{PP5V} > V_{PP\_5V\_RCP}$ , then the PP\_5V path is automatically disabled within  $t_{PP\_5V\_rcp}$ . If the RCP condition clears, then the PP\_5V path is automatically enabled within  $t_{ON}$ .

#### 8.3.3.1.6 PP\_CABLE Current Clamp

When enabled and providing VCONN power, the TPS25751A PP\_CABLE power switch clamps the current to  $I_{VCON}$ . When the current through the PP\_CABLE switch exceeds  $I_{VCON}$ , the current clamping circuit activates within  $t_{OS\_PP\_CABLE}$  and the switch behaves as a constant current source.

### 8.3.3.1.7 PP\_CABLE Local Overtemperature Shut Down (OTSD)

When PP\_CABLE clamps the current, the temperature of the switch begins to increase. When the local temperature sensors of PP\_5V or PP\_CABLE detect that  $T_J > T_{SD\_PP5V}$ , the PP\_CABLE switch is disabled and latched off within  $t_{PP\_CABLE\_off}$ . The port then enters the USB Type-C ErrorRecovery state.

### 8.3.3.1.8 PP\_CABLE UVLO

If the PP5V pin voltage falls below the undervoltage lock out threshold ( $V_{PP5V\_UVLO}$ ), then the PP\_CABLE switch is automatically disabled within  $t_{PP\_CABLE\_off}$ .

### 8.3.3.2 TPS25751AD Internal Powerpath

The TPS25751AD has internal controls for internal FETs (GATE\_VSYS and GATE\_VBUS as shown in [Internal Powerpath](#)) that require that VBUS\_IN be above  $V_{VBUS\_UVLO}$  before being able to enable the powerpath. [Internal Powerpath](#) shows a diagram of the powerpath. When a powerpath is enabled, the circuitry includes a slew rate control loop to make sure that external switches do not turn on too quickly (SS). The TPS25751AD senses the PPHV and VBUS voltages to control the gate voltages to enable or disable the FETs.

The powerpath control includes overvoltage protection (OVP) and reverse current protection (RCP).

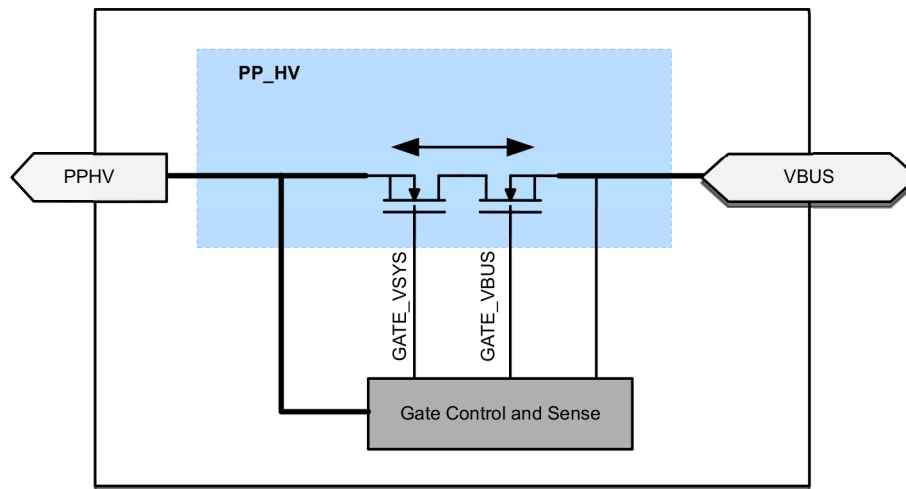


Figure 8-13. Internal Powerpath

#### 8.3.3.2.1 Overvoltage Protection (OVP)

The application firmware enables the OVP and configures the device based on the expected VBUS voltage. When the VBUS voltage surpasses the overvoltage protection parameters, the external powerpath is disabled. If the voltage on VBUS surpasses the configured threshold  $V_{OVP4V_{SYS}} = V_{OVP4RCP}/r_{OVP}$ , then GATE\_VSYS is automatically disabled within  $t_{PPHV\_FSD}$  to protect the system. If the voltage on VBUS surpasses the configured threshold  $V_{OVP4RCP}$ , then GATE\_VBUS is automatically disabled within  $t_{PPHV\_OVP}$ . When  $V_{VBUS}$  falls below  $V_{OVP4RCP} - V_{OVP4RCPH}$ , GATE\_VBUS is automatically re-enabled within  $t_{PPHV\_ON}$  because the OVP condition has cleared. This action allows two sinking power paths to be enabled simultaneously and GATE\_VBUS disables when necessary to make sure that  $V_{VBUS}$  remains below  $V_{OVP4RCP}$ .

While the TPS25751A is in BOOT mode in a dead-battery scenario (that is  $V_{IN\_3V3}$  is low), the device handles an OVP condition slightly differently. As long as the OVP condition is present, GATE\_VBUS and GATE\_VSYS are disabled. Once the OVP condition clears, both GATE\_VBUS and GATE\_VSYS are re-enabled. Because this mode is a dead-battery condition, the TPS25751A draws approximately  $I_{VIN\_3V3, ActSnk}$  from VBUS during this time to help discharge it.

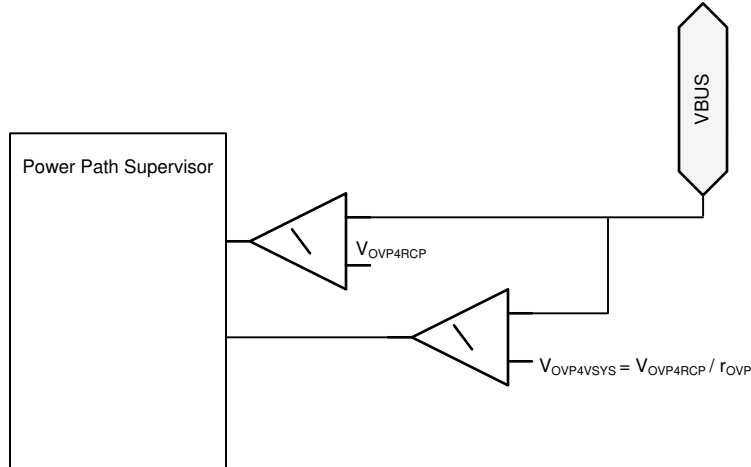
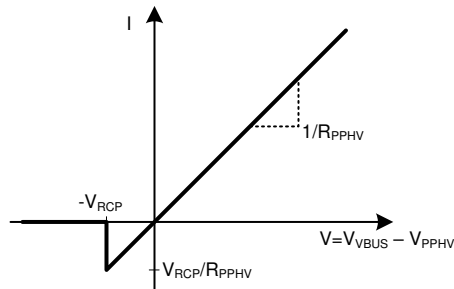


Figure 8-14. Diagram for OVP Comparators

### 8.3.3.2.2 Reverse-Current Protection (RCP)

The VSYS gate control circuit monitors the PPHV and VBUS voltages and detects reverse current when the  $V_{V_{SYS}}$  surpasses  $V_{V_{BUS}}$  by more than  $V_{RCP}$ . When the reverse current condition is detected, GATE\_VBUS is disabled within  $t_{PPHV\_RCP}$ . When the reverse current condition is cleared, GATE\_VBUS is re-enabled within  $t_{PPHV\_ON}$ . This action limits the amount of reverse current that can flow from PPHV to VBUS through the external N-ch MOSFETs. In reverse current protection mode, the power switch controlled by GATE\_VBUS is allowed to behave resistively until the current reaches  $V_{RCP} / R_{PPHV}$  and then blocks reverse current from PPHV to VBUS.



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Figure 8-15. Switch I-V Curve for RCP on Powerpath Switches

### 8.3.3.2.3 VBUS UVLO

The TPS25751A monitors VBUS voltage and detects when the voltage falls below  $V_{VBUS\_UVLO}$ . When the UVLO condition is detected, GATE\_VBUS is disabled within  $t_{PPHV\_RCP}$ . When the UVLO condition is cleared, GATE\_VBUS is re-enabled within  $t_{PPHV\_ON}$ .

### 8.3.3.2.4 Discharging VBUS to Safe Voltage

The TPS25751A has an integrated active pulldown ( $I_{DSCH}$ ) on VBUS for discharging from high voltage to VSAFE0V (0.8V). This discharge is applied when the device is in an Unattached Type-C state.

### 8.3.3.3 External Powerpath Control PP\_EXT

The TPS25751AS has two N-ch gate drivers designed to control a sinking path from VBUS to VSYS and a sourcing path from VSYS to VBUS. The charge pump for these gate drivers requires VBUS to be above  $V_{VBUS\_UVLO}$ . When a sink path is enabled, the circuitry includes a slew rate control loop to make sure that external switches do not turn on too quickly (SS). The TPS25751AS senses the VSYS and VBUS voltages to control the gate voltages to enable or disable the external FETs.

The high voltage power path control includes overvoltage protection (OVP), and reverse current protection (RCP). Adding resistance in series with a GATE pin of the TPS25751AS and the gate pin of the N-ch MOSFET slows down the turnoff time when OVP or RCP occurs. Any such resistance must be minimized, and not allowed to exceed  $3\Omega$ .

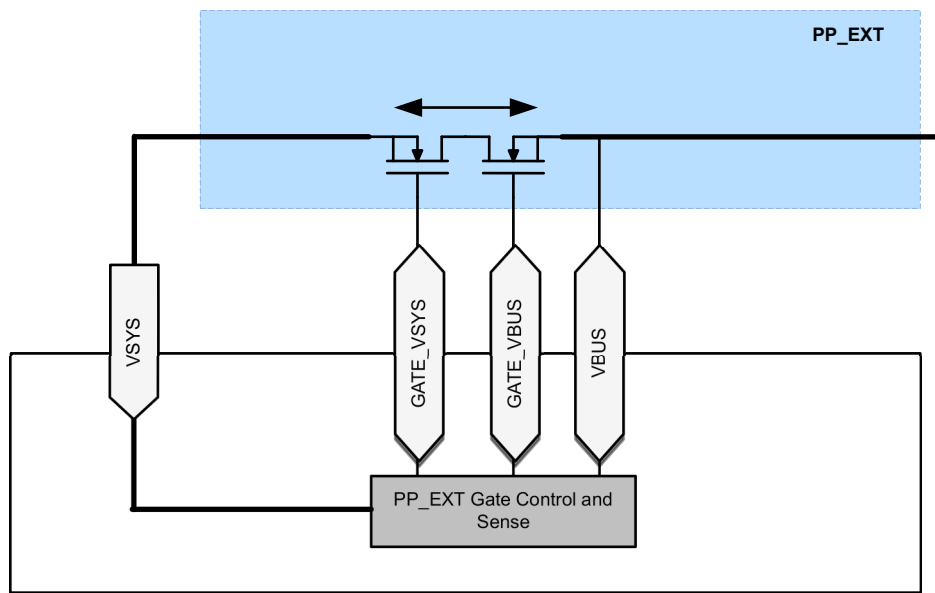


Figure 8-16. PP\_EXT External Powerpath Control

[Details of the VSYS Gate Driver](#) shows the GATE\_VSYS gate driver in more detail.

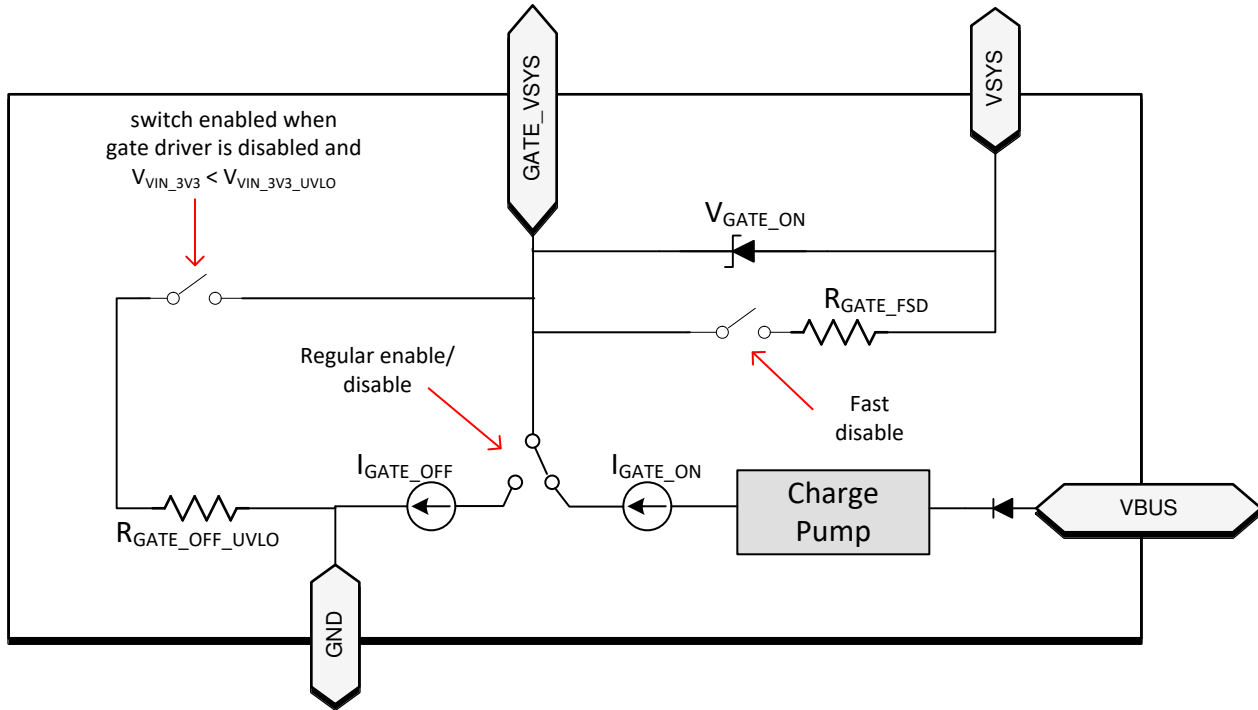
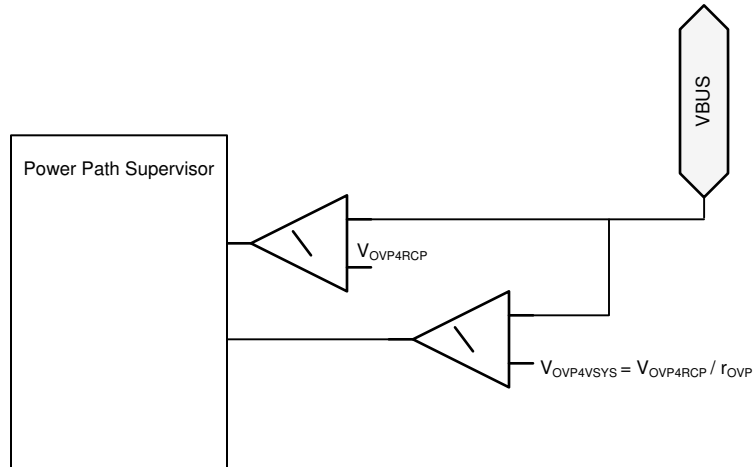


Figure 8-17. Details of the VSYS Gate Driver

#### 8.3.3.3.1 Overvoltage Protection (OVP)

The application firmware enables the OVP and configures the device based on the expected VBUS voltage. When the VBUS voltage surpasses the overvoltage protection parameters, the external powerpath is disabled. If the voltage on VBUS surpasses the configured threshold  $V_{OVP4V_{SYS}} = V_{OVP4RCP}/r_{OVP}$ , then GATE\_VSYS is automatically disabled within  $t_{PPHV\_FSD}$  to protect the system. If the voltage on VBUS surpasses the configured threshold  $V_{OVP4RCP}$ , then GATE\_VBUS is automatically disabled within  $t_{PPHV\_OVP}$ . When  $V_{VBUS}$  falls below  $V_{OVP4RCP} - V_{OVP4RCPH}$ , GATE\_VBUS is automatically re-enabled within  $t_{PPHV\_ON}$  because the OVP condition has cleared. This action allows two sinking power paths to be enabled simultaneously and GATE\_VBUS disables when necessary to make sure that  $V_{VBUS}$  remains below  $V_{OVP4RCP}$ .

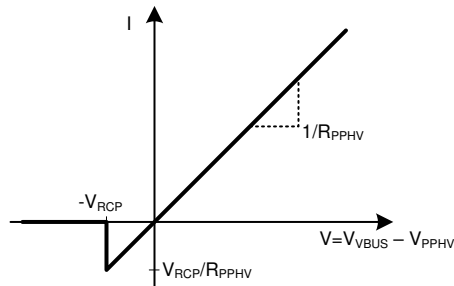
While the TPS25751A is in BOOT mode in a dead-battery scenario (that is  $V_{IN\_3V3}$  is low), the device handles an OVP condition slightly differently. As long as the OVP condition is present, GATE\_VBUS and GATE\_VSYS are disabled. Once the OVP condition clears, both GATE\_VBUS and GATE\_VSYS are re-enabled. Because this mode is a dead-battery condition, the TPS25751A draws approximately  $I_{VIN\_3V3, ActSnk}$  from VBUS during this time to help discharge it.



**Figure 8-18. Diagram for OVP Comparators**

### 8.3.3.3.2 Reverse-Current Protection (RCP)

The VSYS gate control circuit monitors the PPHV and VBUS voltages and detects reverse current when the  $V_{V_{SYS}}$  surpasses  $V_{V_{BUS}}$  by more than  $V_{RCP}$ . When the reverse current condition is detected, GATE\_VBUS is disabled within  $t_{PPHV\_RCP}$ . When the reverse current condition is cleared, GATE\_VBUS is re-enabled within  $t_{PPHV\_ON}$ . This action limits the amount of reverse current that can flow from PPHV to VBUS through the external N-ch MOSFETs. In reverse current protection mode, the power switch controlled by GATE\_VBUS is allowed to behave resistively until the current reaches  $V_{RCP} / R_{PPHV}$  and then blocks reverse current from PPHV to VBUS.



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**Figure 8-19. Switch I-V Curve for RCP on Powerpath Switches**

### 8.3.3.3.3 VBUS UVLO

The TPS25751A monitors VBUS voltage and detects when the voltage falls below  $V_{VBUS\_UVLO}$ . When the UVLO condition is detected, GATE\_VBUS is disabled within  $t_{PPHV\_RCP}$ . When the UVLO condition is cleared, GATE\_VBUS is re-enabled within  $t_{PPHV\_ON}$ .

### 8.3.3.3.4 Discharging VBUS to Safe Voltage

The TPS25751A has an integrated active pulldown ( $I_{DSCH}$ ) on VBUS for discharging from high voltage to VSAFE0V (0.8V). This discharge is applied when the device is in an Unattached Type-C state.

### 8.3.4 Cable Plug and Orientation Detection

Figure 8-20 shows the plug and orientation detection block at each CCy pin (CC1, CC2). Each pin has identical detection circuitry.

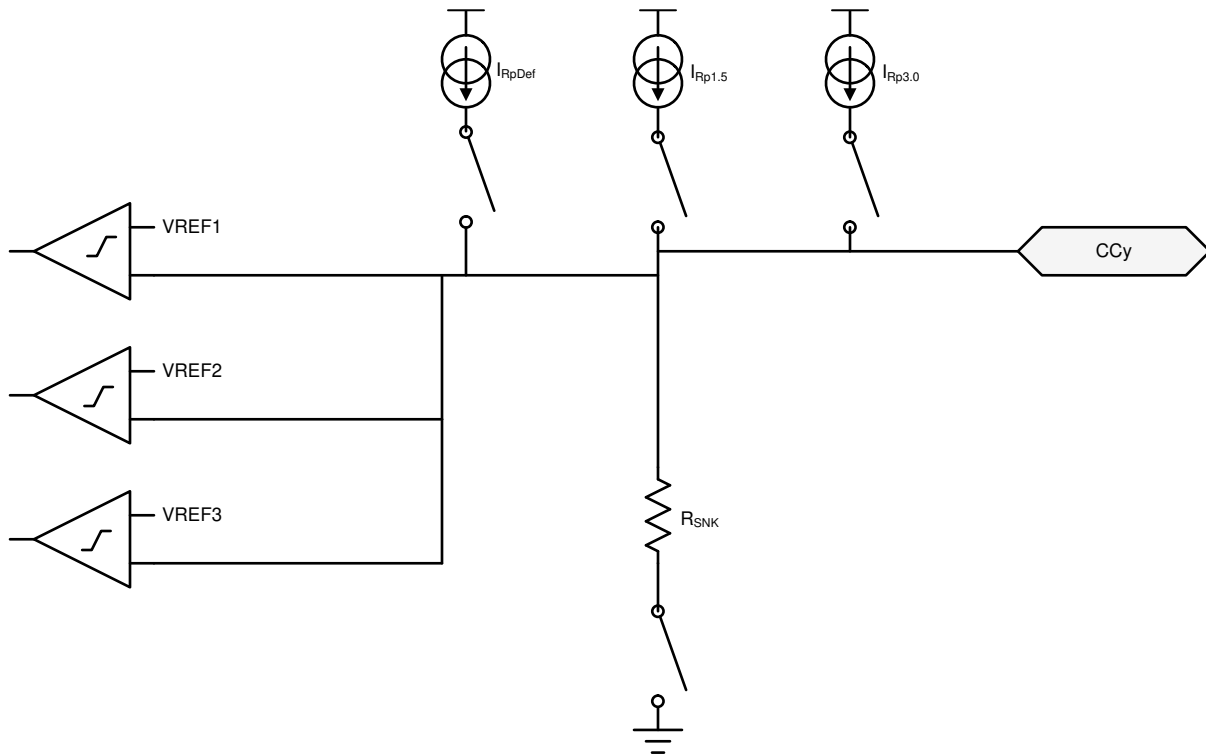


Figure 8-20. Plug and Orientation Detection Block

#### 8.3.4.1 Configured as a Source

When configured as a source, the TPS25751A detects when a cable or a Sink is attached using the CC1 and CC2 pins. When in a disconnected state, the TPS25751A monitors the voltages on these pins to determine what, if anything, is connected. See [USB Type-C Specification](#) for more information.

[Cable Detect States for a Source](#) shows the cable detect states for a source.

Table 8-1. Cable Detect States for a Source

CC1	CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both CCy pins for attach. Power is not applied to VBUS or VCONN.
Rd	Open	Sink attached	Monitor CC1 for detach. Power is applied to VBUS but not to VCONN (CC2).
Open	Rd	Sink attached	Monitor CC2 for detach. Power is applied to VBUS but not to VCONN (CC1).
Ra	Open	Powered Cable-No UFP attached	Monitor CC2 for a Sink attach and CC1 for cable detach. Power is not applied to VBUS or VCONN (CC1).

**Table 8-1. Cable Detect States for a Source (continued)**

CC1	CC2	CONNECTION STATE	RESULTING ACTION
Open	Ra	Powered Cable-No UFP attached	Monitor CC1 for a Sink attach and CC2 for cable detach. Power is not applied to VBUS or VCONN (CC1).
Ra	Rd	Powered Cable-UFP Attached	Provide power on VBUS and VCONN (CC1) then monitor CC2 for a Sink detach. CC1 is not monitored for a detach.
Rd	Ra	Powered Cable-UFP attached	Provide power on VBUS and VCONN (CC2) then monitor CC1 for a Sink detach. CC2 is not monitored for a detach.
Rd	Rd	Debug Accessory Mode attached	Sense either CCy pin for detach.
Ra	Ra	Corrosion Mitigation	Sense either CCy pin for detach.

When a TPS25751A port is configured as a Source, a current  $I_{RpDef}$  is driven out each CCy pin and each pin is monitored for different states. When a Sink is attached to the pin, a pulldown resistance of  $R_d$  to GND exists. The current  $I_{RpDef}$  is then forced across the resistance  $R_d$ , generating a voltage at the CCy pin. The TPS25751A applies  $I_{RpDef}$  until the device closes the switch from PP5V to VBUS, at which time application firmware can change to  $I_{Rp1.5A}$  or  $I_{Rp3.0A}$ .

When the CCy pin is connected to an active cable VCONN input, the pulldown resistance is different ( $R_a$ ). In this case, the voltage on the CCy pin lowers the PD controller recognizes the pulldown as an active cable.

The voltage on CCy is monitored to detect a disconnection depending upon which  $R_p$  current source is active. When a connection has been recognized and the voltage on CCy subsequently rises above the disconnect threshold for  $t_{CC}$ , the system registers a disconnection.

#### 8.3.4.2 Configured as a Sink

When a TPS25751A port is configured as a Sink, the TPS25751A presents a pulldown resistance  $R_{SNK}$  on each CCy pin and waits for a Source to attach and pull up the voltage on the pin. The Sink detects an attachment by the presence of VBUS and determines the advertised current from the Source based on the voltage on the CCy pin.

#### 8.3.4.3 Configured as a DRP

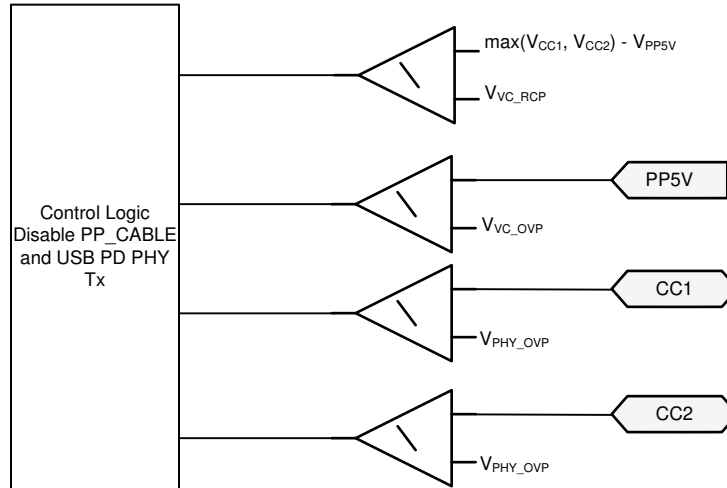
When a TPS25751A port is configured as a DRP, the TPS25751A alternates the CCy pins of the port between the pulldown resistance,  $R_{SNK}$ , and pullup current source,  $I_{Rp}$ .

#### 8.3.4.4 Dead Battery Advertisement

The TPS25751A supports booting from no-battery or dead-battery conditions by receiving power from VBUS. Type-C USB ports require a sink to present  $R_d$  on the CC pin before a USB Type-C source provides a voltage on VBUS. TPS25751A hardware is configured to present this  $R_d$  during a dead-battery or no-battery condition. Additional circuitry provides a mechanism to turn off this  $R_d$  once the device no longer requires power from VBUS.

#### 8.3.5 Overvoltage Protection (CC1, CC2)

The TPS25751A detects when the voltage on the CC1 or CC2 pin is too high or there is reverse current into the PP5V pin and takes action to protect the system. The protective action is to disable PP\_CABLE within  $t_{PP\_CABLE\_FSD}$  and disable the USB PD transmitter.



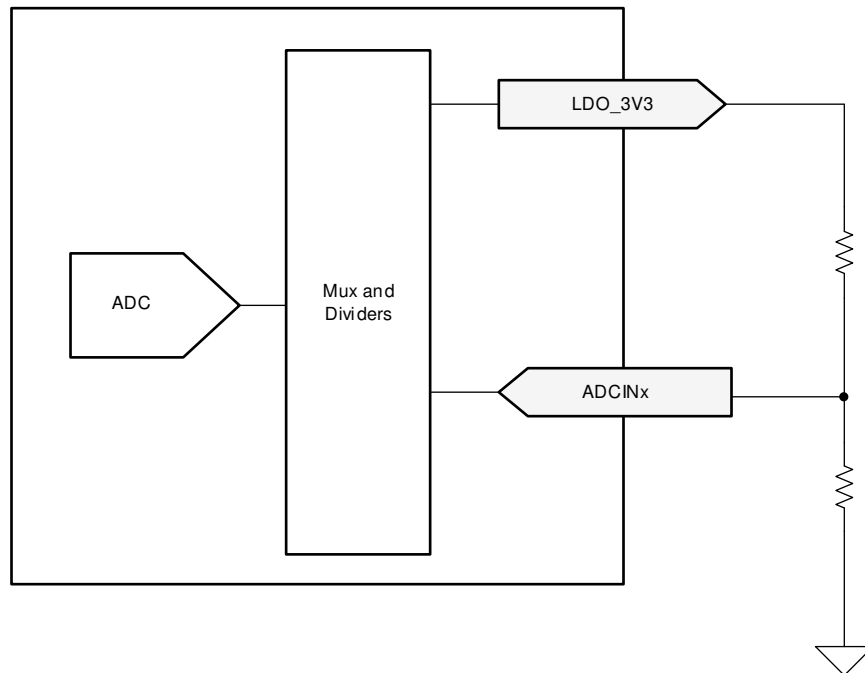
**Figure 8-21. Overvoltage and Reverse Current Protection for CC1 and CC2**

### 8.3.6 Default Behavior Configuration (ADCIN1, ADCIN2)

**Note**

This functionality is firmware controlled and subject to change.

The ADCINx inputs to the internal ADC control the behavior of the TPS25751A in response to VBUS being supplied when VIN\_3V3 is low (that is the dead-battery scenario). The ADCINx pins must be externally tied to the LDO\_3V3 pin via a resistive divider as shown in the following figure. At power-up the ADC converts the ADCINx voltage and the digital core uses these two values to determine start-up behavior. The available start-up configurations include options for I<sup>2</sup>C target address of I2Ct\_SCL/SDA, sink path control in dead-battery, and default configuration.



**Figure 8-22. ADCINx Resistor Divider**

The device behavior is determined in several ways depending upon the decoded value of the ADCIN1 and ADCIN2 pins. The following table shows the decoded values for different resistor divider ratios. See [Pin Strapping to Configure Default Behavior](#) for details on how the ADCINx configurations determine default device behavior. See [I<sup>2</sup>C Address Setting](#) for details on how ADCINx decoded values affects default I<sup>2</sup>C target address.

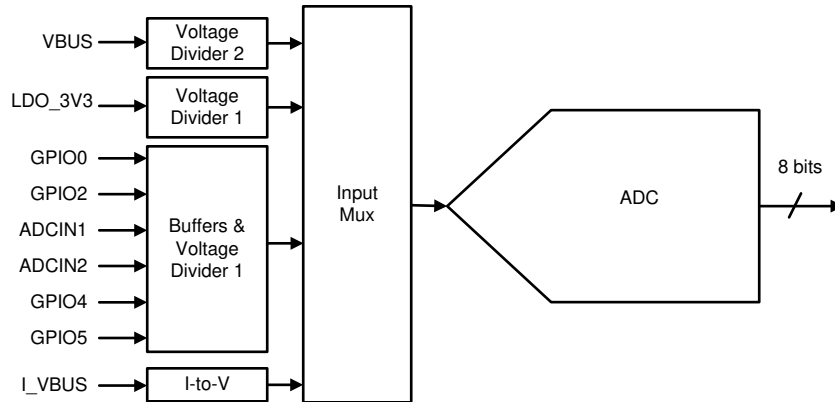
**Table 8-2. Decoding of ADCIN1 and ADCIN2 Pins**

DIV = R <sub>DOWN</sub> / (R <sub>UP</sub> + R <sub>DOWN</sub> ) <sup>(1)</sup>			Without Using R <sub>UP</sub> or R <sub>DOWN</sub>	ADCINx Decoded Value <sup>(2)</sup>
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

- (1) See [I<sup>2</sup>C Address Setting](#) to see the exact meaning of I<sup>2</sup>C Address Index.
- (2) See [Pin Strapping to Configure Default Behavior](#) for how to configure a given ADCINx decoded value.

### 8.3.7 ADC

The TPS25751A ADC is shown in [Figure 8-23](#). The ADC is an 8-bit successive approximation ADC. The input to the ADC is an analog input mux that supports multiple inputs from various voltages and currents in the device. The output from the ADC is available to be read and used by application firmware.



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**Figure 8-23. SAR ADC**

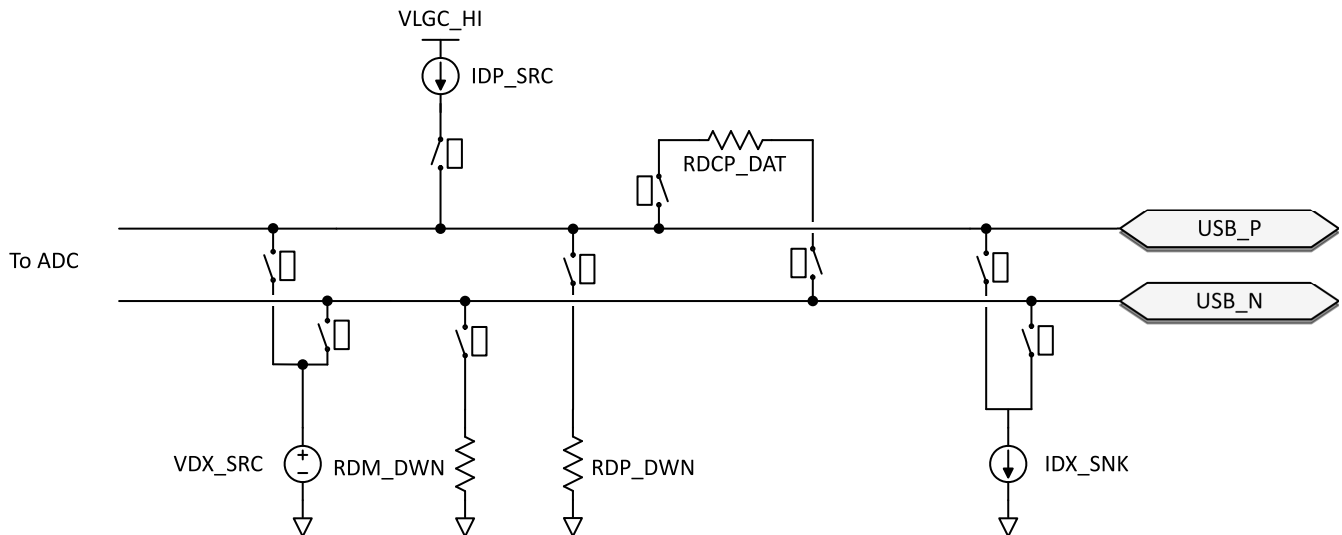
### 8.3.8 Liquid Detection

The TPS25751A features liquid detection and corrosion mitigation through monitoring the voltage on pins from the connector. The device monitors pins periodically checking for variations on the pin voltage indicating a short. When configured for corrosion mitigation, the PD controller disconnects from the far end device and monitors for voltage readings indicating the liquid is no longer present.

For additional information, refer to the [Section 9](#) section.

### 8.3.9 BC 1.2 (USB\_P, USB\_N)

The TPS25751A supports BC 1.2 as a Portable Device or Downstream Port using the hardware shown in [Figure 8-24](#).



**Figure 8-24. BC1.2 Hardware Components**

### 8.3.10 Digital Interfaces

The TPS25751A contains several different digital interfaces which can be used for communicating with other devices. The available interfaces include one I<sup>2</sup>C controller, one I<sup>2</sup>C target and additional GPIOs.

#### 8.3.10.1 General GPIO

GPIOx pins can be mapped to USB Type-C, USB PD, and application-specific events to control other ICs, interrupt a host processor, or receive input from another IC. This buffer is configurable to be a push-pull output, a weak push-pull, or open drain output. When configured as an input, the signal can be a de-glitched digital input. The push-pull output is a simple CMOS output with independent pull-down control allowing open-drain connections. The weak push-pull is also a CMOS output, but with GPIO\_RPU resistance in series with the drain. The supply voltage to the output buffer is LDO\_3V3 and LDO\_1V5 to the input buffer. When interfacing with non 3.3V I/O devices the output buffer can be configured as an open drain output and an external pull-up resistor attached to the GPIO pin. The pull-up and pull-down output drivers are independently controlled from the input and are enabled or disabled via application code in the digital core.

**Table 8-3. GPIO Functionality Table**

PIN NAME	TYPE	SPECIAL FUNCTIONALITY
GPIO0	I/O	General-purpose input or output, or LD1 for Liquid Detection
GPIO1	I/O	General-purpose input or output
GPIO2	I/O	General-purpose input or output, or LD2 for Liquid Detection
GPIO3	I/O	General-purpose input or output
GPIO4	I/O	D+, general-purpose input or output
GPIO5	I/O	D-, general-purpose input or output
GPIO6	I/O	General-purpose input or output
GPIO7	I/O	General-purpose input or output
I2Ct_IRQ(GPIO10)	O	IRQ for optional I2Ct, or used as a general-purpose output
GPIO11	O	General-purpose output
I2Cc_IRQ(GPIO12)	I	IRQ for I2Cc, or used as a general-purpose input

### 8.3.10.2 I<sup>2</sup>C Interface

The TPS25751A features two I<sup>2</sup>C interfaces that use an I<sup>2</sup>C I/O driver like the one shown in Figure 8-25. This I/O consists of an open-drain output and an input comparator with de-glitching.

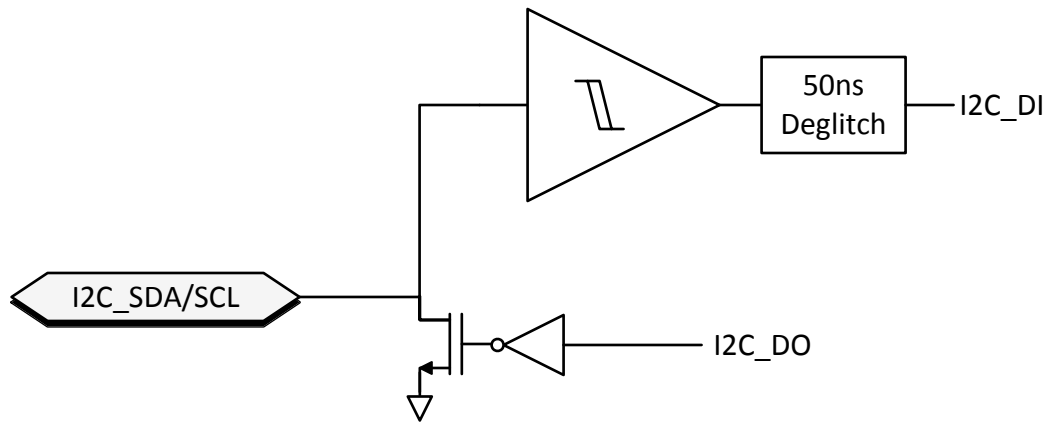


Figure 8-25. I<sup>2</sup>C Buffer

The TPS25751A has one I<sup>2</sup>C target interface ports: I2Ct. I2C port I2Ct is comprised of the I2Ct\_SDA, I2Ct\_SCL, and I2Ct\_IRQ pins. This interface provide general status information about the TPS25751A, as well as the ability to control the TPS25751A behavior, supporting communications to/from a connected device and/or cable supporting BMC USB-PD, and providing information about connections detected at the USB-C receptacle.

When the TPS25751A is in 'APP' mode TI recommends to use standard mode or Fast mode (that is a clock speed no higher than 400kHz). However, in the BOOT mode when a patch bundle is loaded Fast Mode Plus can be used (see  $f_{SCLs}$ ).

The TPS25751A has one I<sup>2</sup>C controller interface port. I<sup>2</sup>C is comprised of the I2Cc\_SDA, I2Cc\_SCL, and I2Cc\_IRQ pins. This interface can be used to read from or write to external target devices.

During boot, the TPS25751A attempts to read patch and Application Configuration data from an external EEPROM with a 7-bit target address of 0x50. The EEPROM must be at least 32 kilo-bytes.

Table 8-4. I<sup>2</sup>C Summary

I <sup>2</sup> C BUS	TYPE	TYPICAL USAGE
I2Ct	Target	Optionally can be connected to an external MCU. Also used to load the patch and application configuration.
I2Cc	Controller	Connect to a I <sup>2</sup> C EEPROM, Battery Charger. Use the LDO_3V3 pin as the pullup voltage. Multi-controller configuration is not supported.

#### 8.3.10.2.1 I<sup>2</sup>C Interface Description

The TPS25751A supports Standard and Fast mode I<sup>2</sup>C interfaces. The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pullup resistor. Data transfer can be initiated only when the bus is not busy.

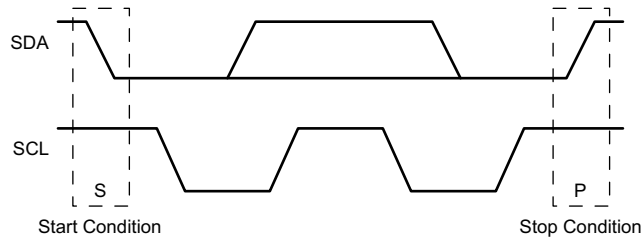
A controller sending a Start condition, a high-to-low transition on the SDA input and output, while the SCL input is high initiates I<sup>2</sup>C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The controller sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

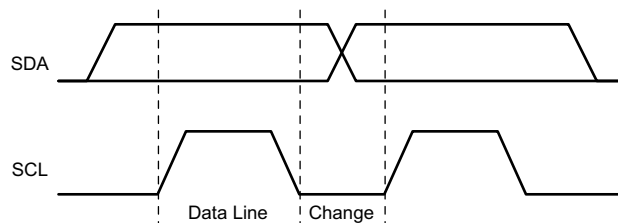
Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met for proper operation.

A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.

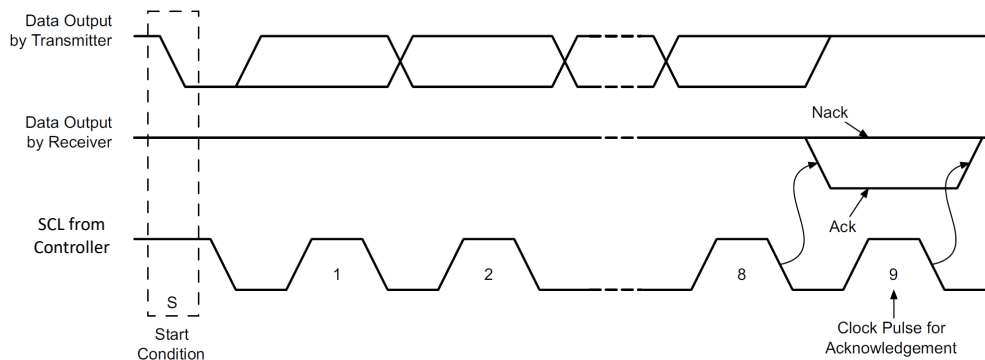
Figure 8-26 shows the start and stop conditions of the transfer. Figure 8-27 shows the SDA and SCL signals for transferring a bit. Figure 8-28 shows a data transfer sequence with the ACK or NACK at the last clock pulse.



**Figure 8-26. I<sup>2</sup>C Definition of Start and Stop Conditions**



**Figure 8-27. I<sup>2</sup>C Bit Transfer**



**Figure 8-28. I<sup>2</sup>C Acknowledgment**

### 8.3.10.2.1 I<sup>2</sup>C Clock Stretching

The TPS25751A features clock stretching for the I<sup>2</sup>C protocol. The TPS25751A target I<sup>2</sup>C port can hold the clock line (SCL) low after receiving (or sending) a byte, indicating that the bus is not yet ready to process more data. The controller communicating with the target must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the target is clock stretching, the clock line remains low.

The controller must wait until the clock line transitions high plus an additional minimum time (4µs for standard 100kbps I<sup>2</sup>C) before pulling the clock low again.

Any clock pulse can be stretched and typically the clock pulse before or after the acknowledgment bit is stretched.

### 8.3.10.2.1.2 I<sup>2</sup>C Address Setting

The I<sup>2</sup>C controller must only use I2Ct\_SCL/SDA for loading a patch bundle.

Once the boot process is complete, the port has a unique target address on the I2Ct\_SCL/SDA bus as selected by the ADCINx pins.

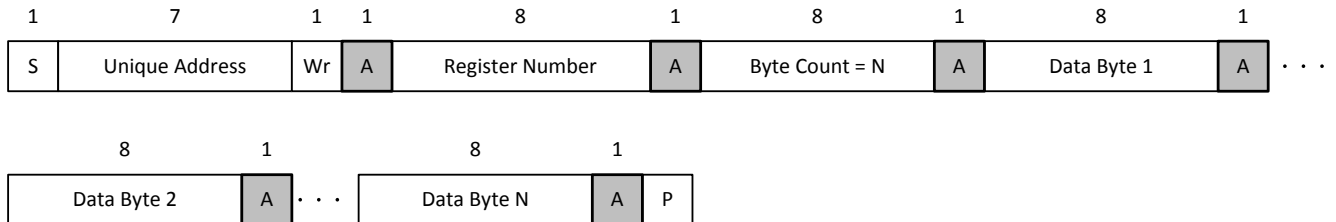
**Table 8-5. I<sup>2</sup>C Default Target Address for I2Ct\_SCL/SDA.**

I <sup>2</sup> C ADDRESS INDEX (DECODED FROM ADCIN1 AND ADCIN2) <sup>(1)</sup>	TARGET ADDRESS								AVAILABLE DURING BOOT
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
#1	0	1	0	0	0	0	0	R/W	Yes
#2	0	1	0	0	0	0	1	R/W	Yes
#3	0	1	0	0	0	1	0	R/W	Yes
#4	0	1	0	0	0	1	1	R/W	Yes

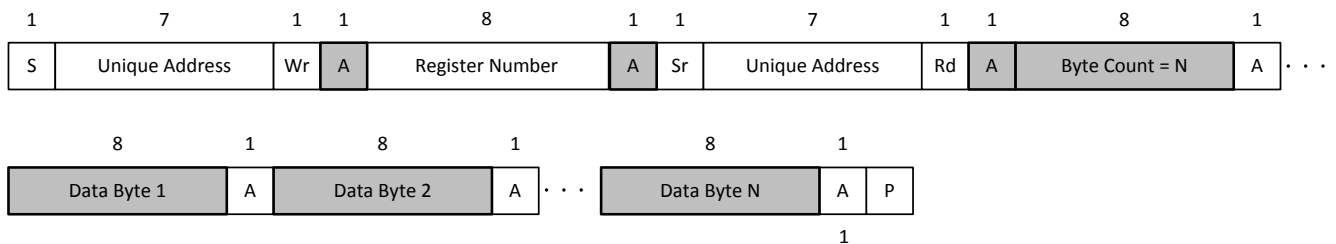
(1) See [Pin Strapping to Configure Default Behavior](#) details about ADCIN1 and ADCIN2 decoding.

### 8.3.10.2.1.3 Unique Address Interface

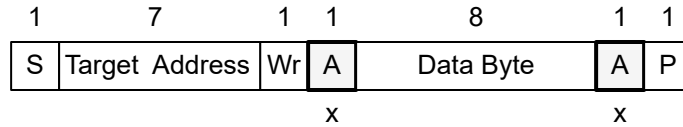
The Unique Address Interface allows for complex interaction between an I<sup>2</sup>C controller and a single TPS25751A. The I<sup>2</sup>C target sub-address is used to receive or respond to Host Interface protocol commands. [Figure 8-29](#) and [Figure 8-30](#) show the write and read protocol for the I<sup>2</sup>C target interface, and a key is included in [Figure 8-31](#) to explain the terminology used. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.



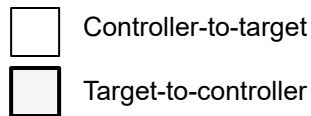
**Figure 8-29. I<sup>2</sup>C Unique Address Write Register Protocol**



**Figure 8-30. I<sup>2</sup>C Unique Address Read Register Protocol**



- S Start condition
- SR Repeated start condition
- Rd Read (bit value of 1)
- Wr Write (bit value of 0)
- X Field is required to have the value x
- A Acknowledge (this bit position is either 0 for an ACK or 1 for a NACK)
- P Stop condition



• • • Continuation of protocol

**Figure 8-31. I<sup>2</sup>C Read/Write Protocol Key**

**8.3.10.2.1.4 Pin Strapping to Configure Default Behavior**

During the boot procedure, the device reads the ADCINx pins and set the configurations based on the table below. The device then attempts to load a configuration from an external EEPROM on the I2Cc bus. If no EEPROM is detected, then the device waits for an external host to load a configuration.

When an external EEPROM is used, each device is connected to a unique EEPROM, and cannot be shared for multiple devices. The external EEPROM is set at 7-bit target address 0x50.

**Table 8-6. Device Configuration using ADCIN1 and ADCIN2**

ADCIN1 DECODED VALUE <sup>(2)</sup>	ADCIN2 DECODED VALUE <sup>(2)</sup>	I <sup>2</sup> C ADDRESS INDEX <sup>(1)</sup>	DEAD BATTERY BOOT CONFIGURATION
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded. This configuration is used with an external embedded controller. The embedded controller manages the battery charger in the system when present.
5	5	#2	
2	0	#3	
1	7	#4	
7	0	#1	SafeMode: The device does not enable the sink path. USB PD is disabled until configuration is loaded. Note that the configuration can put the device into a source-only mode. This is recommended when the application loads the patch from EEPROM. SafeMode is recommended when the PD controller manages the battery charger when present.
0	0	#2	
6	0	#3	
5	7	#4	

(1) See Table 8-5 to see the exact meaning of I<sup>2</sup>C Address Index.  
 (2) See Decoding of ADCIN1 and ADCIN2 for how to configure a given ADCINx decoded value.

### 8.3.11 Digital Core

Figure 8-32 shows a simplified block diagram of the digital core.

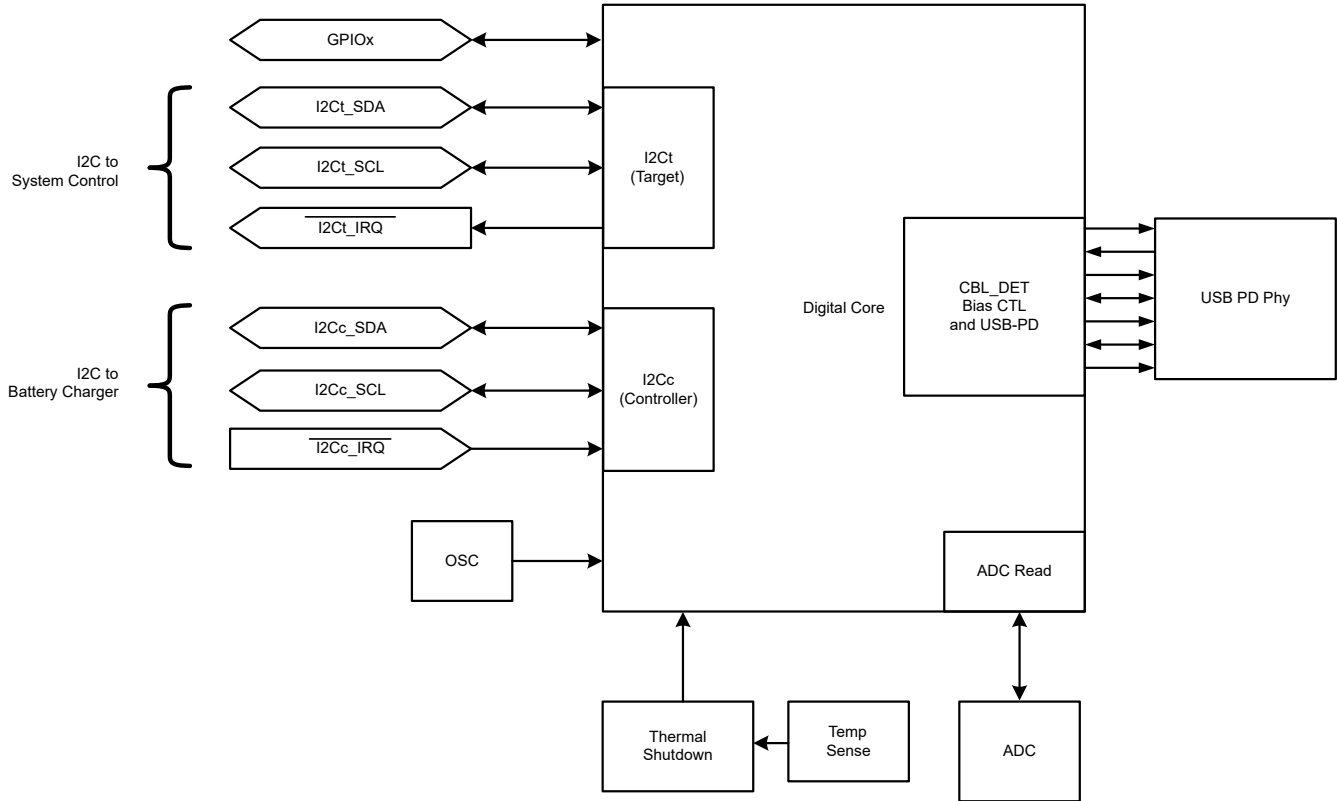


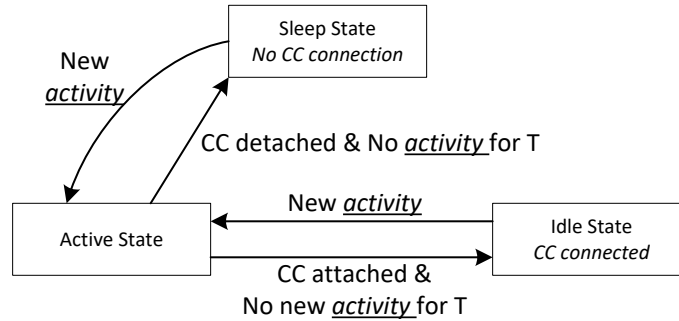
Figure 8-32. Digital Core Block Diagram

## 8.4 Device Functional Modes

### 8.4.1 Power States

The TPS25751A can operate in one of three different power states: Active, Idle, or Sleep. The Modern Standby mode is a special case of the Idle mode. The functionality available in each state is summarized in [Section 6.7](#). The device automatically transitions between the three power states based on the circuits that are active and required. See [Figure 8-33](#). In the Sleep state, the TPS25751A detects a Type-C connection. Transitioning between the Active mode to Idle mode requires a period of time (T) without any of the following activity:

- Incoming USB PD message
- Change in CC status
- GPIO input event
- I<sup>2</sup>C transactions
- Voltage alert
- Fault alert



**Figure 8-33. Flow Diagram for Power States**

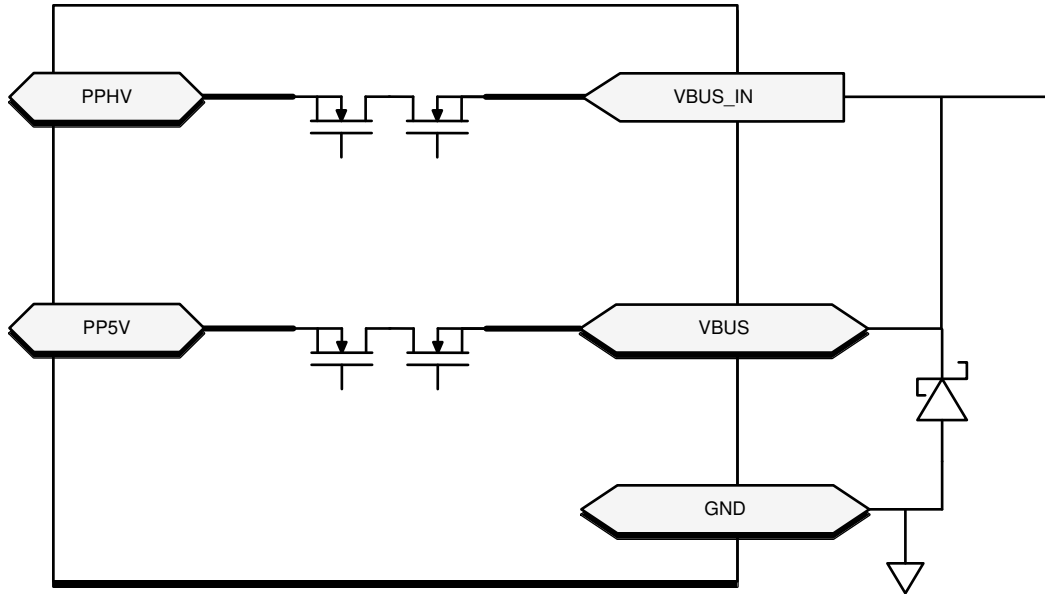
**Table 8-7. Power Consumption States**

	ACTIVE PP_5V SOURCE MODE <sup>(1)</sup>	ACTIVE PP_HV SOURCE MODE <sup>3</sup>	ACTIVE SINK MODE <sup>3</sup>	IDLE PP_5V SOURCE MODE	IDLE PP_HV SOURCE MODE	IDLE SINK MODE	SLEEP MODE <sup>2</sup>
PP_5V	Enabled	Disabled	Disabled	Enabled	Disabled	Disabled	Disabled
PP_HV (TPS25751AD)	Disabled	Enabled	Enabled	Disabled	Enabled	Enabled	Disabled
PP_EXT (TPS25751AS)	Disabled	Enabled	Enabled	Disabled	Enabled	Enabled	Disabled
PP_CABLE	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Disabled
External CC1 Termination	Rd	Rd	Rp 3.0A	Rd	Rd	Rp 3.0A	Open
External CC2 Termination	Open	Open	Open	Open	Open	Open	Open

- (1) This mode is used for:  $I_{VIN\_3V3,ActSrc}$
- (2) This mode is used for:  $I_{VIN\_3V3,Sleep}$
- (3) This mode is used for:  $I_{VIN\_3V3,ActSnk}$

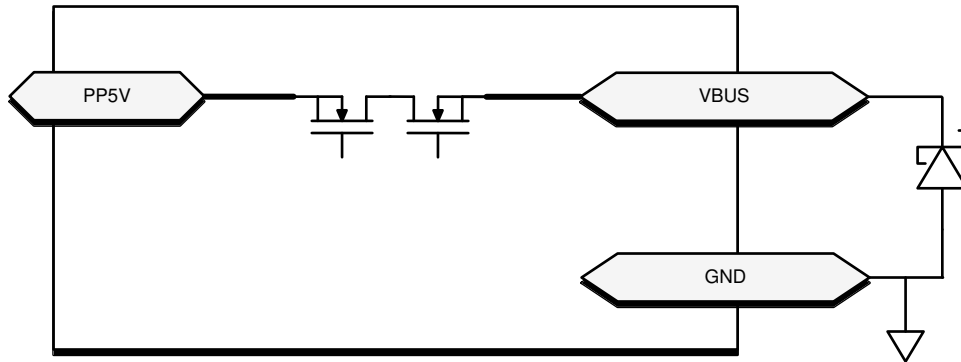
#### 8.4.2 Schottky for Current Surge Protection

To prevent the possibility of large ground currents into the TPS25751A during sudden disconnects due to inductive effects in a cable, TI recommends that a Schottky diode be placed from VBUS to ground.



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**Figure 8-34. TPS25751AD Schottky for Current Surge Protection**



**Figure 8-35. TPS25751AS Schottky for Current Surge Protection**

### 8.4.3 Thermal Shutdown

The TPS25751A features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all functions except for supervisory circuitry when die temperature goes above a rising temperature of  $T_{SD\_MAIN}$ . The temperature shutdown has a hysteresis of  $T_{SD\_MAIN}$  and when the temperature falls back below this value, the device resumes normal operation.

The power path thermal shutdown monitors the temperature of each internal PP5V-to-VBUS power path and disables both power paths and the VCONN power path when either exceeds  $T_{SD\_PP5V}$ . The temperature shutdown has a hysteresis of  $T_{SD\_PP5V}$  and when the temperature falls back below this value, the path can be configured to resume operation or remain disabled until re-enabled by firmware.

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS25751A is a stand-alone Type-C PD controller for power-only USB-PD applications. The [USBPD Application Customization Tool](#) provides a graphical interface for configuring the TPS25751A including power role, data role, battery charger integration, GPIO, and liquid detection. The Web Tool generates a binary image that is programmed onto the device during boot. The PD controller loads the device configuration from an external EEPROM or MCU through the I<sup>2</sup>C interface.

The TPS25751A is applicable in single port power applications supporting the following PD architectures.

- Designs for both Power Provider (Source) and Power Consumer (Sink)
- Designs for Power Consumer (Sink)

### 9.2 Typical Application

The following block diagrams provide an example of a complete system architecture; certain blocks may not be applicable in all designs.

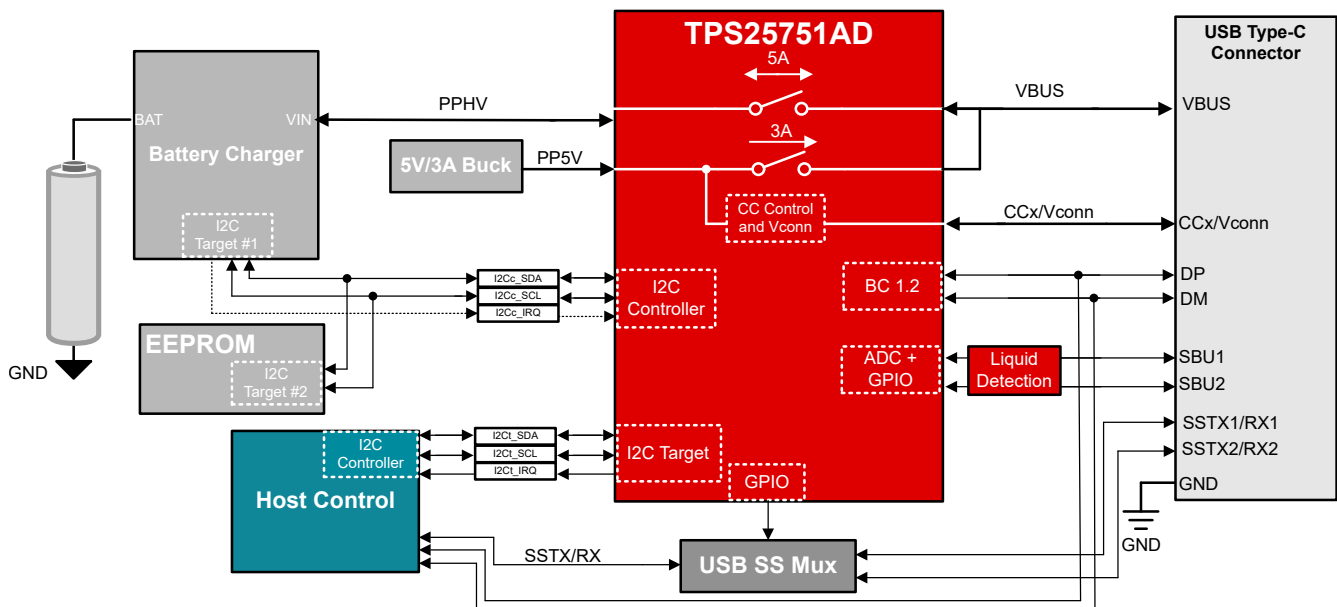


Figure 9-1. TPS25751AD Battery Charger and Full System Block Diagram

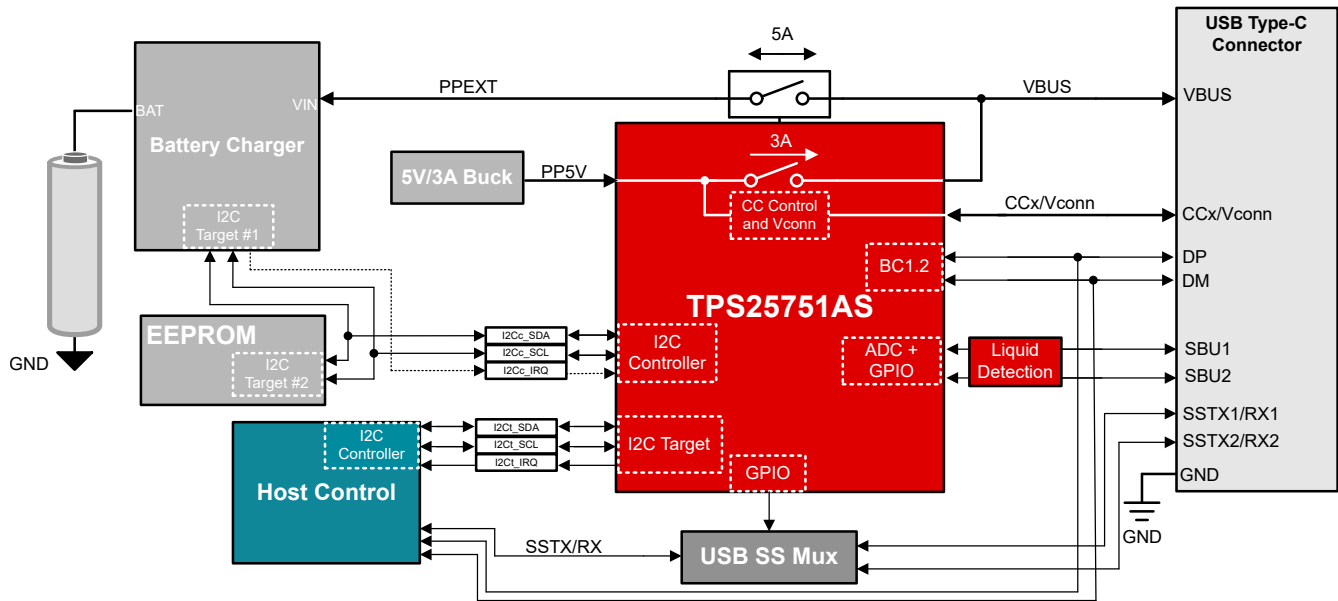


Figure 9-2. TPS25751AS Battery Charger and Full System Block Diagram

## 9.2.1 Design Requirements

### 9.2.1.1 Liquid Detection Design Requirements

Liquid detection is a safety and protection mechanism used in USB Type-C ports to detect the presence of moisture or debris. The TPS25751A supports detecting liquid by measuring the leakage voltage between pins on the Type-C connector using dedicated internal ADC pins. Table 9-1 shows examples of various shorts that can occur in both connected and unconnected states.

Table 9-1. Liquid Detection Resistive Short Examples

Resistor	Description
RSaV	Resistive short to VBUS
RSaCC	Resistive short to CC
RSaG	Resistive short to GND

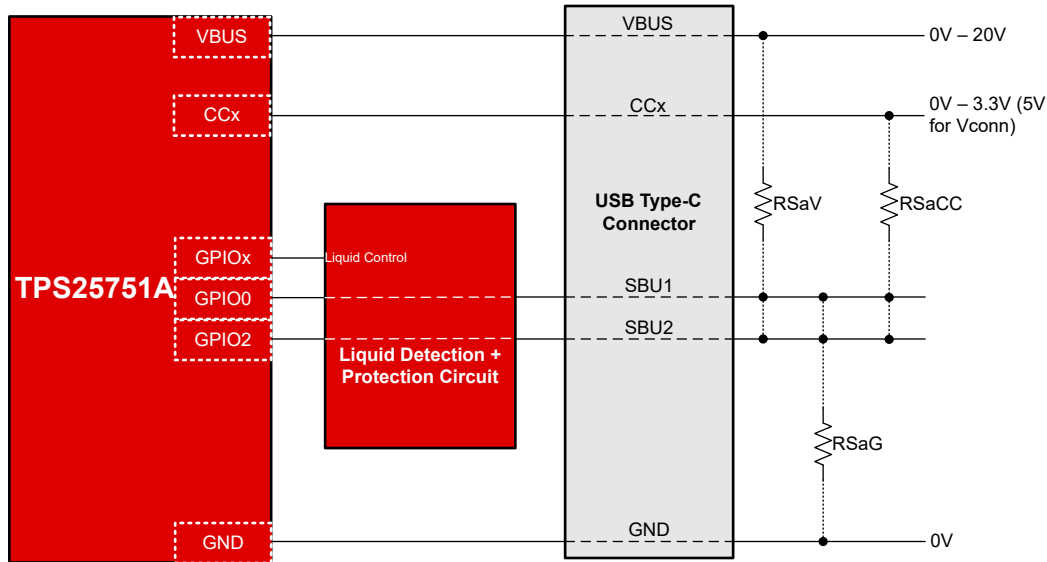


Figure 9-3. Liquid Detection Cases

### 9.2.1.2 BC1.2 Application Design Requirements

The PD controller uses the USB D+ and D- pins to provide BC1.2 detection and advertisement. The USB D+ and D- are connected to the USB Host (DFP) or USB Device (UFP) from the Type-C connector for Charging Data Port applications.

### 9.2.1.3 USB Data Support Design Requirements

For USB3 operation, the SSTX/RX are muxed to the Type-C connector. A SuperSpeed Mux generally has two control signals; enable and plug orientation. The PD controller determines when a connection is detected and drives the required GPIO to control the SuperSpeed Mux.

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Liquid Detection

The TPS25751A supports liquid detection using the built-in internal ADC and GPIO with external circuitry. [TPS25751A Liquid Detection Block Diagram - CC1 and CC2 Monitor Pins](#) and [TPS25751A Liquid Detection Block Diagram - SBU1 and SBU2 Monitor Pins](#) show the hardware implementation using CC1/2 and SBU1/2 pins for liquid detection with the TPS25751A. The [TPD4S201](#) is used to protect the ADC pins from over voltage conditions when there is liquid shorting VBUS to the monitoring pins. When liquid is detected, the TPS25751A takes action to protect the Type-C port. Systems using an embedded host controller can leverage the Host Interface for additional notification and control.

Table 9-2. Liquid Detection GPIO Pin Function

Pin	Function
GPIO0 and GPIO2	Internal ADC to measure the biased voltage on the monitoring pins.
GPIOx	Output GPIO that controls the biasing voltage that drives the monitoring pins High and Low.
GPIOy	Input GPIO that initiates Type-C Error Recovery when a fault is detected by the protection device.

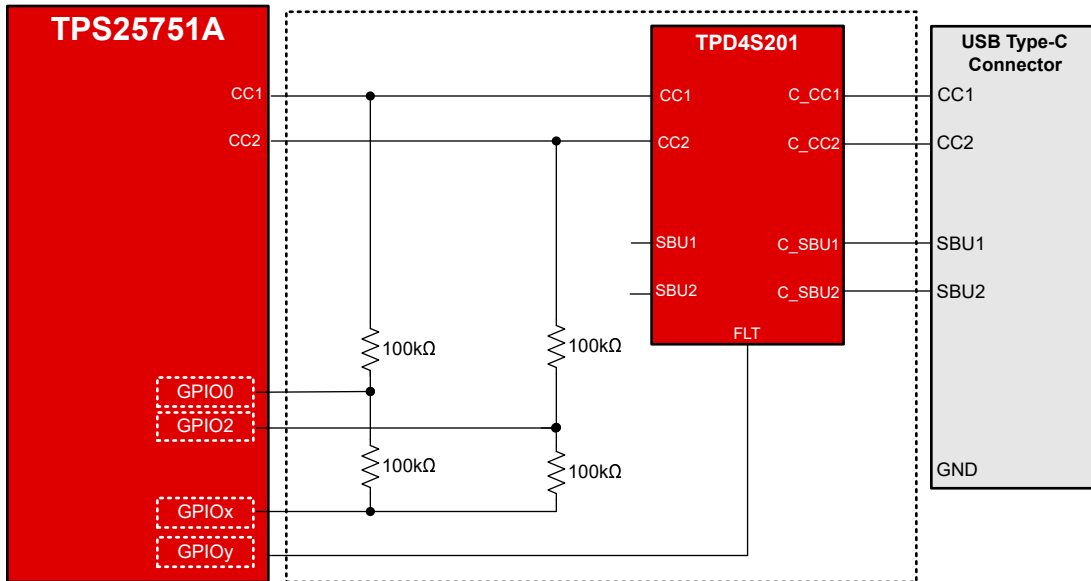


Figure 9-4. TPS25751A Liquid Detection Block Diagram - CC1 and CC2 Monitor Pins

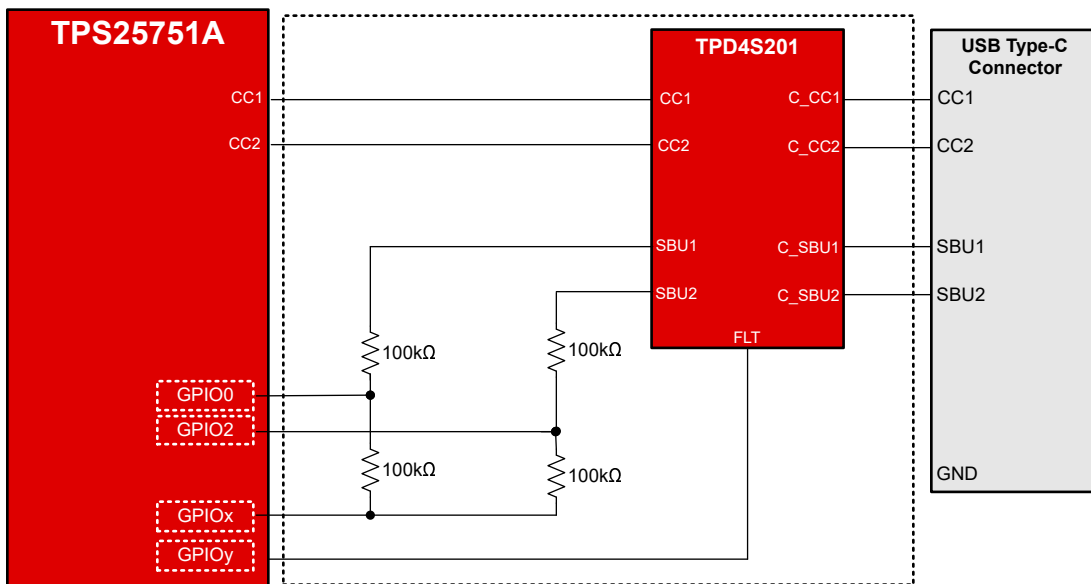


Figure 9-5. TPS25751A Liquid Detection Block Diagram - SBU1 and SBU2 Monitor Pins

### 9.2.2.2 BC1.2 Application

The TPS25751A supports BC1.2 detection and advertisement modes and are configurable through the [Web Tool](#).

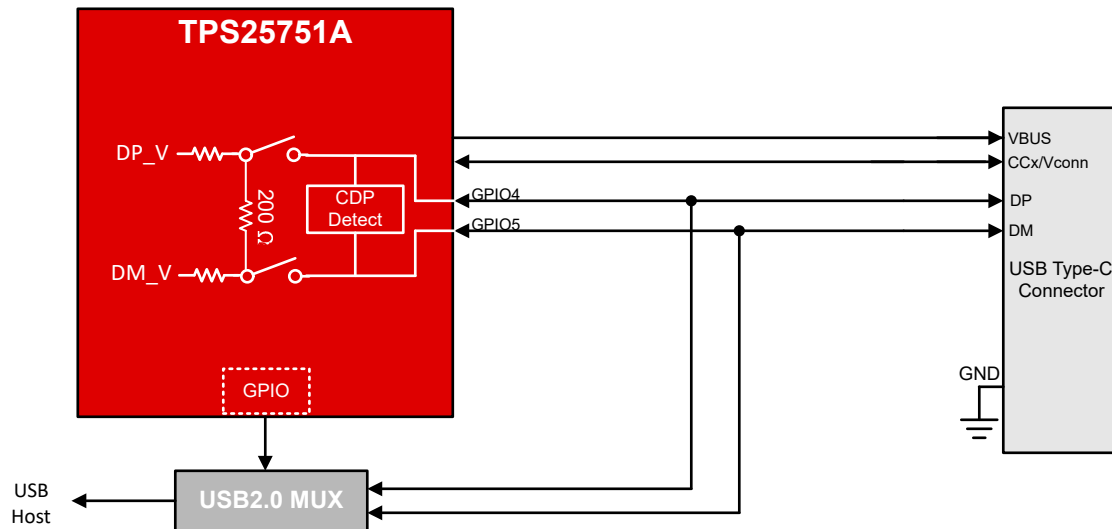


Figure 9-6. BC1.2 Application Block Diagram

### 9.2.2.3 USB Data Support

The TPS25751A supports USB data speed up to USB 3.2Gen 2. When entering USB enumeration, the TPS25751A controls USB SuperSpeed Mux ([TUSB1142](#)) using GPIO controls. The GPIO control is configured through using the [Application Customization Tool](#), GPIO events are found in the [Technical Reference Manual](#).

### 9.2.3 Application Curves

#### 9.2.3.1 Liquid Detection Application Curves

The figures below show the liquid detection behavior with corrosion mitigation disabled and enabled. Liquid is detected on both [Liquid Detection Behavior - No Corrosion Mitigation](#) and [Liquid Detection Behavior - Corrosion Mitigation](#) on the SBU2 pin. The number of samples, timing, and hysteresis voltage range of liquid detection is configurable through the [Web Tool](#).

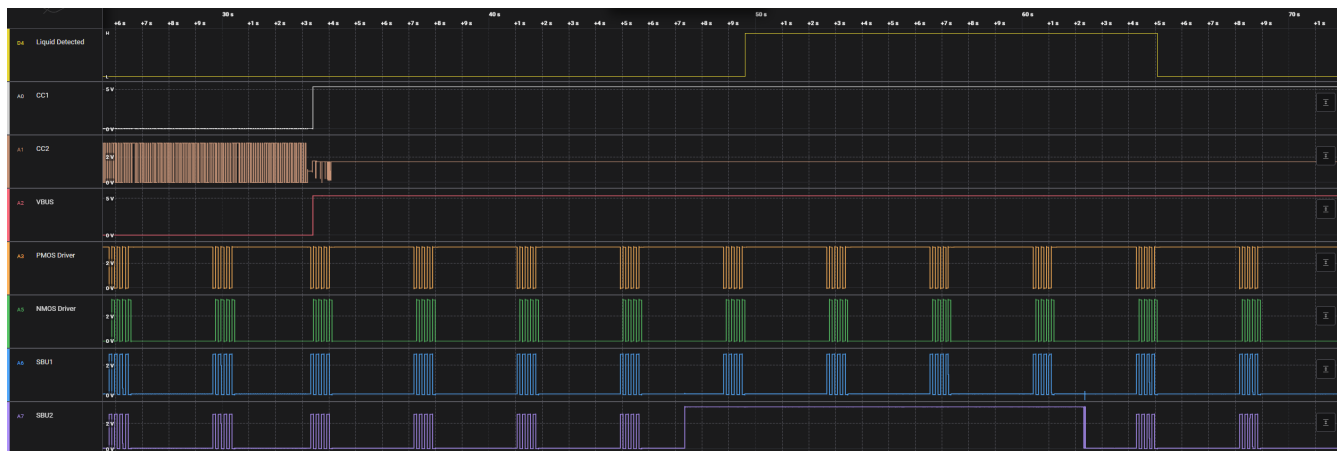


Figure 9-7. Liquid Detection Behavior - No Corrosion Mitigation

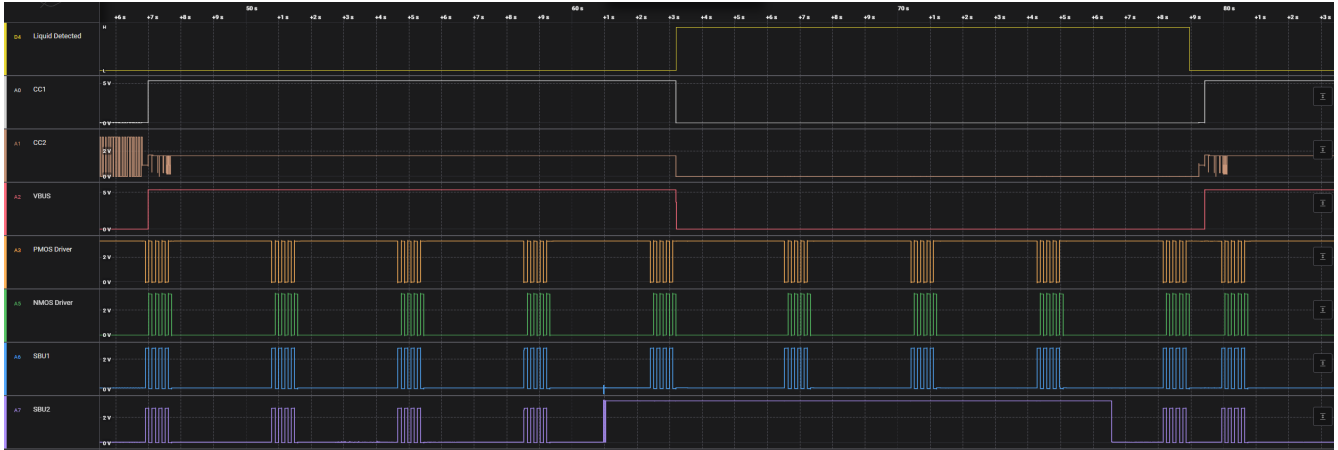


Figure 9-8. Liquid Detection Behavior - Corrosion Mitigation

### 9.2.3.2 BC1.2 Application Curves

The plots below show the BC1.2 advertisement and detection with the TPS25751A.

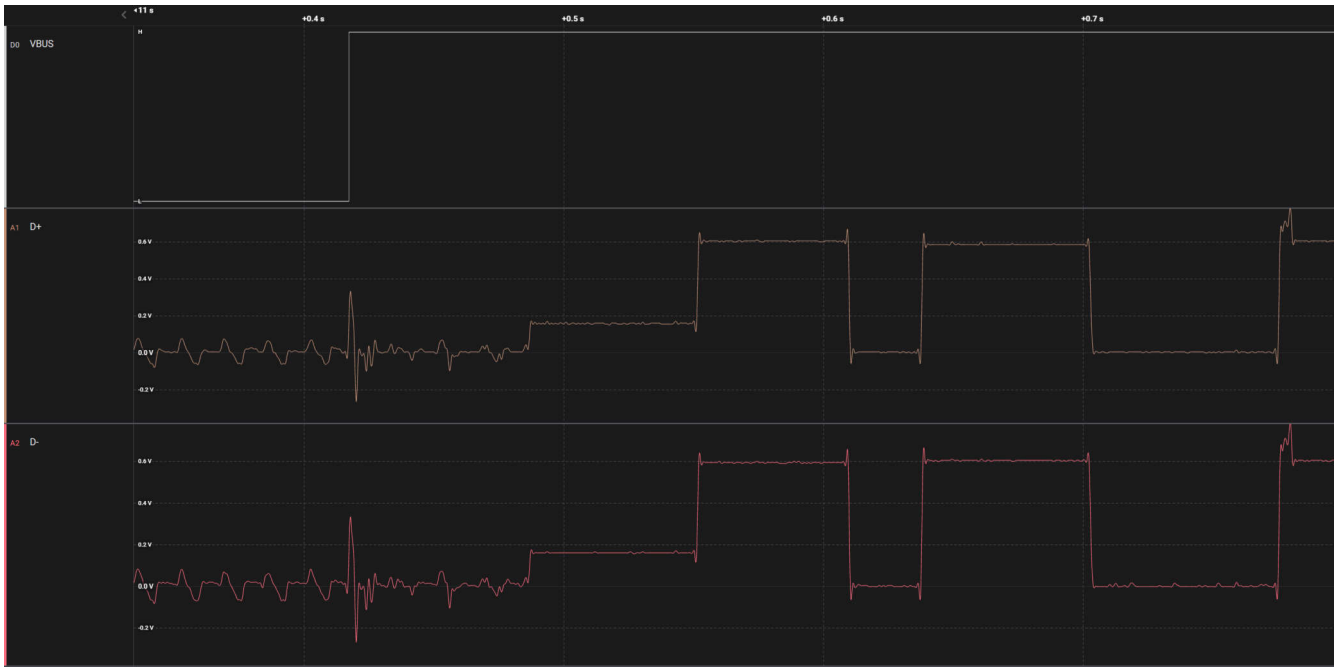


Figure 9-9. BC1.2 DCP Advertisement

### 9.2.3.2 BC1.2 Application Curves (continued)

The plots below show the BC1.2 advertisement and detection with the TPS25751A.

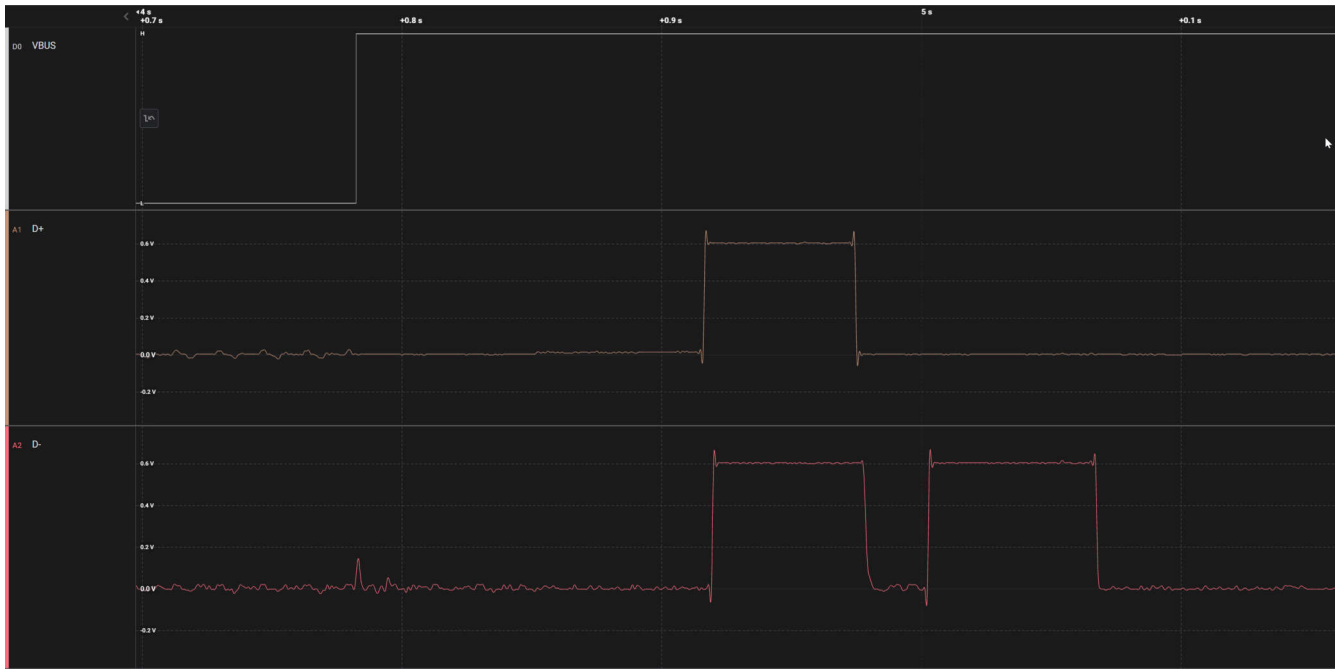


Figure 9-10. BC1.2 CDP Advertisement

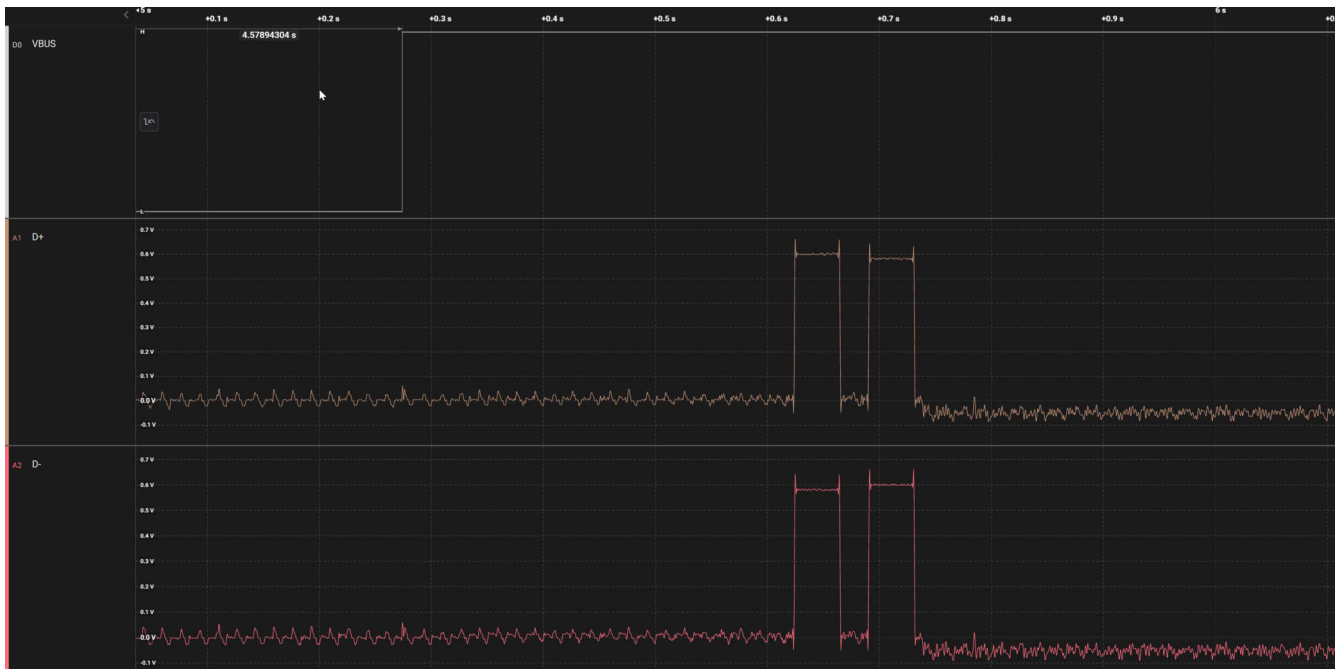


Figure 9-11. BC1.2 DCP Detection

### 9.2.3.2 BC1.2 Application Curves (continued)

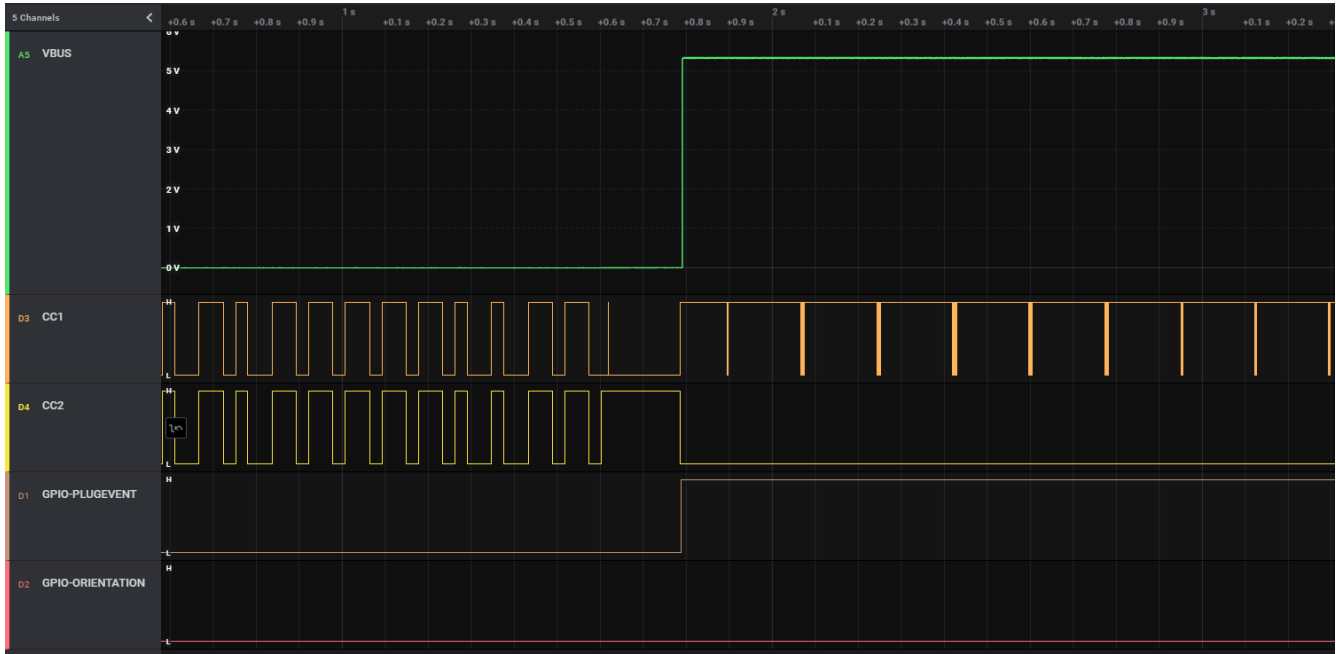
The plots below show the BC1.2 advertisement and detection with the TPS25751A.



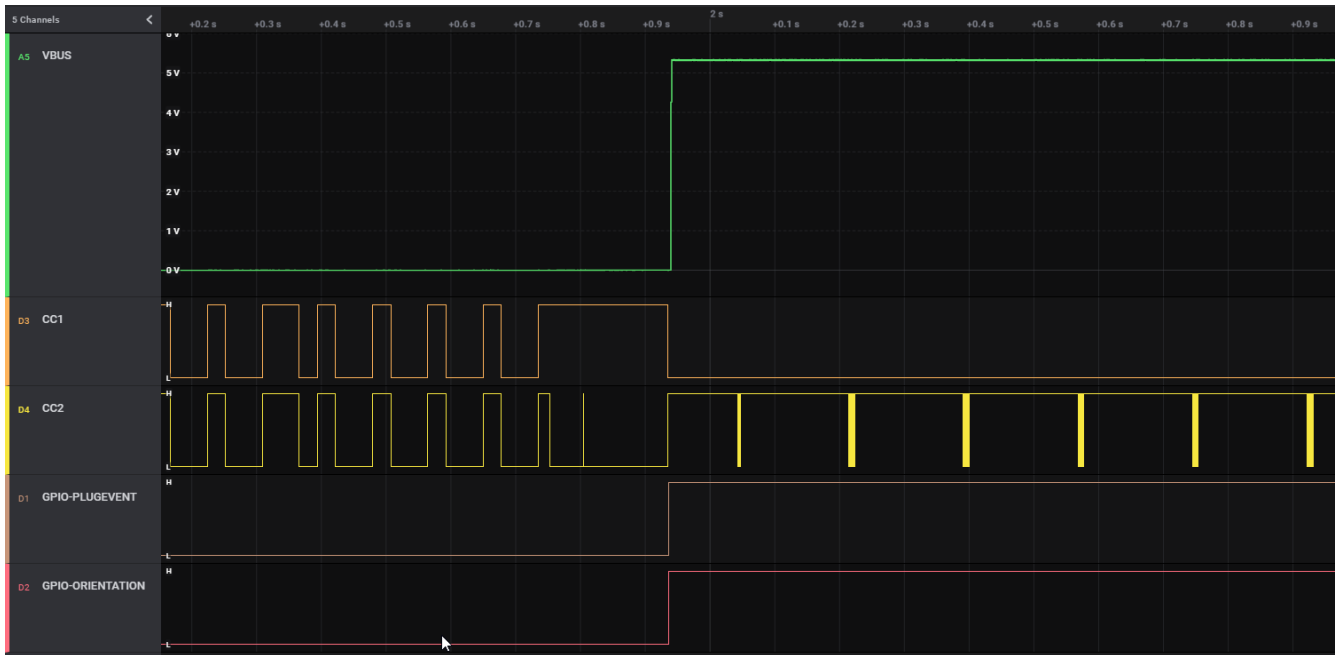
Figure 9-12. BC1.2 CDP Detection

### 9.2.3.3 USB Data Support Application Curves

The following show the control signals used by a USB SuperSpeed Mux. For a normal orientation, the CC1 pin is connected. For a flipped orientation, the CC2 pin is connected.



**Figure 9-13. USB SuperSpeed Mux Control - Normal Orientation**



**Figure 9-14. USB SuperSpeed Mux Control - Flipped Orientation**

## 9.3 Power Supply Recommendations

### 9.3.1 3.3V Power

#### 9.3.1.1 VIN\_3V3 Input Switch

The VIN\_3V3 input is the main supply of the TPS25751A device. The VIN\_3V3 switch (see [Section 8.3.2](#)) is a uni-directional switch from VIN\_3V3 to LDO\_3V3, not allowing current to flow backwards from LDO\_3V3 to VIN\_3V3. This switch is on when the 3.3V supply is available and the dead battery flag is cleared. The recommended capacitance  $C_{VIN\_3V3}$  (see [Section 6.4](#)) must be connected from the VIN\_3V3 pin to the GND pin. Do not power VIN\_3V3 from VBUS.

### 9.3.2 1.5V Power

The internal circuitry is powered from 1.5V. The 1.5V LDO steps the voltage down from LDO\_3V3 to 1.5V. The 1.5V LDO provides power to all internal low-voltage digital circuits which includes the digital core and memory. The 1.5V LDO also provides power to all internal low-voltage analog circuits. Connect the recommended capacitance  $C_{LDO\_1V5}$  (see [Section 6.4](#)) from the LDO\_1V5 pin to the GND pin.

### 9.3.3 Recommended Supply Load Capacitance

[Section 6.4](#) lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowed for tolerances and voltage derating ensuring proper operation.

## 9.4 Layout

### 9.4.1 TPS25751AD - Layout

#### 9.4.1.1 Layout Guidelines

Proper routing and placement maintain signal integrity for high speed signals and improve the heat dissipation from the power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. Best practice is to consult with board manufacturing to verify manufacturing capabilities.

##### 9.4.1.1.1 Recommended Via Size

Proper via stitching is recommended to carrying current for the VBUS power paths and grounding. The recommended minimum via size is shown below, but larger vias are an option for low density PCB designs. A single via is capable of carrying 1A, verify the tolerance with the board manufacturing. Vias are recommended to be tented when located close to the PD controller.

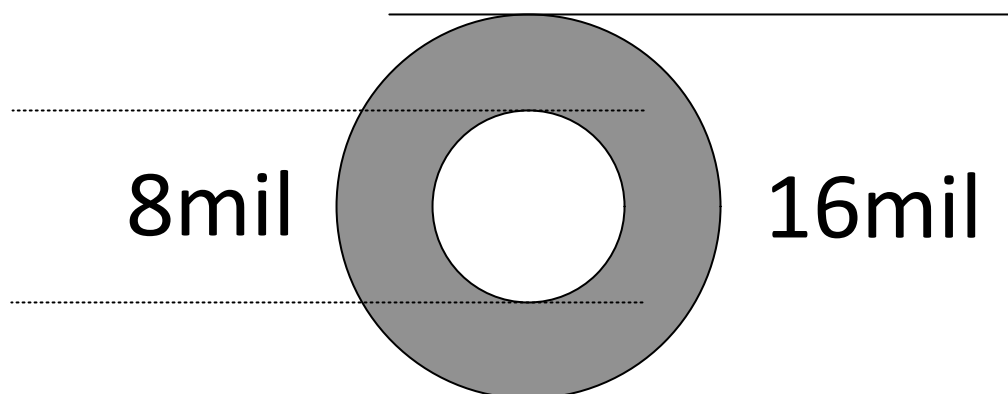


Figure 9-15. Recommend Minimum Via Size

##### 9.4.1.1.2 Minimum Trace Widths

Below are the minimum trace widths for analog and digital pins. The trace width limitations are also defined by the board manufacturing process used. Consult with manufacturing for determining the minimum trace widths and tolerance.

**Table 9-3. Minimum Trace Width**

Route	Minimum Width (mils)
CC1, CC2	10
VIN_3V3, LDO	10
Component GND	16
GPIO	4

### 9.4.1.2 Layout Example

#### 9.4.1.2.1 TPS25751AD Schematic Layout Example

Follow the differential impedances for Super / High Speed signals defined by their specifications (USB2.0). All I/O are fanned out to provide an example for routing out all pins, not all designs utilize all of the I/O on the TPS25751AD.

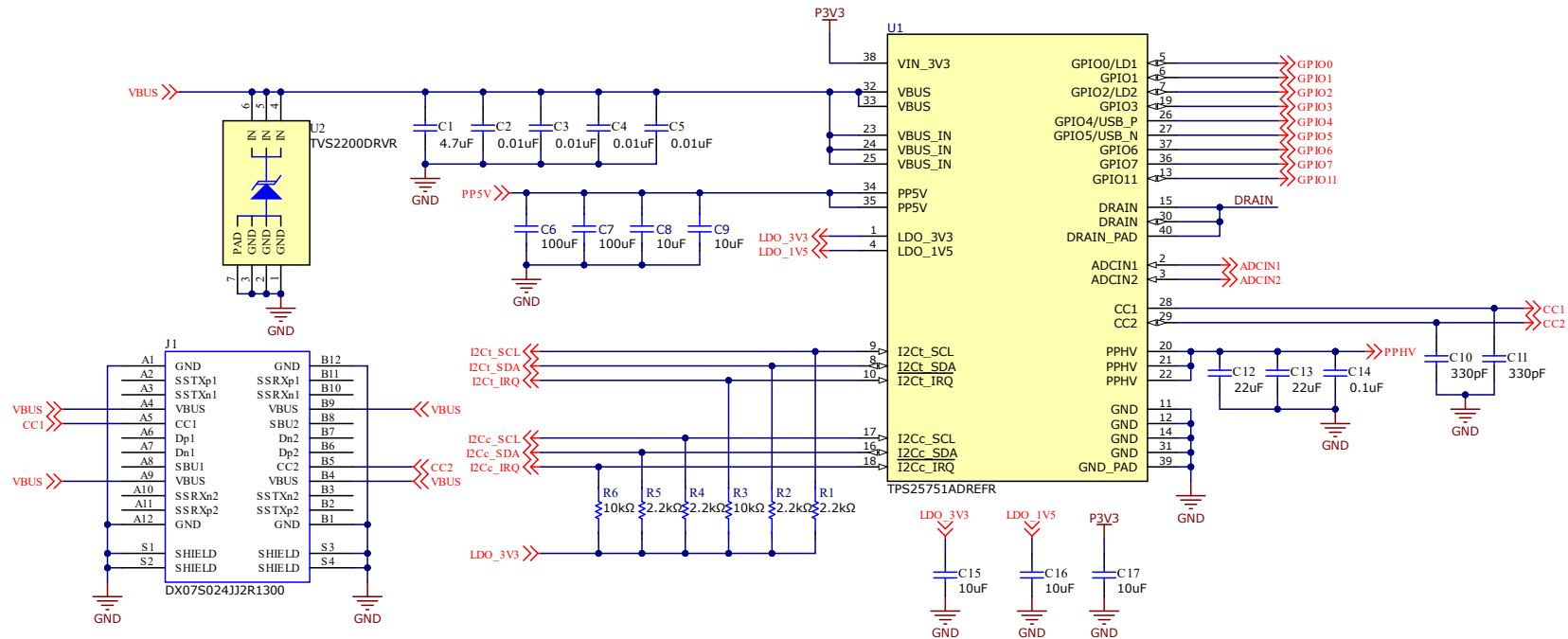


Figure 9-16. TPS25751AD Example Schematic

#### 9.4.1.2.2 TPS25751AD Layout Example - PCB Plots

The following TPS25751AD PCB Layout figures show the recommended layout, placement, and routing.

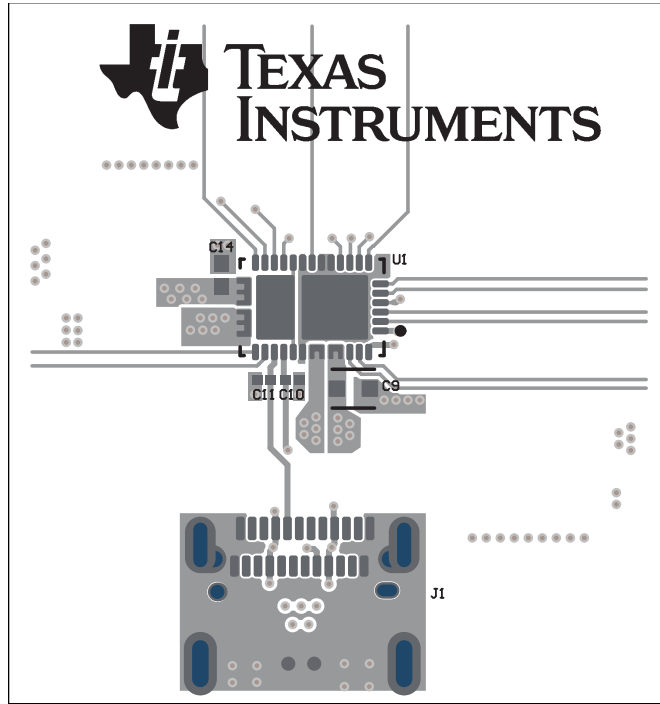


Figure 9-17. TPS25751AD PCB Layout - Top Composite

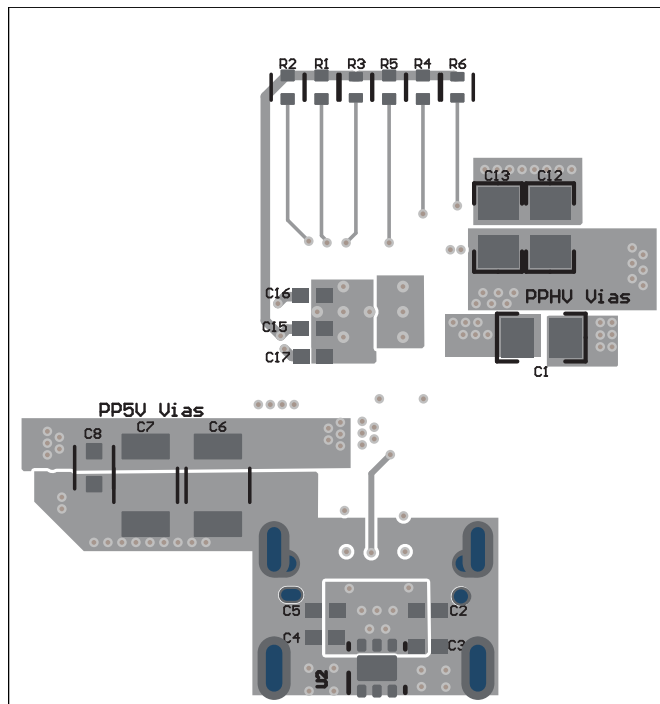


Figure 9-18. TPS25751AD PCB Layout - Bottom Composite

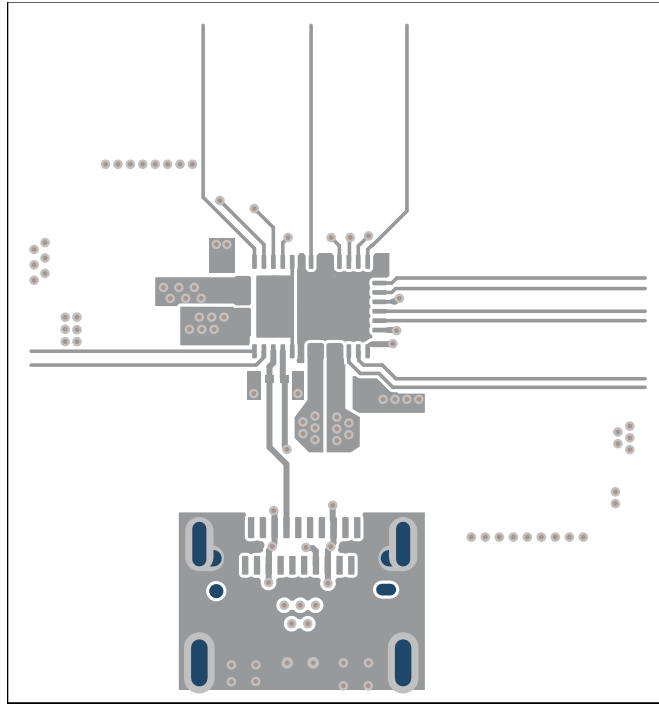


Figure 9-19. TPS25751AD PCB Layout - Top Layer Routing

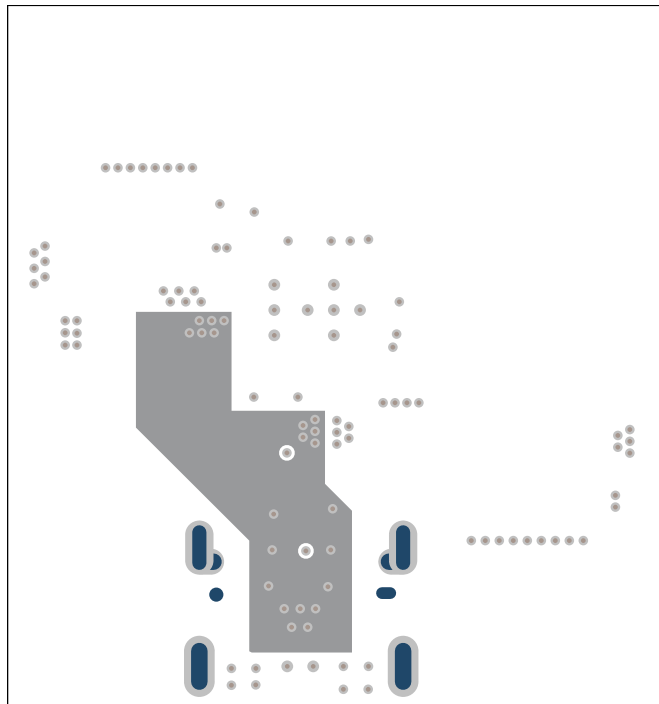
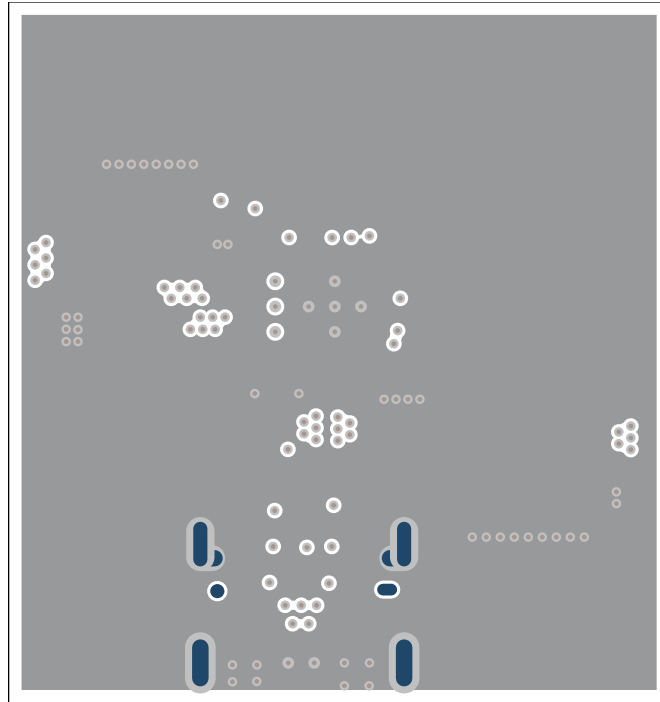
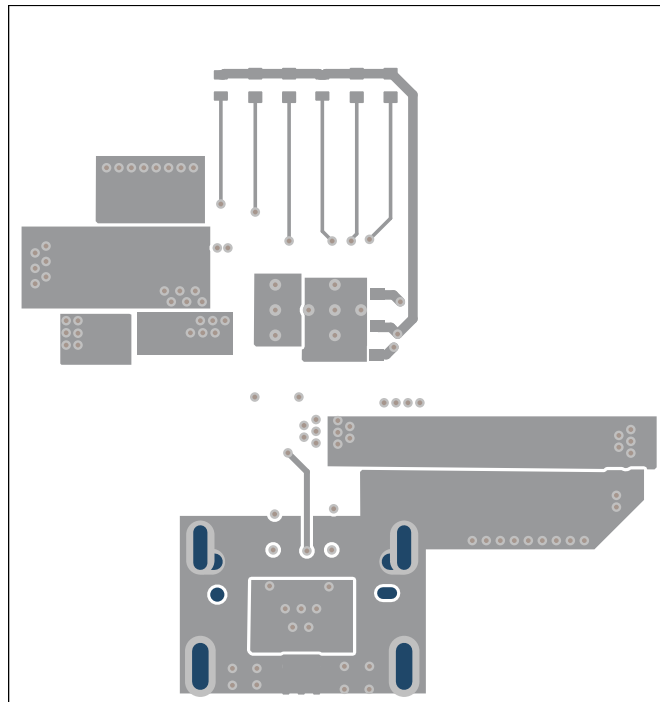


Figure 9-20. TPS25751AD PCB Layout - Internal Power Layer



**Figure 9-21. TPS25751AD PCB Layout - GND Layer**



**Figure 9-22. TPS25751AD PCB Layout - Bottom Layer**

#### 9.4.1.2.2.1 TPS25751AD Component Placement

##### LDO\_1V5 (pin 4), LDO\_3V3 (pin 1), and VIN\_3V3 (pin 38)

The decoupling capacitors for LDO\_3V3, LDO\_1V5, and VIN\_3V3 (C15, C16, and C17 respectively) need to be placed as close as possible to TPS25751AD device for optimal performance. To minimize solution size, the decoupling capacitors are placed on the bottom layer with their ground pads directly underneath the ground pad of TPS25751AD. Use a maximum of one via per pin from TPS25751AD to the decoupling capacitors if placed on a different layer. Use a minimum of 10mil trace width to route these three traces, preferably with 16mil trace width if possible.

##### CC1 (pin 28) and CC2 (pin 29)

CC1 (C11) and CC2 (C10) capacitors need to be placed as close as possible to their respective pins and on the same layer as the TPS25751AD device. When routing the CCx traces, DO NOT via to another layer in between the CCx pins of the TPS25751AD to the CCx capacitors. Check to make sure the CCx capacitors are not placed outside the CC trace creating an antenna, instead have the traces pass directly through the CCx capacitor pads as shown in the example layout (refer to TPS25751AD PCB Layout - Top Composite). Use a minimum of 10mil trace width to enable Vconn support (5V/0.6A).

#### 9.4.1.2.2.2 TPS25751AD PP5V

The 10uF decoupling capacitor (C9) need to be placed as close as possible to the PP5V pins of TPS25751AD. DO NOT use traces for PP5V. The PP5V power plane needs to be sized to support up to 3.6A (up to 3A for sourcing, 600mA for Vconn). When connecting the PP5V pins (pins 34 and 35) to the 5V power plane, use a minimum of 4 vias in parallel and close to the device to improve current sharing. Minimize the bottle necks cause by other vias or traces, large bottle necks reduces the efficiency of the power plane.

The bulk capacitors (C6, C7, and C8) represent capacitances from the system 5V rail, these are placed further away from TPS25751AD on the same PP5V power plane. Refer to [Figure 9-17](#) and [Figure 9-18](#) for placement and trace reference.

#### 9.4.1.2.2.3 TPS25751AD PPHV

Place the PPHV decoupling capacitors (C12, C13, and C14) as close as possible to TPS25751AD, these do not need to be on the same layer as the device. The PPHV power plane needs to be sized to support up to 5A of current. When connecting the PPHV plane to a different layer, use a minimum of 6 vias in parallel per layer change. It is highly recommended to have more than 6 vias if possible for layer change to improve current sharing and efficiency.

#### 9.4.1.2.2.4 TPS25751AD VBUS

##### VBUS (pins 32 and 33) and VBUS\_IN (pins 23, 24, and 25)

Place the VBUS decoupling capacitor (C1) as close as possible to TPS25751AD, the capacitor does not need to be on the same layer as the device. The VBUS power plane need to be sized to support up to 5A of current if 100W application is required. When connecting the VBUS pins (pins 32 and 33) plane to a different layer, use a minimum of 3 vias per layer change. When connecting the VBUS\_IN pins (pins 23, 24, and 25) plane to a different layer, use a minimum of 6 vias per layer change. Refer to [Figure 9-17](#) and [Figure 9-18](#) for capacitors and via placement.

At the Type-C port/connector, it is recommended to use minimum of 6 vias from the connector VBUS pins for layer changes. Place the 10nF caps (C2, C3, C4, and C5) and the 22V TVS diode (U2) as close as possible to the connector VBUS pins as shown in [Figure 9-18](#).

When routing the VBUS power plane from the Type-C connector to the TPS25751AD VBUS pins, minimize bottle necks caused by other vias and traces to improve current flow. [Figure 9-20](#) uses an internal layer to route the VBUS plane from the connector to TPS25751AD.

#### 9.4.1.2.2.5 TPS25751AD I/O (I2C, ADCINs, GPIOs)

##### I2C, ADCIN1/2, and GPIO pins

Fan these traces out from the TPS25751AD, use vias to connect the net to a routing layer if needed. For these nets, use 4mil to 10mil trace width.

#### **I2Cc\_SDA/SCL/IRQ (pins 8, 9, and 10) and I2Ct\_SCL/SDA/IRQ (pins 16, 17, and 18)**

Minimize trace width changes to avoid I2C communication issues.

#### **ADCIN1 and ADCIN2 (pins 2 and 3)**

Keep the ADCINx traces away from switching elements. If a resistor divider is used, place the divider close to LDO\_3V3 or LDO\_1V5.

#### **GPIO (pins 5, 6, 7, 19, 26, 27, 37, 36, and 13)**

Separate GPIO traces running in parallel by a trace width. Keep the GPIOx traces away from switching elements.

##### **9.4.1.2.2.6 TPS25751AD DRAIN**

The DRAIN pad is used to dissipate heat for the internal high voltage power path (PPHV). Connect the Drain pins (pins 15 and 30) to the Drain pad underneath the TPS25751AD device. Connect the through hole vias from the drain pad on the top layer to a copper pour on the bottom layer to help dissipate heat. Additional vias can be added to improve thermal dissipation.

##### **9.4.1.2.2.7 TPS25751AD GND**

The GND pad is used to dissipate heat for the TPS25751AD device. Connect the GND pins (pins 11, 12, 14 and 31) to the Ground pad underneath the TPS25751AD device. Connect the through hole vias from the ground pad on the top layer to a copper pour on the bottom layer to help dissipate heat. Additional vias can be added to improve thermal dissipation.

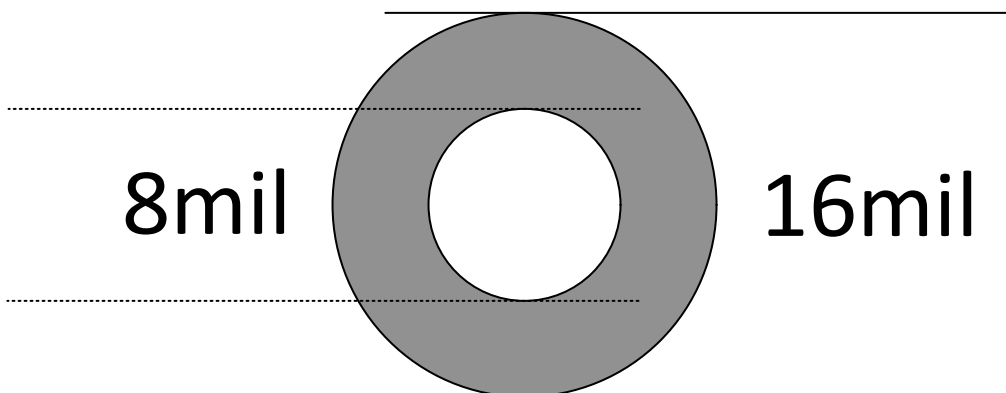
#### **9.4.2 TPS25751AS - Layout**

##### **9.4.2.1 Layout Guidelines**

Proper routing and placement maintain signal integrity for high speed signals and improve the heat dissipation from the power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. Best practice is to consult with board manufacturing to verify manufacturing capabilities.

##### **9.4.2.1.1 Recommended Via Size**

Proper via stitching is recommended to carrying current for the VBUS power paths and grounding. The recommended minimum via size is shown below, but larger vias are an option for low density PCB designs. A single via is capable of carrying 1A, verify the tolerance with the board manufacturing. Vias are recommended to be tented when located close to the PD controller.



**Figure 9-23. Recommend Minimum Via Size**

#### 9.4.2.1.2 Minimum Trace Widths

Below are the minimum trace widths for analog and digital pins. The trace width limitations are also defined by the board manufacturing process used. Consult with manufacturing for determining the minimum trace widths and tolerance.

**Table 9-4. Minimum Trace Width**

Route	Minimum Width (mils)
CC1, CC2	10
VIN_3V3, LDO	10
Component GND	16
GPIO	4

### 9.4.2.2 Layout Example

#### 9.4.2.2.1 TPS25751AS Schematic Layout Example

Follow the differential impedances for Super / High Speed signals defined by their specifications (USB2.0). All I/O are fanned out to provide an example for routing out all pins, not all designs utilize all of the I/O on the TPS25751AS.

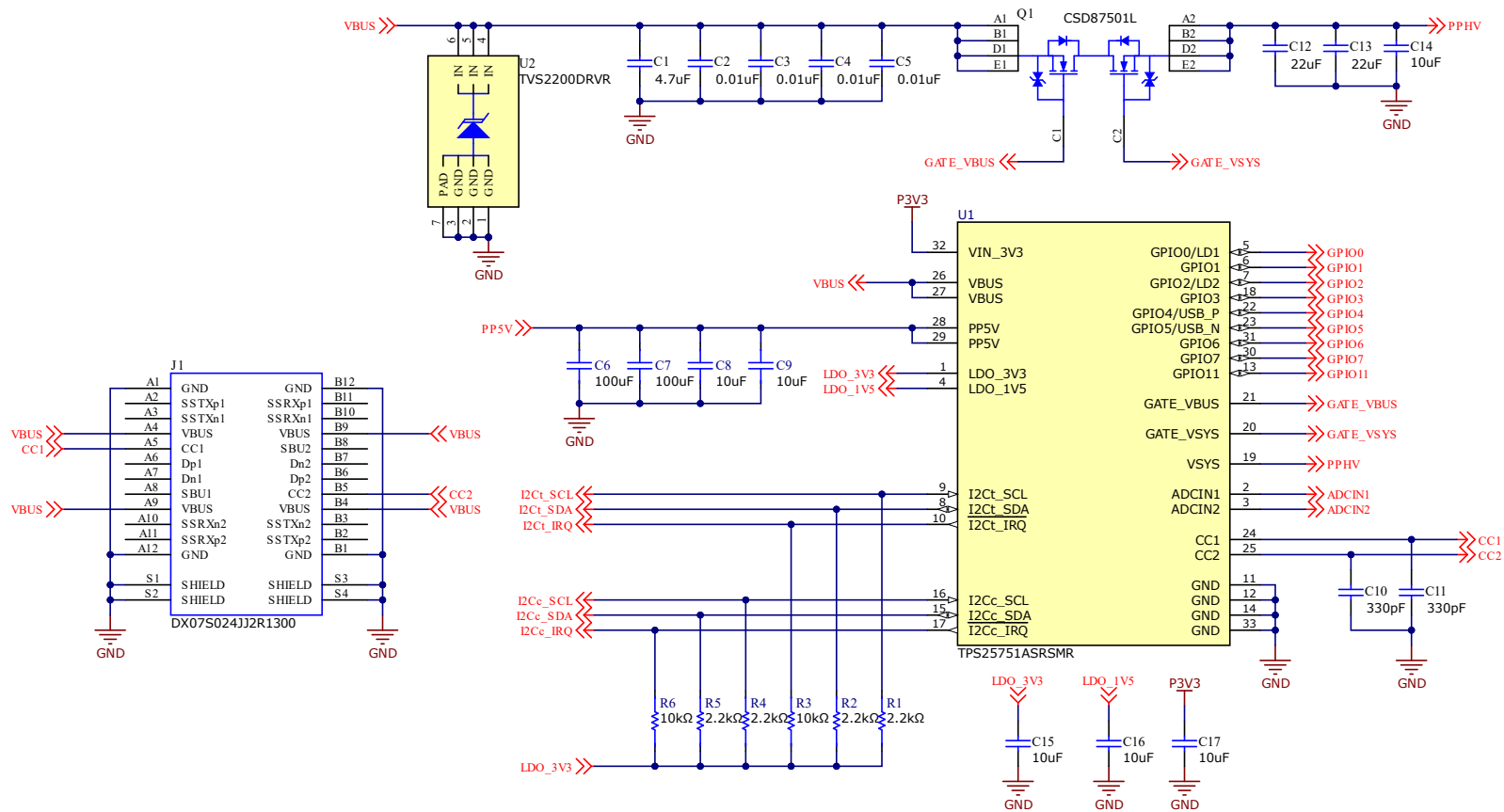


Figure 9-24. TPS25751AS Example Schematic

#### 9.4.2.2.2 TPS25751AS Layout Example - PCB Plots

The following TPS25751AS PCB Layout figures show the recommended layout, placement, and routing.

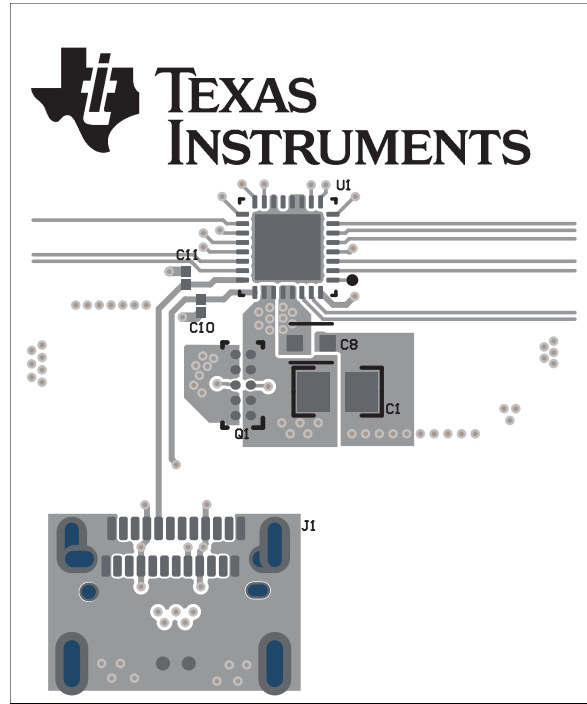


Figure 9-25. TPS25751AS PCB Layout - Top Composite

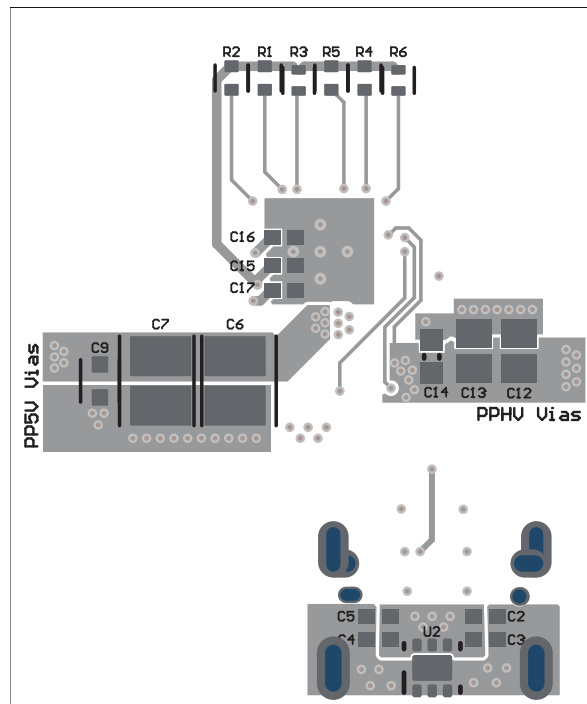
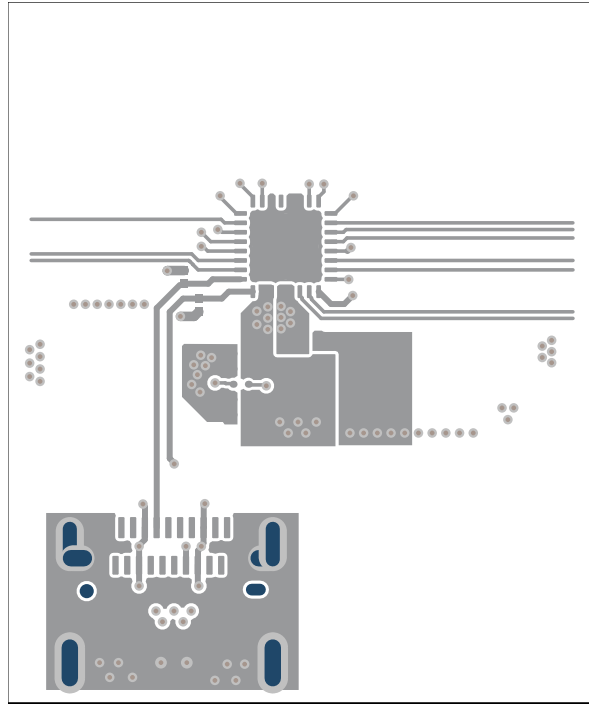
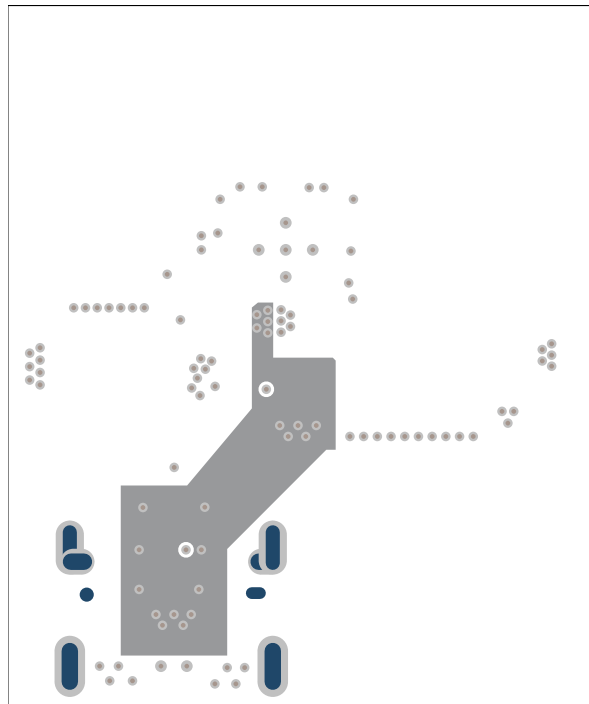


Figure 9-26. TPS25751AS PCB Layout - Bottom Composite



**Figure 9-27. TPS25751AS PCB Layout - Top Layer Routing**



**Figure 9-28. TPS25751AS PCB Layout - Internal Power Layer**

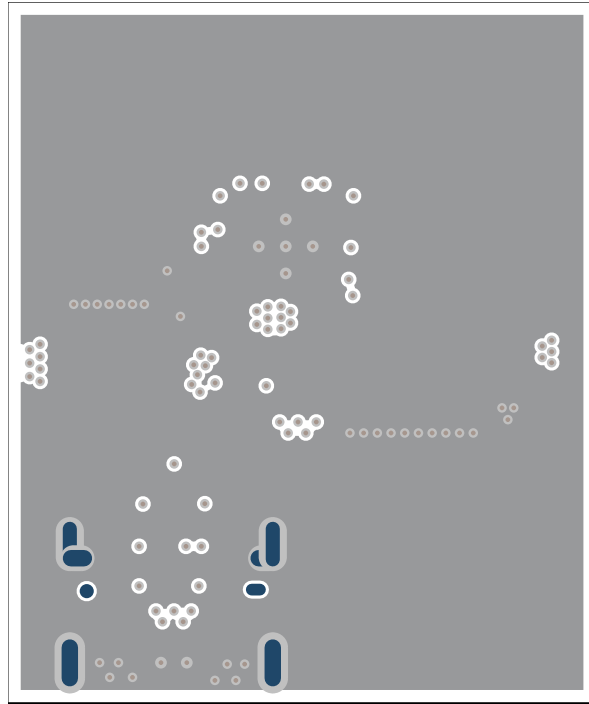


Figure 9-29. TPS25751AS PCB Layout - GND Layer

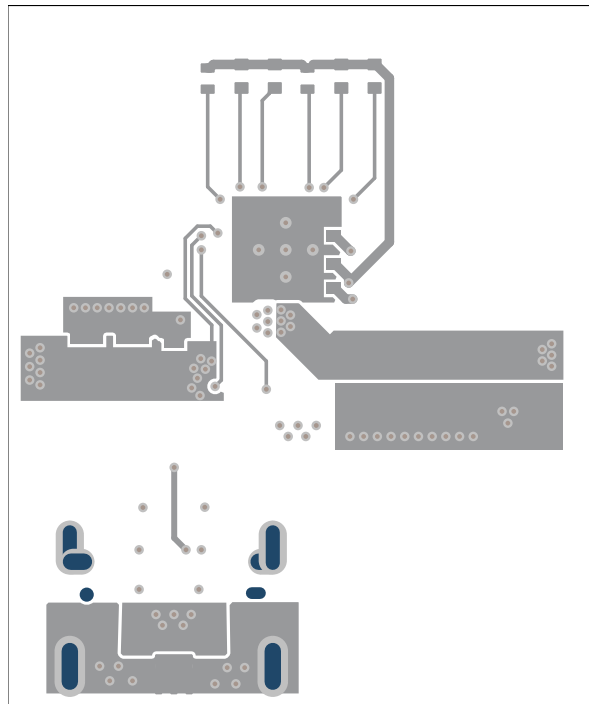


Figure 9-30. TPS25751AS PCB Layout - Bottom Layer

#### 9.4.2.2.2.1 TPS25751AS Component Placement

##### **LDO\_1V5 (pin 4), LDO\_3V3 (pin 1), and VIN\_3V3 (pin 32)**

The decoupling capacitors for LDO\_3V3, LDO\_1V5, and VIN\_3V3 (C15, C16, and C17 respectively) need to be placed as close as possible to TPS25751AS device for optimal performance. To minimize solution size, the decoupling capacitors are placed on the bottom layer with their ground pads directly underneath the ground pad of TPS25751AS. Use a maximum of one via per pin from TPS25751AS to the decoupling capacitors if placed on a different layer. Use a minimum of 10mil trace width to route these three traces, preferably with 16mil trace width if possible.

##### **CC1 (pin 24) and CC2 (pin 25)**

CC1 (C11) and CC2 (C10) capacitors need to be placed as close as possible to their respective pins and on the same layer as the TPS25751AS device. When routing the CCx traces, DO NOT via to another layer in between the CCx pins of the TPS25751AS to the CCx capacitors. Check to make sure the CCx capacitors are not placed outside the CC trace creating an antenna, instead have the traces pass directly through the CCx capacitor pads as shown in the example layout (refer to [Figure 9-25](#)). Use a minimum of 10mil trace width to enable Vconn support (5V/0.6A).

#### 9.4.2.2.2.2 TPS25751AS PP5V

The 10uF decoupling capacitor (C8) need to be placed as close as possible to the PP5V pins of TPS25751AS. DO NOT use traces for PP5V. The PP5V power plane needs to be sized to support up to 3.6A (up to 3A for sourcing, 600mA for Vconn). When connecting the PP5V pins (pins 28 and 29) to the 5V power plane, use a minimum of 4 vias in parallel and close to the device to improve current sharing. Minimize the bottle necks caused by other vias or traces, large bottle necks reduce the efficiency of the power plane. The bulk capacitors (C6, C7, and C9) represent capacitances from the system 5V rail, these are placed further away from TPS25751AS on the same PP5V power plane. Refer to [Figure 9-25](#) and [Figure 9-26](#) for placement and trace reference.

#### 9.4.2.2.2.3 TPS25751AS PP\_EXT

Place the PP\_EXT decoupling capacitors (C12, C13, and C14) as close as possible to TPS25751AS. These capacitors do not need to be on the same layer as the device. The PP\_EXT power plane needs to be sized to support up to 5A of current. When connecting the PP\_EXT plane to a different layer, use a minimum of 6 vias in parallel per layer change. It is highly recommended to have more than 6 vias if possible for layer change to improve current sharing and efficiency.

##### **VSYS (pin 19)**

The VSYS pin (pin 19) can be connected with a trace (recommended 6mil trace width) to any of the vias on the PPHV plane. It is recommended to connect to a via close to the source pin of the VSYS N-ch MOSFET (pins A2, B2, D2, and E2 of the Q1 FET in the example schematic) to improve reverse current sensing protection. Refer to the [Detailed Description for RCP](#) for additional information on RCP.

#### 9.4.2.2.2.4 TPS25751AS VBUS

##### **VBUS (pins 26 and 27)**

Place the VBUS decoupling capacitor (C1) as close as possible to TPS25751AS, the capacitor does not need to be on the same layer as the device. The VBUS power plane need to be sized to support up to 5A of current if 100W application is required. When connecting the VBUS pins (pins 26 and 27) plane to a different layer, use a minimum of 3 vias per layer change. When connecting the VBUS power plane to a different layer, use a minimum of 6 vias per layer change. Refer to [Figure 9-25](#) and [Figure 9-26](#) for capacitors and via placement.

At the Type-C port/connector, it is recommended to use minimum of 6 vias from the connector VBUS pins for layer changes. Place the 10nF caps (C2, C3, C4, and C5) and the 22V TVS diode (U2) as close as possible to the connector VBUS pins as shown in [Figure 9-26](#).

When routing the VBUS power plane from the Type-C connector to the TPS25751AS VBUS pins, minimize bottle necks caused by other vias and traces to improve current flow. The example layout shown in [Figure 9-28](#) to route the VBUS plane from the connector to TPS25751AS.

#### 9.4.2.2.2.5 TPS25751AS I/O

##### I2C, ADCIN1/2, and GPIO pins

Fan these traces out from the TPS25751AS, use vias to connect the net to a routing layer if needed. For these nets, use 4mil to 10mil trace width.

##### I2Cc\_SDA/SCL/IRQ (pins 8, 9, and 10) and I2Ct\_SCL/SDA/IRQ (pins 15, 16, and 17)

Minimize trace width changes to avoid I2C communication issues.

##### ADCIN1 and ADCIN2 (pins 2 and 3)

Keep the ADCINx traces away from switching elements. If a resistor divider is used, place the divider close to LDO\_3V3 or LDO\_1V5.

##### GPIO (pins 5, 6, 7, 13, 18, 22, 23, 30, and 31)

Separate GPIO traces running in parallel by a trace width. Keep the GPIOx traces away from switching elements.

#### 9.4.2.2.2.6 TPS25751AS PPEXT Gate Driver

##### GATE\_VSYS (pin 20)

The GATE\_VSYS pin (pin 20) can be connected with a trace (recommended 6mil trace width) to the gate pins of the N-ch MOSFET with source tied to PPHV. It is recommended to **NOT** via directly to the gate pin of the N-ch MOSFET, instead use via(s) to connect the GATE\_VSYS pin from the TPS25751AS to the gate pin of the N-ch MOSFET. Refer to [Figure 9-25](#) and [Figure 9-26](#) for examples on how to connect the traces.

##### GATE\_VBUS (pin 21)

The GATE\_VBUS pin (pin 21) can be connected with a trace (recommended 6mil trace width) to the gate pins of the N-ch MOSFET with source tied to VBUS. It is recommended to **NOT** via directly to the gate pin of the N-ch MOSFET, instead use via(s) to connect the GATE\_VBUS pin from the TPS25751AS to the gate pin of the N-ch MOSFET. Refer to [Figure 9-25](#) and [Figure 9-26](#) for examples on how to connect the traces.

#### 9.4.2.2.2.7 TPS25751AS GND

The GND pad is used to dissipate heat for the TPS25751AS device. Connect the GND pins (11, 12, and 14) to the Ground pad underneath the TPS25751AS device. Connect the through hole vias from the ground pad on the top layer to a copper pour on the bottom layer to help dissipate heat. Additional vias can be added to improve thermal dissipation.

## 10 Device and Documentation Support

### 10.1 Device Support

#### 10.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 10.2 Documentation Support

#### 10.2.1 Related Documentation

- [USB-PD Specifications](#)
- [USB Power Delivery Specification](#)

### 10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.4 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.5 Trademarks

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All trademarks are the property of their respective owners.

### 10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2026	*	Initial Release

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS25751ADREFR</a>	Active	Production	WQFN (REF)   38	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25751A D
<a href="#">TPS25751ASRSMR</a>	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25751A S

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

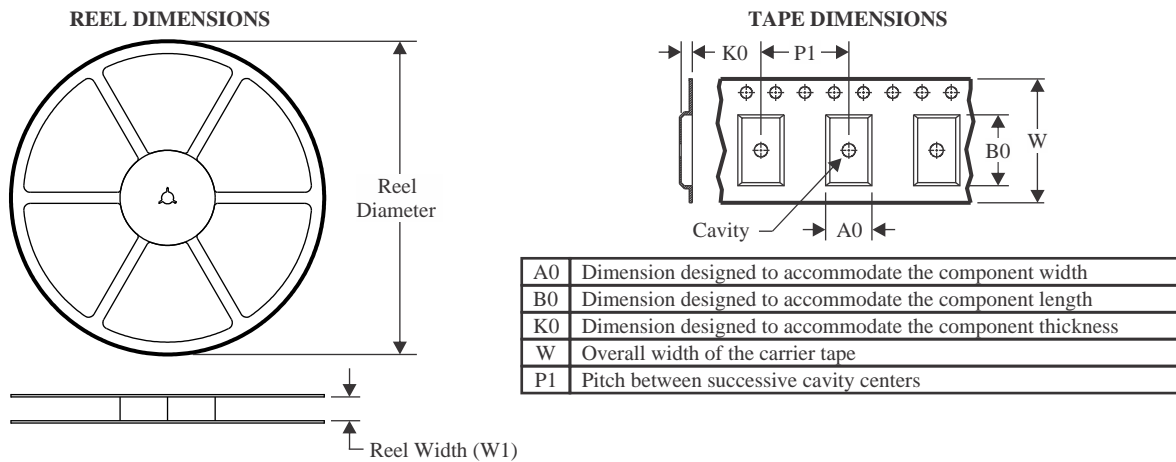
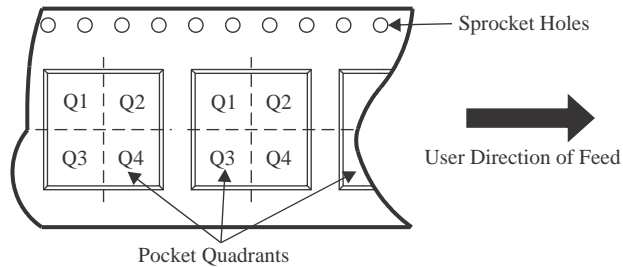
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


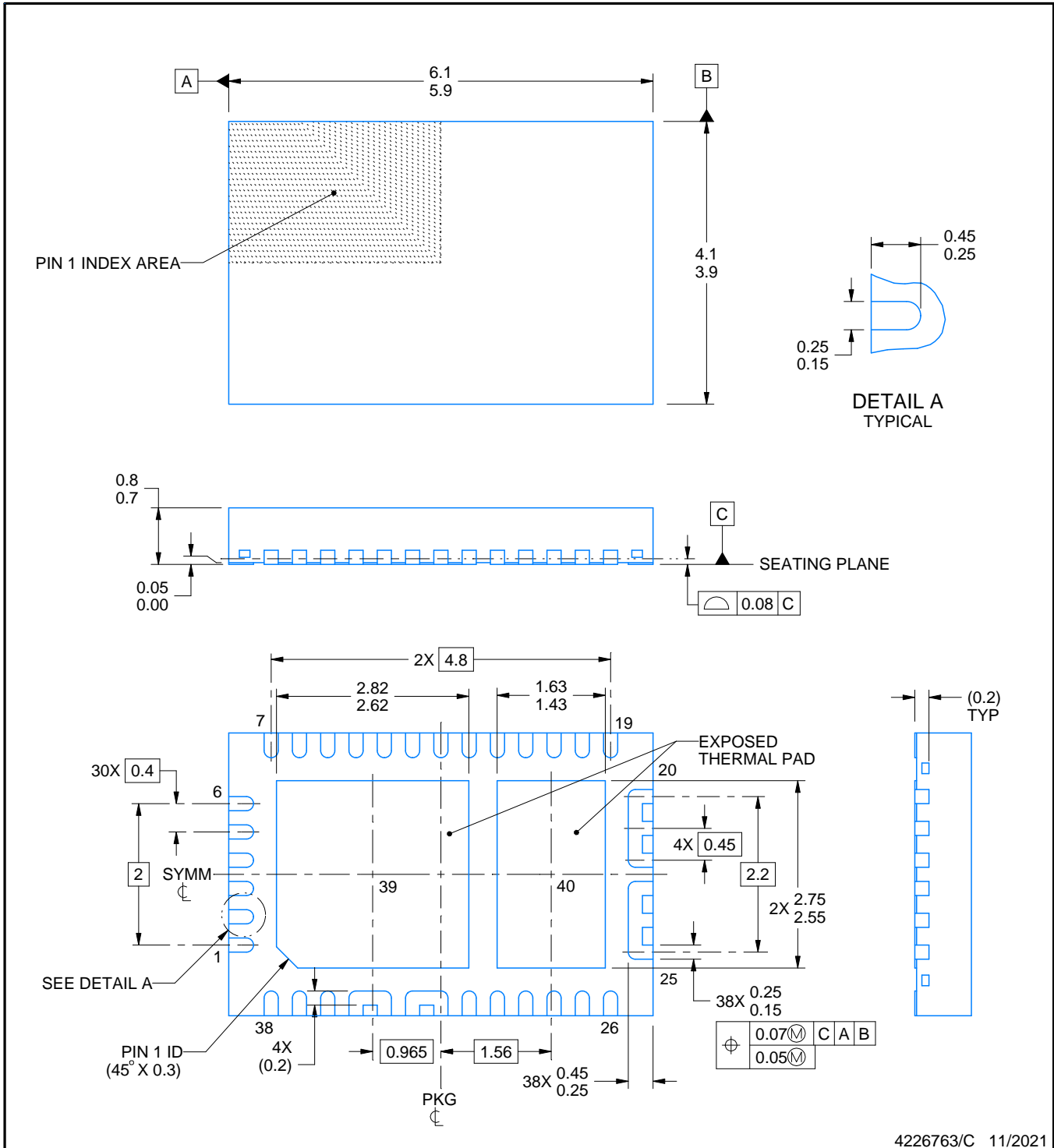
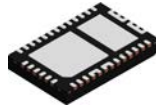
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25751ADREFR	WQFN	REF	38	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TPS25751ASRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25751ADREFR	WQFN	REF	38	3000	367.0	367.0	35.0
TPS25751ASRSMR	VQFN	RSM	32	3000	360.0	360.0	36.0



4226763/C 11/2021

NOTES:

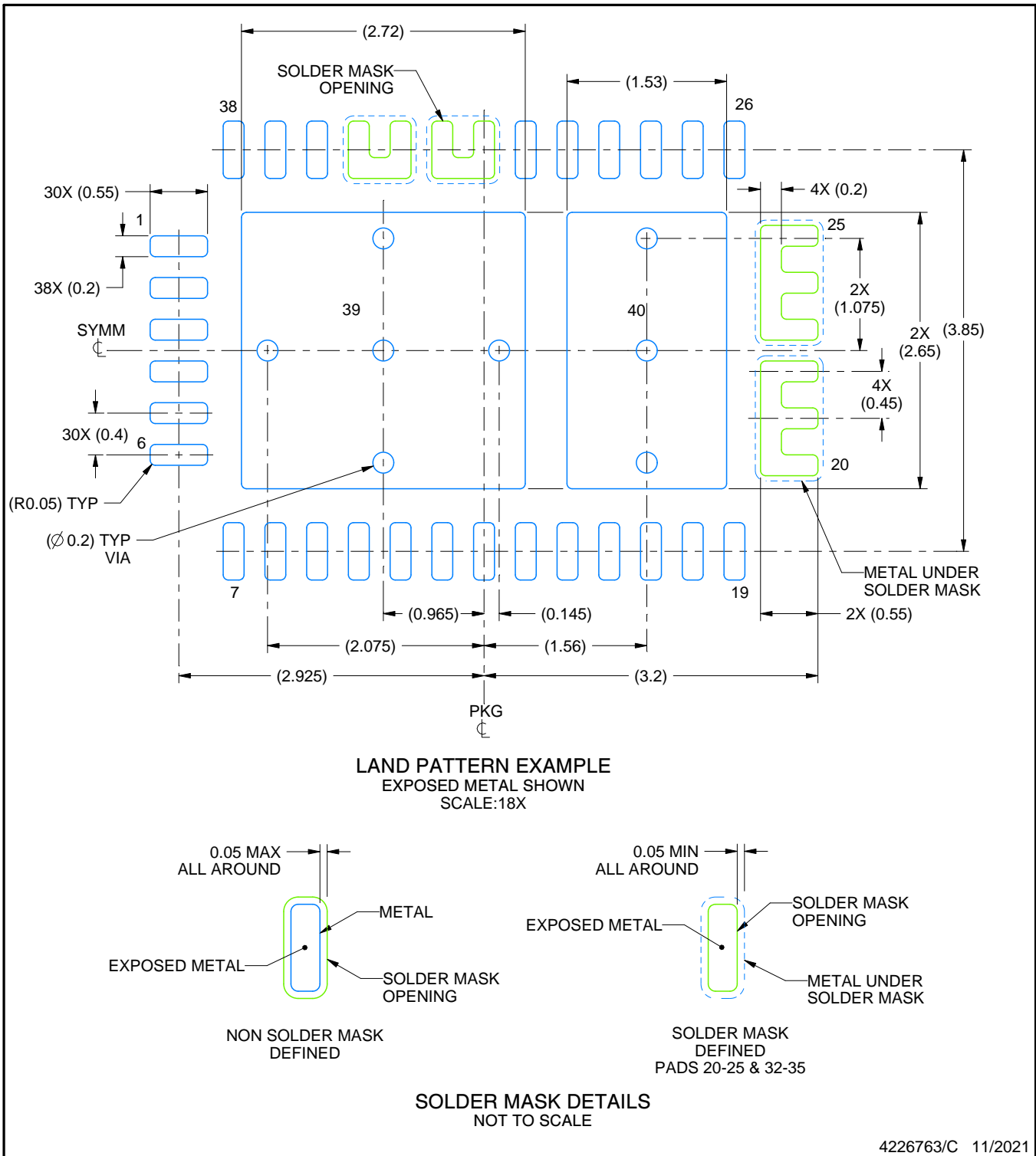
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

REF0038A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4226763/C 11/2021

NOTES: (continued)

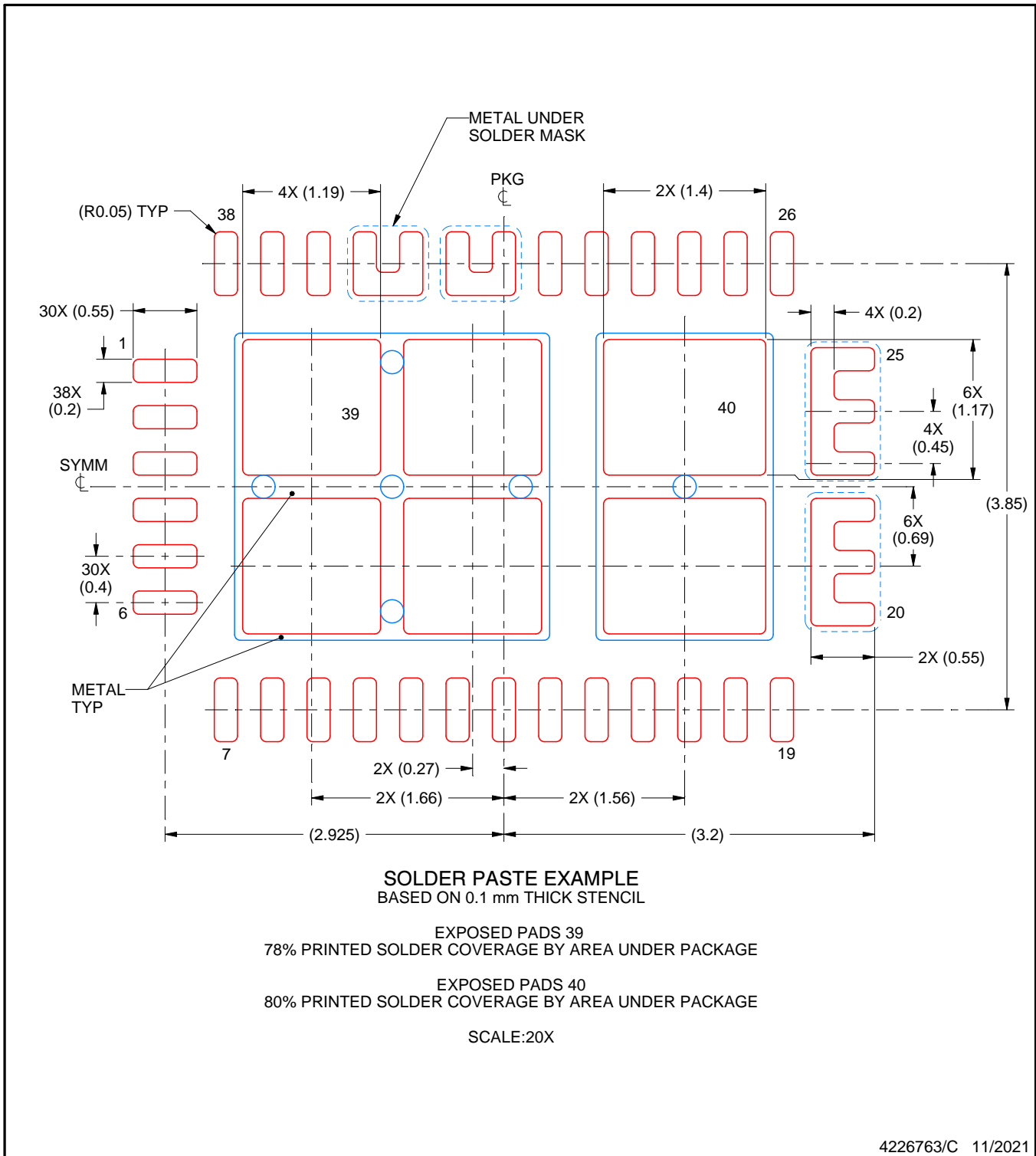
- This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

REF0038A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

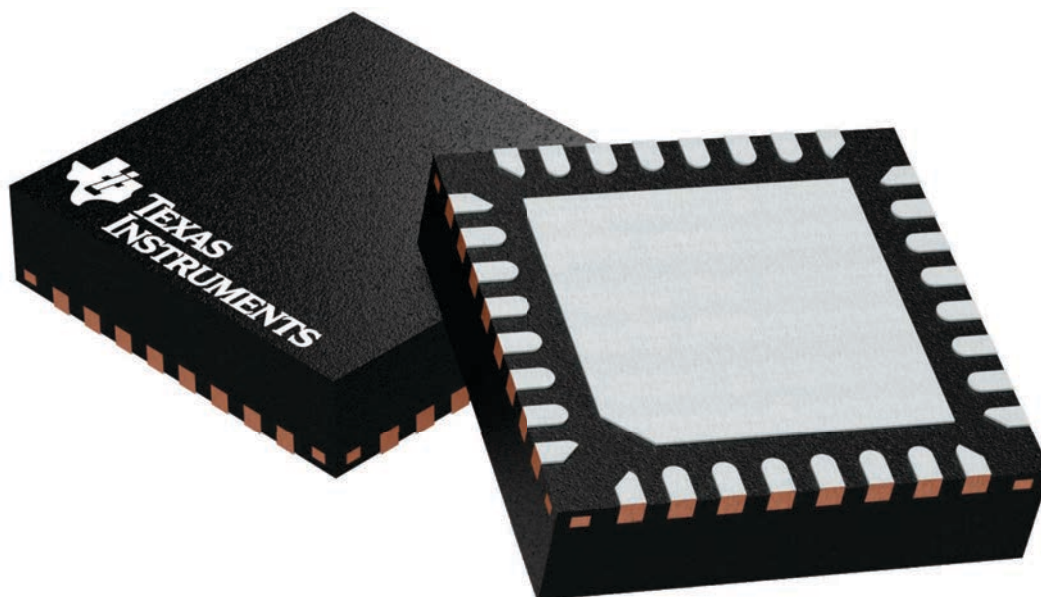
**RSM 32**

**VQFN - 1 mm max height**

4 x 4, 0.4 mm pitch

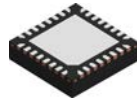
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224982/A

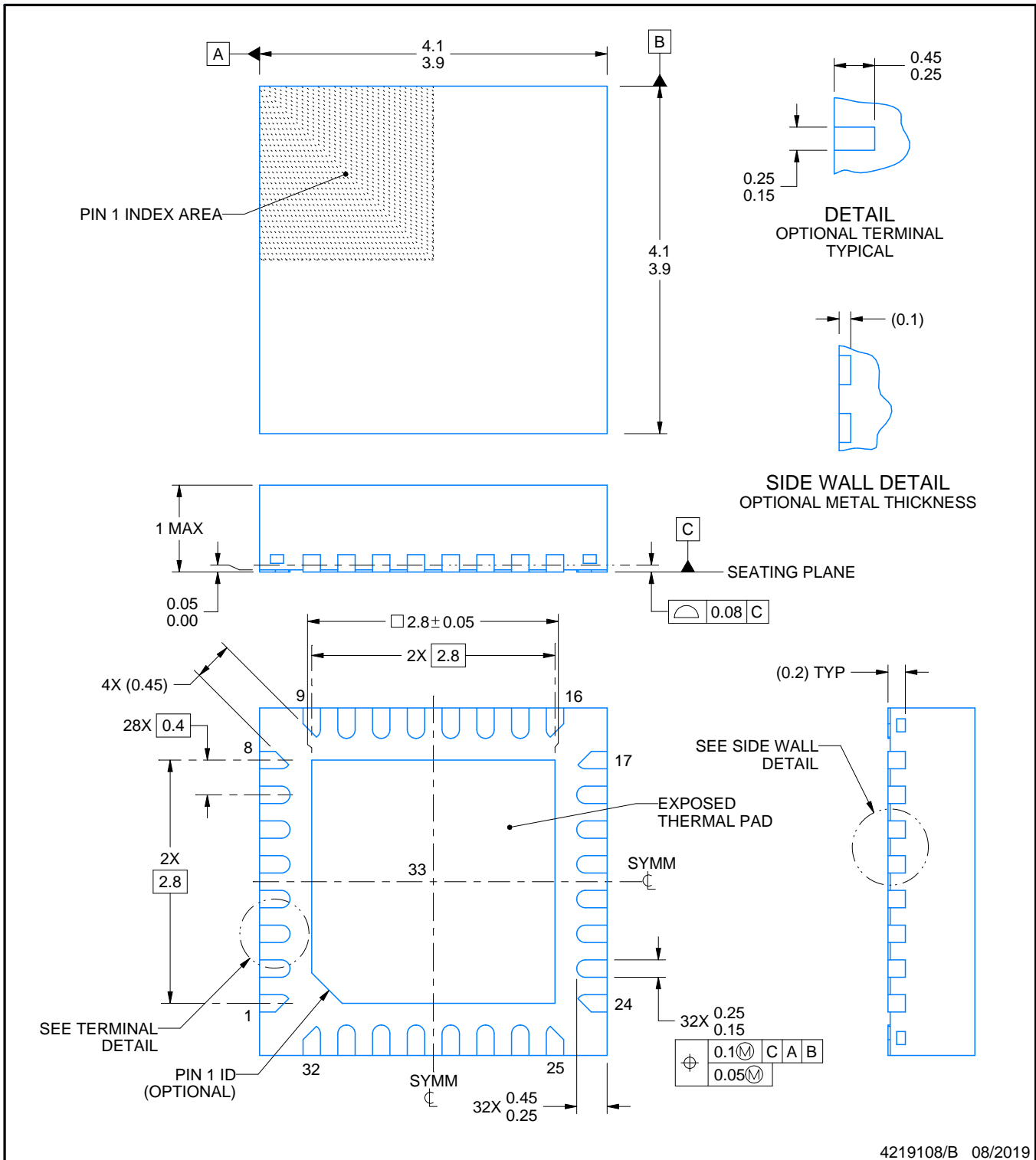
# RSM0032B



# PACKAGE OUTLINE

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219108/B 08/2019

### NOTES:

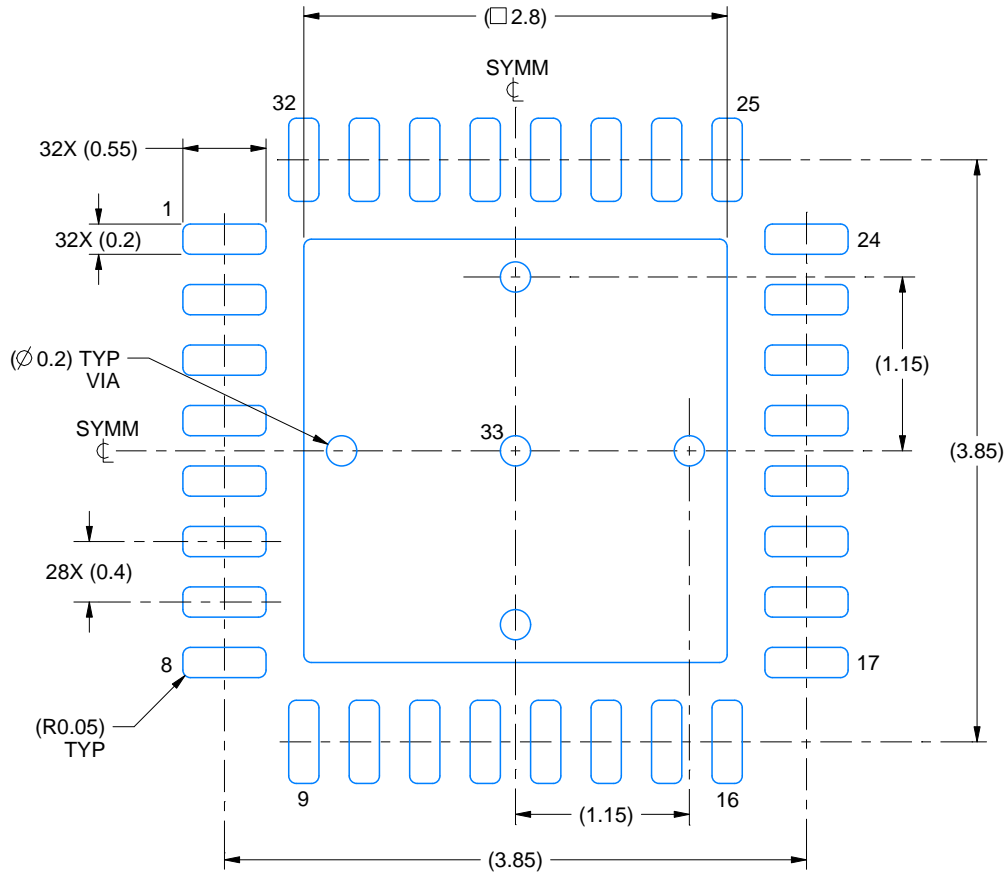
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

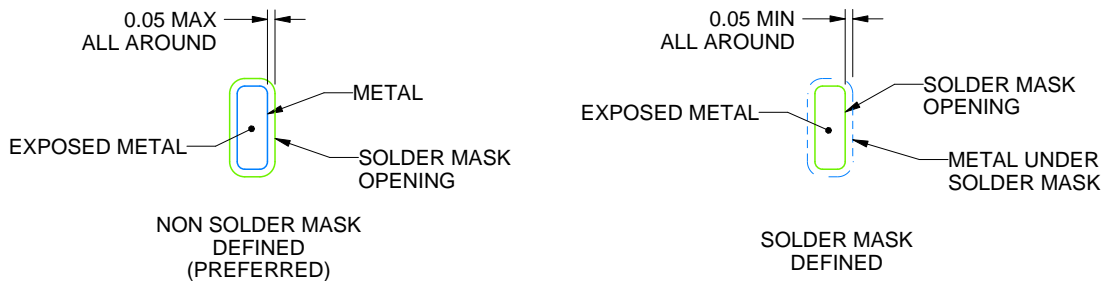
RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

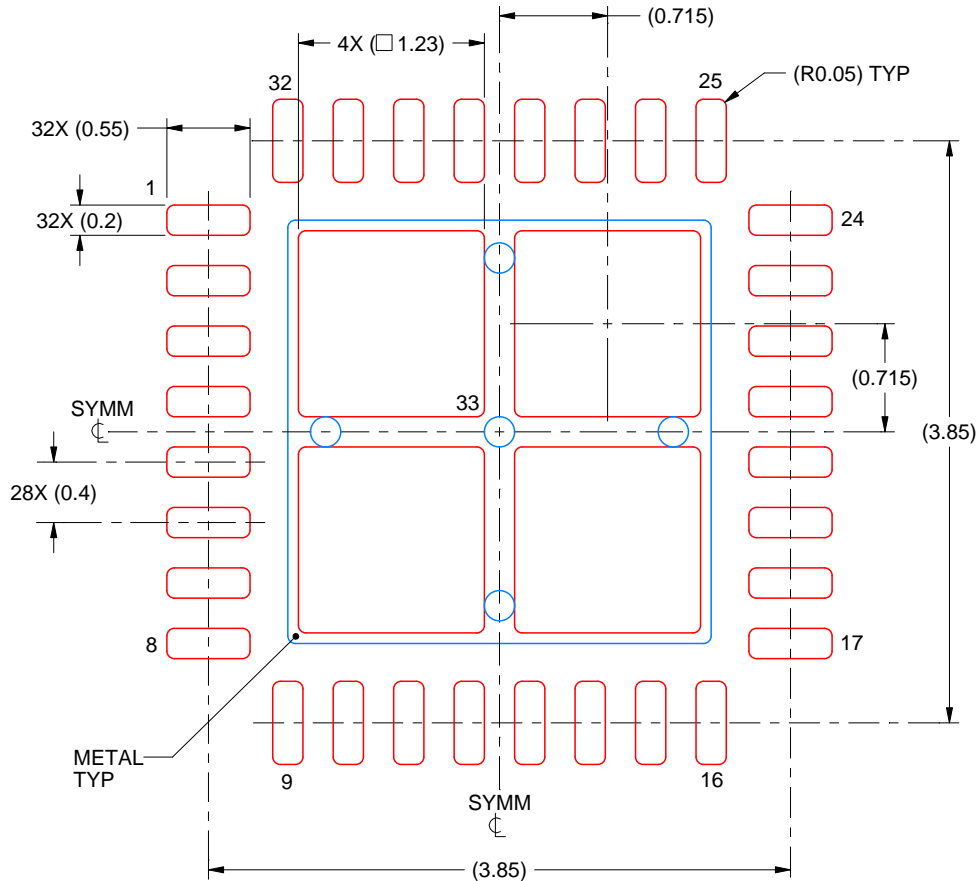
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:  
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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